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ORIGINAL RESEARCH PAPER

Design criteria of solid-state circuit breaker for low-voltage microgrids

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Abstract

Solid-state circuit breakers (SSCB) show great promise to become the key element in the protection of low-voltage direct current microgrids. SSCBs operate in the microsecond range and employ semi-conductor devices that have strict safe operation area limits. Therefore, the design of the SSCB needs to consider the effects of fault detection delays and semi-conductor safe operation area limitations. This paper derives SSCB design criteria that consider the effect of different detection methods with different detection delays under varying system constraints. The design space is investigated in a sensitivity analysis, which provides insights into the operation boundaries of SSCB and explains how a combination of fault detection methods can reduce the SSCB size. The insights from the theoretical and sensitivity analysis are used to propose an SSCB design flowchart. SSCB prototype is developed and tested in different scenarios under nominal grid voltage and current. The derived design constraints can be used for efficient SSCB design and also to evaluate the effects of different protection schemes on the required SSCB size.

1 | INTRODUCTION

As renewable energy sources are becoming cheaper and cost-competitive with coal, the electrical energy distribution needs to change accordingly to meet the needs of the emerging energy mix [1]. In the contemporary research, it is widely accepted that the direct current (dc)-based networks are the most suitable interface for the integration of large numbers of renewable energy sources, storage devices and electric vehicles [2–5]. The core advantages of low-voltage direct current (LVDC) compared to the alternating current (ac) networks are the increase in the system efficiency due to the reduced number of conversion steps, reduction of the material used due to high switching frequencies of the dc–dc converters and the straightforward integration of storage devices [4]. While LVDC networks are a promising concept, for large-scale adoption, the short-circuit protection and efficient power flow control must be addressed [5].

An example of an LVDC microgrid relying on solid-state protection is shown in Figure 1. The LVDC microgrid is connected to the medium voltage ac grid via a step-down transformer and active front-end (AFE) converter. As was argued in [6], the protection requirements can significantly influence the overall design of the grid converters. Using the solid-state circuit breaker (SSCB) on the low-voltage side to protect the substation is favourable compared to implementing the protection on the medium voltage side as the SSCBs do not have to be rated for high overvoltages. The houses are connected to the microgrid via SSCBs; the power flow in the grid can be controlled with power flow control converters such as [7]. Inside the house, several protection groups can be defined similarly as is done in the contemporary electric installations.

1.1 | LVDC microgrids protection challenges and requirements

The main goals of protection systems are detection, location and isolation of faults [2]. To successfully meet these three goals, knowledge about the system and its behaviour is necessary. The short-circuit protection of LVDC systems has several peculiarities compared to ac-based counterparts. The dc networks are usually highly capacitive and have comparably small inductances, as a result of using predominantly voltage source converters [8]. Consequently, in a low impedance-grounded LVDC system during the short-circuit fault, the short-circuit

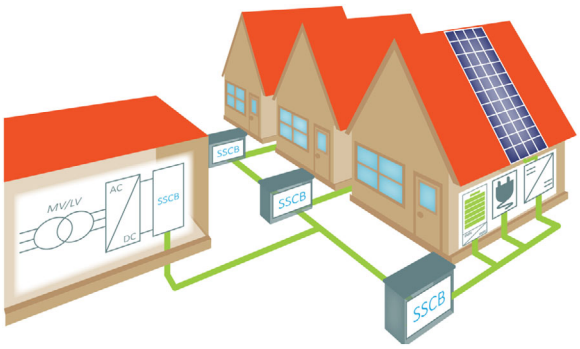

FIGURE 1 Direct current houses can be connected to the microgrid via SSCBs instead of fully rated dc/dc converters to make the system more efficient. The power flow in the grid can be controlled with power flow control converters [7]

current rises rapidly. The fast current rise can deplete the dc bus capacitors and cause blackout due to undervoltage. Therefore, systems as the one shown in Figure 1 require short-circuit ultra-fast detection systems. Otherwise, the system needs to be able to supply the short-circuit current for a prolonged period. Moreover, all components including cables, source converters and circuit breakers would need to be rated for higher short-circuit currents. The resulting oversizing would make the system less efficient and more expensive.

In [9], a simple short-circuit current calculation method based on the Laplace transform neglecting the node capacitor is proposed. A generalized approach, suitable for meshed dc systems, is presented in [10]. However, the matrices are not directly suitable for threshold selection. A model providing an insightful expression of the short-circuit currents was derived in [11], and another simple approach for LVDC was proposed in [9]. A unit-based protection was proposed for LVDC systems in [8] and [12]. The unit-based protection relies on communication and generally takes several milliseconds to detect a fault. While such delays are acceptable for high power systems, it is likely that in LVDC small power systems unit-based protection would have several unwanted consequences as discussed above. Therefore, approaches not relying on communications are more interesting for small dc systems like the one shown in Figure 1. Non-unit based protection using $\frac{di}{dt}$ was proposed in [13] and [14]. In both cases, the protection scheme is tested only with simulation and under the assumption of very high analog-to-digital conversion (ADC) sampling speeds, which increases the cost of the SSCB. Other non-unit based protection approaches rely on overcurrent or undervoltage threshold [15, 16]. Combination with external circuitry that can inject known frequency to detect high impedance faults is proposed in [17]. However, the reported works do not consider the effect of the detection methods on the design of the protection devices and validate the results with simulation studies.

1.2 | Circuit breakers for LVDC microgrids

While on the system level, the research is focused on coordination and selectivity in complex network topologies, on the device level, two main research areas can be identified: hybrid circuit breakers (HCB) [18] and SSCBs [19, 20]. The main advantage of the HCBs are the small on-state losses; one of the main HCBs limitations is the reliability of the mechanical part caused by the mechanical contact erosion [18]. The HCBs open short-circuits in the range of milliseconds, which is significantly faster than the traditional circuit breakers. However, for low-power microgrids with small nominal operating currents, the fault clearing periods in the range of milliseconds are not acceptable [21, 22]. Therefore, for small dc nanogrids or microgrids, fast SSCBs are preferred [23].

One of the main challenges regarding the use of the SSCBs are the on-state losses [4, 24]. A popular choice for SSCBs are Si insulated gate bipolar transistor (IGBTs) [19] and less often Si or silicon carbide (SiC) MOSFETs [23]. Integrated gate-commutated thyristor (IGCT)-based solutions prove to be more efficient in systems with a nominal current in the range of kA [25]. Si MOSFETs have limited minimum voltage breakdown amplitude compared to the Si IGBTs. Moreover, Si IGBTs are more robust in terms of power dissipation capability and short-circuit withstand capability. However, in the case of SSCB, the conduction losses are of paramount importance. In MOSFETs, they are defined by a classical resistance; in IGBTs, there is a fixed conduction loss determinator in the form of a knee voltage plus a differential resistance of the output characteristic. Therefore, the conduction losses of an SSCB based on MOSFETs can be reduced almost arbitrarily by paralleling of MOSFETs. However, when IGBTs are used the conduction loss limit remains at the knee voltage regardless of the number of devices used. This key difference can have paramount influence especially for smaller nominal currents, for example, tens of amperes. The use of MOSFETs can improve the efficiency of the SSCB in terms of energy and cost in systems with smaller operating voltages and currents [23]. The emerging SiC field-effect transistor (FETs) are a promising technology for the use in SSCB. However, they are likely to suffer the highest short-circuit current relative to their chip size due to the intrinsic properties of the SiC BJT [26, 27]. Therefore, the short-circuit detection time is very crucial when SiC MOSFETs are used in SSCB. Furthermore, the higher the short-circuit current, the higher the voltage spike after the opening of the SSCB; as a result, snubber circuits size becomes significant [28]. Different overvoltage snubbers are described in [19].

Previous research in SSCB focused on the development of autonomous and cost-efficient topologies [29] and extra functionalities [30, 31]. In [29], the design of a cost-efficient solution-based SiC JFET is investigated. The main advantage is the combination of a detection circuit with an auxiliary power circuit, which enables self-powering of the SSCB during the fault. The circuit from [29] was studied to increase its blocking voltage capability in [32] and to increase its current carrying capability in [33]. For systems with high nominal currents novel topologies that introduce fault current limiting is investigated [20, 34]. The fault location functionality can be added to SSCB using current injection at a known frequency [35, 36]. However, the proposed fault location techniques introduce more components and make the clearing process longer.

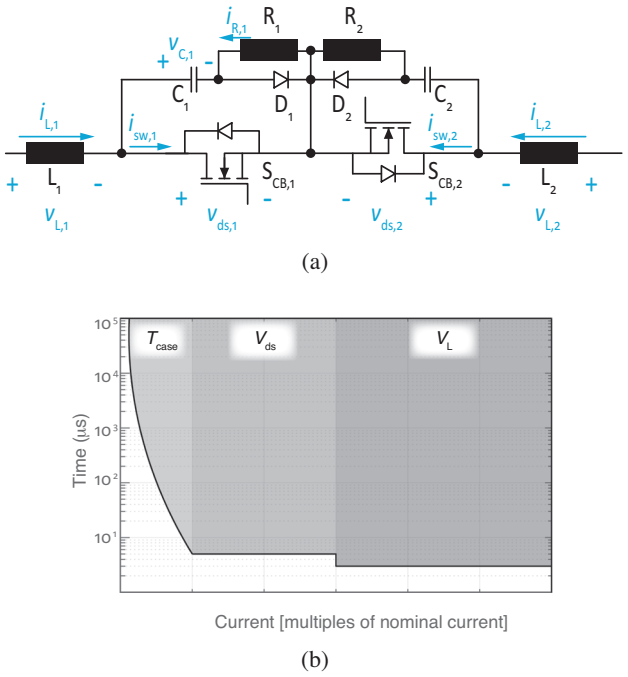

FIGURE 2 SSCB topology is shown in (a), and in (b) the current–time characteristics with the type of short-circuit detection is shown

1.3 | Studied SSCB and contribution

As discussed above the Si and especially SiC-based devices are sensitive to overcurrent and overvoltage. Therefore, the design of the short-circuit detection must ensure that the SSCB always meets the system requirements, ensure that the SSCB always operates within its safe operating area and meets the cost criteria. The SSCB topology used in this study is in Figure 2(a), with three distinct short-circuit detection mechanisms. The slowest mechanism is thermal protection which is also used in today's electromechanical circuit breakers. The faster protection during short-circuits is provided by the overcurrent detection and a complementary rate of change of current (ROCOC) detection. The role of the overcurrent detection is to detect short-circuits that are further away from the SSCB and are characterized by higher fault inductance. The overcurrent detection is implemented via drain-source voltage measurement. The drain-source voltage monitoring was chosen as this method does not introduce any further losses and does not have a tight bandwidth limit. However, when the short-circuit occurs at the terminals of the SSCB, use of overcurrent detection only can result in the destruction of SiC switches. Therefore, a complementary ROCOC detection is implemented, that improves the SSCB performance in the cases with no external inductance.

The main contributions of this paper are the derivation of the design criteria of SSCB for LVDC grid that take into consideration the effects of different short-circuit detection methods, sensitivity analysis of SSCB design space and development of an SSCB prototype. The design space of the SSCB is analyzed in a sensitivity study that is based on the review of LVDC microgrid requirements and highlights the limits and potential of SiC MOSFET-based SSCBs. The insights from the sensitivity analysis and the derived designed criteria are used to develop an SSCB design flowchart. Using the developed design guide, a prototype SSCB is designed and developed. The SSCB prototype ability to effectively interrupt short-circuits with minimal delay time is validated in experiments with varying loop inductance. The SSCB prototype ability to avoid spurious tripping during large load steps is also validated. The experiments are not scaled down, that is, the experiments are done at nominal grid voltage and current levels.

1.4 | Organization

The rest of the paper is organized as follows. Section 2 investigates the SSCB operation and derives the design criteria. Section 3 contains a sensitivity analysis of the SSCB design space, highlighting the effect of different detection methods and detection delay time. Section 3 ends with a proposed SSCB design flowchart and an elaboration on the design procedure. Section 4 presents experimental results. Section 5 closes the paper with a summary and an outlook on future work.

2 | SSCB OPERATION ANALYSIS

The line-to-ground fault and line-to-line fault are the two main types of short-circuiting. The line-to-ground fault is formed when either the positive or negative phase touches the ground, while the line-to-line fault occurs when a low impedance connection between the phases of the system is formed. In the case of low resistance grounded systems, both faults have similar behaviour that is characterized by the large currents and fast $\frac{di}{dt}$; therefore both can be approximated by the bolted fault [37].

2.1 | SSCB operation analysis

The operation of the SSCB during a bolted fault can be divided into three distinct stages as shown in Figure 3. In the operation analysis, it is assumed that the capacitance of the short-circuit current source is sufficiently large and during the short-circuit, it appears as an ideal voltage source V_{DC}, the short-circuit current is characterized by the inductance between the source and the loop L_{total} and by the fault impedance R_{SC} (for bolted fault $R_{SC} \to 0$). The loop inductance L_{total} is a sum of the SSCB current limiting inductances L_1, L_2 and any additional inductance present in the loop $L_{ext.}$. The parasitic line capacitance in the LVDC systems is in general very low and is neglected.

Figure 3 shows that after the fault occurs in Stage 1 the current flows through the SSCB MOSFETs. Stage 1 is bounded by the time of the fault $t_{ft} = 0$ and turn-off of the SSCB MOSFETs t_{tr}. In the first stage, the circuit is described by a first-order differential equation

$$L_{total}\frac{d}{dt}i_{L,1}(t) = V_{DC} - \underbrace{R_{SC}i_{L,1}(t)}_{V_{SC}\to 0}, \quad (1)$$

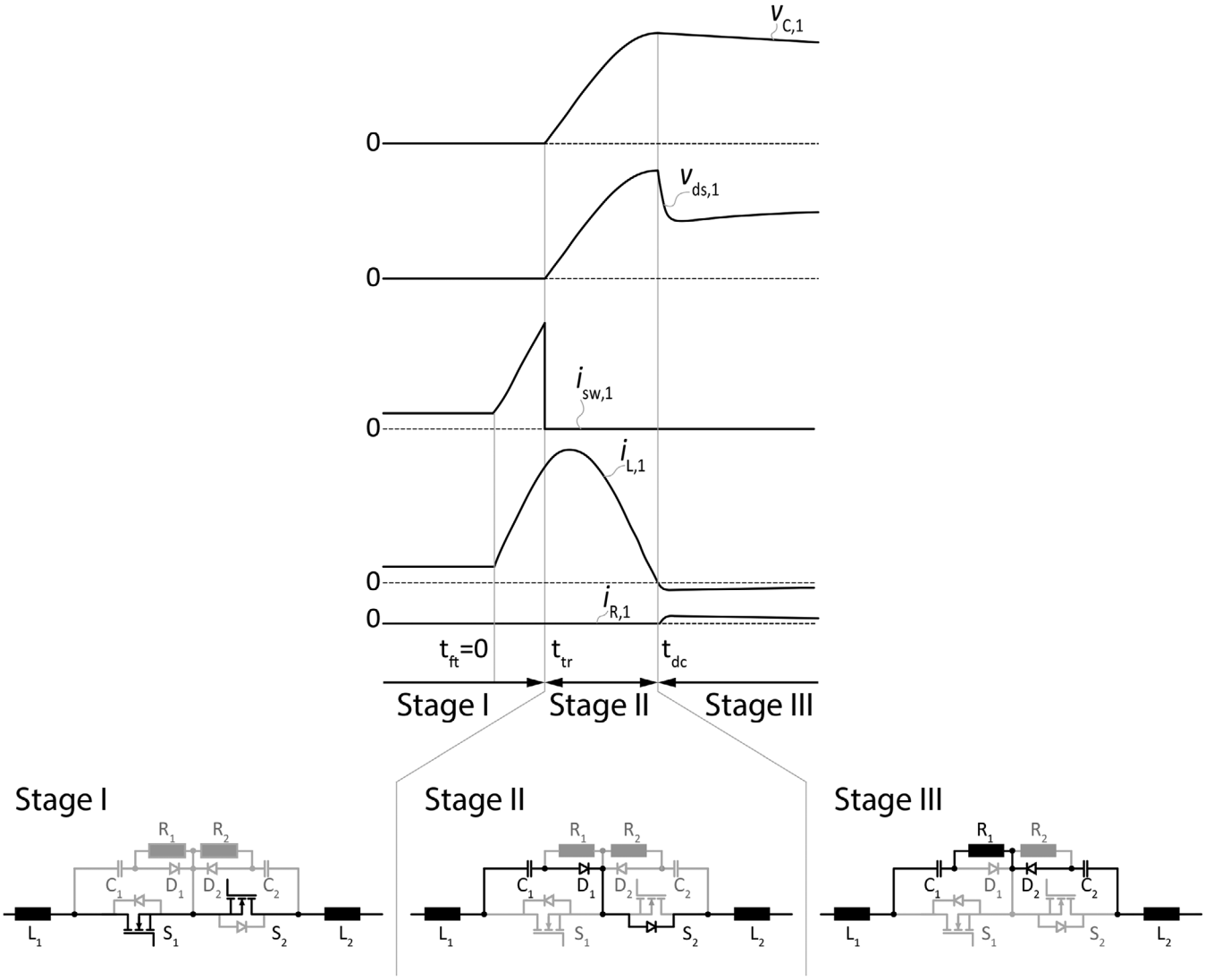

FIGURE 3 SSCB operation during the fault clearing. Stage 1 starts after the fault occurrence and the circuit is dominated by the inductance. Stage 2 starts after the SSCB MOSFETs are opened and is characterized by charging of the snubber capacitor. The last stage is the discharge of the snubber capacitor

where $i_{\mathrm{L},1}$ is the current through the inductor and equals the short-circuit current. The voltage across the capacitor C_1 in the first stage is assumed to be

$$v_{\mathrm{C},1} = v_{\mathrm{ds},1} \approx 0. \tag{2}$$

The solution of the first-order system in the time domain is

$$i_{\mathrm{L},1}(t) = I_{\mathrm{L},0} + \frac{V_{\mathrm{DC}}}{L_{\mathrm{total}}} t, \tag{3}$$

where $I_{\mathrm{L},1}(0) = i_{\mathrm{L},1}(t_{\mathrm{ft}})$ is the current at the time of the fault occurrence.

After the short-circuit passes the defined threshold, the SSCB turns-off the MOSFETs and Stage 2 starts. Stage 2 is bounded by the turn-off of the SSCB MOSFETs t_{tr} and the time when the snubber capacitor starts to discharge into the snubber resistor t_{dc}. As shown in Figure 3, the current commutes to the snubber diode and starts charging the snubber capacitor C_1. In the analysis, it is assumed that the diode is ideal and the commutation from MOSFET to snubber diode is instant. The circuit is described by two differential equations

$$L_{\mathrm{total}} \frac{d}{dt} i_{\mathrm{L},1}(t) = V_{\mathrm{DC}} - v_{\mathrm{C},1}(t) - \underbrace{R_{\mathrm{SC}} i_{\mathrm{SC}}(t)}_{V_{\mathrm{SC}} \to 0}, \tag{4}$$

$$C_1 \frac{d}{dt} v_{\mathrm{C},1} = i_{\mathrm{L},1}(t). \tag{5}$$

Moreover, the initial conditions are

$$\begin{aligned} i_{\mathrm{L},1}(t = t_{\mathrm{tr}}) &= I_{\mathrm{L},0} + \frac{V_{\mathrm{DC}}}{L_{\mathrm{total}}} t_{\mathrm{tr}}, \\ v_{\mathrm{C},1}(t = t_{\mathrm{tr}}) &= 0. \end{aligned} \tag{6}$$

The current and voltage are a solution of the second-order system (4)–(5) and are

$$i_{\mathrm{L},1}(t) = A\cos\left(\omega(t - t_{\mathrm{tr}}) + \varphi_1\right), \tag{7}$$

$$v_{\mathrm{C},1}(t) = B\sin\left(\omega(t - t_{\mathrm{tr}}) + \varphi_1\right) + V_{\mathrm{DC}}, \tag{8}$$

where

$$A = \sqrt{\left(I_{\mathrm{L},0} + \frac{V_{\mathrm{DC}}}{L_{\mathrm{total}}}t_{\mathrm{tr}}\right)^2 + \frac{C_1}{L_{\mathrm{total}}}V_{\mathrm{DC}}^2},$$

$$B = \sqrt{\frac{L_{\mathrm{total}}\left(I_{\mathrm{L},0} + \frac{V_{\mathrm{DC}}}{L_{\mathrm{total}}}t_{\mathrm{tr}}\right)^2}{C_1} + V_{\mathrm{DC}}^2},$$

$$\omega = \frac{1}{\sqrt{L_{\mathrm{total}}C_1}},$$

$$\varphi_1 = -\arcsin\left(\sqrt{\frac{1}{1 + \frac{\left(I_{\mathrm{L},0} + \frac{V_{\mathrm{DC}}}{L_{\mathrm{total}}}t_{\mathrm{tr}}\right)^2}{\omega^2 C_1^2 V_{\mathrm{DC}}^2}}}\right). \tag{9}$$

During Stage 3, the snubber capacitor is discharged via the snubber resistor, thus $v_{\mathrm{C},1}$ will decrease and $i_{\mathrm{L},1}$ will also be very small due to the snubber resistor dumping. Therefore, Stage 3 is omitted in the analysis.

2.2 | Design constraints

Different detection methods have different time delays and influence design parameters. The main parameters of interest are the peak values of the short-circuit current, the peak overvoltage on the blocking MOSFET of the SSCB and the total fault clearing time.

2.2.1 | Overcurrent detection

It uses threshold of the current $I_{\mathrm{th.}}$ to detect fault. Once the measured current reaches the threshold, the MOSFET is turned off. However, in reality, there is always a delay T_d between the time the current reaches the threshold and the time the MOSFETs open t_{tr}. The delay effect can be taken into account by rewriting (3)

$$\underbrace{i_{\mathrm{L},1}(t_{\mathrm{tr}})}_{I_{\mathrm{th.}}} = I_{\mathrm{L},0} + \frac{V_{\mathrm{DC}}}{L_{\mathrm{total}}}t_{\mathrm{tr}}, \tag{10}$$

and the actual time of SSCB MOSFET turn-off can be obtained from

$$t_{\mathrm{tr}} = T_d + \frac{L_{\mathrm{total}}}{V_{\mathrm{DC}}}\left(I_{\mathrm{th.}} - I_{\mathrm{L},0}\right), \tag{11}$$

then the current at the trip time is

$$i_{\mathrm{L},1}(t_{\mathrm{tr}}) = I_{\mathrm{th.}} + \frac{V_{\mathrm{DC}}}{L_{\mathrm{total}}}T_d. \tag{12}$$

The time when the peak voltage is reached is the time when current passes zero for the first time can be found by investigating equation (7) and is

$$t_{dc} = t_{\mathrm{tr}} + \frac{1}{\omega}\left(\frac{\pi}{2} + \varphi_1\right). \tag{13}$$

During the short-circuit, surge energy is supplied. This energy can be dissipated in components both in the SSCB and in the faulted system. Thus, it is directly proportional to the self-hating of the system and system components during the fault. The energy that is dissipated during the fault is defined as

$$E_{\mathrm{sg}} = r\int_{t_{\mathrm{ft}}}^{t_{\mathrm{dc}}} i_{\mathrm{L},1}^2(\tau)dt, \tag{14}$$

where r is a system-dependent parameter; it represents the equivalent resistance of the line and the line components. This parameter can be used as an abstract measure of the distance of the fault (or line length), as was done for example in [38]. The inductor current is chosen for the definition, as this current flows through the system, the semi-conductors and the overvoltage surpassing circuit for the entire duration of the fault. Since r is component-specific, the design constraint can be obtained as a surge energy index, defined as

$$E_{\mathrm{ds}} = \frac{E_{\mathrm{sg}}}{r} = \int_{t_{\mathrm{ft}}}^{t_{\mathrm{dc}}} i_{\mathrm{L},1}^2(\tau)dt = \int_0^{t_{\mathrm{tr}}} i_{\mathrm{L},1}^2(\tau)dt + \int_{t_{\mathrm{tr}}}^{t_{\mathrm{dc}}} i_{\mathrm{L},1}^2(\tau)dt. \tag{15}$$

Substituting (13), (11) and (12) into (15) the energy index is obtained as

$$E_{\mathrm{ds}} = \frac{I_{\mathrm{th.}}^2\tau_{\mathrm{SSCB}}}{k_1^2}\left(\frac{k^3}{3} + \frac{\pi}{4}\left(1 + k^2\right) + \frac{1}{2}\left(1 + k^2\right)\arctan\left(\frac{1}{k}\right) - \frac{k}{2}\frac{\left(3k^2 - 1\right)}{1 + k^2}\right), \tag{16}$$

where

$$\tau_{\mathrm{SSCB}} = \sqrt{L_{\mathrm{total}}C_1}, \tag{17}$$

$$k_1 = \frac{Z_{\mathrm{SSCB}}}{Z_{\mathrm{sys}}} = \frac{L_{\mathrm{total}}}{C_1}\frac{I_{\mathrm{th.}}}{V_{\mathrm{DC}}}, \tag{18}$$

$$k_2 = \frac{T_d}{\tau_{\mathrm{SSCB}}} = \frac{T_d}{\sqrt{L_{\mathrm{total}}C_1}}, \tag{19}$$

$$k = k_1 + k_2. \tag{20}$$

TABLE 1 Governing design constraints of solid-state circuit breaker for LVDC grid protection

Design constraint	Overcurrent detection	ROCOC detection
Maximum voltage	$V_{DC}\sqrt{1+k^2}+V_{DC}$	$V_{DC}\sqrt{1+k_0^2}+V_{DC}$
Maximum current	$I_{th.}\frac{\sqrt{1+k^2}}{k_1}$	$\frac{I_{th.}}{k_1}\sqrt{1+k_0^2}$
Energy index	$\frac{I_{th.}^2\tau_{SSCB}}{k_1^2}\left(\frac{k^3}{3}+\frac{\pi}{4}(1+k^2)+\frac{1}{2}(1+k^2)\arctan\left(\frac{1}{k}\right)-\frac{k}{2}\frac{(3k^2-1)}{1+k^2}\right)$	$\frac{I_{th.}^2\tau_{SSCB}}{k_1^2}\left(\frac{1}{3}k_0^3+\frac{\pi}{4}\left(1+k_0^2\right)+\frac{1}{2}\left(1+k_0^2\right)\arctan\left(\frac{1}{k_0}\right)-\frac{k_0}{2}\frac{\left(3k_0^2-1\right)}{1+k_0^2}\right)$
Discharge time	$T_d+\frac{L_{total}}{V_{DC}}(I_{th.}-I_{L,0})+\frac{1}{\omega}\left(\frac{\pi}{2}+\varphi_1\right)$	$T_d+\frac{1}{\omega}\left(\frac{\pi}{2}+\varphi_1\right)$

The peak voltage for the overcurrent detection can be rewritten using (18)–(20) as

$$V_{C,1,max}=V_{ds,1,max}=V_{DC}\sqrt{1+k^2}+V_{DC}. \tag{21}$$

The maximum current can be found by substituting (12) into (7), and written using (18)–(20) as

$$I_{L,1,max}=I_{th.}\frac{\sqrt{1+k^2}}{k_1}. \tag{22}$$

2.2.2 | ROCOC detection

It is implemented by measuring the voltage drop $v_{L,1}$ on L_1. The peak voltage, peak current and surge energy constraints are different for this detection method compared to the threshold current detection. The condition for tripping of the detection is

$$v_{L,1}(t=t_{ft})=V_{dc}\frac{L_1}{L_{total}}\geq V_{L,th}. \tag{23}$$

The condition for tripping of the rate of change current detection expressed in (23) does not require the current to rise to $I_{th.}$ instead it is tripped when the current is $I_{L,0}$. However, the detection circuit still introduces delay T_d, which is considered. Therefore, in the equations for the ROCOC detection the threshold current is replaced with $I_{L,0}$. The time when the capacitor discharge starts can be then written as

$$t_{dc}=T_d+\frac{1}{\omega}\left(\frac{\pi}{2}+\varphi_1\right). \tag{24}$$

The surge energy index can be defined as

$$E_{ds}=\frac{I_{th.}^2\tau_{SSCB}}{k_1^2}\left(\frac{1}{3}k_0^3+\frac{\pi}{4}\left(1+k_0^2\right)+\frac{1}{2}\left(1+k_0^2\right)\arctan\left(\frac{1}{k_0}\right)-\frac{k_0}{2}\frac{\left(3k_0^2-1\right)}{1+k_0^2}\right), \tag{25}$$

where

$$k_0=\frac{I_{L,0}}{I_{th.}}k_1+k_2. \tag{26}$$

TABLE 2 Sensitivity analysis parameters

Parameter	Acronym	Value
Voltage	V_{DC}	350 [V]
Initial current	$I_{L,0}$	8 [A]
Threshold current	$I_{th.}$	32 [A]

The peak voltage can be then written as

$$V_{C,1,max}=V_{ds,1,max}=V_{DC}\sqrt{1+k_0^2}+V_{DC}. \tag{27}$$

The peak current that will be reached when ROCOC detection is used is

$$I_{L,1,max}=\frac{I_{th.}}{k_1}\sqrt{1+k_0^2}. \tag{28}$$

The above mentioned design constraints are summarized in Table 1

3 | DESIGN SENSITIVITY ANALYSIS

In the previous section, SSCBs operation stages and design constraints that takes into account the difference between the applied detection methods were described. This section provides a sensitivity analysis of the design space and design constraints. The parameters used in the sensitivity analysis are summarized in Table 2.

In the following analysis, the influence of the system on the SSCB operation is considered with the total inductance of the circuit. The current threshold values for which the SSCB needs to be rated can be calculated using IEC61660 standard. The influence of the meshed topology can be taken into account using a matrix approach presented in [10, 39]. The SSCB needs to be rated to be capable of carrying the short-circuit currents and open them at given maximum inductance of the circuit. Similarly, the SSCB must be able to interrupt extremely fast-rising current at minimum inductance. The grid sources are assumed to behave as ideal voltage sources, as the operation of SSCB is in range of μs. The size of the fault inductance can be considered as a measure of fault distance, as the fault inductance increases with the fault distance from the SSCB.

A crucial design parameter for the SSCB design is the maximum voltage that appears across the blocking MOSFET after

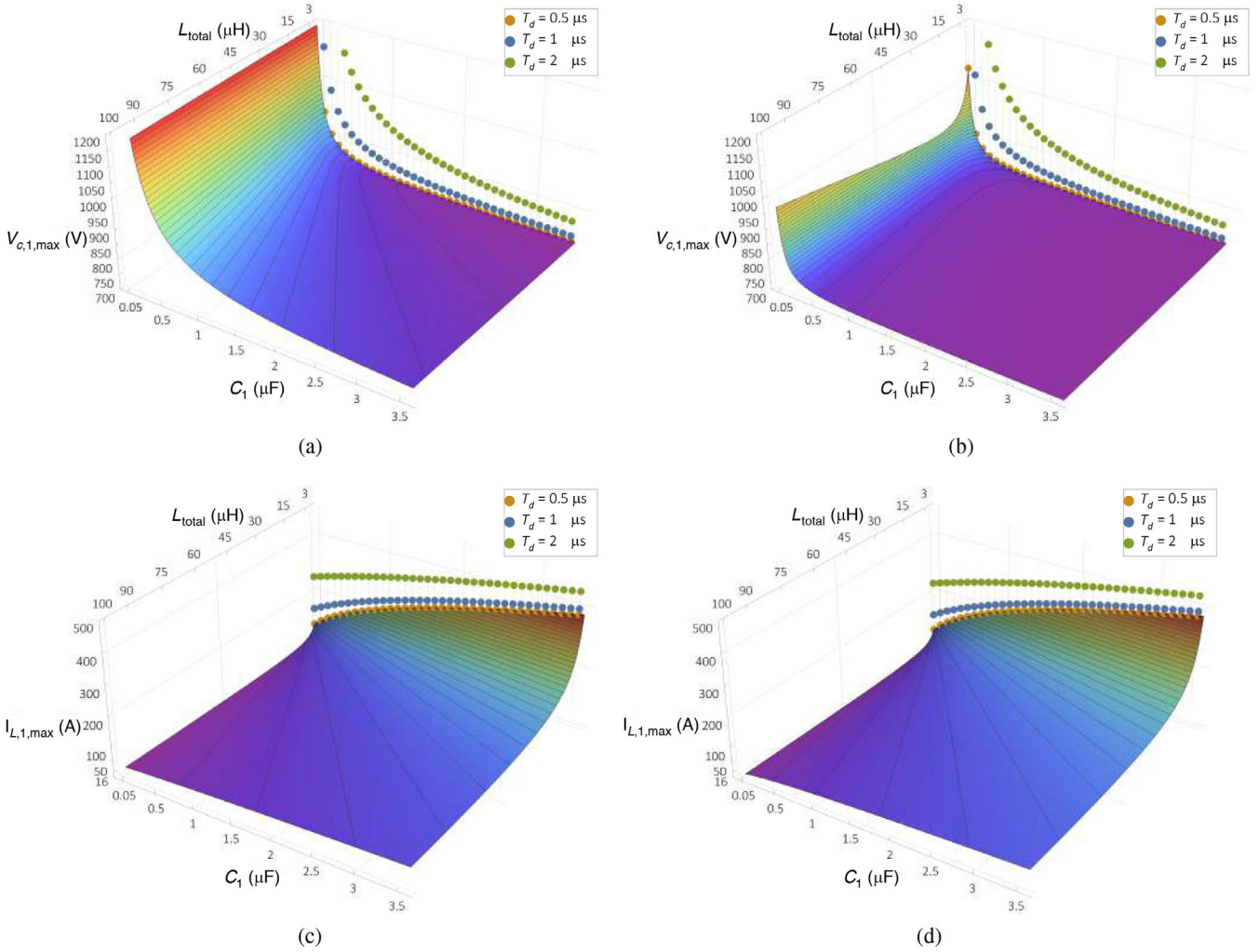

FIGURE 4 Peak current and voltage as a function L_{total} and C_1. In (a) is the peak voltage when overcurrent detection is used and in (b) is the peak voltage when ROCOC detection is used. Panels (c) and (d) show the peak current when overcurrent detection and ROCOC detection are tripped, respectively

the opening of the faulted circuit. Figure 4 shows the peak voltage that is reached during the clearing process for both overcurrent and ROCOC detection method. By comparing Figures 4(a) and (b), it is clear that the overcurrent detection method results in overvoltages above 800 V for all values of the total loop inductance when the snubber capacitor is smaller than 1 μF. However, the ROCOC detection is capable of limiting the overvoltages for minimal loop inductances even with snubber capacitance less than 500 nF.

The effect of increased detection delay T_d can be studied in Figures 5 and 7. Figure 5 shows the effect of changing detection delay when L_{total} is fixed at 3 μH. For both methods, it can be observed that the longer the delay, the higher are the resulting overvoltages. Moreover, with the increased capacitor size, the difference caused by the delay diminishes as well as the difference between the detection methods. When the loop inductance is minimal, the ROCOC detection effectively reduces the maximum voltages provided that the detection delay is within 1 μs. A detailed switching model of LTSpice using SiC MOSFETs is used to confirm the analysis of the detection delay. In Figure 6 are shown the simulation results when the overcurrent detection is used and L_{total} is fixed at 3 μH and C_1 is fixed at 0.05 μF. Observing the overvoltage in Figure 6(a) that would potentially appear on the blocking MOSFET the simulation and analysis results match. It is observed, that the MOSFET would most likely undergo a catastrophic breakdown if the delay is 2 μs. It is interesting, however, to observe a slight difference in the peak fault current in Figure 6(b). The results match when the delay is shorter than 2 μs. For longer delay times, the dependence of the switch on-resistance on the drain current influences the results. The on-resistance of the MOSFET increases with the drain current and the switch dissipates more energy. This effect can potentially reduce the peak fault currents, however, the MOSFET can undergo a thermal runaway if the dissipated energy is too high.

Figure 7 shows the effect of different detection delay times when the loop inductance is fixed at 100 μH. For very large loop inductance, the ROCOC detection is never activated as the current change is very slow. Therefore, the results for ROCOC are not shown. Figure 7 shows that even though the peak current is very low, the maximum voltage is very high. For highly inductive faults reducing the detection delay is ineffective and

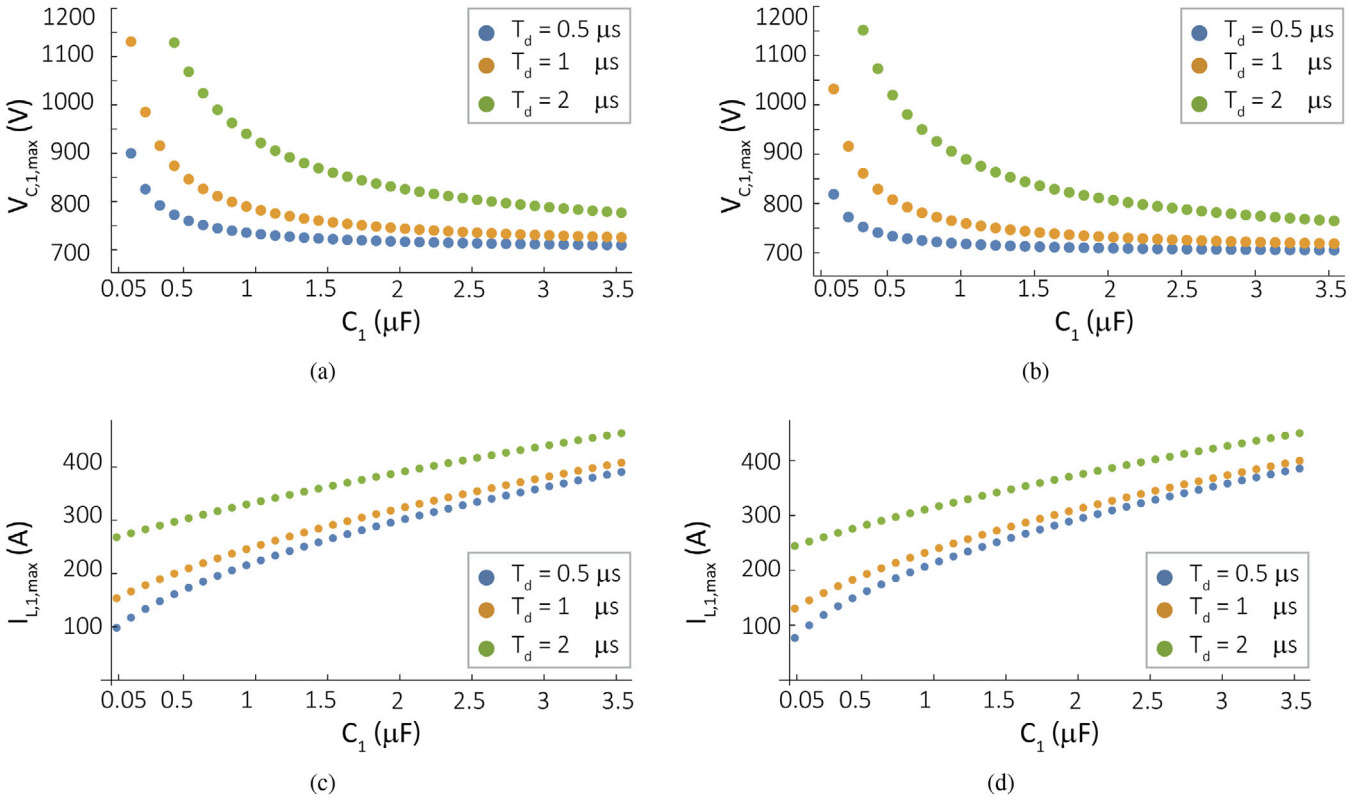

FIGURE 5 Peak current and voltage as a function of C_1 for different detection delay times T_d, when L_{total} is fixed at 3 μH. In (a) is the peak voltage when overcurrent detection is used and in (b) are the peak voltages when ROCOC detection is used. Panels (c) and (d) show the peak currents when overcurrent detection and ROCOC detection are tripped, respectively

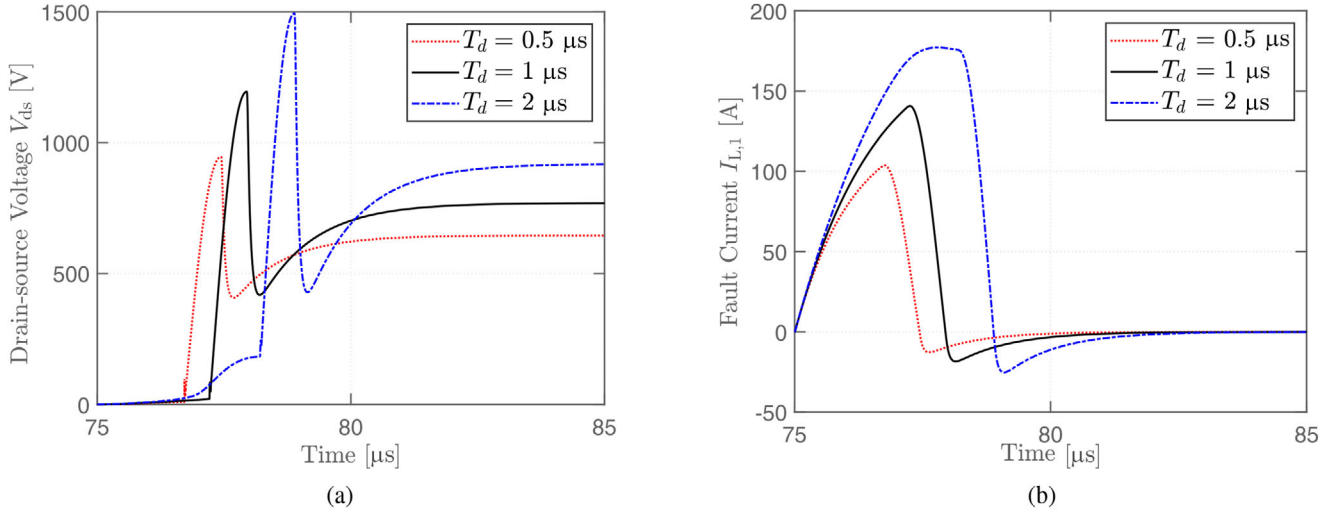

FIGURE 6 LTSpice simulation detailing the effect of the detection delay on the maximum short-circuit current and peak voltage. In (a) is the drain-source voltage on the blocking MOSFET and in (b) is the short-circuit current

only increasing the size of the snubber capacitor can limit the maximum voltage.

The snubber capacitance should not be oversized as it directly increases the maximum value of current flowing in the circuit during short-circuit as is visible in Figures 4(c) and (d). From figures, it is also visible that for both methods for substantial capacitor sizes, the difference caused by different delay times is diminished. This effect can be explained by the fact that the clearing process is dominated by Stage 2, that is, the stage bounded by the time of MOSFET turn-off t_{tr} and time t_{dc} at which the short-circuit current crosses zero for the first time. The influence of different detection delays, however, is

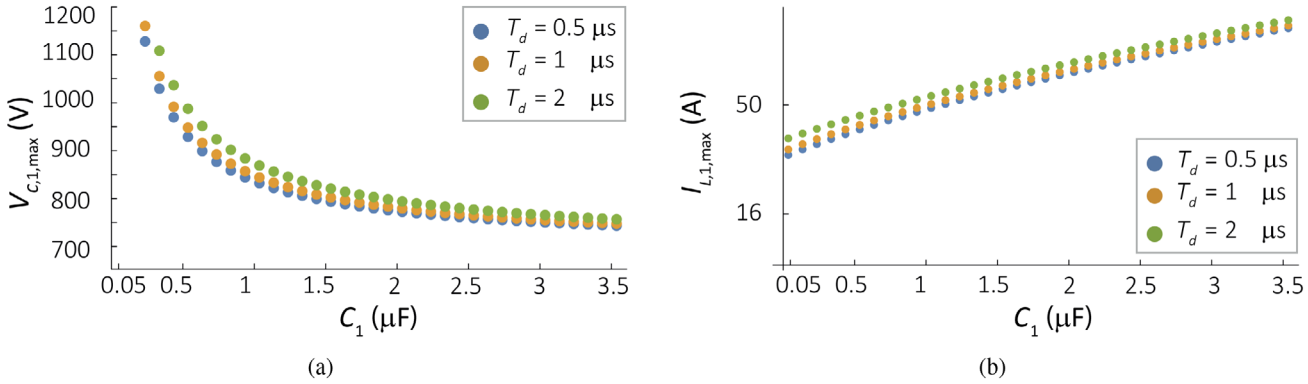

FIGURE 7 Peak current and voltage as a function of C_1 for different overcurrent detection delay times T_d, when L_{total} is fixed at 100 μH. In (a) is the peak voltage when overcurrent detection is used and in (b) are the peak currents

very strong for small snubber capacitors as can be seen in both Figures 4(c) and (d). The influence of the detection delay is stronger for ROCOC detection, which can limit the short-circuit current peak below 100 amperes for snubber capacitors smaller than 500 nF. The detail of the influence of different detection delays is shown in Figure 5. Comparing peak currents in Figures 5(c) and (d), it is clear that fast ROCOC detection is capable of limiting the peak currents better than slower overcurrent detection when the circuit has minimal self-inductance inductance.

The increase of time t_{dc} and energy index E_{ds} caused by the increase of the snubber capacitor is further illustrated in Figure 8. As is visible oversizing of the snubber capacitor results in a significant increase of the energy index, especially for minimal loop inductance. This can be explained by the fact that when the loop inductance is small, the current rises very fast, the large snubber capacitor causes prolongation of the entire clearing time, and that results in the high energy index. Further insights about clearing time can be gain by observing Figures 8(c) and (d). It is clear that the total clearing time is longer for overcurrent detection, and the difference is becoming more evident as the inductance of the circuit is increased. However, for large loop inductance, the ROCOC detection will not be activated as the current rise would be too small.

From the above discussion, it can be concluded that the overcurrent detection and the ROCOC can complement each other. The ROCOC detection is viable to reduce the voltage stress when the loop inductance is minimal, thus minimizing the requirement on the snubber capacitor. The overcurrent detection is viable when the current rise is slower, and the ROCOC detection is not activated. Furthermore, it can be concluded that the SSCB must specify the maximum loop inductance it can safely open as the overvoltages can be very high even when the short-circuit currents are relatively small.

3.1 | Effect of switch parasitics

The SSCBs peak current amplitude and its duration are limited by the semi-conductor junction temperature. The peak voltage is limited by the semi-conductor minimum breakdown voltage. The influence of the non-ideal behaviour of the devices on the peak voltage across the blocking semi-conductor and the peak inductor current has three common parasitic sources: drain-source capacitance, drain path inductance and source path inductance.

Typical values of the drain-source capacitance of SiC MOSFETs are in the range of hundreds of picofarads. From the sensitivity analysis, it can be observed that practical snubber capacitances C_1 and C_2 are several hundred up to thousands of times larger than the parasitic capacitance. Therefore, the influence of the drain-source capacitance on the peak values will be minimal. The parasitic inductances occur in the drain and the source path and tend to influence high-speed switching circuits. If the parasitic inductances are not limited, they can have a harmful influence on the switching behaviour of the employed MOSFETs. However, in the case of SSCB, these parasitic inductances will have a relatively small influence on the peak fault current and peak overvoltage. The sensitivity analysis shows that practical minimum values of limiting inductances that are part of the SSCB start at hundreds of nH. This value is significantly higher than the parasitic inductance of any semi-conductor package.

The operation of MOSFETs, in general, is influenced by the junction temperature. One of the well-known impacts of varying junction temperature is the rise of drain-source on resistance and restriction of the safe-operating area of the semiconductor. The change of the drain-source resistance over a temperature range is not linear. The variation of on-resistance should be taken into account when using drain-source voltage as a fault indicator. During the fault clearing, the difference of on-resistance on its own is not significant enough to notably influence the peak fault current or the overvoltage after interruption of the fault current.

3.2 | SSCB design

Insights and observations from the previous sections are transformed into an SSCB design flowchart shown in Figure 9. The design inputs specify the operation voltage band and

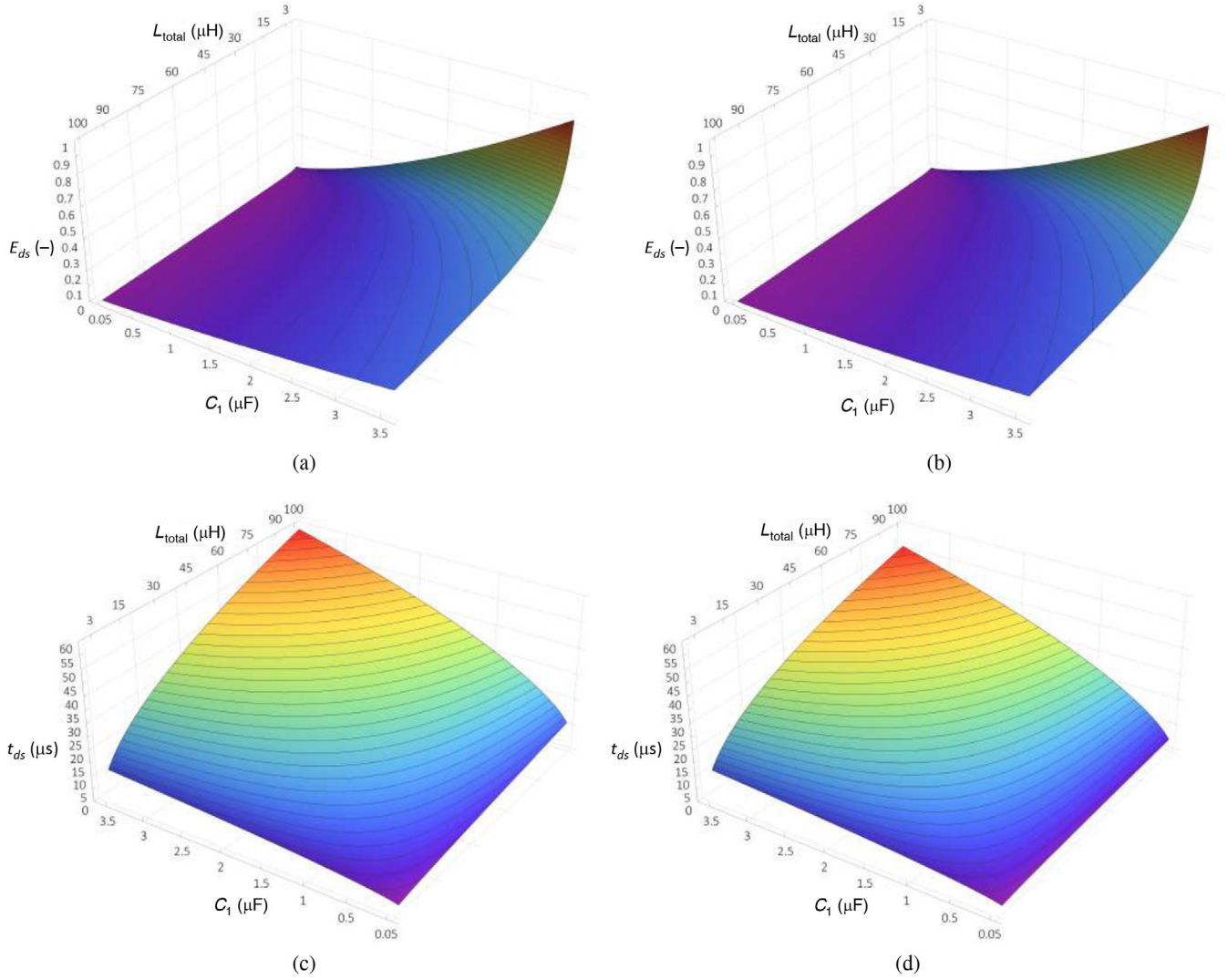

FIGURE 8 Energy index and time period $t_{dc} - t_{ft}$ as a function L_{total} and C_1. The results are obtained for detection delay T_d of 1 μs. In (a) is the energy index when overcurrent detection is used and in (b) is the energy index when ROCOC detection is used. Panels (c) and (d) show the time period $t_{dc} - t_{ft}$ when overcurrent detection and ROCOC detection are tripped, respectively

the nominal current of the LVDC system, required overload capability and maximum allowable losses per pole. Furthermore, the design criteria focus on peak overvoltage and peak pulse current. The design starts with a selection of MOSFETs that have a breakdown voltage rating at least double the grid nominal rating. The requirement is a consequence of (21). Using the maximum allowed losses per pole, the number of paralleled devices can be calculated. Afterward, SSCB overload capability needs to be verified. The overload capability of the SSCB is the capability to withstand higher than nominal pulse currents for a given period. Typically these requirements are given for circuit breakers as time–current characteristic as the one shown in Figure 2(b). At this step, if necessary, the number of paralleled MOSFETs must be increased to withstand the required current pulse. Alternatively, a device with smaller $R_{ds,on}$ can be chosen and the calculation repeated. When the overload capability condition is met, the design can continue to the overvoltage surpassing snubber design.

For the snubber design, the absolute maximum current pulse amplitude and maximum voltage are specified from the previous part. Snubber design starts with the selection of the minimum short-circuit inductance. The minimum inductance defines the current rise during a bolted short-circuit on the SSCB terminals. If the ROCOC detection is used as a complementary short-circuit detection, a smaller minimum inductor can be chosen. After the minimum inductor choke is designed, the snubber capacitor must be chosen such that it is capable to store the energy that was stored during the short-circuit in the circuit inductance. At this step, the snubber capacitance can become too large and MOSFET with higher breakdown voltage must be chosen and the first part of the design process repeated. The measure of the C_{sn} size can be the peak current that occurs due to capacitor charging during start-up or a practical limitation such as the size of the SSCB. After successful C_{sn} selection, the design must be verified for the operation with minimum short-circuit inductance. The last step is the selection of the

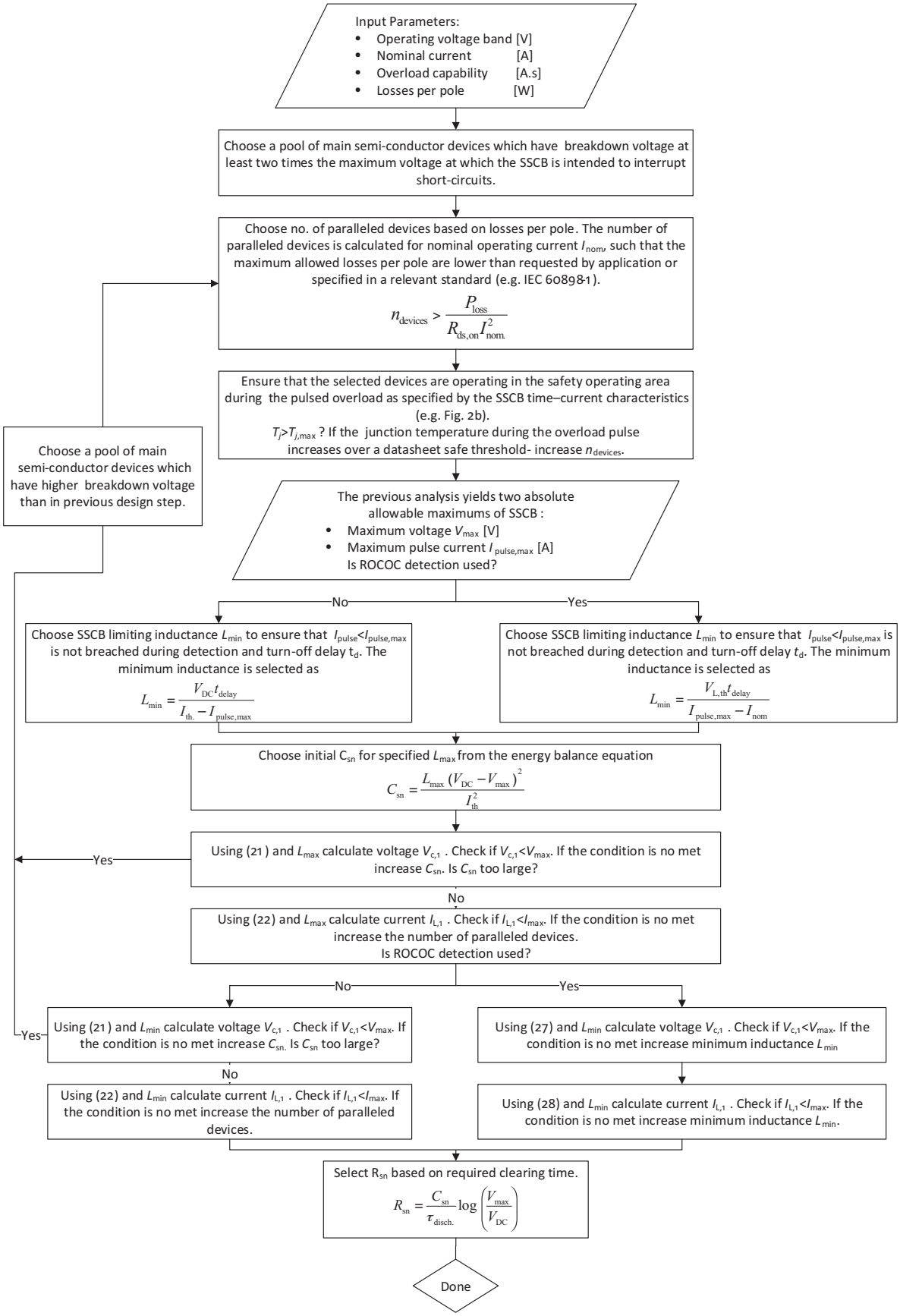

FIGURE 9 SSCB design flowchart

TABLE 3 Prototype and test circuit parameters

Parameter	Acronym	Value
Nominal voltage	V_{DC}	350 [V]
Nominal current	$I_{nom.}$	16 [A]
Threshold current	$I_{th.}$	32 [A]
On-resistance	R_{on}	32 [mΩ]
Limiting inductance	L_x	1.5 [μH]
Snubber capacitance	C_x	0.32 [μF]
Snubber resistance	R_x	39 [Ω]
Line resistance	$R_{Line,x}$	2 [Ω]
External capacitance	C_{DC}	1.2 [mF]
External inductance	$L_{ext.}$	6 [μH]
Short-circuit resistance	R_{SC}	1 [Ω]

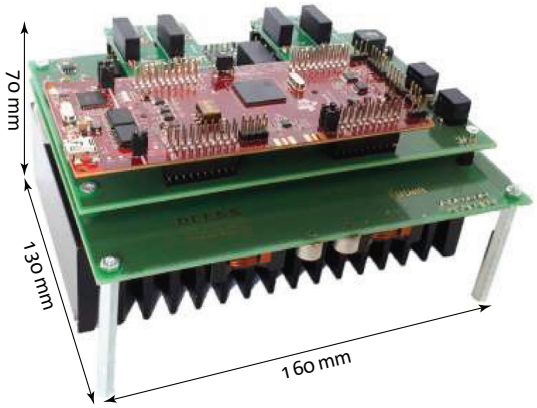

FIGURE 10 Prototype SSCB

snubber capacitor which is chosen based on the desired discharge time.

4 | EXPERIMENT

The SSCB prototype parameters are summarized in Table 3. The prototype is shown in Figure 10. The prototype schematic is shown in Figure 2(a). The prototype used in the experiments uses in total four SiC MOSFETs. On the prototype, the overcurrent detection is implemented using drain-source voltage measurement using the method adopted from [40]. The ROCOC is based on the differential measurement of the voltage drop across the current limiting inductor L_1. The measured values are fed to analogue comparator modules on microcontroller unit (MCU). The use of analogue comparator modules significantly reduces the detection delay time compared to ADC modules.

4.1 | SSCB prototype design

In this subsection, the SSCB prototype design is explained using design steps introduced in the design flowchart in Figure 9. In the first step, the appropriate semi-conductor is

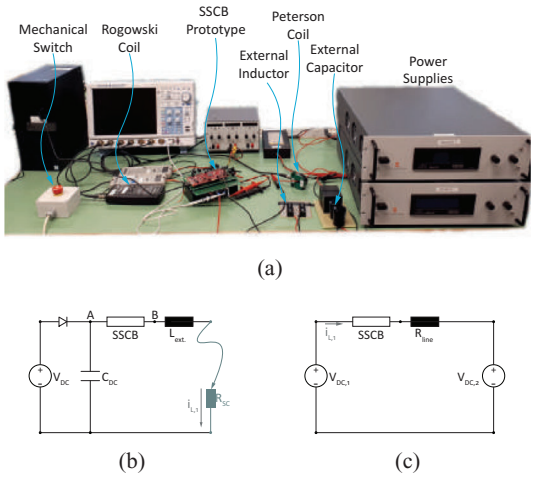

FIGURE 11 Evaluation Circuits. In (b) is the circuit used in the laboratory to evaluate the short-circuit detection. In (c) is the circuit used to ensure the resistivity of the detection method to load steps.

selected—C3M0021120K. The efficiency of the SSCB at $I_{nom.}$ should be above 99% [22]. If two devices are paralleled, the SSCB efficiency at $I_{nom.}$ is 99.9%. The overcurrent threshold of the SSCB is 32 A. C3M0021120K at 145°C case temperature has continuous drain current of 50 A. C3M0021120K is an appropriate choice, and overvoltage snubber can be designed in the following steps.

The choice of the minimum inductor that is integrated within SSCB must consider prospective $\frac{di}{dt}$, detection delay and the inductor saturation. To achieve higher versatility of the laboratory prototype, the prototype was designed to operate with and without the ROCOC detection. Using the equation for minimum inductance when only overcurrent detection is used and the worst-case detection delay of 1 μs is considered the required minimum inductance is 2 μH. Due to component availability with sufficient saturation current, a value of 3 μH is used.

The maximum value of loop inductance L_{max} is not chosen by the SSCB designer. It is a property of the system in which the SSCB is used. L_{max} can be estimated from the cable type and cable length. Moreover, the system may require extra inductance to reduce the current ripple or extra inductance is added to achieve selective operation of short-circuit protection. For the prototype, a conservative value of 200 μH is assumed, the resulting snubber capacitor size is 0.29 μF. The SSCB designer should consider the effect of capacitor ageing and voltage derating if ceramic capacitors are used. The prototype SSCB has slightly larger capacitance, as a result of using discrete devices with pre-defined values. Using (22) it can be confirmed that the maximum current is well below the maximum pulse current of the C3M0021120K. As the last step, the snubber resistor is chosen using the equation shown in the flowchart.

4.2 | Experimental setup

The short-circuit was created with a mechanical switch. A complete test bench is shown in Figure 11(a). The prototype was

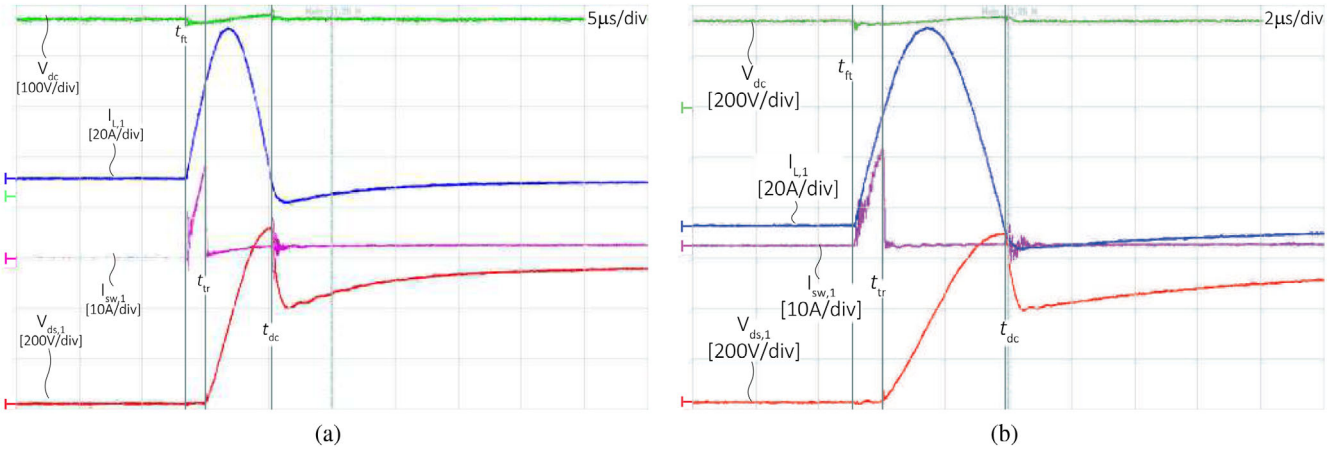

FIGURE 12 Experimental results for fault at node B. In (a) are the power waveforms of the SSCB with external inductance added to the circuit. In (b) are the power waveforms of the SSCB without the external inductance, when ROCOC detection is activated

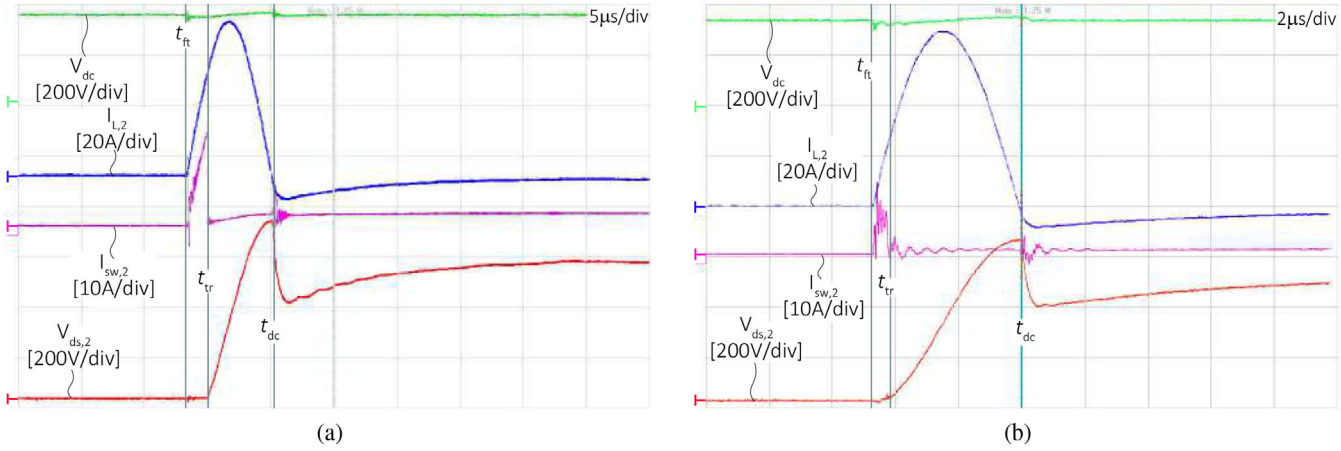

FIGURE 13 Experimental results for fault at node A. In (a) are the power waveforms of the SSCB with external inductance added to the circuit. In (b) are the power waveforms of the SSCB without the external inductance, when ROCOC detection is activated

tested in two test circuits shown in Figures 11(b) and (c). The circuit in Figure 11(b) was used to test the short-circuit detection and clearing capabilities of the SSCB. During the short-circuit tests, an external capacitor was added to the source to emulate ideal voltage source behaviour better. The experiment was repeated with external inductance $L_{ext.}$ and without. As discussed with minimum loop inductance, the current rises faster, and the ROCOC detection is activated. When external inductance is added, the overcurrent detection is activated. The circuit in Figure 11(c) was used to test the behaviour of the SSCB during large load steps. The current through the drain of the MOSFET was measured with Rogowski coil and the current through the SSCB during short-circuit detection with a Peterson coil.

4.3 | Overcurrent detection experiment

The experimental results for the short circuit detection when the SSCB orientation is as in Figure 11(b) are shown in Figure 12. The detection based on measurement of the drain-source voltage $v_{ds,1}$ is shown in Figure 12(a). Figure 12(a) shows the power signals in the circuit - current through the SSCB $i_{L,1}$, current through the drain of the blocking MOSFET $i_{ds,1}$, the voltage on the external capacitor V_{DC} and the voltage on the drain-source of the blocking MOSFET $v_{ds,1}$. As shown in the figure, the total time after the fault inception to the turn-off is 2 μs. After the SSCB MOSFETs are turned off, the current continues to flow and charges the snubber capacitor. Because the external inductor is part of the circuit, the charging process takes up to 6 μs. After the capacitor is charged, the current reverses its direction, and the capacitor is discharging through the snubber resistance. During this stage, the MOSFET body diode is used. The transition to the MOSFET body diode is visible in Figure 12(a) where the noise in the drain current marks the transition. The process ends when the capacitor is discharged, and the voltage is blocked as is visible from $v_{ds,1}$.

The experiment with added external inductance was repeated with the SSCB inverted compared to Figure 11(b), that is, the short circuit is at node A. The results are shown in Figure 13(a). The results show that the SSCB trips at the same thresholds for

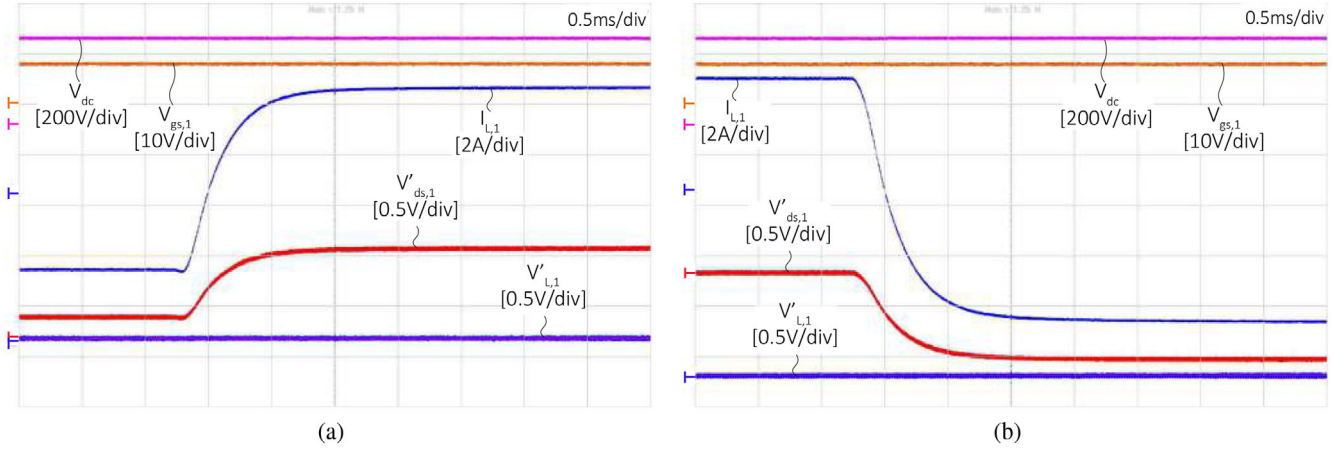

FIGURE 14 Reaction of the SSCB to load steps

both locations of fault, and the differences between the signals are minimal. Confirming the bidirectional operation capabilities of the design SSCB.

4.4 | ROCOC detection experiment

As was discussed when the short-circuit is located at the terminals of the SSCB, the overcurrent protection is not able to limit the overvoltages after opening. Therefore, the experiment in Figure 11(b) was repeated with zero external inductance. The current rises more than two times faster after the short circuit inception.

The experimental waveforms of the ROCOC detection are shown in Figure 12(b) for the fault located at node B. On the power waveforms in Figure 12(b), the fast current rise through the SSCB and the blocking MOSFET can be observed. The fault is detected within 1 μs as can be seen from the current through the drain $i_{ds,1}$. The current after opening continues to rise and reaches its peak faster than when the external inductance is in the circuit. When ROCOC detection is used, the total time from fault inception to discharge of the capacitor is 1 μs shorter than when overcurrent detection is used. The results show that the total clearing time is dominated by the time taken to charge the snubber capacitor.

The experiment was repeated with the fault located at the terminal A, and the results are shown in Figure 13(b). When the fault is located at terminal A, the time taken by the detection is 300 ns faster. The difference is caused by the fact that the fault is located closer to the inductor on which the voltage drop is measured.

4.5 | Load steps

In SSCB prototype, ROCOC detection is implemented. ROCOC detection can be prone to be activated by fast load trips. Experiment with fast load step is executed, to strengthen the confidence in the designed SSCB prototype. In [41], the load step was 1.6 A over 100 ms. In [42], the load step was 1.5 A over 400 ms. In [43], the load step was 2.3 A over 100 ms. In [7], the load step was 5 A over 50 ms. The load step is almost a hundred times faster than in the preceding works. Figure 14 shows the results of the experiments executed on the test circuit shown in Figure 11(c). The voltage source and load $V_{DC,1}$ and $V_{DC,2}$ were emulated with Delta Elektronika SM-15K. The results of step-up of the current through the SSCB and step-down are shown. As is visible, the current rises to five times the original value. In both Figures 14(a) and (b), the measured voltage across the blocking switch $v'_{ds,1}$ follows the current through the SSCB. The voltage $v'_{L,1}$ is the trip signal of the ROCOC detection method. As is visible during the load steps, it remains zero and does not initiate spurious trips.

5 | CONCLUSION

Design criteria and constraints of an SSCB for an LVDC microgrid protection were derived based on the SSCB operation analysis. The design criteria consider the effect of different system parameters, detection methods and detection delay times. The design space and the limitations of the SSCB with different detection methods are analysed via sensitivity analysis. The findings about the SSCB operation and operating limits are used to propose an SSCB design procedure which is summarized in a simple design flowchart. SSCB prototype is developed, and its performance is evaluated in different operating scenarios under nominal grid voltage and current.

Sensitivity analysis presents the ROCOC detection as a useful tool to optimize the size of the snubber capacitors when the SSCB is expected to operate in grids with minimal self-inductances. The analysis demonstrates the vitality of the optimal size of the snubber capacitance as it is directly linked to the total clearing time and the peak short-circuit currents. Moreover, it is shown that the maximum loop inductance is an important design parameter that needs to be specified for every SSCB.

As clarified in the analysis for maximum values of the loop inductance, the detection delay has minimal effect and only increasing the snubber capacitor can limit the maximum voltage on the blocking MOSFET.

Derived design constraints are a useful tool to optimize the size of the SSCB equipped with a combination of detection methods for different grid parameters. Moreover, the derived constraints are compact and can be used as an effective tool to evaluate the effect of different LVDC grid protection schemes on the size of the SSCB.

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