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Design of moisture vapor pressure sensor for popcorn failure analysis in molding compound

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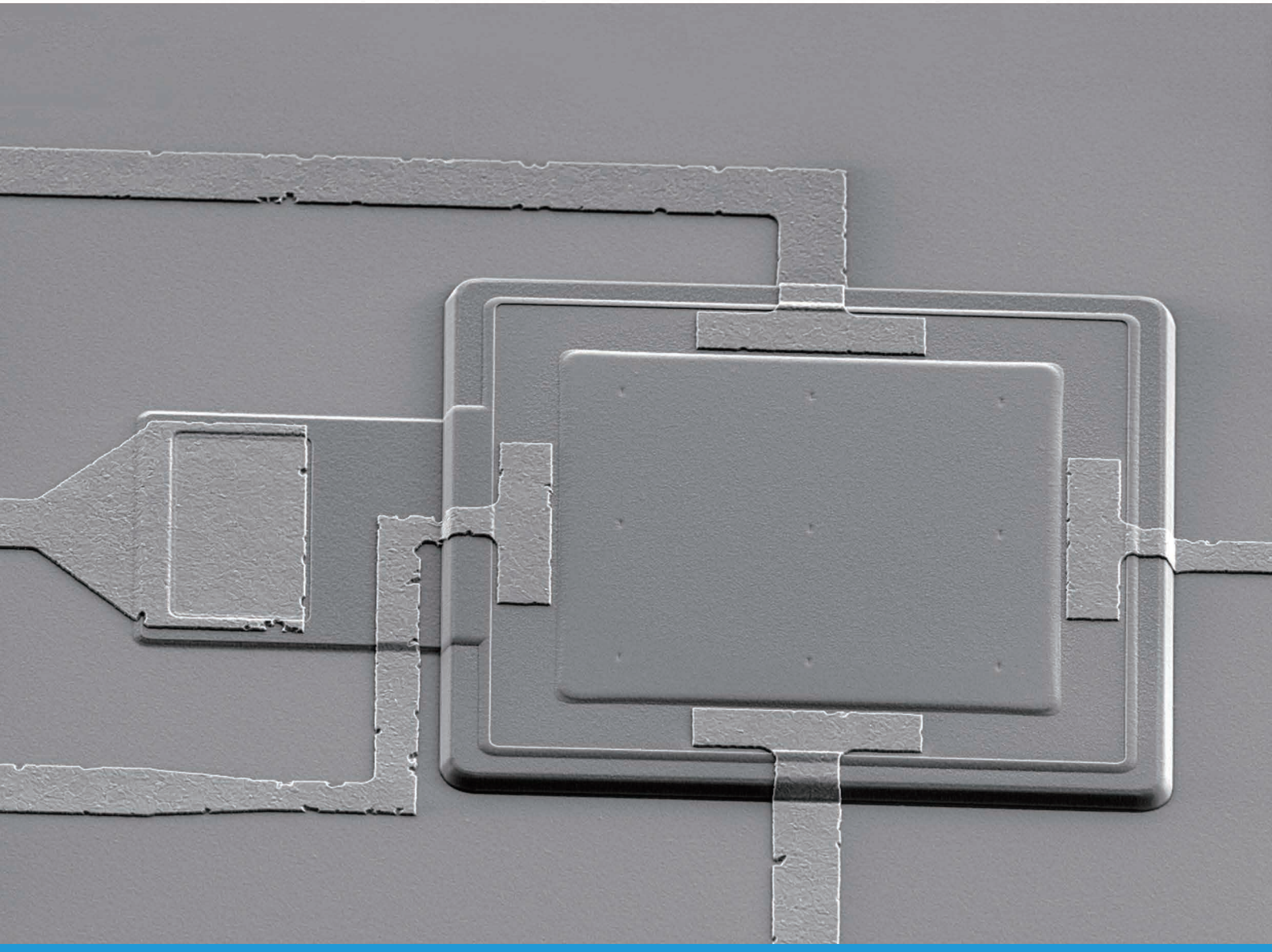

DESIGN OF MOISTURE VAPOR PRESSURE SENSOR FOR POPCORN FAILURE ANALYSIS IN MOLDING COMPOUND

by

Shuhan Yang

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Thesis committee: Prof. dr. ir. G.Q. Zhang
Prof. dr. X. Fan
Dr. ir. A. Bossche
Ir. J. Mo

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ABSTRACT

Moisture absorbed by the hygroscopic polymers like molding compound and die-attach vaporizes during reflow lead to a high vapor pressure inside the electrical components lead to failure in the electrical device, named as popcorn failure. Popcorn failure in plastic encapsulated microcircuits has been a critical issue for electronic device reliability. Researches have been conducted on investigating the failure mechanism. Among all the factors that contributed to the failure, vapor pressure is one of the primary sources of stress that causes crack of the molding compound and delamination between critical interfaces. Numerous publications demonstrate the vapor pressure evolution and contributing factors with mathematical models, simulations, and tests. However, direct measurement of vapor pressure is not yet reported.

This thesis presents the design and fabrication verification of a pressure sensor to measure the vapor pressure evolution in moisture-containing polymers at reflow temperatures. The specifications and requirements are extracted from the failure mechanism reported in literature. A touch-mode capacitive pressure sensor with in-situ doped poly-SiC is designed to measure vapor pressure from atmospheric pressure to 8 MPa under reflow temperature up to 300 °C. Simulation on touch mode capacitive readout is performed to verify the design parameters and provide an estimation of device performance. The fabrication process is designed and conducted with several methods for crucial steps along with different structure dimensions to investigate an optimal solution.

A complete fabricated device is achieved with measured initial capacitance from 12.3 to 26.7 pF for different sizes of diaphragms. The deviation between the measured results and simulation results due to fabrication problems is analyzed. Possible causes and solutions of problems that occurred in fabrication and measurement, such as unexpected upward bending of the diaphragm, leakage current between the capacitor electrode plate, and uniformity of SiC layer fabrication, are discussed. Problem correction, device optimization, complete characterization, and experiments for vapor pressure measurement in molding compound remains as future work.

Keywords: Vapor pressure sensor, MEMS, popcorn failure analysis, touch mode capacitor, high temperature, high-pressure sensing.

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November 26th, 2021
Shuhan Yang

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ACRONYMS

1 INTRODUCTION

1.1 MOTIVATION

"Popcorning" is a type of failure that occurs in plastic encapsulated microcircuit (PEM). The hygroscopic molding compound used in electronic packages absorbs moisture during storage and shipment. During the reflow soldering process for assembly of the electronic component into a printed circuit board (PCB), the moisture content vaporizes quickly due to rapid environment temperature change from room temperature to a typically reflow peak temperature up to 260 °C according to standard reflow profile [2] (Table 1.1).

Table 1.1: Standard Pb-Free Reflow Process temperatures (Tc) [2].

Package Thickness	Volume (mm^3) < 350	Volume (mm^3) 350 - 2000	Volume (mm^3) > 2000
$< 1.6mm$	260 °C	260 °C	260 °C
$1.6mm - 2.5mm$	260 °C	250 °C	245 °C
$> 2.5mm$	260 °C	245 °C	245 °C

Stress caused by multiple mechanisms at the reflow temperature is the main factor of popcorn failures like delamination and cracks. When the package stress exceeds the adhesion strength of the molding compound/die interface, delamination is initiated and propagates when the vapor accumulates inside the delaminated cavity (Figure 1.1a). When stress inside the molding compound grows larger than the fracture toughness, cracks will occur (Figure 1.1b). Those failures may lead to many reliability problems, such as corrosion-induced failures due to ionic contamination and electrical failures due to sheared ball bonds [12].

Package stress are composited of several mechanisms modeled in Figure 1.2. Moisture itself generates hygro-mechanical stress due to coefficient of moisture expansion (CME) and, at a higher temperature, vaporized as steam to reduce adhesive strength and contribute to vapor pressure; The heat, on the other hand, causes thermal-mechanical stress at interfaces due to coefficient of thermal expansion (CTE) and also decrease fracture toughness of molding compound above glass transition temperature. These are the main factors that result in popcorn failure. Among all the factors, vapor pressure contributes to a large percent of stress in the theoretical models. Therefore, research of the vapor pressure and moisture behavior inside PEM is essential for predicting and improving popcorn failure related reliability

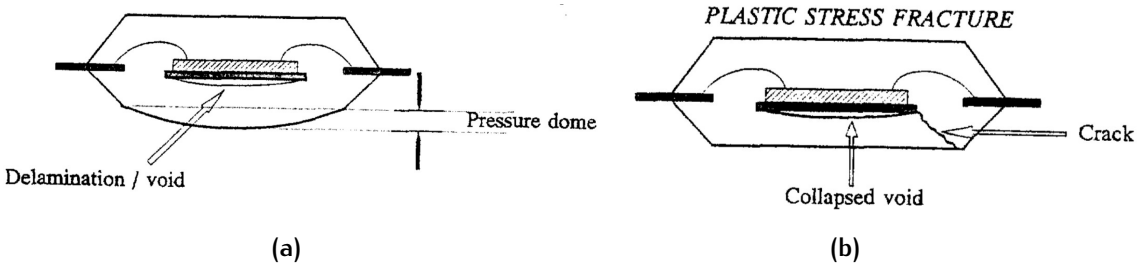


Figure 1.1: Mechanism of popcorning: (a) Moisture vaporization during reflow, demaniation initiated; (b) Cracks occur when internal stress grows larger than fracture toughness [12].

problem [1].

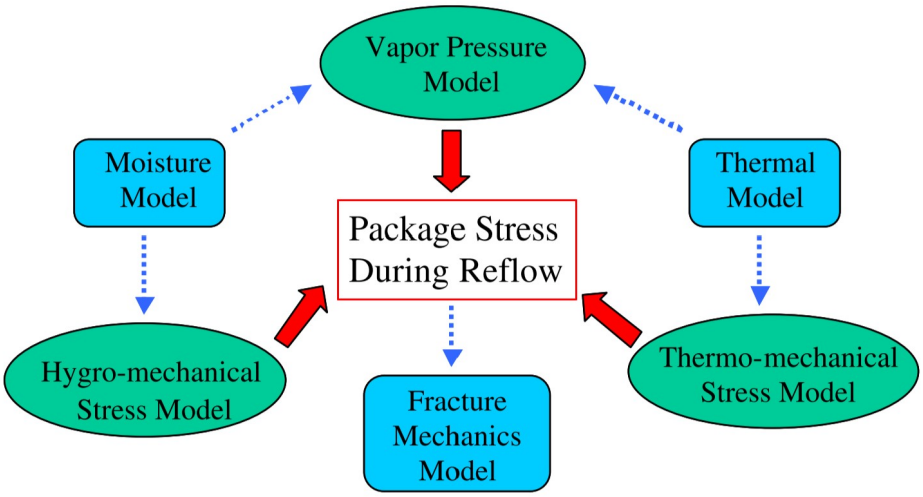


Figure 1.2: Integrated stress composition model in package during reflow [1].

Analysis of vapor pressure inside molding compound is essential for understanding moisture-induced failure mechanisms in electronic packaging. Researchers have been investigating the failure mechanism and searching for possible solutions. Experimental analyses were performed to investigate the relations among critical parameters such as temperature, humidity, and failure rate. Theoretical models were developed based on experimental results and mathematical explanations to describe contributing mechanisms such as moisture absorption, moisture diffusion, and vapor pressure accumulation [13]. Numerical approaches to calculating moisture concentration and vapor pressure were published. Simulations on moisture behavior and vapor pressure generation were also reported.

However, there is a missing gap in popcorn failure analysis. No research is reported to measure the quantified value of vapor pressure inside the electric components. The measurement of vapor pressure caused by moisture absorption inside the mold-

ing compound is essential to verify the existing theories and create a profile for further failure mechanism analysis. The challenge exists in the measurement of vapor pressure due to the high reflow temperature, possibly high-pressure range, and sensor implantation. Multiple reasons lead to the challenge will be illustrated in Section 2.1.

1.2 APPROACHES

Sensor technology is one of the eye-catching and fast-developing high-tech in the world today. It is also an important symbol of the development of contemporary science and technology. Whether in the field of industrial production or daily life, every technology is inseparable from sensors. Among various sensors, pressure sensors have the advantages of small size, lightweight, high sensitivity, stability and reliability, low cost, and easy integration. Pressure sensors provide the possibility for inline measurement of vapor pressure during the reflow process.

Especially with the development of micro-electro-mechanical systems (MEMS) technology, semiconductor sensors are developing towards miniaturization, with low power consumption and high reliability. With the micro-machining process, pressure sensors with micron-level grooves, stripes, and films can be processed under precise control, thereby becoming an ideal solution to vapor pressure measurement in molding compounds. However, commercially available pressure sensors can not meet the requirements of operating pressure range, operating temperature range, and device dimensions simultaneously.

Two alternative approaches can be considered for monitoring the value of vapor pressure during the reflow process. The first approach is to design a specific setup with commercial sensors to isolate the pressure sensor from applied heat on the molding compound by transmitting the pressure to an external sensing device with low thermal conductivity materials. This option provides an experimental setup for the vapor pressure measurement at a lower cost. However, the repeatability of the setup is compromised, and inline measurement is hard to achieve. Another approach is to design a customized sensor for vapor pressure measurement in molding compounds during the reflow soldering process. This option provides a more general solution for failure analysis research and industrial reliability tests because of its smaller size, better repeatability, easier mass production, and possible inline measurement. The disadvantage of this option is a longer development period and higher research costs.

MEMS technology enables the realization of the second approach. Micro-machined MEMS sensors play an important role in various applications such as biomedical, automotive, and aviation industries. The MEMS devices have advantages of high

flexibility, adaptability, repeatability, and miniaturization. They are easier to implant inside a package to be measured, and protocols can be investigated for a more general process [14]. Therefore, designing a MEMS device for vapor pressure measurement in this application also enables future integration in functional chips for stability monitoring.

Table 1.2: Properties of several materials used in MEMS sensors, adapted from [15, 16].

Properties	SiC	Si	Al
Young's modulus (GPa)	300 to 500	130 to 180	70
Fracture strength (GPa)	max. 21	1 to 3	-
Thermal conductivity ($Wcm^{-1}K^{-1}$)	5	1.5	2.37
Thermal explansion coefficient (ppm/K)	4.2 to 5.6	2.33	25
Energy gap (eV)	2.3(3C-SiC) to 3.4(2H-SiC)	1.12	-
Chemical Inertness	Excellent	Poor	Poor
MEMS compatibility	Good	Excellent	Good
Avaibility/Cost	Fair	Good	Excellent

Moreover, the desired MEMS sensor should be harsh environment compatible, considering the harshness brought by the reflow process. Silicon carbide (SiC) has been reported as a promising material for MEMS devices that requires operating in high temperatures, high pressures, and corrosive chemicals because of its excellent mechanical and electrical properties as shown in Table 2.4 [17]. The higher Young's modulus of SiC can provide higher sensitivity as a pressure sensing element than silicon and aluminum; a larger bandgap makes SiC perform better as an electrical component at a high-temperature environment when the performance of silicon is compromised. SiC is suitable for high-pressure measurement due to its larger fracture strength. Therefore, SiC is a competitive candidate for both sensing and structural material and electrical integrated circuit (IC) at elevated temperatures. Considering all these excellent properties, SiC MEMS sensor is a promising solution for vapor pressure sensing in molding compounds at reflow temperatures. Many articles reported the performance of SiC pressure sensors in the past years. New sensor structures were also designed to adapt to harsh environments. Based on these researches, designing a sensing device specifically for vapor pressure measurement in molding compound during reflow is possible.

1.3 OBJECTIVES

In this project, a pressure sensor, as the tool for vapor pressure measurement in molding compounds, will be designed based on previous researches on popcorn failure mechanisms and high-temperature compatible sensors. There are several requirements for pressure sensor design. Firstly, the sensor should properly function throughout the reflow process with a peak reflow temperature up to 300°C. Secondly, the sensor should be designed to measure the moisture vapor pressure

inside the molding compound, as high as a few MPa. The position of the sensor should be considered to best measure the vapor pressure generated by the molding compound. Thirdly, the sensor needs to have enough sensitivity to measure the pressure change from precondition temperature to reflow temperature. Finally, materials under test, like molding compounds, should be able to assemble on the sensor. A suitable sensor is vital to measure the vapor pressure generated from the molding compound.

This project aims at designing a MEMS pressure sensor for this specific application. Previously, Luke's Ph.D. thesis work [18] provided a reference for designing and fabricating a piezoresistive pressure sensor that could work under a higher temperature range. In combination with other pressure sensing methods for high-temperature applications, Luke's pressure sensor can be modified to fit the requirements. Finite element analysis (FEA) simulations will be performed to aid optimization of the design parameters. The fabrication process will also be designed and verified for realizing the designed sensor structure based on technology in cleanroom 100. Brief measurements of the sensor will be performed to check fabrication outcome. The objectives of the thesis project are listed as follows:

1) Investigate the mechanism of vapor pressure generation for the pressure sensor design based on literature review.

2) Define specifications and functions of MEMS pressure sensing device for measuring vapor pressure generated by molding compound at reflow temperature.

3) Design a MEMS pressure sensor to measure vapor pressure inside the molding compound during reflow.

4) Design and verify fabrication process for the device with available technologies.

1.4 CONCLUSIONS AND OUTLINE

This thesis presents a complete process of designing and fabricating a pressure sensor for vapor pressure analysis in the molding compound, including project definition, preparatory study of the failure mechanism and pressure sensor technology, defining function and specifications, sensor device design with FEA simulations, process design and device fabrication. The contents of the thesis report are organized as follows:

Chapter 1, this chapter, gives an overview of the thesis project. The problem of popcorn failure analysis is briefly described, and two possible approaches

are discussed based on previous researches of related technologies. Expected workflow and outcomes are presented, and the project objectives are listed based on the discussions.

Chapter 2 will discuss the background knowledge of the popcorn failure mechanism and the theory of vapor pressure generation, which are critical foundations for project definition and sensing device design. The basic principles, promising structures, and state-of-the-art of pressure sensors, especially devices for high-temperature applications, will also be explained as design reference.

Chapter 3 gives the complete design flow of the device, which includes specifications definition, design principles, analytical models, and device structures. FEA simulations using COMSOL are carried out to verify the viability of designed structures and provide reference of critical dimensions and parameters. At the end of this chapter, a group of designed parameters is listed.

Chapter 4 will illustrate the fabrication process of the device. Firstly, process flow is explained along with designed device structures. Then a short description of photomask designed for device process is presented. Then critical fabrication steps and encountered problem will be discussed, possible reasons are proposed. Finally, the fabricated device and simple measurement results are shown.

Chapter 5 provides a conclusion of this thesis and the achieved workflow. Also the outcome of this thesis is discussed. Finally, potential future work for this project is proposed.

2 BACKGROUND RESEARCH

This chapter will discuss some background knowledge. Firstly, useful knowledge of the popcorn failure mechanism will be given in Section 2.1, including an introduction on the failure mechanism, previous research for failure analysis, and some critical information required for the sensor design. Then results for literature research in pressure sensors will be given in Section 2.2.

2.1 POPCORN FAILURE MECHANISM

2.1.1 Previous work summary

Moisture related reliability problem has been a concern in electronic packages for many years. Moisture content inevitably absorbed by plastic package components during storage and shipment vaporizes quickly during soldering reflow due to the abrupt change of temperature. High vapor pressure accumulates inside the plastic molding compound and results in failures such as crack and delamination inside the package. This type of failures is known as "popcorn failure".

The popcorn failure was first mentioned by Fukuzawa et al. [19] in 1985. Numerous researches have been done after Fukuzawa to investigate the vapor pressure evolution in moisture absorbale polymers under reflow environment. Theoretical analysis for vapor pressure evolution in different kinds of packages has been conducted and various of mathematical models were published [20, 21, 22, 3, 10]. FEA simulations of vapor pressure and related based on the theoretical models were presented in some publications. Experimental tests have also been performed to verify the theories. Methods such as measuring weight gain, cracking temperature dependency were published [23, 21].

In literature, two types of theoretical approaches are discussed. The first approach, micro-mechanics-based theories, modeled the molding compound as pores material and the vapor pressure generated inside the molding compound when exposed to reflow temperature [1, 10, 24]. The vapor pressure generated during heating depends on the current state of moisture in package voids, and the maximum pressure remains at saturated pressure when the moisture is in mixed liquid/vapor phase.

Another approach is to study the vapor pressure in a delamination-induced internal cavity between molding compound and die pad. These models assumed an initial cavity exist in material or the interfaces to deduce vapor pressure evolution when initial delimitation exists based on Henry's law. Different assumptions, mathematical derivations, and results are presented in the literature [3, 22]. Some typical mathematical approaches of water vapor pressure generation were summarized in a review by Chen [20]. The conclusions of the theories were found to be contradictory in the articles.

Vapor pressure models formulated by previous researches are critical reference for the sensor design. The measured pressure and temperature range, the position for the sensing structure, sensor dimension, test method, and potential research aspects will be determined by theories and simulations mentioned in this section. Moreover, the contradictory conclusion of the two theories made measurement of the actual vapor pressure more essential. The vapor pressure models contributed to sensor design will be discussed in Section 2.1.4.

2.1.2 Preconditioning and reflow temperatures

The hygroscopic polymers absorb moisture under a specific procedure called preconditioning in reliability tests. Temperature, time, and humidity are the three parameters to describe the precondition environment. JEDEC STANDARD [2] is widely used in both modelling and experimental tests for moisture related failure analysis. Figure 2.1 lists the moisture soak times suggested in JEDEC Standard 22-A113D.

Hygroscopic polymers used in packages absorb a certain amount of moisture after preconditioning. Then the electrical component will be undergoing soldering reflow for surface mounting. Different reflow profiles (Figure 2.2) apply to different kinds of assembly methods, which can also be found in the JEDEC STANDARD. The highest reflow peak temperature can be higher than 250 °C for lead-free assembly.

Under reflow temperature, which varies from room temperature to peak temperature within 8 minutes, water content inside polymers vaporizes quickly, thus generating vapor pressure inside the polymer or other microcavities near the polymer. The vapor pressure can be calculated with the moisture concentration after precondition and temperature variation from precondition to reflow temperatures discussed in the following section.

Level	Floor fife		Soak requirements			
			Standard		Accelerated equivalent [1]	
	Time	Conditions	Time (hours)	Conditions	Time (hours)	Conditions
1	Unlimited	≤30 °C/85% RH	168 +5/-0	85 °C/85% RH		
2	1 year	≤30 °C/60% RH	168 +5/-0	85 °C/60% RH		
2a	4 weeks	≤30 °C/60% RH	696[2] +5/-0	30 °C/60% RH	120 +1/-0	60 °C/60% RH
3	168 hours	≤30 °C/60% RH	192[2] +5/-0	30 °C/60% RH	40 +1/-0	60 °C/60% RH
4	72 hours	≤30 °C/60% RH	96[2] +2/-0	30 °C/60% RH	20 +0.5/-0	60 °C/60% RH
5	48 hours	≤30 °C/60% RH	72[2] +2/-0	30 °C/60% RH	15 +0.5/-0	60 °C/60% RH
5a	24 hours	≤30 °C/60% RH	48[2] +2/-0	30 °C/60% RH	10 +0.5/-0	60 °C/60% RH
6	Time on Label (TOL)	≤30 °C/60% RH	TOL	30 °C/60% RH		

Figure 2.1: Required soak times in hours [2].

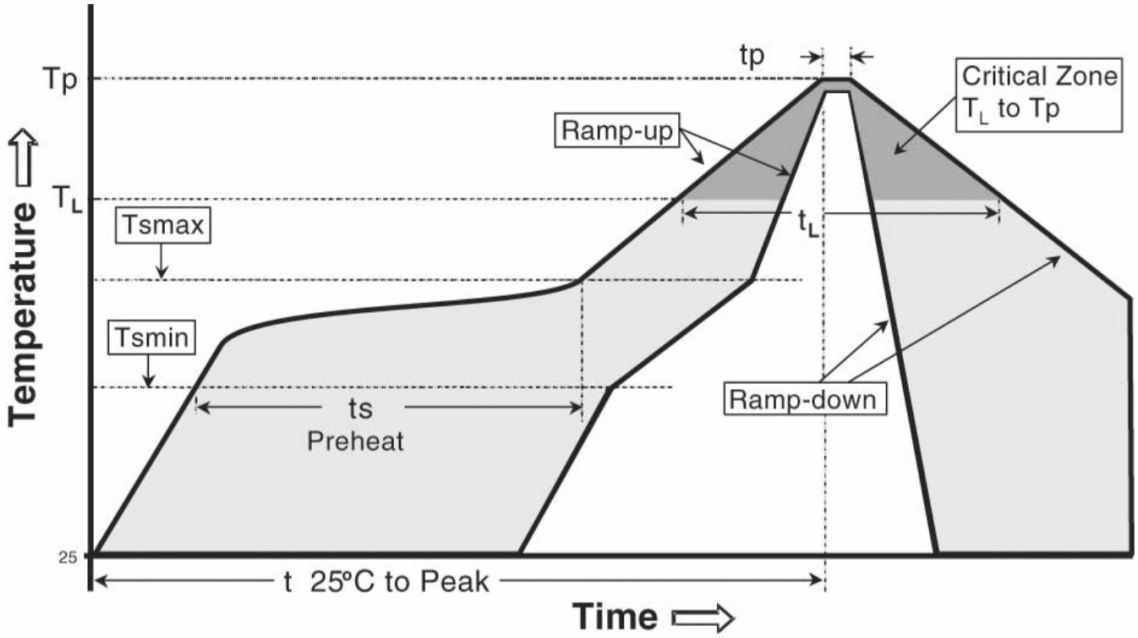


Figure 2.2: Reflow temperature profile [2].

2.1.3 Moisture absorption and diffusion

Moisture absorption and diffusion models were built in several publications to predict moisture concentration variation at certain ambient environment in packages [10, 25, 26, 27]. The amount of encapsulated moisture vaporized at high reflow temperature determines the generated vapor pressure level.

Moisture absorption

Moisture concentration is determined by material properties, the external ambient environment (Ambient temperature and Humidity), and absorption time. In both micro-mechanics based theories and Henry's law based theories, the moisture absorption is deduced by material properties and preconditioning parameters. Moisture will saturate to a certain value when sufficiently exposed to the external ambient. Table ?? adapted from the micro-mechanic based pressure model article [10] gives the moisture and vapor pressure properties of typical molding compound based on three preconditioning levels.

Table 2.1: Moisture related properties of typical molding compound [10].

Precondition	Saturated vapor density $\rho_{sat}(g/cm^3)$	saturated vapor pressure $p_{sat}(MPa)$	Ambient vapor density $\rho_{ext}(g/cm^3)$	Ambient vapor pressure $p_{ext}(MPa)$	Moisture Diffusivity $\alpha_D(cm^2/s)$	Saturated moisture concentration $C_{sat}(g/cm^3) = p_{ext}S$
30 °C/60 %RH	3.04×10^{-5}	4.24×10^{-3}	$0.6\rho_{sat}$	$0.6p_{sat}$	3.13×10^{-9}	7.86×10^{-3}
85 °C/60 %RH	3.58×10^{-4}	5.87×10^{-2}	$0.6\rho_{sat}$	$0.6p_{sat}$	2.85×10^{-8}	8.84×10^{-3}
85 °C/85 %RH	3.58×10^{-4}	5.87×10^{-2}	$0.85\rho_{sat}$	$0.85p_{sat}$	2.85×10^{-9}	1.25×10^{-3}

The Henry's law based theories give the equilibrium concentration in molding compound by Equation 2.1 under a particular environment. The saturated molar density of water $\mu(mole/m^3)$ is used by both theories:

$$\mu = SP \tag{2.1}$$

Where $P(Pa)$ is the partial pressure of water vapor in the ambient derived by saturated vapor pressure (Given by Shirley [26]), relative humidity H and temperature T:

$$P = HP_{sat}(T) \tag{2.2}$$

And S is the solution coefficient where Kitano [25] give $S_\infty = 2.75 \times 10^{-8} mole/m^3 Pa$ and $Q_m = 38.7kJ/mole(0.401eV)$. $R = 8.3145J/mole\ K$ is the universal gas constant, T is absolute temperature.

$$S = S_\infty exp(\frac{Q_m}{RT}) \tag{2.3}$$

Or with molar concentration of water vapor $\rho(mole/m^3)$ in ambient $\rho = P/RT$, the ratio of saturated and ambient water density is then derived by

$$\frac{\mu}{\rho} = SRT \tag{2.4}$$

Moisture diffusion

The moisture will diffuse into the polymer with time. Fick's law describes moisture diffusion in one dimension:

$$D\frac{\partial \mu}{\partial x} = -J \tag{2.5}$$

$$\frac{\partial \mu}{\partial t} = D\frac{\partial^2 \mu}{\partial x^2} \tag{2.6}$$

Where x and t are position and time, J is the flux, and $D(m^2/s)$ is the diffusivity:

$$D = D_\infty exp(-\frac{Q_d}{RT}) \tag{2.7}$$

Where $D_\infty = 4.72 \times 10^{-5} m^2/s$, and $Q_d = 48.4kJ/mole(0.502eV)$ given by Kitano [25]. The moisture concentration should reach equilibrium throughout the package when exposed to the preconditioning ambient with sufficient time.

The micro-mechanics-based theory modeled the molding compound as porous material and the moisture will absorbed and trapped in the pores. Free volume fraction is used to describe the calculate the moisture absorption level based on moisture concentration C, saturated moisture concentration C_{sat}, moisture density ρ, and saturated moisture density [10]. Where the saturated moisture concentration can be also derived by solubility S and the ambinet vapor pressure:

$$S = C_{sat}/p_{ext} \tag{2.8}$$

The moisture concentration as a function of time and distance to surface were derived by Gebhart [27]. An important conclusion for this deduction is that moisture concentration along the interfaces is not continuous, while the partial vapor pressure and the flux of moisture is continuous.

The principles and results of the two types theories varies in determining the moisture concentration and models in different articles also give different results. Nevertheless, the conclusions are the same. The Henry's law based theories indicate the saturated moisture concentration, which is achieved by sufficient exposure time, is dependent on material property, the ambient humidity and temperature.

2.1.4 Vapor pressure models

Vapor pressure models were built cased on the moisture concentration research. Two models were a whole field vapor pressure model by provide complete analysis, simuation of the micro-mechanic based theory. Another Henry's law based model gives a detailed theory of vapor pressure evaluation in an initial cavity.

Vapor pressure model - Micro-mechanics based

The micro-mechanics based model concluded that the vapor pressure inside porous material is determined by moisture concentration and moisture states. Mathematical approach [10] and theory based simulations [1] will be discussed in this section as a reference for developing vapor pressure measurement method. Void volume fraction f, defined as the number of free spaces in an element volume (Equation 2.10), is used to describe the porous property in compounds.

$$f = \frac{\mathrm{d}v_f(Voidvolume)}{\mathrm{d}v(Elementvolume)} \tag{2.9}$$

$f = 1$ stands for a fully voided cavity. A representative volume element (RVE) approach is applied to estimate the vapor pressure generated inside the material. The moisture density ρ in voids will be:

$$\rho = \frac{\mathrm{d}m}{\mathrm{d}v_f} = C/f \tag{2.10}$$

Where $\mathrm{d}m$ is moisture mass (mass of moisture per unit volume of free spaces material). There are three moisture states in a porous material, pure vapor phase, and mixed liquid/vapor phase. For a device stored in initial temperature of T_0, when the current temperature T reaches phase transition temperature T_r, the moisture will fully vaporize. At the precondition temperature $T = T_0$, two possible states of moisture will be:

1 $\rho \leq \rho_{sat}(T_0)$ for vapor phase.

2 $\rho > \rho_{sat}(T_0)$ for the mixed liquid/vapor phase.

The vapor pressure in the vapor phase can be derived by ideal gas law:

$$p = \rho RT \tag{2.11}$$

In the mixed liquid/vapor phase, the vapor pressure maintains saturated vapor pressure as a function of temperature from the steam table (Table 2.2) [13]. However, some articles mentioned the vapor pressure could be higher than the saturated value [20].

Table 2.2: Saturated water vapor density and saturated vapor pressure at different temperature [13].

T°C	100	110	120	130	140	150	160	170	180	190	200	210	220	230	240	250	260
$\rho_{sat}(kg/m^3)$	0.6	0.83	1.12	1.5	1.97	2.55	3.26	4.12	5.16	6.4	7.86	9.59	11.62	14	16.76	19.99	23.73
$p_{sat}(kg/m^3)$	0.1	0.15	0.2	0.28	0.38	0.5	0.65	0.84	1.1	1.37	1.72	2.14	2.65	3.25	3.97	4.83	5.84

The vapor pressure can be calculated by three cases based on current moisture states and temperature condition.

1. $T_r < T_0 < T_{peak}$: $\rho(T_0) \leq \rho_{sat}(T_0)$ and $\rho(T) < \rho_{sat}(T)$
   The moisture density is lower than saturated value both during preconditioning and current temperature. The temperature of entire process keep moisture in single vapor phase. Vapor pressure can be calculated with the ideal gas law between precondition temperature and reflow peak temperature:

$$p(T) = \frac{Tf_0C}{T_0fC_0} = \frac{CT}{\rho_{sat}fT_0}p_{sat}(T_0)[1 + 3\alpha\Delta T] \tag{2.12}$$

2. $T_0 < T_{peak} < T_r$: $\rho(T_0) > \rho_{sat}(T_0)$ and $\rho(T) \geq \rho_{sat}(T)$
   Moisture keeps the mixed liquid/vapor phase from preconditioning to the current temperature. The vapor pressure maintains saturated between precondition temperature and reflow peak temperature:

$$p(T) = p_{sat}(T) \tag{2.13}$$

3. $T_0 < T_r < T_{peak}$: $\rho(T_0) > \rho_{sat}(T_0)$ and $\rho(T) < \rho_{sat}(T)$
   Moisture is in the mixed liquid/vapor phase at preconditioning, then after the temperature reaches transition temperature, it fully vaporizes. Thus Moisture keeps the single vapor phase at the current temperature. For $T_0 < T < T_r$, moisture in mixed liquid/vapor phase, vapor pressure keeps saturated:

$$p(T) = p_{sat}(T) = \frac{p_sat(T_r)T}{T_r} \tag{2.14}$$

   For $T_r < T < T_{peak}$, moisture in the single vapor phase and vapor pressure follows ideal gas law:

$$p(T) = p_{sat}(T)\frac{f(T_r)}{f}\frac{1 - 3\alpha(T - T_0)}{1 - 3\alpha(T_r - T_0)} \tag{2.15}$$

From the results of this model, the vapor pressure in porous material is able to be higher than saturated vapor pressure in the steam table. However, contradicted results mentioned in other micro-mechanic models.

vapor pressure model in an initial cavity

Shirley [3] presents a one-dimensional model of the vapor pressure inside a plastic package with a cavity. Figure 2.3 shows the moisture concentration level before and after heating. The influence of molding compound and cavity size were analyzed with derived formula.

The moisture content inside packges will go through three critical stages before mounted on the PCB. The three stages are:

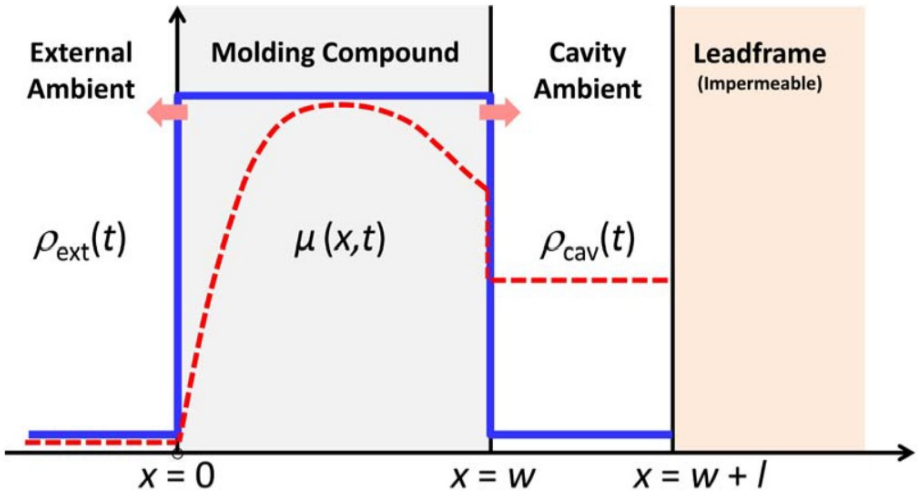


Figure 2.3: One-dimensional model of a plastic package with a cavity between molding compound and lead frame. Solid blue line: The moisture concentration after preconditioning with sufficient time; Dashed red line: Moisture concentration after exposure to the reflow ambient [3].

.

1. **Preconditioning:** The device first exposed to precondition ambient T_0, H_0 for sufficient time to reach the initial equilibrium moisture concentration. Moisture molar density in the molding compound saturated to μ_0. Initial concentration profile is determined by the humidity of precondition ambient H_0, material solubility S_0 at ambient temperature T_0, and the saturated vapor pressure at ambient temperature $P_sat(T_0)$:

$$\mu(x,0) = H_0 P_{sat}(T_0) S_0 \equiv \mu_0 \qquad (0 \leq x \leq w, t = 0) \tag{2.16}$$

2. **Reflow:** Assuming the reflow started at t=0, the device is exposed to the reflow ambient T_1, H_1. Moisture inside molding compound vaporizes at certain condition and diffuses into cavity and reflow ambient environment. Moisture concentration and pressure increased to μ_1 and P_1.

3. **After reflow:** If keep the device in certain ambient, moisture concentration and pressure will reduce to equilibrium with the ambient moisture concentration.

Vapor pressure evolution during the four stages are derived by moisture concentration with Henry's law. According to Shirley, the boundary conditions at the interfaces are determined on the reflow ambient. The moisture concentration at molding compound and enternal environment surface (Equation 2.17) and the external ambient (Equation 2.18) are both constant at the reflow condition ($T_1, H_1, x = 0, t > 0$) due to continuity:

$$\mu(0,t) = H_1 P_{sat}(T_1) S_1 = \mu_1 \qquad (x = 0, t > 0) \tag{2.17}$$

$$\rho_{ext}(t) = \frac{H_1 P_{sat}(T_1)}{RT_1} \qquad (t > 0) \tag{2.18}$$

Another boundary condition at the interfaces between molding compound and the internal cavity during reflow ($x = w, t > 0$) is then dereived by Henry's law:

$$\mu(w,t) = RT_1 S_1 \rho_{cav}(t) \qquad (x = w, t > 0) \tag{2.19}$$

At the moment reflow started, the moisture concentration at inner surface of molding compound ($x = w$, $t = 0^+$) is then derived by the equilibrium moisture condition Equation 2.4:

$$\mu(w, t = 0_+) = RT_1 S_1 \rho_0 = \frac{T_1 S_1}{T_0 S_0} \mu_0 \tag{2.20}$$

The moisture flux change from the molding compound boundary into the cavity contributes to another boundary condition:

$$-AD_1 \frac{\partial \mu}{\partial x}|_{x=w} = JA = Al \frac{\partial \rho}{\partial t}(mole/s) \tag{2.21}$$

Where Al is the volume of the cavity. And then the differential equation of cavity vapor pressure will be:

$$\frac{\partial \mu}{\partial t} + h' \frac{\partial \mu}{\partial x}|_{x=w} = 1 \qquad (x = w, t > 0) \tag{2.22}$$

Where

$$h' = \frac{RT_1 S_1 D_1}{l} \tag{2.23}$$

Several solutions of the above differential equation were brought up by Shirley. First defined m, f, ϵ, h as:

$$m = \mu - \mu_0 \qquad f = \frac{D_1 t}{w^2} \tag{2.24}$$

$$\epsilon = \frac{x}{w} \qquad h = RT_1 S_1 \frac{w}{l} \tag{2.25}$$

$$a = \mu_1 - \mu_0 \qquad b = \mu_0 (\frac{T_1 S_1}{T_0 S_0} - 1) \tag{2.26}$$

One solution for a long period of time were concluded based on VanSant's catalog [28]:
For $a = 1, b = 0$

$$m_a(\epsilon, f, h) = 1 - \sum_{\infty}^{n=1} \frac{2(\gamma_n^2 + h^2)\sin(\gamma_n \epsilon)}{\gamma_n(\gamma_n^2 + h^2 + h)} exp(-\gamma_n^2 f) \tag{2.27}$$

For $a = 0, b = 1$

$$m_b(\epsilon, f, h) = \sum_{\infty}^{n=1} \frac{2h \sin(\gamma_n \epsilon)}{\sin \gamma_n (\gamma_n^2 + h^2 + h)} exp(-\gamma_n^2 f) \tag{2.28}$$

where $\gamma_n = +\sqrt{\arctan h}$
While another solution for short time changes is given by Carslaw and Jaeger [29]:

$$m_a(\epsilon, f, h) \sim erfc(\frac{\epsilon}{2\sqrt{f}}) = \frac{2}{\sqrt{\pi}} \int_0^{2\sqrt{f}} e^{-t^2} dt \tag{2.29}$$

For $a = 0, b = 1$

$$m_b(\epsilon, f, h) \sim exp[h(1-\epsilon) + h^2 f] erfc[\frac{1-\epsilon}{2\sqrt{f}} + h\sqrt{f}] \tag{2.30}$$

The final solution to the moisture concentration evaluation can be expressed with value of m_a and m_b in Equation 2.27 and Equation 2.28, or Equation 2.29 and Equation 3.1:

$$\mu(x, t, h) = \mu_0 + (\mu_1 - \mu_0) m_a(\epsilon, f, h) + \mu_0 (\mu_0 (\frac{T_1 S_1}{T_0 S_0} - 1) m_b(\epsilon, f, h) \tag{2.31}$$

By Henry's law, the partial pressure water vapor in cavity would be:

$$P_{cav}(t) = \frac{\mu(x = w, t, h)}{S_1} \tag{2.32}$$

By Boyle's law, the molar concentration of water vapor in cavity would be:

$$\rho_{cav}(t) = \frac{P_{cav}(t)}{RT_1} \tag{2.33}$$

Shirley gives several examples about the influence of cavity and Package dimensions on the vapor pressure in the initial cavity based on the final equation derived above (Equation 2.31, Equation 2.32).

Figure 2.4 drawed by Shirley shows the moisture concentration evolution during reflow with exposure time and the distance from external ambient [3]. A 0.2 cm slab of molding compound with a cavity of width 0.01cm is preconditioned at T_0 = 85 °C and H_0 = 85 % for enough time to reach equilibrium, then exposed to step reflow for T_1 = 215 °C and H_1 = 0.1 %. The moisture concentration evolves with time according to Equation 2.31.

- At the beginning of heating, moisture flows into cavity, and the cavity moisture concentration μ increases.

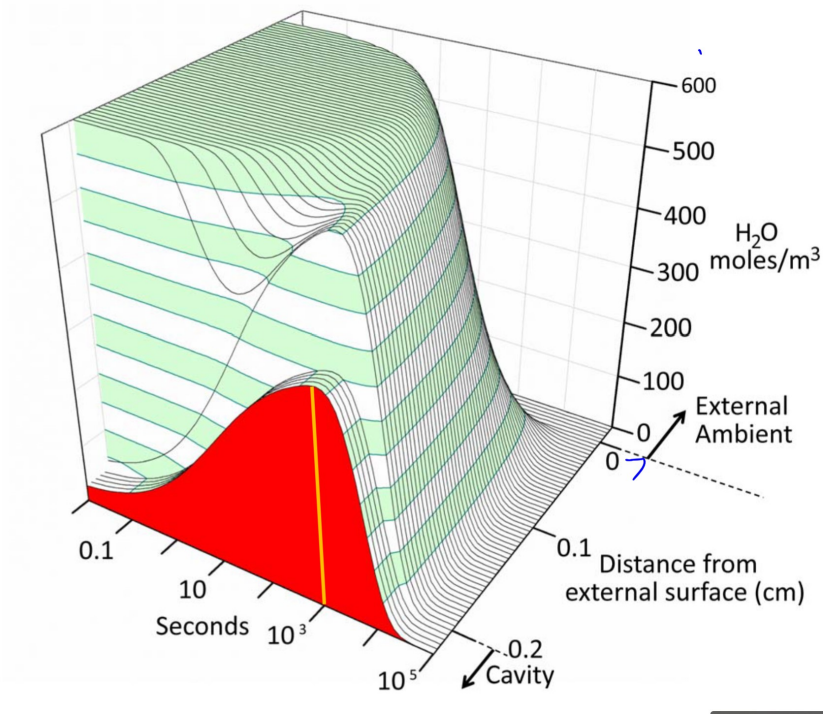


Figure 2.4: Evolution of molar concentration of water in a **0.2 cm slab of molding compound** and a **0.01 cm cavity** preconditioned at $T_0 = 85°C$ and $H_0 = 85\%$ for enough time to reach equilibrium, then exposed to step reflow for $T_1 = 215\,°C$ and $H_1 = 0.1\%$ [3].

- Then cavity moisture concentration reaches peak after time t_{peak}.
- Moisture flow out to external ambient through drying molding compound, cavity moisture concentration μ falls to equilibrium value with the reflow ambient.

The yellow line shows t_{peak} where maximum concentration μ_{max} achieved inside the cavity.

The cavity pressure can be then computed by Equation 2.32 with the moisture concentration. Figure 3.3 from Shirley shows the evolution of cavity pressure for a molding compound with a certain thickness (0.2 cm) as a function of cavity size with exposure time. The cavity pressure evolution with time is similar with moisture concentration:

- Cavity pressure first increases to maximum P_{max} with the moisture gradually diffuse into the cavity, then decreases when moisture vapor escaped to reflow ambient.
- Cavity pressure rises more quickly to maximum P_{max} with smaller cavity size (blue line in Figure 3.3).

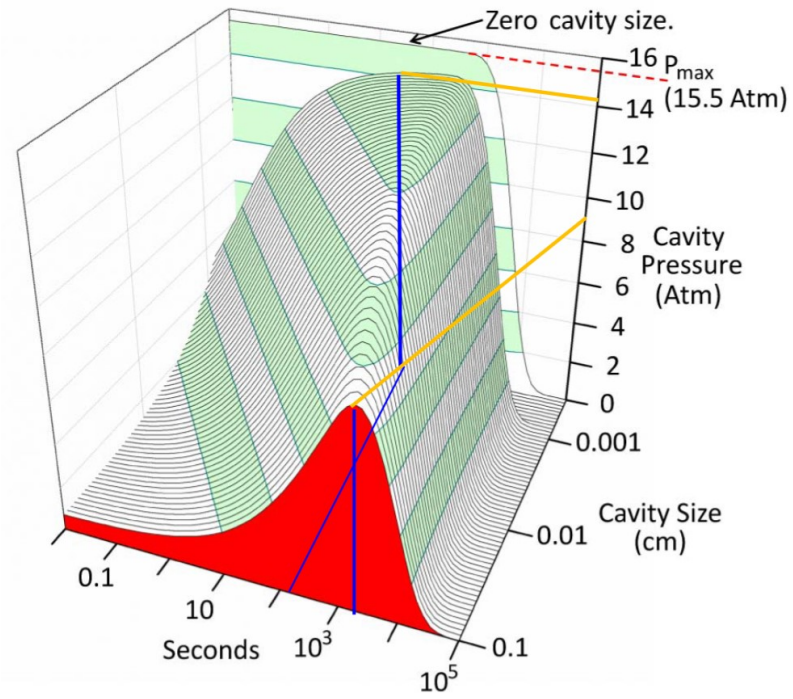


Figure 2.5: Evolution of cavity pressure in a **0.2 cm slab of molding compound** and **various cavity size** preconditioned at T_0 = 85 °C and H_0 = 85 % for enough time to reach equilibrium, then exposed to step reflow for T_1 = 215 °C and H_1 = 0.1 %. Limit (P_{limit}) at zero cavity size [3].

- Maximum cavity pressure P_{max} increases with cavity size decrease; P_{max} reaches limit maximum possible pressure P_{limit} when there is no cavity (yellow line).

The limited possible pressure P_{limit} for zero cavity size can be derived by Equation 2.31 and Equation 2.32 for $h \to \infty$:

$$P_{limit} = \frac{\mu_0}{S_1} \tag{2.34}$$

$$= H_0 P_s at(T_0) \frac{S_0}{S_1} \tag{2.35}$$

$$= H_0 P_s at(T_0) exp[\frac{Q_m}{R}(\frac{1}{T_0} - \frac{1}{T_1})] \tag{2.36}$$

The limited vapor pressure P_{limit} can be regarded as the vapor pressure inside the molding compound, and is:

- Independent of H_1. Reflow ambient humidity only determines the equilibrium state and will not influence pressure limit.

- Strongly dependent on T_1. Reflow temperature is the most decisive factor of pressure limit.

- Proportional to H_0. Preconditioning humidity determines how much moisture trapped in the molding compound, therefore determines the pressure generated by moisture vaporization.
- Weakly dependent on T_0. Precondition temperature has a week influence on the saturated moisture concentration in molding compound when exposed to a certain precondition humidity.

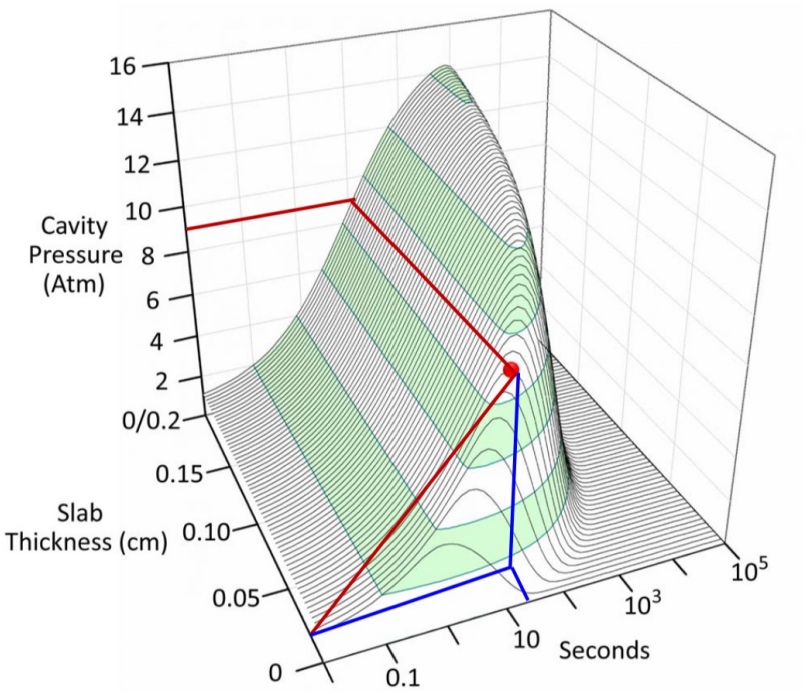


Figure 2.6: Evolution of cavity pressure in a **0.01 cm cavity** and **various molding compound size** preconditioned at $T_0 = 85°C$ and $H_0 = 85\,\%$ for enough time to reach equilibrium, then exposed to step reflow for $T_1 = 215\,°C$ and $H_1 = 0.1\,\%$.The dot shows the slab thickness (0.02 cm) which just reaches the example damage threshold of 9 Atm in 13 seconds [3].

Figure 2.6 by Shirley shows a the evolution of cavity pressure for fixed cavity size (0.01cm) as a function of molding compound thickness. Simple conclusion can be drawn from the figure that, the thinner themolding compound, the earlier and lower is the peak pressure.

Vapor pressure model distribution simulation

On basis of the theories developed in the many articles, simulations were carried out to verify thermal, moisture and stress distributed in electrical components. The distribution of moisture vapor pressure is essential for measurement device design. Whole field vapor pressure distribution before delamination in different packages and contributing parameters such as moisture concentration was modeled by Tee [1, 30]. An comprehensive approach to model the quad flat non-lead (QFN) package

stress [1] provides both analytical models for different stress compositions mentioned in Figure 1.2 and also simulation discussions. Simulation of moisture, thermal, and vapor pressure distribution and evolution are present systematically with integrated stress analysis. The vapor pressure distribution is concluded in the article based on the micro-mechanics model mentioned earlier. The integrated stress modelling of QFN package (Figure 2.7) was established. The vapor pressure model is related to moisture and thermal behavior of molding compound as shown in Figure 1.2.

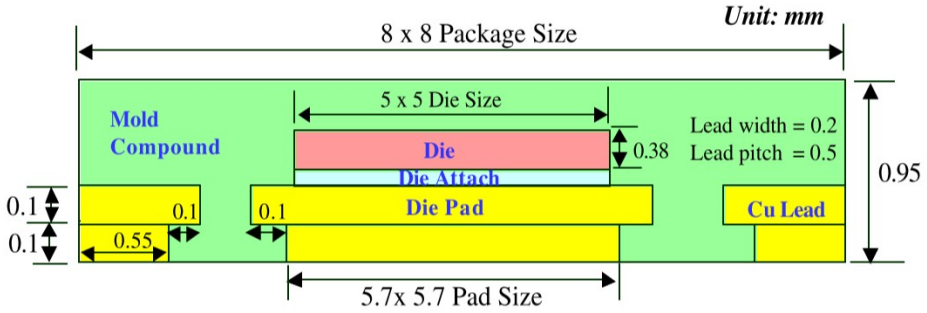


Figure 2.7: Schematic of typical QFN package [1].

The study of thermal diffusion is needed for both understanding the mechanism and design of the sensor. We need to consider the temperature distribution inside electrical components. And the sensor needs to reach the highest possible temperature during reflow. Figure 2.8a shows the heat distribution after 5-minutes temperature rise from 25 °C to 220 °C. The internal package reaches a uniform temperature within a few seconds. Figure 2.8b shows the moisture distribution of QFN package

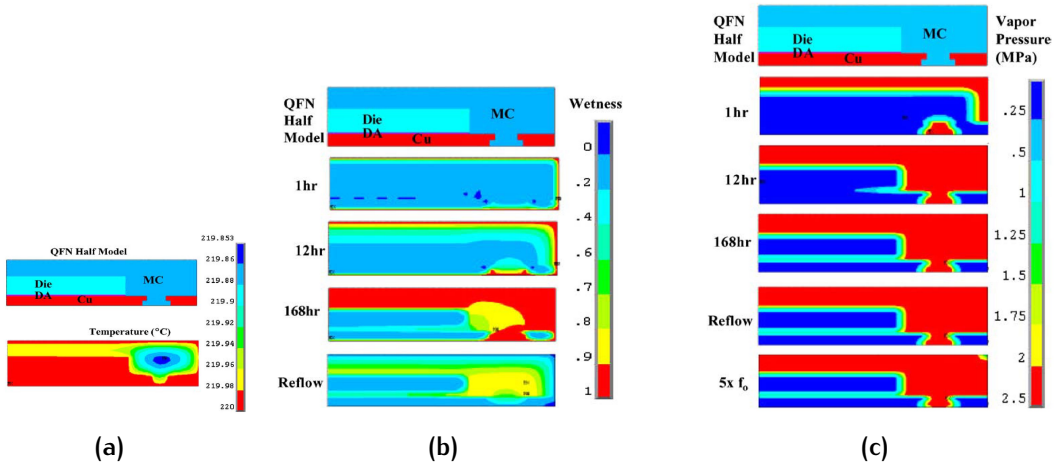


Figure 2.8: Simulation results adapted from Tee's work. (a) Package temperature distribution during reflow; (b) Transient moisture distribution in QFN package model; (c) Vapor pressure distribution after 5-minute' reflow with different time of precondition [1].

with different precondition period and after 5-minutes reflow. The precondition

environment is set as LEDEC level 1, which is 85 °C and 85 % relative humidity. Moisture is fully saturated after 168 hours of preconditioning. During reflow, the external package surface loses a significant amount of moisture due to high moisture desoption rate. The moisture diffusivity is a few orders higher at the reflow tmeperautre than precondition temperature. Moisture concentration in the interior of the package is almost unchanged at the die/mold compound interfaces. Figure 2.8c gives the vapor pressure distribution with different preconditioning time. The vapor pressure reaches saturated pressure at reflow temperature with only 12h of moisture preconditioning under 85 °C 85 %RH. The highest vapor pressure can be seen in the simulation as 2.5 MPa (25 bars). When adding an initial crack of 0.1 mm at the die corner, vapor pressure fills up the cavity quickly, and saturated vapor pressure of 2.32 MPa is generated to open-up and extend the crack length [30].

2.1.5 Conclusion and consideration

In this section, the popcorn failure mechanism was studied by reviewing previous researches. The mechanism and theories of vapor pressure generation provide an essential reference for pressure sensing device design in this application. Critical requirements can be summarized for the vapor pressure measurement. The measurement device should be able to survive and measure vapor pressure up to a few MegaPascals. The device's operating temperature is restrained by reflow temperature, which could be as high as 300 °C. The structure of the sensor should also be carefully designed for the measurement results to reflect real-time vapor pressure value generated by moisture in the molding compound. Considerations such as the ability to implant molding compound, experiment flow, or even real-time vapor pressure measurement in the reflow machine for future improvement can also be extracted based on the theories. In the next section, suitable pressure sensors will be searched to meet the requirements based on vapor pressure generation theories. The literature also provides a reference for future data comparison. Further design considerations will be discussed in the design section.

2.2 PRESSURE SENSORS

As mentioned in Section 2.1, vapor pressure measurement in molding compounds faces many challenges. With the mechanism of vapor pressure generation illus-

trated, the goal is to find a suitable measurement technique. Among all the pressure measurement instruments, pressure sensors are the most suitable for this application in certain aspects. The pressure sensor is a type of devices that first transduce pressure into other types of physical quantities such as mechanical strain, stress, and deformation.(mechanical domain) by pressure sensing elements like train gauge and deformable membrane. Then the physical quantities are converted to a readable output in the electrical domain, such as resistance change, capacitance change, etc.

Macroscopic mechanical based pressure transducers that convert pressure to mechanical displacement and use pointers to indicate pressure levels has been widely used for process control since the Industrial Revolution. Figure 2.9 shows some microscopic pressure sensor structures. These were the most common sensors used in industries at old times, especially in the harsh environment, because pure mechanism structures with mature materials and technologies provide reliable readings [4].

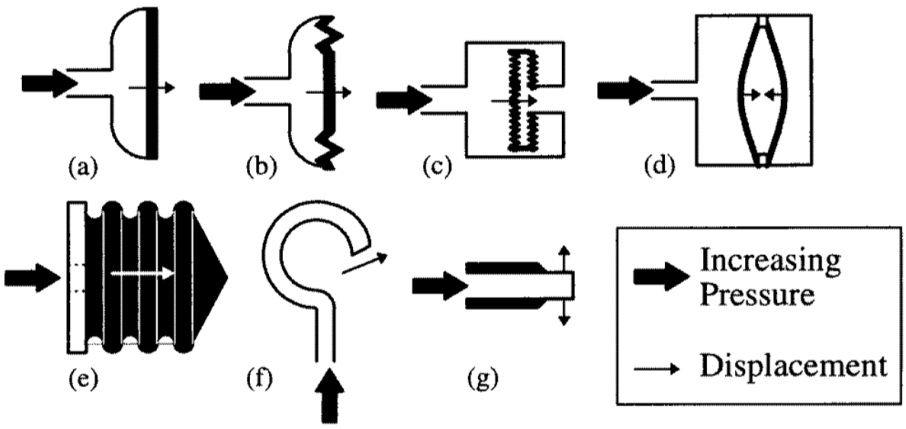


Figure 2.9: Macroscopic pressure sensors: (a) simple diaphragm; (b) corrugated diaphragm; (c) capsule; (d) capacitive sensor, (e) bellows; (f) Bourdon tube; (g) straight tube [4].

With the development of semiconductor technology, a variety of modern pressure sensors have been invented. Thanks to the evolution of IC technology, silicon abased MEMS smart pressure sensors took over the market because the advantages of small dimension, lightweight, high sensitivity, high reliability, low cost, ease of integration, and most importantly, the ability of inline measurement. Therefore, they are widely used in thousands of daily and industrial applications nowadays. MEMS pressure sensors sense pressure by not only deformation but also other mechanisms and finally give an electrical output. These characteristics enable the sensors to be implanted in IC design technology and manufacturing processes to carry out high-precision, automated pressure measurement, thereby enabling consumer electronics and industrial process control products to full automation and make MEMS pressure

sensor the most promising candidate in this project.

Pressure sensors are usually composed of pressure-sensitive components and signal processing units. Different sensing mechanisms can be selected to design pressure sensors according to specific measurement purposes, measured objects, and measurement environments. Therefore, pressure sensors vary drastically in technology, design, performance, application suitability, and cost in terms of applications. An overview of pressure sensors will be discussed in this section to find suitable sensing mechanisms, structures, materials, and process technology for vapor pressure sensing in molding compounds based on the previous research in failure mechanisms. Principles, materials, sensor structures, and possible process technologies of pressure sensors will be summarized. Important references will be illustrated in detail.

2.2.1 Pressure sensor principles

Different pressure sensors are used for different scenarios in terms of pressure ranges, measured medium, and types of operation. Several types of pressure sensors will be discussed later to find the most suitable mechanism in vapor pressure sensing requirement discussed earlier in Section 2.1.

(1) Pressure mechanism overview

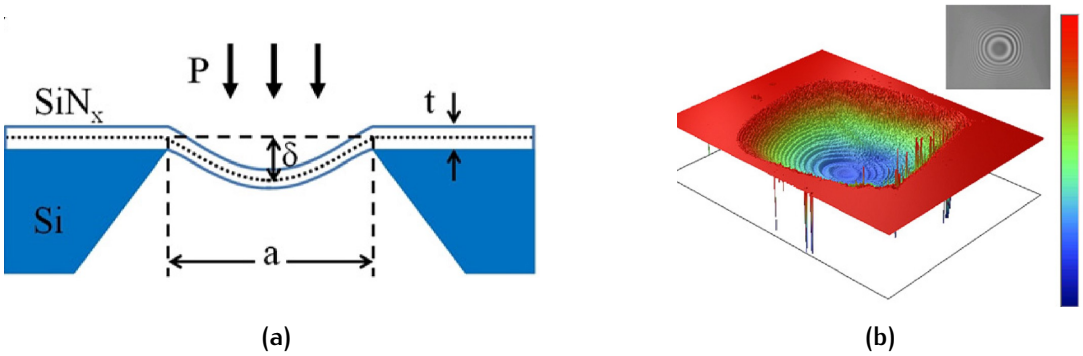
Pressure sensors can be classified by the transduction principle. Force collector is the most common type of pressure sensor, including strain gauges, Capacitive, electromagnetic, piezoelectric, optical, potentiometric, and force balancing pressure sensors. These pressure sensors are operated based on the deformation of mechanical structures due to the applied pressures and with a specific mechanism to translate the deformation to an electrical signal. Most force collector types of pressure sensors, especially for vapor/gas pressure sensing, use a suspended membrane as sensing elements. When pressure applies, the membrane deforms due to the pressure difference on two sides of the membrane, as shown in Figure 2.10a.

The shape of the membrane is arbitrary, but mostly circular and square. For a circular diaphragm slightly deformed, the deflection can be calculated by:

$$w(r) = \frac{Pa^4}{64D}[1 - (\frac{r}{a})^2)] \tag{2.37}$$

Where w, r, and a are respectively the displacement, the radial distance from the diaphragm's center, and diaphragm radius. D is the flexural rigidity, a material property, given by:

$$D = \frac{Eh^3}{12(1 - v^2)} \tag{2.38}$$



(a) (b)

Figure 2.10: Pressure sensing diaphragm example. (a) Schematic of suspended Silicon Nitride diaphragm under the applied pressure; (b) 3D deformation image of the membrane [31].

Where E is Young's modulus, h is the thickness of the membrane, and v is the Poisson's ratio. The pressure-deformation relation is linear for small deflection of circular diaphragms [32].

For square membrane, the applied pressure difference is related to deformation or mechanical strain by:

$$P = E\frac{h^4}{a^4}[g_1\frac{w_0}{h} + g_2(\frac{w_0}{h})^3] \tag{2.39}$$

Where $P[Pa]$ is the applied pressure, E is Young's modulus, $h[m]$ is the thickness of the membrane, a is the half of membrane width, $w[m]$ is the maximum deflection of the membrane in the center of square diaphragm. g_1 and g_2 are constant with Poison ratio v:

$$g_1 = \frac{4.13}{(1-v^2)} \tag{2.40}$$

$$g_2 = \frac{1.98(1-0.585v)}{1-v} \tag{2.41}$$

For the square diaphragm, the pressure P is linearly linked to maximum deflection w when the first term is much smaller than the second term ($g_1\frac{w_0}{h} \ll g_2(\frac{w_0}{h})^3$) [8].

Other types of pressure sensors use different parameters changed with pressure, for example, the change of thermal conductivity, change of gas ions, and change of resonant frequency. Both thermal conduction and ionization pressure sensors make use of gas properties. The thermal conduction types of pressure sensors detect changes in gas thermal conductivity under different pressure levels based on ideal gas law. The density of gases, which determines thermal conductivity, changes when pressure is applied [33]. The ionization pressure sensors (also named ion gauge) measure the number of charged gas particles inside a specific volume. The charged gas module per unit volume (density) changes when pressure changes. Electrons generated by electron generators accelerate and collide with gas modules, and a pair

of electron-ion is produced with collisions. The positive ions are received by the cathode and electrons received by the anode. The number of ions generated due to collision is translated into the electrical output on the cathode. When the pressure increases, the number of ionized module increases due to a change of density [34]. Thermal conduction and ionization pressure sensor are usually used to measure gas or vapor pressure at a low-pressure range, mainly vacuum pressure because their operation principle is based on characteristics of gas modules. Therefore, they are not suitable for this project due to the required high vapor pressure range in this application.

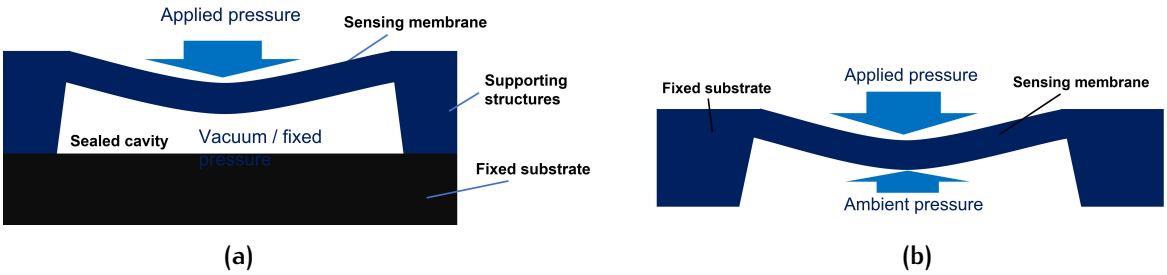


Figure 2.11: Simple schematic of (a) abosolute pressure sensor; (b)differential pressure sensor.

All pressure sensors can be grouped into two categories, absolute and differential. Absolute pressure sensors (Figure 2.11a) compare the measured pressure to an absolute vacuum or a fixed pressure. A reference sealed cavity is usually designed between sensing elements and fixed supporting structures. The absolute pressure sensors are used in applications that require a constant reference, such as biomedical systems, industrial process measurement and control, and environmental monitoring [35]. Differential pressure sensor (Figure 2.11a) measures pressure differences of two sides of the sensing elements. This type of sensor is widely used in many applications such as flow rate measurement, fluid level detection by measuring pressure difference.

After tranduced from pressure to physical mechanical parameters by pressure sensing elements, electrical elements translate the mechanical change into other signals that can be read out with various mechanisms. Several mechanisms that can be utilized in high vapor pressure measurement at a high temperature will be discussed following.

Piezoresistive pressure sensors

Since Smith discovered the piezoresistive effect in 1954, the semiconductor pressure sensors developed quickly. Nowadays, piezoresistive pressure sensors are the most popular type in the market for general purposes. This type of pressure sensor made use of the piezoresistivity property in some semiconductor materials like Silicon.

Piezoresistive pressure sensors work on the principle that the resistance changes due to the change in the effective mass of holes and electrons and the band diagram in the piezoresistive materials when pressure deforms the sensing structure. The resistance of a piezoresistive element is given by

$$R = \rho \times \frac{l}{A} \tag{2.42}$$

Where ρ is resistivity; l is the length of the resistor, and A is the area of the resistor. It should be noted that the area A perpendicular to the orientation of the current. In order to sense the deformation, piezoresistive elements will be implanted on the deforming parts as shown in Figure 2.12a. Resisance change is obtained by placing

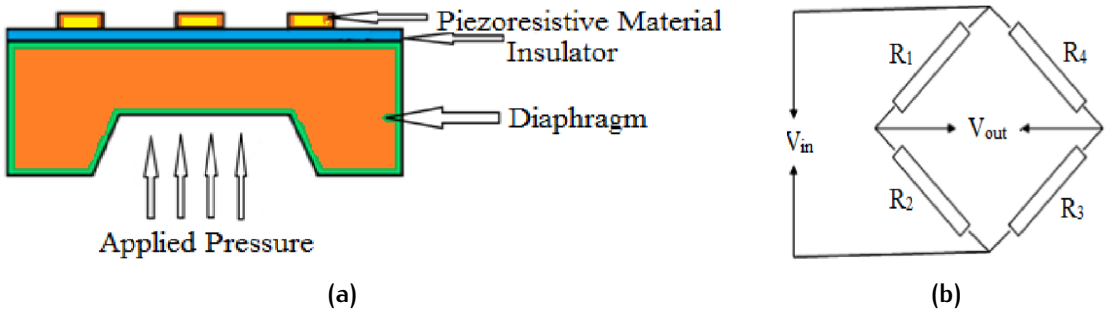
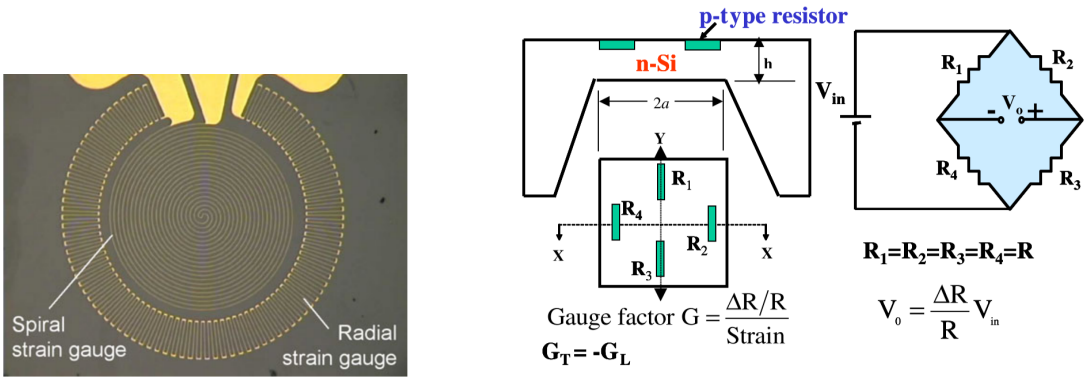


Figure 2.12: (a) The typical structure of the piezoresistive pressure sensors; (b) Wheatstone readout circuit [36].

strain gauges or piezo-resistors on top of the pressure-sensitive diaphragm , and gauges are usually connected in a Wheatstone bridge configuration (Figure 2.12b). When there is a pressure difference, the diaphragm bends, and an internal strain is generated in the attached piezoresistors, which alters its resistivity. By applying voltage to the input nodes of the Wheatstone bridge, the resistance change is translated into a voltage output.

Two common piezoresistive elements are metal strain gauges and semiconductor material in which a p-type region has been diffused into an n-type base [37]. Metal stain gauges are not precisely "piezoresistive sensors" because the change of resistivity in metal gauges is mostly due to the change of wire cross-section dimension. There are two types of metal resistance strain gauges: wire strain gauges and metal foil strain gauges. Usually, the strain gauge is tightly bonded to the mechanical strain matrix through a unique adhesive. When the matrix is subjected to a stress change, the resistance strain gauge also deforms so that the resistance value of the strain gauge changes, and then the voltage applied to the resistor changes. The resistance change of this strain gauge is usually small when it is stressed. Generally, this strain gauge is composed of a strain bridge, which is amplified by a subsequent instrument amplifier, and then transmitted to the processing circuit. Afterwards, the signal is sent to display or actuators. The resistance of the metal strain gauge changes slightly with deformation due to stress. Figure 2.13a shows a spiral



(a) (b)

Figure 2.13: (a) Strain gauge example: A strain gauges made of gold on a glass plate [38]; (b) Single crystal silicon piezoresistive pressure sensor [39].

and a radial strain gauge made of gold on a glass diaphragm [38]. Compared with metal materials, the sensitivity of semiconductor materials is dozens of times higher, which is determined by the piezoresistive characteristics of semiconductor materials. The piezoresistive properties of semiconductor materials also depend on the crystal's doping concentration and alignment direction. Figure 2.13b shows four p-type silicon resistors integrated on an N-type silicon membrane with a Wheatstone bridge connection. The resistance change ΔR due to mechanical strain ϵ in a rectangular conductor is:

$$\frac{\Delta R}{R} = (1 + 2\nu)\epsilon + \frac{\Delta\rho}{\rho} \tag{2.43}$$

The first term $(1 + 2\nu)\epsilon$ is the geometrical changes in resistivity due to stress, and the second term $\frac{\Delta\rho}{\rho}$ is the change in resistivity due to piezo-resistivity. In metal under stress, the first term is dominant; In semiconductors, the first term is neglectable, and the second term $\frac{\Delta\rho}{\rho}$ is dominant [40]. The stress σ on piezo-resistor is expressed by:

$$\frac{\Delta\rho}{\rho} = \pi\sigma \tag{2.44}$$

Where π is the piezo-resistive coefficient. The gauge factor, defined as the ratio of relative change in resistance to the strain, is determined by a piezoresistive coefficient and Young's modulus of the material E. For the same original resistance of R in the Wheatstone bridge, the gauge factor of structure in Figure 2.13b is obtained by

$$G = \frac{\frac{\Delta R}{R}(for R_1 = R_2 = R_3 = R_4 = R)}{Strain} = E\pi \tag{2.45}$$

With the output voltage and the gauge factor, the strain can be obtained, and then the pressure can be derived by Equation 2.37 [39].

Capacitive pressure sensors

The capacitive pressure sensor is another type of pressure sensor widely used in the market. The working principle of the capacitive pressure sensor is that the relative position of the capacitor plate will change with the pressure change, which will cause the change of the capacitance. The pressure measurement is realized through the measurement of the capacitance by the detection circuit. Figure 2.14 shows a typical MEMS capacitive pressure sensor. A substrate usually made of silicon or

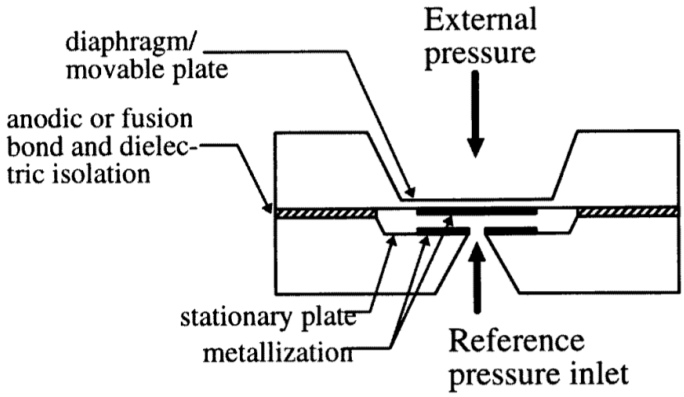


Figure 2.14: Cross section shcematic of a bulk-micromachined capacitive pressure sensor [4].

glass is isolated with a sensing diaphragm. A cavity sealed or connected to another reference pressure (typically atmospheric pressure) is generally made between the substrate and the sensing diaphragm. Two plates are bonded respectively to the diaphragm and the bottom of the cavity. The moving plate and the fixed plate form a capacitor. The capacitance C of parallel plate capacitor is

$$C = \frac{\varepsilon A}{d} \tag{2.46}$$

Where ε, A, and d are respectively the dialect permittivity, the plate area, and distance between the plates, when external pressure is applied on top of the diaphragm, a pressure difference is generated on both sides of the diaphragm. The diaphragm, along with the top plate, bends to the lower pressure side. The displacement $w(r)$ causes the change of capacitance [41]. Similar with circular diaphragm mentioned earlier this section in Equation 2.37. The capacitance after deformation is then:

$$C = \int\int \frac{\varepsilon}{d - w(r))} r dr d\theta \tag{2.47}$$

where $w(r)$ is the deflection same as Equation 2.37. The applied pressure can be then calculated.

Optical pressure sensor

Optical pressure sensors sense the strain on pressure sensing diaphragms by the relation between displacement and light properties. Several approaches such as to measure the change of Fabry-Perot cavity height due to diaphragm deflection with optical spectrum modulation [42], using the photoelastic effect to modulate the light proportion input fibers to output fibers [43], or detect the interference of resonant frequency for optically excited vibrating elements [44].

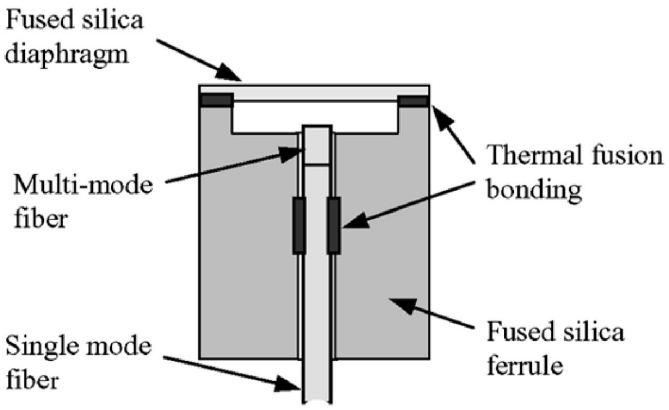


Figure 2.15: Structure of an optical fiber pressure sensor [5].

An example of an optical fiber pressure sensor is shown in Figure 2.15. The base and sensing diaphragm is made of fused silica, which can operate under high temperatures up to 700 °C. When the pressure is applied to the top of the diaphragm, the diaphragm will deflect. Thus, the height of the air cavity (Fabry-Perot cavity) will decrease. The light injected into the fiber propagates perpendicular to the diaphragm and will be partially reflected by the bottom surface of the diaphragm and the end of the optical fiber. These two reflections propagate back and generate interference fringes through the fiber. Then the change of cavity height can be calculated by the characteristic of the interference fringes [5].

The reflectance R can be calculated by the refractive index n_{silica} and $n_{fiber-end}$, the wavelength of input light Λ and the cavity depth h, the reflectance R:

$$R = \left| r_1^+ + \frac{t_1^+ t_1^- r_2^+ e^{i\phi}}{1 - r_1^+ r_2^+ e^{i\phi}} \right|^2 \tag{2.48}$$

Where

$$
\begin{aligned}
r_1^+ &= \frac{n_{fiber-end} - 1}{n_{fiber-end} + 1} \\
t_1^- &= \frac{2}{n_{fiber-end} + 1} \\
r_2^+ &= \frac{n_{silica} - 1}{n_{silica} + 1} \\
t_1^+ &= \frac{2n_{fiber-end}}{n_{fiber-end} + 1}
\end{aligned}
\tag{2.49}
$$

and

$$
\phi = \frac{2\pi(2h)}{\lambda_0} \tag{2.50}
$$

The reflected light intensity R varies with the cavity depth h as Equation 2.48. By measuring the reflected light intensity or the interference, we can also get the deflection [45].

The applied pressure P is then calculated by the center deflection y when $y_{max} \leq 0.3h$ (for circular diaphragm):

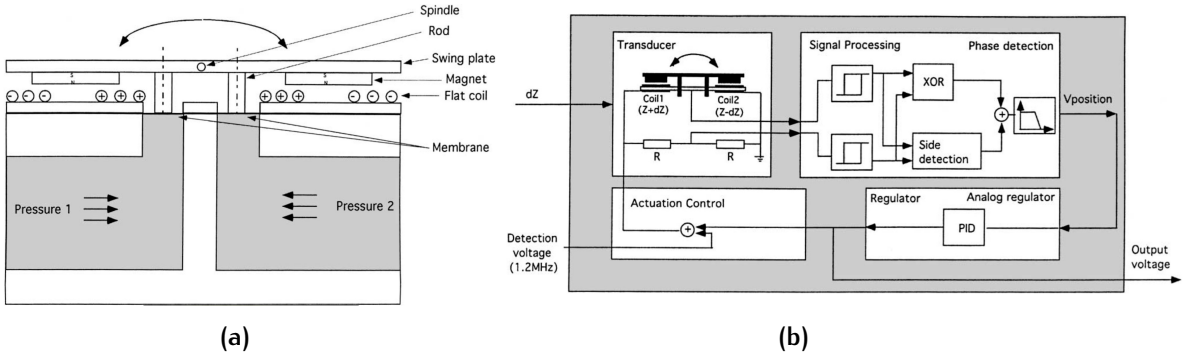
$$
y = \frac{3(1-\mu^2)P}{16Eh^3} r^4 \tag{2.51}
$$

Where μ, h, r, and E are respectively the Poisson's ratio, the thickness and the effective radius, and Young's module of the diaphragmm [46].

Electromagnetic pressure sensor

The electromagnetic pressure sensors translate the displacement of the diaphragm due to pressure to electric output by changes in inductance (reluctance), LVDT, Hall Effect, or eddy current principle. An example of an electromagnetic pressure sensor is given in Figure 2.16a. It's also a **force-balancing** types of sensor.

The system schematic of this sensor is given in Figure 2.16b. The measured pressure and the reference pressure respectively cause deflection on two membranes. The pressure difference makes the membrane bend in different displacements. A plate supported by the two membrane swings because of the different positions of the membranes. Two magnets are bonded to the bottom of the plate. When the plate swings, the magnets move relative to the flat coils placed on top of the substrate and modify the impedance of the coils. The phase shift due to the impedance change will be measured by a Wheatstone bridge and transformed to the voltage output. Then a compensation voltage is generated by a PID controller and fed back to the coils. The magnetic field generated by the coil acts with the magnets and produces a force to drive the plate back to its original position. The compensating



(a) (b)

Figure 2.16: (a) An example Schematic of a differential electromagnetic pressure sensor based on force balancing principle; (b) The system diagram of the electromagnetic pressure sensor including feedback [47].

voltage is proportional to the input pressure difference. Therefore, the pressure can be derived after the calibration of this device [47].

Piezoelectric pressure sensors

Piezoelectric pressure sensors make used of piezoelectric effect of materials which generate electrical charges when pressure is applied. Therefore, piezoelectric pressure sensors are active devices. When pressure is applied, the sensing structure deforms so that generated mechanical stress polarizes the piezoelectric sensing element and yields a proportional electric charge as output [48].

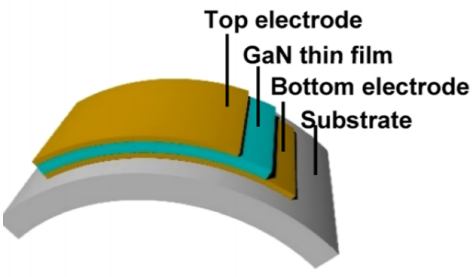


Figure 2.17: Schematic structure of a GaN thin-film piezoelectric generator (PEG) [6].

The piezoelectric pressure sensor uses piezoelectric materials as a sensing diaphragm. Figure 2.17 shows an example of a piezoelectric diaphragm. Two electrodes are bonded to both sides of the GaN thin film on the substrate. The transduction mechanism from mechanical strain to electric output shows in Figure 2.18. When the diaphragm bends because of applied pressure on its surface, the polarization of GaN generates electricity, and electrons flow from one electrode to another. The

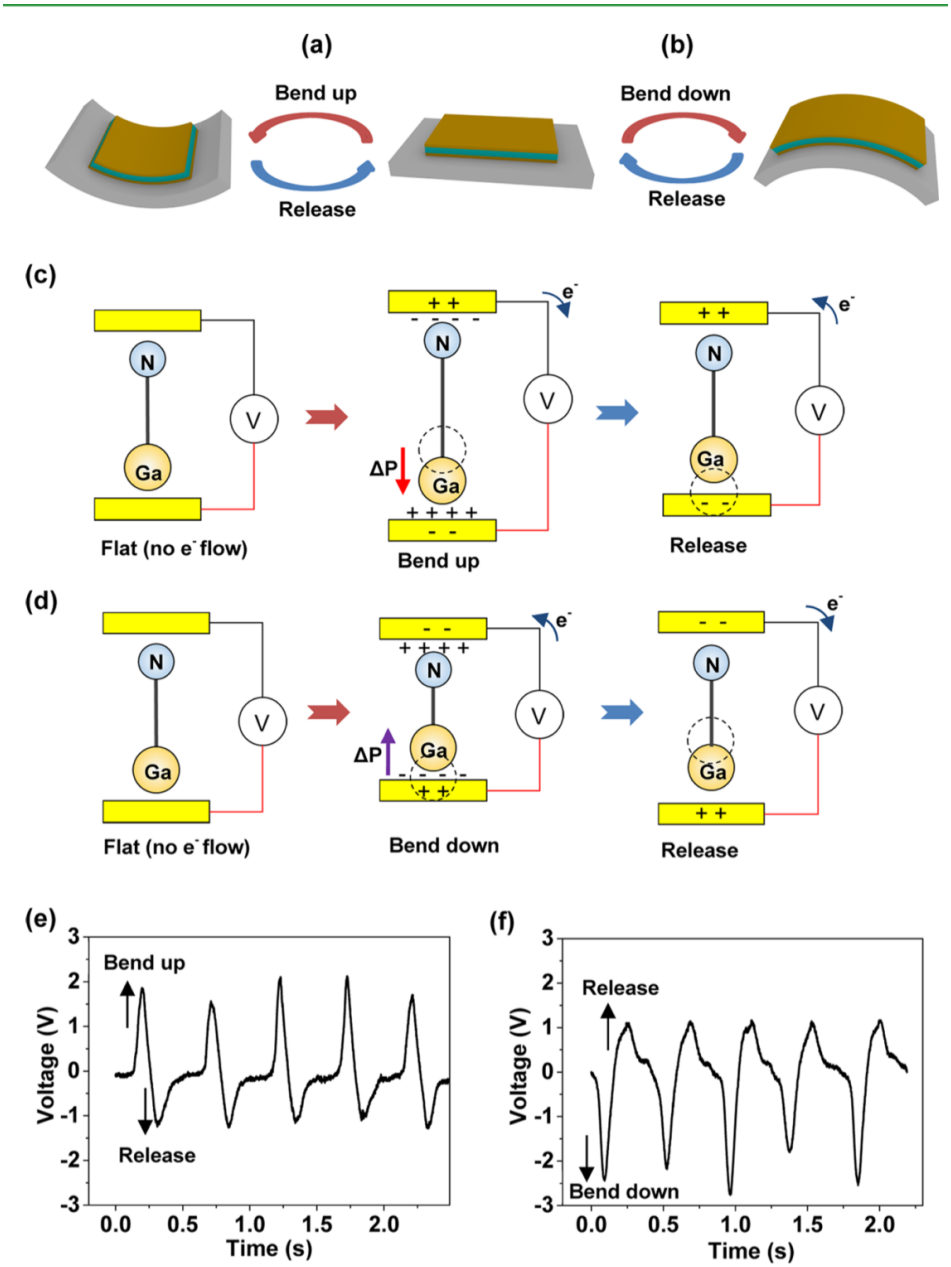


Figure 2.18: Principle of piezoelectric diaphragm translate mechanical strain to output voltage: (a) bend up-release and (b) bend down-release processes. Polarization induced electricity during (c) bend up-release and (d) bend down-release processes. Corresponding voltage response during repeated (e) bend up-release and (f) bend down-release processes by human fingers, with positive input (red) of electrometer connected to Ga-face electrode and negative input (black) connected to N-face electrode, with a load resistance of 1 $M\Omega$ (adapted from [6]).

effective piezoelectric constant $\bar{e}$ and effective dielectric constant $\bar{k}$ is material properties. The output voltage will be:

$$V_{oc} = \frac{\bar{e}}{\bar{k}} \delta t_T \tag{2.52}$$

The potential change detected reflects the degree of mechanical strain. Then the applied pressure can be derived based on Equation 2.37 [6].
An overall formula is given by [49]:

$$V_{out} = \frac{\sigma A}{C} = \frac{e\frac{P}{E}A}{\frac{k\varepsilon_0 A}{t}} = \frac{ePt}{k\varepsilon_0 E} \tag{2.53}$$

Where The output potential V_{out} is related to surface charge density σ, surface area A, and capacitance C. The applied pressure P can be calculated with the elastic modulus E, the dielectric constant k, thickness of film t, piezoelectric coefficient e, and strain σ.

Force-balanced pressure sensors

The force-balanced type of pressure sensor uses feedback external force such as electromagnetic force [47] and electrostatic force [7] to balance the diaphragm deformation due to applied pressure. The closed-loop configuration of an electrostatic force-balanced pressure sensor is given in Figure 2.20. Firstly, a pressure sensor transforms the pressure to displacement and produces an electrical output after amplification. Then the output signal is processed and drives an actuator to generate a force to compensate for the displacement, driving the sensing element to its original position. The measured pressure can be derived based on the given compensation force and voltage. This method is frequently used for the calibration of pressure sensors [50].

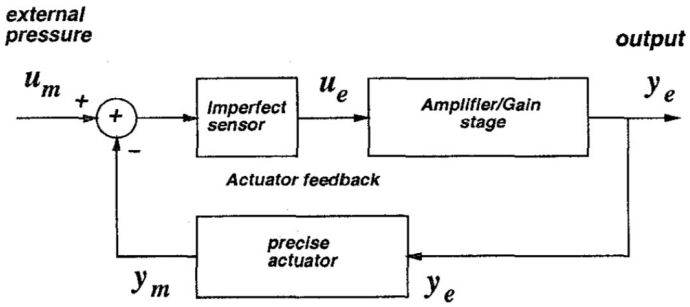


Figure 2.19: The closed loop configuration of the force-balanced pressure sensor [7].

One example of an electromagnetic force-balanced sensor is illustrated at Figure 2.19. Another example of an electrostatic force balanced sensor is shown in Figure 2.20. This sensor is made of three plates and two outputs. The force balancing a plate and the fixed restoring plate forms a parallel plate electrostatic actuator. The cavity is sealed in a vacuum environment. When pressure P_0 is applied to the sensing diaphragm, the connected force balancing plate will bend with the diaphragm. The

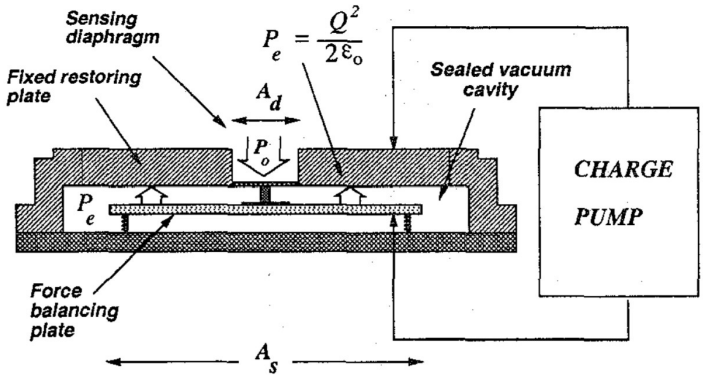


Figure 2.20: Multiplying force balancing scheme for low voltage pressure sensing with hermetically sealed actuator [7].

charge pump generates charges with a charge density of Q on the plates and results in an electrostatic pressure of :

$$P_e \approx \frac{Q^2}{2\epsilon_o} \tag{2.54}$$

With force balanced relation of :

$$P_e A_d = P_0 A_s \tag{2.55}$$

The pressure P_0 can be derived by the driving voltage of the electrodes:

$$V_{drive} = \sqrt{\frac{2P_0 A_s}{\epsilon_o A_d}} h_0 \tag{2.56}$$

Where h_0 is the actuator plate gap [7].

Resonant pressure sensor

The resonant pressure sensors measure resonant frequency change due to the stress or deformation of sensing elements under applied pressure. The change of resonant frequency can be measured by the methods introduced above. Resonators are used in this type of sensor to generate vibration to pressure sensing elements such as membranes or beams. When the pressure is applied, the resonant frequency changes due to the internal strain of particular material.In this way, the pressure is related to the frequency that can be detected.

Figure 2.21 present a piezoelectric bimorph static pressure sensor. A circular piezoceramic membrane is assembled on a steel base. The membrane consists of two thin disks, which are made of piezoelectric ceramic PZT and metal bonded by epoxy resin (Figure 2.21b). A circular chamber is etched on center of the base (Figure 2.21a). When applying an ac electric field with two electrodes on the membrane,

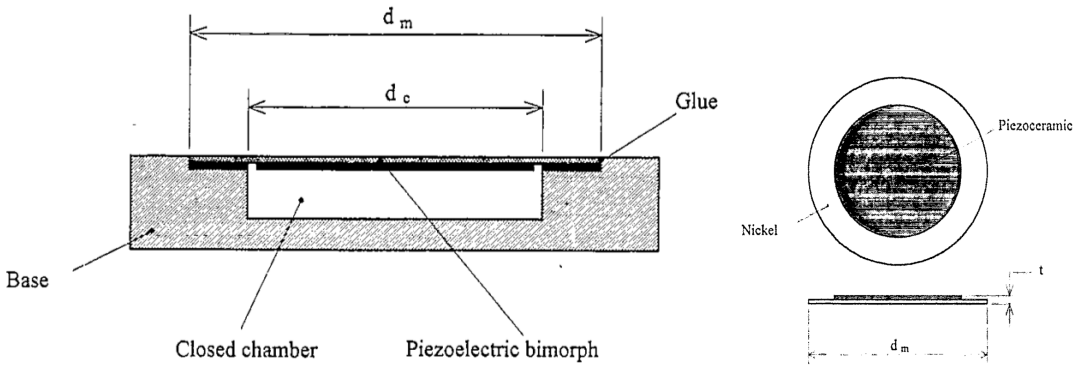


Figure 2.21: Piezoelectric bimorph static pressure sensor: (a) Cross-section of sensor structure; (b) Bimorph membrane as an active element [51].

the membrane will start vibrating. The resonance frequency of the membrane can be calculated:

$$f = \frac{2\lambda^2}{\pi d_c^2}\sqrt{\frac{\bar{E}t^3}{12(1-\bar{v}^3)\bar{\rho}}} = \frac{2\lambda^2}{\pi d_c^2}\sqrt{\frac{\bar{D}}{\bar{\rho}}} \tag{2.57}$$

Where t, d_c, $\bar{E}$, $\bar{v}$, and $\bar{\rho}$ are respectively the thickness of the diaphragm, the diameter of the chamber, Young's modulus, Poisson ratio, and weight to surface ratio [51].

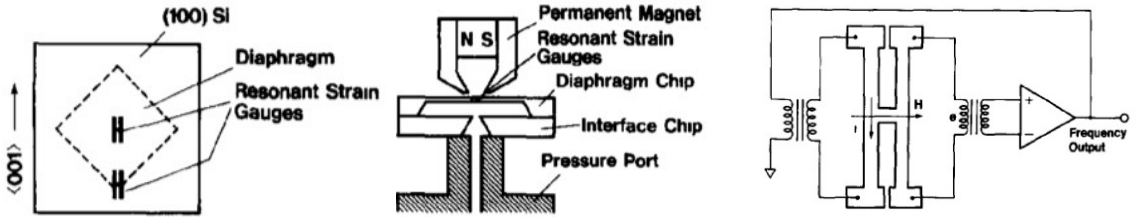


Figure 2.22: An example of a resonant strain gauge (a) Strain gauges on the diaphragm (b)Construction of the resonant pressure sensor; (c)Schematic of the resonator [52].

Strain gauges are sometimes bonded on the surface of the diaphragm to increase sensitivity. Figure 2.22a shows two train gauges with four ends bonded on the diaphragm inside a vacuum cavity. A resonator composed of the two strain gauges and an oscillation circuit is excited by an alternating output current feedback circuit. It generates fixed vibration on the strain gauges (Figure 2.22c). When pressure applies, the natural frequency of each strain gauges changes differently due to strain.

Then pressure can be obtained by the frequency difference with a third-order equation:

$$P = A(\frac{f_c}{f_{c0}} - \frac{f_r}{f_{r0}})^3 + B(\frac{f_c}{f_{c0}} - \frac{f_r}{f_{r0}})^2 + C(\frac{f_c}{f_{c0}} - \frac{f_r}{f_{r0}}) + D \tag{2.58}$$

Where f_{c0} and f_{r0} are respectively the center gauge reference frequency and corner gauge reference frequency, f_c and f_r are respectively the center gauge frequency and corner gauge frequency after pressure applied. A to D are calibration constants [52].

2.2.2 Pressure sensing structures and materials

During the reflow process, the temperature is relatively high, and the pressure caused by moisture vapor reaches dozens of times the atmospheric pressure. Therefore, the sensor is required to have good tolerance or isolation to the harshness. Apart from the requirement from the failure parameters, the limitation of accessible tools should also be considered for the choice of sensing technology.

Firstly, type of pressure reference is selected. As earlier stated, absolute pressure sensor has relatively high stability and accuracy. However, the dynamic range is smaller for high-pressure measurement due to the larger pressure difference on the two sides of the membrane. Differential pressure sensors are relatively easy to design and fabricate compared to absolute sensors. However, the output of differential sensors is dependant on the ambient environment, so accuracy is compromised [53]. Therefore, absolute pressure sensors are more suitable for this project due to the potentially varied ambient environment.

From the characteristics of different types sensing mechanisms presented earlier in Section 2.2.1, types of transduction mechanism suitable for this application can be selected. Firstly, several sensing mechanisms can be excluded due to several reasons. Piezoelectric devices are reported with excellent long-term stability, high sensitivity, high dynamic range, high-temperature range, and low power consumption [54]. No external power source is needed to drive the device makes it suitable for power limited pressure measurement. However, piezoelectric devices are not suitable for static pressure measurement because the electric charge will only generated during pressure changes. Considering the vapor pressure change in the molding compound during reflow does not have a rapid dynamic change, the piezoelectric mechanism is excluded from the selection. Attributes of possible mechanism is listed in Table 2.3

Table 2.3: Attributes of usable pressure sensing mechanism.

Attributes	Piezoresistive	capacitive	Optical	Resonant	Force-balanced
Sensitivity	Good	Good	Excellent	Good	Fair
Dynamic Range	Good	Fair	Excellent	Good	excellent
Dimension	Excellent	Excellent	Poor	Fair	Fair
Complexity	Low	Medium	High	Medium high	medium high
High-temp compatible	Up to material	Fair	Excellent	Poor	Poor
Temperature dependency	High	Low	None	Medium	Medium
robustness	Fair	Good	Excellent	Fair	Poor

Optical fiber-based pressure sensors are suitable for remote monitoring and have high sensitivity, high accuracy, and are independent of environment temperatures, making them a good choice for vapor pressure sensing in molding compounds. However, optical sensors require an additional light source, optical sensors, light modulation, optical fiber, which lead to a more complex system. Similar to force-balanced and electromagnetic pressure sensors, system complexity is the biggest problem for the design of vapor pressure sensing systems regardless of their excellent performance in high-pressure range sensing.

Piezoresistive and capacitive pressure sensors are commonly used in many applications because of their relatively smaller and simple fabrication, larger bandwidth, higher sensitivity, and compatibility for IC integration. More importantly, both piezoresistive and capacitive MEMS sensors have relatively simple structures and can be fabricated using the tools in the Else Kooi Lab (EKL). Therefore, piezoresistive and capacitive devices are considered in this project. Previous works involving piezoresistive and capacitive pressure sensors with similar requirements such as high-temperature and high-pressure environment provides reference for the moisture vapor pressure sensor design.

SiC piezoresistive pressure sensors for harsh environment

As discussed earlier, piezoresistive pressure sensors transduce mechanical stress to change in electrical resistance. They can be used not only for pressure sensors but also other sensors that turn the measurand into mechanical stress in academic research and commercial products. By selecting materials, designing structures, and fabricating with proper techniques, piezoresistive pressure sensors can be adapted for pressure sensing in many applications.

Varieties of materials give different characteristics to the pressure sensors. Silicon has excellent strength and mechanical properties and has the advantages of overvoltage capability and low hysteresis compared over most metals. The use of a silicon diaphragm can significantly improve the dynamic response performance of the sensor and reduce the sensitivity to acceleration. Silicon-based piezoresistive pressure sensors using surface micro-machining processes occupied major applica-

tions in the market. Silicon as a piezoresistive material has the advantage of high sensitivity, reproductivity, and mechanical stability because of its mono-crystalline structure [55]. However, silicon piezo-resistors have a vital problem of junction leakage at a temperature higher than 125 °C makes it not an ideal material for higher temperature applications [56]. silicon On insulator (SOI) pressure sensors solved the problem of leakage current by isolating the piezo-resistor from the bulk with insulation film like silicon dioxide. Pressure sensors with piezo-resistor made on SOI wafer are able to have a better performance than traditional silicon pressure sensors up to a temperature of 350 °C [57]. However, the stability of high-temperature performance of SOI based sensor is still limited due to the limitations of Silicon piezoresistive elements.

In recent years, the piezoresistive effect on several semiconductors with a large bandgap, such as silicon carbide, gallium nitride (GaN), and diamond, has been studied and tested [58]. Among all the materials, SiC shows its advantage in harsh-environment compatible MEMS device not only because of its stable electrical property at high temperatures but also because of its excellent mechanical properties. Table 2.4 compares the properties of these materials. The fracture toughness of 3C-SiC on silicon was measured almost three times larger than silicon, and Young's modulus of SiC is also more than two times larger than silicon [59], making it a better material for pressure sensing diaphragm.

Table 2.4: Properties of several materials used in MEMS sensors (adapted from [15, 16]).

Properties	SiC	Si	Diamond	GaN
Energy gap (eV)	2.3(3C-SiC) to 3.4(2H-SiC)	1.12	5.5	3.4
Electron mobility (cm^2/Vs)	1000	1500	2200	900
Relative dielectric constant (F/m)	9.8	11.8	5.5 to 10	8.90
Young's modulus (GPa)	300 to 500	130 to 180	1000	200 to 300
Thermal conductivity ($Wcm^{-1}K^{-1}$)	5	1.5	20	1.3
Chemical Inertness	Excellent	Poor	Good but burn	Good
MEMS compatibility	Good	Excellent	Poor	Fair
Avaibility/Cost	Fair	Excellent	Poor	Fair

Several pieces of research have been done on SiC piezoresistive pressure sensors. Luke [8] presents an absolute pressure sensor using polycrystalline 3C-SiC fabricated by surface micromachining and integrated SiC CMOS readout on SiC substrate. An in-situ doped poly SiC diaphragm was designed as piezoresistive pressure sensing element. A sealed cavity with reference pressure is created by a polycrystalline 3C-SiC membrane deposited by low pressure chemical vapour deposition (LPCVD). The membrane consists of a stack of an intrinsic poly-SiC layer and a piezoresistive in-situ n-type doped poly-SiC layer. The piezoresistive layer will directly transduce the pressure-induced strain of the membrane into a resistance variation. Electrodes are patterned directly on top of the cavity at the maximum stress position of the membrane, enabling four-point resistance measurements. The

structure shows in Figure 2.23.

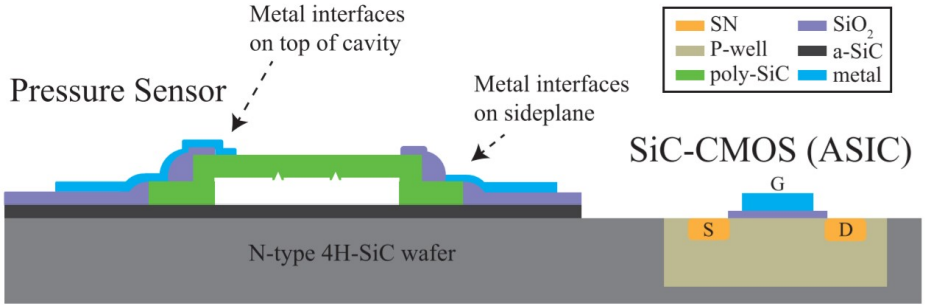


Figure 2.23: Monolithic integration of the designed MEMS pressure sensor with SiC-CMOS [8].

The device was also fabricated in EKL by Luke [8] illustrated in Figure 2.24. Electrically insulating layer using plasma enhanced chemical vapour deposition (PECVD) low-stress amorphous SiC is deposited for isolate the membrane and substrate and etch barrier of further steps. PECVD SiO_2 was deposited and etched a reactive ion etching (RIE) etcher to form a sacrifical structure for the vaccum cavity. An intrin-

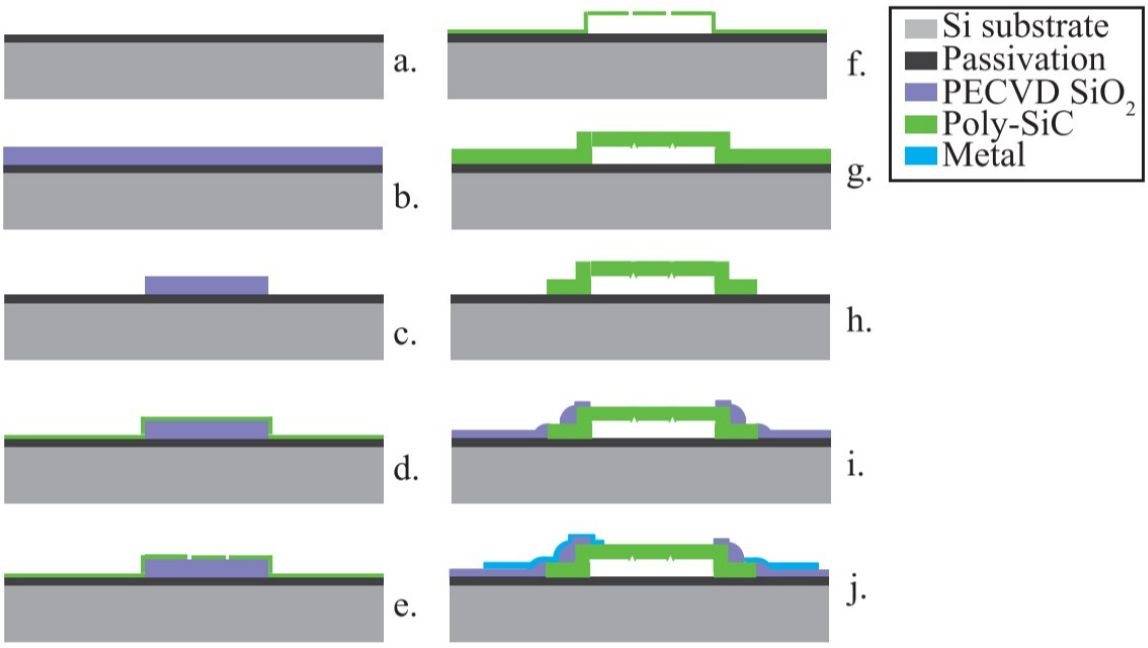


Figure 2.24: Fabrication process of the All-SiC selfsensing piezoresistive pressure sensor [8].

sic poly-SiC layer deposited in a hot-wall LPCVD furnace operating at 860 °C and 80 Pa with a bulk resistivity of 439.8 $\Omega \cdot$ cm is used as the first structural layer of the pressure sensing diaphragm. Oval-shaped release holes with a size of several

micrometers are etched on the first layer of the diaphragm by the deep reactive ion etching (DRIE) etcher for releasing of the sacrificial SiO_2. The width of holes is carefully designed to be at most half of the target thickness of the second SiC diaphragm deposition to ensure sealing of the cavities. The second doped poly-SiC layer is then deposited after the sacrificial layer is etched by vapor HF. NH_3 is added for deposition as an n-type dopant so that the layer itself is worked as a piezo-resistor and have a bulk resistivity of $0.02\,\Omega \cdot$ cm. A layer of SiO_2 was deposited on the wafers to isolate and passivate the functional SiC layer. SiO_2 was etched on the electrodes and top of the membrane (SiO_2 affects mechanical properties of poly-SiC membrane). Metal electrodes were designed for the largest resistance change in the diaphragm to be collected.

Gauge factor of -91 was reported by Luke [8]. However, the device was only tested under 20 °C. Higher temperature behavior was not tested. The thin-film poly-crystalline 3C-SiC used for pressure sensing prevents complex bulk micromachining and fits in back-end processing of SiC CMOS, and has the potential to be fabricated on different types of substrate (e.g., Si substrate). Because of the high cost of SiC wafers, substitution methods of using silicon wafers are explored.

3C-SiC is intended to fabricate on silicon substrate for a lower price. However, the lattice and thermal mismatches between silicon and 3C-SiC lead to high leakage currents at elevated temperatures. One proposed solution to isolate the 3C-SiC and Si interface is to use thin silicon-on-insulator (SOI) wafers as the substrate for 3C-SiC growth to carbonize the entire thin silicon later to create $3C - SiC/SiO_2/Si$ substrates. Then dielectrically isolated 3C-SiC piezo-resistors can be fabricated on silicon diaphragms. The problem in epitaxially grown SiC is that it cannot be completely converted, leading to hybrid SiC/Si piezo-resistors. Piezoresistive differential pressure sensors using poly 3C-SiC as sensing diaphragm fabricated with bulk etching of silicon substrate was reported by Wu et al. [60] to improve the method. Two approaches are discussed in the paper. The first one used phosphorus-doped atmospheric pressure chemical vapor deposition (APCVD) polycrystalline 3C-SiC for both piezo-resistors and sensing diaphragm. LPCVD SiN is used for electrical isolation between diaphragm and piezo-resistors. Another approach used epitaxially-grown unintentionally nitrogen-doped single-crystalline 3C-SiC piezoresistive fabricated on silicon membrane with thermally grown SiO_2 for electrical isolation.

Figure 2.25a shows the pressure sensor with poly-SiC piezo-resistors electrically isolated from poly-SiC diaphragm by LPCVD Si_3N_4 films fabricate with bulk micromachining of double-side polished (100) silicon substrate. Firstly, a 10-μm-thick poly-SiC film is deposited on the silicon substrate with APCVD. Then, a 0.2-μm-thick Si_3N_4 was deposited on the poly-SiC film by LPCVD as insulation between the SiC diaphragm and piezo-resistors. low-temperature oxide (LTO) was deposited as SiC lift-off sacrificial pattern. Then 0.5μm-thick poly-SiC film was deposited on the oxide SiC diaphragm to form piezo-resistors after sacrificial removal by HF. The SiC

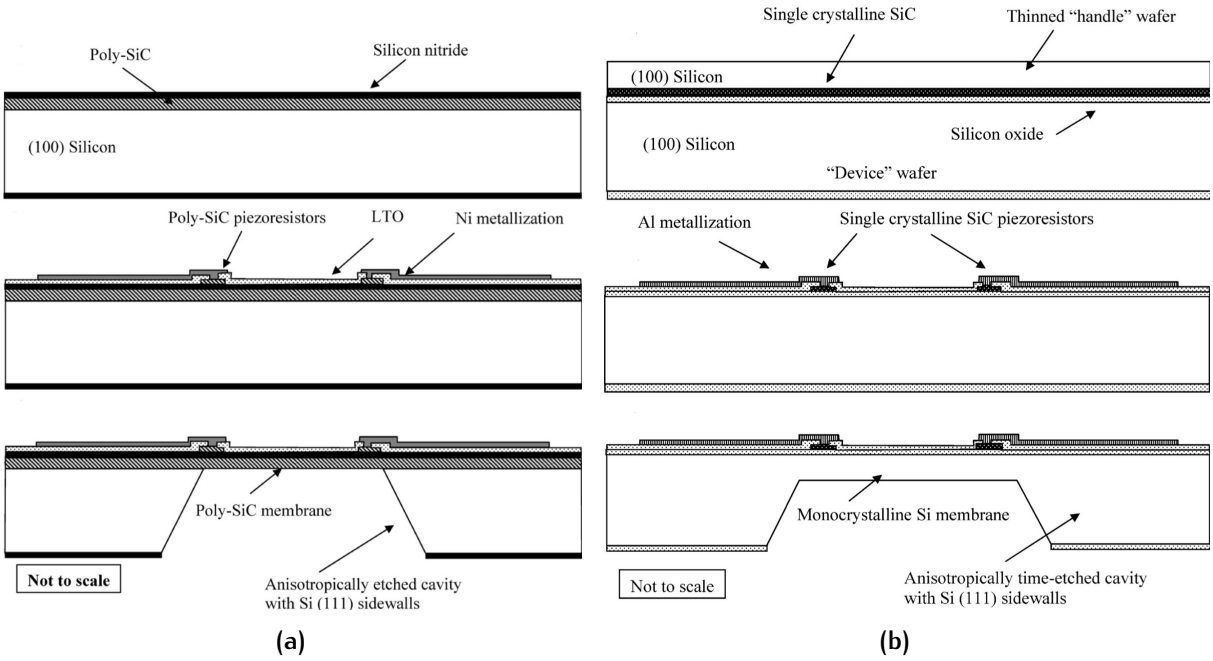
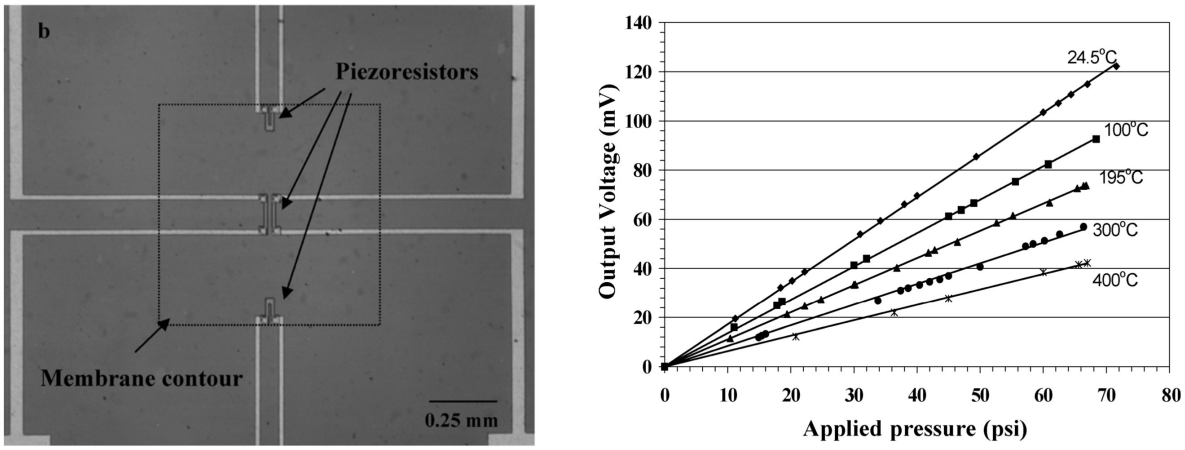


Figure 2.25: Cross-section schematic of fabrication process for pressure sensor on Silicon substrate with (a) poly-SiC piezoresistors on SiC diaphragm; (b) poly-SiC piezoresistors on Si diaphragm [60].

diaphragm was achieved by KOH etching of the Si substrate backside. This method achieved a highest gauge factor of -2.1 and sensitivity of 20.9 $-\mathrm{mV/V \cdot psi}$ at room temperature [60].

The second method with nitrogen-doped single-crystalline 3C-SiC piezo-resistors with 3C-SiC/SiO_2/Si substrate shows in Figure 2.25b. The single crystalline 3C-SiC piezo-resistor was achieved by heteroepitaxial growth on a "handle" silicon wafer by APCVD. An unintentional nitrogen-doped n-type SiC was formed due to the composition of gases in the deposition environment. Polysilicon was then deposited and completely oxidized to form SiO_2 layer on the SiC film. Thermal SiO_2 is also grown on another "device" wafer and processed to bond with the "handle" wafer. After KOH etching of silicon, a Si/SiO_2/SiC substrate with piezo-resistors on silicon diaphragm was processed. This method achieved a gauge factor of -18 at room temperature and -7 at 400 °C. The sensitivity is as high as 63.1 $-\mathrm{mV/V \cdot psi}$at a higher temperature of 400 °C. However, this method requires delicate, complex fabrication, and the operating pressure range is limited due to the properties of the silicon diaphragm.

Piezoresistive pressure sensors with these new technologies provided pressure measurement with a large dynamic range and good linearity. However, the piezoresistive effect has strong temperature dependency as shown in Figure 2.26b, this makes the piezoresistive coefficient varies with temperature change. Therefore, pressure measurement with temperature changes is critical for piezoresistive pressure sen-



(a) (b)

Figure 2.26: Single crystalline n-type doped 3C-SiC piezoresisor on Si diaphragm (a) Optical image of optimized piezo-resistor position; (b) Sensor output with 10V applied DC voltage vs pressure under different operating temperatures [60].

sors. Deviation of gauge factors from theoretical design to actual experimental results is reported in the article possibility because of the difference in doping type, dopant concentration, and crystal orientation [61].

High-temperature compatible capacitive pressure sensors

MEMS capacitive pressure sensor is also a dominant type in the market because of high sensitivity, low power consumption, and insensitivity to temperature variation. As discussed earlier in Section 2.2.1, capacitive pressure sensor usually contains a fixed electrode and a movable plate that deforms when the pressure difference is applied. The electrostatic capacitance changes with the distance between the electrodes changes. The capacitance can be processed by varies of readout circuits [62, 63]. With the development of new micro-machining sensor technologies with new materials such SOI, Silicon on sapphire (SOS), SiC, and carbon nanotube (CNT), MEMS capacitive pressure sensors are evolving towards harsh environment applications [64].

Capacitive pressure sensors are usually designed with thin-film plates with small deflections (plate thickness should be as least four times larger than maximum deflection) to ensure linearity. The high-pressure sensitivity of the capacitive pressure sensor is achieved by increasing diaphragm size, reducing diaphragm thickness, and decreasing the sensing gap. However, the trade-off in capacitor gap and maximum diaphragm deflection cause non-linearity and limited dynamic range. Therefore, capacitive sensors are usually used for low-pressure measurement. Technology improvements on solving the problem of linearity, trade-off in limited dynamic range and sensitivity has been reported in many literature by designing of new

structures [9], application of new materials [65], and explore new operation mode [66].

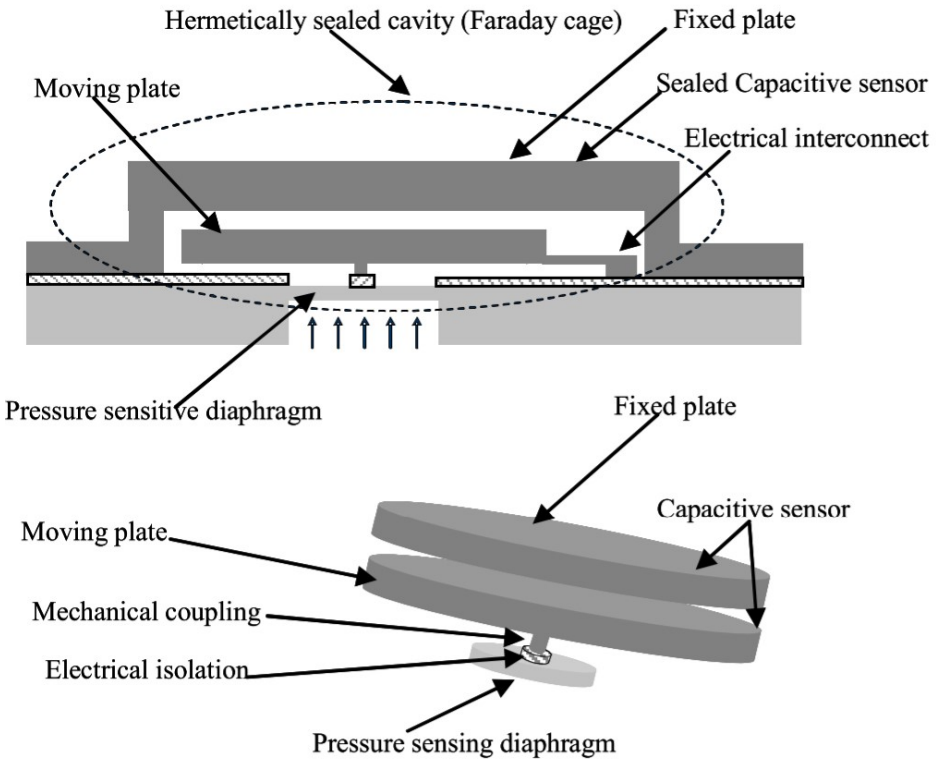


Figure 2.27: Schematic of the capacitive pressure sensor structure [9].

A high-sensitive capacitive pressure sensor reported by Zhang et al. [9] is shown in Figure 2.27. The pressure sensing element is decoupled from the capacitive sensing element. The dynamic range can be increase by reduce dimension of the pressure sensitive diaphragm, while the capacitor sensitivity can be improved by increase capacitor plate area and reduce the capacitor gap. Therefore, both high sensitivity and large dynamic range can be achieved. Although complex structure solve the trade-off problem in capacitive sensor design, more complex fabrication process and delicate device structure make the device fragile for high pressure measurement with a lower stability.

New method developed for capacitive pressure sensor to adapt high pressure measurement. Touch-mode capacitive pressure sensor [66] are developed with larger dynamic range and better linearity. Conventional capacitive pressure sensor using diaphragm as capacitor moving plate remains a gap with the fixed plate at the entire pressure range. While in touch mode operation, pressure sensing diaphragm starts touching the fixed plate and landed on an insulation layer as shown in Figure 2.28b. Capacitive pressure sensing diaphragm designed to operate in touch mode are constrained to maximum deflect with designed gap distance. The major

capacitance output is determined by the conjuction area of the plates and properties of the insulation layer rather than capacitor air gap.

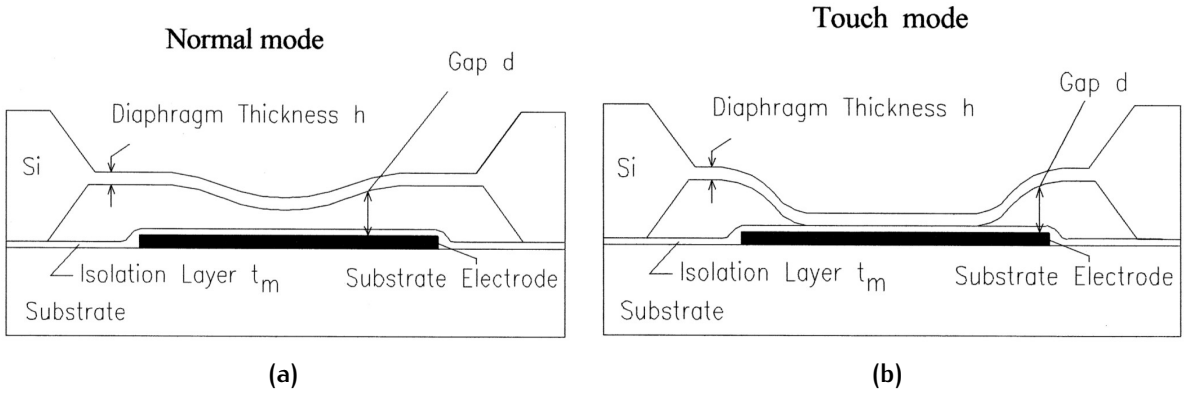


Figure 2.28: Simple schemetic of typical capacitive sensor in (a) normal mode; (b) touch mode [66].

The touch mode capacitor is able to provide larger over-range pressure measurement with improved linearity. However, mechanical toughness is highly required in this type of sensor due to a larger deflection rate at the edge at higher pressure. SiC as capacitance sensing diaphragm has been reported for measurement of higher pressure. An all-SiC based capacitive pressure sensor is designed and tested by Chen et al. [67] for in-cylinder pressure measurement up to 5 MPa operated under 574 °C. Both contact mode and non-contact mode are investigated in Chen's work. In situ ammonia-doped low resistivity LPCVD poly-SiC film is deposited on insulated SiC wafer as capacitor bottom plate. After another insulation layer and LTO sacrificial layer, a poly-SiC thin film is deposited as the sensing diaphragm as shown in Figure 2.29a.

Figure 2.29b shows measured capacitance response of the device. improved linearity is obtained in the contact mode, and pressure up to 800 psi can be measured with a total capacitance change of almost 2.5 pF. The highest temperature coefficient is reported as 0.05 % at 574 °C with a relatively stable long-term performance. Chen's work proves the promising application of poly-SiC in touch mode capacitive pressure sensors for high-pressure measurement under high temperatures. This device does not require bulk etching of SiC substrate, therefore, reduce fabrication difficulty.

2.3 CONCLUSION

This chapter first provides the background research of the popcorn failure mechanism in Section 2.1. The mechanism of possible failures, reflow environmental

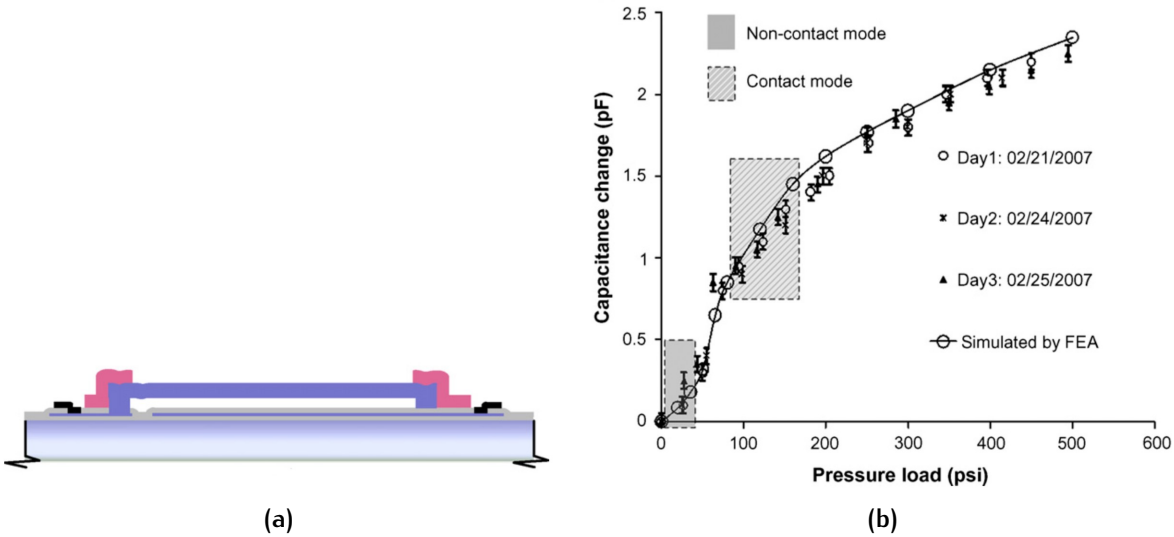


Figure 2.29: All-SiC capacitive pressure sensor (a) Croess section schematic; (b) capacitive responce with up to 800 psi pressure load [67].

factors, moisture behavior, vapor pressure level, and distribution is studied as the foundation of designing the measurement device. The reflow temperature profile is summarized to provide the temperature range of measurement. Rough vapor pressure ranges along with spatial distribution are presented. Pressure sensors are introduced in Section 2.2. Different sensing mechanisms of common pressure sensors were first studied and evaluated. Absolute piezoresistive and capacitive pressure sensors are selected in terms of application requirements (Section 2.1) from various sensing mechanisms, with consideration of potential performance, fabrication complexity, and fabrication viability with tools in EKL. Then, various piezoresistive and capacitive pressure sensors from the previous publications were reviewed and compared. Finally, touch mode capacitive pressure sensors using silicon substrate and SiC diaphragm as sensing elements is selected for this thesis by comprehensive considerations of dynamic range, high-temperature compatibility, temperature dependency, complexity, fabrication accessibility, and costs. All information obtained from the literature review provides references for device and process design that will be discussed in the following chapters.

3 DESIGN AND SIMULATIONS

This chapter will present the vapor pressure sensor design based on the information obtained from the literature review in Chapter 2. Firstly, design considerations such as design specifications, device functions, required structures, and sensing element material will be discussed. Based on the considerations, the overall device structure is designed. The working principle and analytical model of the touch mode capacitive pressure sensor are illustrated. The detailed device parameters will be analyzed and verified by FEA simulations using COMSOL Multiphysics. Finally, the complete designed parameters will be given at the end of this chapter.

3.1 DESIGN CONSIDERATIONS

In order to measure the vapor pressure generated inside the molding compound during reflow process and give a comprehensive analysis of the failure mechanism, a test sensor is designed. Design considerations are first discussed in this section to give an overview of design criteria. Device function and requirements are concluded in Section 3.1.1 from earlier studies of popcorn failure mechanism. Combining the design specifications and accessible technologies of MEMS sensor development, useful sensing principles, possible structures, and critical material selection are summarized in Section 3.1.2.

3.1.1 Specifications

The first step for a sensor design is to define the sensor's specifications based on the features of the measured object. In this thesis, the sensing device will be designed to monitor the vapor pressure level generated by moisture vaporization inside the molding compound at high temperatures. The specifications and device functionalities are determined by the failure mechanism introduced in Section 2.1.

The basic functionality of the device is vapor pressure measurement. The operating pressure range is determined by the maximum potential vapor pressure range generated by a typical molding compound in the reflow environment. According to Section 2.1.4, the vapor pressure is mostly determined by the reflow temperature

and precondition humidity. The saturated vapor pressure value under different temperatures is shown in Figure 3.1. According to the saturated vapor pressure values, the pressure to be measured ranges from atmospheric pressure to 7.45 MPa at 290 °C. In some theories, the actual vapor pressure is slightly higher than the saturated value [68]. Therefore the designed pressure range for the vapor pressure sensor is set from 0.1 MPa to 8 MPa (slightly higher than 7.45 MPa), corresponding to reflow temperature up to 290 °C [10].

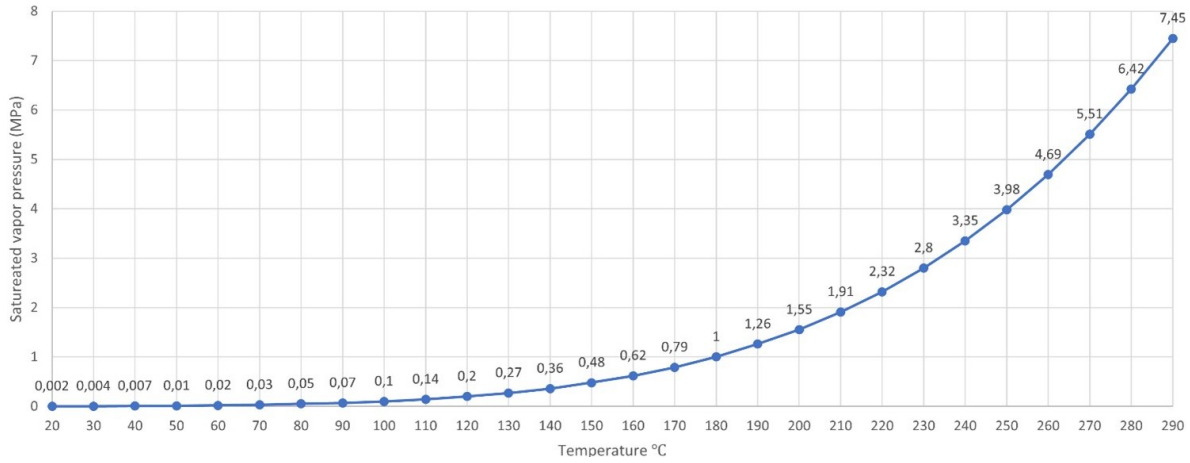


Figure 3.1: The change of saturated vapor pressure with temperature [10].

Pressure sensitivity is mostly required from the minimum pressure change with the applied temperature step. Saturated vapor pressure rises quickly after 100 °C. Based on the data, the resolution of the sensor should be better than 0.1 MPa per 10 °C temperature step over 150 °C, and should be even better than 0.01 MPa if lower temperatures (<150 °C) are applied. The readout circuit partly decides device resolution, so the resolution requirement is a reference for future work.

Operating temperature is another critical requirement. Whether used for an experimental measurement that mimics the reflow environment or used in a reflow soldering machine, device operating temperature should cover the possible temperature range of the reflow process. Based on the industry-standard (PC/JEDEC J-STD-020D) [2], the targeted temperature at reflow is 265 °C to 280 °C for lead-free solder. In literature, vapor pressure behavior is studied until 300 °C [10]. The minimum operating temperature will be room temperature. Therefore, the operating temperature range is set as 20 °C to 300 °C.

The specifications defined above are summarized in Table 3.1. Apart from the basic functionality of vapor pressure measurement, optional functionalities can be considered. According to the literature, the moisture level is an essential parameter to the vapor pressure evolution. The theory derives vapor pressure levels based on the moisture condition in the package. Therefore, a moisture sensor can also be implanted beside the pressure sensor to indicate the moisture level during pressure

Table 3.1: Design specifications

Design parameter	Value			Unit
	Min.	Middle	Max.	
Meassured pressure range	0.1	1	8	MPa
Operating temperature	20	180	300	°C
Resolution		0.01	0.1	MPa

measurement.

3.1.2 Overall structure considerations

Overall device structure and critical structure materials are firstly considered by combining the targeted device specifications and previous literature study on pressure sensors and failure mechanisms.

First of all, the position of the sensing structure is crucial for the indication of correct vapor pressure levels in the molding compound. The measurement of vapor pressure inside the molding compound is a challenge because a zero gap between the interfaces is difficult to achieve. From Figure 2.8c in Section 2.1.4, the vapor pressure reaches an uniform distribution throughout the package with sufficient soaking time at preconditioning. Theoretically, the vapor pressure in the molding compound/die interface should have the same value as inside the molding compound. When a delaminated cavity exists between the molding compound and the die, moisture vapor generated inside the molding compound crosses the interface and fills a crack of 0.1 mm with the same saturated value [1]. Therefore, the sensor can be fabricated in a cavity with designed dimensions where the molding compound can be mounted on top. With properly sealing of molding compound, the sensing device is able to measure the accumulated moisture and vapor pressure in the cavity. In literature, a mathematical approach modeled the vapor pressure in a delamination-induced internal cavity between the molding compound and die pad [3]. The cavity size will be designed based on vapor pressure diffusion and accumulation behavior based on this literature in Section 3.2.1.

A possible pressure sensing mechanism is discussed earlier in Section 2.2. The touch mode capacitive pressure sensor is the most suitable sensor type for this application in terms of requirements, performance, complexity, and fabrication viability. The theoretical measured pressure range is relatively large and requires to be measured with temperature changes. The touch mode capacitive sensing mechanism is able to provide an output with relativity smaller stress on the membrane under the high temperature due to the limited deflection degree, less temperature dependency, and higher sensitivity. The touch mode piezoresistive readout can also be

investigated on the same device with additional electrodes. Therefore, the sensing membrane will act as a pressure sensing element, capacitor moving plate, as well as a piezo-resistor. The possibility of integrating both capacitive and piezoresistive mechanisms on the contact mode diaphragm can be investigated. In conclusion, the main structures for this device are pressure sensing diaphragm, fixed capacitor plate, insulation layer, substrate, and vapor accumulation cavity.

The performance of the device is also determined by structural material properties. Silicon wafers will be used as substrate due to lower cost and easier accessibility. Capacitive sensors sometimes use ion-implanted silicon substrate as the fixed electrode. However, it is not applied in this thesis because silicon's high-temperature performance is compromised, and ion implantation takes too much time. Therefore, the substrate will only be used as a supportive base for the sensor because of lower cost and accessibility for research purposes. Furthermore, using bulk micromachining techniques with high structure accuracy, the vapor accumulation cavity is easier to fabricate on a silicon wafer.

As discussed earlier in Section 2.2.2, poly-SiC is a suitable material for high-pressure measurement at elevated temperature due to its excellent mechanical and electrical properties as introduced in the background section. LPCVD Poly-SiC deposition and etching recipes were developed and tested in EKL by Bruno Morana in his doctoral thesis [69]. Luke Middelburg then improved the process and developed a SiC integrated smart sensor chip with integrated SiC-CMOS electronics and fabricated in EKL [18]. Their work proves the feasibility of utilizing an LPCVD poly-SiC membrane as a pressure sensing element with available tools in EKL. In this thesis, a diaphragm made of in-situ N-doped LPCVD poly-SiC will be designed as the pressure sensing element.

The material characteristics are first summarized from previous works. The electrical and mechanical property of LPCVD poly-SiC was studied in PhD thesis of B. Morana [69] and L.M. Middelburg [18]. Different diaphragm properties are obtained from deposition parameters such as gas flow ratios, temperature, pressure, and time. Six typical layers with different parameters shown in Table 3.2 were investigated by Bruno [69].

Table 3.2: Gas flow ans deposition times for LPCVD SiC deposition in different layers. (adapted from [69]).

Layer ID	SiH_2Cl_2	$C_2H_2(5\%in H_2)$	$NH_3(5\%in H_2)$	Total gas flow	Deposition time
D-0	80 sccm	320 sccm	0 sccm	400 sccm	120 min
D-1	80 sccm	320 sccm	15 sccm	415 sccm	80 min
D-2	80 sccm	320 sccm	30 sccm	430 sccm	75 min
D-3	80 sccm	320 sccm	45 sccm	445 sccm	75 min
D-4	80 sccm	320 sccm	60 sccm	460 sccm	75 min
D-5	80 sccm	320 sccm	75 sccm	475 sccm	75 min
D-6	80 sccm	320 sccm	90 sccm	490 sccm	70 min

The properties of the deposited SiC layer were measured and concluded by Bruno listed in Table 3.3. The residual stress and resistivity can be used as a reference for device and process design. Resistivity of the diaphragm layer can be selected based on the piezoresistive response to investigate the piezoresistive effect in the contacted capacitive readout mode.

Table 3.3: Growth rate, stress, and resistivity of depostied SiC in different layers. (adapted from [69]).

Layer ID	NH_3 sccm	$GR_{avg}(nm/min)$	σ_{r-av} MPa	$\rho^{-3}\ \Omega \cdot cm$
D-0	0	5.4	0	3422
D-1	0.75	8.0	320	68.08
D-2	1.5	8.1	437	20.56
D-3	2.25	8.1	547	9.92
D-4	3	8.2	596	4.99
D-5	3.75	7.9	570	3.86
D-6	4	7.9	471	3.49

For piezoresisitve response, highest gauge factors are reported for a target bulk resistivity of polycrystalline 3C-SiC of approximately $0.1\,\Omega \cdot$ cm [15, 70]. D-2 layer are selected both as diaphragm layer and capacitor plate with a resistivity of $0.02\,\Omega \cdot$ cm by referencing piezoresistive behavior in Luke's work [8]. Useful properties of LPCVD poly-SiC are also adpated from Luke's thesis for design reference shown in Table 3.7.

Table 3.4: Material properties used in design and simulation.

Property	Value
LPCVD SiC Young's modulus (E)	430 GPa [8]
LPCVD SiC Poisson ratio (ν)	0.168 [8]
LPCVD SiC Density (ρ)	3.18 kg m^{-3} [8]
LPCVD SiC Critical stress (σ_c)	3.16 GPa [8]
LPCVD SiN dielectic constant (ε_i)	6 to 7 [71]

Furthermore, molding compound assembled in the further experiment should survive during the heating and measurement steps. The strength of the molding compound should be able to endure the predicted vapor pressure. Fukuzawa [19] proposed a model to describe the maximum stress on the die pad border Equation 3.1. The crack will occur when this stress exceeds the strength of the molding compound.

$$\sigma_{max} = 6K(\frac{a}{t})^2 P \tag{3.1}$$

Where K is the geometrical factor ($K \cong 0.05$ for a square pad), a is the length of the long side of the die, and t is the molding compound thickness over the die or the pad. A typical bending strength of molding compound is around 10 MPa at reflow temperature of 215 °C given in literature [72]. The size and material of the compound should be selected based on this principle.

3.2 DEVICE STRUCTURE DESIGN

An overview of the designed device is shown in Figure 3.2. Sensing structures are integrated inside a cavity etched on surface of the substrate. Molding compound can be placed on top of the chip and form a sealed cavity where the moisture vapor generated in the molding compound will diffuse and accumulate. Touch-mode capacitive pressure sensing structures and other test structures are designed inside the cavity. The SiC diaphragm acts as a pressure sensing diaphragm (Green) that deflects with vapor pressure rises inside the cavity, which will change both the capacitance (formed by the diaphragm as a moving plate and an insulated fixed plate) and the resistivity (due to the piezoresistive effect of the diaphragm). The capacitor bottom electrode is made of the same material as the diaphragm for fabrication considerations. The sensing structures are insulated from the substrate by a layer of LPCVD silicon nitride (Orange). Another silicon nitride layer is deposited on top of the bottom capacitor plate to insulate the two conductive layers. Metal interconnects insulated from the conductive structures expected for contact openings. Electrodes transmit the electrical signal to outer metal pads by contact openings etched through the insulation layers. Before further experiments, a protection layer

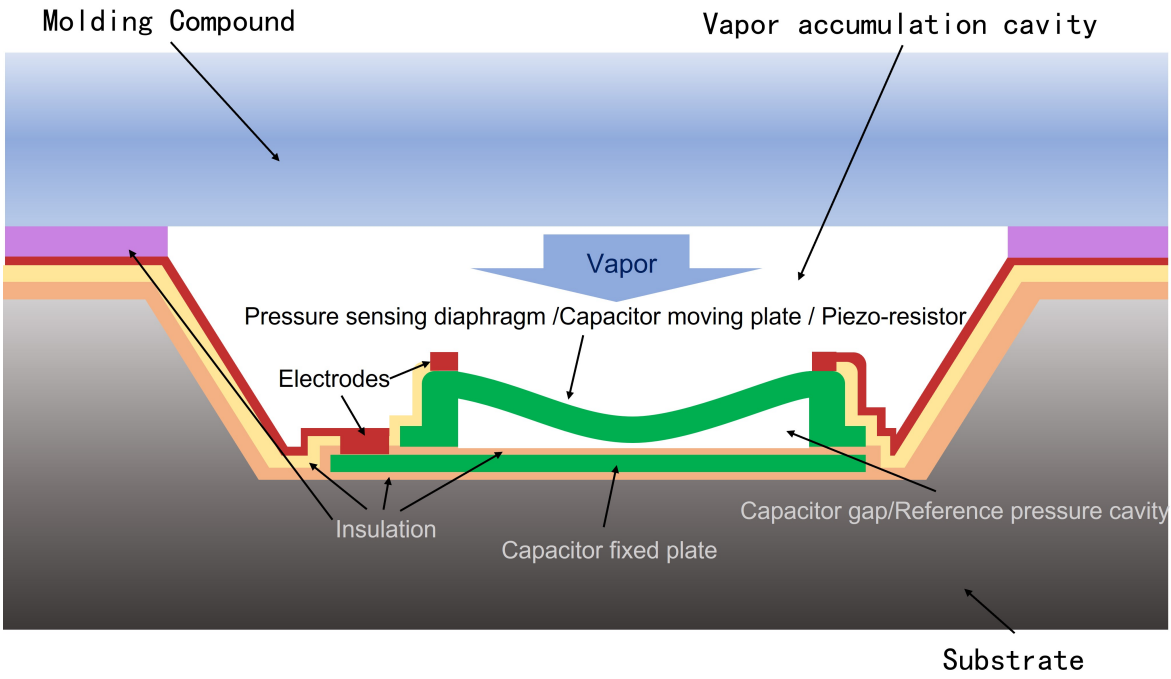


Figure 3.2: Overall cross-section schematic of the pressure sensing device.

is deposited on top of the cavity to protect the interconnects from damage. By changing the thickness of the protective layer, the depth of the vapor accumulation cavity can be changed. Detailed design principles, parameters, considerations will be discussed in this section.

3.2.1 Vapor accumulation cavity

A well is designed on the substrate to form a cavity between the molding compound and the sensors. Moisture vapor generated by the molding compound will diffuse and accumulate to a specific vapor pressure level inside the cavity. The dimension of the cavity is designed based on the dimensions of structures inside the well, properties of the molding compound, and most importantly, the behavior of vapor pressure inside the cavity.

According to literature, vapor pressure inside the cavity is closer to the value inside the molding compound when cavity depth is small enough with the assumption of an infinite cavity-molding compound interface [3]. A deeper cavity makes the peak pressure lower and later reached. From Figure 3.3, a cavity size of 1 mm reduce about half of the peak pressure (From 16 atm to 9 atm); cavity size of 10 µm only slightly reduce the peak pressure (From 16 atm to 15.5 atm). Therefore, the ratio of cavity-compound interface area and cavity depth should be designed considerably

larger for more vapor to diffuse and build up inside the cavity.

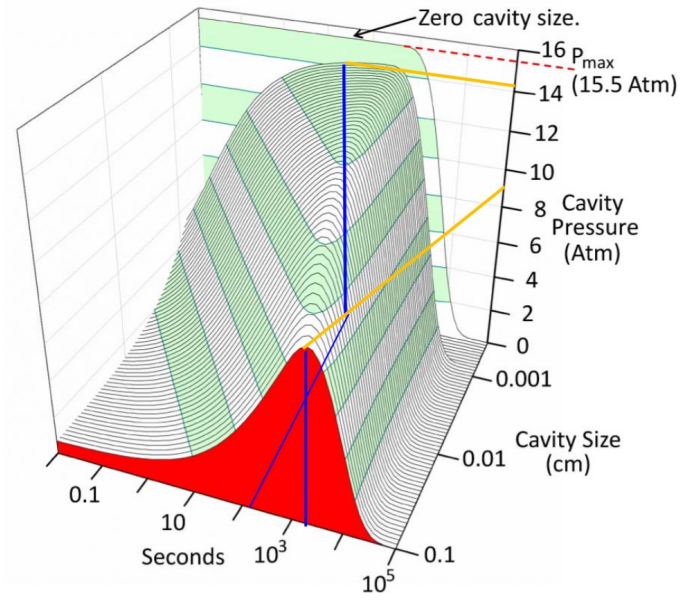


Figure 3.3: Evolution of cavity pressure in a 0.2 cm **slab of molding compound** and **various cavity size** preconditioned at T_0 = 85 °C and H_0 = 85 % for enough time to reach equilibrium, then exposed to step reflow for T_1 = 215 °C and H_1 = 0.1 %. Limit (P_{limit}) at zero cavity size [3].

Different cavity depths can be fabricated on the substrate to verify its influence on vapor pressure levels. Assuming an infinite thick molding compound with no gap between the molding compound and the sensing membrane, the vapor pressure can reach the limit highest pressure P_{limit} quickly. Keep one group of molding compound thickness constant and vary the cavity size up to 1 mm (At cavity size 1 mm, the vapor pressure reduces about half of value as shown in Figure 3.3). The device is designed to easily change the cavity size by bulk etching of silicon substrate or increase the deposition thickness of the insulation layer on top of metal interconnects. The influence on vapor pressure level by the size of molding compound can also be investigated with this device to verify the theoretical models.

Besides the consideration of vapor pressure level, surrounding structures also give constraints to cavity dimensions as elaborated in Figure 3.4. The minimum area of the well should be larger than the total area of inner structures (Sensing structures, test structures and interconnections). This is decided by how many structures are designed inside the well. As discussed later, 20 Diaphragms with different sizes will be designed inside the well to test the performance. Each structure occupy 300 µm × 300 µm area. Test structures for testing resistance and capacitance will also take space. By a rough calculation and arrangement, the structures will take 2 mm × 2 mm spaces. The total area is add to 3 mm × 3 mm to leave enough space

for metal interconnects. In order to fit in a typical 10 mm × 10 mm die, the chip should leave a space for metal pads outside the cavity area. The size of the tested molding compound for the further experiment should be large enough to cover the cavity and smaller than the designed outer metal pad for wire bonding.

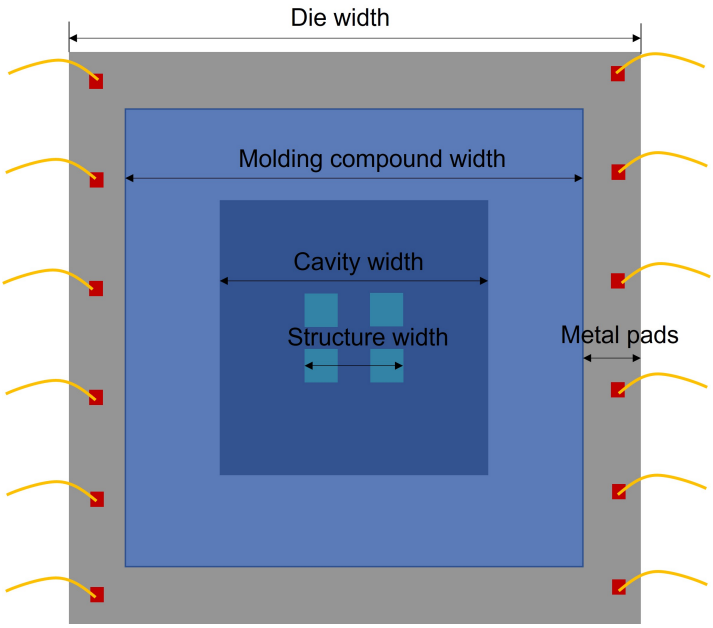


Figure 3.4: Topview illustration of cavity width design consideration with surrounding structures.

The minimum depth of the cavity is decided by two factors: surface roughness of molding compound and the maximum height of the sensing structures. Because of the surface roughness of the molding compound, space is needed between molding compound and the sensors to protect the delicate structures. The depth can be designed a few microns larger than the structures' height. The molding compound surface roughness can be compensated by creating a thick protection SiO_2 layer to increase the gap between the bottom surface of molding compound and the structures. Also, the molding compound can be cured on a smooth surface to reduce surface roughness.

3.2.2 Pressure sensing diaphragm

Pressure sensing diaphragm with touch-mode capacitive readout is designed. The basic principle is illustrated in detail in Chapter 2. An electrically conductive membrane suspended on a vacuum cavity is worked as one plate of the parallel capacitor. Another capacitor conductive electrode at the bottom is insulated from the membrane by a layer of insulating material. The membrane deforms differently when the pressure load on the membrane changes. The cavity gap between the capacitor

electrodes changes until the top plate is in contact with the insulation layer. The capacitance changes with the integrated equivalent dielectric constant, and plate distance changes. The applied pressure difference is then transformed into capacitance change.

In the non-contact mode of operation, the deflection of an edge clamped membrane can be calculated by a general differential equation. Circular and square diaphragms are generally used, and the center deflections can be estimated by the equation given in Section 2.2.1:

$$w(r) = \frac{Pa^4}{64D}[1 - (\frac{r}{a})^2)] \qquad (Circular) \tag{3.2}$$

$$P = E\frac{h^4}{a^4}[g_1\frac{w_0}{h} + g_2(\frac{w_0}{h})^3] \qquad (Square) \tag{3.3}$$

Where P is the applied pressure, E is Young's modulus, h is the thickness of the diaphragm, w_0 is the maximum deflection of the membrane. g_1 and g_2 are constant with Poison ratio ν. For circular diaphragm, r, $w(r)$, and a are respectively the radial distance from the diaphragm's center, the displacement at a radial distance of r, and diaphragm radius; for the square diaphragm, a is the half of membrane width. D is the flexural rigidity given by:

$$D = \frac{Eh^3}{12(1-v^2)} \tag{3.4}$$

Normally, the pressure sensing diaphragm works at small deflections to grantee linearity relation between pressure difference P and diaphragm displacement w_0. In this case, the ratio of w_0/h is usually designed less than 0.2 for the term $g_2(\frac{w_0}{h})^3$ or $(\frac{r}{a})^2$ can be ignored. However, the deflection is too large for the nonlinear terms to be ignored under contact mode operation under high pressures. For large deflection, a simplified equation is given by [32]:

$$w_0 = \frac{Pr^4}{64D}\frac{1}{1 + 0.488\frac{w_o^2}{h^2}} \qquad (Circular) \tag{3.5}$$

$$w_0 = 0.802a\sqrt[3]{\frac{Pa}{Eh}} \qquad (Square) \tag{3.6}$$

The capacitance can be derived from the integrated displacement and dimensions shown in Figure 3.5a. For example, the circular diaphragm capacitance is:

$$C = \int_0^{2\pi}\int_0^a \frac{\varepsilon_0\varepsilon_a\varepsilon_i r \mathrm{d}r\mathrm{d}\theta}{\varepsilon_a t + \varepsilon_i(g - w(r,\theta))} \tag{3.7}$$

Where ε_0 is vacuum permittivity, ε_a is the dielectric constant of the gas inside the cavity, ε_i is the dielectric constant of the insulating material on top of the fixed plate, t is the thickness of insulation layer, g is the initial distance of the capacitor

gap, and $w(r,\theta)$ is diaphragm displacement at position (r,θ). The deflection of the pressure sensing diaphragm is constrained due to the limited capacitor gap distance as shown in Figure 3.5b. When the contact area becomes larger under higher pressure ($g - w(r,\theta) \rightarrow 0$), the capacitance is mainly determined by the thickness and dielectric constant of the insulation layer ($\frac{\varepsilon_0 \varepsilon_i}{t}$).

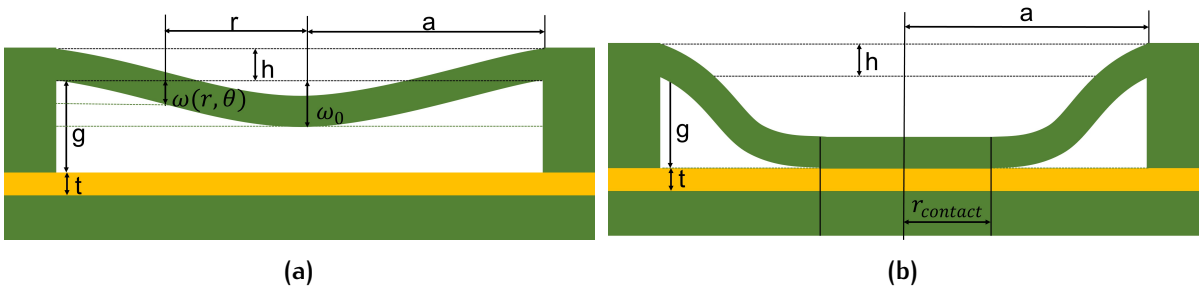


Figure 3.5: Schematic of the diaphragm bending with applied pressure. (a) Non-contact capacitor; (b) Contact capacitor.

Stress is another important parameter for diaphragm design. For edge-clamped diaphragm, the maximum stress σ_{max} appears at the edge of the diaphragm:

$$\sigma_{max} \approx P(\frac{a}{h})^2 \tag{3.8}$$

The design parameter relations can be concluded from Equation 3.7. The change in capacitance is determined by the deflection of diaphragm. Device sensitivity is defined by capacitance change per unit pressure change:

$$S = \frac{\Delta C}{\Delta P} \tag{3.9}$$

Trade-off exists in the parameters shown in Table 3.5.

Table 3.5: Trade-off in design parameters.

Influence when increasing	Diaphragm area	Diaphragm thickness	Capacitor gap	Insulation layer thickness
Capacitance	↑	↓	↓	↓
Sensitivity	↑	↓	-	↓
Dynamic range	↓	↑	↑	-
Diaphragm stress	↓	↑	-	-

Rough diaphragm dimensions are first designed by theoretical calculations based on the analytical models of touch-mode capacitive devices and material data extracted from literature.

Firstly, the thickness of pressure sensing diaphragm is decided by fabrication limitations. The maximum SiC deposition thickness is 5 μm due to the operation limit

of the LPCVD furnace. As discussed above, thinner the diaphragm results in better sensitivity. The ratio of diaphragm width and thickness is decided by material critical stress and maximum applied pressure:

$$(\frac{a}{h} < \sqrt{\frac{\sigma_c}{P_{max}}}) \tag{3.10}$$

Take the value of LPCVD SiC critical stress and maximum pressure of 8 MPa, the ratio fracah is limited to 19.8 for normal mode of diaphragm deflection. A diaphragm thicknes of 2.5 µm results in a diaphragm width of around 100 µm.

The thickness of insulation layer between the plate can be estimated by assuming typically $1/3$ area of the capacitor plates is in contact. With a dielectric constant of 7 for the insulation LPCVD nitride and designed maximum contact capacitance in few pico-farad level [71]. The insulation thickness can be estimated by:

$$t = \frac{\varepsilon_0 \varepsilon_i A}{3C} = \frac{8.85 \times 10^{-12} F/m \times 7 \times (10^{-4})^2}{3 \times 10^{-12}} \approx 200nm \tag{3.11}$$

Static initial capacitance is then calculated roughly to obtain an rough range of capacitor gap. Assume no pressure difference acted on the diaphragm, a typical parallel capacitor is formed. In order to achieve capacitance not smaller than hundards of fF level, the initial capacitance can be calculated by assume a vacuum cavity and substitute derived value in:

$$g \approx \frac{\varepsilon_0 A}{C} \tag{3.12}$$

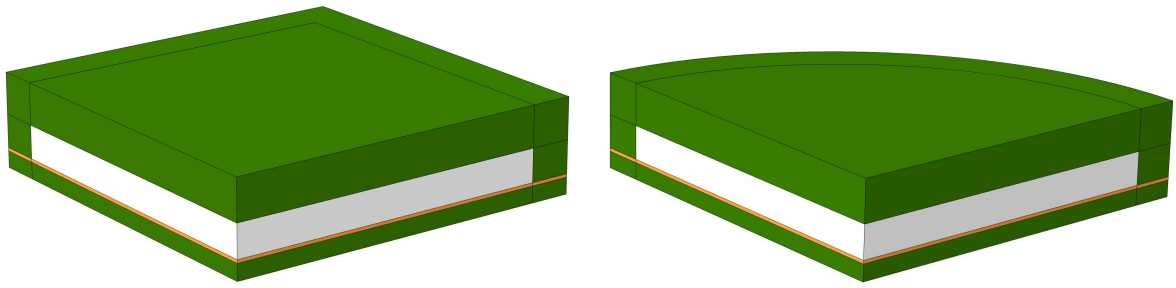
The derived vacuum gap should be around 1 µm. The final derived parameters are listed in Table 3.6. The precise value of structural dimensions will be determined by simulation results in next section. Verification on design parameter relations will also be performed by simulation.

Table 3.6: Estimated design parameters.

Parameter	Value
Diaphragm thickness (h)	2.5 µm
Diaphragm half width (a)	50 µm
Insulation layer thickness (t)	200 nm
Capacitor vaccum gap (g)	1 µm to 3 µm

3.3 PARAMETERS AND SIMULATIONS

FEA simulations are performed with COMSOL Multi-physics to verify the designed dimensions and give an estimated device performance with different structural dimensions of the defined range in the earlier section. Electro-mechanics 3D module which coupled solid mechanics and electrostatic with a moving mesh is applied to model the deformation of electrostatic components. Solid mechanics physics analysis is performed on the solid structures based on solving Navier's equations to compute structure displacement, stress, and strain. The displacement and stress models are derived from this simulation. The electrostatic physics field is applied to compute the electric field distribution with the deformed data resolved by solid mechanics module by Gauss' Law using scalar electric potential as a dependent variable.



(a) (b)

Figure 3.6: COMSOL simulation geometry model. The capacitor plates using poly-SiC is shown in green; the SiN insulation layer is shown in yellow; the vacuum gap is shown in white. (a) Square diaphragm; (b) Circular diaphragm.

Figure 3.6 shows the symmetrical geometry built in COMSOL for simulation. The material parameters are listed in Table 3.7. The poly-SiC capacitor plates (displayed in green) are insulated by 200 nm silicon nitride (displayed in yellow). Both square and circular diaphragm with a fixed thickness of 2.5 µm are modelled. The air gap of the capacitor is set as moving mesh with vacuum relative permittivity of 1 (white). Three parameters, applied pressure, capacitor gap distance, and diaphragm width, are defined to find the optimal dimensions. Boundary conditions are defined on the models to generate reasonable solutions. The bottom surface of the fixed capacitor plate is defined as zero displacements and zero electric potential(Ground). A pressure load $Papp$ is applied on top surface of the diaphragm to mimic the measured pressure with a range from 0 Mpa to 8 MPa. A small voltage is applied to the diaphragm to generate an electric field between the capacitor plates. Then the geometry is meshed by mapped sweeping with different distributions on different

layers to optimize computation accuracy.

In order to simulate the contacted capacitance, the diaphragm displacement should be constrained on top of the nitride insulation layer. However, the contact pair in COMSOL does not support the inner contact of the same defined object due to the inverted mesh element on the air/nitride interface. A special method was developed to simulate the contact of the two capacitor plates. The air gap was defined as a spring to avoid mesh inversion. The extra pressure load induced by the spring was added on the contact bottom diaphragm surface from the bottom direction defined by

$$P_{contact} = tn - en \cdot gap \tag{3.13}$$

When

$$gap = g_{vac} - w_0 \leq 0 \tag{3.14}$$

Where gap is defined as the initial vacuum gap g_{vac} minus the maximum diaphragm center displacement w_0. tn and en are respectively the virtual contact pressure and spring stiffness. When the diaphragm is not in contact with the nitride surface, the spring is neglected with a near-zero pressure. When the gap between the plates is closer to zero, the pressure acted on the bottom surface of the diaphragm increase dramatically as a manual constraint to prevent mesh inversion.

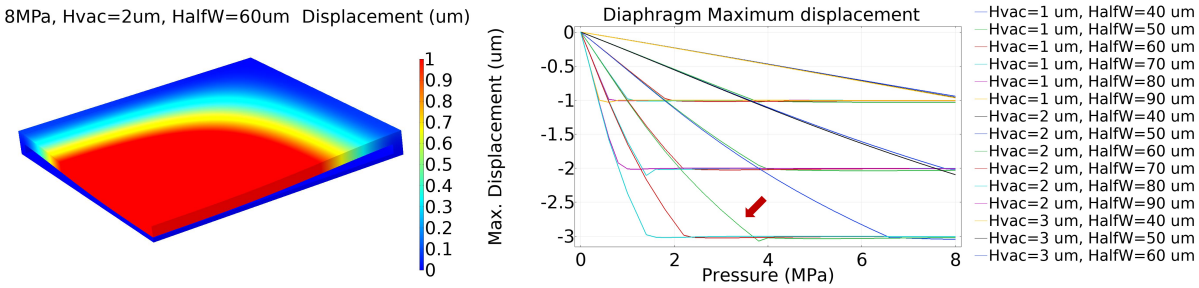
Table 3.7: Simulation parameters

Simulation parameters	Symbol	Value/Range
Applied pressure	Papp	0 [MPa] to 8[MPa]
Insulation layer height	t_{ins}	0.2[μm]
Air gap height	g_{vac}	1 [μm]to 3[μm]
bottom plate thickness	Hbot	1[μm]
Diaphragm thickness	Thickdia	2.5[μm]
Diaphragm half width	HalfW	40 [μm]to 90[μm]
Virtual spring stiffness	en	1e15[Pa/m]
Contact pressure	tn	0.1[MPa]
Top electrode voltage	Vo	100[mV]

Stationary study is computed with applied pressure varies from 0 Mpa to 8 MPa. Two parameters, the vacuum gap distance and diaphragm half-width, are swept to find the optimal design dimensions with consideration of material stress, device sensitivity, and displacement performance. The predicted performance is discussed as follows.

3.3.1 Membrane deflection

According to earlier discussion in Section 3.2.2, a higher pressure sensing sensitivity can be obtained by larger deformation with the same pressure difference, which means thinner diaphragm thickness and larger diaphragm area. However, the maximum diaphragm deflection is constrained by the capacitor gap and limited by the critical stress of diaphragm material. The displacement of the diaphragm was first simulated with several diaphragm widths and a vacuum gap to investigate the contact behaviour.



(a) (b)

Figure 3.7: Square diaphragm displacement simulated at maximum applied pressure of 8 MPa. (a) Total structure displacement for 2 µm vacuum gap and diaphragm half width of 60 µm; (b) Maximum displacement at the center of the diaphragm with varies diaphragm half width and vacuum gap.

Figure 3.8 shows an overview of diaphragm displacement. The maximum displacement occurs in the center before contact. The pressure at which the diaphragm center point is first in contact with the insulation layer is expressed as touchpoint. After the touchpoint, the touch area increase in a circle. Figure 3.7b summarizes the maximum displacement of all designed diaphragm width and vacuum gap at diaphragm center evolved applied pressure. The displacement increase with pressure until it reaches the height of the vacuum gap and touches the insulation layer. The touchpoint reaches earlier with a smaller gap and a larger diaphragm width. For the same vacuum gap, touchpoint comes in lower applied pressure for larger diaphragm width; For the same diaphragm width, the maximum displacement is similar before the touchpoint, which appeared in lower applied pressure for a smaller gap. No contact will appear when the diaphragm width is small enough and the vacuum gap is large enough. Figure 3.7a shows the structure total displacement of a 2 µm vacuum gap and 60 µm diaphragm half-width at 8 MPa. The touchpoint of this combination appears at 4 MPa as marked with the red arrow in Figure 3.7b.

The earliest touchpoint appeared at 0.4 MPa with 1 µm vacuum gap and 90 µm diaphragm half width (Figure 3.8a). The maximum touched area appeared at the

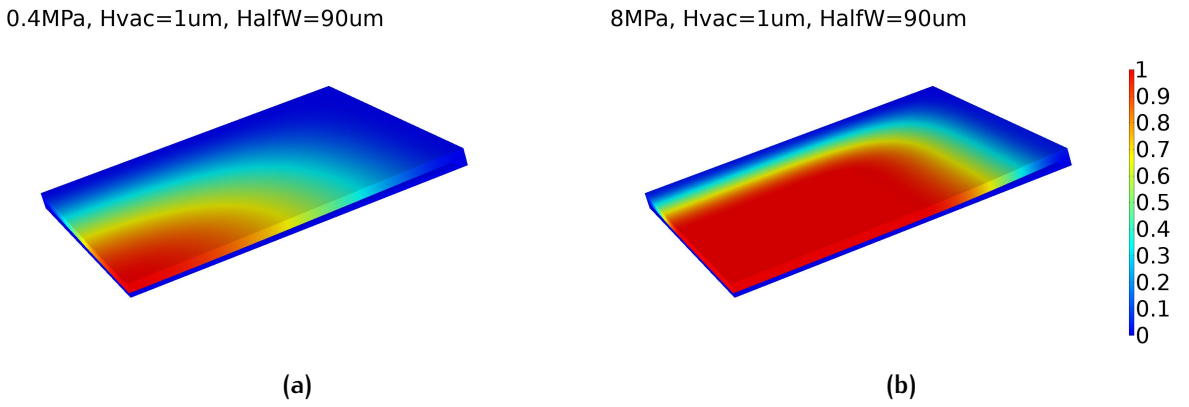


Figure 3.8: Total structure displacement for 1 µm vacuum gap and diaphragm half width of 90 µm at (a) Touch point pressure 0.4 MPa; (b) Maximum pressure of 8 MPa.

same dimension under maximum applied pressure pf 8 MPa Figure 3.8b. No contact appeared in 1 µm gap 40 µm diaphragm half width, 2 µm gap 40 µm diaphragm half width, 3 µm gap 40 µm diaphragm half width, and 3 µm gap 50 µm diaphragm half width. Diaphragm deflection results provide reference for analysis of key parameters. The diaphragm stress and output capacitance will be discussed later based on the diaphragm displacement, touchpoint, and touched area.

3.3.2 Diaphragm stress

As discussed earlier, device sensitivity is limited by diaphragm critical stress. Diaphragm stress induced by deformation should not be higher than the material critical stress to prevent structural failure. Figure 3.9 shows the mechanical stress induced by diaphragm deflection at the maximum applied pressure of 8 MPa. The maximum stress of the diaphragm can be seen in Figure 3.9a, appears in the middle edge. Figure 3.9b shows the stress at the maximum point (middle edge) under 8 MPa applied pressure as a function of diaphragm width with different vacuum gap. The maximum stress appeared at the largest vacuum gap and largest diaphragm width and does not exceed the SiC critical stress 3.16 GPa. Therefore, the diaphragm is safe from the designed pressure load based on the simulation results.

A clear relation between stress and diaphragm displacement can be concluded from Figure 3.9b and Figure 3.9c. A larger diaphragm area typically leads to higher stress due to larger diaphragm deformation under the same applied pressure. However, the diaphragm stress is reduced dramatically with a smaller vacuum gap because the deformation of the diaphragm is restricted by the bottom insulation surface. The stress only changes slightly with the diaphragm width increased after the diaphragm width is large enough to keep contact with the bottom surface. It can be concluded that touch mode operation significantly improved diaphragm stress,

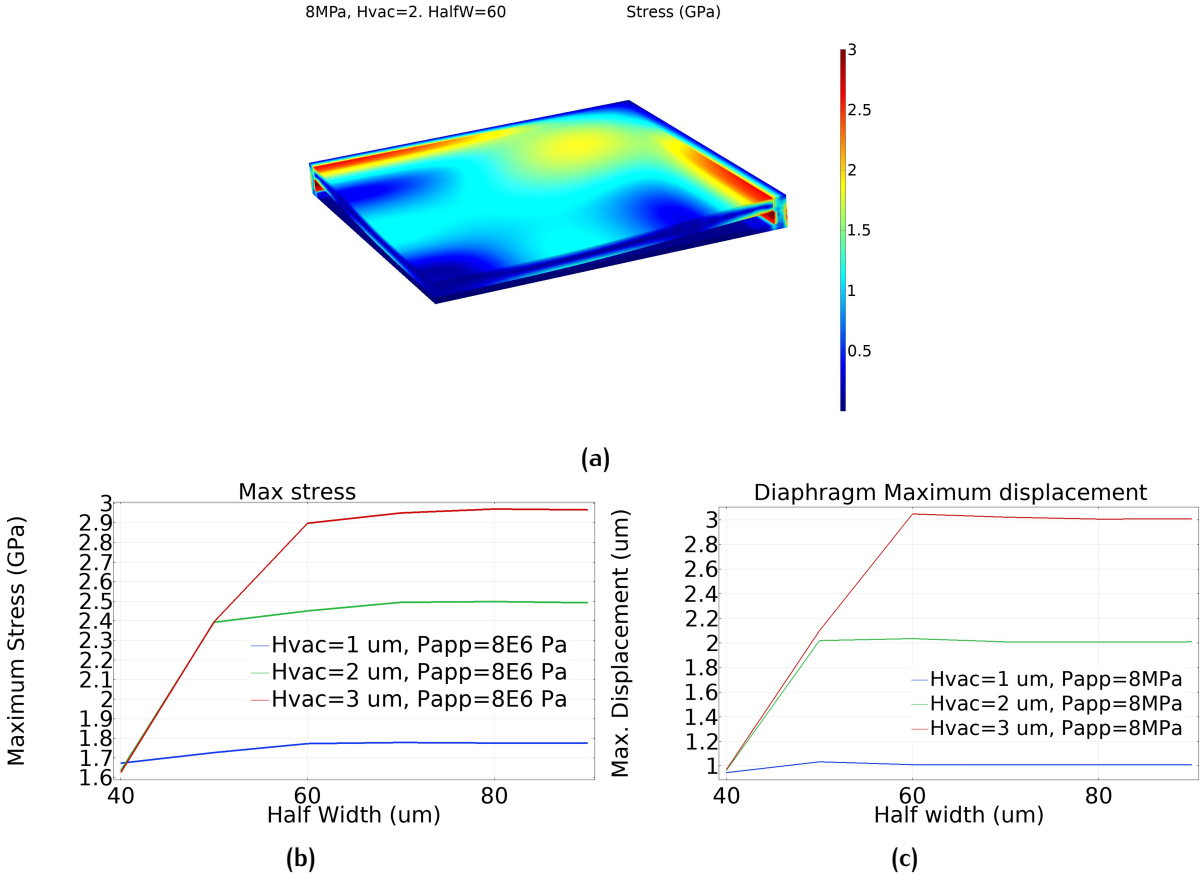


Figure 3.9: Square diaphragm stress simulated at maximum applied pressure of 8 MPa. (a) Stress distribution for 2 µm vacuum gap and diaphragm half width of 60 µm. (b) Stress at the middle edge of the diaphragm at different vacuum gap distance and diaphragm half width. (c) Maximum displacement at different vacuum gap distance and diaphragm half width.

and a smaller vacuum gap should be chosen to reduce stress for better reliability. In order to make sure a secure stress level, two vacuum gap distances, 1 µm and 2 µm, are designed for the device to compare the influence of gap distance on device performance.

3.3.3 Capacitance response

The capacitance response is analyzed to verify the theoretical model and select a group of structure dimensions (Diaphragm size and vacuum gap distance). Figure 3.10 shows a typical capacitance response with applied pressure. The slope of the capacitance response curve suddenly changes when maximum displacement reaches the gap distance (touchpoint). The capacitor works under normal mode (A region) before touchpoint pressure around 1 MPa with a non-linear capacitance change of 20 fF. After a short transition period (B region), the capacitance response curve enters a linear area (C) with a pressure load that exceeds touchpoint pres-

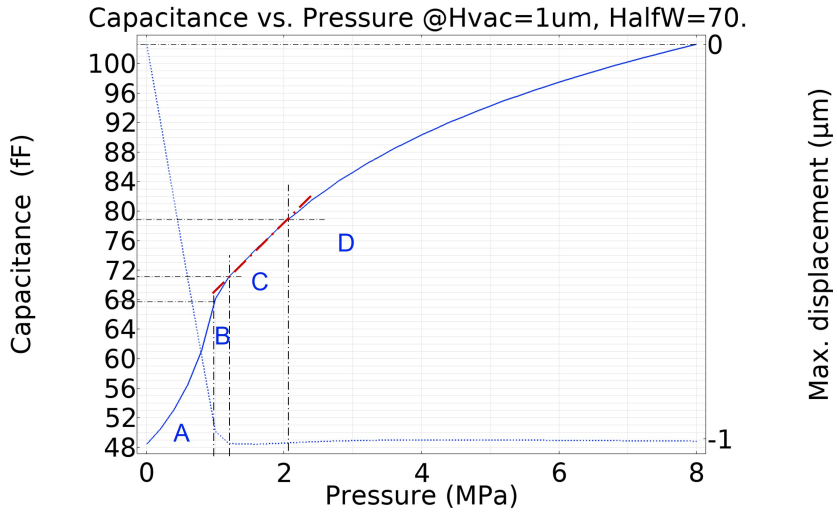


Figure 3.10: A typical response curve covers all operating mode With 1 µm vacuum gap and 70 µm diaphragm half width (A: normal region; B: transition region; C: linear region; D: saturation region).

sure. The linear region has a capacitance change of 8 fF with pressure change from 1.2 MPa to 2 MPa. Then at the saturation region (D), the sensitivity gradually decreases with higher pressure. Capacitance changes 24 fF under pressure load from 2 MPa to 8 MPa. Typically the linear region should be used for a better device linearity performance, but the full range can also be used for large dynamic range measurement after calibration. The vacuum gap and diaphragm size can be investigated to achieve a larger linearity range, a larger overall capacitance change, and higher sensitivity.

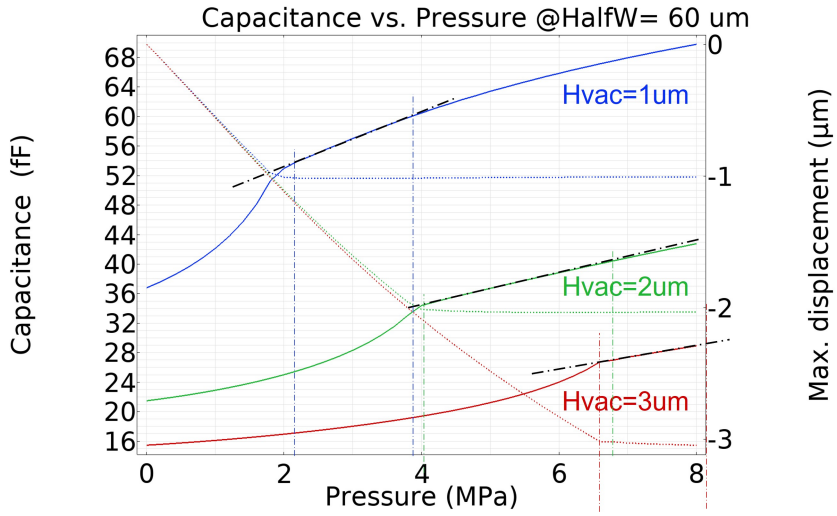


Figure 3.11: Simulated capacitance response vs. pressure load: Capacitance response curve (solid line) @ Diaphram half width of 60 µm with different vacuum gap distance compared with diaphragm maximum displacement (dashed line).

Figure 3.11 compares the capacitance response (in solid line) and diaphragm maximum displacement (in dashed line) under various of pressure load with different vacuum gap at diaphragm half-width of 60 µm. It can be observed that a larger linear region occurs in higher pressure ranges with a larger vacuum gap. However, a smaller capacitance change will be obtained for a large vacuum gap. The capacitance change of the 2 µm gap distance at the critical touchpoint for the diaphragm to operate in normal mode is 14 fF. Under the same pressure with the touchpoint pressure of 2 µm gap distance, the capacitance change of the 1 µm gap distance under touch mode is also to reach 24 fF. A clear sensitivity improvement can be concluded for the same dynamic range with touch-mode operation of capacitive pressure sensing. The gap distance should be designed carefully to balance linearity requirement and sensitivity based on the required dynamic range.

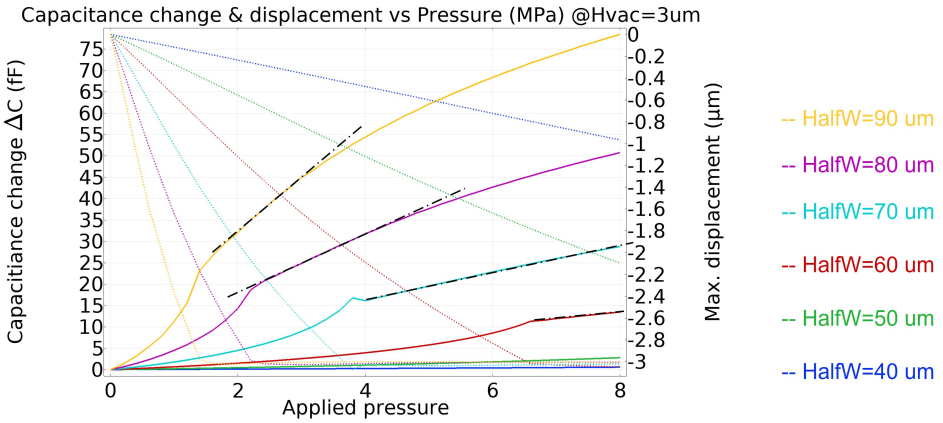


Figure 3.12: Simulated capacitance response vs. pressure load: Capacitance response curve (solid line) @ Vacuum gap of 3 µm with different diaphragm half width compared with diaphragm maximum displacement (dashed line).

Similar trend can be observed in Figure 3.12 shows the capacitance response (in solid line) and maximum diaphragm displacement (in dashed line) under varies of pressure load with different diaphragm half-width at 3 µm vacuum gap. Higher sensitivity can be obtained by increasing diaphragm width with a sacrifice of linearity range.

Figure 3.13 shows the maximum capacitance change, which at 8 MPa, as a function of diaphragm width with three different vacuum gap distances. It clearly indicates that the capacitance change is larger with a larger diaphragm and smaller vacuum gap. Especially for smaller gap distances, the capacitance change rises more quickly with diaphragm size. Capacitance under fF scale is negligible for diaphragm width smaller than 60 µm with 3 µm capacitor gap and 50 µm diaphragm halfwidth with 2 µm gap distance.

Based on the capacitive response, the diaphragm half-width of 60 µm is designed on the device because this diaphragm size covers all the operation modes in the

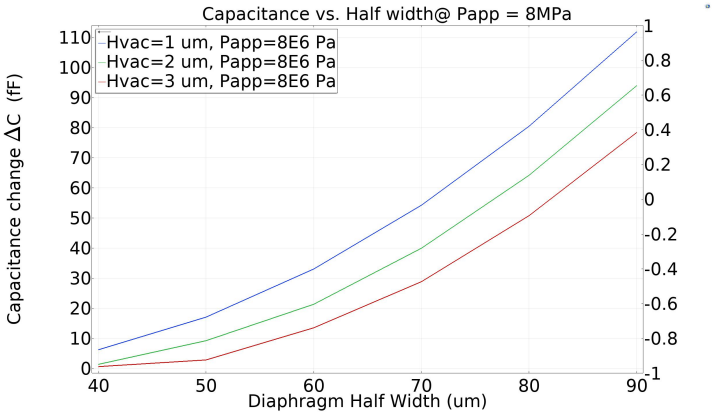


Figure 3.13: Simulated maximum capacitance change @ 8 MPa vs.diaphragm size and vacuum gap distance.

8 MPa range for comparison. Then larger diaphragm half-width of 90 µm is also implemented for better sensitivity. A 100 µm half-width is also designed under a critical stress of 3 GPa. Smaller diaphragm half-width of 30 µm and 40 µm are designed because the diaphragm will not contact throughout the applied pressures in this dimension to study the normal mode operation of this device.

3.3.4 Diaphragm shape

Performance of circular diaphragm is also investigate by simulation. Figure 3.14 shows the capacitance response curve and diaphragm stress with evoluation of pressure load of same sized circular and square diaphragm for comparison. The diaphragm stress at 8 MPa of sqaure diaphram is 1.75 MPa, higher than the circular diaphragm (1.6 MPa) with the same diaphragm radius and vacuum gap.

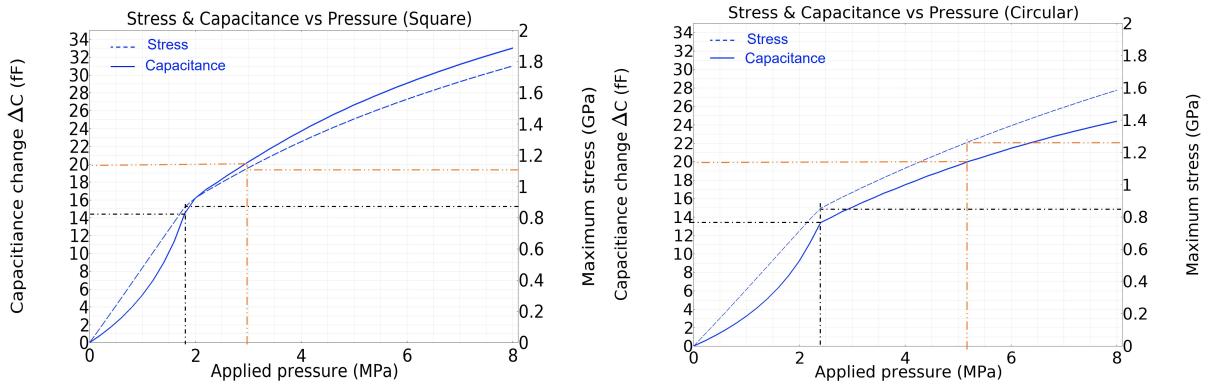


Figure 3.14: Capacitance response (solid line) and diaphragm maximum stress (dashed line) at the diaphragm edge with 1 µm vacuum gap and 60 µm of: (a) Square diaphragm; (b) Circular diaphragm.

However, the difference in stress behavior is mostly due to the difference of diaphragm area for the same circular diaphragm radius with square diaphragm width. The touchpoint of the square diaphragm shown in Figure 3.14a is at 1.8 MPa, earlier than 2.4 MPa of the circular diaphragm as seen from Figure 3.14a. Therefore, the displacement of the square diaphragm is higher than the circular diaphragm with the same parameters under the same pressure load. This is also the reason why the stress of the sqaure diaphragm is larger than the circular shape. Because of the same reason, the capacitance change at the same pressure of the square diaphragm is greater than the circular diaphragm.

The maximum capacitance change of square diaphragm is 33 fF, 9 fF larger than the circular diaphragm. At the touchpoint, the capacitance change and stress for both shapes of the diaphragm are similar, with a value of respectively 14 fF and 0.9 GPa. The stress at the same capacitance change is also investigated. For the same capacitance change of 20 fF, the stress of square diaphragm is 1.1 GPa, smaller than the circular diaphragm stress of almost 1.3 GPa. Therefore, with the same sensitivity at the touch mode, the square diaphragm performs better on stress levels. Both square and circular shapes are designed on the device to compare the experimental performance.

3.3.5 Piezoresistive behavior

The possible piezoresistive effect on SiC touch mode diaphragm is also investigated roughly by simulation. A simpler model was used to compute the piezoresistive effect shown in Figure 2.11a. In this model, the same SiC diaphragm (green) with 120 µm width was built separately with an insulation layer made of silicon nitride (yellow). An aluminum electrode (red) is placed at two sides of the top diaphragm surface.

The simulation parameters are adapted from the literature [18]. The relative resistivity change with pressure load up to 8 MPa is shown in Figure 3.15b.

Table 3.8: Material piezoresistive parameters for simulation [18].

Simulation material parameter	Value
SiC electrical conductivity	$1/300\ S/m$
SiC piezoresistive coupling matrix	$-2.33 \times 10^{-11}\ m^4/(s \cdot A^2)$
SiC relative permittivity	4.5
Aluminum electrical conductivity	$13.77 \times 10^7\ S/m$

The boundary condition of this model is different from the precious capacitive simulation for a simpler simulation. The bottom insulation plate is set as a fixed component, and a contact pair is applied on the insulator top surface and diaphragm

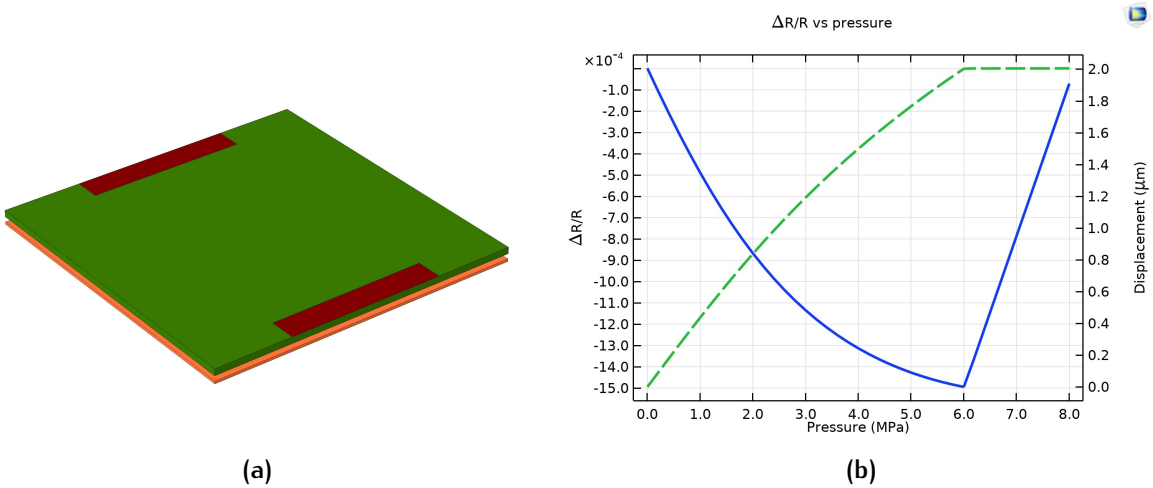


Figure 3.15: Piezoresisitve behavior (solid line) and diaphragm maximum displacement (dashed line) at the diaphragm edge with 2 µm vacuum gap and 120 µm diaphragm width. (a) Model structure; (b) Response curve.

bottom surface. The diaphragm is constrained by the side edges. Because of the difference in the boundary condition, the touchpoint is different from the capacitive model. The rough trend of the piezoresistive change is shown in Figure 3.15b. The relative resistivity first decreases due to the downwards deformation of the diaphragm. After the touchpoint pressure, the contact area of the diaphragm starts to bend upwards compared to the non-contact area, leading to reverse and near-linear resistivity change.

3.4 CONCLUSION

In this chapter, the design flow of the vapor pressure sensing device is illustrated. Device specifications, functionalities, and design considerations are first defined in Section 3.1 based on the vapor pressure generation mechanism studied in the background section. The operating temperature range, the measured pressure load is defined based on the possible vapor pressure ranges generated and the reflow process temperature profile. Then the position of the sensing device is proposed to design inside a cavity based on vapor pressure distribution concluded by simulations in the literature. Material selection is then selected for a touch mode capacitive pressure sensor based on the requirement and accessibility.

Design principle, overall designed structures, and rough parameters are explained in Section 3.2. The pressure sensor is designed based on capacitive diaphragms with normal mode and touch mode operation. The structure dimensions are estimated by pressure range, sensitivity, and material properties. Then FEA simulations are discussed to verify the design theories of the device. Based on the simulation

results on diaphragm displacement, device stress, and capacitive response, several groups of structure dimensions are selected. At the end of the simulation, the piezoresistive behavior of the touch mode device is also investigated. The final design parameters are shown in Table 3.9.

Table 3.9: Important design parameters.

Design parameters	Symbol	Value/Range
Operating pressure range	P	0 [MPa] to 8[MPa]
Operating temperature range	T	20 [°C] to 300 [°C]
Vapor acuumlation cavity depth	H_{cav}	10 μm to 100 μm
Diaphragm thickness	h	2.5[μm]
Diaphragm half width	a	30, 40, 60, 90, 100 [μm]
Insulation layer height	t_{ins}	0.2[μm]
Air gap height	g_{vac}	1 [μm], 2 [μm]

4 PROCESS DESIGN AND VERIFICATION

The chapter will present the design and verification of the device fabrication process. The fabrication methods are developed using previously established experience and available tools in EKL. A non-standard was designed due to the special layout. The complete mask images are attached in Appendix A and the detailed flow chart is attached in Appendix B. The detailed explanation and outcome of critical fabrication steps will be illustrated. Problems that occurred during fabrication will also be listed, and possible causes will be discussed. Finally, the complete device will be presented, along with a brief illustration of capacitance measurement of the fabricated device.

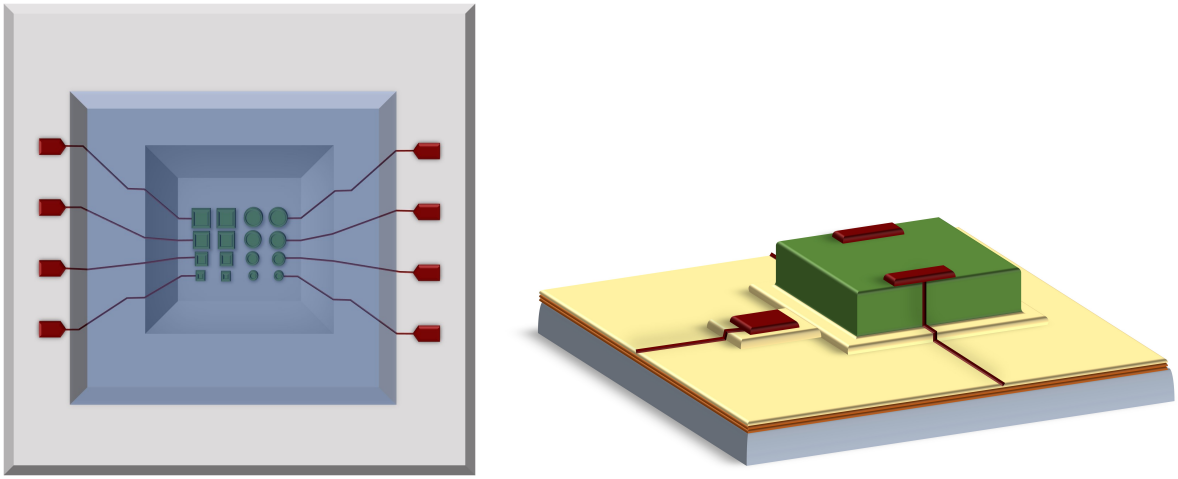
4.1 OVERALL STRUCTURES

Chapter 3 described the design of important device structures and dimensions based on theoretical models. A detailed device structure including pressure sensing element, reference structures, test structures, and the overall layout is designed with consideration of process technologies.

4.1.1 Device structure overview

The device is designed based on 10 mm × 10 mm die size. Figure 4.1a shows a rough structure arrangement on a die. A 3 mm × 3 mm cavity will be created on the surface of the substrate where the pressure sensors will be fabricated inside. Metal wire fabricated on the insulated substrate surface will connect the electrodes of the functional structures to outer metal pads on the edge of the die for wire bonding. A piece of cured molding compound can also be glued on top to form a sealed cavity for easier tests. An insulation layer can also be deposited on top of the substrate surface to protect the metal wires. Pressure sensing structures and some test structures are designed inside the cavity. Pressure sensing structures with both square and circular diaphragms will be fabricated on the cavity bottom. For each diaphragm shape structures with five diaphragm width/radius (60 µm, 80 µm, 120 µm, 180 µm, 200 µm) and two gap distances, in total ten structures, are placed

along with reference capacitor, moisture sensing structure, and test structures.



(a) (b)

Figure 4.1: Illustration of the overall structure configuration. (a) Structure overview; (b) Pressure sensing structure.

4.1.2 Pressure sensing structures

The pressure sensing structure is made of a pressure sensing diaphragm, a capacitor bottom plate, insulation layers, and electrodes as shown in Figure 4.1b. A 500 nm doped LPCVD SiC bottom capacitor plate is insulated both from silicon substrate (grey) and the pressure sensing diaphragm (green) (as moving plate) by silicon nitride layers (orange). The size of the bottom plate is slightly larger than the top structure to reduce the step height of the diaphragm structure for better metal layer coverage. Sacrificial structures are used to form the cavity and will be etched through release holes etched on the first deposited diaphragm layer. A second diaphragm layer will seal the holes and form the complete pressure sensing diaphragm. Another insulation layer (yellow) is then fabricated to insulate the metal interconnects and electrodes (red) from the unwanted conductive area beneath. Contact openings are etched through the insulation layers for the electrodes to be connected to the bottom plate. Insulating material on top of the diaphragm is also etched away for electrode connections and prevents its influence on the designed mechanical performance of the diaphragm. Electrodes are placed on the top side of the diaphragm, where insulation is removed. The electrodes provide interconnections for measuring the capacitance by measuring CV characeterics between the bottom electrode plate and the diaphragm and measuring the response or measuring the diaphragm resistance by applying a current or voltage on the top two electrodes. The detailed process flow for fabricating the structures and layer properties will be presented in Section 4.2.

4.1.3 Reference structures

Apart from the pressure sensing structures, reference structures are designed for characterization and measurement reference. A fixed capacitor which capacitance will not change with pressure load is designed as a constant reference. The structure of the reference capacitor is the same as the functional pressure sensing structure, except the sacrificial structure, will not be etched away to support the diaphragm under applied pressure. Another capacitive structure is designed to provide moisture level reference by measuring the change in capacitance due to permittivity change as shown in Figure 4.2a. The moisture reference structure has the same dimension as the reference capacitor. It will not be sealed so that the capacitor gap will be filled with moisture vapor. The pressure on the top and bottom sides of the diaphragm is balanced, so the diaphragm will not bend, and the capacitance change will be entirely due to the change in relative permittivity at the capacitor gap.

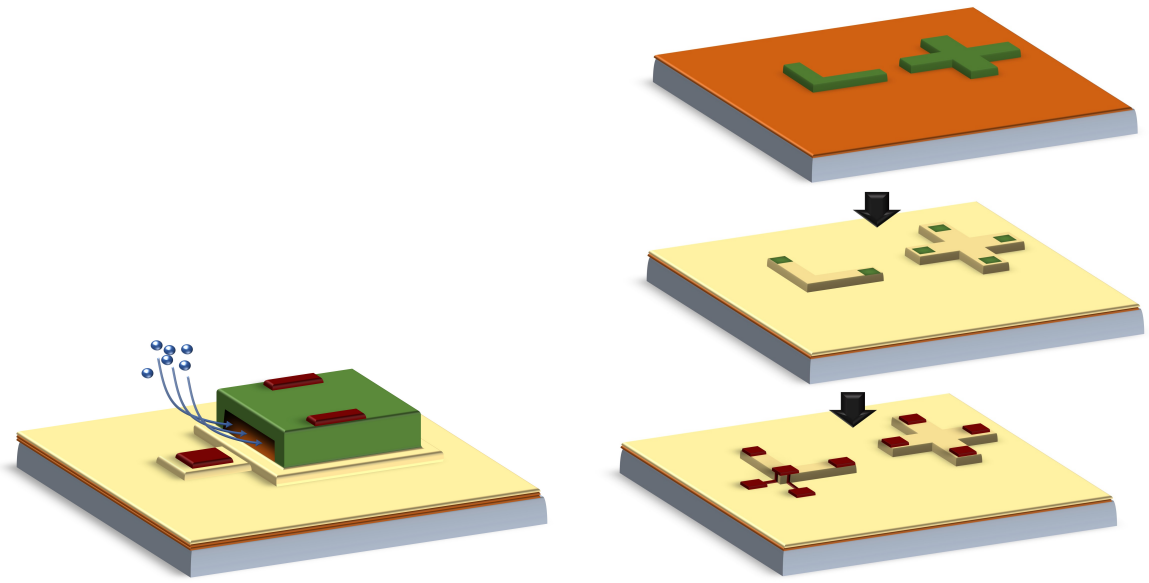


Figure 4.2: Illustration of reference structures. (a) Permitivity measurement structure; (b) Test structures adapted from literature [73].

Typical test structures are designed for the metal/SiC interface contact resistance and layer sheet resistance measurement shown in Figure 4.2b [73]. Kelvin test structure on the left is implemented for contact resistance measurement. Greek cross van der Pauw structure on the right is used for sheet resistance measurement.

4.2 PROCESS DESIGN

A complete process flow is designed for the fabrication of the device. Fabrication of the entire device requires a 10-mask process. 525 µm thick 100 mm diameter single-side polished p-type doped silicon wafers were used as substrate material. The process flow and mask design will be presented in this section, along with some critical design considerations. A 3D overview of the process flow is shown in Figure 4.3. The detailed process information will be illustrated step by step in the following paragraphs.

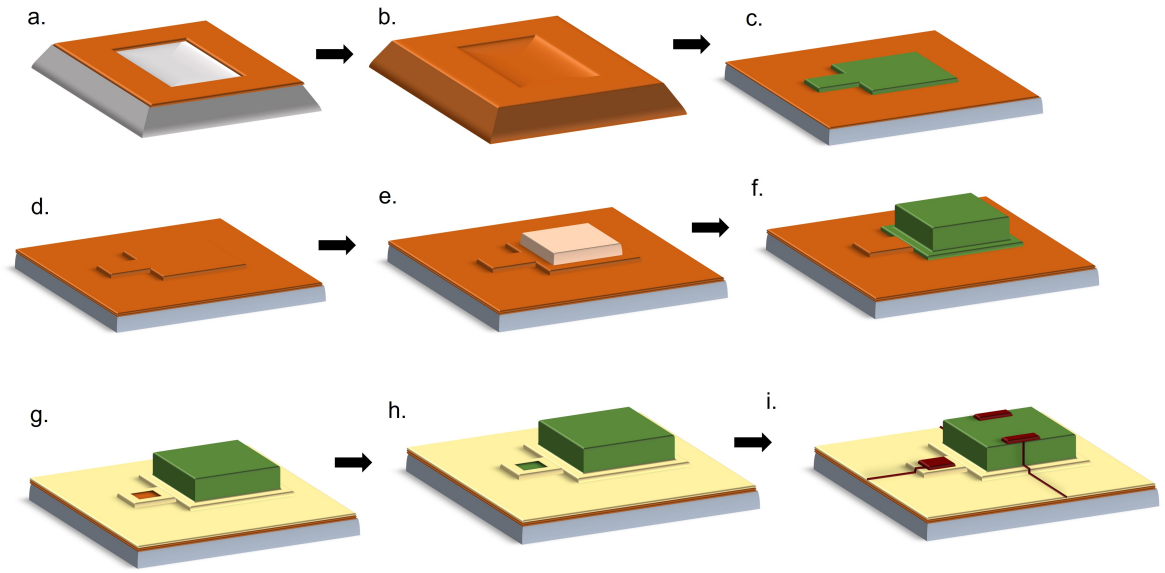


Figure 4.3: Overview of process flow.

4.2.1 Substrate cavity

A 10 µm deep well is firstly etched on substrate surface where the functional structure will be fabricated inside as shown in Figure 4.3 a, b. The silicon cavity is etched by 33 % KOH solution because the etched cavity step will be a slope for better coverage (Figure 4.4c) of the metal interconnects in future steps while dry etching produces a vertical profile. Because photoresist will dissolve in the KOH solution, a hard mask made of material that does not react with the KOH solution is required. Si_3N_4 was used at mask material because Si_3N_4 will also be used as an insulation layer on top of this layer. 200 nm silicon nitride is deposited on the substrate surface by LPCVD (Figure 4.4a) also to protect the backside of the silicon wafer during KOH etching. Nitride hard mask is then etched by RIE etcher with the pattern of the cavity (Figure 4.4b). Another layer of LPCVD Si_3N_4 is then deposited after KOH etching to insulate the above structure from the silicon substrate (Figure 4.4d). Si_3N_4 is used because the next insulation layer (insulate bottom plate

Figure 4.4: Process flow: Preparation of the substrate. (a) 200 nm LPCVD Nitride deposition as hard mask; (b) Nitride RIE etching of cavity pattern; (c) KOH etching of the well on silicon substrate; (d) 500 nm LPCVD nitride deposition for insulation.

and top plate) will be made of the same material. The same material is used to the greatest extent as base material to reduce possible thermal mismatch-induced stress and easier thickness measurement and etching.

4.2.2 Capacitor bottom plate and dielectric insulation

The capacitor bottom plate is then fabricated as the first layer on bottom of insulated substrate cavity. 500 nm ammonia-doped SiC is deposited by LPCVD with two composition of precursor gas flow of 80 sccm SiH_2Cl_2, 320 sccm C_2H_2(5% in H_2), and 60 sccm NH_3(5% in H_2) (D-4 layer in Table 3.2) and 80 sccm SiH_2Cl_2, 320 sccm C_2H_2(5% in H_2), and 30 sccm NH_3(5% in H_2) (D-2 layer in Table 3.2) at 860 °C/80 Pa. Then the layer is etched by plasma etching to create the individual pattern of capacitor bottom plate (Figure 4.5b). Figure 4.3c shows the resulted square capacitor bottom plate. The detailed deposition and etching parameters and tests will be illustrated later in Section 4.4.2.

Figure 4.5: Process flow: Capacitor bottom plate (a) 500 nm LPCVD ammonia-doped SiC deposition; (b) SiC RIE etching of capacitor bottom plate; (c) Si_3N_4 Dielectric insulation layer.

As shown in Figure 4.3d and Figure 4.5c, 200 nm LPCVD Si_3N_4 is deposited to cover the wafer functioned as both insulation layer between the capacitor plates and dielectric layer when the capacitor plates are in contact. The thickness of this layer was determined by capacitive response during device design. In the next step, sacrificial structure made of SiO_2 will be deposited and etched on top of this layer. Therefore, Si_3N_4 is used instead of SiO_2 to avoid being etched for preventing exposure of the bottom conductive layer.

4.2.3 Sacrificial structures

Sacrificial structures is then created to form the shape of the sealed capacitor cavity as shown in Figure 4.3e. The sacrificial layer will be etched after the first supportive diaphragm layer is deposited. Two sacrificial structures are designed for different release hole design and also to achieve both 1 µm (Figure 4.6c) and 2 µm (Figure 4.6d) structure height for different capacitor gap distances.

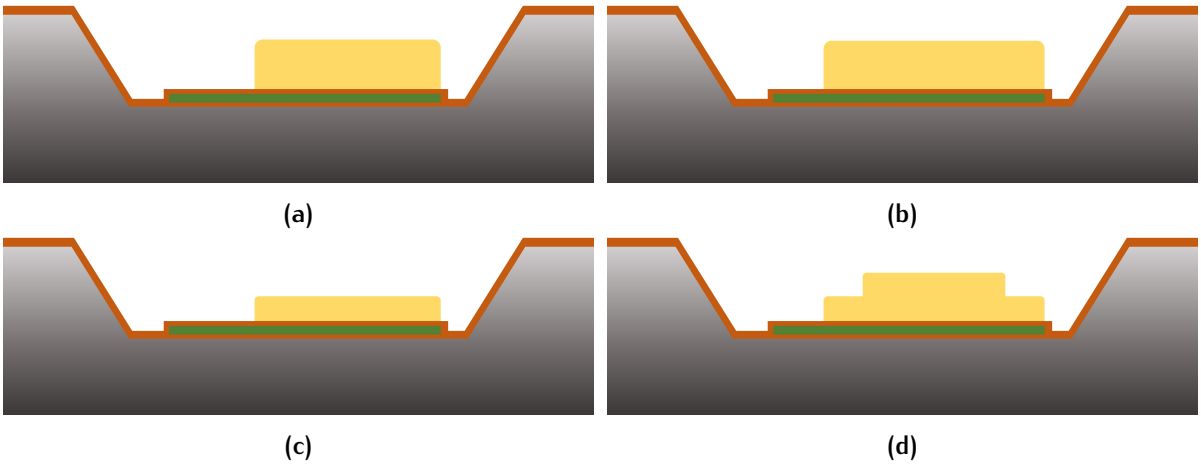


Figure 4.6: Process flow: Sacrificial structures. (a) SiO_2 sacrificial structure for top release holes design after first etching landing on insulation layer obtain 2 µm height; (b) SiO_2 sacrificial structure for side release holes design after first etching landing on insulation layer obtain 2 µm height; (c) SiO_2 sacrificial structure for top release holes design after the second etch obtain 1 µm height. (d) SiO_2 sacrificial structure for side release holes design after second etching obtains a two-step structure.

Firstly, a 2 µm thick PECVD SiO_2 layer is deposited as the sacrificial material because it can be easily etched by chemical to release through release holes in later process conpared. Then the SiO_2 layer is etched two times in BHF(1:7) solution. Wet etching is used because of its better selectivity to protect the insulating nitride layer. The etch rate of PECVD SiO_2 is around 300 nm/min, much higher compared with 12 nm/h to 18 nm/h etch rate of LPCVD nitride. A 2 µm block is obtained from the first etch for both design (Figure 4.6a and Figure 4.6b), which lands on the nitride layer at unwanted area. The second etch process removes 1 µm thick of the sacrificial block for top release hole design and leaves a 1 µm block with the same area (Figure 4.6c). 1 µm height step will be obtained from the second etch for the side release hole design as shown in Figure 4.6d. The diameter/width of the bottom part of the sacrificial layer is 16 µm larger than the top block where the release holes will be etched on top.

4.2.4 Diaphragm

Six process steps are required to obtain the pressure sensing diaphragm shown in Figure 4.3f. A D-2 layer (in Table 3.2) of LPCVD SiC will be deposited on the sacrificial structures as the first supportive layer of the pressure sensing diaphragm shown in Figure 4.7a and Figure 4.7b. Release holes is then etched through this SiC layer with RIE etcher to expose inner SiO_2 for sacrificial release.

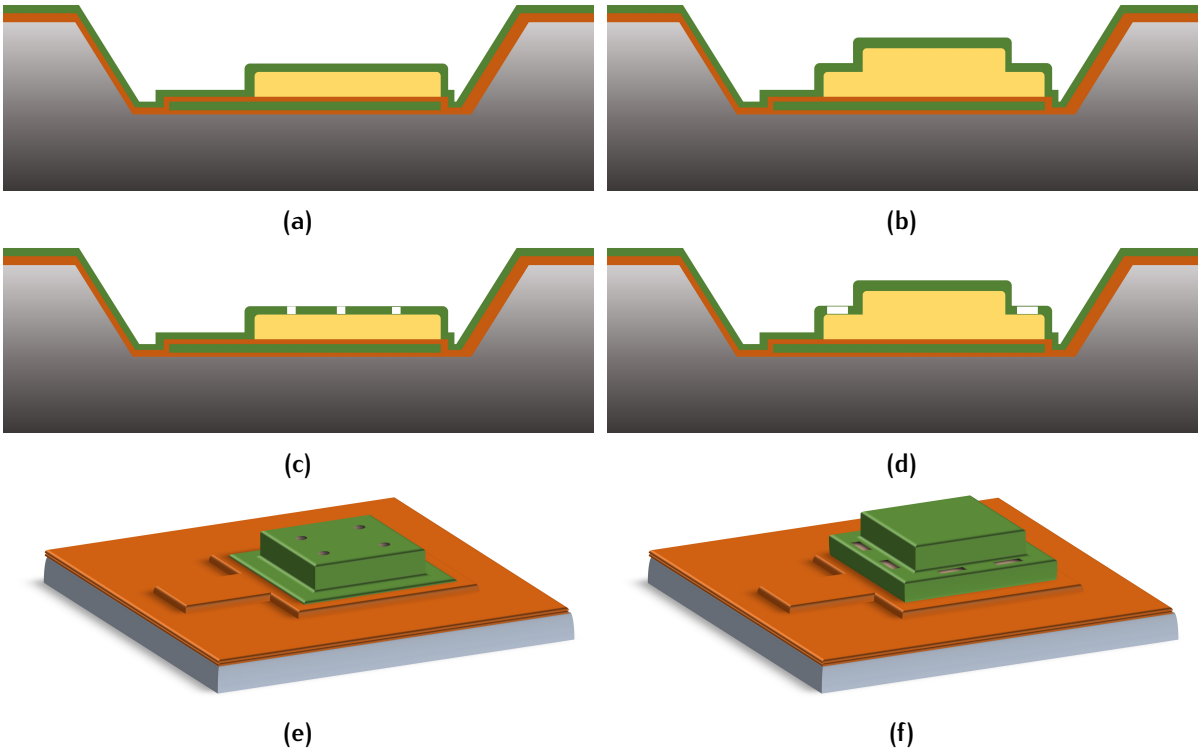


Figure 4.7: Process flow: SiC pressure sensing diaphragm (Capacitor top moving plate).
Step one: A 800 nm thick LPCVD SiC deposited on top of the sacrifical layer for (a) top release hole design; (b) side release hole design.
Step two: SiC Plasma etch through the first layer and expose the sacrifical layer for (c) 2 µm radius circular release holes on diaphragm top; (d) 10 µm × 4 µm sqaure relase holes on diaphragm side.
3D illustrattion of first SiC diaphragm layer with (e) top release hole; (f) side release holes.

Two types of release holes are designed for this step. Typical circular release holes spread on top of the diaphragm is adapted from literature [8] shown in Figure 4.7c and Figure 4.7e. The release holes are designed small enough to be sealed by another SiC layer after sacrificial release due to the anisotropic growth of the LPCVD SiC deposition. These release holes are designed to be sealed by horizontal SiC growth during the second deposition. The circular release hole is 1 µm × 2 µm large, while the second SiC deposition thickness will be 1.7 µm. Therefore, the release holes should be able to be sealed properly. Another attempt was designed for

sacrificial release. As discussed earlier, the sacrificial structure is designed with a 1 µm height, 8 µm wider step for the side release holes. 10 µm × 4 µm square release holes are etched through SiC layer on the sacrificial step and expose a larger area of SiO_2 as shown in Figure 4.7d and Figure 4.7f. These release holes are designed to be sealed vertically from the structure bottom because the exposed area is large enough for SiC to grow inside the release holes. Similarly, 1.7 µm deposition thickness should be able to cover the 1 µm height beneath the release holes.

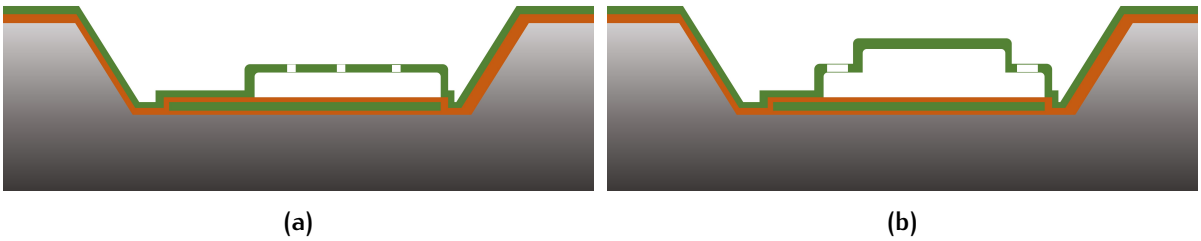


Figure 4.8: Process flow: Sacrifical SiO_2 release results of (a) top release hole design; (b) side release hole design;

The sacrificial SiO_2 is released by vapor HF etching after release holes are made as shown in Figure 4.8a and Figure 4.8b. Vapor HF etching uses vapor phase HF that flow through the release holes to reacts with SiO_2, and the reaction product will be ventilated away to remove the SiO_2 structures and creating a suspended diaphragm on top. Vapor HF etching is better than conventional wet etching because it can prevent the suspended structure from sticking to the bottom layers due to the capillary force at drying progress.

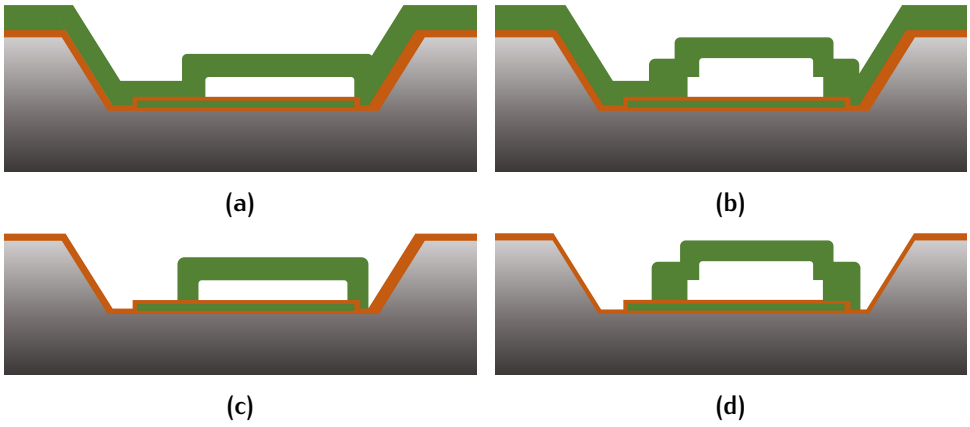


Figure 4.9: Process flow: Complete pressure sensing diaphragm. Second SiC diaphragm layer deposition with thickness of 1.7 µm on (a) top release hole design; (b) side release hole design. SiC etched landing on insulation layer leaving desired diaphragm structures for (c) top release hole design; (d) side release hole design.

1.7 µm thick SiC is deposited with the same parameters of the first layer to seal the release holes and form the complete diaphragm of the designed 2.5 µm thick-

ness. The first diaphragm layer is suspended after sacrificial release and works as a supportive structure. The top release holes are expected to be sealed along the diaphragm surface as shown in Figure 4.9a. After that, SiC at the unwanted area is etched by plasma etching and landed on the insulation layer. Note that the etch time should be carefully calculated to avoid over-etch that may also remove the insulation layer. The resulted structure is shown in Figure 4.9c and Figure 4.9d.

4.2.5 Top insulation and contact openings

In order to make sure no short circuit will occur due to over-etch of the existing insulation layer, another layer of SiO_2 or Si_3N_4 will be deposited on current structures for insulation between metal interconnects and bottom structures (Figure 4.10a, Figure 4.10b). The insulating material is determined by further process which will be discussed in Section 4.2.6.

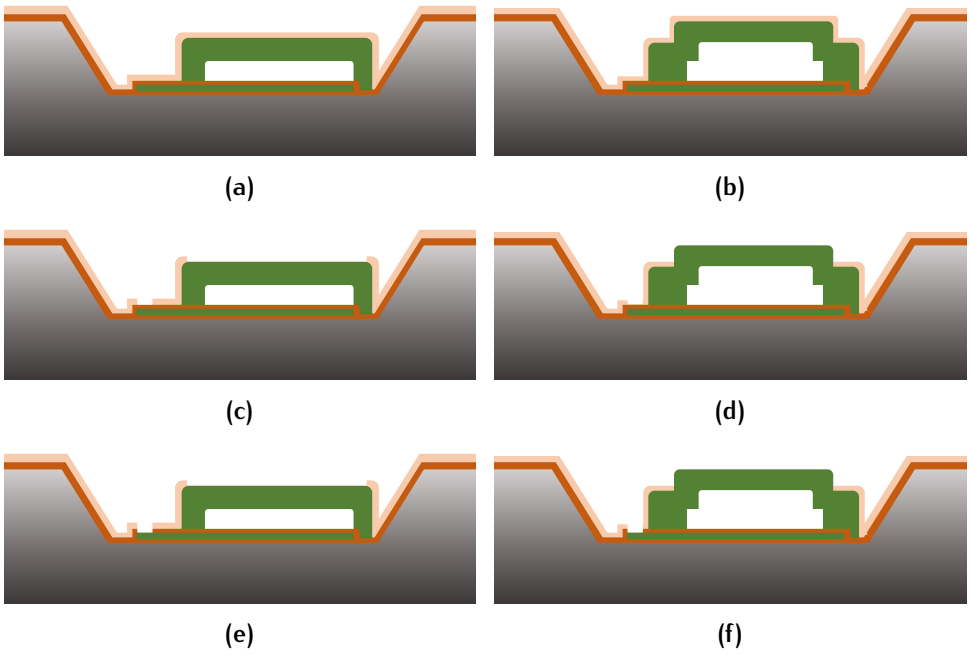


Figure 4.10: Process flow: Insulation between Interconnects and bottom structures.(a,b) Insulation layer deposition on existing structures; (c,d) Etched top insualtion layer for contact openings and expose the diaphragm; (e,f) Etched contact opening on dielectric insulation Si_3N_4 for bottom capacitor plate.

To conducting the signal from bottom capacitor plate, contact openings are etched through the insulation layers as shown in Figure 4.3g,h. Firstly, the insulation SiO_2 are etched by HF solution to expose an square contact area landing on the Si_3N_4 insulation layer between the plates (Figure 4.10b, Figure 4.10d). The SiO_2 on top of the diaphragm is also etched away to prevent the insulation material from influencing the mechanical performance of the diaphragm and to expose the diaphragm

for placing electrodes. Then the Si_3N_4 at top of bottom plate opening is etched by plasma to expose SiC layer as shown in Figure 4.10e, Figure 4.10f.

4.2.6 Metal interconnect and optional structures

A layer of aluminum with 1% silicon is then deposited and etched to exert and transmit electrical signal from the sensing structures as shown in Figure 4.3i and Figure 4.11a. The aluminum is deposited by sputtering and etched either with wet etching or plasma etching. The Etching method is tested to find out the best option. Extra etching is needed to remove the 1% silicon for wet etching.

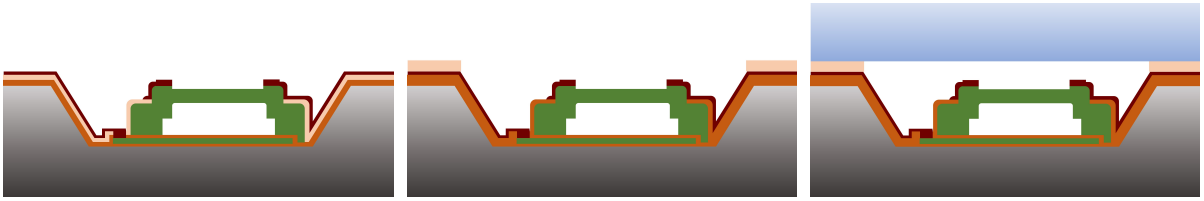


Figure 4.11: Process flow: Metal interconnections and optional structures. (a) Metal layer for electrodes and interconnects; (b) Protection layer deposited for protection of metal layer; (c)Molding compound can be implanted on top of the protection layer.

An optional protection layer can be fabricated on the outer substrate surface to protect the metal wire before molding compound glued on top of the cavity as shown in Figure 4.11c. This layer only works as protection so that this step can be skipped for simply device characterization. SiO_2 is deposited over the structures and removed by wet etching in the cavity area and the outer metal pads. If the protection layer is required, the insulation layer beneath the metal layer should use Si_3N_4 (Figure 4.11b) instead of SiO_2 because all SiO_2 inside the cavity will be removed at this step.

4.3 MASK DESIGN

The fabrication processes of micro-machined devices all rely on photo-lithography technology. In integrated circuit manufacturing, lithography is a process technology that uses optical-chemical reaction principles and chemical/physical etching methods to transfer circuit patterns to fabricated surfaces to form effective functional patterns. The basic principle of lithography is shown in Figure 4.12. A layer of light-sensitive material, photoresist, dispensed on the surface is exposed to UV

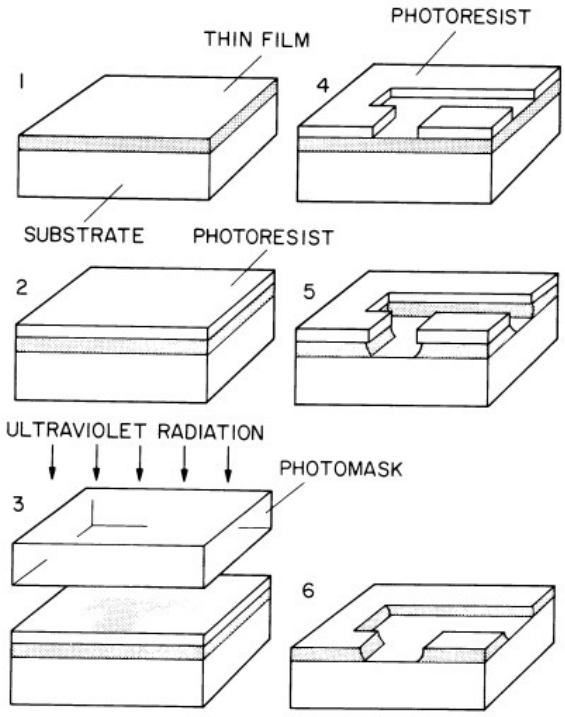


Figure 4.12: Schematic diagram of lithography process to form a patterned underlining layer [11].

light through the mask. Chemical reactions take place in the photoresist in the exposed with enough light exposure. Then the photoresist in the exposed (positive photoresist) or unexposed (negative photoresist) area is dissolved and removed by the development solution so that the pattern on the mask is copied to the photoresist film. Finally, the pattern is transferred to the substrate by etching technology. ASML PAS 5500/80 wafer stepper is used for exposure because of a required 2 µm resolution for this device (the release holes).

Photomask is an important tool for the lithography process. For each patterned layer, a mask image with the exact designed pattern is required. Masks for the wafer stepper has equivalently 21 mm effective area. Typically, four images can be designed on a single mask for 10 mm × 10 mm dies. However, the entire process for fabricating this device requires ten images in total, as mentioned earlier in Section 4.2. Therefore, a non-standard mask is designed for this process to save the mask area.

As earlier stated in the design section, 10 mm × 10 mm die size is adapted for convenient implement of molding compound for further tests. A 3 mm × 3 mm cavity is designed as a vapor accumulation cavity at the center of the die. Therefore, all the layers that will only be etched inside the cavity are designed inside 4 mm × 4 mm images. Figure A.2 shows the complete mask layout designed for this device. Two 10 mm × 10 mm images are designed for the IC layer and the top protection

layer because both layers must be etched throughout the entire die area. Then eight 4 mm × 4 mm images are designed for the inner structures.

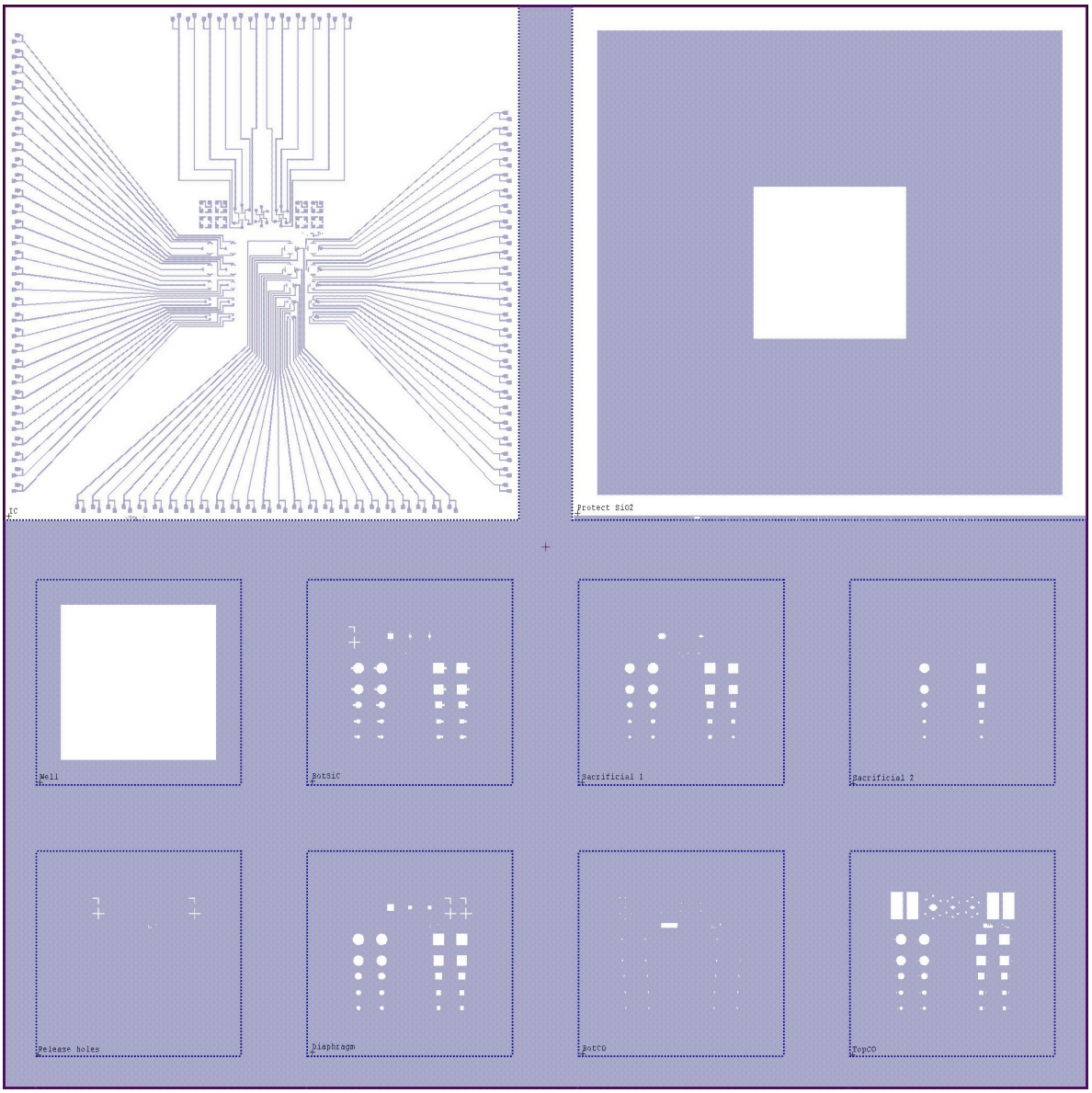


Figure 4.13: Complete mask images. From left to right, top to bottom are respectively images for: IC layer, top protection layer; substrate cavity layer, bottom capacitor plate layer, first sacrificial layer, second sacrificial layer; release hole layer, complete diaphragm layer, bottom contact openings, and top insulation contact openings.

The bright field in the mask will be exposed during the process. The die area outside the 4 mm × 4 mm will never be exposed inside the stepper, so positive and negative photoresists are used in different layers. For the layer that the outer area needs to be preserved during etching, such as the substrate cavity and the contact opening layers, the positive resist will be used; for the layer that the outer area

needs to be etched, i.e. all the sacrificial layers, the positive resist will be used. The type of photoresists and image position is listed in Table 4.1. A special sequence is then created for the stepper to exposure the selected image. The complete device layout and all mask images are attached in Appendix A.

Table 4.1: Type of photoresist, image positions and dimenations of each layer designed on the mask.

IMAGE	Layer	Photoresist	Ceneter x	Center y	Dimension
1	IC	Positive	-5500 (μm)	5500 (μm)	10 x10 (mm)
2	Protection	Positive	5500 (μm)	5500 (μm)	10 x10 (mm)
3	Substrate well	Positive	-7875 (μm)	-2625 (μm)	4 x 4 (mm)
4	Bottom SiC	Negtive	-2625 (μm)	-2625 (μm)	4 x 4 (mm)
5	Sacrificial layer1	Negtive	2625 (μm)	-2625 (μm)	4 x 4 (mm)
6	Sacrificial layer2	Negtive	7875 (μm)	-2625 (μm)	4 x 4 (mm)
7	Release holes	Positive	-7875 (μm)	-7875 (μm)	4 x 4 (mm)
8	Diaphragm	Negtive	-2625 (μm)	-7875 (μm)	4 x 4 (mm)
9	Bottom CO	Positive	2625 (μm)	-7875 (μm)	4 x 4 (mm)
10	Top CO	Positive	7875 (μm)	-7875 (μm)	4 x 4 (mm)

4.4 CRITICAL STEPS AND PROBLEMS

The designed process is verified step by step and obtained a final device. Critical steps and problems that occurred during fabrication will be discussed in this section.

4.4.1 Cavity fabrication on silicon substrate

Two methods is proposed to create the vapor accumulation cavity. The first method is to create a cavity on the silicon substrate by KOH etching using Si_3N_4 as a hard mask at the beginning of the process as shown in Figure 4.14a. The structures will be fabricated inside the cavity in the following steps. This method is able to create a more stable cavity wall. However, fabrication problem occurs due to the deep cavity. Another method is to deposit a thick layer of SiO_2 after the metal layer is fabricated also works as the protection layer shown in Figure 4.14b. This method is fabrication-friendly because of a plainer substrate surface. Both methods is verified with the entire fabrication process to find the optimal choice.

One group of silicon wafers is etched with 10 µm deep, 3 µm × 3 µm width cavity in 33 % KOH solution at 85 °C. The etch rate is tested each time a new KOH solution is mixed to select a proper etch time for an accurate cavity depth because etch rate

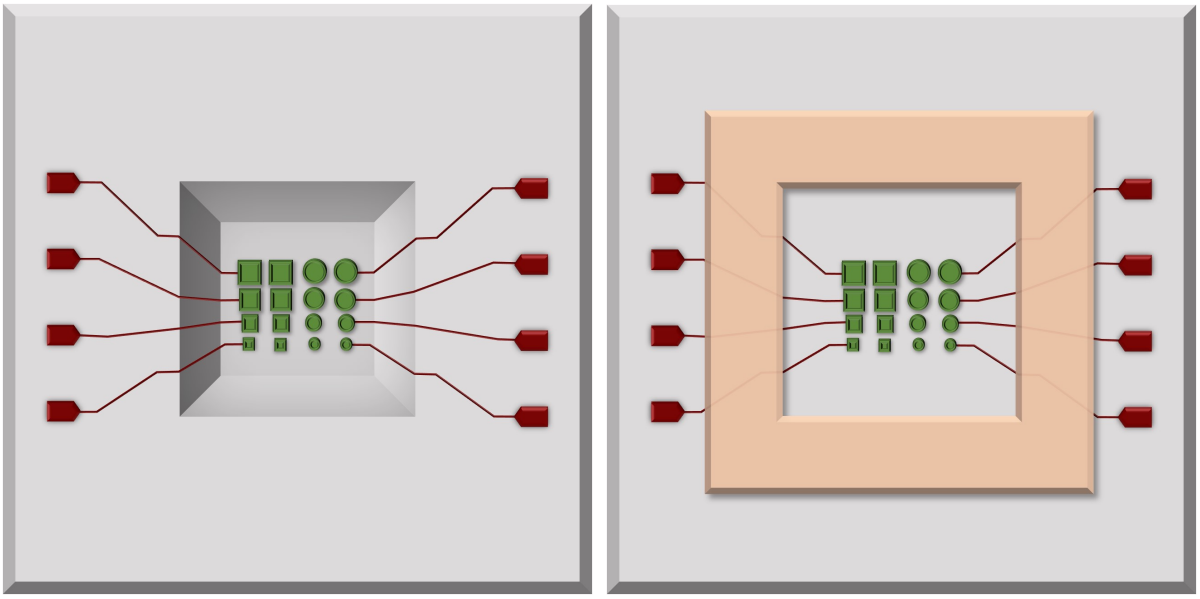


Figure 4.14: Two method for fabricating vapor accumulation cavity. (a) Created on sillicon substrate by KOH etching; (b) Create a thick SiO_2 layer after all other process steps (After metal layer).

is different due to a slight concentration variation of manually mixed KOH solution. Finally, 10.27 µm cavity was measured with Dektak 8 advanced development profiler as a result of 14 min KOH etching. Another group of wafers are not being etched to compare the fabrication viability of the two methods.

The cavity border is examined with scanning electron microscope (SEM) after each critical step as shown in Figure 4.15. A smooth cavity step is achieved after KOH etch (Figure 4.15a). However, problems occur in the lithography process during the fabrication of structures inside the cavity. The top cavity edge is not completely covered with a photoresist leading to unexpected etching on the edge area where should be protected by the photoresist. Figure 4.15b shows the unexpected etching of the cavity edge after the etching of the release holes. The possible reason for this problem is the uniform photoresist layer obtained by spin coating due to the presence of the cavity. Another problem can be observed in the same picture. The dark line shown at the bottom of the cavity indicates photoresist residuals exist at the bottom of the cavity wall. This is possible due to insufficient exposure and development because the deep cavity wall blocks part of the light and may also relate to photoresist accumulation during spin coating.

This will not be a big problem for structures inside the cavity because there are no functional structures at the cavity edge. Moreover, for the layers in earlier steps, the etched top cavity edge and higher bottom edge can be compensated by deposition of the next layer as shown in Figure 4.15c. However, this will cause unexpected etching of insulation layers during etching of contact openings, causing a nonflat cavity

surface. More importantly, the problems are deadly for the IC layer because these will cause short circuits throughout the metal wires and broken wire connection as shown in Figure 4.15d.

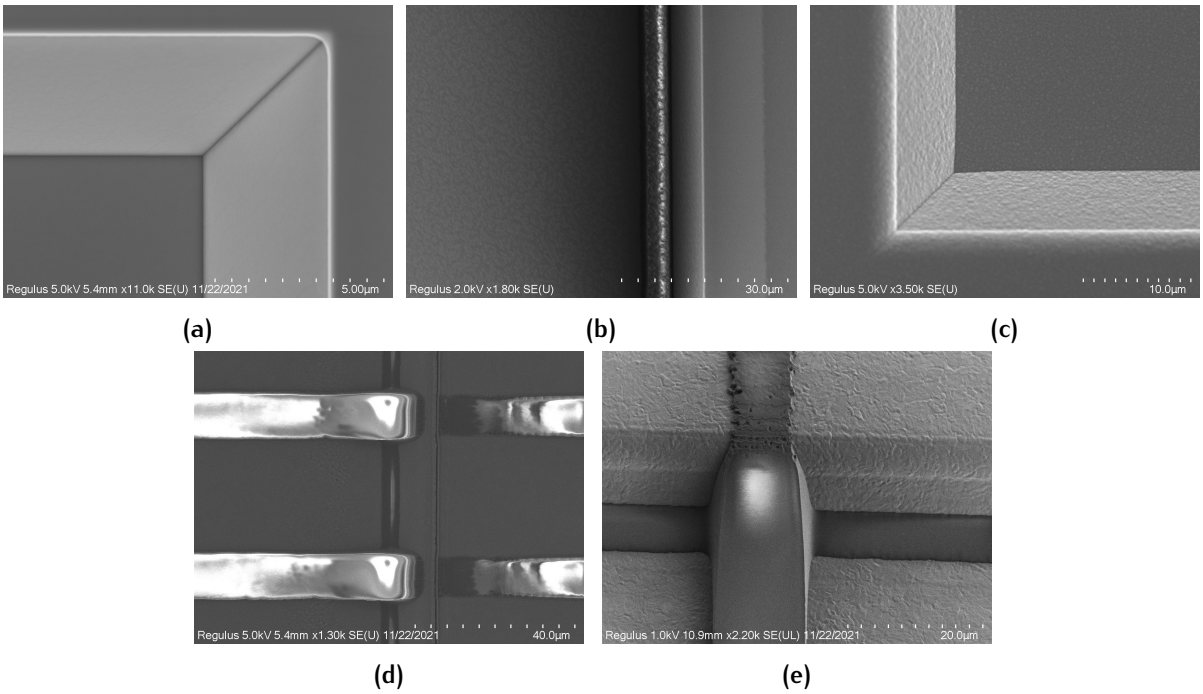


Figure 4.15: SEM image of cavity after different process steps: (a) A clear cavity corner abtained by KOH etching; (b) cavity corner with a unexpected slope along the top cavity edge after ethcing of release holes; (c)cavity corner after deposition of the decond SiC diaphragm layer; (d) disconnected photoresist pattern after developing for the IC layer; (e) accumulation of photoresist after developing for the IC layer.

Both problems are expected to be solved using spray coating instead of spin coating to spray the photoresist on the wafer for a more uniform layer. Larger exposure energy and multiple exposures can be performed along with a larger developing time to solve the problem of photoresist residual at the bottom of the cavity wall. Apart from the problems mentioned above, the first method also requires cavity depth to be measured each time before lithography to select a proper exposure focus. From a fabrication perspective, the second method is easier and has a better fabrication quality.

4.4.2 SiC deposition and etching

The process information of SiC deposition and etching is adapted from previous works [18, 69]. Test wafers are processed along with the process wafers for the measurement of layer information for each SiC layer. As insulation, the test wafers were

first deposited with 549 µm SiO_2 (measured by ellipsometer). SiC used as the bottom capacitor electrode, and pressure sensing diaphragm is respectively deposited with D-4, D-2, and D-2 layer mentioned in Table 3.2. Sheet resistance, the layer thickness is measured for each layer shown in Table 4.2.

Table 4.2: Deposition time, measured thickness, and sheet resistance of the SiC layer.

Layer function	Bottom electrode	1^{st} diaphragm layer	2^{nd} diaphragm layer
Layer ID	D-4	D-2	D-2
Deposition time	75 min	110 min	260 min
Layer thickness	540 nm	740 nm	1835 nm
Sheet resistance	120 Ω/seq	531.5 Ω/seq	316.9 Ω/seq
Resistivity	$6 \times 10^{-5}\,\Omega \cdot m$	$39.3 \times 10^{-5}\,\Omega \cdot m$	$58.1 \times 10^{-5}\,\Omega \cdot m$
Deposition rate	7.2 nm/min	6.73 nm/min	7.05 nm/min

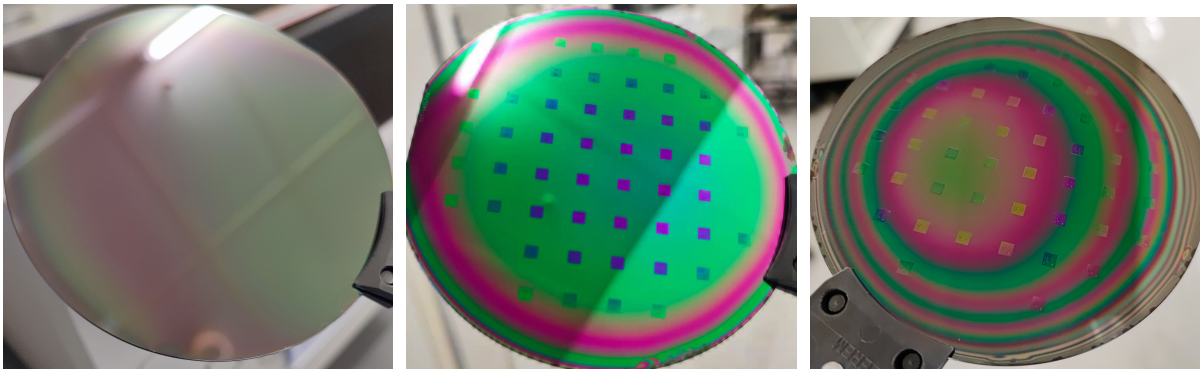
Layer sheet resistance are measured by four point probe. Uneven sheet resistance was found throughout the wafer during sheet resistance measurement. The sheet resistance of the bottom SiC electrode layer varies from 91 Ω/seq to 164 Ω/seq.

Table 4.3: Sheet resistance distribution on test wafers.

Sheet resistance	Avg.	Maximum	minimun	std.dev
Bottom electrode layer	120 Ω/seq	164 Ω/seq	91 Ω/seq	18%
1^{st} diaphragm layer	531.5 Ω/seq	710 Ω/seq	372 Ω/seq	20.1%
2^{nd} diaphragm layer	316.9 Ω/seq	242 Ω/seq	401 Ω/seq	16%

The SiC layer is etched by RIE etcher using combination of HBr and Cl_2 gas. Figure 4.16b and Figure 4.16c are taken respectively after SiC etching of the first SiC layer (bottom electrode) and the third SiC layer (complete diaphragm). Etching uniformity can be clearly observed on the wafer by the color difference. To find out the difference in etch rate, test wafers with approximately 2 µm SiC layer on 549 µm SiO_2 was etched for seven minutes. The etched step was measured after removal of photoresist. The etched step throughout the wafer is listed in Table 4.4.

The large difference in SiC etches rate caused a problem for layer insulation. The insulation layer between the bottom electrode and the diaphragm is only 200 nm thick as designed. However, the maximum difference of etched thickness for 2.5 µm diaphragm can be up to 190 nm. Totally 14 min 15 s was etched for the diaphragm layer divided by two etch sequences due to the limited survival time of 4 µm photoresist. The thickness of the diaphragm layer is measured throughout the test wafer as shown in Table 4.4. Resistivity can be derived from previously measured sheet resistance and layer thickness.



(a) (b) (c)

Figure 4.16: Wafer uniformity after (a) Deposition (b) SiC etch for bottom capacitor electrode layer; (c) SiC etch for complete diaphragm layer.

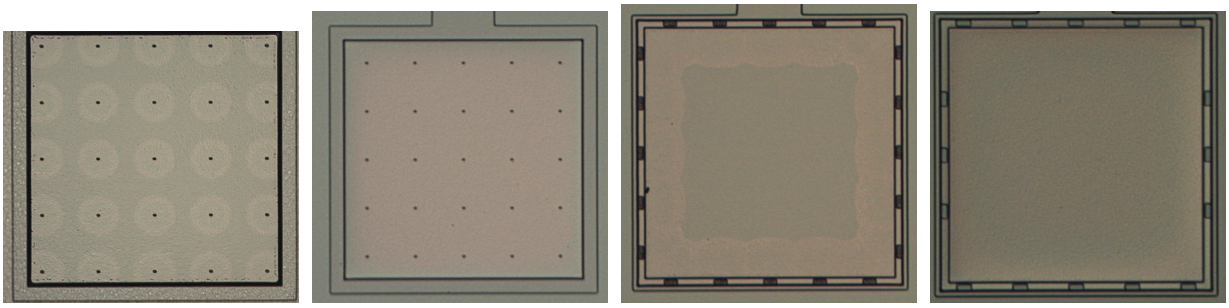
Table 4.4: SiC etch rate distribution and estimated etched thickness for diaphragm SiC layer with etch time of 14 minutes 15 seconds.

Position	Etch rate	Estimated etched diaphragm layer thickness
1.1	194 nm/min	2764 nm
1.2	192.5 nm/min	2743 nm
1.3	190 nm/min	2707 nm
1.4	183.5 nm/min	2614 nm
1.-1	196.2 nm/min	2795 nm
1.-2	196.8 nm/min	2804 nm
1.-3	196.3 nm/min	2797 nm
1.-4	190.5 nm/min	2714 nm
2.-1	196.6 nm/min	2801 nm
3.-1	195.5 nm/min	2785 nm
4.-1	190.5 nm/min	2714 nm

4.4.3 Sacrificial release and release hole sealing

As earlier explained in the process low, the fabrication of the diaphragm consists of four main steps. 2 µm PECVD SiO_2 was first deposited and etched as Sacrificial structures on the insulating dielectric layer as a support to form the capacitor cavity. Then the first SiC layer of the diaphragm was deposited on top of the sacrificial layer as support with a measured thickness of 740 nm. Release holes are etched through the SiC layer to create a path for the inner sacrificial structure to be etched away. Figure 4.17 shows the progress of vapor HF etching of the sacrificial SiO_2 through two kinds of release holes with different etch times. A suspended diaphragm is finally formed for both type of release holes as shown in Figure 4.17b and Figure 4.17d.

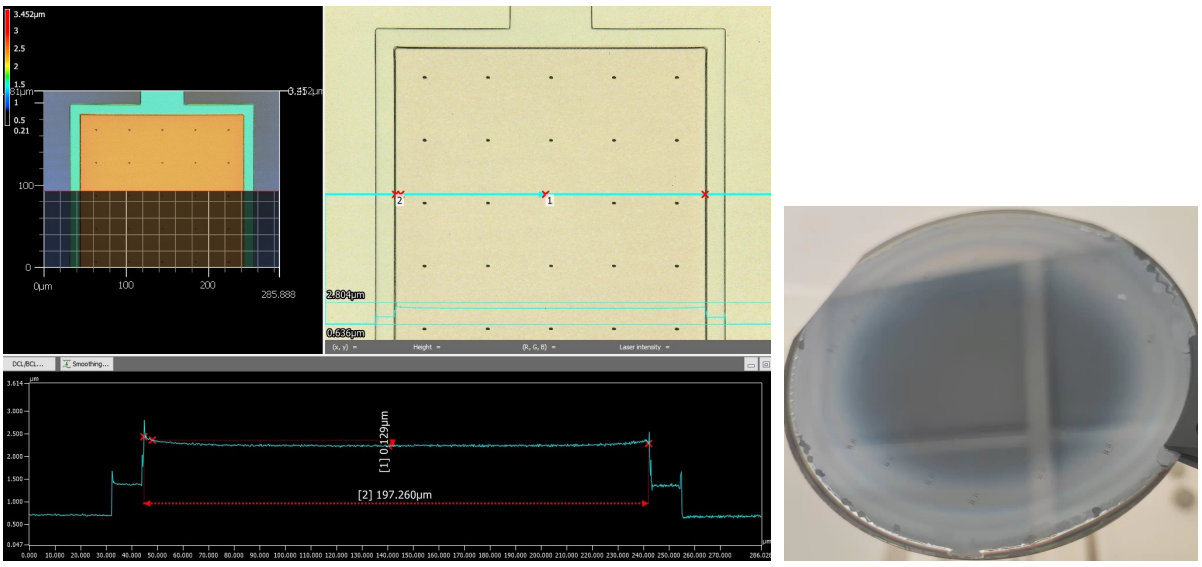
Cross-section profile of released diaphragm was examined by Keyence VK-X250 as shown in Figure 4.18a. The diaphragm bending slightly downwards due to gravity



(a) (b) (c) (d)

Figure 4.17: Results of sacrificial release. (a) Vapor HF etching of 100 minutes with top release holes; (b) Vapor HF etching of 210 minutes with top release holes; (c) Vapor HF etching of 100 minutes with side release holes; (d) Vapor HF etching of 210 minutes with side release holes.

can be observed. The shape of the diaphragm was etched on one test wafer before sacrificial releasing to etch the inner SiO_2 of the moisture testing structure designed in Figure 4.2a. However, an unexpected thin membrane was formed on the wafer surface (Figure 4.18b) due to the unwanted etching of the bottom nitride insulation surface because a ratio of SiO_2:Si_3N_4 =90:1 for HF etching results. To solve this problem, insulation PECVD SiC can replace Si_3N_4 as the dielectric insulation layer.

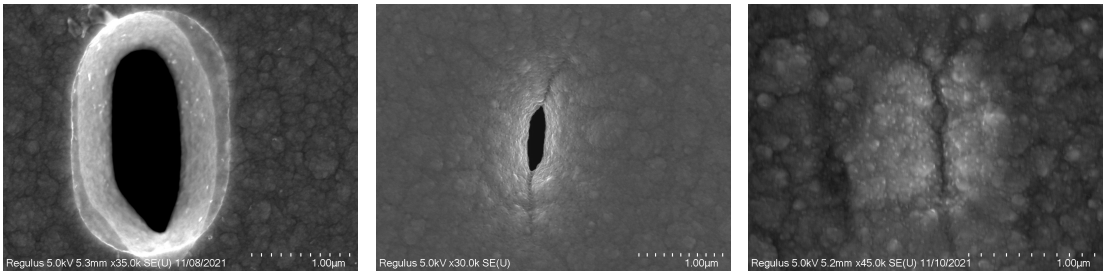


(a) (b)

Figure 4.18: (a)Diaphragm cross-section profile after sacrificial release. (b) Observed thin layer of after sacrificial release with Si_3N_4 exposed.

Suspended diaphragm formed by the first deposited SiC layer after sacrificial structure release works as a support layer for the second SiC deposition. The second SiC deposition seals the release holes and forms a complete diaphragm with measured thickness of 1835 nm to reach a total target thickness of 2.5 µm (measured

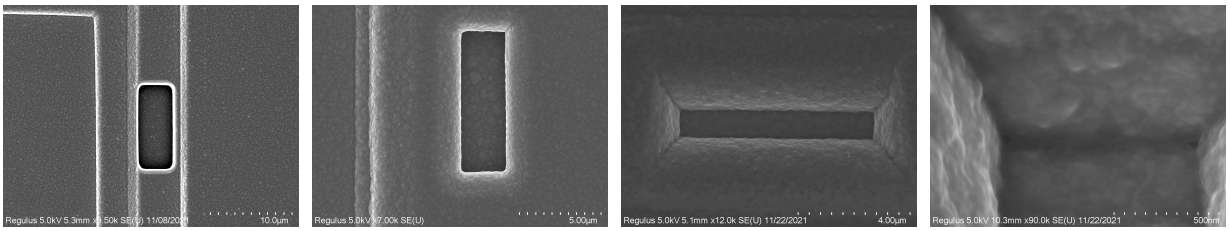
as 3576 nm in the middle die). The top release holes are sealed by the horizontal growth of SiC. Figure 4.19a shows the 2 µm × 1 µm circular release hole after sacrificial release, a clear plasma etched edge can be seen. Figure 4.19b is the result of a 170 minutes deposition of SiC on top of the first diaphragm layer. The release hole is partly sealed with a total deposition thickness of 1200 nm. The release hole is completely sealed after the complete 260 minute deposition of 1835 nm second SiC layer as shown in Figure 4.19c respectively.



(a) (b) (c)

Figure 4.19: SEM image of the top designed release hole: (a) after sacrificial release; (b) after 170 minutes SiC deposition; (c) after 260 minutes SiC deposition.

Figure 4.20a shows the 4 µm × 10 µm square release hole on the side of the diaphragm after sacrificial release. A 1 µm hole can be seen from the shadow underneath the diaphragm surface. Figure 4.20b is the result of a 170 minutes deposition of SiC on top of the first diaphragm layer. The release hole is not yet sealed with a total deposition thickness of 1200 nm growth from the bottom of the cavity. The release hole is sealed after the complete 260 minutes deposition of 1835 nm second SiC layer as shown in Figure 4.19c. The side-release hole is observed to be completely sealed with a tilted angle of 45 deg under SEM shown in Figure 4.20d.

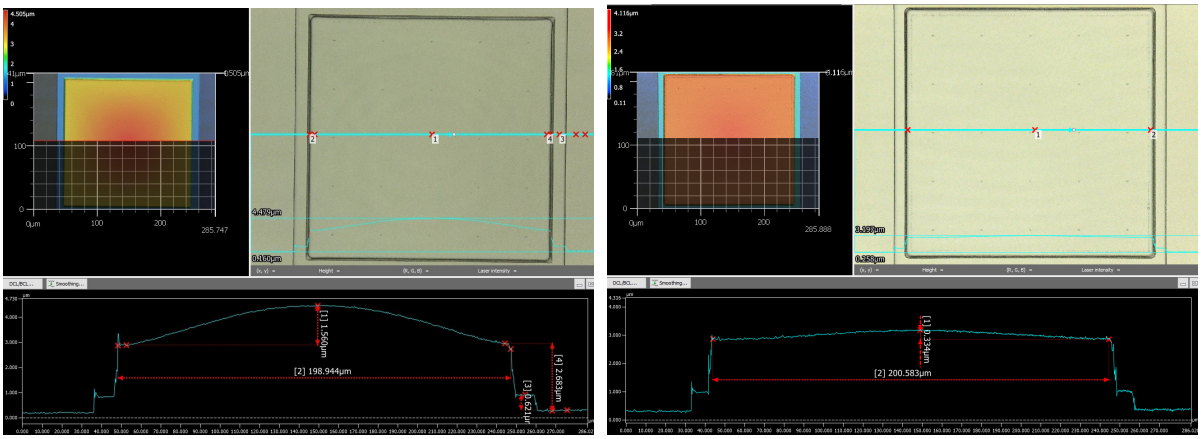


(a) (b) (c) (d)

Figure 4.20: SEM image of the sode designed release hole: (a) after sacrificial release; (b) after 2 hours SiC deposition; (c) after 4 hours SiC deposition; (d) magnified image of side hole sealed in the bottom.

Problem occurs when the diaphragm cross-section profile is examined. Theoretically, the capacitor cavity is sealed during SiC disposition under vacuum conditions, so the diaphragm should bend downwards in atmospheric pressure. However, the

200 µm × 200 µm diaphragm is bending severely upwards for around 1.5 µm as shown in Figure 4.21a after deposition of 1835 nm SiC on top of the initially 740 nm SiC layer. Another wafer was deposited two times, respectively, for 170 minutes and 50 minutes to find the difference. A maximum bending of 0.3 µm in the center of 200 µm × 200 µm diaphragm occurred as shown in Figure 4.21b. The bending of the thinner unsealed layer is smaller than, the thicker sealed layer.



(a) (b)

Figure 4.21: Diaphragm cross-section profile: (a) after second deposition of 1800 nm SiC with same carrier gas flow; (b) after second deposition of 1200 nm SiC and a third deposition of 300 nm with same carrier gas flow.

Two possible reasons for this problem are considered from the diaphragm and cavity perspective. The PECVD SiO_2 used as sacrificial material contains impurities that could leave a residual during vapor HF etching. Also, the Si_3N_4 insulation layer leaves residual during vapor HF due to over-etch. These residues may be trapped inside the cavity and vaporize or generate a new product at 860 °C SiC deposition temperature. Therefore, the cavity is filled with some other gases with pressure higher than atmospheric pressure at room temperature instead of vacuum pressure. To test this theory, another wafer was fabricated with only the first sacrificial structure release step. A 2 µm cavity was obtained beneath the side release hole. Then the same thickness of 1800 nm SiC of the process wafer is deposited, so the side release hole is not sealed for the cavity to have an atmospheric pressure. Maximum upward bending is still observed in the 200 µm × 200 µm diaphragm as shown in Figure 4.22. Therefore, the cavity gas pressure is not likely to be the reason for diaphragm bending.

Another possible cause of the unexpected bending is the different stress levels in the separately deposited SiC layer due to the difference in deposition thickness and possible difference in disposition parameters. It has been concluded that the bending is not caused by cavity pressure, then the Figure 4.21b proves the second theory. The maximum upward bending with the same diaphragm size is smaller (0.3 µm)

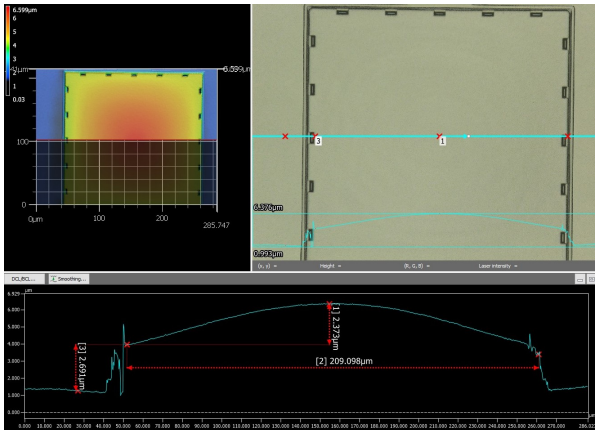


Figure 4.22: Tested diaphragm bending profile with same thickness of 1800 nm SiC on a diaphragm with atmospheric cavity pressure.

for the thinner separately deposited (1.2 µm + 0.3 µm) than bending (1.5 µm) of the thicker one-time deposited layer ((1.8 µm). Proof of the second possibility required stress analysis on the diaphragm fabricated with this method. Simulations can be used to analyze the stress distribution with a given process. Stress on the difference disposition layer can also be measured in the future.

Maximum bending of different diaphragm size is shown in Figure 4.23 for device performance reference. Upward bending of smaller diaphragm is smaller than larger diaphragms.

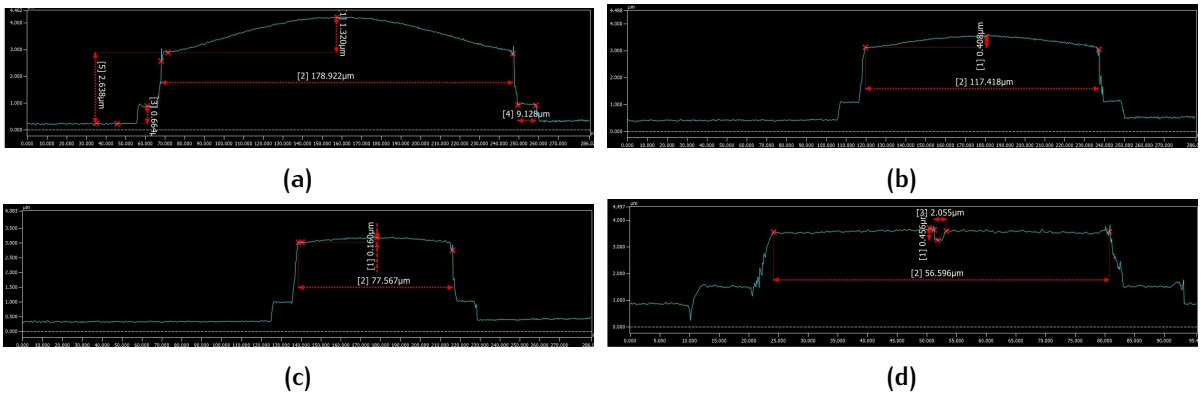


Figure 4.23: 2.5 µm thick diaphragm cross-section profile with designed diaphragm size of: (a) 180 µm × 180 µm; (b) 120 µm × 120 µm; (c) 80 µm × 80 µm; (d) 60 µm × 60 µm.

4.5 FABRICATED DEVICE AND MEASUREMENTS

Regardless of the problems that occurred in the process, a functional wafer is fabricated with designed structures. SEM image of the fabricated structures is shown in Figure 4.24. All the pressure sensing structures with various diaphragm shape and release hole shapes are presented with a clear view of the bottom capacitor electrode plate, the pressure sensing diaphragm, contact openings, and metal wire connections. The defects on the metal wires are caused by wet etching and may slightly influence wire resistance. Figure 4.24d shows the reference structure with 2 µm SiO_2 as dielectric layer. In the future, the SiO_2 can be easily etched to form a moisture sensing device with exist mask by performing vapor HF etching after etching of the diaphragm and using PECVD SiC as the insulating dielectric layer as etch barrier.

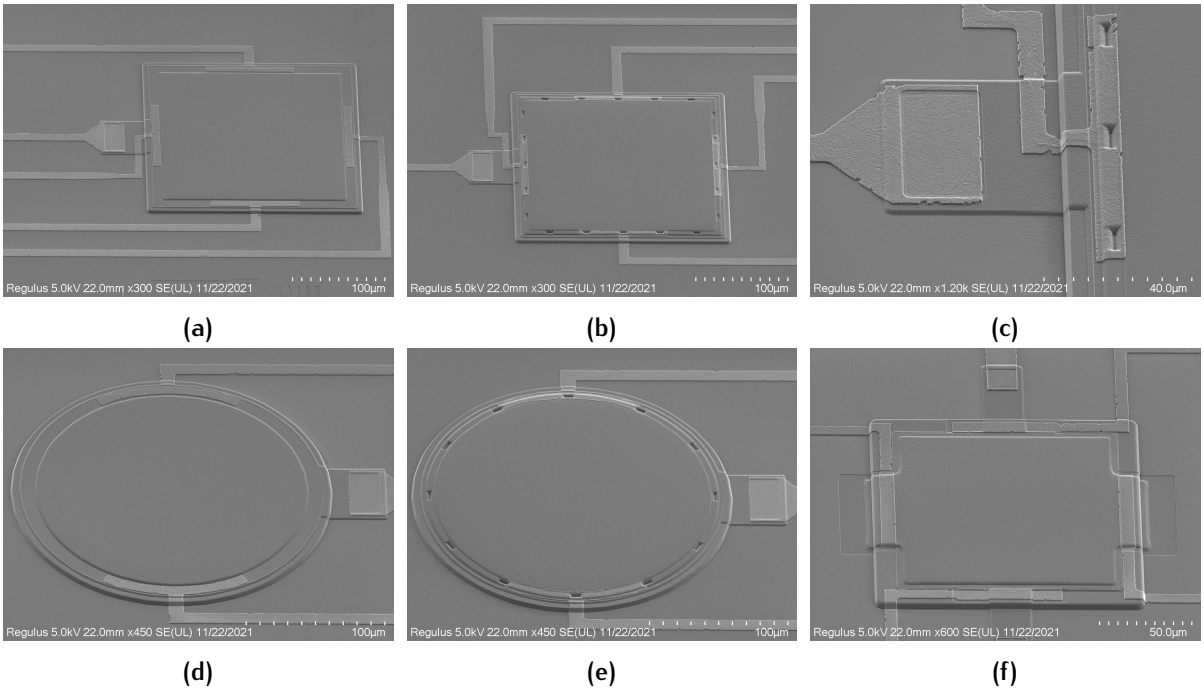


Figure 4.24: SEM image of the fabricated structures: (a) pressure sensing structure with square diaphragm with top release holes; (b) pressure sensing structure with square diaphragm with side release holes; (c) wire connection for the bottom plate and the diaphragm; (d) pressure sensing structure with circular diaphragm with top release holes; (e) pressure sensing structure with circular diaphragm with side release holes; (f) reference structures.

Initial capacitance under atmospheric pressures is measured by the micro probe station for each structures. Capacitance for different square diaphragm size is summarized in Figure 4.25. The capacitance rises with diaphragm size for 60 µm × 60 µm, 80 µm × 80 µm, and 80 µm × 80 µm. This prediction fits the theoretical trend discussed in the design chapter. However, the capacitance decreases suddenly for

larger diaphragm size of 180 µm × 180 µm, and 200 µm × 200 µm. This is because the diaphragm starts to bend more upwards than the small diaphragms, the influence of capacitor gap increase is larger than diaphragm size increase.

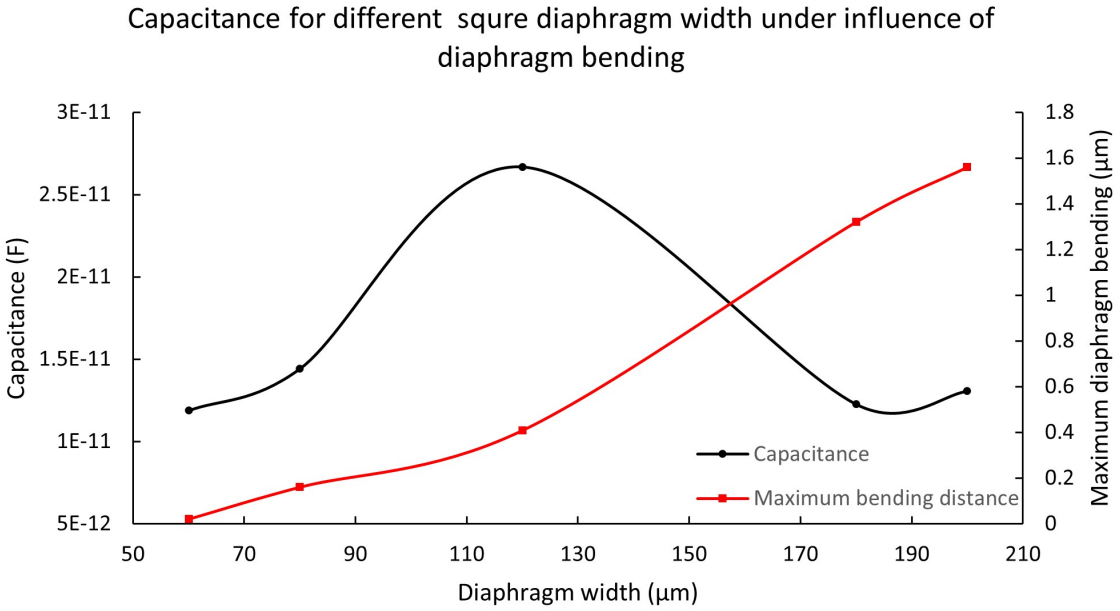


Figure 4.25: Measured initial capacitance of different diaphragm size under the influence of diaphragm upward bending.

The measured capacitance for the diaphragm is at the pF level, almost 1000 times larger than the simulated value. This is possibly due to leakage current between the diaphragm. As earlier mentioned in the fabrication problem, the insulation Si_3N_4 layer may be partly etched during the vapor HF etching of sacrificial oxide. Therefore, some part of the diaphragm is in contact with the bottom capacitor electrode plate, causing a constant current through the capacitor, increasing the total integrated current for capacitor calculation. A reference capacitor with SiO_2 as the dielectric layer, which provides excellent insulation, is measured to verify this explanation. The measured data is shown in Table 4.5.

Table 4.5: Comparison measured capacitance of capacitor with or without SiO_2 dielectric.

Structure type	Capacitance	unit
60 µm × 60 µm diaphragm without SiO_2 dielectric	11.9	pF
120 µm × 120 µm diaphragm without SiO_2 dielectric	26.7	pF
60 µm × 60 µm diaphragm with SiO_2 dielectric	0.34	pF
120 µm × 120 µm diaphragm with SiO_2 dielectric	0.66	pF

An obvious decrease in capacitance can be observed for SiO_2 dielectric between the plate. The simulated capacitance of the 120 µm × 120 µm is 37 fF (in Figure 3.11) 17

times smaller than the measured capacitor value of 660 fF. This can be explained by the difference in structure. Fist of all, the dielectric constant of PECVD SiO_2 is larger than air constant reported from 3.9 to 4.5 [74]. The actual distance is 0.935 µm, slightly smaller than the simulated parameter. Furthermore, parasitic capacitance exists between the surrounding diaphragm layer and bottom capacitor electrode insulated only by 200 nm Si_3N_4, introducing a capacitance in parallel with the functional capacitor. Therefore, the increase of capacitance in the designed structures is very likely due to capacitor plate leakage caused by over-etched insulation dielectric Si_3N_4 layer.

4.6 CONCLUSION

This chapter demonstrated the complete fabrication process of the touch-mode capacitive vapor pressure sensor. The complete process flow illustrate in Section 4.2 and the designed mask is verified by a complete fabrication of the device. Critical fabrication steps are described with results. Possible reason and solutions are analyzed for encountered problems during fabrication except for complex problem such as uneven deposition and etch rate of SiC. Finally, the fabricated pressure sensing structures and reference structures are measured. The deviation between measured results and simulation results are explained.

5 CONCLUSIONS AND FUTURE WORK

5.1 CONCLUSION

This thesis provides a complete workflow for the realization of a pressure sensor in the application of popcorn failure analysis. Firstly, the popcorn failure mechanism was studied for design of the vapor pressure sensor. Specifications and design considerations are presented based on the conclusion from literature review of failure mechanism. Different types of pressure sensors are evaluated and selected for this thesis. A touch mode capacitive vapor pressure sensor is then designed to meet the requirements. Simulations are performed to verify the designed structure and provide data for parameter selection. Fabrication process for this sensor is designed along with the photomask. Finally, the device is fabricated and measured with initial capacitance. Problems that occurred during fabrication and characterization are described, analyzed, and solutions are suggested. Conclusions are summarized as follows:

1. Vapor pressure generated by moisture trapped in the molding compound is one of the leading causes of popcorn failure. Vapor pressure level at reflow process is mainly determined by current temperature and precondition humidity.

2. No direct measurement has been published to measure vapor pressure or moisture level evolution with reflow temperatures changes.

3. The maximum reflow temperature can be up to 290 °C, in this temperature, the saturated vapor pressure reaches 7.45 MPa and the actual vapor pressure could be higher than the saturated value [10, 68].

4. Specification of the vapor pressure sensor is concluded from the last point. Required sensor operating temperature range is from room temperature to 300 °C. Measured pressure should be ranging from atmospheric pressure to 8 MPa. Sensitivity is required for the sensor to recognize 0.1 MPa for pressure ranges from 1 MPa to 8 MPa, and 0.01 MPa for pressure lower than 1 MPa. The resolution of the pressure sensor is also determined by the readout circuit.

5. Two vapor pressure models were studied, micro-mechanics based model and Henry's law based model. The micro-mechanics based model provides vapor pressure evolution throughout the molding compound with a micro-void assumption [10]. Henry's law based model provides the vapor pressure evolution with an initial cavity [3].

6. MEMS piezoresistive and capacitive pressure sensors are the most common type in the market. The potential sensitivity of piezoresistive and capacitive sensors can meet

the requirements with proper structure design and material selection. These two types of sensors are considered for this thesis because of less complexity, smaller size, and easier to fabricate compared to other sensors.

7. Touch mode capacitive pressure sensor is finally designed for application of this thesis because of its high sensitivity, improved dynamic range, less temperature dependency, improved linearity, high temperature comparability, and fabrication viability in EKL. Absolute pressure measurement is designed due to possible environmental parameter change.

8. Material is selected for device structures considering accessibility, performance, and fabrication complexity based on previous work. Ammonia-doped LPCVD poly-SiC is used for pressure sensing diaphragm and capacitor bottom electrode plate because of its higher Young's modulus, fracture toughness, and stable performance at temperature up to 300 °C.

9. Device functional structures are designed inside a vapor accumulation cavity to protect delicate structures and easy implementation of the tested object (moisture contained polymers). This design is based on the conclusions adapted from literature. A uniform vapor pressure distribution throughout the molding compound is obtained with sufficient precondition humidity and time [1]. The vapor pressure diffused into the cavity can be quantified by the vapor pressure model published by Shirley, and the pressure reduction is smaller for a smaller cavity depth and larger thickness of molding compound [3].

10. Two methods for fabricating the cavity are designed and fabricated. The method of creating a wall with SiO_2 protection structure around the already fabricated structures is better than etching a cavity on silicon substrate before fabrication of other structures because the first method is easier for fabrication and obtains better fabrication quality.

11. An irregular ten images photomask with different image sizes is designed to save mask area and reduce costs.

12. Two types of sacrificial release structures are designed and verified. Both are successfully used for sacrificial release and sealed with a second SiC deposition. The side-release-hole design is a new method brought up in this thesis to enable fabrication of this device with lower resolution and accuracy requirements for the equipment.

13. An expected diaphragm upward bending is observed. The cause is most likely to be a stress mismatch between the two SiC diaphragm layers due to thickness difference and a slight difference in deposition conditions.

14. Uniform SiC deposition and etching are reported. The standard deviation of deposited SiC layer sheet resistance throughout the wafer reaches maximum 20.1 % during fabrication. Moreover, a maximum etch rate difference of 13.3 nm/min severely influenced accurate fabrication of the device.

15. Touch mode capacitive pressure sensors are designed with an initial theoretical capacitance of dozens of fF levels. The measured initial capacitance is a few pF due to leakage between the plates. The leakage current is possibly due to an over-etch on the

Si_3N_4 dielectric layer during vapor HF sacrificial SiO_2 etching. A possible solution is to use intrinsic siC instead of Si_3N_4 as a dielectric insulation layer.

16. Five diaphragm sizes (60 µm × 60 µm, 80 µm × 80 µm, 120 µm × 120 µm, 180 µm × 180 µm, 200 µm × 200 µm), two capacitor air gap distance (1 µm, 2 µm), two diaphragm shape (circular and square), reference capacitors (Fixed capacitor with SiO_2 dielectric insulation, moisture level reference capacitor), and test structures (sheet resistance measurement, contact resistance measurement) are designed on the device to test device performance.

17. Measured capacitance change is influenced by upward bending of large size diaphragms (180 µm × 180 µm, 200 µm × 200 µm). Capacitance change of smaller diaphragm size fits the simulated result.

5.2 LIMITATIONS AND FUTURE WORK

As the first attempt in vapor pressure sensor development for popcorn failure analysis, this thesis only brought up a design option with process verification due to the limitation of master thesis workload. Possible reasons and promoted solutions to some problems still need to be verified. Full characterization of materials and the device is also needed to evaluate after solving the problems. A list of possible future work is present below:

1. A full device characterization should be performed before and after improvement of the device with existing problems, such as capacitance response curve with designed pressure load under different temperatures, resistance change under different pressure and temperatures, contact resistance, parasitic resistance, and parasitic capacitance.

2. The unexpected upward bending of the diaphragm should be detailed analyzed by mechanism simulation, layer stress characterization, and further tests. The recipes for SiC deposition and etching should be improved for more accurate fabrication of delicately designed devices. A touch mode capacitive pressure sensor with a dielectric insulation layer made of insulating SiC should be fabricated to solve the leakage between the capacitor plates.

3. The molding compound needs to be fabricated on top of the device for vapor pressure measurement. The implantation methods should be tested. A complete experiment should be performed. The complete device with molding compound sealed the vapor accumulation cavity should first be exposed to a designed precondition environment for sufficient time, then heat the device in a controlled environment with typical reflow temperature change. The sensor readout should be monitored throughout the

process to give a pressure response curve. The measured data can be used to compare with theoretical models and provide essential data for popcorn failure analysis.

4. A complete test chip with other sensors, such as moisture sensors, temperature sensors, stress sensors, and readout circuits integrated on top can be developed. A special packaging method of the test chip can also be developed for inline measurement of the vapor pressure, moisture level, temperature, and structure stress during the reflow process for characterization of different polymers.

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A MASK IMAGES

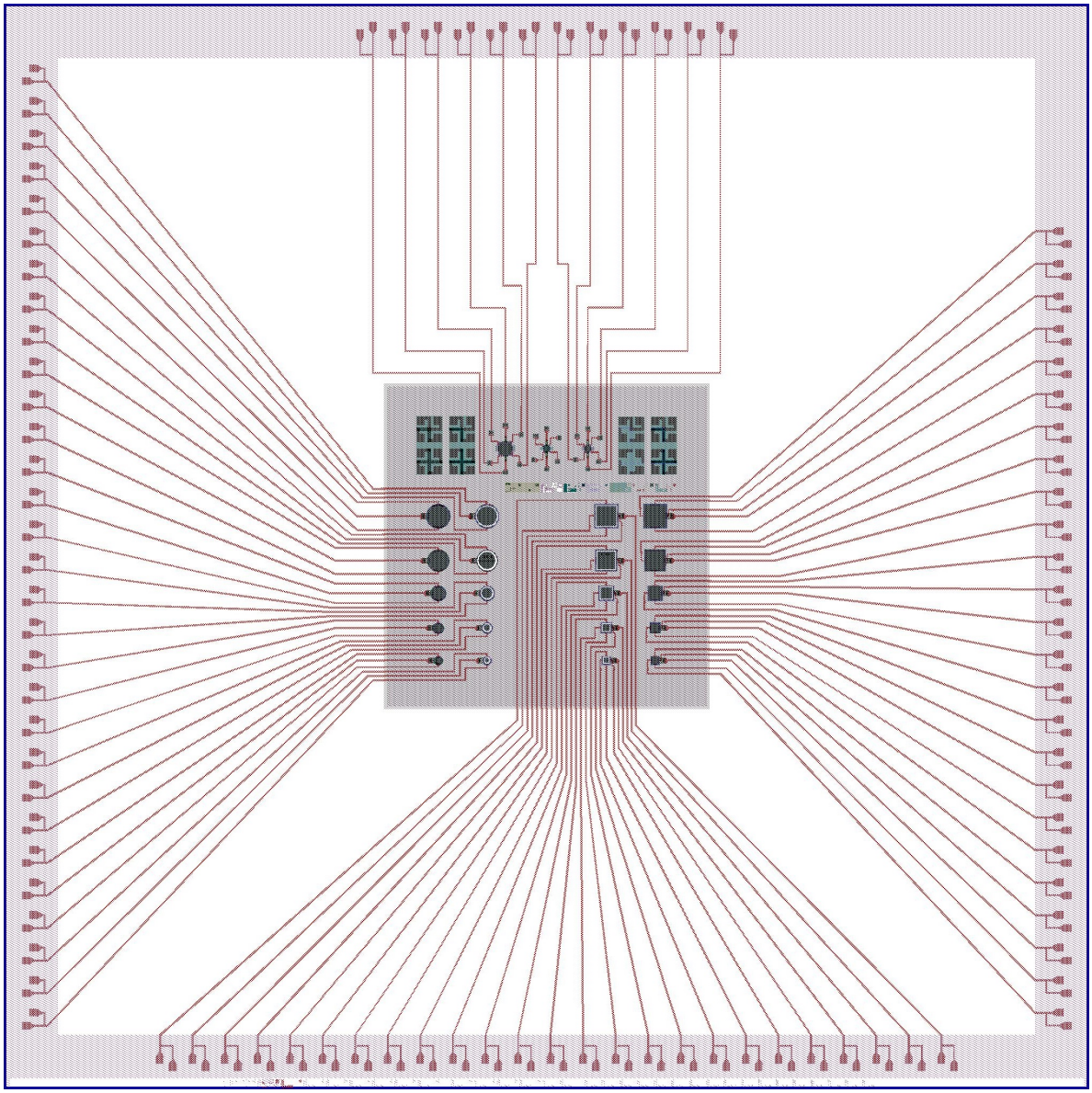

Figure A.1: Complete mask stack in 10mm structures

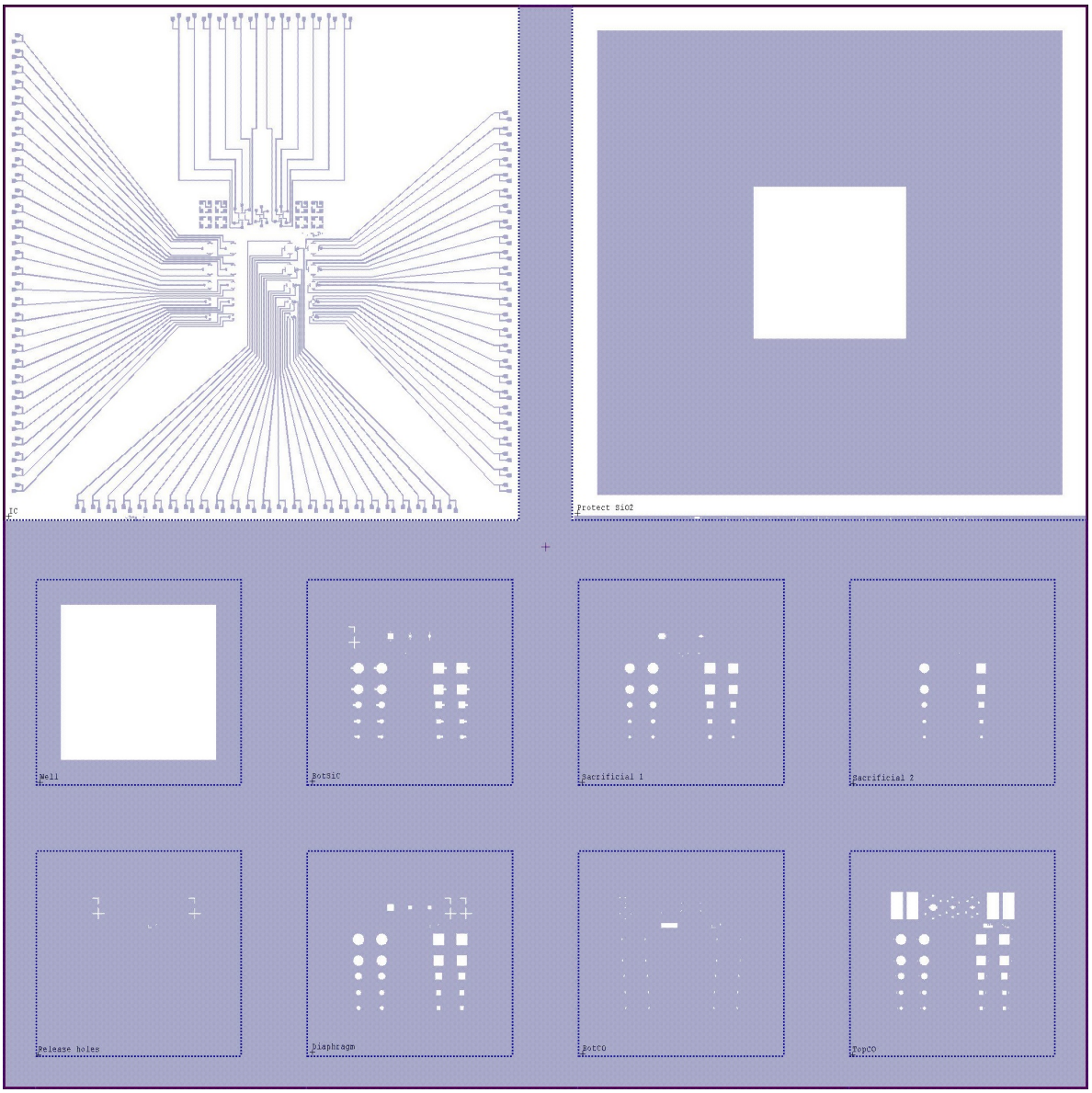

Figure A.2: Mask complete top cell marked

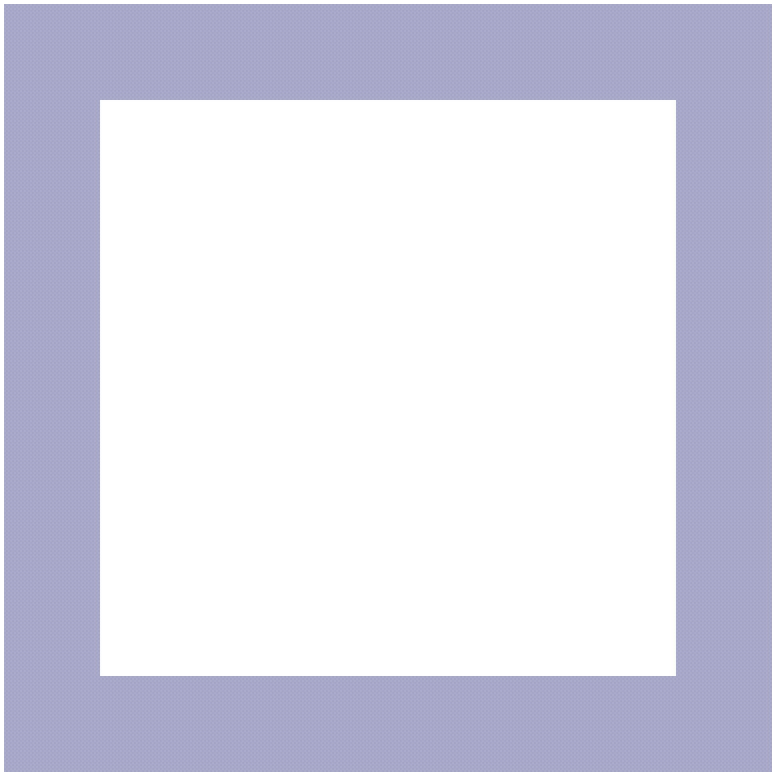

Figure A.3: Cavity

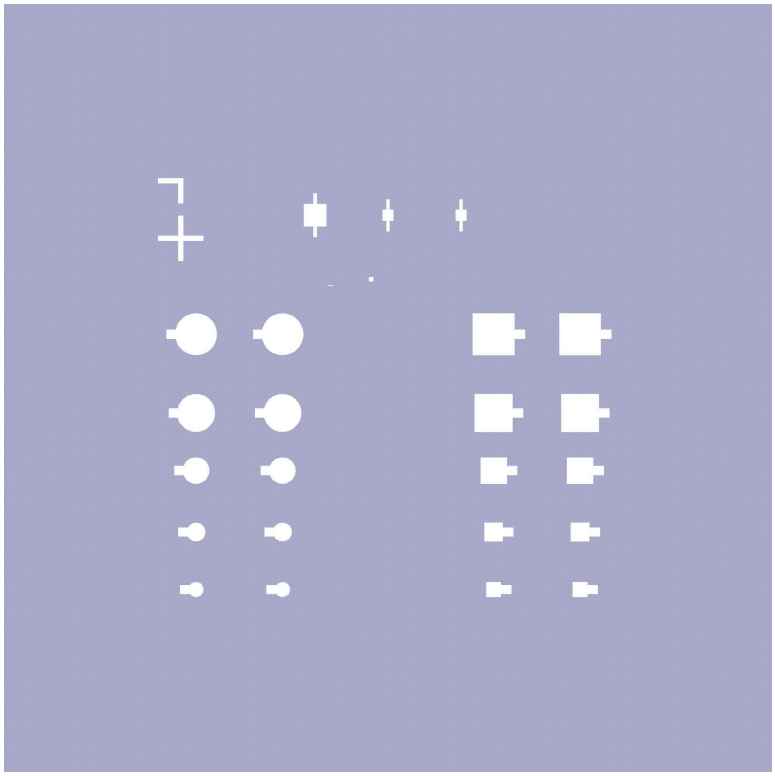

Figure A.4: Bottom SiC

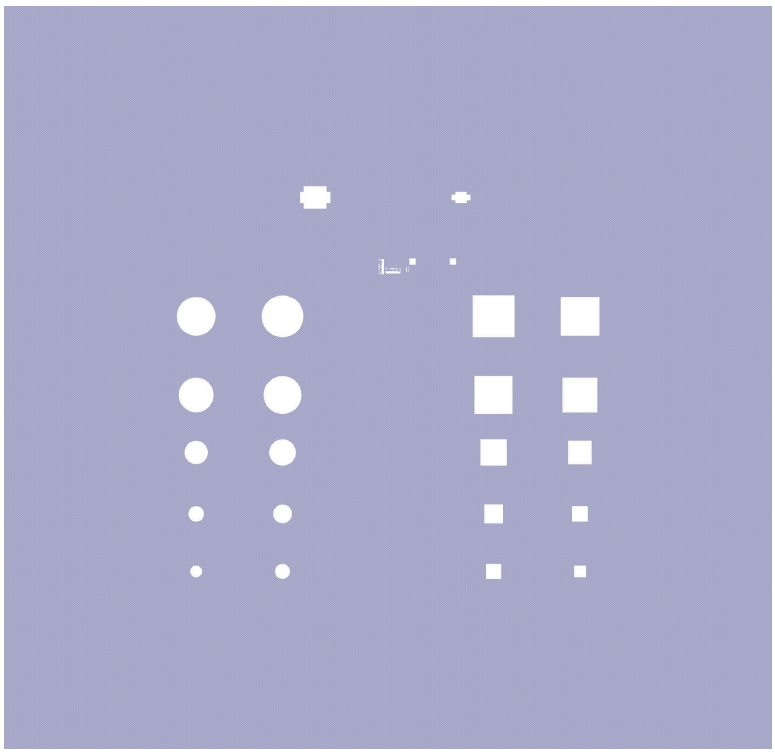

Figure A.5: Sacrificial layer 1

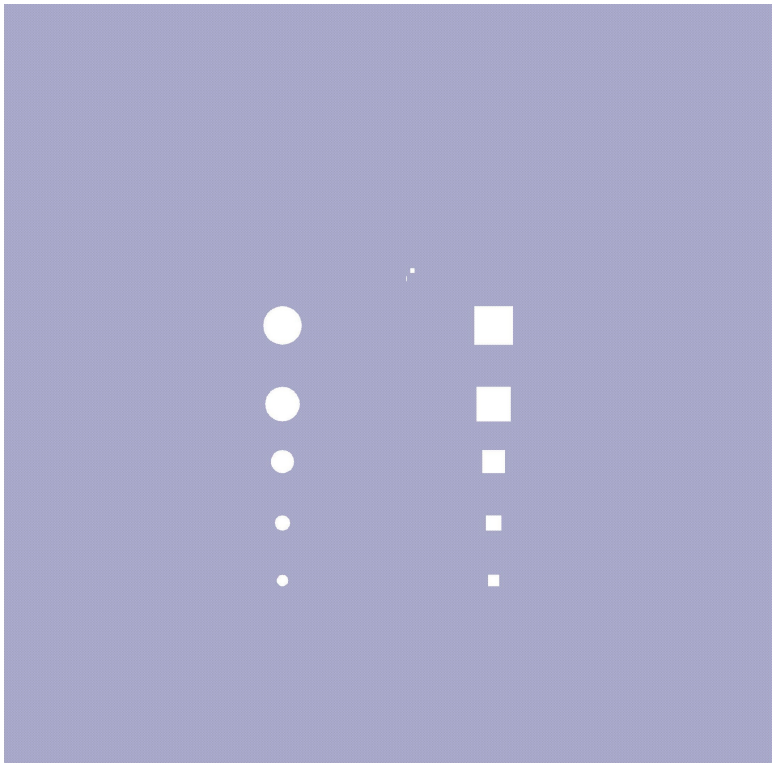

Figure A.6: Sacrificial layer 2

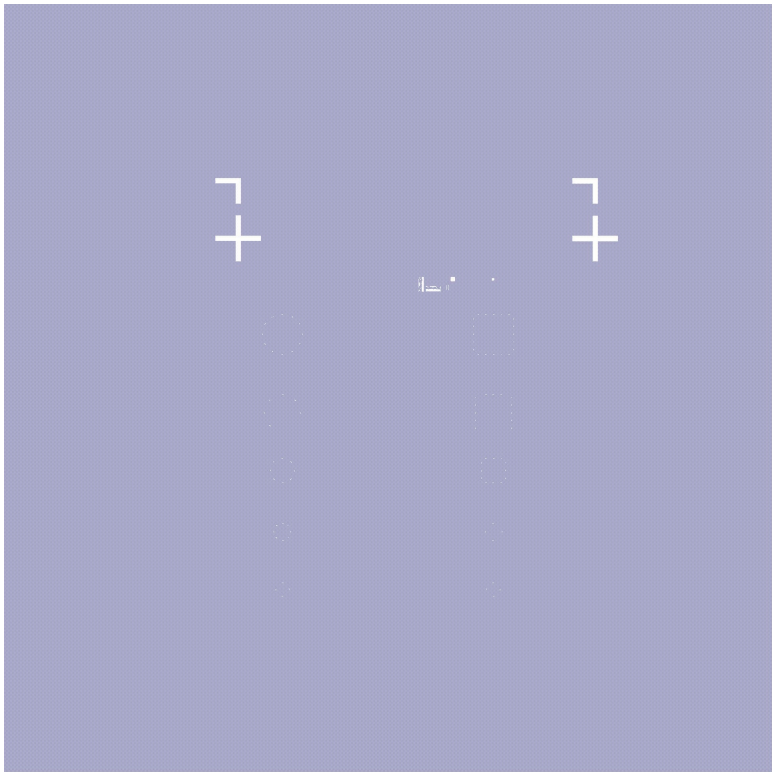

Figure A.7: Release hole

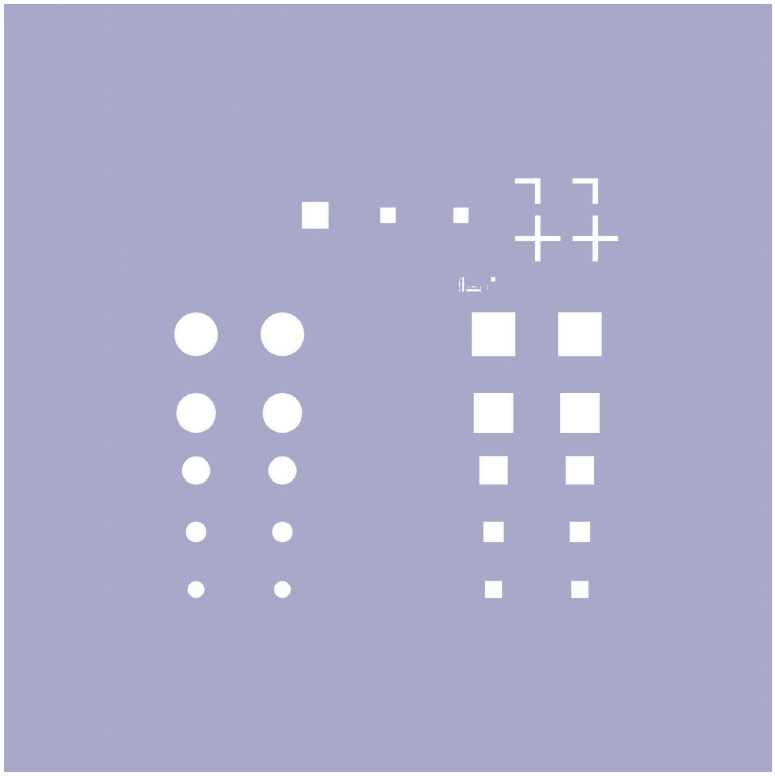

Figure A.8: Diaphragm

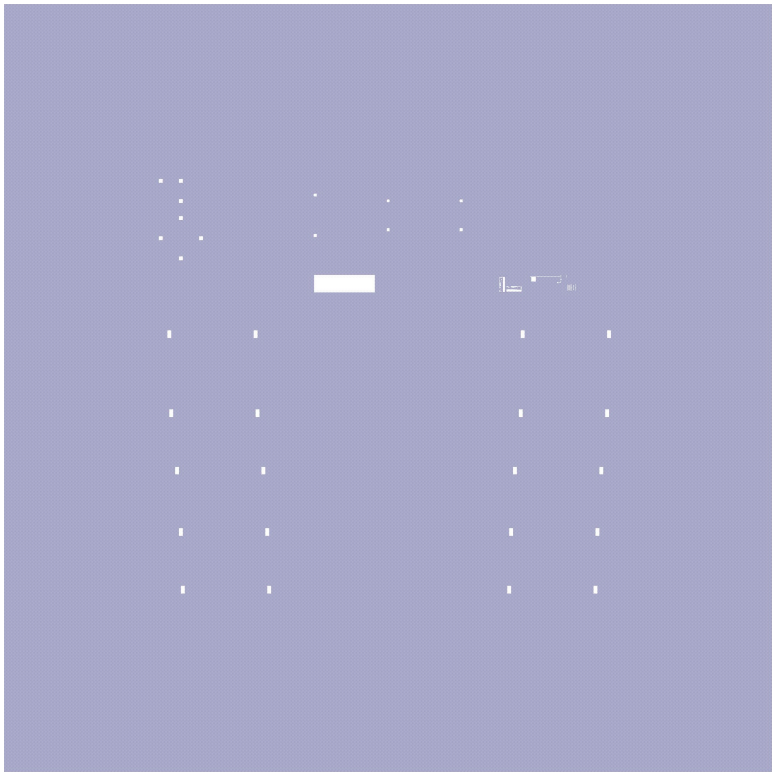

Figure A.9: Capacitor bottom plate

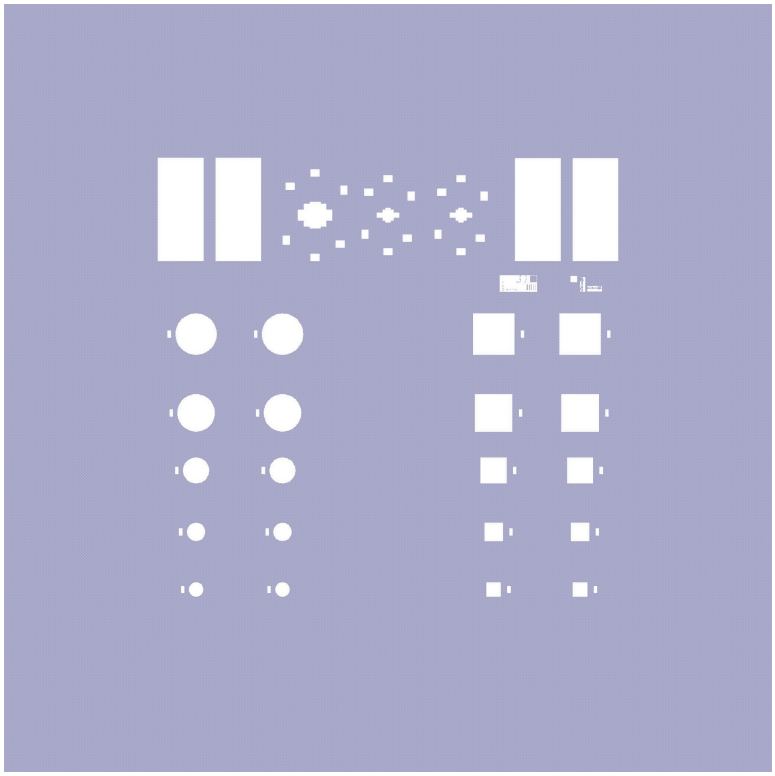

Figure A.10: Capacitor top plate

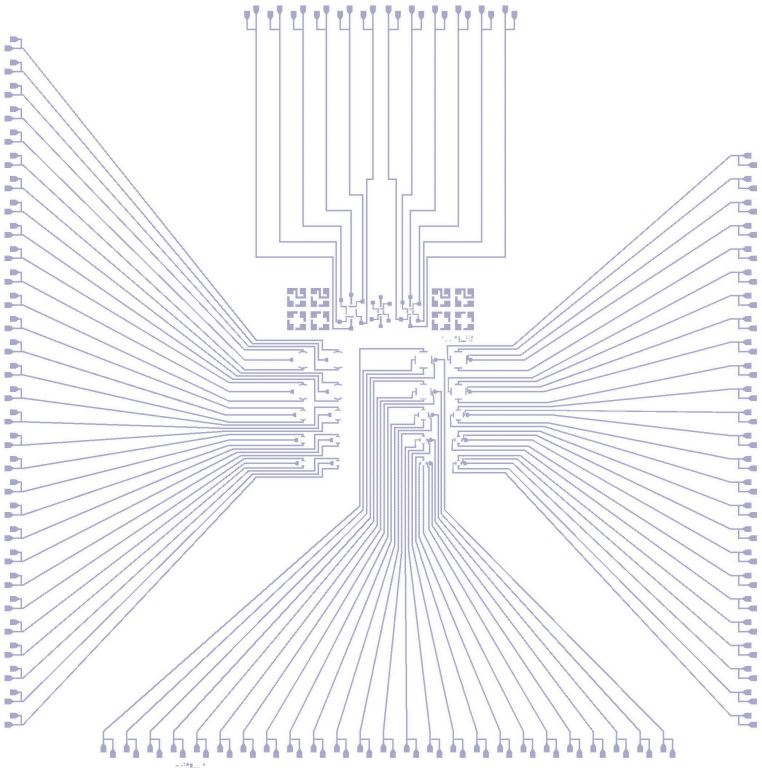

Figure A.11: Interconnect

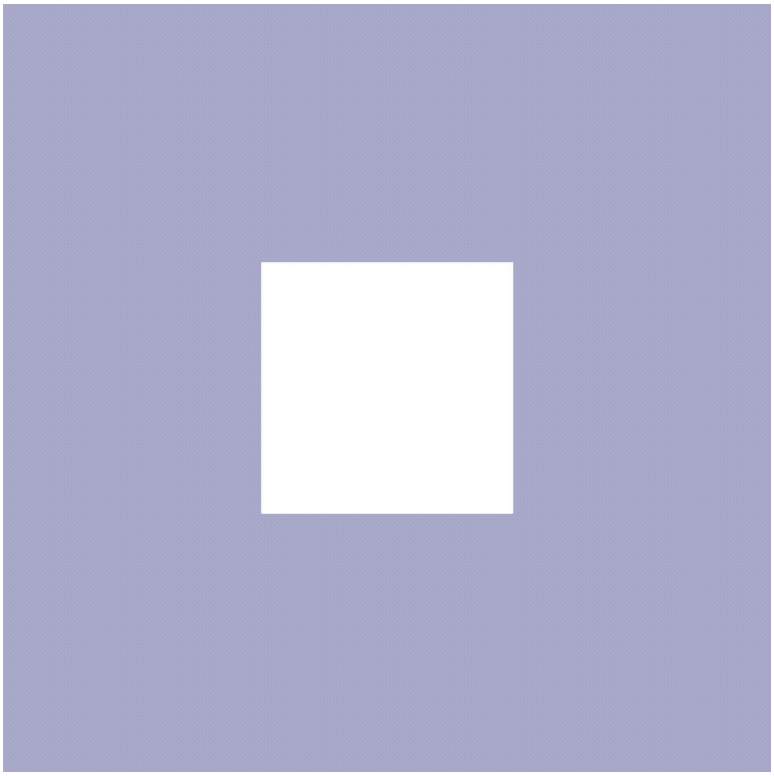

Figure A.12: Top oxide protection layer

B | FLOWCHART

STARTING MATERIAL

Use 10 **SINGLE SIDE** polished **(LRES)** wafers,
with the following specifications:

Brand name:	International Wafer Service (IWS)
Type:	p/B (p-type, boron)
Orientation:	<100>
Resistivity:	1-5 Ωcm
Thickness:	525 μm
Diameter:	100 mm

ZERO LAYER

1. COATING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump
- a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use program "**Co - 3012 - zero layer**". There will be a larger edge bead removal.

2. ALIGNMENT AND EXPOSURE v

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Expose masks **COMURK**, with job "**ZEFWAM**" and the correct exposure energy **120 mJ**
This results in alignment markers for the stepper and contact aligner.

3. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bake at 115 °C for 90 seconds
- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "**Dev - SP**".

4. INSPECTION: Linewidth and overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed

5. PLASMA ETCHING: Alignment markers (URK's) in Silicon

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions and times from the etch recipe!

Use sequence **URK_NPD** (with a platen temperature of **20 °C**) to etch 120 nm deep ASM URK's into the Si.

Process conditions from chamber recipe URK_ETCH:						
Step	Gasses & flows	Pressure	Platen RF	ICP RF	Platen temp.	Etch time
1. breakthrough	CF_4/O_2 = 40/20 sccm	5 mTorr	60 W	500 W	20 °C	0'10"
2. bulk etch	Cl_2/HBr = 80/40 sccm	60 mTorr	20 W	500 W	20 °C	0'40"

6. LAYER STRIPPING: Photoresist

Strip resist — Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. overetching.

ETCH 5UM/10 UM/15UM WELL IN SILICON WAFER
(Use different etching depth to provide options for further coating process.)

7. CLEANING: HNO_3 99% and 69.5%

Clean	**10 minutes** in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "**HNO_3 99% (Si)**" and the carrier with the **white dot**.
Rinse	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Clean	**10 minutes** in concentrated nitric acid at **110 °C**. This will dissolve metal particles. Use wet bench "**HNO_3 69,5% 110C (Si)**" and the carrier with the **white dot**.
Rinse	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Dry	Use the Semitool "rinser/dryer" with the standard program and the white carrier with a **red dot**.

8. LPCVD Nitride Deposition – Hard Mask – 200 nm

Use the LPCVD furnace E2 to deposit silicon nitride. Follow the operation instruction from the manual when using the machine. It is not allowed to change the process conditions and time from the deposition recipe!
Use recipe "**EKL-L-ST**" with a proper deposition time to deposit a **200 nm** thick nitride layer.

Furnace no: **E2** Program name: **EKL-L-ST**
Total time: 20min

Deposition parameters of recipe EKL-L-ST:			
Gasses & flows	Pressure	Temperature	Time
SiH_2Cl_2 / NH_3 = 169.5 / 30.5 sccm	150 mTorr	850 deg C	00:20:00

9. Measurement – Nitride Thickness

Equipment: Woollam Ellipsometer

Thickness: 161nm Measured deposition rate: 8.05nm/min

10. COATING

Use the coater station of the EVG120 system to coat the wafers with **2.1 um** photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of **Shipley SPR3012 positive resist**, dispensed by a pump
- a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use program " **Co - 3012 – 2.1um - noEBR**".

11. EXPOSURE - Well

Alignment and exposure will be done with the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Use the mask **"SICPRESS",** jobname " **SICPRESS** ", layer ID "**SW**", with an energy of **250 mJ cm^{-2} .**
This will result in the pattern of well on the substrate.

12. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- a post-exposure bake at 115 °C for 90 seconds
- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "**Dev - SP**"

13. Dry Etching – Hard mask Nitride

Use the Drytek Triode 384T plasma etcher. Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions from the etch recipe, except for the etch times!
Calculate the etch time based on the measured thickness and etch rate in the menu.

Program: **StdSiN**
Etch rate: 5 nm/s
Time: 161/5 = 32.2s + 2.8s over etch = **35s**

Process conditions from recipe StdSiN:					
Step	Gasses & flows	Pressure	RF power	He pressure	Etch time
1. bulk etch (RIE)	C_2F_6/CHF_3 = 36/144 sccm	180 mTorr	300 W	12 Torr	**35s**

14. LAYER STRIPPING: Photoresist

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. over etching.

15. KOH ETCHING – Well in Silicon substrate

Calculate the etch time based on tested etch rate.

33% KOH (Clean Bench) Etch time: 14min Temp: 85°C
Calculate the time for etching 10 um cavity on Silicon.

Rinse 5 minutes in DI-water.

10% HCl	10 minutes
Rinse	5 minutes in DI-water
Dry	With single wafer dryer – use **Si carrier**

Potassium hydroxide bath preparation:

Magnetic stir-bars are placed in both bath.
When switching on the heater bottom, the corresponding bath start to heat up to 85 degC, with the stir-bar start rotation, cycling the solution continuously.

Procedure of preparation of a fresh bath:

1) Pump away the old KOH solution from the bath.

2) Keep the pump on, and use DI-water to rinse the inter wall and holder dock in the bath to remove any particles from the old solution. Until no visible particle can be found. Pump all water out from the bath as much as possible.

3) Fill the bath (with the dock in) with 4.5 L of DI-water.

4) Switch on the heater, so that the stir-bar start to cycle the solution.

5) Slowly pour KOH pellets into the bath, the total weight of KOH pellet should be 2.25 kg, so to prepare 33% KOH solutions. Check the rotation of the stir-bar. In case the stir-bar is blocked by the pellets, use a Teflon handle to mix the solution, so to accelerate the dissolving of the KOH pellet, until the stir-bar is functional again.

6) Dissolving of the KOH pellets generates heat, the temperature of the bath will increase dramatically. After a full mixing of the solution, the temperature in a fresh KOH bath is close to 85 degC. KOH etching can start immediately.

7) To check the level of the KOH solution, insert the Teflon stick (by the KOH Pt bath) vertically to the bottom of the bath (thicker part to the bottom). The level of the solution should be slightly (0.5 ~ 1 mm) below the carved mark.

16. CLEANING: (HNO3 Si+ Cleaning)

Do this before bring the wafers back to CR100.

Clean	10 minutes in concentrated nitric acid at **110 °C**. This will dissolve metal particles. Use wet bench "**HNO_3 69,5% 110C (Si+)**" and the carrier with the **yellow dot**.
Rinse	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Dry	Use the single wafer dryer.

17. Measurement: Cavity Depth

Cavity Depth:

Wafer number	Designed depth	Etch time	Measured depth	Etch rate
6	5	7 min	5nm	0.71 um/ min
6	10	14 min	10um	0.71um/min
6	15	18 min	12.5 um	0.83um/min
6	20			

INSULATION LAYER DEPOSITION: LPCVD NITRIDE 500NM

18. LPCVD Si_3N_4 DEPOSITION 500nm: Bottom Insulation layer

Use the LPCVD furnace E2 to deposit silicon nitride. Follow the operation instruction from the manual when using the machine. It is not allowed to change the process conditions and time from the deposition recipe!
Use recipe "**EKL-L-ST**" with a proper deposition time to deposit a **500 nm** thick nitride layer.
Time calculated based on previous measured deposition rate 8.05nm/min.

Furnace no: **E2** Program name: **EKL-L-ST**
Total time: 62min

Deposition parameters of recipe EKL-L-ST:			
Gasses & flows	Pressure	Temperature	Time
SiH_2Cl_2 / NH_3 = 169.5 / 30.5 sccm	150 mTorr	850 deg C	01:02:00

19. MEASUREMENT: Nitride thickness

Use the **Woollam Ellipsometer** to measure the nitride thickness:

Program: *DIMES General/LPCVD Lostress SiN [0-1500nm]/DIMES lpcvd losin (0-1.5um)*"

Nitride thickness: 510 nm

BOTTOM SIC CAPACITOR PLATE – 500 NM *(Thickness can be changed if needed)*

20. LPCVD SiC DEPOSITION 500 nm – FURNACE F3

Program name: **SIC_DOPE**
Total time: 60 min /75min

Use furnace **F3** in Class 10000 to deposit the SiC layer. Use progaram "**SIC_DOPE** ". Calculate deposition time according to the logbook to obtain a desired thickness.

Deposition parameters of recipe SIC_DOPE:			
Gasses & flows	Pressure	Temperature	Time
SiH_2Cl_2 / C_2H_2 / NH_3= 80/320/30	80 Pa	860 deg C	**60min**
SiH_2Cl_2 / C_2H_2 / NH_3= 80/320/60	80 Pa	860 deg C	**75min**

21. MEASUREMENT: Sheet resistance

Location: (Class 100)
Equipment: Four probe station

R_measured:

Deposited layer	STD:	Max:	Min:	Std dev
SiH_2Cl_2 / C_2H_2 / NH_3= 80/320/30	1165	899	1466	15%
SiH_2Cl_2 / C_2H_2 / NH_3= 80/320/60	120	91	164	18%

22. COATING

Use the coater station of the **EVG120 system** to coat the wafers with **3.5 um** photoresist. The process consists of:

- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of **AZ Nlof2020 negative resist**, dispensed by a pump
- a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use program " **Co - Topo - Nlof - 3,5µm - no EBR**". (Use topo program)

23. EXPOSURE – SiC bottom plate

Alignment and exposure will be done with the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Use the mask **"SICPRESS"**, jobname " **SH_SICPRESS** ", layer "**BOTSIC**" , with an energy of **450 mJ cm^{-2}**
This will result in the pattern of the bottom SiC layer (Bottom capacitor plate).

24. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- a post-exposure bake at 115 °C for 90 seconds
- developing with **AZ Nlof2020** with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program " **Dev - SP** "

(OR)Spray coating: Because of the depth of the well.

Positive Photoresist 7um~9um:

Coating
Spray coating: Program HP-1000mbar-2ml-8layers
Bake: 115℃ 2min
Spray coating: Program HP-1000mbar-2ml-8layers
Bake: 115℃ 5min
Spray coating: Program HP-1000mbar-2ml-8layers
Wait 15min

Exposure twice: Over exposure required
Use the mask **"SICPRESS"**, jobname " **SH_SICPRESS** ", layer "**BOTSIC**" , with an energy of **600 mJ cm^{-2}**
This will result in the pattern of the bottom SiC layer (Bottom capacitor plate).

Developing:
AZ400 Diluted – H_2O : Dev = 2:1

Negtive Photoresist 7um~9um:

Coating
Spray coating: Program "HP-1000mbar-2ml-8layers"
Bake: 115℃ 2min
Spray coating: Program "HP-1000mbar-2ml-8layers"
Bake: 115℃ 5min
Spray coating: Program "HP-1000mbar-2ml-8layers"
Wait 15min

Exposure twice: Over exposure required
Use the mask **"SICPRESS"**, jobname " **SH_SICPRESS** ", layer "**BOTSIC**" , with an energy of **330 mJ cm^{-2}**
This will result in the pattern of the bottom SiC layer (Bottom capacitor plate).

Soft bake: Use the developer station of the EVG120 system
Program: "xlink-bake-spraycoated"

Developing:
MF322 Developer

25. INSPECTION: Linewidth and overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

26. PLASMA ETCHING – Bottom SiC layer

Use recipe "**SiC-3mu**" on Omega. Adjust the etch time depending on earlier poly-SiC etch experience in order to etch the SiC layer landing exactly on the Nitride layer, leaving only the desired structure.

Program: **SiC-3mu**
Time: 3min15s
Measured etch rate: 185nm/s

27. LAYER STRIPPING: Photoresist

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. over etching.

Note: After this step, the thickness of the deposited SiC and the reamaining nitride can be measured with Dektak 8. The actual thickness of the SiC thickness can be obtained by subtracting thickness of the removed nitride from the total thickness.

28. MEASUREMENT – Thickness SiC & Si_3N_4

Use the **Woollam Ellipsome** to measure oxide thickness of the test wafer. After SiC etch, etch all the oxide layer by wet etching.

Program: *DIMES General/SiO2 on Si (Th.ox, LPCVD-TEOS)/DIMES Oxide 1.5um*
Oxide thickness: 541nm

Use the previous SiC thickness and the nitride thickness acquired in the previous step to determine the thickness of the carbide layer.

Measurement	1 (60min)	2(75min)	3	4	5	6
SiO_2	541nm	541nm				
Step height	985nm	1081nm				
SiC	444nm	540nm				

INSULATION LAYER BETWEEN PLATES – 300NM NITRIDE
(Thickness influence capacitance. Thickness should be enough to survive etching of the 2 um SiC diaphragm)

29. LPCVD Si_3N_4 DEPOSITION 200nm: Insulation layer 2

Furnace no: E2 Program name: 4INCHST
Total time: 24min25s

Use the LPCVD furnace E2 to deposit silicon nitride. Follow the operation instruction from the manual when using the machine. It is not allowed to change the process conditions and time from the deposition recipe!
Use recipe "**4INCHST**" with a proper deposition time to deposit a **300 nm** thick nitride layer.

Deposition parameters of recipe 4INCHST:			
Gasses & flows	Pressure	Temperature	Time
SiH_2Cl_2 / NH_3 = 169.5 / 30.5 sccm	150 mTorr	850 deg C	24min25s

30. MEASUREMENT: Nitride thickness

Use the **Woollam Ellipsometer** to measure the nitride thickness:

Program: *DIMES General/LPCVD Lostress SiN [0-1500nm]/DIMES lpcvd losin (0-1.5um)*"

Nitride thickness: 199.8 nm

SACRIFICIAL LAYER – 2UM OXIDE

(Thickness can be changed to test different cavity size)

31. PECVD TEOS Oxide DEPOSITION: 2 um Sacrificial layer

Use the Novellus Concept One PECVD reactor. Follow the operation instruction from the manual when using the machine. It is not allowed to change the process conditions and time from the deposition recipe!

Use recipe ".**xxxnmteos**" (".**xxxsiostd"**) to deposit a 2000nm thick SiO2 layer on different wafers. Calculate the deposition time.

Program: **xxxnmteos** or **xxxsiostd** Time: 29s

Process conditions from recipe .xxxsiostd:					
Gasses & flows	Pressure	HF power	LF power	Temperature	Time
$N_2/SiH_4/N_2O$ =3150/210/6000 sccm	2.2 Torr	1 kW	0 W	350 °C	29s

Thickness of this layer is critical. Test on the deposition rate can be measured first with test wafer.
(The thickness can be thicker to ensure non-touch mode)

32. MEASUREMENT: TEOS THICKNESS

Use the **Woollam Ellipsome** to measure oxide thickness of the test wafer. After SiC etch, etch all the oxide layer by wet etching.

Program: *DIMES General/SiO2 on Si (Th.ox, LPCVD-TEOS)/DIMES Oxide 1.5um*
Oxide thickness: 2056nm

33. COATING

Use the coater station of the EVG120 system to coat the wafers with **2 um** photoresist. The process consists of:

- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of **AZ Nlof2020 negative resist**, dispensed by a pump
- a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Use program " **Co - Topo - Nlof - 2,0µm -noEBR** "

34. EXPOSURE – Sacrificial layer 1

Use the mask **"SICPRESS"**, jobname " **SH_SICPRESS** ", layer "**SAC1**" , with an energy of **320 mJ cm^{-2}**
This will result in the pattern of the first sacrificial layer (Capacitor gap & reference cavity).

35. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bake at 115 °C for 90 seconds
- developing with **AZ Nlof2020** with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program " **Dev - SP** "

36. WET ETCHING – Sacrificial SiO2 Structure 1

Etchant:	Use **wetbench "BHF (1:7)";** use the carrier with the blue dot
Etch time:	9min14s + 2min over etch; Etch till **2um** PECVD oxide is completely removed and land on the insulation nitride layer at unwanted area. Calculate the etch time.
QDR:	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying:	Use the µProcess Avenger with the standard program, and the white carrier with a red dot.

(This will result in the complete structure of sacrificial layer with top release holes, and the basic structure of the side release holes.)

37. INSPECTION

Visually inspect the wafers through a microscope, and check if the TEOS is fully removed at unwanted area. Check the structures.

38. LAYER STRIPPING: Photoresist

Strip resist	Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier. Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. over etching.

39. COATING

Use the coater station of the EVG120 system to coat the wafers with **2 um** photoresist. The process consists of:

- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of **AZ Nlof2020 negative resist**, dispensed by a pump
- a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Use program " **Co - Topo - Nlof - 2,0µm -noEBR**"

40. EXPOSURE – Sacrificial layer 2

Use the mask **"SICPRESS"**, jobname " **SH_SICPRESS** ", layer "**SAC2**" , with an energy of **320 mJ cm^{-2}**
This will result in the pattern of the complete sacrificial layer (Capacitor gap & reference cavity).

41. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bake at 115 °C for 90 seconds
- developing with **AZ Nlof2020** with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program " **Dev - SP** "

42. Dry Etching PECVD SiO_2 – Sacrificial SiO2 Structure 2 (Or use wet etching)

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions from the etch recipe, except for the etch times!

Use recipe **for TEOS** to etch the oxide layer with a soft landing on the layer underneath

Process conditions from recipe STDOXIDE:					
Step	Gasses & flows	Pressure	RF power	He pressures	Etch time
1. bulk etch (RIE)	C_2F_6/CHF_3 = 36/144 sccm	180 mTorr	300 W	12 Torr	

43. INSPECTION

Visually inspect the wafers through a microscope, and check the structure. Check how the step for side release holes shaped and the remaining structure for the top release hole. Measure critical dimensions.

44. LAYER STRIPPING: Photoresist

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. over etching.

45. MEASUREMENT: Sacrificial THICKNESS

Measure the thickness of the sacrificial layer steps.

1ST SiC DIAPHRAGM LAYER – 800NM SiC & ETCHING OF RELEASE HOLE

(The exposure and etching step can be done several times to make sure the opening of release holes)

46. LPCVD SiC DEPOSITION 800 nm – FURNACE E4 OR F3

Program name: **SIC_DOPE**
Total time: 110min

Use furnace **F3** in Class 10000 to deposit the SiC layer. Use progaram "**SIC_DOPE** ". Calculate deposition time according to the logbook to obtain a desired thickness.

Deposition parameters of recipe SIC_DOPE:			
Gasses & flows	Pressure	Temperature	Time
SiH_2Cl_2 / C_2H_2 / NH_3= 80/320/30	80 Pa	860 deg C	**110min**

47. MEASUREMENT: Sheet resistance & Thickness

Location: (Class 100)
Equipment: Four probe station

R_measured:

Deposited layer	STD:	Max:	Min:	Std dev
SiH_2Cl_2 / C_2H_2 / NH_3= 80/320/30	531.5			

Thickness: 740nm

48. COATING

Use the coater station of the **EVG120 system** to coat the wafers with **4 um** photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of **AZ ECI3027 positive resist**, dispensed by a pump
- a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use program " **Co - Topo - 3027 - 4,0µm - no EBR**".

! Or use the spray coater / Manual coater: Because of the depth of the well / Resist thicknesss.
(Accuracy is critical because pattern of release holes (1 um x 2 um) will be exposed.)

49. EXPOSURE – Release holes on diaphragm layer 1

Use the mask **"SICPRESS"**, jobname " **SH_SICPRESS** ", layer "**RH**" , with an energy of **360 mJ cm^{-2}**
!Adjust exposure focus f=10.2-2=8.2

This will result in the pattern of the release holes.

50. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bake at 115 °C for 90 seconds
- developing with **AZ ECI3027** with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program " **Dev - SP** "

51. INSPECTION: Linewidth and overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

52. PLASMA ETCHING – Release holes

Use recipe "**SiC-3mu**" on Omega. Adjust the etch time depending on earlier poly-SiC etch experience in order to etch the SiC layer landing exactly on the Nitride layer, leaving only the desired structure.

Program: **SiC-3mu**
Time: 4min50s
Measured etch rate: 189nm/s

53. INSPECTION: Release hole

Visually inspect the wafers through a microscope, and check the line width and overlay (Formation of release holes). All release holes should be opened. Measure the size. No resist residues are allowed.

54. LAYER STRIPPING: Photoresist

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. over etching.

SACRIFICIAL RELEASE

55. Vapor HF: Sacrificial releasing

Use the **recipe 3** in the **vapor HF tool** to remove the sacrificial layer. Additional time for over etch is needed to ensure there is no SiO2 residue left inside the cavity.
Cycle: 20
Time:600s

56. INSPECTION

Visually inspect the wafers through a microscope, and check the formation of capacitor cavity. No remaining oxide allowed.

2ND SIC DIAPHRAGM LAYER – 1.2NM SIC & ETCHING OF TOTAL 2UM SIC DIAPHRAGM

(Thickness can be changed for different sensitivity)

57. LPCVD SiC DEPOSITION 1200 nm – FURNACE F3

Program name: **SIC_DOPE**
Total time: 260min

Use furnace **F3** in Class 10000 to deposit the SiC layer. Use progaram "**SIC_DOPE** ". Calculate deposition time according to the logbook to obtain a desired thickness.

Deposition parameters of recipe SIC_DOPE:			
Gasses & flows	Pressure	Temperature	Time
SiH_2Cl_2 / C_2H_2 / NH_3= 80/320/30	80 Pa	860 deg C	**260min**

The deposited SiC should seal the release holes.

58. MEASUREMENT: Sheet resistance

This will measure the total sheet resistance of the top SiC layer.
Location: (Class 100)
Equipment:

Sheet Resistance (Measured): 427
Thickness: 1835nm

59. INSPECTION - Release hole

Visually inspect if the release holes are completely sealed.

60. HDMS TREATMENT

Use the EVG120 system to carry out a HMDS treatment before coating. Use recipe "**1 - only - HMDS - on coater**".

61. Spray coating:

Spray coating: Program "HP-1000mbar-2ml-8layers"
Bake: 115℃ 2min
Spray coating: Program "HP-1000mbar-2ml-8layers"
Bake: 115℃ 5min
Spray coating: Program "HP-1000mbar-2ml-8layers"
Wait 15min before exposture

62. EXPOSURE - Diaphragm

Exposure twice: Over exposure required

Use the mask **"SICPRESS"**, jobname "**SH_SICPRESS**", layer "**DIASIC**", with an energy of **600 mJ cm^{-2}**

This will result in the pattern of the diaphragm.

63. DEVELOPING

Soft bake: Use the developer station of the EVG120 system
Program: "xlink-bake-spraycoated"

Maunal Developing:
MF322 Developer 4min30s

64. INSPECTION: Linewidth and overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

65. PLASMA ETCHING – Diaphragm

Use recipe "**SiC-3mu**" on Omega. Adjust the etch time depending on earlier poly-SiC etch experience in order to etch the SiC layer landing exactly on the Nitride layer, leaving only the desired structure.

Program: **SiC-3mu**
Time: 14min 15s
Measured etch rate: min 183nm/s

66. LAYER STRIPPING: Photoresist

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. over etching.

TOP INSULATION & CO

67. LPCVE TEOS DEPOSITION – Top Insulation

Use furance E1
Change time to get the right thickness **300 nm**. Use existing data in the folder.

Deposition time: 43min

(Optional) LPCVD Si_3N_4 DEPOSITION 300nm: Top Insulation

Furnace no: E2 Program name: 4INCHST
Total time: _____hours

Use the LPCVD furnace E2 to deposit silicon nitride. Follow the operation instruction from the manual when using the machine. It is not allowed to change the process conditions and time from the deposition recipe!
Use recipe "**4INCHST**" with a proper deposition time to deposit a **300 nm** thick nitride layer.

Deposition parameters of recipe 4INCHST:			
Gasses & flows	Pressure	Temperature	Time
SiH_2Cl_2 / NH_3 = 169.5 / 30.5 sccm	150 mTorr	850 deg C	

68. COATING

Use the coater station of the EVG120 system to coat the wafers with **1.4 um** positive photoresist. The process consists of:

- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of **Shipley SPR3012 positive resist**, dispensed by a pump
- a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Use program "**Co -Topo- 3012 – 1.4µm-noEBR**".

69. EXPOSURE – Top CO

Use the mask **"SICPRESS",** jobname "**SH_SICPRESS**", layer "**TOPCO**" , with an energy of **120 mJ cm^{-2}**
This will result in the pattern of the top contact opening.

70. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- a post-exposure bake at 115 °C for 90 seconds
- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "**Dev - SP**"

71. WET ETCHING – Top CO

Etchant:	Use wetbench "BHF (1:7)"; use the carrier with the blue dot
Etch time:	Etch till 300nm TEOS oxide is completely removed and land on the insulation nitride the contact opening and diaphragm. Calculate the etch time.
QDR:	Rinse in the Quick Dump Rinser with the standard programe until the resistivity is 5 MΩ.
Drying:	Use the µProcess Avenger with the standard program, and the white carrier with a red dot.

(Optional) Dry Etching – 2nd LPCVD Nitride – Bottom CO

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions from the etch recipe, except for the etch times!

Use recipe **StdSiN** to etch the nitride layer.

72. INSPECTION

Visually inspect the wafers through a microscope, and check if the TEOS/Nitride is fully removed at unwatned area. Check the structures.

73. LAYER STRIPPING: Photoresist

Strip resist	Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier. Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. over etching.

74. COATING

Use the coater station of the EVG120 system to coat the wafers with 1.4 um positive photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of **Shipley SPR3012 positive resist**, dispensed by a pump
- a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use program " **Co – Topo - 3012 – 2.1um - noEBR**".

75. EXPOSURE – Bottom CO

Alignment and exposure will be done with the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Use the mask **"SICPRESS"**, jobname " **SH_SICPRESS** ", layer "**BOTCO**", with an energy of **350 mJ cm^{-2} .** This will result in the pattern of bottom contact opening.

76. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bake at 115 °C for 90 seconds
- developing with **Shipley SPR3012** with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "**Dev - SP**"

77. INSPECTION: Linewidth and overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

78. Dry Etching – 2nd LPCVD Nitride – Bottom CO

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is **not** allowed to change the process conditions from the etch recipe, except for the etch times!

Use recipe **StdSiN** to etch the nitride layer.

Process conditions from recipe StdSiN:					
Step	Gasses & flows	Pressure	RF power	He pressure	Etch time
1. bulk etch (RIE)	C_2F_6/CHF_3 = 36/144 sccm	180 mTorr	300 W	12 Torr	**45s**

79. LAYER STRIPPING: Photoresist

Strip resist — Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. over etching.

METAL IC – 675NM AL / 500NM TI

80. SPUTTERING: Metallization

Use recipe "AlSi-675nm-350C" to deposit a 675nm thick 99% Al with 1% Si .

81. COATING

Use the coater station of the EVG120 system to coat the wafers with **1.4 um** positive photoresist. The process consists of:

- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of **Shipley SPR3012 positive resist**, dispensed by a pump
- a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Use program " **Co -Topo- 3012 – 1.4 um - noEBR** ".

82. EXPOSURE – IC

Use the mask **"SICPRESS"**, jobname "**SH_SICPRESS**", layer "**IC**" , with an energy of **150 mJ cm^{-2}**
This will result in the pattern of IC.

83. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- a post-exposure bake at 115 °C for 90 seconds
- developing with **Shipley SPR3012** with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "**Dev - SP**"

84. INSPECTION

Visually inspect the wafers through a microscope and check the line width and overlay. No resist residues are allowed.

85. WET ETCHING – IC

Etchant:	Use wet bench "Al etch (35 ◦C)" and the carrier with the yellow dot. The bath contains PES at temperature 35 ◦C. A typical etch rate of Al is 170 nm/min;
Etch time:	4 minutes 30 seconds; Etch till only desiried IC Al remains.
QDR:	Rinse in the Quick Dump Rinser with the standard programe until the resistivity is 5 MΩ.
Etch:	Etch Use wet bench "Poly-Si etch" and the carrier with the green dot to remove the 1 % silicon.
Etch time:	30 seconds;
QDR:	Rinse in the Quick Dump Rinser with the standard programe until the resistivity is 5 MΩ.
Drying:	Use "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a black dots.

As for the Ti metallization, use the Trikon Omega 201 plasma etcher with a sequence "Ti-500nm".

86. LAYER STRIPPING: Photoresist

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper and use the quartz carrier.

Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. over etching.

87. CLEANING: 100% HNO3 (metal)

Cleaning:	10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 100% and the carrier with the red dot.
Rinse:	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Dry Use "Avenger Ultra-Pure 6" rinser/dryer with the standard program. Always use the special orange carrier.

88. Annealing

Use C4 furnace and program "**ALLOY1**" for this step.

TOP PROTECTION LAYER (OPTIONAL)

(Thickness can be varied to compensate surface roughness of compound. Should be completely etched in unwanted area.)

89. PECVD TEOS DEPOSITION – Top protection

Use the Novellus Concept One PECVD reactor.

Change time to get the right thickness **10 um**. Use existing data in the folder.

Process conditions from recipe xxxsiostd:					
Gasses & flows	Pressure	HF power	LF power	Temperature	Time
$N_2/SiH_4/N_2O$ =3150/210/6000 sccm	2.2 Torr	1 kW	0 W	350 °C	10.5 $^{sec}/_{station}$

90. COATING

Use the coater station of the EVG120 system to coat the wafers with **1.4 um** positive photoresist. The process consists of:

- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
- spin coating of **Shipley SPR3012 positive resist**, dispensed by a pump
- a soft bake at 95 °C for 90 seconds
- an automatic edge bead removal with a solvent

Use program "**Co – Topo - 3012 – 1.4 µm -NoEBR**".

91. EXPOSURE – Top Protect

Use the mask **"SICPRESS"**, jobname "**SH_SICPRESS**", layer "**PROT**" , with an energy of **115 mJ cm^{-2}**
This will result in the pattern top protection layer.

92. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- a post-exposure bake at 115 °C for 90 seconds
- developing with Shipley MF322 with a single puddle process
- a hard bake at 100 °C for 90 seconds

Always follow the instructions for this equipment.

Use program "**Dev - SP**"

93. WET ETCHING – Top Protect

Use the wet bench with green metal allowed

(This will result in the top protection SiO2 structure.)

94. INSPECTION

Visually inspect the wafers through a microscope, and check if the TEOS is fully removed at unwatned area. Check the structures.

95. LAYER STRIPPING: Photoresist

Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper and use the quartz carrier.
Use **program 1**: 1000 watts power and automatic endpoint detection + 2 min. over etching.

96. Dicing: MEMS lab