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10.3 A 0.12mm² Wien-Bridge Temperature Sensor with 0.1°C (3σ) Inaccuracy from -40°C to 180°C

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Resistor-based temperature sensors can achieve much higher resolution and energy efficiency than conventional BJT-based sensors [1], but they typically occupy more area (>0.25mm²) and have lower operating temperatures (≤125°C) [2-4]. This work describes a 0.12mm² resistor-based sensor that uses a Wien-bridge (WB) filter to achieve 0.1°C (3σ) inaccuracy from -40°C to 180°C. Compared to a state-of-the-art WB sensor [4], it occupies 6× less area and achieves comparable relative accuracy over a 76% wider operating range.

As shown in Fig. 10.3.1, the heart of the sensor is a Wien Bridge (WB) bandpass filter made from polysilicon resistors (R_{WB} = 64kΩ) and MIM capacitors (C_{WB} = 5pF). Unlike Wheatstone-bridge sensors [2,3], WB sensors only require one type of resistor, resulting in higher accuracy, and facilitating the experimental characterization of undocumented resistor properties such as 1/*f* noise and stress sensitivity. The filter is driven by a fixed-frequency square wave (f_{drive} = 500kHz) so that its temperature-dependent phase-shift ϕ_{WB} can be digitized by a phase-domain delta-sigma modulator (PDΔΣM) [3]. In the PDΔΣM, phase detection is performed by a chopper in the feedback loop of the 1st integrator (Fig. 10.3.2). Depending on the state of the bitstream BS, the chopper is driven by one of two reference phases $\phi_{0,1}$ (90°±30° w.r.t. to the phase of f_{drive}) such that the DC component of the integrated current is either positive or negative. The integration capacitor C_{int} must then be dimensioned to filter out the resulting ripple and ensure that the output of the 1st integrator does not clip. In [4], this required a 180pF capacitor that occupied more than half of the sensor's area.

To reduce the size of C_{int}, R_{WB} can be increased, but this will be at the expense of worse resolution. A better approach is to increase the output swing of the 1st integrator. In this work, the 1st integrator is built around a two-stage Miller-compensated opamp based on current-reuse amplifiers (Fig. 10.3.2). The 1st stage provides good energy efficiency, while the 2nd uses high-V_T devices to efficiently provide a near rail-to-rail output swing. Compared to the conventional choice of two common-source stages, the second stage provides twice the output current for the same bias current. Together with the doubling of R_{WB}, this allows the value of C_{int} to be reduced from the 180pF used in [4], to 23pF. At room temperature (RT), the amplifier draws 14μA and has a gain bandwidth product of 17MHz. To further reduce area, the 2nd integrator and the feed-forward coefficient are realized in a switched-capacitor manner, thus avoiding the large resistors used in [4]. The associated folded-cascode amplifier draws only 2.5μA at RT. On-chip logic generates the drive signal f_{ref} and the phase references $\phi_{0,1}$ from an external 6MHz frequency reference.

However, reducing C_{int} will increase the opamp's closed-loop input impedance Z_{in} ($\propto 1/(C_{int}\cdot GBW)$). This is in series with the WB and is thus a source of spread and 1/*f* noise. To minimize spread, a constant-Gm biasing circuit based on a resistor of the same type as R_{WB} ensures that Z_{in} tracks R_{WB} over a wide temperature range. Although the opamp is effectively chopped, the 1/*f* noise present in its bias current will modulate Z_{in}, and thus R_{WB}, causing residual 1/*f* noise. To minimize this, the core of the biasing circuit was realized with large PMOS devices (W/L = 40μm/5.5μm), and critical current mirrors were realized with the standard NPN transistors available in the chosen process (Fig. 10.3.2). Simulations show that the 1/*f* corner of the sensor is then about 1Hz and that R_{WB} is less than 1% of Z_{in} over corners.

Three pairs of identical sensors based on silicided p-poly (SP), unsilicided n-poly (NP) and high-resistive poly (HRP) resistors were fabricated on the same die in a 0.18μm CMOS process (Fig. 10.3.7). This facilitates the use of differential measurements to distinguish sensor drift from the inevitable ambient temperature drift. Each sensor consumes 29μA from a single 1.8V supply and occupies 0.12mm², of which the WB occupies 25%. PSDs of the bitstream outputs of the three sensors are shown in Fig. 10.3.3 (top) based on differential data captured during a 100s measurement interval. Figure 10.3.3 (bottom) shows the calculated resolution of each sensor versus conversion time. Due to its greater temperature coefficient (TC), the SP sensor exhibits the best resolution: 460μK in a 10ms conversion time, corresponding to a 110fJ·K² resolution FoM. For longer conversion times, sensor resolution is limited by 1/*f* noise. The corner frequencies are ~4Hz (NP and HRP), and ~1Hz (SP). However, the SP corner frequency is limited by the readout electronics.

10 chips (60 sensors) from a single batch were packaged in ceramic DIL and characterized from -40°C to 180°C. To correct for the inherent cosine nonlinearity of the PDΔΣM and the non-linear relationship between ϕ_{WB} and R_{WB} (Fig. 10.3.1, bottom), a 7th-order polynomial is used to translate the decimated output of each sensor into an equivalent sensor resistance R_{WB}. Since the temperature dependency of polysilicon resistors is comparatively linear, this approach minimizes the residual error after a 1st-order fit [4]. Figure 10.3.4 (top) shows the resulting temperature dependence of each resistor type. The following RT TCs were extracted: 0.31%/°C (SP), -0.15%/°C (NP) and -0.10%/°C (HRP), which agree with the process documentation. After a 1st-order fit to compensate for process spread, followed by the use of a fixed 6th-order polynomial to correct for the systematic non-linearity of the sensors, their residual spread is shown in Fig. 10.3.4 (bottom). The sensors achieve 3σ inaccuracies of 0.1°C (SP), 0.4°C (NP) and 0.9°C (HRP) from -40°C to 180°C. After a correlated 1-point trim [3], the SP sensor achieves an inaccuracy of 0.4°C (3σ), which is comparable with that of BJT-based sensors [5].

To observe the effects of mechanical stress, 10 chips from the same batch were characterized in injection-molded plastic QFN packages. Figure 10.3.5 (top) shows the average dependency of R_{WB} for both the ceramic and plastic packaged chips. After using the same non-linearity correction polynomials determined for the ceramic packaged chips, the inaccuracy after a 1st-order fit increases by only 0.2°C for the SP sensors, but to 1.4°C for the NP sensors, and even 2.5°C for the HRP sensors (Fig. 10.3.5 (bottom)). The sharp inflexion in all the inaccuracy plots around 100°C is probably due to the effects of moisture on the plastic packages [7]. Of the three resistor types, the SP resistor is clearly the least stress sensitive, exhibiting a packaging shift similar to that of BJT-based sensors [6].

In Fig. 10.3.6 the performance of the SP sensor is summarized and compared to the state-of-the-art. Compared to a state-of-the-art WB sensor [4], this design has a 76% larger operating range and occupies 6× less area. The latter is achieved at the expense of somewhat less relative inaccuracy [1]. Compared to a state-of-the-art WhB sensor [3], it achieves better accuracy and occupies 2× less area, but is less energy efficient. Measurements in plastic packages show that the SP sensors are quite insensitive to packaging stress (< 0.2°C packaging shift) and obtain good accuracy after a 1-point trim. They can thus replace BJT-based sensors in applications where both a wide temperature range and a high resolution are required.

Acknowledgments:
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References:

[1] K. A. A. Makinwa, "Smart Temperature Sensor Survey", [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls

[2] C. H. Weng et al., "A CMOS Thermistor-Embedded Continuous-Time Delta-Sigma Temperature Sensor With a Resolution FoM of 0.65 pJ°C²," *IEEE JSSC*, vol. 50, no. 11, pp. 2491-2500, Nov. 2015.

[3] S. Pan and K. A. A. Makinwa, "A 0.25 mm²-Resistor-Based Temperature Sensor With an Inaccuracy of 0.12 °C (3σ) From -55 °C to 125 °C," *IEEE JSSC*, Oct. 2018.

[4] S. Pan et al., "A Resistor-Based Temperature Sensor with a 0.13pJ·K² Resolution FOM," *IEEE JSSC*, vol. 53, no. 1, pp. 163-174, Jan. 2018.

[5] K. Souri et al., "A 40μW CMOS Temperature Sensor with an Inaccuracy of ±0.4° C (3σ) from– 55° C to 200°C," *ESSCIRC*, pp. 221-224, Sept. 2013.

[6] B. Yousefzadeh et al., "A BJT-Based Temperature Sensor with a Packaging-Robust Inaccuracy of ±0.3°C (3σ) from -55°C to +125°C After Heater-Assisted Voltage Calibration," *ISSCC*, pp. 162-163, Feb. 2017.

[7] U. Ausserlechner et al., "Drift of Magnetic sensitivity of smart Hall sensors due to moisture absorbed by the IC-package," *IEEE Sensors*, pp. 455-458, Oct. 2004.

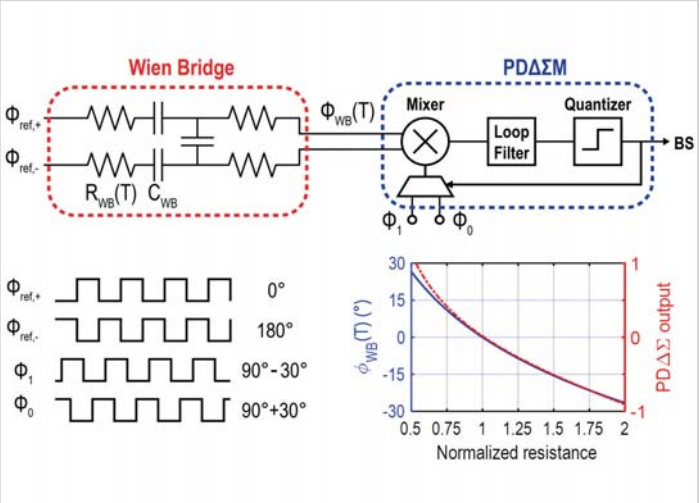

Figure 10.3.1: CTΔΣ readout of a Wien-bridge temperature sensor (top), waveforms, phase response of the Wien bridge and BS average of the PDΔΣM (bottom).

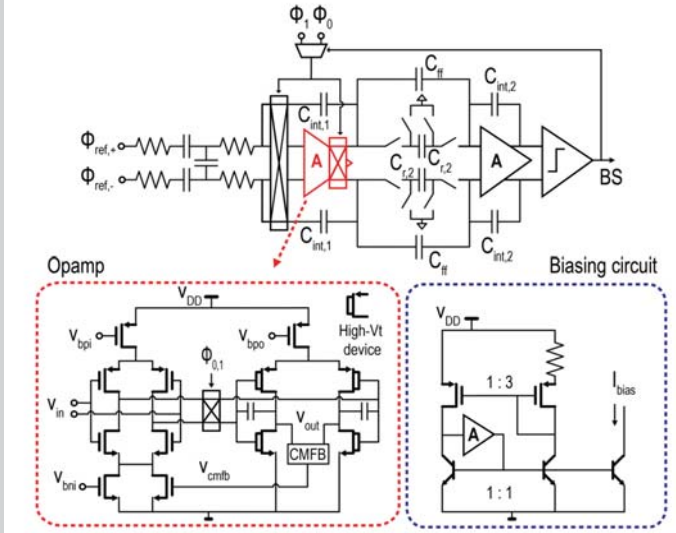

Figure 10.3.2: Block diagram of the PDΔΣM. Simplified diagram of the 1st-stage amplifier and the biasing circuit.

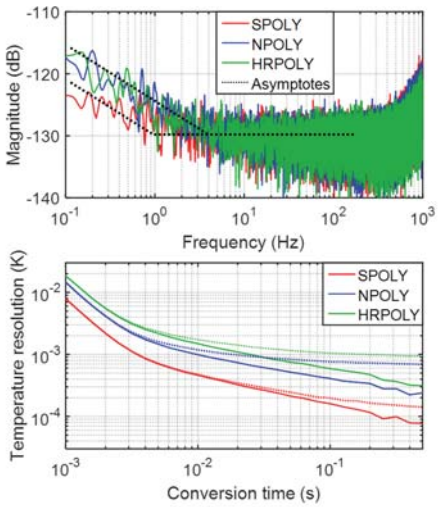

Figure 10.3.3: Bitstream spectra (100s interval, Hanning window) (top); Resolution vs. conversion time for 1s (solid lines) and 100s (dashed lines) intervals (bottom).

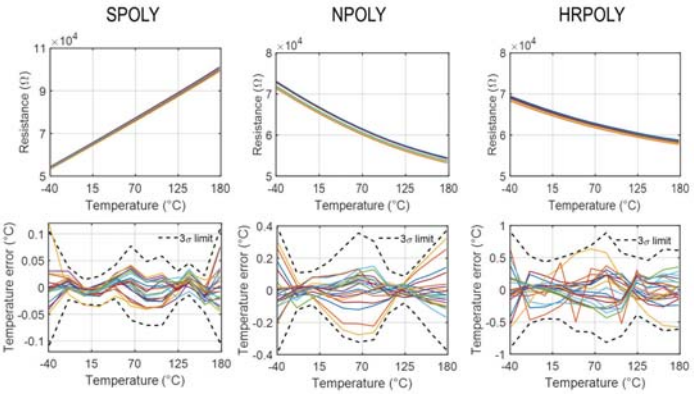

Figure 10.3.4: Extracted sensor resistance R_{WB} with ceramic packaging (top); Inaccuracy after a 1st-order fit and systematic non-linearity correction (bottom).

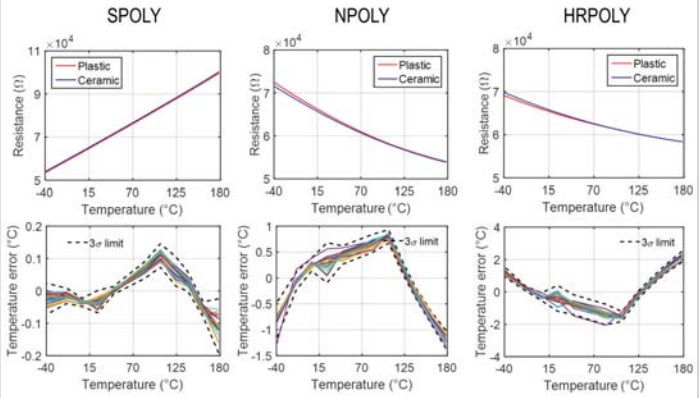

Figure 10.3.5: Average resistance vs. temperature of three types of resistors in different packages (top); Inaccuracy of plastic packaged sensors after a 1st-order fit and system non-linearity correction from ceramic packaged sensors (bottom).

	[2]	[3]	[4]	[5]	This Work	
Sensor type	Resistor WhB	Resistor WhB	Resistor WB	BJT	Resistor WB	
Technology	0.18µm	0.18µm	0.18µm	0.16µm	0.18µm	
Area [mm²]	0.43	0.25	0.72	0.1	0.12	
Temperature range	-40°C to 125°C	-55°C to 125°C	-40°C to 85°C	-55°C to 200°C	-40°C to 180°C	
Trimming points	2 [a]	2 [b]	2 [b]	1	1	2 [b]
3σ inaccuracy [°C]	0.4	0.12	0.03	0.4	0.4	0.11
Relative inaccuracy	0.48%	0.13%	0.05%	0.33%	0.36%	0.10%
Supply voltage [V]	1.5	1.8	1.8	1.6	1.8	
Power [µW]	65	94	160	35	52	
Conversion time [ms]	0.1	5	5	4.2	10	
Resolution [mK]	10	0.29	0.41	20	0.46	
Resolution FoM [fJ·K²] [c]	650	40	130	59000	110	

[a] 1-point trim and 1st-order fit. [b] 1st-order fit. [c] Energy / Conversion x (Resolution)².

Figure 10.3.6: Summary of measurement results and comparison with previous work.

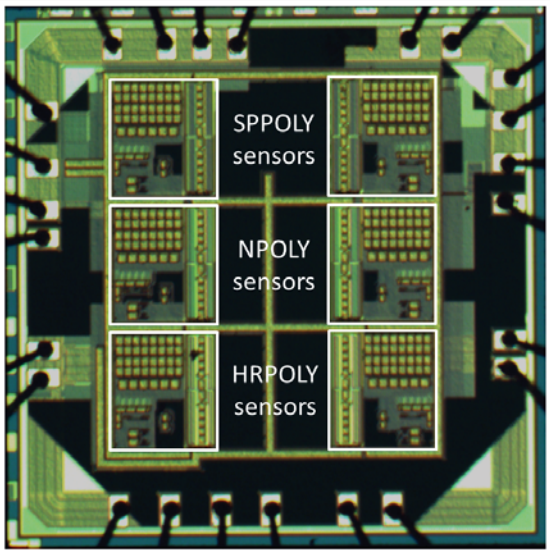

Figure 10.3.7: Micrograph of six temperature sensors on one die.

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