AN APPROACH TO SYSTEMATIC

PHASE-LOCK LOOP DESIGN

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AN APPROACH TO SYSTEMATIC PHASE-LOCK LOOP DESIGN

Proefschrift

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door

Richard Cornelis den Dulk,
geboren te Leidschendam,
elektrotechnisch ingenieur.

Dit proefschrift is goedgekeurd door
prof. dr. ir. R.H.J.M. Otten.

To Marianne,
Paul, Annemarie and Eveline.

ABSTRACT

The analysis of Phase-Lock Loops (PLL's) is treated from a 'design' point of view i.e. it must contribute to a general procedure for the electronic design of phase-lock (sub)systems. The PLL is studied with an eye to a generalized design method suitable for examining dynamic loop properties.

The linear PLL phase model is first analyzed, and properties obtained as a function of the loop filter and input/output topology. The non-linear PLL phase model is then derived based on the essentially non-linear operation characteristic of phase detection. This results for single-loop PLL's with standard phase detectors in design equations yielding the range of operation. Analysis of the noise behavior and the phase detector ripple complete the design analysis. At this point one can start determining the values of the loop components. When specifications cannot be met, the designer has to apply an alternative topology.

The phase-and-frequency detector is investigated and the quadrature loop principle is analyzed. To widen the scope of the study and obtain more design-related information, various topologies for meeting design criteria and their implementation with the simplest electronic circuitry are considered. The adaptive phase detector can be applied to establish independent tracking and acquisition behavior. To obtain high switching speed and low spurious signals, the accumulator type rate multiplier can be employed in combination with a digital harmonic mixer for the frequency control of a sampled PLL frequency multiplier. Frequency detector aided PLL's under conditions with excessive input noise are examined and a multiplying charge-pump phase detector is presented which is ideally suited for implementation of Frequency-and-Phase-Lock Loops.

The design and implementation of All-Digital PLL's is described with emphasis on implementing digitally controlled oscillators. An approach is presented that permits implementation-independent modeling. A new all-digital PLL, based on a combination of two oscillator techniques, is introduced that enlarges the application area of ADPLL's considerably.

An overview is presented that summarizes a priori information, required for design. An example is given of an interactive questionnaire that is used in computer-aided PLL design. A systematic framework for a generally applicable PLL design strategy that emphasizes the choices the designer must make is further explicated.

Case studies are given for the operating conditions of a PLL. Circuits and methods for improved PLL performance, based on cycle slip detection are presented. Studies for the digital implementation of the phase-lock principle are given and the circuit implementation of a new multiplying phase detection method is proposed.

AN APPROACH TO SYSTEMATIC PHASE-LOCK LOOP DESIGN

PREFACE

Work on PLL's within the Department of Electrical Engineering of the Delft University of Technology has a long tradition. Mathematical models of feedback and control systems in pulse and digital circuits were studied by the late Prof. J.W. Alexander. In the early nineteen sixties the special properties of the basic PLL's with a sinusoidal non-linearity were analyzed in 'phase-plane' plots, in order to obtain stability limits.

The (phase-lock) synchronization of stable oscillators to 'standard frequency' transmitters has been a subject of research for many years. A variety of phase-lock tracking receiver architectures have been investigated for obtaining accurate local frequency sources. The phase-lock principle has also been applied to tuning the local oscillator of a communication receiver using the principle of superheterodyne mixing. The dynamic range and the accuracy of the input mixing stage were the subject of research as well.

The design of a receiving system for weather satellite signals was the author's first confrontation with the phase-lock principle. In both the satellite receiver and in the satellite tracking system, phase-locking proved superior to other principles. In particular the phase-tracking monopulse receiver system yielded high quality weather satellite pictures.

By the mid seventies, receiver tuning was accomplished with the aid of a "loose" phase-lock frequency synthesizer in the laboratory of the late Prof. T. Poorter. The phase-lock principle was also employed extensively in the laboratory of Prof. J. Davidse for synchronization in video applications.

The accumulation in Delft of extensive expertise in applying PLL's and the growing need of Dutch industry for more detailed design insight led the late Prof. T. Poorter to initiate, in Januari 1980, a *post-academic course on PLL's, an international symposium on PLL's and applications*, and thereafter regular lectures on *Phase-Lock Loop- and Frequency-synthesis Techniques*.

Consequently research at the DUT was intensified with staff as well as students contributing to a number of publishable results. Study of the PLL has proven to be an extremely fertile substratum for electronics education and electronics research and development. In particular the design and implementation of application-specific communication IC's as well as the investigations to electronic design methodologies and verification strategies are challlenging areas for the employment of phase-lock circuits.

CHAPTER I INTRODUCTION

In the year 1665 the phenomenon of 'phase-lock' was observed for the first time. *Christiaan Huygens* perceived that two adjacent pendulum clocks synchronize over a long time period. Various experiments showed that the synchronism was caused by the fact that the two clocks influence each other by coupling via the wall. The experiments are described in his famous publication from 1673, *"Horologium Oscillatorum"*.

An electronic implementation of the phase-lock principle was first applied by the Frenchman *H. de Bellescize* in 1932. He tried to realize a radio receiver in which the antenna signal was directly converted to base-band (audio). The local oscillator had to be in accurate synchronism with the input carrier frequency.

In spite of the fact that the basic principle was well known, the Phase-Lock Loop (PLL) remained for most electrical engineers a complex concept which was rather sparsely applied. The great breakthrough for the technique came in the forties and fifties with the need for a synchro-nization system for television receivers [*Wendt/Fredenhall*, 1943, *Richman*, 1954]. In order to obtain a recognizable television picture it is

essential that the display and the transmitter are in synchronism. In the case of noise added to the received signal, phase-lock synchronization appeared to yield better results than the circuits previously applied.

IC technology has given another great impulse to the application of phase-lock circuits. An integrated PLL circuit can be used as a 'building block'. Knowledge of external circuit properties is sufficient for the applications engineer. The PLL is then one more part in the 'standard components box' of the electronics designer. *Design* knowledge and experience has, however, not kept pace with the availability and development of integrated PLL circuits. In spite of the overwhelming number of publications in the field, successful applications still come from specialists.

The primary purpose of this thesis is to make a contribution to a *structured design procedure* for applications of the phase-lock principle.

I.1 PLL OPERATION

PLL operating principle: In general the PLL consists of three basic blocks: a phase detector (PD), a loop filter (LF) and a controllable oscillator, e.g. a voltage controlled oscillator (VCO). These three basic components are connected as shown in Fig. 1.1.

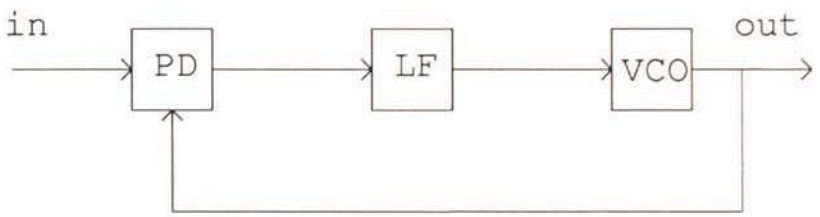


Fig. 1.1 Block diagram PLL

The phase detector compares the phase angle θ_i of an input signal with the phase angle θ_o of the output signal of the VCO. The output voltage of the phase detector is a measure of the phase difference $(\theta_i - \theta_o)$ between these signals and consists generally of a DC component and an AC component. Assuming that the AC component has been suppressed by the loop

filter, the remaining voltage serves as a control signal for the VCO. The control signal modifies the frequency of the VCO in such a way that the phase difference between the input signal and the oscillator signal decreases.

If the loop is *phase locked* the average period of the input signal is equal to the average period of the output signal of the VCO.

The dynamics of this configuration can be inductively derived using linear sub-system transfer functions:

phase detector : $v_d(s) = K_d\ \theta_e(s)$, in which $\theta_e(s) = \theta_o(s) - \theta_i(s)$, and

K_d in units of e.g. [V / rad] or [V / cycle]

loop filter : F(s)

oscillator : $\theta_o(s) = \dfrac{K_o\ v_c(s)}{s}$, with

K_o in units of e.g. [rad / s / V] or [Hz / V]

This leads to the linear PLL phase model of Fig. 1.2, which has been used as a starting point for the analysis.

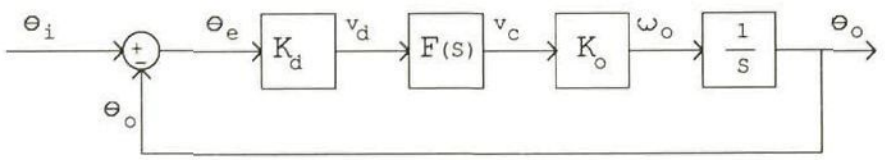


Fig. 1.2 Linear PLL phase model

For this model the transfer functions :

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_d F(s)}{s + K_o K_d F(s)} \quad \text{and} \quad H_e(s) = \frac{\theta_e(s)}{\theta_i(s)} = \frac{s}{s + K_o K_d F(s)}$$

have been derived.

Cursory examination of these expressions yields the insight that even for a loop filter with F(s) = 1, the transfer from input to output is characteristicly lowpass and that from input to error highpass.

This is of course similar to the well-known behavior of nearly all feedback and control systems. The controlled quantities are, however, phase and frequency, because frequency is defined as the the time derivative of phase. This fact is most likely a barrier to understanding PLL technique and application. For example, it is difficult to visualize the frequency spectrum of the phase variation.

I.2 PLL LITERATURE

There are many books on the analysis and design of PLL's. The interrelation between PLL system performance and electronic implementation has received however little attention. The standard PLL books are mainly written from an analysis point of view.

PLL books: The following books in the field, ordered chronologically, have been examined in order to extract the design information needed for the simplest electronic realization that meets particular specifications.

F.M. Gardner
Phaselock techniques
Wiley, New York, 1966

Phaselock techniques 2nd ed.
Wiley, New York, 1979

A.J. Viterbi
Principles of Coherent Communication
McGraw-Hill, New York, 1966

J.J. Stiffler
Theory of Synchronous Communications
Prentice-Hall, Englewood Cliffs, 1971

J. Klapper, J.T. Frankle
Phase-locked and Frequency Feedback Systems
Academic Press, 1972

W.C. Lindsey
Synchronization Systems in Communication and Control
Prentice-Hall, Englewood Cliffs, 1972

V.P. Kroupa
Frequency synthesis
Griffin, London, 1973

J. Gorski-Popiel
Frequency synthesis: Techniques and Applications
IEEE Press, New York, 1975

A. Blanchard
Phase-Locked Loop: Application to Coherent Receiver Design
Wiley, New York, 1976

V. Manassewitch
Frequency synthesizers: Theory and design
Wiley, New York, 1976

W.C. Lindsey, M.K. Simon (Eds.)
Phase-Locked Loops and Their Application
IEEE Press, New York, 1978

H. Geschwinde
Einfuehrung in die PLL technik
Vieweg & Sohn, Braunschweig, 1978

J. Davidse, R.C. den Dulk, E. Nordholt, L.K. Regenbogen
Phase-Lock Loop, post-academic course book
TU Delft, Fac. Electrical Engineering, January 1980

R.E. Best
Theorie und Anwendungen des Phase-Locked Loops
AT Verlag, Aarau, 1981

W.F. Egan
Frequency Synthesis by Phaselock
Wiley, New York, 1981

U.L. Rohde
Digital PLL Frequency Synthesizers
Prentice-Hall, Englewood Cliffs, 1983

R.E. Best
Phase-Locked Loops
McGraw-Hill, New York, 1984

Generally, the link to the electronic circuitry in modern PLL IC's is missing. The relevance of this link has been recognized, as illustrated by the following quotation from Gardner, 1979, p.6:

> "Implementation problems in the loop components, namely loop filter, phase detector, and VCO are discussed in Chapter 6. The design engineer ought to become familiar with this material before attempting any but the simplest of circuits"

In more recent books (circa 1980) numerical examples have been found of IC realizations of PLL's. Most recently, attempts have been made to develop some form of systematization for computer-aiding of the PLL design procedure [Philips, 1989]. The design decision as to whether or not to use an alternative for a single loop has not been treated.

Communication books: In the main application area of PLL's, communications, standard books and related system-oriented books devote little space to the functional behavior of the PLL. Examination of the following books shows that a consistent design procedure is absent. Generally only one section of a chapter on FM demodulation is devoted to PLL's followed on occasion by a section on phase-lock frequency synthesis. In fact, in at least one case a proposed PLL circuit implementation will oscillate[†] .

H. Taub and D.L. Schilling
Principles of Communication systems
McGraw-Hill, New York, 1971

K.K. Clarke and D.T. Hess
Communication circuits
Addison-Wesley, Reading, 1971

W.D. Gregg
Analog & digital Communication
Wiley, New York, 1977

R. Gagliardi
Introduction to communications engineering
Wiley, New York, 1978

J. Hardy
High Frequency Circuit Design
Reston Publishing, Reston, 1979

[†] *[Hardy, 1986, p.301]*

J. Hardy
Electronic Communications Technology
Prentice-Hall, Englewood Cliffs, 1986

W.McC. Siebert
Circuits, Signals and Systems
MIT Press/McGraw-Hill, New York, 1986

For communication electronics, in which phase-lock techniques play an important role, no *structured electronics design procedure* has been proposed. This is surprising, considering the amount of literature available. A recent computer-aided literature search in the general field of *phase-lock loops* delivers an overwhelming number of 4874 references covering the period 1968 to June 1989. Intersect *design* with phase-lock loops reduces the total to about 400 references. Further intersection with *electronics* yields a total of approximately 50 references on electronic design and implementation of PLL's. A closer examination shows that these references primarily concern the design and implementation for more or less specialized applications.

I.3 DESIGN AUTOMATION

A global analysis of the principal design methods suitable for automation is given from the PLL designer's point of view. The term automation is used for the present, shifting role of Computer-Aided Design tools. The role of CAD tools is evolving in the direction of the replacement of human beings in the design process by computerized counterparts.

Design and implementation: The simultaneous application of digital and analog circuitry is significant in communication system implementation. Although the digital share in communication electronics is increasing rapidly, analog circuits continue to be required for signal conditioning. The design process may be reduced to the specification of subsystem requirements such as bandwidth, frequency and signal levels and to the choice of implementation technology and topology. The numerical values for the elements may be analytically verified or simulated.

Communication system-simulation programs (e.g. TOPSIM), which employ the PLL as a building block, are available for the design of communication systems. For example, a Costas PLL is defined as a demodulator block for

BPSK signals. No link to the electronic implementation is required at this abstraction level. It has been shown [Duym, 1986] that to get reliable BPSK demodulator design rules, a lower level of abstraction is required in which the configuration of the demodulator is described.

Simulation programs (e.g. CSMP III or PSI) are available for the block-oriented analysis and design of PLL configurations. It has become clear [Niekolaas, 1982, VanBerkel, 1983, Hakkesteegt, 1987, Grift, 1987, Rudenko, 1988, Regenbogen, 1989], that results of these programs for PLL simulation should be approached with some caution.

For digital (sub)systems several IC-design CAD programs and methods have been developed. The difficult management of the complexity of large circuits, demands highly structured design methods in this field. Amongst others, programs are available to simulate and analyze timing behavior. Simulation of digital phase detector timing behavior [Mulders, 1983, Niekolaas, 1985] has proven to be quite a problem. In verifying phase detector transfer functions with respect to a local non-linearity, partitioning of the circuit turned out to be difficult.

For analog (sub)systems, structured design methods are under investigation, although they are mainly concerned with the basic function of amplification. Circuit simulation programs have been available for a long while. In order to improve correlation with the measured response, the parameters of the device models have to be measured, as has been shown for the modified analysis of a digital phase detector [Mulders, 1985].

To arrive at one general design method for electronic system implementation of the phase-lock principle, the methods for digital and for analog design will be examined in more detail.

Electronic design, analog and digital:

Design methods have been described in hierarchical terms of top-down and bottom-up. Top-down means that the level of abstraction, as the design process unfolds, gradually becomes more detailed. The designs are partitioned into modules in accordance with certain rules. The design rules enable the modules to be designed independently of each other. Bottom-up means that the level of abstraction becomes less detailed during the design process. The desired functionality is achieved through the appropriate selection of components. Only in rare instances will the

designer find components that precisely meet his specifications.

The choice of the electronics designer for a top-down or bottom-up approach will to a great extent depend on either the availability of suitable partitioning *rules*, on the availability of a *circuit catalog*, or on past experience in combining components or modules to realize the desired functionality. The definition or specification step for the functional performance to be realized provides important criteria for this choice. The decision is also dependent on the initial conditions of the design. The design cycle itself is in general precipitated by market-pull or by technology-push mechanisms. *System definition and specification* may come from various sources. Specifications should be met in the case of specific customer requirements, or alternatively the feasibility of a technology may be presented to the market.

Digital design procedures: In the literature several overviews are given that describe IC-design methodologies for automation [Niessen, 1983, Shiva, 1983, Lipp, 1983]. Rules for breaking the design into independent modules at different levels of abstraction are well defined. Specifications and definitions are generally assumed to be clear and fixed by the logic designer, so that the electronics design procedure can proceed in a straight-forward manner.

If a complete catalog of subcircuits is available the design will be bottom-up; if there are regular structures and clear rules for dividing the design into modules the design will be top-down.

Analog design procedures: The choice of analog components in an electronic system is generally dictated by linearity and/or signal-continuity requirements for a voltage or current information carrier. Analog basic functions are: amplification, addition, multiplication, filtering, DC and AC reference generation. Main design goals are: minimal noise generation, maximal linear dynamic range, impedance matching and accuracy. At first sight a principal difference from digital design procedures lies in the impossibility of specifying partitioning rules.

Design methodologies for automating analog IC designs have been described in [Carley/Rutenbar, 1988, Harjani et al., 1987, Degrauwe et al., 1987]. These knowledge-based systems employ building blocks which,

unlike the ones used in bottom-up methods, are not fixed designs from a circuit catalog. According to rules given by specialists, they can be varied infinitely to approach specifications more closely than is possible with a catalog of fixed circuit designs.

The rules can be obtained by defining a hierarchy of basic analog functions that can be independently designed as modules. These basic functions can be well defined by comparing the linearity and/or the signal-continuity requirements to fundamental or technological limitations. If the main design aims have been met, then the analog system can be realized using the modules. The realization of functional blocks whose performance approaches fundamental limits confronts the designer with a difficult problem. He must try to improve the basic functionality, or he must decide to choose a new configuration.

Improvement of the basic function by 'essential measures' is proposed in a recent approach to a "strategic method to analog circuit design" [Montagne/Nordholt, 1989]. This interesting approach seems to be complementary with design automation in that the essential measures establish the limits for varying the automated design of the building blocks.

All approaches reported thus far share one limiting design step: if one intends to generate the *simplest* system realization that approaches the ideal performance as closely as possible, limiting oneself to (improved) basic functions, then the choice of a new configuration is avoided. The criteria for digital, analog or mixed configurations must be examined with the aim of identifying and characterizing those configurations of independent building blocks, that are most likely to meet the specifications, in accordance with the usual practice of the specialist. Explicitly the interrelations between system performance and the electronic implementation must be known.

PLL design approach: In order to provide a unifying design method for electronic system implementation of the phase-lock principle, methods for digital and analog design have been examined. Due to the complex interrelation between PLL system performance and considerations governing the electronic implementation of the circuitry, there is no obvious solution. It will be shown that a topological approach leads in a natural way to the required relations.

Design and implementation procedures have been characterized in various diagrams. In Fig. 1.3 one design model is depicted in which fundamental design steps are given.

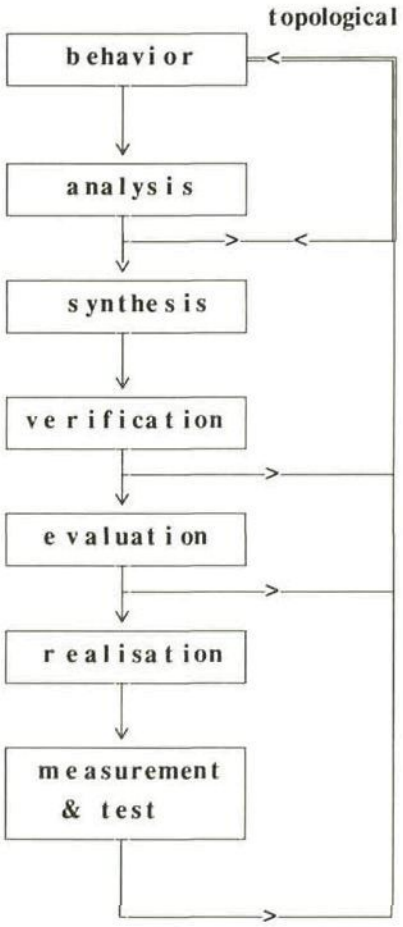


Fig. 1.3 General design cycle

The required subsystem functionality and specifications are described by the general term *global behavior.*

Analysis is employed to obtain insight into and knowledge about the object to be designed. At this point the designer has already chosen a configu-

ration that probably meets some of the behavioral requirements.
Synthesis is the transformation from one abstraction level to a lower level, in which additional detail is introduced. Synthesis implies the choice of a topology at that level. At the highest level only the behavior has been specified. Generally various iterative synthesis steps are required to arrive at a final design.
Verification is the step to validate the behavioral properties at a specific abstraction level.
Evaluation is the step in which alternative solutions are reviewed, and where the choice of a new topology is indicated.
Topology plays an important role in almost every design step.

System definition and subsystem specification are often objects of discussion between the system designer and the electronics designer. Specifications for the behavior of electronic systems are generally not complete. Given a proposed system which is to be implemented electronically, it is the task of the electronics designer to emphasize the interrelation between the required system performance and the best electronic circuit realization in terms of *analog, digital, mixed analog/digital hardware and accompanying software.*

Digital and analog design procedures have a number of aspects in common, since they share the same ultimate purpose.
Steps in digital design procedures can be summarized as:

- behavioral description
- manual or computer-aided logic design
- computer-aided logic simulation
- structural test design
- layout design

Steps in analog design procedures can be characterized as:

- behavioral description
- manual or computer-aided circuit design
- computer-aided circuit analysis
- layout design

At the very least the structure of the decision process for progressing from one step to the next, will in the two cases bear some resemblance.

We have found that the information structure may be likened to that of a questionnaire: *design questions* must be answered. The information itself mainly concerns the validity of the *model descriptions* employed. The final result is always dependent on the chosen topology.

Design generalization:

Almost every design problem can be characterized by two recurrent, general and fundamental steps:

- Choice of a configuration topology that probably meets at least some of the requirements. Choice is an *heuristic* process, in which the experience and skill of the designer implicitly determines the performance.
(heuristics = the skilled art required to meet a specific truth by step-by-step logical reasoning) [Greek *heuriskoo* = to discover].

- Dimensioning of the elements of the topology. Dimensioning is an *algorithmic* process, in which the validity of the models used plays an important role.
(algorithm = the art of arithmetic, the science of numbering, the art of computation) [Lat. *algorismus* from Arab. *al-Chwarizmi* = the man from Khiwa (nickname of an Arab mathematician)].

In order to obtain systematic design procedures, more information about the configuration choice is required, and the questions which have been posed in that step, must be examined. The step-by-step logical reasoning must be traced for recovering and recording practical design knowledge. This approach is labeled topological because it emphasizes the sequential way along the interconnections pattern of the available material.

It will be proposed and illustrated for the design of PLL's and related phase-lock systems that a topological characterization can make a contribution to structured electronics design and consequently to design automation.

I.4 TOPOLOGICAL PLL INFORMATION

To obtain systematic design information on PLL's, the design *questions* must be made explicit and the common *model* descriptions must be analyzed.

It is possible to divide the various applications of the PLL into distinct classes and to test for appropriate design constraints. This would shift the question of model validity into the background.

We could also propose distinct classes, based on the dominating application constraint or property such as: Signal-to-Noise Ratio, which is small or large; the frequency range (f_{max} - f_{min}) that can be small or large compared to f_{in}; the level of the input signal, which can be variable or fixed, small or large; the waveform of the input signal; the dynamic control properties, the order and type of the feedback loop; the phase detector type; the phase and frequency control capabilities; etc.

Preliminary study has shown that these approaches would lead inevitably to entanglement in multi-level decision processes

Considered analysis of general design procedures, and on the basis of substantial experience we have chosen the following global route in the multi-dimensional web of PLL design and application:

- Linear PLL phase model analysis
- Black-box approach for applications design
- In-loop components examination
- Dimensioning limitations
- Peripherals, Out-of-loop components
- Multi detector loops properties
- Special circuitry and design constraints
  - tracking and acquisition
  - spurious suppression and switching speed
  - acquisition and noise
- All-Digital PLL's

The topological description of a PLL consists of the interrelation between system performance and electronic implementation for loop configuration,

loop filter, input/output relations, non-linearities and peripheral circuits.

Outline of the thesis

The operative principle has been described in Chapter I. No structured information on the design and implementation of PLL's turned up in an extensive search of the literature, due undoubtedly to the inter-relation between PLL system performance and implementation considerations. Design procedures for communication systems, control systems, digital IC design and analog IC design have been examined to find useful methods for PLL design. This survey has in turn led to a design generalization that defines the topological approach to be further explored in this thesis.

In Chapter II the fundamental linear analysis of single-loop PLL's is reviewed in order to obtain design limits for the dynamic properties desired. Dimensioning then leads to the basic (non-linear) analysis of standard PLL topologies, which facilitates the derivation of operating range, etc. Synthesis of applications leads to inherent design compromises for the linear and the non-linear operating modes, which are circuit dependent.

In Chapter III design is emphasized. Performance improvement of the single-loop topology can be obtained by better loop components or by a multi-detector topology. Several new circuit solutions are presented that relieve design compromises such as tracking and acquisition, switching speed and spurious suppression, as well as acquisition and noise.

All-Digital PLL's are described in Chapter IV. The principles for implementing digitally controlled oscillators are reviewed. The possibilities for implementing digital loops are described and an approach for a general model is proposed. The designer can then conclude in which applications an all-digital solution is appropriate. A new All-Digital PLL topology, based on rate multiplier techniques, that considerably enlarges the area of applicability of ADPLL's is introduced.

In Chapter V an overview is given of PLL design, in which a PLL-Design-Questionnaire is described that can be used as a checklist. A systematic procedure for step-by-step PLL design is presented that emphasizes the substantive answers to the design questions at each step.

Chapter VI is composed of the publications of case studies performed by the author on PLL implementation and related subjects. The operating conditions of PLL's have been examined, proposals for circuit implementation for improved PLL performance have been presented and digital PLL implementations have been studied. Finally a charge-pump compatible multiplicative phase detector is presented that may be used when excessive input noise is present.

In Chapter VII conclusions are drawn with respect to the design aspects that have been discussed in this thesis.

CHAPTER II PLL ANALYSIS

PLL's with specific dynamic properties can be designed with the aid of the linear model given in Chapter I and various loop filter topologies. Design constraints will be given for the most frequently applied loop filters. Study of input/output topology leads in a natural way to application in modulation and demodulation. The introduction of a divider in the standard loop extends the input/output topology to sixteen possible single-input/single-output combinations of which nine are useful applications in the communication area. Initial restrictions for this simple design model manifest themselves when modulation is considered.

An alternative linear model will be presented, the *PLL Frequency Model*, in which frequency is the controlled quantity. The PLL is a *phase-control* system and consequently also a *frequency-control* system (frequency being defined as the time derivative of phase $\omega = d\phi/dt$, or, in other words, frequency is the angular speed).

In practice, PLL response is limited in the magnitude of the phase error. This will be modeled in section II.2 by the inherent non-linearity of the phase detector. The design formulas for the operating ranges are derived from the *non-linear model* of the PLL. Furthermore, the non-linear

model gives design constraints for PLL's operating with input noise as well as unwanted AC components of the phase detector (ripple). In completion, switching effects and sampling of phase detectors are reviewed.

II.1 LINEAR ANALYSIS

The linear loop analysis is treated from the designer's point of view. Although much of the material will be known, arranging the material according to our method, yields design restrictions that may be recognized immediately, and will show some aspects, which have mostly been ignored in literature. Single loop performance depends on the PLL topology elements:

- Loop Filter F(s),
- I/O, input/output,
- Phase Detector.

The design constraints of the dynamic properties that were developed from the loop filter configuration and from the input/output relations will be examined. The linear model assumes that the PLL is in lock, i.e. the average output frequency of the loop is equal to the average input frequency. Only small phase variations will assumed to be present. The dynamic properties are determined by the small-signal transfer factors of the loop components.

II.1.A Loop filter considerations

The dynamic requirements of the application are specified in terms of response time or bandwidth. The topology and time constants of the loop filter are the keys to controlling the dynamic performance. In the loop filter, dynamic parameters can be traded off most easily to meet the requirements. The other loop components have values that cannot be changed as easily.

Unless stated otherwise we will assume fixed values for K_o and K_d.

No Loop Filter: If the loop does not have a loop filter, the loop shows a first order dynamic behavior, so if F(s) = 1 the PLL transfer functions will be:

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_d}{s + K_o K_d} \qquad H_e(s) = \frac{\theta_e(s)}{\theta_i(s)} = \frac{s}{s + K_o K_d}$$

Consequently the design constraints of a first order loop will be:
Loop gain $K_o K_d = \omega_L = 2\pi f_L = 1/\tau_L = \omega_{0dB}$(open loop) = ω_{-3dB}(closed loop).

The dynamic behavior of the first-order PLL is fully determined by the loop gain, which can be only altered by inserting an amplifier or an attenuator between phase detector and oscillator.

To avoid confusion in calculations, it should be noted, that the loop gain $K_o K_d$ has been expressed fundamentally as angular frequency ω_L, regardless of the (of course equally referenced) units of K_o and K_d.

Passive loop filter: With a first-order loop filter second-order dynamic performance can be realized for the loop. The simplest implementation for this is the passive loop filter shown in Fig. 2.1.

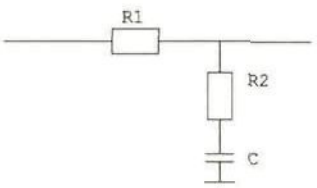


Fig. 2.1. Passive loop filter

With $R_1C = \tau_1$ and $R_2C = \tau_2$ its transfer function can be written as

$$F(s) = \frac{s\tau_2 + 1}{s(\tau_1+\tau_2)+1}.$$

The transfer function of the PLL then becomes:

$$H(s) = \frac{K_o K_d (s\tau_2 + 1)/(\tau_1+\tau_2)}{s^2 + s\left(\frac{1+K_o K_d \tau_2}{\tau_1+\tau_2}\right) + \frac{K_o K_d}{\tau_1+\tau_2}}$$

When we define the undamped angular frequency ω_n as

$$\omega_n = \left(\frac{K_o K_d}{(\tau_1+\tau_2)} \right)^{1/2}$$ and the damping factor ζ as

$$\zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_o K_d}\right)$$ we obtain

$$H(s) = \frac{s\omega_n\left(2\zeta - \frac{\omega_n}{K_o K_d}\right) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \{1\}$$

The phase error transfer function becomes

$$H_e(s) = \frac{s^2 + s/(\tau_1+\tau_2)}{s^2 + s\left(\frac{1+K_o K_d \tau_2}{(\tau_1+\tau_2)}\right) + \frac{K_o K_d}{(\tau_1+\tau_2)}} = \frac{s^2 + \frac{\omega_n^2}{K_o K_d} s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \{2\}$$

The natural frequency ω_n and the damping factor ζ can be determined independently, by calculating the values of the two loop filter time constants τ_1 and τ_2. However, examination of {1} yields a basic loop design constraint for a loop with a passive loop filter:

If $\tau_2 > 0$, then $\frac{\omega_n}{2\zeta} < K_o K_d$ must hold.

This can also be concluded from:

$$K_{AC} = \frac{K_o K_d \tau_2}{(\tau_1+\tau_2)} = 2\zeta\omega_n - \frac{\omega_n^2}{K_o K_d} \quad \text{or} \quad \frac{2\zeta}{\omega_n} = \tau_2 + \frac{1}{K_o K_d}$$

Consequently, there is an upper bound for the fraction of the design quantities that determine the PLL's dynamic properties for any realizable, passive loop filter:

> $\omega_n/2\zeta$ must be smaller than the loop gain $K_o K_d$.

This means that in any case the control bandwidth is smaller than the one of the first-order loop.

If $R_2 = 0$ the transfer function of the loop filter is: $F(s) = \dfrac{1}{s\tau_1 + 1}$

The PLL transfer functions then become:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad H_e(s) = \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \{3\}$$

In this case the design constraints to choose the dynamic properties are:

$$2\zeta\omega_n = 1/\tau_1 \quad \text{or} \quad \frac{\omega_n}{2\zeta} = K_o K_d$$

This means that the natural frequency and the damping factor cannot be designed independently. The value of the time constant τ_1 of the filter determines ω_n and ζ simultaneously. This is equal to the limiting case of the above-mentioned upper bound for $\omega_n/2\zeta$.

Active Loop Filter: With a first-order active loop filter, a second-order, type-2 dynamic loop performance can be realized. The active loop filter is shown in Fig. 2.2.

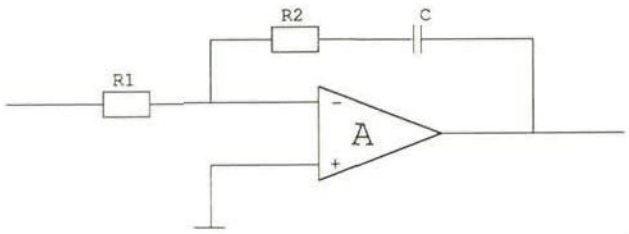


Fig. 2.2. Active loop filter

With $A = F(0) \gg 1$ and for frequencies $\omega \ll \omega_A$ (ω_{0dB}, open-loop gain cross-over of the amplifier), the transfer function of the loop filter ($R_1C = \tau_1$ and $R_2C = \tau_2$) can be written as:

$$F(s) = \frac{-A(s\tau_2 + 1)}{(1 + A)s\tau_1 + s\tau_2 + 1} \approx -\frac{s\tau_2 + 1}{s\tau_1} = -\frac{\tau_2}{\tau_1}\left(1 + \frac{1}{s\tau_2}\right) = -K_p\left(1 + \frac{1}{s\tau_2}\right) \quad \{4\}$$

With the definitions $\omega_n = \left(\frac{K_o K_d}{\tau_1}\right)^{1/2}$ and $\zeta = \omega_n \tau_2/2$ the PLL transfer functions become:

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \text{and} \qquad \{5\}$$

$$H_e(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \{6\}$$

We can define $\tau_{loop} = 1/\zeta\omega_n$ and the AC loop gain $2\zeta\omega_n$ (= open loop ω_{0dB})

$$2\zeta\omega_n = K_o K_d \frac{\tau_2}{\tau_1} = K_o K_d K_p = K_{AC}$$

Then the natural angular frequency and the damping factor can be defined as:

$$\omega_n = \sqrt{\frac{K_{AC}}{\tau_2}} \qquad \zeta = \tfrac{1}{2}\sqrt{K_{AC}\,\tau_2}$$

From examining the expressions, it may be concluded that both parameters ω_n and ζ can be determined independently by calculating τ_1 and τ_2, or, in other terms, by calculating K_p and τ_2. Unlike the passive loop filter, there is virtually no restriction in the range for ω_{0dB} caused by the loop gain $K_o K_d$.

High-gain loop performance approximation: When we look at the above given PLL transfer functions H(s) and $H_e(s)$, we can conclude that in certain cases the loop transfer functions for PLL's with passive loop filter can be approximated by those of the second-order type-2 PLL. In this case the PLL with passive loop filter will be called a high-gain loop.

□ For a PLL with an active loop filter, the open loop gain A of the amplifier must be much larger than τ_2/τ_1. This can be verified by inspecting the formulas {4}. For special applications this condition can be met by implementing the loop filter according to the last expression of {4}. For frequency synthesis this was implicitly proposed in [Underhill/Jordan, 1979].

□ In addition to the literature on this subject, a loop with passive filter with $\tau_2 > 0$, must *simultaneously* satisfy the *two* relations:

$$\boxed{\frac{\omega_n}{2\zeta} \ll K_o K_d \quad \& \quad \omega_n^2 \ll K_o K_d/\text{sec}}$$

or, expressed in quantities of the loop components:

$$\boxed{K_o K_d \gg \frac{1}{\tau_2} \quad \& \quad K_o K_d/\text{sec} \gg \omega_n^2}$$

This can be verified by comparing the formulas {1} and {2} to {5} and {6}.

□ A comparison of the formulas in {3} to those in {5} and {6} shows that one can never realize high-gain performance with a passive filter loop in which $\tau_2 = 0$.

□ Loops with a passive loop filter, in which $\tau_2 = 0$ and $\tau_1 \leq \dfrac{1}{4K_o K_d}$, can be approximated by the transfer functions a first-order loop.

Noise: In many applications, the requirements for the dynamic loop properties in the presence of input noise, will be specified in terms of noise bandwidth of the loop, or variance of the output phase. For the above mentioned loop filters, design expressions will be given here concerning noise [Gardner, 1979]. The noise bandwidth of a practical filter is defined as the ideal bandwidth (infinite steep slopes) that has the same power transfer. The noise bandwidth B_L expressed in [Hz] for the above mentioned loop filters, is given by:

first-order loop: $$B_L = K_o K_d/4$$

passive filter loop:

$$B_L = \frac{K_o K_d}{4} \frac{K_o K_d \tau_2^2 + \tau_1 + \tau_2}{K_o K_d \tau_2 (\tau_1+\tau_2) + \tau_1 + \tau_2} = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta} - \frac{\omega_n}{K_o K_d} + \frac{\omega_n^2}{4\zeta (K_o K_d)^2} \right)$$

active filter loop:

$$B_L = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta} \right)$$

For Gaussian, additive, 'white' noise over the input noise bandwidth B_i, the output (phase) noise has been approximated with [Gardner, 1979]:

Variance of output phase $$\overline{\theta_{no}^2} = \frac{2B_L N_0}{V_i^2},$$

in which B_L is the noise bandwidth of the loop in [Hz], N_0 is the uniform spectral power density of the additive input noise in [W/Hz] and V_i is the amplitude of the input signal (see also section II.2D).

Settling Time and Overshoot, Steady-state Errors: These quantities are often specified for the dynamic properties of the loop. The settling time and the overshoot of the step response are important design requirements. These are given here for a predominantly second-order loop.

The settling time for $\zeta < 1$ is expressed as $t_{5\%} \approx \frac{3}{\zeta\omega_n}$ or $t_{2\%} \approx \frac{4}{\zeta\omega_n}$, which are comparable to 3τ and 4τ of a first order system respectively.

The response has no overshoot when the damping factor $\zeta \geq 1$. If $\zeta < 1$ the overshoot equals $M_{\%} = \exp\left[\frac{-\pi\zeta}{1-\zeta^2}\right].100\%$ for any second order system.

By means of the final value theorem of Laplace transforms, the steady-state phase error resulting from a step change of the input phase can be determined. Any phase-lock loop does not show a steady-state error when the input phase is changed, independently of the loop filter. It should be noted that this does not hold for a step change in the time derivative of the input phase, or, in other words, for an input frequency step. This steady-state error is a function of the DC loop gain.

Linear loop model: The above described expressions are applicable to small-signal situations, in which the loop can be described by means of the linear model. The dynamic properties of the PLL have been characterized as linear quantities like: ω_n, ζ, B_L, $H(s)$ and $H_e(s)$. It should be noted that in practice a PLL always has a limited response in phase error, so this linear model has to be extended by non-linearities.

Higher order loops: So far the discussion may suggest that the highest loop order in practice is two. And indeed, many control systems can be

considered as predominantly second-order, but there are applications in which a higher order loop is necessary. To our knowledge no loop has been constructed with an intended order higher than three, although it is not impossible that extraordinary applications require fifth order loops.

A higher order than three, however, is more difficult to stabilize. From control theory the second-order loop, as commonly built, is unconditionally stable, as far as the model description is valid. Parasitic circuit elements often cause an intended second-order loop to be of higher order. Usually the loop is treated as basically second-order, whereas the differences are handled separately as deviations.

In the non-linear analysis, we will meet situations in which a second-order loop design results in a real third-order loop. Third order loops are found in frequency synthesis [Underhill, 1980], motor speed control, and doppler frequency tracking systems.

II.1.B Input / output considerations

So far, we have analyzed the single loop topology with input and output as usual. It is taken for granted that the standard loop I/O, considering the two input signals (θ_i and θ_o) of the phase detector as respectively input and output of the loop, includes the signal of the voltage controlled oscillator (θ_o). The transfer function matching this I/O is given as H(s). From a tactic point of view no reason is mentioned for giving also the error transfer function $H_e(s)$. From control theory we know that, in case of a unity feedback system, $H_e(s)$ can be expressed as $H_e(s) = 1 - H(s)$. Naturally a reason for providing this 'redundant' information is present.

First, to obtain the complete conditions for a PLL with passive filter to behave as a 'high-gain' loop, it was necessary to take $H_e(s)$ into consideration. Another reason will be given in this section, where we will examine the possible inputs and outputs of the PLL. A third reason will be given in the section concerning the non-linear PLL model.

Fig. 2.3 shows the linear model of the PLL with the useful input and output (I/O) signals. In this figure it is shown that the phase error signal θ_e can be used for I/O through the phase detector.

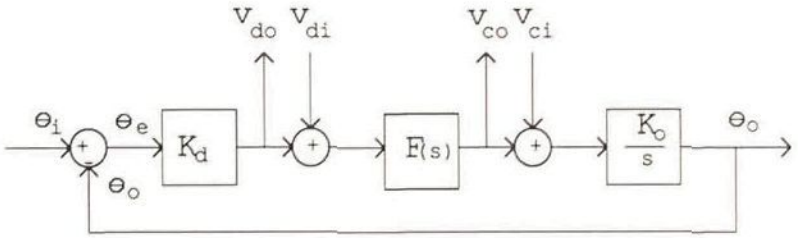


Fig. 2.3 I/O model of linear Phase-Lock Loop

Three possible input signals and three possible output signals are given. If we consider the PLL as a 'black box', nine (single input/ single output) combinations can be used as applications of the linear model.

These I/O combinations are shown in the application chart of Fig. 2.4. The familiar applications as tracking filter/synchronization, modulation, and demodulation will easily be recognized. We will examine these applications for design purposes. For each application, except measurement[†] , the transfer functions and the restrictions will be given.

out \ in	θ_i	v_{di}	v_{ci}
θ_o	tracking filter	PM modulation	FM modulation
v_{do}	PM demodulation	measurement	measurement
v_{co}	FM demodulation	measurement	measurement

Fig. 2.4 I/O applications cross-tabulation chart [‡]

[†] *In this thesis the 'measurement' applications are considered as to be far beyond the 'communication electronics' field.*

[‡] *FM modulation I/O can also be used if a variable, high-power noisy oscillator has to be 'cleaned up' by the PLL. The self-noise of the oscillator is modeled as variations of* v_c.

The following transfer functions can be derived from the I/O model in Fig. 2.3. The quantities v_{di}, v_{do}, etc have been used for reasons of compactness and must be read as $v_{di}(s)$ etc. The transfer functions for these applications are expressed in terms of H(s) and $H_e(s)$ from the standard I/O.

	demodulation	modulation
PM	$\frac{v_{do}}{\theta_i} = K_d H_e(s)$	$\frac{\theta_o}{v_{di}} = \frac{H(s)}{K_d}$
FM	$\frac{v_{co}}{\theta_i} = \frac{s \cdot H(s)}{K_o}$	$\frac{\theta_o}{v_{ci}} = \frac{K_o H_e(s)}{s}$

A closer examination of these expressions yields the requirements for the dynamic properties of these input/output relations. Possible design constraints for the intended applications will be expressed in terms of dynamic properties of the standard loop.

For $\frac{\theta_o}{\theta_i} = H(s)$ no additional restrictions can be derived yet for the linear PLL phase model. The purpose of angular modulation and demodulation is to obtain a frequency-independent transfer of the amplitude of the modulation signal.

The *amplitude of variations* of phase or frequency as a controlled variable follows the fundamental relations of angular modulation:

$$\text{Phase deviation } \Delta\phi = \frac{\text{frequency deviation } \Delta\omega}{\text{modulation frequency } \mu} = \text{Modulation index m}$$

For PM (phase modulation) the amplitude $\Delta\phi$ is proportional to the modulation amplitude for all modulation frequencies; for FM (frequency modulation) the amplitude $\Delta\omega$ is proportional to the modulation amplitude for all μ.

If μ is the modulation frequency of the PM input signal, the transfer function to the PM output is $\frac{v_{do}}{\theta_i} = K_d H_e(s)$. The transfer function $H_e(s)$ has a highpass behavior, so for frequency-independent demodulation of PM the condition holds: $\omega_n \ll \mu$.

The opposite holds for PM modulation due to the lowpass behavior of H(s) in the expression $\frac{\theta_o}{v_{di}} = \frac{H(s)}{K_d}$. The condition is: $\omega_n \gg \mu$.

Frequency-independent FM demodulation via $\frac{v_{co}}{\theta_i} = \frac{s \cdot H(s)}{K_o}$ is conditioned by $\omega_n \gg \mu$. At first sight this is a logical condition, because H(s) has a lowpass behavior, but the differentiation represented by s in the numerator is a highpass action. This apparent contradiction will be explained below.

The transfer function $\frac{\theta_o}{v_{ci}} = \frac{K_o H_e(s)}{s}$ is frequency-independent if $\omega_n \ll \mu$. We find differentiation and integration in the transfer functions for FM demodulation and modulation respectively. This is caused by the definition: the momentary frequency is the time derivative of phase. A model will be introduced in which frequency deviation $\Delta\omega$ and modulation frequency μ easily can be modeled by the addition of an input oscillator.

The *PLL-Frequency Model* is shown in Fig. 2.5. The variable for the integrator at the input represents the implied variable ω_i of the input *variable* θ_i *used so far. The quiescent frequencies* Ω_o *and* Ω_i *of the* VCO and the input signal can be introduced respectively by summing points after K_o and before the input integrator.

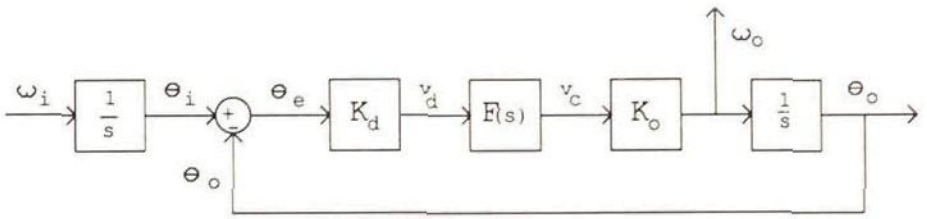


Fig. 2.5 Frequency model of linear PLL

The quantities Ω_o and Ω_i have been assumed implicitly for the linear model in literature, but now these have become explicit. This was allowed, because the assumptions were $\Omega_i = \Omega_o = 0$. Only the deviations from a fixed

quantity have been investigated until now.
This model can be modified into a simpler PLL frequency model by application of block diagram algebra from control theory. The two integrator blocks can be shifted through the summing point. This yields the PLL Frequency Model of Fig. 2.6.

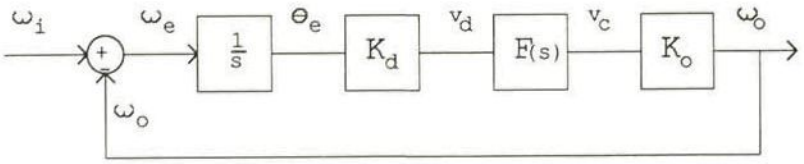


Fig. 2.6 Simple frequency model of linear PLL

It should be noted that consequently the function of the phase detector is now changed into a *frequency difference detector*. The model gives a good idea of the operation of the PLL as a FM demodulator.
The following transfer functions have been derived from this model:

$$\frac{\omega_o(s)}{\omega_i(s)} = H(s), \text{ the frequency transfer function,}$$

$$\frac{v_c(s)}{\omega_i(s)} = \frac{H(s)}{K_o}, \text{ the FM demodulation transfer function, and}$$

$$\frac{\omega_o(s)}{v_c(s)} = K_o H_e(s), \text{ the FM modulation transfer function,}$$

in which $H(s)$ and $H_e(s)$ are equal to those from the PLL Phase Model.
From this transfer functions we can clearly see that the modulation frequency μ and the natural undamped frequency ω_n must satisfy certain *design* conditions to yield a frequency-independent transfer.

Also the determination of the steady-state errors becomes easier. It is clear, that no steady-state frequency error remains after a frequency step. The steady-state phase error after a step $\Delta\Omega$ in frequency is found by applying the final value theorem to: $\theta_e/\omega_i = 1/(s + K_d K_o F(s))$.

The steady-state phase error becomes $\theta_{e,t\to\infty} = \dfrac{\Delta\Omega}{K_d K_o F(0)}$

A much more important conclusion can be derived from the frequency transfer function $\omega_o(s)/\omega_i(s)$ of the PLL Frequency Model. This transfer function is *exactly equal* to the phase transfer function θ_o/θ_i. Consequently the performance must be the same and design limits for the dynamic properties as a function of loop filter topology, derived for phase variations, must be equal. The quantity $K_o K_d$ has been defined as loop gain, which is equal to the loop bandwidth ω_{-3dB} for a first order loop. The loop gain determines the dynamic properties of the loop and should be smaller than the input frequency. The frequency of variations of *frequency* as a controlled variable, should be lower than the variable itself. This may be explained for practical design purposes by considering $K_o K_d$ as the modulation frequency μ of the output signal of the loop.

The value of *frequency* μ *of variations of phase* as a controlled quantity seems to be unlimited. This follows from the description of an angular modulated signal:

$\sin\left[\omega_c t + \dfrac{\Delta\omega}{\mu}\sin\mu t\right]$, in which ω_c is the carrier frequency, $\Delta\omega$ is the frequency deviation and μ is the modulation frequency.

The 'frequency of the *frequency*', however, is still a strange term, because it means the same modulation frequency μ of the time derivative of phase, so this frequency seems to be unlimited as well. The instantaneous angular frequency $\dfrac{d\phi}{dt} = \omega_c + \Delta\omega\cos\mu t$ shows no other limit than $\Delta\omega < \omega_c$. The modulating frequency μ may be unlimited. This can be verified by examining modulation with a physically realizable step change (infinite bandwidth) in frequency.

However, from modulation theory we know the purpose of modulation: modulating means shifting the baseband function to a bandpass function. Angular modulation is non-linear modulation employing an infinite frequency band in theory. In practice this is approximated by a frequency spectrum $2\Delta\omega + 2\mu$ (Carson's rule) on a center frequency ω_c. For real frequencies the limit to avoid baseband and bandpass overlap, must satisfy

the relation: $\omega_c - (\Delta\omega + \mu) > \mu$. This implies for $\Delta\omega \to 0$, that the modulation frequency $\mu < \omega_c/2$

It will be equally easy to explain that frequency shift keying modulation with a frequency higher than $(\omega_c - \varepsilon)/2$ is meaningless, even for a magnitude of the frequency steps $\Delta\Omega \to 0$. The period time of successive single cycles of the carrier frequency cannot be distinguished from each other for demodulation. In other words, the repetition rate of variations f_m with respect to the controlled quantity 'repetition rate' f_i should be lower than $f_i/2$. This is an absolute design limit, when frequency variables are defined as the inverse of their repetition time.

From experience, we know that ignoring this *design limit* is the most probable erroneous step in the design.

So far the requirements for the dynamic properties of the standard loop consisting of phase detector, loop filter and oscillator have been analyzed as a function of the implementation of the loop filter. The approach concerning the I/O relations, considered the single loop PLL as a 'black box' and extracted design information for main applications. In addition the PLL Frequency Model was introduced, to explain the transfer functions of FM applications. We showed that this PLL Frequency Model reveals a practical design limit for the dynamic properties of PLL's that has not been given anywhere so far.

II.1.C Linear loop model with divider

The single loop topology with different input and output has been analyzed. The I/O considerations lead to modulation and demodulation applications, in which the matching transfer functions have been given as H(s) and $H_e(s)$. Although in the case of a unity feedback system, $H_e(s)$ can be expressed as $H_e(s) = 1 - H(s)$, the purpose of also giving the error transfer function $H_e(s)$ became clear from the highpass loop behavior required for FM modulation and PM demodulation.

In many applications a divider with division factor N is used within the loop. Then it depends on the I/O relation whether the relation between $H_e(s)$ and H(s) is still valid. A PLL with divider may be modeled as a non-unity feedback system or as a basic configuration with modified (=

divided) oscillator. The loop behavior for the latter, is then explained by converting the oscillator transfer factor K_o to a new one K_o/N , and by using the basic model to obtain more information.

We will first consider the differences with the previous PLL I/O model, and then the validity of the model approach. In Fig. 2.7 a PLL with divider is shown as I/O model.

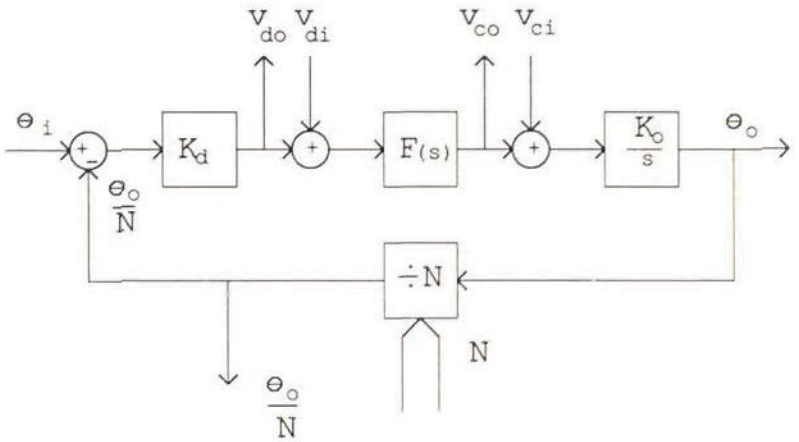


Fig. 2.7 I/O model of linear Phase-Lock Loop with divider

Compared to the I/O model of Fig. 2.3, with three inputs and three outputs the addition of the divider increases potential input signals and output signals by one. The PLL, again as a 'black box', therefore has sixteen (single input/single output) combinations. These I/O combinations are shown in the application cross-tabulation chart of Fig. 2.8.

In the new chart there are at least two new applications: frequency synthesis and a tracking filter with an oscillator with multi-phase outputs. We also see two additional possibilities for PM and FM modulation. To find design limitations, we will first examine the transfer functions H(s) and $H_e(s)$, which determine the dynamic properties of the loop with divider. Then the I/O transfer functions will be investigated.

in / out	θ_i	v_{di}	v_{ci}	N
θ_o	fixed freq.synth.	PM modulation	FM modulation	freq.ch. synth.
v_{do}	PM demodulation	measurement	measurement	measurement
v_{co}	FM demodulation	measurement	measurement	measurement
θ_o/N	tracking filter multi-phase osc.	PM modulation	FM modulation	measurement

Fig. 2.8 I/O applications cross-tabulation chart

Loop dynamics did not really change, because the configuration can still be modeled as a single loop. For a first order loop the transfer functions become:

$$H(s) = \frac{\theta_o/N}{\theta_i} = \frac{K_o K_d / N}{s + K_o K_d/N} \quad \text{and} \quad H_e(s) = \frac{\theta_e}{\theta_i} = \frac{s}{s + K_o K_d/N}$$

For a second order loop with passive filter in which $\tau_2 > 0$, the expressions for the natural loop frequency and the damping factor become:

$$\omega_n = \left(\frac{K_o K_d}{N(\tau_1+\tau_2)} \right)^{1/2} \quad \text{and} \quad \zeta = \frac{\omega_n}{2} \left(\tau_2 + \frac{N}{K_o K_d} \right)$$

We obtain the expressions for the transfer functions:

$$H(s) = \frac{s\omega_n \left(2\zeta - \frac{N\omega_n}{K_o K_d} \right) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad H_e(s) = \frac{s^2 + \frac{N\omega_n^2}{K_o K_d} s}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

For a second order loop with active filter the expressions for the dynamic properties and transfer functions are:

$$\omega_n = \left(\frac{K_o K_d}{N\tau_1}\right)^{1/2} \quad \text{and} \quad \zeta = \omega_n \tau_2/2$$

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad H_e(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

If we take the output signal from the divider, θ_o/N, the basic expressions are only modified in this respect: the oscillator transfer factor K_o has changed into K_o/N.
For most formulas this does not cause different dynamic behavior. The realization of ω_n and ζ does not pose additional problems. Only the conditions for the high-gain approximation of a loop with realizable passive filter seem to become more stringent, because the loop gain is decreased by factor N.
The approximation of high-gain behavior of a passive filter loop, in which $\tau_2 > 0$, is valid when

$$\frac{\omega_n}{2\zeta} \ll \frac{K_o K_d}{N} \quad \& \quad \omega_n^2 \ll \frac{K_o K_d/\text{sec}}{N} \quad \text{or} \quad K_o K_d \gg \frac{N}{\tau_2} \quad \& \quad K_o K_d/\text{sec} \gg N\omega_n^2$$

One might think that it is more difficult (because of this factor N) to meet these requirements. Fortunately this is not true in general, because joining the division factor N in the loop causes an increase of the output frequency by factor N. Most probably also K_o is a factor N higher, so the conditions for high-gain behavior of a loop with passive filter are not that different.

The transfer functions from the I/O model in Fig. 2.7 will be derived in the following. These will be expressed in terms of H(s) and $H_e(s)$.

Tracking filter with multi-phase oscillator: $\dfrac{\theta_o/N}{\theta_i} = H(s)$

Fixed frequency synthesis: $\dfrac{\theta_o}{\theta_i} = N.H(s)$

The modulation and demodulation transfer functions are conveniently arranged as follows:

	demodulation	modulation	
PM	$\frac{v_{do}}{\theta_i} = K_d H_e(s)$	$\frac{\theta_o/N}{v_{di}} = \frac{H(s)}{K_d}$	or $\frac{\theta_o}{v_{di}} = \frac{N \cdot H(s)}{K_d}$
FM	$\frac{v_{co}}{\theta_i} = \frac{s.H(s).N}{K_o}$	$\frac{\theta_o/N}{v_{ci}} = \frac{K_o H_e(s)}{N \cdot s}$	or $\frac{\theta_o}{v_{ci}} = \frac{K_o H_e(s)}{s}$

The last column shows the transfer functions of the additional modulation possibilities for this I/O.

For frequency-channel synthesis, a change in the division factor has to be considered as an input variable, and the transfer function changes simultaneously. A change in division factor from $N_1 \Rightarrow N_2$ gives a change of the dynamic parameters $\omega_{n1}, \zeta_1 \Rightarrow \omega_{n2}, \zeta_2$. In this case the dynamic properties of the loop are dependent on the input variable. The perturbation of the loop is a step change in frequency, possibly in combination with a *step in phase. A change from* $N_1 \Rightarrow N_2$ *is controlled in a time proportional* to $1/\omega_{n2}\zeta_2$, while a change from $N_2 \Rightarrow N_1$ has a switching speed proportional to $1/\omega_{n1}\zeta_1$. The minima and maxima of the dynamic loop parameters ω_n and ζ should be examined carefully: $\frac{\zeta_{max}}{\zeta_{min}} = \frac{\omega_{n,max}}{\omega_{n,min}} = \sqrt{\frac{N_{max}}{N_{min}}}$.

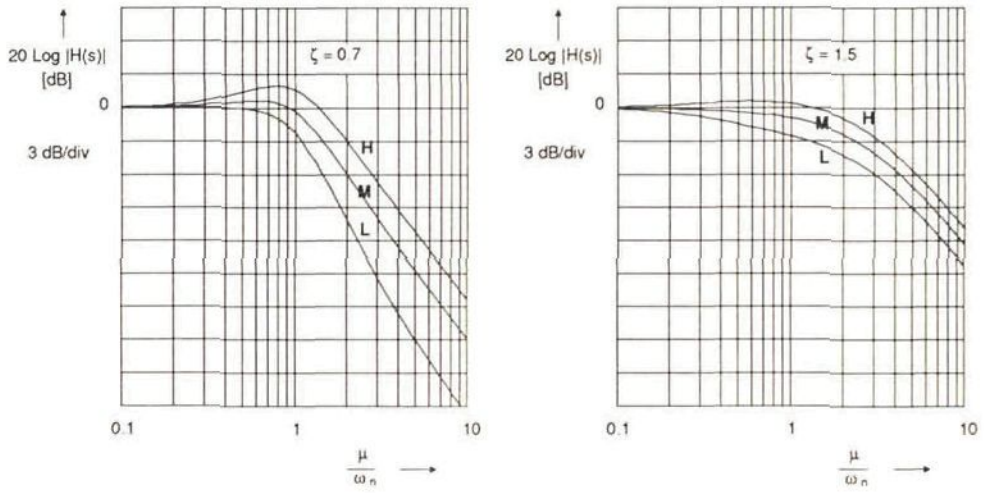
If for example N is increased by factor 25, the damping and natural frequency will vary factor 5, which yields a mostly intolerable factor 25 variation. Special measures are then needed to obtain a response that is fast enough [see also Underhill et al., 1978].

If the output signal is taken directly from the oscillator, the loop functions as a frequency multiplier. It should be noted that for fixed and frequency-channel synthesis, the input noise power density on the phase detector input is multiplied by N. Under conditions of high multiplication factors, the input signal should have very low phase noise to obtain a good spectral purity of the output signal.

II.1.D Time and frequency responses

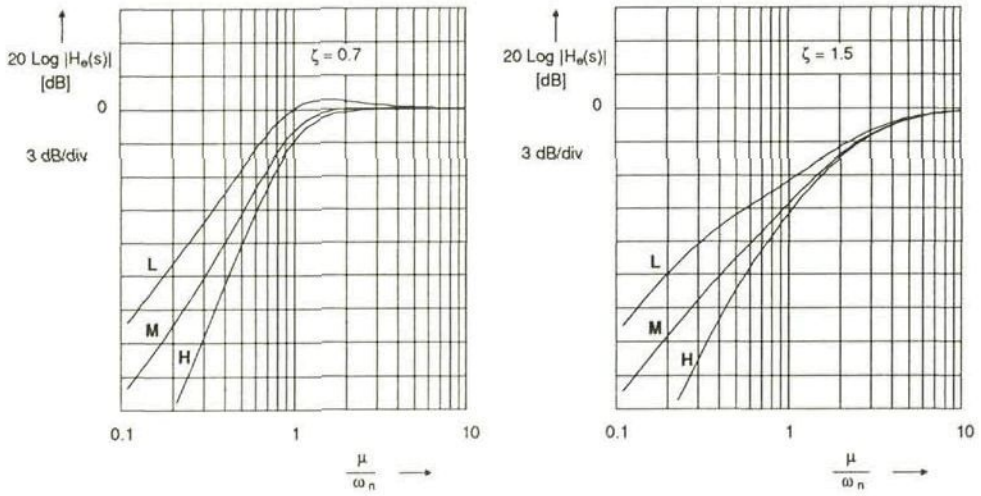
From the loop filter considerations and the I/O combinations in particular a classification of (linear) frequency and time responses can be derived, providing an insight into design objectives such as settling time. Contrary to what is done in literature, our purpose is to have distinct responses of different loop filter configurations.

Figs. 2.9 to 2.13 show different responses for low (L), medium (M), and high gain (H) conditions of passive filter loops, with ω_n/K_oK_d = 1, 1/2, and 1/10, respectively. Fig. 2.14 shows the differences between high-gain passive filter loops (H) and active filter loops (A).



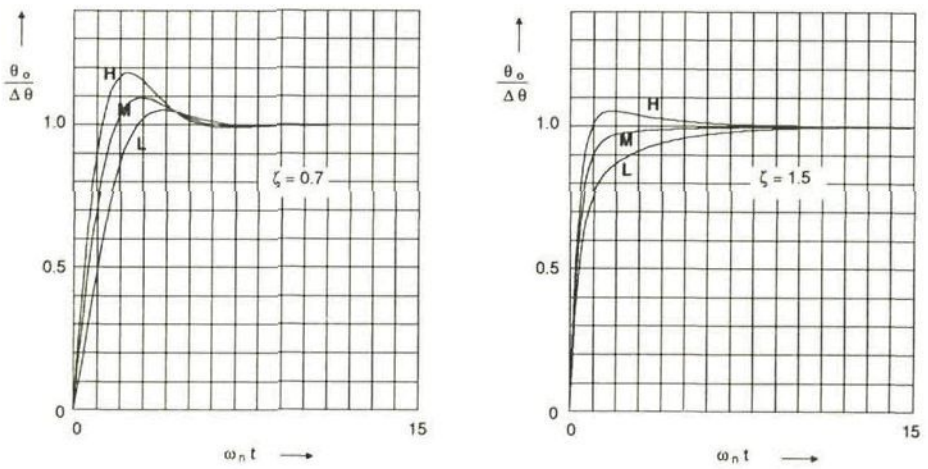
a) *b)*

Fig. 2.9 Normalized Bode plots H(s) (μ is the modulation frequency)



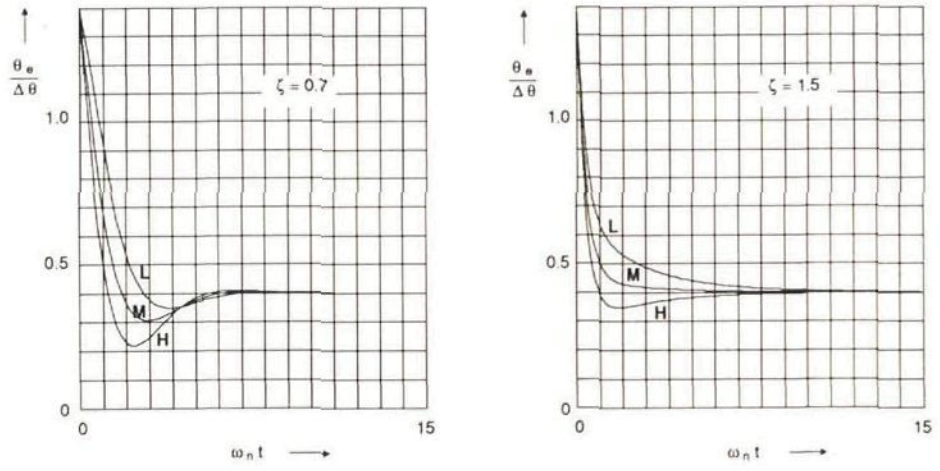
a) *b)*

Fig. 2.10 Normalized Bode plots $H_e(s)$



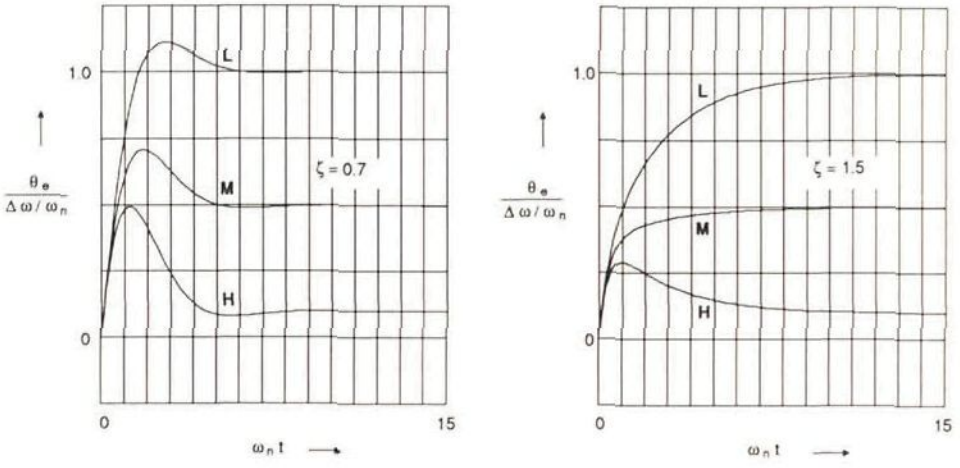
a) *b)*

Fig. 2.11 Normalized time responses θ_o on phase step



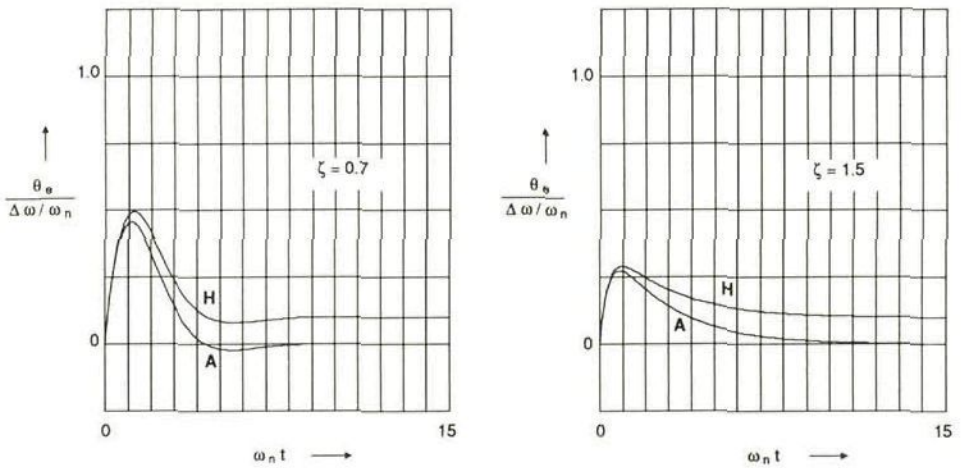
a) *b)*

Fig. 2.12 Normalized time responses θ_e on phase step



a) *b)*

Fig.2.13 *Normalized time responses θ_e on frequency step low, medium and high gain passive filter loops*



a) *b)*

Fig. 2.14 Normalized time responses θ_e *on frequency step high-gain passive (H) and active filter loops (A).*

II.1.E Linear design conclusions

Considering loop filter topologies led to different dynamic properties and transfer functions. Passive loop filters forced the control bandwidth to be smaller than K_oK_d, and active loop filters showed a great flexibility in determining the dynamic behavior. Complete conditions were given for the 'high-gain' approximation of passive filter loops.

Classification on the basis of the I/O configuration led to 16 applications nine of which were taken into consideration. The introduced PLL Frequency Model turned out to be useful in examining modulation and demodulation applications. Moreover, this PLL Frequency Model revealed a practical design limit of PLL's unknown in literature. The frequency-channel synthesis application was considered as a time-varying network.

After a step change in phase no steady-state phase error remained. From the PLL frequency model was derived that a step change of frequency left no steady-state frequency error. The steady-state phase error after a step change of frequency, however, depended on the DC loop gain. Neither phase nor frequency deviation limits could derived by linear analysis because it considered the PLL to be in lock under any condition.

II.2 NON LINEAR ANALYSIS

The linear analysis always has a PLL in lock. This cannot be correct, because it implies that any value of the phase difference is represented by a specific value of the phase detector output voltage. In any real system the output quantity is limited to a certain range of values, so phase detection must be non-linear. The analysis from the designer's point of view has to be extended with the non-linear region.

A significant characteristic of non-linear systems is their changing dynamic behavior at different magnitudes of the input quantity. For PLL's this is the phase of the input signal, which is compared to the phase of the locally generated signal. This phase angle difference may have a considerable magnitude.

This characteristic of PLL's is the source of limitations of the operating ranges of the PLL, which will be treated as a function of phase detectors and loop filters. The non-linearity causes further certain limits under conditions of additive input noise, and implies the generation of unwanted signals and departures from the 'continuous-time approach' followed so far.

II.2.A Phase detection

Angle and phase are relative quantities. The phase of a sinusoidal signal can be visualized by means of the angular position of a rotating vector. If the vector rotates with a constant speed ω_1, the angle as a function of time may be expressed as $\theta_1(t) = \omega_1.t + \theta_1(0)$, in which $\theta_1(0)$ is the position of the vector for t=0, related to a reference axis. If another vector rotates with ω_2, this angle is expressed as $\theta_2(t) = \omega_2.t + \theta_2(0)$.

In electrical measurements the projection of these vectors is represented on a reference axis as being a signal. This implies that the angle is non-linearly converted by means of a sine or cosine. To determine the angle, the length of the vector must be known, i.e. the amplitude of the sinusoidal signal should be measured.

Generation of a phase difference signal can be performed by multiplying two projected signals. If two projections on the same reference

axis are multiplied, two cosine functions will be generated, with arguments of the angular sum and the angular difference respectively:

$$\cos[\theta_1(t)]\cos[\theta_2(t)] = 1/2\ \cos[\theta_1(t)-\theta_2(t)] + 1/2\ \cos[\theta_1(t)+\theta_2(t)].$$

These are even functions, so the sign of the phase difference is missing. To determine phase difference we must know the magnitude and the sign. If projections on perpendicular axis are multiplied, the required phase difference function can be obtained:

$$\sin[\theta_1(t)]\cos[\theta_2(t)] = 1/2\ \sin[\theta_1(t)-\theta_2(t)] + 1/2\ \sin[\theta_1(t)+\theta_2(t)].$$

It should be noted that the method of using the projections of a vector on a reference axis implies a periodical non-linearity. One cannot determine different cycles. The periodicity equals 2π.

Phase measurement is usually considered as angle measurement of signals with equal angular speed. The term phase difference is also used for two signals with unequal angular speeds. In this case phase difference has to be called *accumulated* phase difference. For signals with equal frequency, i.e. period time, the term phase difference will be applied. The mechanization of the phase measurement device should be called phase comparison circuit. The name *phase detector* will still be used throughout, because of its widespread usage.

Phase detector transfer function: In Fig. 2.15 the functional block diagram of a phase detector is shown. In the case of phase-lock, the output quantity, for example the output voltage, is intended to be independent of the amplitude V_x and frequency ω_x of the input signals.

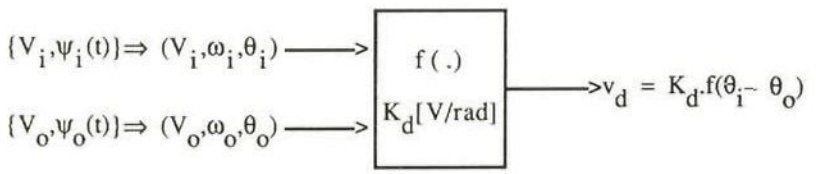


Fig. 2.15 Functional phase detector model

In general the output voltage v_d is a function $f(\theta_e) = f(\theta_i - \theta_o)$, multiplied by a conversion constant K_d.

The PD model of the linear analysis was $v_d = K_d.\theta_e$ for $-\infty < \theta_e < +\infty$, independent of input amplitudes and frequencies. Due to circuit limitations, this model could not be further employed in this form.

Any phase detector circuit implementation yields a *maximum* output voltage $v_{d,max}$, or a maximum output current $i_{d,max}$, and has a maximum phase error range $\theta_{e,max}$.

The combination seems to imply a maximum conversion factor $K_{d,max} = \dfrac{v_{d,max}}{\theta_{e,max}}$

If we define K_d as $\left.\dfrac{\partial v_d}{\partial \theta_e}\right|_{\theta_e=0}$, and consider $v_{d,max} = V_d$ and a linear phase error range of $\theta_{e,lin}$, then a maximum obtainable phase detector conversion factor[†] is $K_{d,max} = \dfrac{V_d}{\theta_{e,lin}}$.

All combinations within a maximum phase range and below a maximum output voltage have been considered in literature. It depends on the application which phase detector characteristic is constructed. E.g. for frequency synthesis a very high transfer factor (typ. 3000V/cycle) is employed by Clark/Underhill.

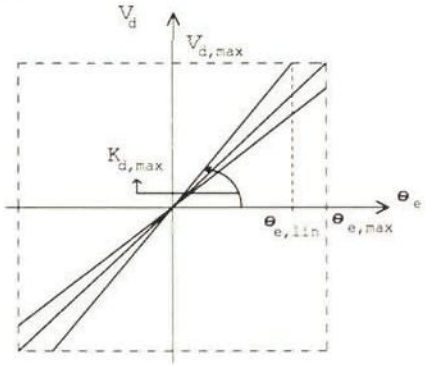


Fig.2.16 Phase detector output constraints

The phase detector output voltage v_d is mostly a baseband function;

[†] *Unless stated otherwise, quantities such as V_d and θ_e are considered to be peak values, i.e. single-sided quantities such as amplitude.*

this means that the signal is averaged. The circuit implementation of an averaging filter requires a lower limit of the input frequency. There also is a maximum input frequency, due to the finite gain-bandwidth product of the phase detector circuit. When the phase detector works in the area where these operational restrictions are satisfied, the phase detector transfer characteristic still forms a non-linear element in the PLL. This is a very important factor for the design.

Phase detector implementation: In order to get design information with respect to the non-linearity, the standard phase detector implementations will be reviewed. On the basis of the waveforms of the input signals, the operating principles will be described and the transfer factors K_d will be derived from the transfer functions obtained.

Analog implementations: If both input signals of the phase detector are sinusoidal, two phase detector implementation can be realized:

- vector multiplier v_d = mean(S1.S2)

The signal $V_i\sin(\omega_i t+\phi_i)$ multiplied by $V_o\cos(\omega_o t+\phi_o)$ yields

$$v_d(t) = \frac{V_i V_o}{2}\left[\sin((\omega_i+\omega_o)t+\phi_i+\phi_o) + \sin((\omega_i-\omega_o)t+\phi_i-\phi_o)\right].$$

The sum term $\omega_i+\omega_o$ is assumed to be attenuated in the loop filter. If K_m is the gain constant of the multiplier circuit, the phase detector transfer factor is: $K_d = \frac{V_i V_o K_m}{2}$.

- vector sum/difference: S1+S2 = Σ, S1-S2 = Δ, v_d = abs(Σ)-abs(Δ)

The operating principle [Gardner,1966] is based on the vectorial addition (Σ) and subtraction (Δ) of two sinusoidal signals $v_i=V_i\sin\omega t$ and $v_o=V_o\cos(\omega t+\theta)$.

From a vector diagram and according to the law of cosines it follows:

$\Sigma^2=V_i^2+ V_o^2+ 2V_i V_o\sin\theta$ and $\Delta^2=V_i^2+ V_o^2- 2V_i V_o\sin\theta$

$\Sigma^2 - \Delta^2 = 4V_i V_o\sin\theta$

The phase detector output signal is equal to the difference of the two

rectified signals $v_d = \Sigma - \Delta = \dfrac{4V_i V_o \sin\theta}{\Sigma + \Delta}$.

If $V_o \gg V_i$, then $\Sigma+\Delta \approx V_o$ and $v_d \approx 4V_i \sin\theta$.

Both implementations yield a sinusoidal transfer characteristic and can be represented by a *sinusoidal* non-linearity.

Switching implementations: If one or both input signals of the phase detector have a block waveform, phase detector operation implies a switching action. In some cases, the switching action requires a system description in the discontinue-time domain. We restrict ourselves at this instant first to the non-linearity of phase detector implementations which permit at least one input signal having a block form. A distinction will be made between multiplicative and sequential phase detectors.

□ sine multiplied by block

The signal $V_i\sin(\omega_i t+\phi_i)$ multiplied by $\mathrm{sgn}\left[V_o\cos(\omega_o t+\phi_o)\right]$,

in which $\mathrm{sgn}(x) = +1$ for $x>0$ and $\mathrm{sgn}(x) = -1$ for $x<0$, yields

$$\frac{2.V_i}{\pi}\left[\sin((\omega_i-\omega_o)t+\phi_i-\phi_o) + \sin((\omega_i+\omega_o)t+\phi_i+\phi_o) + \text{higher harmonics}\right]$$

The phase detector transfer factor $K_d = \dfrac{2.V_i}{\pi}$, the non-linearity is sinusoidal.

□ block multiplied by block

The signal $\mathrm{sgn}\left[V_i\sin(\omega_i t+\phi_i)\right]$ multiplied by $\mathrm{sgn}\left[V_o\cos(\omega_o t+\phi_o)\right]$ yields a complex expression. Each harmonic of the input, multiplied by the same harmonic of the oscillator, contributes to the averaged output signal[†]. If the frequency spectrum is the aim of the investigations, the expression

---

[†] *Strictly speaking, the definition of phase difference as an angle has to be revieved, because the relation between amplitude and phase of a sinusoidal waveform has been broken. Either positive or negative zero crossings can be used as reference points. In order to obtain some similarity with a sine, also the centers between the edges can be used as a reference point.*

must be written out completely. The electronic circuit to multiply two block forms is very simple, namely the XOR. A time-domain approach to characterize the non-linearity proves that, after averaging, the non-linearity has a *triangular* shape with a periodicity of 2π.

The transfer factor ‡ is $K_d = \frac{2V_d}{\pi}$.

□ edge-triggered

A time-domain approach to phase detection reveals an interesting possibility i.e. the set/reset flip-flop (SRFF), which has to be considered as a sequential phase detector. If we accept the duty cycle of a switched signal as a measure for the phase difference of two other signals, then the SRFF gives a linear phase transfer characteristic over 2π peak-to-peak phase error [Byrne, 1962]. The non-linearity is a *sawtooth.*

The transfer factor is $K_d = \frac{V_d}{\pi}$

The sequential Phase-and-Frequency Detector (PFD), implemented in PLL IC's, also yields a sawtooth-like shaped non-linearity.

The transfer factor is $K_d = \frac{V_d}{2\pi}$.

The operation of the PFD will be explained extensively in Chapter III.

Phase detector non-linearity: Conclusions from the above-described phase detector implementations yield three distinctions with respect to the non-linearities: sinusoidal, triangular, and sawtooth (*) . These non-linearities can be treated following an approach from the feedback and control theory. However, to obtain *design information* from this analysis, we have to deviate from the analysis given in literature.

A criterion must be chosen for the derivation of the design equations of the operating ranges. It is possible to normalize PD characteristics on having equal transfer factors K_d, which is illustrated in Fig. 2.17.

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‡ *The quantity $2V_d$ is equal to the logic swing of the used digital circuit.*

(*) *Bang-bang non-linearity has been left out of consideration, because it is not applied in integrated PLL circuits separately.*

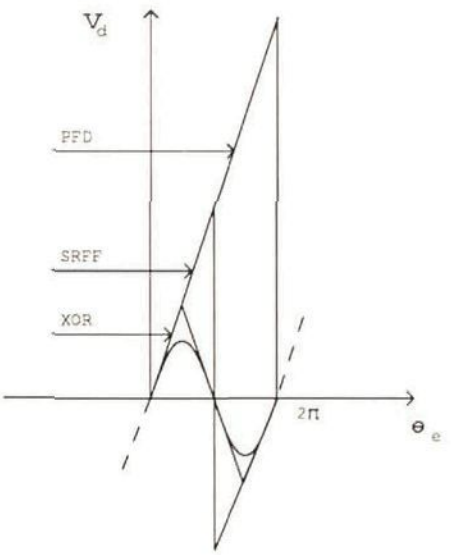

Fig. 2.17 Transfer functions of standard phase detectors, normalized to have equal K_d.

It seems to be more useful to refer to one of the fundamental limits of the system, namely the maximum output. From the discussion in the linear analysis section, we know that K_d is only one of the parameters such as K_o, τ_1, etc, determining the dynamic properties of the loop. Normalization for equal maximum output quantity leads to Fig. 2.18.

We see from this figure that the sinusoidal characteristic has the steepest slope, so the highest relative K_d, given a maximum output voltage. At this point, it would be tempting to conclude that the sinusoidal characteristic produces the best overall performance.

The design equations based on the normalization for equal maximum voltage will be described and the verification of this preliminary statement is postponed until more information is obtained.

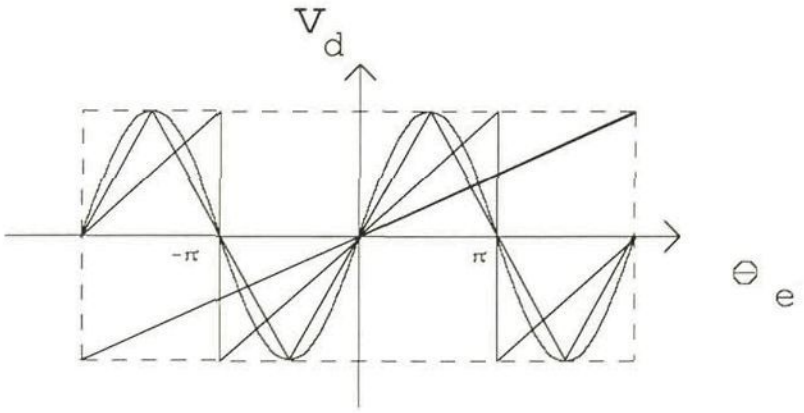

Fig. 2.18 Transfer functions of standard phase detectors, normalized to maximum output.

We proceed with the performance of common PLL's in terms of two loop filter configurations: active and passive loop filters for the commonly used second order PLL, and the standard I/O relation: input and output on the phase detector. The latter choice is permitted, because we have proved in the foregoing sections that the behavior of all other I/O topologies can be expressed in terms of H(s) and $H_e(s)$ of the basic model. This implies that in case of a division factor N >1 the output is taken from the divider output.

II.2.B PLL operating ranges

Because of the limited output range of the phase detector and the *limited phase error range, the PLL may be out of lock. For analysis* purposes several operating ranges are distinguished. Under the condition that the static phase error is equal to zero, the operating ranges of the PLL are defined as:

hold range, $\Delta\omega_H$, static operating range

This is the range of frequencies over which the loop will remain locked when the input frequency changes very slowly. A loop is considered to be

out of lock when the average output frequency is not equal to the average input frequency. The hold range expressions are only valid if the limits are caused by reaching the maximum permissible phase error range. For active filter loops the hold range is mostly determined by the maximum permissible control range of the frequency of the oscillator.

pull-out range, $\Delta\omega_{PO}$, maximum input frequency step while being in lock

The minimum step in frequency at the input, which causes a locked loop to loose lock, is called pull-out range. This is determined by the maximum of the phase error response and the maximum permissible phase error range of the phase detector.

direct lock range, $\Delta\omega_L$, maximum frequency difference for entering phase-lock within one cycle ; T_L is lock time

This is the frequency range over which an unlocked loop can acquire lock without cycle slip. The time to acquire lock is called lock time and is determined by the time constant that is relevant to the control speed of the loop. Obviously, this time is related to the common term 'settling time' from control theory.

pull-in range, $\Delta\omega_P$, maximum frequency difference for coming once into phase-lock; T_P is pull-in time

The frequency range over which the PLL can acquire lock. This range which is determined by the operation of the PLL as a frequency detector, is usually proportional to the tracking bandwidth. This means that the design requirements can be in conflict with each other. The acquisition time is called the pull-in time T_P.

From the specification of the small-signal dynamic properties, the designer has to optimize simultaneously two or more of the following design aims mentioned so far: static phase error; noise bandwidth; settling time; hold range; lock range; pull-in range; pull-in time, under various input and output signal conditions. Design expressions will be presented in the following for the various operating ranges.

For verification of the design, measurements in this area are very extensive, owing to the number of parameters that influence the PLL

performance. In Chapter VI, section VI.1, a method is given that quickly displays some operating ranges of phase-lock loops and related circuitry under various input conditions.

II.2.C Basic design equations for PLL ic's

From the analysis of phase detection one can conclude that phase detection is a non-linear operation and the shape of the non-linearity can be chosen by the designer. We will restrict ourselves to the non-linearities typical for integrated circuits. For multiplicative phase detectors these non-linearities are either:

- *sinusoidal* (at least one signal is SINE) or
- *triangular* (XOR).

Sawtooth non linearities occur in integrated circuits with a sequential phase detector (SRFF, PFD).

The design equations have been obtained partly by simulation and partly by analysis. These have been compared with those found in publications and handbooks. It should be noted that the *design* equations are not always properly described in literature.†

The linear design formulas for the second-order PLL with a passive ($\tau_2 > 0$) and an active loop filter have been summarized below.

---

† *In an, on the whole, very good textbook [Best, 1984], the formulas contain errors in at least ten cases; four formulas are missing, four formulas contain essential errors, and two cases are described incompletely and can be expressed in a simpler way.*

Parameter	Formulas	
	active	passive
ω_n	$\left[\frac{K_o.K_d}{N\ .\ \tau_1}\right]^{1/2}$	$\left[\frac{K_o.K_d}{N\ .\ (\tau_1+\tau_2)}\right]^{1/2}$
ω_{0dB}	$\frac{K_o K_d \tau_2}{N\ .\ \tau_1}$	$\frac{K_o K_d \tau_2}{N\ .\ (\tau_1+\tau_2)}$
ζ	$\frac{\omega_n \tau_2}{2}$	$\frac{\omega_n}{2}\left[\tau_2+\frac{N}{K_o K_d}\right]$
ω_{-3dB}	$\omega_n\sqrt{1+2\zeta^2+\sqrt{(1+2\zeta^2)^2+1}}$	see note*

settling time: $t_{5\%} \approx \frac{3}{\zeta\omega_n}$ $\quad \zeta<1$

overshoot in % : $\exp\left[\frac{-\pi\zeta}{1-\zeta^2}\right]$ 100% $\quad \zeta<1$

The conditions for a loop with a passive filter featuring high-gain dynamic (small-signal) behavior are:

$$\frac{N.\omega_n}{2.\zeta} \ll K_o K_d \quad \text{and} \quad N\omega_n^{\ 2} \ll K_o K_d/\text{sec}$$

An active filter loop can never be equal to a passive filter loop that meets the above-mentioned 'high-gain' conditions. This follows from the design equations for the various operating ranges.

The following design equations have been normalized with respect to the input frequency or, in other words, the phase comparison frequency. A closer examination of the conversion of the phase detector signal for the PFD will be given in Chapter III.

---

* *Same expression, except the term* $1 + 2\zeta^2$ *must be replaced by the term* $1+2\zeta^2-(4\zeta-\omega_n/K_oK_d).\omega_n/K_oK_d$.

DESIGN FORMULAS

HOLD RANGE $\Delta\omega_H$: These results are obtained from the steady-state phase error for step changes of the input frequency. This operating range can also be bounded by the frequency control range $(\omega_{max} - \omega_{min})/2$ of the oscillator and by the maximum output voltage of an active loop filter.

	passive	active, F(0)=A (DC gain)
sine	$K_o K_d/N$	$K_o K_d F(0)/N$
exor	$\pi/2.K_o K_d/N$	$\pi/2.K_o K_d F(0)/N$
srff	$\pi K_o K_d/N$	$\pi K_o K_d F(0)/N$
pfd†	$2\pi K_o K_d/N$	$2\pi K_o K_d F(0)/N$

LOCK RANGE $\Delta\omega_L$: These results are derived analytically from the open-loop gain. The begin condition for phase error has been ignored. This may result into an approximate factor two increase of the lock time.

	passive	active
sine	$2\zeta\omega_n - \frac{N\omega_n^2}{K_o K_d}$	$2\zeta\omega_n$
exor	$\pi\zeta\omega_n - \frac{N\pi\omega_n^2}{2K_o K_d}$	$\pi\zeta\omega_n$
srff	$2\pi\zeta\omega_n - \frac{N\pi\omega_n^2}{K_o K_d}$	$2\pi\zeta\omega_n$
pfd	$4\pi\zeta\omega_n - 2\pi\frac{N\omega_n^2}{K_o K_d}$	$4\pi\zeta\omega_n$

Lock time $T_L = \frac{1}{\zeta\omega_n} \cdot \left[\text{function}\{\theta_e(0)\}\right] \approx \frac{1}{\zeta\omega_n}$

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† *These results hold for a voltage source output of the PFD, see also Chapter III*

PULL-IN RANGE $\Delta\omega_P$: These results have been derived by modification of the acquisition model from literature as to a sine-shaped phase detector. In the model it is assumed that a frequency difference causes a small DC voltage, the pull-in voltage, via modulation of the VCO. This voltage is then accumulated by the loop filter until the loop enters the lock range.

	passive	active
sine	$\sqrt{2}\sqrt{2\zeta\omega_n K_o K_d/N - N\omega_n^2}$	$2\sqrt{\zeta\omega_n K_o K_d F(0)/N}$
exor	$2\sqrt{2\zeta\omega_n K_o K_d/N - N\omega_n^2}$	$2\sqrt{2}\sqrt{\zeta\omega_n K_o K_d F(0)/N}$
srff	$2\sqrt{\pi}\sqrt{2\zeta\omega_n K_o K_d/N - N\omega_n^2}$	$2\sqrt{2\pi}\sqrt{\zeta\omega_n K_o K_d F(0)/N}$
pfd	$\pi K_o K_d/N + 2\sqrt{2\pi}\sqrt{2\zeta\omega_n K_o K_d/N - N\omega_n^2}$	$\pi K_o K_d F(0)/N + 4\sqrt{\pi}\sqrt{\zeta\omega_n K_o K_d F(0)/N}$

PULL-IN TIME T_P: These results are taken from section VI.4

sine $$T_P \approx \frac{\Delta\omega_o^2}{2\zeta\omega_n^3}$$

exor $$T_P \approx \frac{6}{\pi^2}\frac{\Delta\omega_o^2}{2\zeta\omega_n^3}$$

srff $$T_P \approx \frac{1.5}{\pi^2}\frac{\Delta\omega_o^2}{2\zeta\omega_n^3}$$

pfd $$T_P \approx \frac{\Delta\omega_o}{\pi\ \omega_n^2}$$

Discussion: For the derivation of the pull-in time, it is tacitly assumed, that the approximation holds: active filter ≈ passive, high loopgain. This was proved by Blanchard for passive filter loops with a sine-shaped phase detector characteristic [Blanchard, 1976]. No exact information for

passive filter loops with other phase detectors is known yet. Measurements of T_P are difficult.

To present a *maximum* T_P the quantity $\Delta\omega_o$ has to be examined carefully. It seems reasonable to choose this equal to $2\Delta\omega_P$. In practice $\Delta\omega_P$ will often be larger than $\Delta\omega_H$, because the frequency control range of the VCO will most likely be the maximum frequency range. If so, to calculate $T_{P,max}$, the maximum time a PLL needs to come into lock, the quantity $\Delta\omega_o$ must equal the total control range of the VCO divided by N.

PULL-OUT RANGE $\Delta\omega_{PO}$: The sine case is well known in literature, the exor result is based on extensive simulation results, and the results for the srff and pfd have been derived analytically from the phase error response on a step change in frequency. It is generally supposed that the results for loops with a passive filter can be approximated with those of active loop filters. No exact information with respect to $\Delta\omega_{PO}$ for passive filter loops is known yet.

sine	$\lvert\Delta\omega_{PO}\rvert \simeq 1.8\ \omega_n(\zeta + 1)$	$.5 < \zeta < 1.4$
exor	$\lvert\Delta\omega_{PO}\rvert \simeq .7\ \pi\omega_n(1.78\zeta + 1)$	$.3 < \zeta < 5$
srff	$\lvert\Delta\omega_{PO}\rvert \simeq \pi\omega_n(2\zeta + 1)$	$.3 < \zeta < 5$
pfd	$\lvert\Delta\omega_{PO}\rvert \simeq 2\pi\omega_n(2\zeta + 1)$	$.3 < \zeta < 5$

II.2.D Extended non linear analysis

The foregoing analysis resulted in design equations for the operating ranges of the PLL, expressed in terms of input frequencies of the phase detector. From the I/O aspects we cannot but conclude that the operating ranges must be examined for the specific functional relations. Moreover the non-linear model must be verified for the noise behavior; if there are limits for the operating ranges, this will also result in probable restrictions for the noise.

A phase detector not only causes a non-linearity in the loop in terms of the wanted time-invariant output signal, but also generates an unwanted AC signal (ripple), that may disturb the operation as obtained from the foregoing non-linear model. The disturbances must be further examined for switching and sampling consequences on loop behavior.

The presented design equations can only be applied if θ_i is the input and θ_o/N is the output , i.e. the PLL is used as a tracking filter. The (de)modulation and frequency synthesis applications from the I/O cross-tabulation chart, however, need more design information.

The linear model imposes restrictions on the modulating frequency μ. Due to the restricted phase error range of the phase detector that made the non-linear model necessary, there must also be limits for the phase deviation $\Delta\phi$ in case of angular modulation. This can be analyzed by examining the phase error θ_e.

For *demodulation* of phase steps (PSK) and frequency steps (FSK), we already know the limits:

- The *phase step* $\Delta\phi_i$ must in any case be smaller than the one-sided phase error range of the phase detector. For a sine, triangular and sawtooth PD characteristic this is equal to π. However, for linear response of the triangular PD, the phase step has to be $< \pi/2$ and the sinusoidal PD requires $\Delta\phi$ to be $\leq\approx \pi/4$ (10% error) or $\Delta\phi \leq\approx \pi/3$ (20% error)
- The *frequency step* $\Delta\omega_i$ must be smaller than the pull-out range $\Delta\omega_{PO}$ as stated before.
- The data rate must be lower than the response time of the loop. Any foregoing disturbance must be smoothed.
- These limits hold for any divider factor N in the loop.

To determine the operation limits of the non-linear model for demodulation of *sinusoidal angular modulation* we must examine the sinusoidal frequency response of the phase error.

- For demodulation of PM modulated signals (with fixed phase deviation $\Delta\phi$) we already know the phase error versus modulation frequency characteristic $H_e(s)$. The phase error is equal to the input phase deviation of the modulation frequency $\mu \gg \omega_n$. So for the phase deviation the same limits are valid as for PSK demodulation.
- *For demodulation of FM modulated signals (with fixed frequency deviation* $\Delta\omega$) the loop must follow the momentary input frequency. The phase deviation $\Delta\phi$ decreases inversely proportional with the modulation frequency μ, while the phase error increases until $\mu = \omega_n$ is reached. Then the

transfer factor $\theta_e/\Delta\phi \approx 1$. The phase error is maximum for $\mu = \omega_n$ and has a peak amplitude of approximately $\Delta\omega/2\zeta\omega_n$ [Gardner, 1979, p.52]. So we can derive the design restriction of a loop with ω_n for staying in lock:

$$\frac{\Delta\omega}{2\zeta(\mu_{max}=\omega_n)} < \text{phase error limits given above.}$$

- These limits hold for any divider factor N in the loop, because the factor N is incorporated in the loop expressions for ω_n and ζ.

However, this does not hold for the *angle modulator* in which the output signal is taken directly from the oscillator. In the following we will assume that the divider in the loop has a value $N > 1$. Restrictions equivalent to those for demodulation can be derived for angle *modulation*:

- PSK modulation step has to be smaller than the phase error range of the phase detector *multiplied* by N. No real phase steps can be realized due to the limited response time of the loop.

- FSK modulation steps $\Delta\omega$ must be smaller than the pull-out range multiplied by N : $\Delta\omega < N.\Delta\omega_{PO}$

- PM sinusoidal modulation peak phase deviation $\Delta\phi$ must be smaller than the phase error range multiplied by N for modulating frequencies $\mu \ll \omega_n$. The main distortion source will most likely be the non-linearity of the phase detector transfer characteristic.

- FM sinusoidal modulation peak frequency deviation $\Delta\omega$ for modulating frequencies $\mu \gg \omega_n$ produces a peak phase error of $\Delta\omega/2\zeta\mu_{min}$. This must be smaller than the phase error range of the phase detector multiplied by N. We can also use this expression for determining the distortion of the FM modulation for a sinusoidal PD characteristic, because the error between a sine and a straight line can be noticed. Nevertheless the main distortion source for FM modulation is most likely due to the non-linearity of the K_o of the oscillator. This can be seen by examining the expressions of the linear PLL phase model. The spectral components of the distorted FM fall far beyond the loop bandwidth and can be neglected for the loop operation.

The above-mentioned design limitations have been deduced from the non-linear model with the help of the limited phase error range of the

phase detector. It will follow that this argument is very tricky if applied to noise disturbances.

Noise: Noise behavior is often considered to be as caused by the addition of several random input disturbances (such as phase steps, frequency steps, etc). However, the out-of-lock approach from excessive input noise is not the right way. Instead, going out-of-lock is mainly caused by the phase fluctuations or output-phase-noise of the *local oscillator*. Here we will investigate the basic question: "How a PLL is unlocked by noise?". As a result we will obtain quantitative answers that show a good correspondence with literature in this respect design limitations will be clear.

Narrowband, additive, gaussian, white noise: In order to found the used notations a brief description is given of noise properties.

The 'noise bandwidth' B_N of a practical filter is the ideal bandwidth (infinite steep slopes) with equal power transfer, following the definition:

$$B_N = \int_0^\infty |H(j\omega)|^2 df \; / \; |H(j\omega_r)|^2, \text{ in which } \omega_r \text{ is a reference value.}$$

'Baseband' is defined as frequencies from 0 – B_i. The amplitude density is gaussian. If we consider a frequency ω_i, then the noise in a noise bandwidth of $2B_i$ can be described as 'narrowband' with the expression:

$$n_i(t) = n_s(t)\sin\omega_i t + n_c(t)\cos\omega_i t,$$

in which n_s and n_c are two independent baseband noise processes. If $n_i(t)$ has a uniform power density N_0 (white noise) over a noise bandwidth B_i, then both n_s and n_c have a uniform power density $2N_0$ over a bandwidth of $B_i/2$.

'Additive' means the vectorial addition of noise to a signal vector. If we depict noise as a vector, and we display just one vector, the noise vector generally rotates slower than the signal vector. The maximum rotation speed of the noise vector for the narrowband approach is twice the midband signal frequency ω_i.

The total noise 'power' P_N for a constant power density N_0 over a noise bandwidth B_i is equal to N_0B_i. For additive noise half of the power is

amplitude noise and the other half is *phase noise*, because we can decompose the noise vector into one vector parallel to the signal vector and one vector perpendicular. The perpendicular vector represents the phase noise. It is clear that there is a relation between Signal-to-Noise Ratio (SNR) and phase fluctuations due to noise. A momentary phase value can be deduced from the vectorial addition: $\phi = \arctan\{n_c/(V_i+n_s)\}$. For small RMS values of the noise with respect to the signal amplitude this can be a linear relationship.

Open loop model, noise transfer of a vector multiplier as PD: For determining the noise that the loop enters, we will examine the operation of a vector multiplier under conditions of input noise. This circuit multiplies the sum of the signal and noise at the input,

$$v_i(t) = V_i\sin(\omega_i t+\theta_i) + n_s(t)\sin\omega_i t + n_c(t)\cos\omega_i t$$

with a sinusoidal oscillator signal, assumed to be pure and clean,

$$v_o(t) = V_o\cos(\omega_o t+\theta_o).$$

Under the conditions $\omega_i = \omega_o$ and ignoring the double frequency terms, the output voltage becomes

$$v_d(t) = \frac{V_i V_o}{2}\sin(\theta_i - \theta_o) + \frac{V_i V_o}{2}\, n^*(t)$$

in which $n^*(t) = \frac{n_c(t)}{V_i}\cos\theta_o - \frac{n_s(t)}{V_i}\sin\theta_o$

We find that the signal term is the same as the one without noise, but now an additional noise term $(V_iV_o/2)n^*(t) = K_d n^*(t)$ is present. This term has a zero mean value (average value, DC value) and a spectral power density of N_0 / V_i^2 over $-B_i/2$ till $+B_i/2$, or, for positive frequencies $2N_0 / V_i^2$ over $0 - B_i/2$.

This noise term could be thought of as being caused by a low-frequency phase-modulation of the input signal by the process $n^*(t)$. The multiplier output would then be $v_d(t) = K_d \sin\left[\theta_i - \theta_o + n^*(t)\right]$. This is only equal to the derived expression as far as the approximation $\sin(x) \approx x$ holds. We have not used this approximation at all, so the noise transfer of the vector multiplier is linear with respect to the noise.

The output signal of the PD partly runs through the loop filter and modulates the VCO, i.e. performs a non-linear modulation operation. The oscillator signal in a closed loop cannot be considered pure and clean as we have assumed before. Another approach will be taken now, in which the PLL has been seen as a 'phase noise filter'. It will appear that this yields a quantitative explanation of unlocking by the noise.

Closed loop model, the PLL considered as a filter: We assume that the PLL is not sensitive for amplitude noise, but only for phase noise. The phase noise is thought of as the angular modulation of the input signal. This is valid for small values of the phase fluctuations. The PLL follows the low frequency components of this modulation and converts these to the output with a transfer factor $H(s) = 1$, and a bandwidth $2B_L$ (modulation). The output noise power (phase noise) would then be half N_0 times $2B_L$ equals N_0B_L. This would be identical to a normal filter. However, the PLL input phase noise power is normalized with respect to the input signal power P_s. The phase noise power output is equal to $N_0.B_L/P_s$. From modulation theory we know that the power in the sidebands is proportional to $\Delta\phi$ for small phase deviation. We can use the power expression to examine the magnitude of the output phase fluctuations. The RMS value of the output phase noise is equal to

$$\sigma = \sqrt{\frac{2N_0B_L}{V_i^2}} = \sqrt{\frac{1}{2SNR_L}}$$

In practice we can, dependent on the measurement conditions, successfully employ the approximation of a *quasi peak-to-peak value* of 6 times the RMS value. For gaussian noise 9973 of the 10^4 samples are in a range *of* -3σ *and* $+3\sigma$.

From investigations of the non-linear model we know that the meta-stable points of the phase detector's phase error range are situated 2π apart. Linearizing a sinusoidal phase detector characteristic means approximating $\sin\theta_e$ by θ_e for $-\pi/3 < \theta_e < \pi/3$. Looking at the phase of the oscillator signal (phase error ψ between the clean input signal component and the oscillator), yields that the linear approximation must fail for $\psi_{peak\text{-}peak} > 2\pi/3$.

Together with the above-mentioned quasi peak-to-peak value of gaussian noise this results in:

$$6\sqrt{1/2SNR_L} < 2\pi/3 \Rightarrow SNR_L > 4.1 \equiv 6.1 \text{ dB}.$$

If the input noise causes peak-to-peak phase variations of the oscillator larger than $2\pi/3$, the linear approximation fails, and an operation range under conditions with noise has been defined.
If we assume that the linear approximation holds for a range $-\pi/2 < \psi < \pi/2$, then

$$6\sqrt{1/2SNR_L} < \pi \Rightarrow SNR_L > 1.8 \equiv 2.6 \text{ dB}.$$

For the total range of $\psi_{p\text{-}p} = 2\pi$ the linear approximation is certainly not valid anymore, but the same derivation results in $SNR_L > 0.45 \equiv -3.4$ dB.

This approach yields important design information: If the loop noise bandwidth B_L is sufficiently small, the PLL would be in lock. The input bandwidth B_i seems to be of no influence, only the input noise power density N_0 determines, together with the loop noise bandwidth B_L, the out of lock behavior. However, in practice the input bandwidth does play a role.

It is stated [Gardner, 1979], that it is only possible to stay in lock for a ratio B_i/B_L smaller than approx. 10^2 to 10^3. He proposes to represent this property by a so called 'phase detector threshold'. In our opinion the influence of <u>all</u> loop components has to be considered, together with the maximum dynamic control range. Experiments show that for a carefully designed PLL a ratio $B_i/2B_L$ of $0.63.10^5$ avoids unlocking [VanderPlas, 1985]. This property is further discussed in section III.3.C.

As a part of the extended non-linear analysis, an elegant explanation was found for the unlock property of a PLL under conditions with input noise, which yielded a decisive answer for the designer. In another approach for the noise behavior, the value of the oscillator's signal term could be considered as a function of the effective phase modulation index. This will be left for future investigations. In order to obtain more information on the consequences of the non-ideal filtering of the phase detector's ripple term, in the following the standard phase detectors will

be examined, together with the standard loop filters.

Phase detector ripple suppression: Almost any phase detector generates an unwanted AC term (ripple) in addition to a wanted DC signal. It has been assumed continuously, that the AC signal would be suppressed in the loop filter. However, in practice the suppression cannot be perfect, so a part of the PD ripple is at the control input of the VCO and influences the VCO operation. To determine the consequences for design, the ripple signal has to be analyzed for the standard phase detectors of the non-linear model.
For a sinusoidal phase characteristic the sinusoidal ripple has an amplitude K_d and a frequency of $2\omega_i$.
For an XOR the 50% duty cycle block form ripple has a peak-peak amplitude $2V_D$ and a fundamental frequency of $2\omega_i$.
For a SRFF the 50% duty cycle block form ripple has a peak-peak amplitude $2V_D$ and a fundamental frequency of ω_i.
For a PFD the block form ripple has a peak-peak amplitude of V_D and a fundamental frequency of ω_i or a peak -peak value of $2V_D$ and a frequency $\omega_i/2$ (see also section III.1.B). This frequency and the duty cycle depend on *the the stability of the input signals.*
Because the amplitude of the first harmonic term of the ripple will cause the largest influence on the loop properties, only this term will be examined.

The ripple term which is transferred via the loop filter to the oscillator input is partly suppressed. For a first order loop it is clear that the full ripple signal modulates the VCO. However, from modulation theory we know that modulation is only useful for modulating frequencies that are smaller than the carrier frequency. The lower sideband frequency must be larger than zero. This therefore leads to a strongly distorted VCO signal. A real first order loop seems indeed to generate a distorted oscillator signal. An oscillator signal with frequency ω_i is distorted by 'modulating' with a ripple term with frequency $2\omega_i$ or ω_i.

When a topology is used with a divider in the loop, the frequency of the oscillator is equal to $N\omega_i$, so when $N > 2$, we may speak of unwanted modulation or 'spurious'. Moreover, a real first order loop without parasitic poles is rarely used, so the transfer factor of the loop filter

can be incorporated in our analysis. If we restrict ourselves to second order loops and N > 2, and take only the first harmonic term ω_R of the ripple into account, the control voltage can be expressed as:

passive amplitude of ripple term x $\tau_2/\tau_1+\tau_2$

active ripple amplitude x τ_2/τ_1

This must be multiplied by K_o and divided by the modulation frequency $\mu=\omega_i$ or $\mu=2\omega_i$, to obtain the modulation index m of the oscillator signal. This yields for $m \ll 1$, according to the Bessel function $J_1(m)$, an inversely proportional measure ($\approx 2/m$) for the carrier-to-spurious ratio (CSR).

This open-loop approach is correct because the feedback transfer of the spurious frequency components through the divider N is equal to zero. The angular modulation that causes the spurious is completely absorbed by the divider.

Under the condition, that $m < 0.5$ ($J_0(.5) = 0.938$ and $J_1(.5) = 0.242$), or in other words CSR > 12 dB, our calculations for the standard phase detector's ripple signals yield the following results:

Carrier-to-Spurious Ratio (CSR)

	active filter	passive filter
sinusoidal	$-20\log \frac{N\zeta\omega_n}{2\omega_i}$	$-20\log\left[\frac{N\zeta\omega_n}{2\omega_i} - \frac{N\omega_n^2}{4\omega_i K_o K_d}\right]$
exor	$-20\log \frac{N\zeta\omega_n}{\omega_i}$	$-20\log 2.\left[\frac{N\zeta\omega_n}{2\omega_i} - \frac{N\omega_n^2}{4\omega_i K_o K_d}\right]$
srff	$-20\log 4.\frac{N\zeta\omega_n}{\omega_i}$	$-20\log 8.\left[\frac{N\zeta\omega_n}{2\omega_i} - \frac{N\omega_n^2}{4\omega_i K_o K_d}\right]$

pfd $-20\log(2N\zeta\omega_n t_\delta)$ or $-20\log(4N\zeta\omega_n t_\delta)$ for $\omega_R = \omega_i/2$,

in which t_δ is the absolute pulse width of the control action.

Discussion: It is assumed that the phase-and-frequency detector controls the loop via a standard loop filter, which means that the so called Charge-Pump has not yet been considered. In Chapter III the impact of the Charge-Pump will be investigated. For the moment, the investigations show that the best CSR seems to be a result of the conventional voltage-source approach.

A charge-pump as a method to convert the phase detector signal to a signal for a special loop filter is based on the switching action of the phase detector. Therefore, the consequences of the switching action of the phase detector will be examined.

Switching effects, sampling: Until now the analysis is based on averaged-response, time-continuous operation of the loop. A lot of phase detectors however, have an implied switching action. There are features arising from the actual time-discontinuous operation that need attention. In nearly every case, the phase-lock loop operates on a sampled basis and not as a continuous-time circuit. A sampled system has more stability problems.

In [Gardner, 1980] an analysis is given of a PLL with phase-and-frequency detector as a sampled-data system. A final result is a stability limit for a second-order loop (expressed in continuous-time, perfect second-order loop quantities).

The second-order loop is only stable for $\frac{\omega_i}{\omega_n} > \pi\zeta + \pi\sqrt{\zeta^2+1}$, which means $\omega_i/\omega_n > 6$ for $\zeta = 0.7$.

The phase detector ripple nearly always shows switching actions. When we have a closer look at the real phase detector signal by examining the response on a voltage step, the second-order loop filter output voltage has a step of $V_d.\tau_2/\tau_1$. The frequency of the VCO follows the voltage steps, so there will be frequency deviations of $K_o V_d.\tau_2/\tau_1$. Any real VCO has a finite frequency range in which it can be tuned. If control voltages outside this range are applied, the VCO is unable to follow. The frequency jumps must remain within the allowable tuning range of the oscillator. As an extreme instance, the frequency jumps must not exceed the input frequency. This results in a limit condition:

$\frac{\omega_i}{\omega_n} > 4\pi\zeta$, which means $\omega_i/\omega_n > 9$ for $\zeta = 0.7$.

Because the control range of the oscillator is nearly always well within the range of 0 to $2\omega_i$, this condition is the actual restriction for any practical sampled second-order type-2 PLL. The frequency jumps cannot be accepted and additional filtering is often included to attenuate the ripple.

In [Underhill, 1980] a sampled-data analysis is given for the transient settling time of a PLL frequency synthesizer. The second-order type-2 loop is analyzed to obtain an optimal response. The final result is that the fastest sampled response can never be achieved in practice, due to saturation effects like those described above.

One should be aware of the fact that the continuous-time approximation is not valid if the loop bandwidth approaches the frequency ω_i of the input signal. In that case, the time-discontinuous or sampled nature of the loop must be described. From the linear analysis in section II.1, conditions were derived for the maximum ratio ω_n/ζ of a passive filter loop, being smaller than the loop gain $\omega_L = K_o K_d$. This will most likely be much smaller than the input frequency ω_i. From the designer's point of view the continuous-time description for an active filter loop can still be safely applied if the input frequency ω_i exceeds the PLL's open-loop unity-gain point $K_d K_o F(s)/s$ by factor 10 to 15.

II.3 DESIGN RESULTS, LIMITATIONS

Non-linear PLL analysis has provided additional insight into loop properties. The phase detector performance has been shown to be limited with respect to phase error range and/or output level. For passive and active filter loops employing standard phase detectors this leads to the determination of operating ranges and related time intervals to obtain lock. I/O considerations lead in turn to maximum phase deviation limitations for modulation and demodulation. Out-of-lock restrictions in the presence of input noise were explained and the carrier-to-spurious ratio

was derived for passive and active filter loops using standard phase detectors. A closer examination of the switching action of phase detectors led to restrictions on a continuous-time description.

An attempt at a preliminary, global hierarchy for the design requirements may now be made: Firstly the PLL should operate over a specified frequency range, so that the hold range becomes the first design objective; the highest and the lowest operating frequency having been chosen. Usually the limits for the control voltage are set by the voltages used in the system, and therefore the minimal oscillator transfer factor $K_{o,min}$ is fixed. For the transfer factor K_d there is a limited choice from among the standard phase detectors. The order of magnitude of the loop gain ω_L is then fixed. Secondly the PLL should have specific, dynamic, (small signal) properties for fulfilling conditions on noise bandwidth, settling time or modulation bandwidth. It should be noted that even these two simple design requirements can be conflicting. If a low settling time is required with consequently a high natural frequency of the loop, a passive filter loop must meet the condition $\omega_n/2\zeta \leq \omega_L$ In an active filter loop the continuous-time considerations lose validity when the input frequency ω_i becomes too low compared with ω_n.

From the linear and the non-linear analysis we can conclude that there are several cases, in which the designer has to choose and/or discuss for the realization of a useful PLL. The design step of calculations of the system parameters provides the information whether or not the requirements and system specifications are met.

If at this point of the design path the conclusion is reached that the specifications will not be met in a standard, single loop configuration, the designer must choose a new topology. He may consider other phase detectors, multi-detector loops, additional compensatory circuitry, etc. In the next chapter, design information is extracted by following another route through the material.

CHAPTER III PLL DESIGN

In the design analysis the block parameters were taken to be constant in the linear as well as in the non-linear analysis. We investigated topological aspects relative to loop filter and input/output. The transfer function of the loop was examined in order to obtain the dynamic behavior. In the case of a divider in the loop, the loop properties vary as a function of the division factor. The non-linear analysis demonstrated that phase detection in essence must be non-linear. The character of the non-linearity determines design equations for the operating ranges. Thus far the PLL has been analyzed, as being a 'black box'. The only out-of-loop consideration introduced, was the input filter bandwidth, for the case when the noise transfer design equation was presented. In addition, several assumptions for the standard phase detectors of PLL IC's, were made. For the phase detectors with triangular and sawtooth shaped transfer functions, it was assumed that the PLL was preceded by an out-of-loop band-limited amplitude (hard)limiter.

In this chapter we will continue this integral treatment and emphasize the basic choice a designer must make, i.e. improvement of a

single loop by considering other phase detectors, or application of new topology such as multi-detector loops, additional help circuitry, etc. Improvements of single loops will be examined and properties of multi-detector loops will be derived. It will become clear that these measures can be considered as single loops with special phase detector characteristic. However, the design information is still incomplete, and the path of step-by-step examination design questions seems to come to a dead end. In order to extend the design information, special approaches and solutions of specific design compromises will be presented. These fundamental compromises concern: tracking and acquisition limits, suppression of spurious signals and switching-speed limits and noise limitations.

III.1 SINGLE LOOP TOPOLOGY

Improving the single-loop properties for a more relaxed design and dimensioning procedure implies examining of the implementation of the loop components. To obtain a suitable transfer characteristic, it may be possible to modify the implementation of the loop filter, the phase detector or the VCO. A modification of the VCO transfer function can only be of help if some form of feed forward control is possible. The implementation of special (non-linear) loop filters is beyond the scope of this work and therefore restrictions have been made to the phase detector implementation in a single loop.

III.1.A Phase detector improvement

There are two ways to modify the phase detector transfer characteristic (see also section II.2.A):

- increasing the transfer factor and consequently shrinking the usable phase range, or
- extending the phase range and consequently decreasing the transfer factor.

Which of the two methods is preferable depends on the input/output topology.

Increasing the transfer factor K_d is advantageous in frequency synthesis applications, if it possible to decrease the ratio with respect to the ripple amplitude (K_d/V_R) simultaneously. Then the Carrier-to-Spurious Ratio can become higher than predicted with standard PD's from the fore-

going analysis in section II.2.D. A sample-and-hold circuit combines this requirements.

Sampling PLL: The introduction of a sample-and-hold circuit as a phase detector can improve the performance of a PLL considerably.

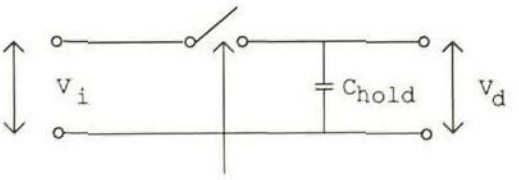


Fig. 3.1. Diagram of Sample-and-Hold (SH-PD)

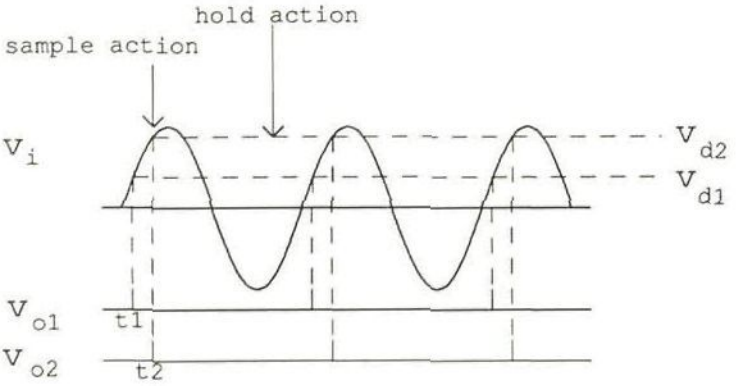


Fig. 3.2. Waveforms of SH-PD

The figures illustrate that the output signal of the phase detector is a DC control signal without any ripple term. Moreover, the sample-and-hold phase detector can also be employed for harmonic locking. Whether one or more periods of the input waveforms are not sampled is not important for the generation of a measure for the phase. However, the phase information is only available at the sampling instants. This must be modeled in a delay T_s. The phase transfer characteristic has the same shape as the input waveform and its properties can be summarized as follows:

- transfer function modifications can be obtained,
- phase detector ripple can be low,
- input frequency multiplication loop; sampling by input signal
- input frequency division loop; sampling by VCO signal

Although a trade off is possible between phase range and transfer factor, the phase error characteristic is still periodical, so the phase range cannot be more than 2π.

In practice, the properties are determined by the so called sample efficiency, i.e. the imperfect operation due to the charging time constant of the hold capacitor. This is modeled by an additional phase shift in the loop, that causes a lower phase margin and a decrease of loop stability. Low-ripple realization is only possible by means of a careful circuit design. Reduction of the feed-through, droop, blow-by, etc., due to the parasitic elements of the sample-switch device, is very difficult at high frequencies.

A phase detector circuit that also generates a low ripple term, is the phase-and-frequency detector (PFD). The design of a phase-and-frequency detector is much easier, because it is realized with digital circuits.

III.1.B Phase-and-Frequency Detector (PFD),

A special improvement of the phase detector of a single loop, is obtained by extending the principle of the SR flip-flop sequential phase detector which was described in II.2.A. If we combine two flip-flops we can extend the phase range from the original 2π to 4π. Furthermore, the circuit operates as a phase detector *and* as a frequency detector.

From the designer's point of view the latter property is advantageous to an improvement of the acquisition behavior. The frequency detector property will be illustrated by means of the special, non-periodical phase transfer characteristic.

The operation of the PFD: The operation of the PFD can be described from the hardware model as given in Fig. 3.3a.

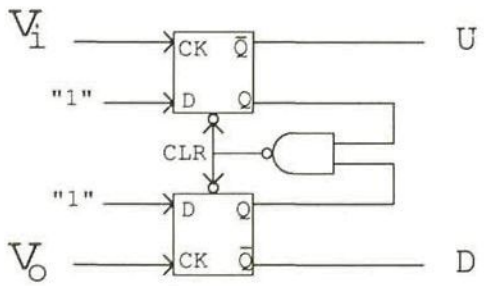


Fig. 3.3a. Positive edge-triggered PFD

In contrast to standard phase detectors the circuits have two outputs U and D. We find that both flip-flop outputs Q cannot be '1' at the same time. In this case the flip-flops are cleared and the circuit is in the (U,D) = (1,1) state. If the circuit is in the (0,1) state, the V_i signal leads. In the (1,0) state the V_o signal leads.

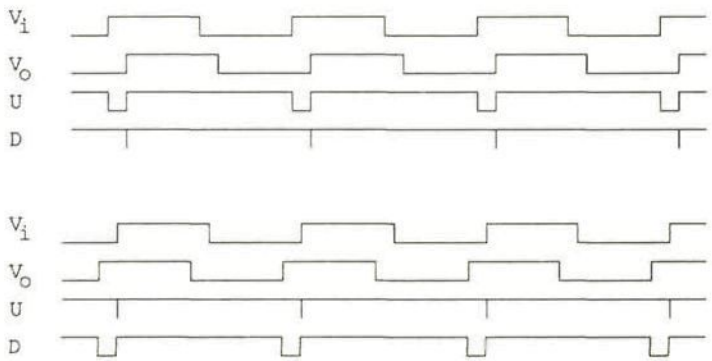
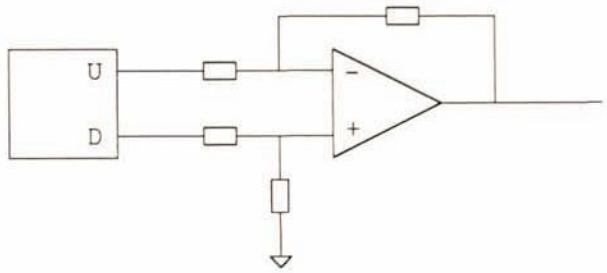
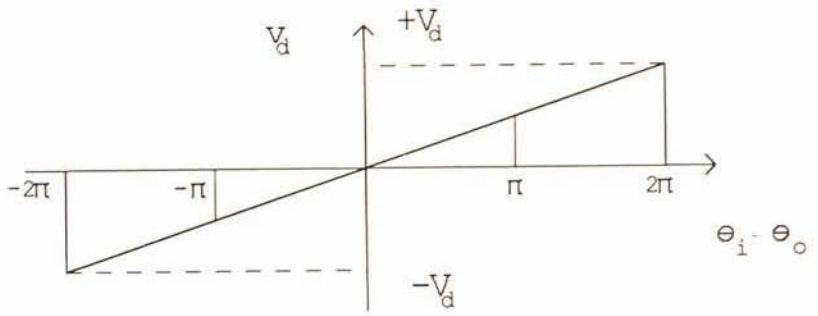


Fig. 3.3b. Time diagram of the input and output signals of the PFD

Combining the signals U and D by a subtracting amplifier as in Fig. 3.4.a, yields the transfer characteristic of Fig. 3.4.b.



(a)



(b)

Fig. 3.4. a) Combination of the two output signals of the PFD in a subtracting amplifier. b) Linear characteristic over phase range of 4π.

The characteristic is linear from -2π to $+2\pi$ with a special property around the equilibrium point. Contrary to standard phase detectors the output signal has a low duty cycle here, and only produces a small amount of phase detector ripple. The design equations of Chapter II can be applied, if the output of the phase detector is taken from the subtracting amplifier.

Charge-Pump concept: The two output terminals of the PFD can also be combined to form a so called Charge-Pump [Gardner, 1980] for converting the phase detector signal to a signal for the loop filter. In logical

design terms a Charge-Pump can be thought of as a three-state output stage for driving the loop filter. In Fig. 3.5 voltage source and current source charge-pumps are shown with passive and active loop filters.

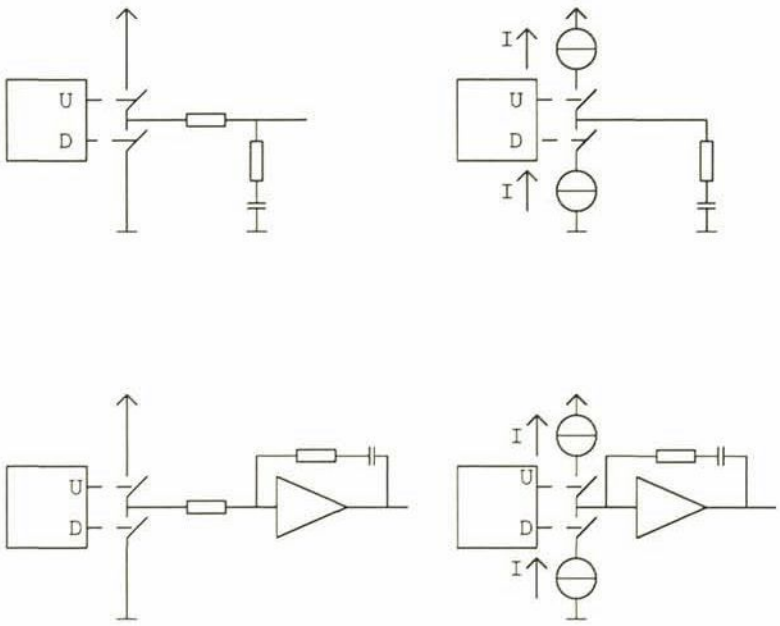


Fig. 3.5. Charge-Pumps

Frequency detector operation: The frequency detector operation becomes clear by analyzing the circuit for absolute phase differences larger than 2π. For phase measurement it is impossible to discover any difference in successive periods. Hence the periodical nature of the transfer characteristic for the standard phase detectors. In contrast, the PFD combines two transfer characteristics viz. the U output and the D output. Each of the separate characteristics looks like the original SR flip-flop characteristic. The combination yields a phase transfer characteristic as is shown in Fig. 3.6.

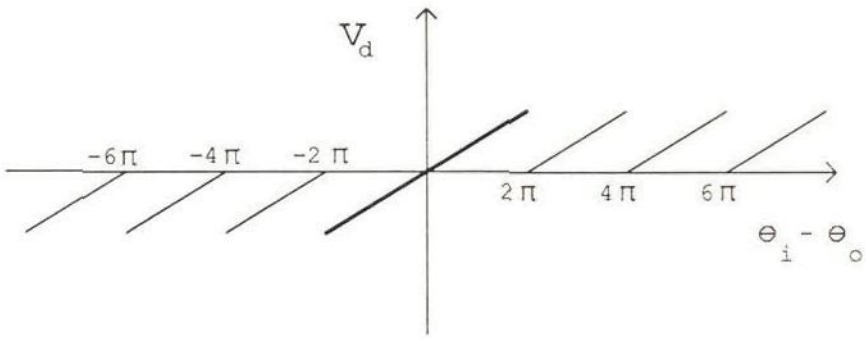


Fig. 3.6. Combination of SR-flip-flop characteristics.

The frequency detector operation can be illustrated with this characteristic, because a positive frequency difference equals an increasing accumulated phase difference:

If $\omega_i \neq \omega_o$, $v_i(t) = \sin\omega_i t$

and $v_o(t) = \sin(\omega_o t+\phi)$,

$v_o(t)$ can be rewritten as:

$$\sin\left[\omega_i t + (\omega_o - \omega_i)t + \phi\right].$$

According to the definition of frequency $\omega = d\phi/dt$, $\psi(t) = \int_0^t \omega(t)dt$, this can be expressed as:

$$v_o(t) = \sin\left[\omega_i t + \psi(t)\right], \text{ with}$$

$\psi(t) = \int_0^t (\omega_o - \omega_i)dt + \phi$ the accumulated phase difference.

For a *positive* frequency difference $\omega_i > \omega_o$ the phase difference runs through the positive part of the characteristic and the U output produces an average *positive* voltage. In Fig.3.7 the waveforms are drawn for a frequency ratio of 10/9.

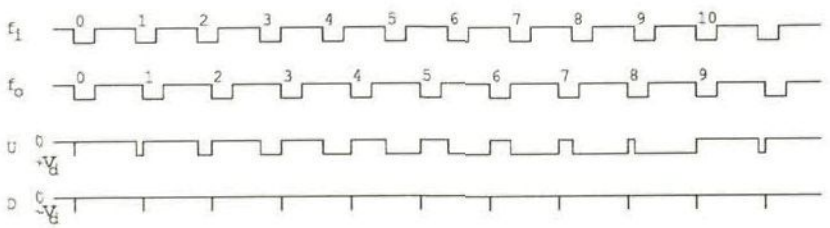


Fig. 3.7 Output signals of the PFD for a frequency ratio of 10/9.

It is clear that for a large frequency difference the average output voltage will be close to the positive voltage, because the PFD is seldom set to the neutral state; for a small frequency difference the average output voltage is close to half the positive voltage.

It will now be shown that a rough approximation of the frequency detector transfer factor, contrary to literature, yields:

$K_f \approx \dfrac{V_D}{2\omega_e}$ for $\dfrac{|\omega_e|}{\omega_i} \ll 1$ and $|\omega_e| \gg 0$, instead of $V_D/2\omega_i$[†] .

It was shown [H.Huisman, 1982] that the duty cycle of the U output must be expressed as: $\left[1 - \dfrac{\omega_o}{2\omega_i}\right]$ for $\omega_i > \omega_o$, and for the D output as: $-\left[1 - \dfrac{\omega_i}{2\omega_o}\right]$ for $\omega_i < \omega_o$. For a frequency difference $\omega_e \ll \omega_i$ and $\omega_e \ll \omega_o$, and $\omega_i \approx \omega_o$, the duty cycle can be approximated by $\dfrac{\omega_e}{\omega_i} + \dfrac{1}{2}$.

The average output voltage then is $V_D\left[\dfrac{\omega_e}{\omega_i} + \dfrac{1}{2}\right]$, which should be equal to $K_f\omega_e$, because it is a frequency detector. This yields the given expression for the transfer factor K_f.

[†] *Best, 1984, p.299*

The characteristic of Fig. 3.6 provides enough information to explain the operation as a frequency detector. This characteristic is, however, not complete. A phase error larger than 2π means that one active edge is ignored (see e.g. edge 10 of f_i in Fig. 3.7). The phase is again measured modulo 2π. The complete characteristic is shown in Fig. 3.8.

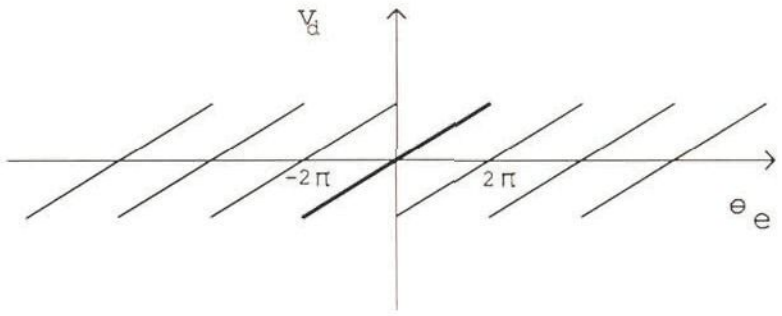


Fig. 3.8. Set of transfer characteristics of the PFD

There is not a one-to-one relation between the phase difference and the output voltage. The following cases can be distinguished:

- An increasing phase difference produces a positive voltage.
- A decreasing phase difference produces a negative voltage.
- The combination characteristic of the two SR flip-flops will be used after a change of sign of the time derivative of phase difference.

The latter is the phase detector characteristic and the first two cases describe the operation as a frequency detector.

The impact of the Charge-Pump: The two outputs of the PFD can be combined to form a Charge-Pump by two switches. The most important property of a Charge-Pump PLL (CPPLL) is that one can obtain properties of a PLL with *active* filter, while using only a passive loop filter.

This is an important *design conclusion*, because for the standard phase detectors the design concept assumes that loop filter and phase detector can be considered as independent elements. The linear approach assumes that only the loop filter and input/output considerations are of

main concern. In the non-linear approach only the non-linearity of the phase detection function determines the design equations for an active or passive filter. Here, the conversion of the phase detector signal to a signal for the loop filter determines the loop properties too.

Let us briefly review the steps in the design analysis for the Phase-and-Frequency Detector:

- Combination by means of a subtracting amplifier yields a 'standard' design; an active loop filter or a passive loop filter determines the performance as given in Chapter II.
- Phase detector ripple or spurious suppression is also predicted by the given formulas of Chapter II.
- Combination in a Charge-Pump and a passive filter almost yields a 'PLL with active filter' performance; there is some additional non-linearity depending on the locked frequency for a voltage charge-pump.

The prediction of the spurious in case of the charge-pump application is heavily circuit dependent. In Chapter VI, section VI.2 an analysis is given of the false-lock sources in charge-pump PLL's. False lock can occur due to the finite source impedance in the high-Z state, and due to the switch-off pulse width (clear action in Fig. 3.3) to come into the high-Z state. The pulse width is inversely proportional to the spurious suppression. Due to parasitic capacitance the pulse width can become considerably wider than the internal switch-off pulse. The prediction of the CSR by the given expressions is rather optimistic.

III.2 MULTI DETECTOR TOPOLOGY

It is possible to improve a single detector topology, but there are still combinations of desired properties, that cannot be realized with a single loop. Design problems appear for the required frequency acquisition time, the suppressed carrier in symmetric BPSK modulation and in PRNS-code, and for the information about the locked or unlocked state.
Applications in which these shortcomings are manifest are frequency synthesis, carrier-tracking of Binary Phase Shift Keying (BPSK) signals, and Pseudo-Random Noise Sequence (PRNS) code tracking in direct-sequence

spread-spectrum signals.

A phase detector that employs two quadrature versions of the input signal can yield a more reliable angle measurement. In some cases two versions of the locally generated waveform can be applied to enhance phase detection, but this requires a considerable amount of additional circuitry. The classical design problem arises: – What is the 'simplest' implementation that meets the specifications? – This sort of design problems will now be described. Then the performance of PLL's with these circuits will be compared to standard performance predicted by the design equations of Chapter II.

Before looking at multi-detector loops, we will illustrate the lock-detection problem. Although this can be solved with a multi-detector topology, a very simple digital lock-detection circuit is also adequate.

III.2.A Lock detection

An example of lock detection will be found when investigating the Phase-and-Frequency Detector more thoroughly. Lock detection and frequency-difference detection have some aspects in common. If the incoming frequency differs from the locally generated frequency, the PLL will definitely be out of lock.

In section III.1.B. a frequency difference was detected if the accumulated phase difference exceeded 2π. If two quadrature versions of the signal are available, another method for detecting a frequency difference is feasible, although its circuitry is more complex. This will be explained in section III.2.B. One has to distinguish circuits that detect the unlocked state and circuits that support auto-acquisition in the PLL.

A digital lock-detection circuit is described in section VI.3. This circuit can be used in combination with all known sequential phase detectors. The principle of operation is based on the detection of cycle slips, which is one of the possible out-of-lock definitions.

The purpose of lock detection is to indicate the validity of the output information and/or to give out-of-lock rate-information for changing e.g. the bandwidth of the PLL. Definitions of phase-lock and the related lock detection circuits are based on:

1) The time derivative $d\theta_e/dt$ and the noise bandwidth B_L; detectable by measuring the voltage across the 'zero' resistor R_2 in the loop filter,

2) The average value and the variance of the phase error; detectable by an extra quadrature phase detector, or

3) Cycle slips; detectable by observing the periodicity of the phase detector output signal.

Each of the definitions is used in different application areas.

The quality of lock detection is indicated by its reliability and its speed. The reliability depends on two probabilities: the probability of being in-lock, whereas the lock detector indicates out-of-lock; and the probability of being out-of-lock, the lock detector indicating in-lock. *The requirements for the speed of indication are strongly application-*specific.

A lock-detector circuit which can be applied in digital circuitry environment is found in the general purpose CMOS integrated circuit 4046. Pulses are derived from the output signals of a phase-and-frequency detector. They supply the information of the momentary positive and negative phase error in the form of a pulse width. Discrimination of the widths of the phase pulses does not give a reliable lock detection criterion. Besides, this method is strongly dependent on the input frequency and the static phase error of the loop. Of the definitions of phase-lock only some form of 2) is adequate in that case. The energy content of phase pulses is averaged by a filter and the resulting DC level is used by a Schmitt-trigger to give out-of-lock indication.

Fully digitally implemented lock detection can only be achieved by detecting cycle slips (CS) in the loop. The absence of cycle slips as definition of phase-lock is given by [Gardner, 1979, Ch.6]. The occurrence of cycle slips is an important phenomenon to determine the non-linear behavior of PLL's and can be easily implemented into general purpose PLL IC's.

Proposed lock detector circuits: In Fig. 3.9 the equivalent circuit (see also Chapter III.1.B) of a sequential PFD is given with the proposed digital circuitry to detect cycle slips easily.

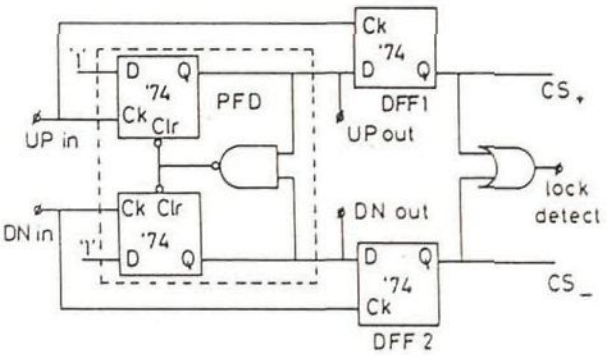


Fig. 3.9 Proposed circuit as an extension of a common phase-and-frequency detector

A cycle slip occurs when two successive active edges are applied to one of the two inputs of a sequential PD. In DFF1 the information about the positive cycle slip (CS_+) is present and DFF2 indicates a negative cycle slip (CS_-). The proposed circuit yields out-of-lock information that is independent of the static phase error. At the same time the output pulse width is never smaller than the period time of the input signal.

Discussion: The absence of cycle slips is used as the definition of phase-lock. This is a useful definition of phase-lock because cycle-slipping indicates that the PLL is sometimes out-of-lock and definitely gives a situation in which the common linear PLL model is not valid, provided that the input signal is not too noisy.

The statistics of cycle slip occurrence play an important role in determining the nearly unlocked, non-linear state of the PLL. To get exact unlock information the given method can be extended by cascading the cycle slip DFFs. The contents of the thus created up (CS_+) and down (CS_-) cycle slip registers tell about the synchronous state of the PLL.

In summary, the foregoing discussions illustrate the design problems with respect to cycle slips and noise, and acquisition and noise. The digital lock detection circuit employs phase detector signals that for

spurious suppression has been considered as unwanted. In a similar manner these subjects were treated in the non-linear analysis of section II.2.D. In order to obtain more design information, loops with more than one version of the oscillator signal will be examined. In many areas signal processing was done by means of two quadrature versions of the signal, based on the Hilbert transform from modulation theory. This approach may yield more insight in these problems.

III.2.B Quadrature loops

Phase-Lock Loops based on the Quadrature principle are characterized by the fact that two quadrature versions of the input signal, the oscillator signal or both signals are used in the loop. PLL's based on this principle can perform special functions.

In certain cases it is possible to operate from nearly zero input frequency and the undamped natural loop frequency can then be higher than the input frequency. Also the quadrature versions can be used to perform frequency difference functions and squaring functions. The possibility to operate on higher frequencies than the undamped angular loop frequency seems to be contradictory with the earlier determination of a practical design limit from the PLL Frequency Model. This will be explained at the end of this section.

Theory of Quadrature principle: The essential difference between Quadrature and conventional PLL's is the application of a two-phase input signal and/or a two-phase oscillator signal (sine and cosine versions). The block scheme of a full Quadrature PLL is shown in Fig. 3.10. Note that this principle can be extended for more phases [Baldwin, 1969]. The two-phase signals may have any waveform, but for a full advantage of this topology the signals have to be sinusoidal.

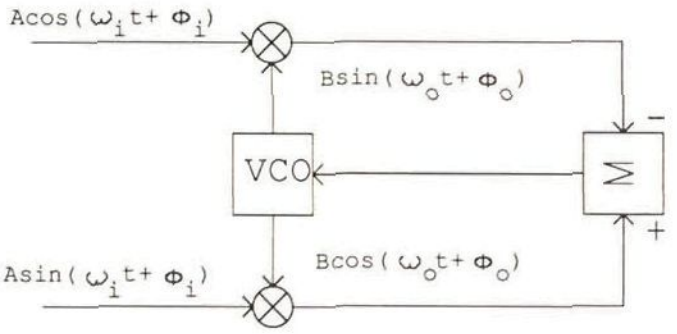


Fig.3.10 Full Quadrature Phase-Lock Loop.

The input signal version $A\cos(\omega_i t+\phi_i)$ multiplied by $B\sin(\omega_o t+\phi_o)$ yields $\frac{AB}{2}\left[\sin((\omega_i+\omega_o)t+\phi_i+\phi_o) - \sin((\omega_i-\omega_o)t+\phi_i-\phi_o)\right]$

$A\sin(\omega_i t+\phi_i)$ times $B\cos(\omega_o t+\phi_o)$ equals

$$\frac{AB}{2}\left[\sin((\omega_i+\omega_o)t+\phi_i+\phi_o) + \sin((\omega_i-\omega_o)t+\phi_i-\phi_o)\right]$$

Subtracting the two multiplication results gives

$$AB\sin((\omega_i-\omega_o)t+\phi_i-\phi_o).$$

This signal controls the oscillator.

When the loop is in lock then $\omega_i = \omega_o$ and the control signal will be $AB\sin(\phi_i-\phi_o)$. This DC signal is a measure for the phase difference. The double frequency term has disappeared in this topology. In a conventional single detector topology for attenuating this term a loop filter is needed.

Operation from $\omega_i >\approx 0$: For a single loop, the loop filter pole will certainly be at a lower frequency than $2\omega_i$. Also for an active loop filter

the pole can be close to zero, but it cannot be exactly zero.

In view of these considerations a conventional loop cannot operate from nearly zero frequency, because in that case the loop filter pole must be at zero, implying an infinite steep filter curve. Thanks to the subtraction a Quadrature loop, however, has no double frequency term and consequently does not need a loop filter.

Operation for $\omega_n > \omega_i$*:* As given in Chapter II the undamped natural loop frequency ω_n is determined by K_o, K_d and τ_1. To increase ω_n we can enlarge the factor K_oK_d by using an amplifier in the loop. However, as stated before, due to the phase detector ripple on a frequency of either ω_i or $2\omega_i$, the designer has to calculate the loop filter time constants in such a way that the ripple term does not enter the oscillator control input.

The operation of a single loop PLL requires that the undamped natural frequency is much lower than the double input frequency. Generally this aspect is not emphasized in literature. The linear (phase) model is mostly used, extended with any of the properties of the non-linear model. In the quadrature PLL the double frequency term is canceled out, so for sinusoidal signals the natural frequency ω_n can be chosen freely.

Overview Quadrature topologies: Here various types of PLL's and related circuits, based on the quadrature principle will be described. It should be mentioned that there are certainly more circuits, but generally they can be reduced to one of the topologies described here.

Standard Quadrature PLL: The standard Q-PLL can be implemented as in Fig. 3.10 above. The multipliers have to be of the vector multiplier type. The amplitude of the signals determines the 'phase detector' transfer factor. A real first order loop can be designed without a loop filter.

A loop filter can be placed before the control input of the oscillator to realize second or higher order loops. The loop can be used for very low frequencies and an ω_n can be chosen higher than the input frequency ω_i.

Quadrature PLL with vector sum/difference phase detectors: The standard topology can also be implemented as is shown in Fig. 3.11. [Kaplan, 1986]. The differences with the standard Q-PLL are:

The input signal version $\sin(\omega_i t+\phi_i)$ summed to $\sin(\omega_o t+\phi_o)$
gives $2\sin[((\omega_i+\omega_o)t+\phi_i+\phi_o)/2] \bullet \cos[((\omega_i-\omega_o)t+\phi_i-\phi_o)/2] = \Sigma_{sin}$

$\cos(\omega_i t+\phi_i)$ summed to $-\cos(\omega_o t+\phi_o)$ yields

$$2\sin[((\omega_i+\omega_o)t+\phi_i+\phi_o)/2] \bullet \sin[((\omega_i-\omega_o)t+\phi_i-\phi_o)/2] = \Delta_{cos}$$

If Δ_{cos} is divided by Σ_{sin} the signal $\tan\left[\frac{(\omega_i-\omega_o)t+\phi_i-\phi_o}{2}\right]$ remains.
If the loop is in lock this signal will be $\tan((\phi_i-\phi_o)/2)$.

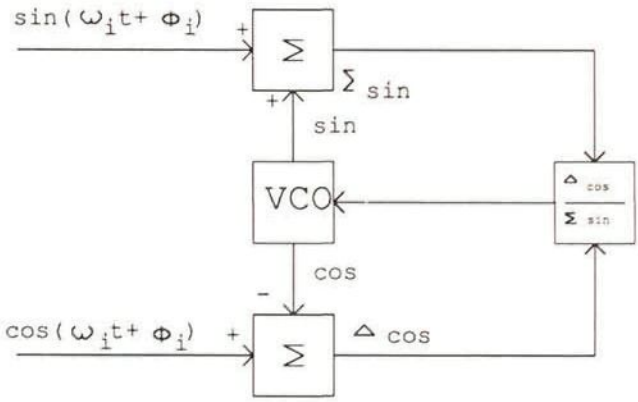


Fig. 3.11. Standard Q-PLL implementation with other blocks

Again the double frequency term is canceled out. The 'phase detector' characteristic is now tangentially shaped. For small phase errors the loop can be designed as a linear loop; however, for larger phase errors the derivative of the characteristic (K_d) increases. A larger 'momentary' K_d yields a faster response. This is just the opposite of the sinusoidal characteristic in which K_d decreases for larger phase errors. As described in II.2.D noise transfer will be non-linear.

A disadvantage of this topology is the fact that the amplitudes of

the input signal and the oscillator signal must be exactly equal. When the amplitudes are not equal there are additional terms which are not completely canceled out. This fact is not mentioned by Kaplan et al.

In practice it is difficult to cancel out the double frequency term. In this implementation the phase range is divided by two, compared with the standard quadrature loop. A similar shaped, non-linear phase transfer characteristic over a phase range of 4π, has been realized with digital circuitry (section III.3.A).

Frequency Translation Loop: The input frequency is not equal to the VCO frequency. There is a difference frequency signal, that is phase compared to a fixed-frequency local oscillator signal. A possible configuration [Gardner, 1979, p.204] is given in Fig. 3.12. This principle is used e.g. in communications for SSB demodulation. The non-quadrature version is called 'summing loop' in frequency synthesis and 'long loop' in phase-lock receivers.

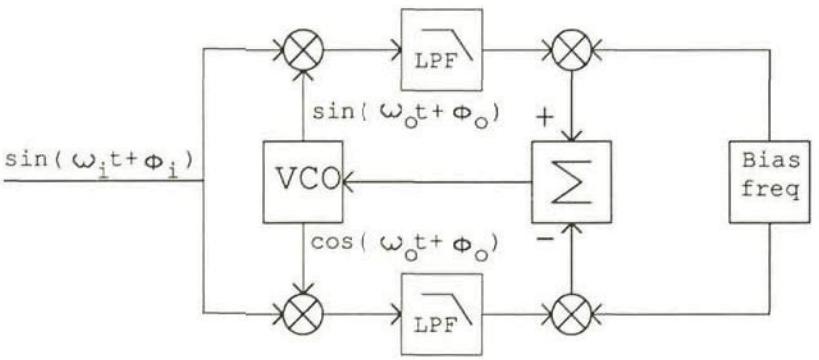


Fig. 3.12 Frequency Translation Loop

The diagram of Fig. 3.12 is only one of the possible configurations. A generalized block diagram is given in Fig. 3.13, in which the signal sources have not yet been called input, VCO, etc.

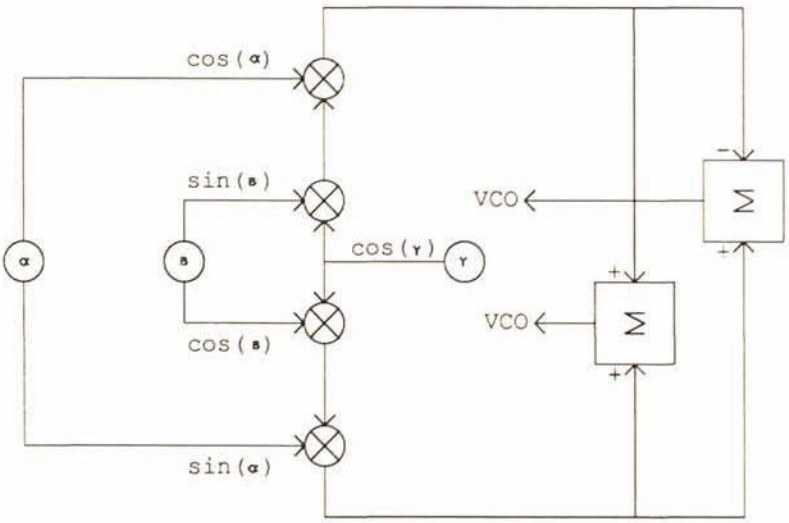


Fig. 3.13. Generalized block diagram

The diagram can also be drawn with the sin(α) and cos(α) signals exchanged [Hakkesteegt, 1987]. Then the scheme of Fig. 3.12 is obtained. PLL's operating from nearly zero frequency must have a two-phase very-low frequency source.

Another aspect can be derived from these topological models, namely that there have to be attenuated sum frequency components. It seems possible to choose ω_o much larger than ω_i, for realizing an ω_n higher than ω_i. In that case the difference frequency should be higher than the input frequency. The lowpass filter can then have a pole frequency higher than ω_i and ω_n. We will the be faced with the realization of sufficient attenuation of the sum frequency component

Costas PLL: The scheme of the original Costas PLL [Costas, 1956] is given in Fig. 3.14. The configuration shows resemblance to the topology of Fig. 3.12.

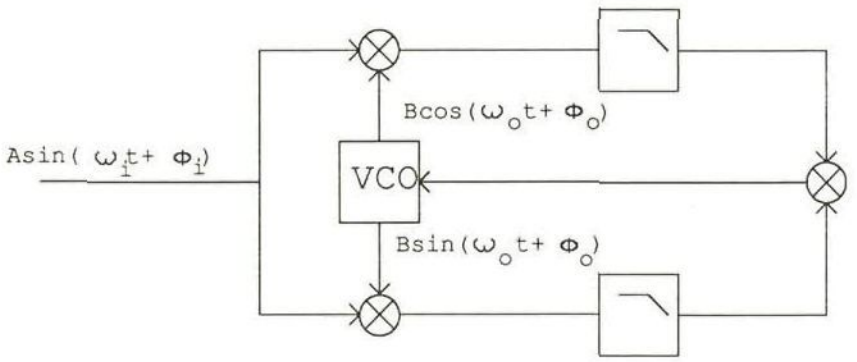


Fig. 3.14. Costas Phase-Lock Loop

The input signal $A\sin(\omega_i t+\phi_i)$ multiplied by $B\cos(\omega_o t+\phi_o)$ (upper arm)

yields $$\frac{AB}{2}\left[\sin((\omega_i+\omega_o)t+\phi_i+\phi_o) + \sin((\omega_i-\omega_o)t+\phi_i-\phi_o)\right]$$

Lowpass filtering removes the sum frequency term and gives the Q signal:

$$\frac{AB}{2}\sin((\omega_i-\omega_o)t+\phi_i-\phi_o)$$

$A\sin(\omega_i t+\phi_i)$ times $B\sin(\omega_o t+\phi_o)$ (lower arm) is:

$$\frac{AB}{2}\left[-\cos((\omega_i+\omega_o)t+\phi_i+\phi_o) + \cos((\omega_i-\omega_o)t+\phi_i-\phi_o)\right]$$

Lowpass filtering yields the I signal:

$$\frac{AB}{2}\cos((\omega_i-\omega_o)t+\phi_i-\phi_o)$$

Multiplication of the I signal and the Q signal

$$\frac{(AB)^2}{8}\sin 2\left[(\omega_i-\omega_o)t+\phi_i-\phi_o\right].$$

If the loop is in lock the control signal becomes $\frac{(AB)^2}{8}\sin 2\left[\phi_i-\phi_o\right]$, which means that the phase error $\phi_i-\phi_o$ can only vary between $-\pi/4$ and $\pi/4$. The periodicity of the 'phase detector' characteristic shows a period of π

instead of the common single loop phase detector periodicity of 2π. The latter property is the main reason for its application on carrier recovery: it is possible to track signals in which phase steps of π are present. This is the case in Binary-Phase-Shift-Keyed (BPSK) signals. The Costas loop is therefore ideally suited to demodulate these signals. The demodulated signal is available in the loop itself in the form of the 'I signal.'

Quadricorrelator: The 'quadricorrelator' has a special place in this overview of loops based on the quadrature principle, because it is not a Phase-Lock Loop. The configuration resembles the Costas PLL except for one arm. Its original version [Richman, 1954] has a differentiator in one arm.

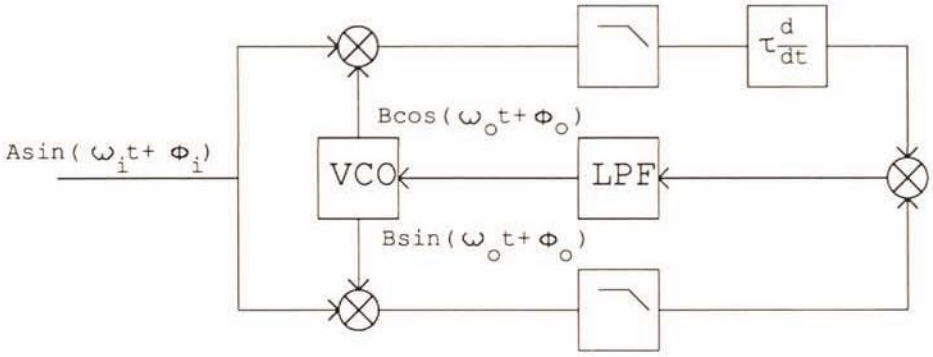


Fig. 3.15 Quadricorrelator

In the upper arm the signal $A\sin(\omega_i t+\phi_i)$ is multiplied by $B\cos(\omega_o t+\phi_o)$

$$\frac{AB}{2}\left[\sin((\omega_i+\omega_o)t+\phi_i+\phi_o) + \sin((\omega_i-\omega_o)t+\phi_i-\phi_o)\right]$$

Lowpass filtering removes the sum frequency term to obtain the Q signal

$$\frac{AB}{2}\sin((\omega_i-\omega_o)t+\phi_i-\phi_o)$$

At this point there is a difference with the Costas PLL, because this signal is differentiated:

$$\frac{AB}{2}\tau_d(\omega_i-\omega_o)\cos((\omega_i-\omega_o)t+\phi_i-\phi_o) \qquad (\text{'}Q^*\text{-signal'})$$

In the lower arm the signal $A\sin(\omega_i t+\phi_i)$ is multiplied by $B\sin(\omega_o t+\phi_o)$, yielding

$$\frac{AB}{2}\left[-\cos((\omega_i+\omega_o)t+\phi_i+\phi_o) + \cos((\omega_i-\omega_o)t+\phi_i-\phi_o)\right]$$

Again the sum frequency term is removed by lowpass filtering, leaving the I signal

$$\frac{AB}{2}\cos((\omega_i-\omega_o)t+\phi_i-\phi_o).$$

Multiplication of the I signal and the Q^* signal produces

$$\frac{(AB)^2}{8}\tau_d(\omega_i-\omega_o)\left\{1+\cos\ 2\left[(\omega_i-\omega_o)t+\phi_i-\phi_o\right]\right\}.$$

We find a DC term and a term with the double difference frequency. The double frequency term is also present in the Costas PLL; the DC term which is proportional to the frequency difference is absent there.

The additional differentiator makes the amplitude of the Q^* signal frequency dependent and introduces an additional phase shift of $\pi/2$. It is possible to realize a symmetric version with an additional differentiator, multiplier and summator [Gardner, 1985]. In this case the double difference ripple term is canceled out.

The quadricorrelator operates as a Frequency-Lock Loop (FLL), that is in lock when the frequency difference $\omega_e = \omega_i-\omega_o$ is equal to zero. The error voltage before the loop filter is proportional to the frequency difference and may be employed to speed up the frequency acquisition of a PLL (see section III.3.C).

Implementation aspects: Note that until now the signals were always sinusoidal. This does not yield the simplest system implementation in terms of electronic circuitry. If we are able to use binary signals, the circuitry mostly becomes simpler and more reliable. For example, a block form oscillator with two quadrature signals can easily be made with the following digital circuit:

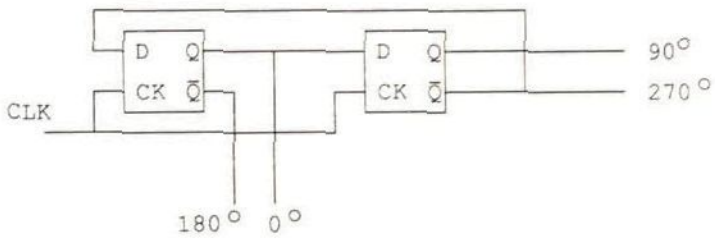


Fig. 3.16 Reliable four quadrature signal generation

With only two flip-flops in a Johnson counter configuration driven by a four times higher frequency we can make reliable quadrature signals. Contrary to proposals in literature [Gardner, 1979, p.206] the output phase relations are fixed and independent of the starting (power-up) conditions. The principle can be extended for multi-phase signals.

Multiplication with block waveforms: The consequences of the application of binary signals will be examined. When in the standard Q-PLL the oscillator signals are block forms, the multiplications yield:

□ upper arm:

$$\cos\omega_i t \bullet \left[\sin\omega_o t + 1/3\ \sin 3\omega_o t + 1/5\ \sin 5\omega_o t + ...\right] =$$

$$1/2\ \sin(\omega_i+\omega_o)t - 1/2\ \sin(\omega_i-\omega_o)t +$$

$$1/6\ \sin(\omega_i+3\omega_o)t - 1/6\ \sin(\omega_i-3\omega_o)t +$$

$$1/10\ \sin(\omega_i+5\omega_o)t - 1/10\ \sin(\omega_i-5\omega_o)t + ...$$

□ lower arm:

$$\sin\omega_i t \bullet \left[\cos\omega_o t - 1/3\ \cos 3\omega_o t + 1/5\ \cos 5\omega_o t + ...\right] =$$

$$1/2\ \sin(\omega_i+\omega_o)t + 1/2\ \sin(\omega_i-\omega_o)t +$$

$-1/6\ \sin(\omega_i+3\omega_o)t - 1/6\ \sin(\omega_i-3\omega_o)t +$

$1/10\ \sin(\omega_i+5\omega_o)t + 1/10\ \sin(\omega_i-5\omega_o)t + ...$

- subtraction of upper arm signal from lower arm signal

$sin(\omega_i-\omega_o)t - 1/3\ sin(\omega_i+3\omega_o)t + 1/5\ sin(\omega_i-5\omega_o)t + ...$, so in lock there are terms on $4\omega_i$, $8\omega_i$, etc.

The additional components due to the block form of the oscillator signals cannot be canceled out, but must be filtered by means of an additional filter.

For comparative reasons the ripple terms are given for various topologies, normalized to the single loop with vector multiplication:

- single loop; sine times cosine $\sin(\phi_i-\phi_o)+\sin2\omega_i t$
- single loop; sine times block $\sin(\phi_i-\phi_o)+4/3\ \sin2\omega_i t+8/15\ \sin4\omega_i t+...$
- quadrature; sine times cosine $\sin(\phi_i-\phi_o)$
- quadrature; sine times block $\sin(\phi_i-\phi_o) + 8/15\ \sin4\omega_i t + ...$

It would be possible to realize a Q-PLL with $\omega_n>\omega_i$, because the first unwanted term on $4\omega_i$ can still be filtered out.
For signals as generated by sample-and-hold circuits many more terms have to be taken into account. To obtain appropriate design questions and to investigate the behavior of a certain topology, with a view to obtain decisive answers for the choice of that topology, we will not describe these discrete signals.

Discussion: The possibility to track signals with $\omega_n > \omega_i$, follows from the examination of an angular modulated signal description:

$\sin\left[\omega_c t + \frac{\Delta\omega}{\mu}\ \sin\mu t\right]$, in which

ω_c is the carrier frequency,
$\Delta\omega$ is the frequency deviation and
μ is the modulation frequency.

The instantaneous angular frequency $\frac{d\phi}{dt} = \omega_c + \Delta\omega \cos\mu t$ shows no other limit than $\Delta\omega < \omega_c$. So, the angular modulating frequency can be unlimited.

However, in the PLL Frequency Model we introduced the quantity repetition frequency as a practical design limit, which implies that the period of the modulating signal is at least twice the period of the carrier signal. The virtual contradiction is caused by the different definitions, which have been in use for periodical signals.

Conclusion quadrature loops: For the *design* of QPLL's it is concluded that
- there are several applications in which the single loop cannot be used
and
- the basic problems of the operating ranges of single loops are still
present for multiple detector topologies.

It should be noted that to determine the operational properties from the linear and the non-linear analysis, the multiple detector topologies can be replaced by equivalent, single loop detectors with special properties.

□ *Example 1*

This can be seen in an application for phase-tracking of a Pseudo Random Noise Sequence (PRNS code), Direct-Sequence Spread-Spectrum signal. This signal has to be correlated with a local replica of the sequence. The auto-correlation function of the sequence has a triangular-like form as shown in Fig. 3.17.

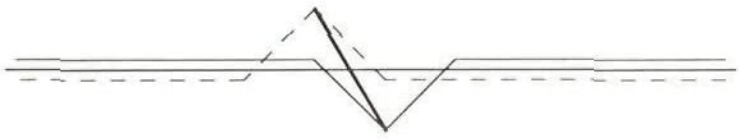


Fig. 3.17 Auto-correlation and control characteristic of PRNS-code

Correlation is essentially the same process as phase detection, viz. multiplication followed by integration, so if this code has to be phase locked, a control characteristic can be formed by subtracting of the correlation with another version (dotted line) from the local replica of the sequence. The control characteristic has been drawn in bold line type which connects the maxima of correlation. [ETET/GPS research reports, 1985-1989].

□ *Example 2*

If the Quadricorrelator is used as an acquisition-aid for a single loop, the designer has to choose whether or not he will incorporate the phase detector of the PLL into the quadricorrelator. He also has to choose whether or not the double difference frequency ripple filter of the quadricorrelator can be combined with the loop filter of the PLL. Any combination will form a so called Frequency-and-Phase-Lock Loop. Furthermore, the designer must determine whether or not the quadricorrelator operation must be switched off when the PLL is in lock. [Huizer, 1981]

□ *Example 3*

When a sample-and-hold circuit is used as a phase detector, problems may arise as to locking to the right harmonic, due to the switching actions and the harmonic sensitivity. Moreover (false)locking is possible for fractional harmonics. It is possible to employ the quadricorrelator principle in sampled PLL's [Regenbogen, 1980].

III.3 DESIGN AIMS

There are still a number of design compromises to be discussed. They produce specific questions when choosing a topology or configuration or they are manifest while calculating the values of the PLL circuit. Generally the designer will first try to improve single loop configurations before considering multi detector configurations. It is not clear yet which design questions have to be asked to obtain decisive answers. To that purpose we will now extend the earlier approach.

The ultimate aim of the topological approach was gathering design questions establishing the validity of the relevant models. The approach *will now be extended with a survey on recent, interesting case studies and* developments in handling the design compromises of PLL's.

The design compromises can be divided into four groups:

- TRACKING AND ACQUISITION
- SPURIOUS AND SPEED
- NOISE
- DIGITAL DESIGN

Of each group the fundamentals are first described together with proposals for circuits and/or design procedures. From these descriptions design questions may be extracted.

III.3.A Tracking and acquisition limitations

Adaptive Phase Detector (APD): A major problem in phase-lock loop (PLL) design is to meet the requirements of both fast signal acquisition and good synchronous mode behavior. In section VI.4 this relation is reviewed for different types of phase detectors. The emphasis is on digital phase detector implementation.

Several authors have described the behavior of PLL's with digital phase detectors, but little attention has been paid to the separation of the two basic operation modes of the PLL, the synchronous (filtering) mode, and the acquisition mode. Byrne [Byrne, 1962] and Goldstein [Goldstein, 1962] have analyzed the properties of PLL's with a sawtooth phase detector, realized with a set/reset flip flop. Compared to the use of sinusoidal PD, this device produces a better pull-in performance of the

loop because of the full linear range. The acquisition properties, however, are still limited by the periodic nature of the transfer function of the sawtooth PD. This problem can be relieved by employing frequency acquisition aids such as frequency sweep, frequency discrimination or feed-forward control. However, the acquisition aids require much additional hardware, and feed-forward control assumes an a priori knowledge of the disturbance.

Oberst [Oberst, 1971] showed that a digital phase detector can be modified into a phase-and-frequency detector (PFD) by adding a few logic gates, yielding a nonperiodic, but repetitive transfer function. In his paper he summarized the implementation of several pulse-type phase detectors and phase-and-frequency detectors. These PFD's enabled frequency acquisition without additional circuitry. The significant improvement of PLL acquisition performance with phase-and-frequency detectors was stated.

However, full separation of the two basic operation modes of the PLL cannot be realized. Only the sign of the frequency difference during acquisition is added; the maximum obtainable control voltage is still determined by filtering parameters.

A class of integrated phase-and-frequency detectors which significantly separate both modes is also presented in section VI.4. They may be considered as an adaptive acquisition control circuit. These adaptive detectors, which are based on the up-down counting principles, are investigated in a commonly used second-order PLL with a perfect integrator.

The idea behind it, is to combat the considerable difference between the direct lock time (T_L, see section II.2.C) and the pull-in time (T_P) by designing the PLL in such a way, that the loop never reaches the pull-in operation mode. In section III.2.A the lock-detection principle was described that also detects the entering of the PLL into the pull-in mode. This was combined with the up-down counter operation (see III.1.B) by increasing the number of counting cells from three to five. With the added outer cells the effective transfer factor of the PD is enlarged in such a way, that the loop still remains in the phase control mode.

The pull-in time is calculated exactly for the analysis of a PLL with the proposed phase detector in the appendix of section VI.4. It is shown that fast signal acquisition is possible without affecting the filtering properties of the loop. Experimental results of the acquisition behavior

of a second-order type-2 loop show a good correspondence with the theoretical analysis. The application of a five-cell adaptive phase comparator decreases the frequency acquisition time in this case by factor 50 at least.

Design conclusions: The properties of commonly used second-order loops that employ the adaptive phase-and-frequency detector based on up-down counting techniques have been discussed. Emphasis was on pull-in behavior and on a comparison with other phase detectors. Numerical results, both theoretical and experimental, were given for the situation of high signal-to-noise ratios[†] . They show a considerable speed improvement for high initial frequency detunings with regard to the loop bandwidth. It is possible to choose the loop bandwidth a lot smaller than usual, based upon the conventional compromise, without affecting the acquisition properties. This adaptive five-cell phase-and-frequency detector, used instead of a three-cell detector, can provide for an easy design procedure in many PLL applications.

Implementation aspects: It should be noted that in practice the use of conventional up-down counters has some restrictions, because of their vulnerability to simultaneous input pulses, which may result in a wrong counter state. This deranges the control action of the loop. This defect, inherent in conventional UDC's, can be avoided by gating both input signals, which causes a dead phase zone in the middle of the control range.

The novel circuit implementation for an adaptive phase-and-frequency detector, which can be seen as a 5-cell up-down counter (UDC), is proposed in section VI.5. This circuit can handle coincident input signals and has no dead phase zone or intermediate states.

The circuit is based on a different concept of up-down counting: for example, the use of two independent ring counters, one counting up pulses and the other counting down pulses. The state information is obtained from

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[†] *A preliminary estimation yields that the input SNR should be higher than approx. +10 dB.*

the combination of the contents of the distinct counters in a decoding circuit. Coincident input signals will cause a change in the state of the sequential, counting part, but because of the decoder the outputs of the UDC will not be different.

To prevent overflow the ring counters are only gated, when an outermost state is active. This indeed introduces a dead phase zone, which, nevertheless, is shifted to the extreme parts of the transfer characteristic. Hence this will not affect the synchronous mode performance, although theoretically the acquisition behavior is affected. In practice, however, the influence is negligible, but the circuit implementation of this phase detector is quite difficult, due to the requirements for the bounding actions and the counting scheme.

In the outermost positions special measures must be taken to prevent the UDC from jumping into the wrong position, because this will cause the sign of the phase error information to get lost. After the UDC has reached an outermost position, the leading signal must be suppressed. If the leading pulse occurs before the lagging signal, the leading pulse will be ignored and a cycle slip will result. However, the sign of the phase error is maintained.

The propagation delays for the bounding actions of the two counters determine the maximum phase comparison frequency. The counting scheme of the two counters should avoid intermediate states, i.e. no spikes may occur, when the UDC jumps from one stable position to another. The difference in the contents of the two counters is the measure for the position of the phase detector. A special difference counting and decoding scheme has been used to obtain a minimized logic design without intermediate states.

Improved circuit implementation: The described method of employing two distinct counters, for implementing an adaptive phase detector circuit, has a maximum phase comparison frequency that is severely limited by the bounding and debounding operations in the outermost cells. Investigations to speed up the operation have resulted in a new method that is as fast as the sequential elements themselves.

The improved implementation of an Adaptive Phase Detector (APD)

circuit is presented in section VI.6. A new design concept leads to a circuit with a higher maximum operation frequency while maintaining the basic requirements of handling coincident input signals and absence of intermediate states. The circuit is based on the application of a number of identical logic elements that are placed in a ring structure.

In an adaptive phase detector (APD) containing a separate up-counting and down-counting section, the bounding information can only be obtained from the outputs of the decoder. This global bounding method uses the outputs of the APD to control its inputs and will therefore be quite slow. A much faster bounding method is achieved when the bounding signals are directly obtained from the sequential elements. In this local bounding method the delay through the decoder is avoided. The maximum frequency of the circuit solely depends on the speed of the sequential elements. To implement this local bounding method quite a different sequential circuit is necessary.

The circuit consists of a number of identical elements placed in a ring. Each of the elements resembles a master/slave flip-flop except for the two clock inputs, an up clock and a down clock input. The setup signals of the element, derived from the neighboring elements, determine whether it is sensitive to its up or down clock. The five-cell up-down counter APD requires a ring of six elements, which must contain a string of k consecutive *ones* (indicating the elements which are set) with $1 \leq k \leq 6$. On successive up and down pulses the string circles in the ring in a fixed direction. Up pulses will add *ones* at the front of the string, whereas down pulses will turn *ones* into *zeros* at the tail of the string.

The position of the UDC is derived from the number of set *consecutive* elements in the sequential circuit, irrespective of the absolute position in the ring. The very fast, local bounding method has the disadvantage that processing fails if the *ones* in the ring no longer constitute a consecutive ring. If such a forbidden state arises, the circuit has to be reset to a permitted state. A special detection and reset circuit must be added to this purpose.

Adaptive Phase Detector, concluding remarks: In retrospective, the proposed application and IC realizations of the adaptive phase detector implies a considerable amount of work for the *industrial* PLL designer to redesign

a completely, new circuit, which is rather difficult. In addition some doubt about the final results come up when comparing it with other configurations. Although it is clear that the separation of design steps for the acquisition mode and the tracking mode relieves the common compromise, it is not yet completely known what the specific design advantages are in terms of decisive answers for the one simple topology or another.

Therefore a method is proposed which employs commercially available PLL IC's and that can speed up frequency acquisition considerably. The method for enhancing frequency acquisition performance of Phase-Lock Loops (PLL) is presented in section VI.7. This technique can be used in all PLL's that employ sequential phase detectors. The proposed method always forces the PLL into the phase-acquisition mode by realizing a phase detector transfer characteristic with a 'pseudo-linear, infinite' phase range. Especially in the case of Charge-Pump PLL's the proposed method is very useful. Practical results show that the acquisition performance can increase by nearly two orders of magnitude. As will be described, this method is difficult to implement in full integrated form, however.

Simple fast acquisition method: The frequency acquisition (pull-in) time of a PLL strongly increases with the initial frequency difference. Even with a linear sawtooth-like phase detector transfer characteristic, such as the already-mentioned phase-and-frequency detector (PFD), the acquisition time is much longer than expected from a linear model behavior.

The normalized acquisition time in the linear range (the settling time or phase-acquisition time) is approximately equal to

$\omega_n T_p < 5/\zeta$ for $\Delta\omega_0 < \pi.2\zeta\omega_n$ if the phase range is $(-\pi,+\pi)$.

In section VI.4 an overview is presented for frequency acquisition with various phase detectors. The given quasi-stationary approximation for a PLL with a perfect integrator in the loop yields:

$$\omega_n T_p < c.\ \frac{1}{2\zeta}\left(\frac{\Delta\omega_0}{\omega_n}\right)^2 \qquad \begin{array}{ll} c = 1 & \text{for sinusoidal,} \\ c = 6/\pi^2 & \text{for triangular,} \\ c = 1.5/\pi^2 & \text{for sawtooth-shaped transfer functions} \end{array}$$

The normalized frequency acquisition time $\omega_n T_P$ increases quadratically with the initial frequency difference $\Delta\omega_0$. Phase detectors with a built-in

acquisition-aid such as the PFD have the sign of the frequency difference added to the control action during pull-in. The acquisition time in this case is:

$$\omega_n T_p = \frac{1}{\pi} \frac{\Delta\omega_0}{\omega_n}.$$

Pull-in time is merely specified through filtering parameters. A method to separate acquisition and tracking performance into one circuit, is the application of an adaptive phase detector.

Another approach is to examine the signals in a PLL during pull-in. This leads to the proposed 'pseudo-linear' PD characteristic. During frequency acquisition the phase error increases proportional to the frequency difference ($\theta_e = \Delta\omega_0 . t$) and discontinuities are exceeded. So the linear model is no longer valid.

Besides, in terms of phase error the discontinuities are equivalent to phase steps. A phase step of 2π during the frequency acquisition process is a control action in the wrong direction and gives in a second order PLL with a PFD and an active filter a PD output voltage step equal to $V_{dd}/2$ and a control voltage step of $V_{dd}/2 . \tau_2/\tau_1$.
The output frequency steps in terms of loop parameters are equal to: $\Delta\omega = 2\pi.2\zeta\omega_n$.
This frequency step is also in the wrong direction and the acquisition is considerably slowed down.

If these steps are compensated, a full linear characteristic is made and phase acquisition is always maintained with a much smaller acquisition time as a consequence. The magnitude of the compensation can be simply determined from the loop parameters.

The remaining question is how to detect a discontinuity. In section III.2.A, a digital lock-detection circuit was given that is perfectly suited to this purpose, if the unlock flip-flop operation is modified (self- clear) and followed by a mono-stable. The method was shown to be applicable to integrated PLL's with phase detector transfer characteristics containing step discontinuities, such as a SR flip-flop and a phase-and-frequency detector. Experimental results show an acquisition-time improvement of nearly two orders of magnitude.

In contrast to the proposed adaptive phase detector for improving

acquisition time, this method is difficult to incorporate in a fully integrated design, due to the applied mono-stables.

This method emanates from a close examination of in-loop signals and topology which leads to a simple compensation of non linearities. The realization of a so called pseudo linear infinite phase range of the phase detector characteristic is useful when the input signal is not excessively disturbed by noise and there is no a priori information available about the disturbance. An approach to acquisition in case of input noise will be given in the section on noise.

Now we restrict ourselves to the situation that the disturbance is deterministic as in frequency synthesis. This means that the new frequency of the PLL is given and the design aims are mainly high switching speed and suppression of spurious.

III.3.B Spurious and switching speed limitations

Introduction: For frequency synthesis the following system requirements are mostly subjects for investigation on design and realization of frequency synthesizers:

- frequency range
- frequency resolution
- signal-noise ratio
- signal-spurious ratio, or Carrier-to-Spurious Ratio (CSR)
- settling time, or switching speed
- pull-out range
- complexity
- modulation

In Chapter II the input/output cross-tabulation chart shows for a PLL with divider P in the loop that the output frequency is equal to $f_{out} = P.f_{in}$. If the input frequency is obtained from a stable frequency source f_{ref} by means of a fixed divider Q one can perform the basic frequency-channel synthesis function:

$$f_{out} = \frac{P}{Q} f_{ref}$$

with a PLL in which the divider P can be varied. The frequency resolution (frequency-channel distance) is equal to f_{ref} / Q.

Switching speed and suppression of spurious: As has been investigated in Chapter II in the section on extended non linear analysis, the CSR depends on ω_n, ζ, P, ω_{ref}, and the phase detector topology. The settling time is mainly determined by ω_n and ζ.

It is clear that especially the requirements for CSR and settling time are in conflict. One cannot simultaneously achieve a high CSR and a low settling time with a single loop.

The function $f_{out} = \frac{P}{Q} f_{ref}$ can also be realized directly with one digital circuit that is called Rate Multiplier (RM). The switching speed is very high; almost instantaneously the new frequency is given. The output signal of a rate multiplier circuit, however, is not spectrally pure.

Rate multiplier loops: The rate multiplier signal was used to control a 'loose' Phase-Lock Loop with dead phase zone [Regenbogen, 1978], [DenDulk/VanWilligen, 1979]. In Fig. 3.18 a rate multiplier loop for frequency synthesis is shown. The rate multiplier signal is compared with the signal of a controllable oscillator in a phase detector with dead zone. The magnitude of the dead phase zone is dependent on the peak-to-peak phase error of the rate multiplier signal.

The 'PLL' has to compensate long-term frequency instability of an oscillator by referring to the perfect long-term stability of a rate multiplier signal from a long term stable frequency source.

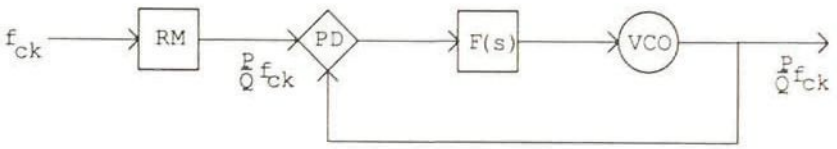


Fig. 3.18 Rate multiplier loop

An accumulator type rate multiplier has a much smaller peak-to-peak phase error than the commonly used rate multiplier. If an accumulator type rate multiplier is used together with a digital Harmonic Mixer (HM) and a special implementation of the adaptive phase detector as in Fig. 3.19, a closer tracking (smaller dead phase zone) can be obtained.

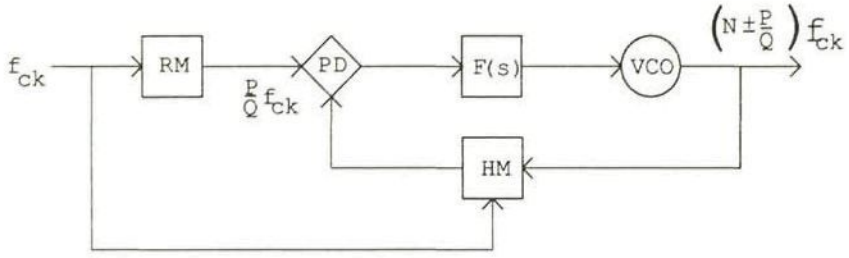


Fig. 3.19 Rate multiplier loop with harmonic mixer

This configuration which generates a frequency of $(N \pm P/Q).f_{ref}$, shows a much closer phase tracking, owing to the resemblance of the two signals. Rate Multiplier circuits based on the accumulation principle are not yet commercially available.

CMOS Accumulator-type Rate Multiplier: The promising concepts for frequency synthesis leads to the design and realization of such a circuit in CMOS. A versatile rate multiplier/variable divider integrated circuit that produces an optimally spaced output signal is presented in section VI.8. This includes a comparison of the commonly used rate multiplication scheme and the accumulator rate multiplier principle.

The design considerations for speed improvement are described, together with a scheme that leads to the special feature of a programmable denominator. In this case, the circuit can be used as a binary rate multiplier, BCD rate multiplier, or variable divider. Moreover the circuit may replace a number of commercially available rate multiplier IC's.

Cascading possibilities of the circuit are shown, and some application areas are given. The circuit is perfectly suited to be used as a microprocessor-compatible peripheral circuit in digital control systems.

Rate multiplier integrated circuits have been based on the principle of combining internally generated non-coincident pulse sequences. This pulse sequence combination scheme does not supply the best possible pulse distribution. When more IC's of this type are cascaded, the irregularity will increase substantially. For frequency synthesis this signal is not directly applicable. For other applications the momentary time error may be excessively large in many cases.

The accumulator type rate multiplier principle always provides the best possible digital approximation of a regular signal. The programmed number P is added to a register with capacity Q each clock period. On overflow, a clock pulse is generated. It is intuitively clear that this principle must produce an optimally spaced output pulse pattern because upon overflow the remaining value is still stored in the register. The next overflow condition is biased with this value.

The accumulator scheme has only one disadvantage: it is inherently slower than the pulse sequence combination scheme. The IC design was focused on speed improvement. In addition, the accumulator scheme can potentially broaden the range of applicability considerably.

The accumulator scheme for rate multiplication can easily be implemented. For a symmetrical clock pulse the main speed restriction is caused by the propagation delay of the overflow signal. If the carry signal is resynchronized with one additional flip-flop, a speed improvement of at least factor two is gained. Further speed improvements are possible by extending the pipeline technique for every bit section. We have made a compromise to restrict one pipeline section to 4 bits so that the circuit will not be slowed down too much and versatility will be gained if binary and BCD rate multiplication can be combined into one circuit.

The chip is realized using an industrial polysilicon gate CMOS process with a 4 μm gate length and local oxidation.

The proposed circuit is suitable for frequency synthesis in a quantized phase-lock loop. The circuit is also perfectly suited to realize a simple All-Digital PLL (see also Chapter V). Besides, the circuit can be applied to meet design requirements for a *new fractional harmonic synthesis* topology for low-power, relatively small-bandwidth, high-resolution, and fast-acquisition frequency generation [Wiltschut, 1982].

Fractional harmonic frequency synthesis topology: The application of a digital harmonic mixer† avoids high speed dividers at high synthesizer output frequencies and reduces power consumption. In combination with the accumulator type Rate Multiplier as a direct frequency synthesizer and an implementation of the Adaptive Phase Detector, a frequency synthesis topology is achieved with a very high frequency-acquisition speed.

However, the phase tracking still shows a dead phase zone resulting from the harmonic mixer. The dead phase zone can be diminished and fixed by using an accumulator type rate multiplier with a prime number denominator. In this case the dead phase zone is fixed for each frequency of the range $(N \pm P/Q).f_{ref}$.

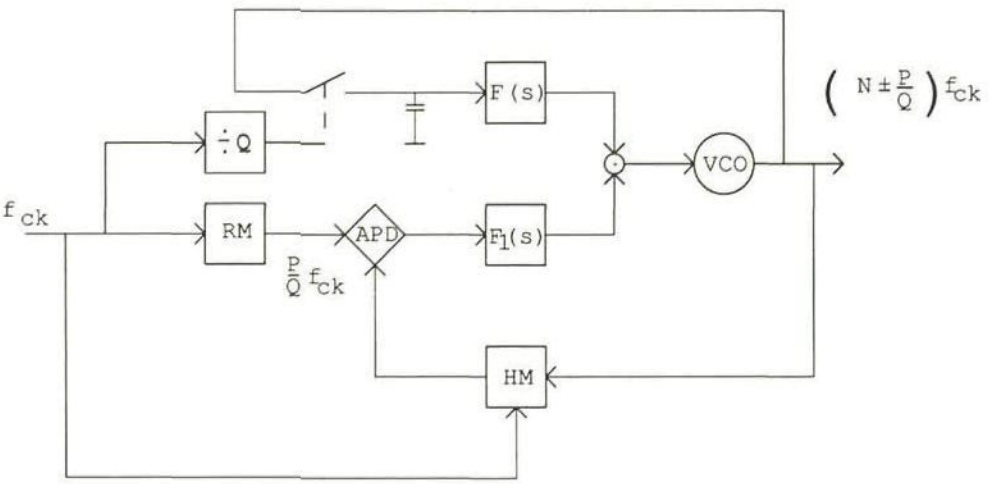


Fig. 3.20 Fractional harmonic frequency synthesis

The expression for the generated frequencies can also be written as

$(N.Q \pm P).\frac{f_{ref}}{Q} = M.\frac{f_{ref}}{Q}$, in which M may be very large.

---

† *See also section VI.9 in which the frequency transfer characteristic of a harmonic mixer is shown.*

This expression resembles the application of a sample-and-hold as a phase detector in a phase-lock frequency multiplier (see also section III.1.A.). A sampled frequency multiplier is difficult to design, because the frequency of the oscillator must be preset close to the required harmonic. When the sampling loop is combined with the above mentioned rate multiplier loop, an elegant low-power frequency synthesis topology has been realized. This topology is shown in Fig. 3.20.

The phase tracking, or small signal properties are independently designable by using a Sample-and-Hold circuit as a harmonic phase detector. The acquisition properties are determined by the rate multiplier controlled part of the configuration. The proposed topology can be seen as a Sampled PLL frequency multiplier with high frequency resolution and high Carrier-to-Spurious Ratio, which is controlled by a quantized frequency-and-phase-lock loop with high switching speed.

In conclusion, the different approaches to frequency synthesis on the basis of a special type of rate multiplier circuit have shown the following in terms of design aspects.

The design compromise was first investigated from the direct frequency synthesis point of view. This predicted fast frequency settling and good long-term stability. With digital circuitry as a fractional frequency source also inherently spectral impurity was achieved. A 'loose' phase-lock loop assured the long-term frequency stability.
Second the dead phase zone was decreased by the realization of an accumulator type rate multiplier integrated circuit and the introduction of a digital harmonic mixer, which increased the applicability simultaneously.

Finally, a configuration was investigated, that appeared to function as a sampled phase-lock frequency multiplier with high resolution (= high multiplication factor), that is frequency controlled by a rate multiplier signal.

In retrospect, configurations have been combined that have complementary properties, that, on their own, cannot fulfill the design requirements. In a multi-detector combination the switching speed and spurious requirements can be dimensioned virtually independent.

III.3.C Noise limitations

Introduction: Acquisition and tracking under conditions with *additive input noise* require special electronic implementations to ensure correct operation. The specifications for the tracking mode and the acquisition mode are conflicting. Besides, the question must be answered when lock-detection is required and in which cases acquisition enhancement is useful.

We have already found that under conditions of relatively high input signal-to-noise ratios many elegant circuit topologies can be used. These topologies are mainly based on the principle that *the limits for the PLL's linear state* can be established. In that case special measures can be applied to design the non linear frequency-acquisition properties.

The effect of additive input noise must now be investigated in more detail. Only then it will be possible to give topological design information for the simplest electronic implementation. In Chapter II the relation between additive input noise and the operating range of the PLL in terms of permitted output phase variance was investigated. The linear approximation for the phase difference between the clean input signal component and the oscillator signal turned out to be not valid when the *oscillator quasi peak phase noise* (= approx. 3σ) exceeds $\pi/3$. In that case the PLL probably fails to stay in lock.

Detecting the limits for the PLL's linear state is equivalent to frequency difference detection, i.e. detection of the number of events compared to a reference frequency.

Noise and frequency detection: Both in the linear model and in the non-linear model noise is generally considered as additive, gaussian, narrowband, white noise, that generates relatively small phase fluctuations in a linearized way. Half the noise power is phase noise and half the power is called amplitude noise. The variance of the phase noise is expressed as

$$\overline{\theta_{ni}^2} = \frac{1}{2SNR_i} = \frac{P_N}{2P_S} = \frac{N_0 B_i}{V_i^2}.$$

The phase noise is a relative quantity with respect to the signal power. A phasor diagram of the signal vector and a vector of the noise ensemble can be drawn. According to the narrow band approximation of noise, the noise vector can be decomposed into independent, perpendicular, base band noise vectors n_s and n_c. A closer examination of the angle between the signal vector and the noise vector gives a momentary value of

$$\phi = \arctan \frac{n_c}{n_s + V_i} \approx \frac{n_c}{V_i}, \text{ for } n_c \approx n_s \ll V_i.$$

This condition is certainly not fulfilled, when the momentary value of the noise is larger than the signal amplitude. In that case so called 'clicks' are generated, i.e. extra and missing zero-crossings relative to the number of zero-crossings of the signal. According to the approximation of a noise 'peak amplitude' of 3 times the RMS value in section II.2.D, this simplified estimation shows that, if the SNR is smaller than approx. 10dB, clicks are generated. These clicks have to be treated as additional momentary frequency fluctuations and are important for the acquisition mode of the PLL.

The acquisition mode of the PLL can be seen as the built-in frequency detector operation of a PLL. During pull-in, the initial frequency difference causes a small DC component, the so called pull-in voltage, that controls the VCO frequency for decreasing the frequency difference. This auto-acquisition operation of the PLL is essentially a frequency detector operation. As a consequence, the clicks from the input noise can severely disturb acquisition.

The noise transfer of the linear model (see section II.1.A) may be modified because of the two aspects we have mentioned: The linear approximation of the phase noise variance and the generation of clicks in the input signal.

Acquisition-aiding: Nearly all acquisition methods consist of adding some form of Frequency Detection (FD) to the loop (Fig. 3.21).

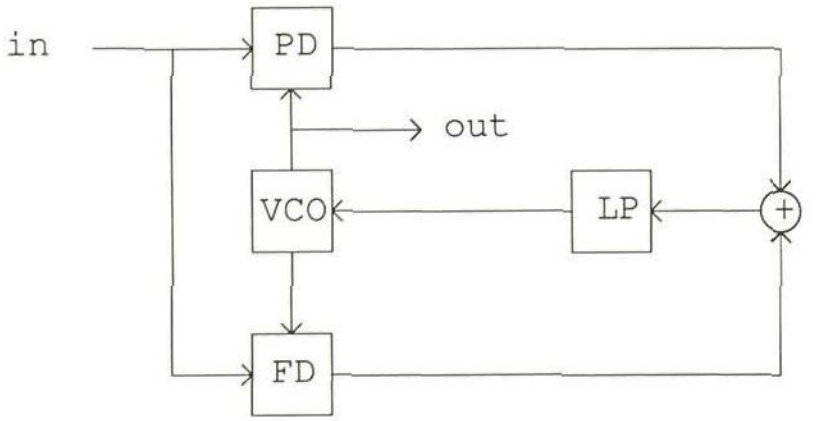


Fig. 3.21 PLL with frequency detector for acquisition-aiding

The FD loop is used to decrease the frequency difference between the input signal and the locally generated signal. If the frequency difference has become sufficiently small, the PLL will take over and will lock within one cycle of the momentary frequency difference.

Frequency detection, which is a wideband process, can disturb the acquisition and the tracking performance of the PLL under conditions of low signal-to-noise ratios. Investigations on a Frequency-and-Phase-Lock Loop (FPLL) [Huizer, 1981] show that an additional noise term is present due to the clicks, which deteriorates the acquisition behavior considerably.

Under in-lock conditions, the FD increases the oscillator phase noise. In the tracking mode of the PLL, the FD may be disconnected by means of a suitable Lock Detector (LD). In Fig. 3.22 a total block diagram is given for acquisition-aided PLL's.

Lock detection must show a close resemblance to frequency detection, because the operation consists of detecting phase or frequency fluctuations that deviate from those in the locked state of the PLL. In section III.2.A definitions of phase-lock were proposed. The lock detection method described there was based on the detection of cycle slips. Now the definition that considers the phase noise variance of the oscillator will be used.

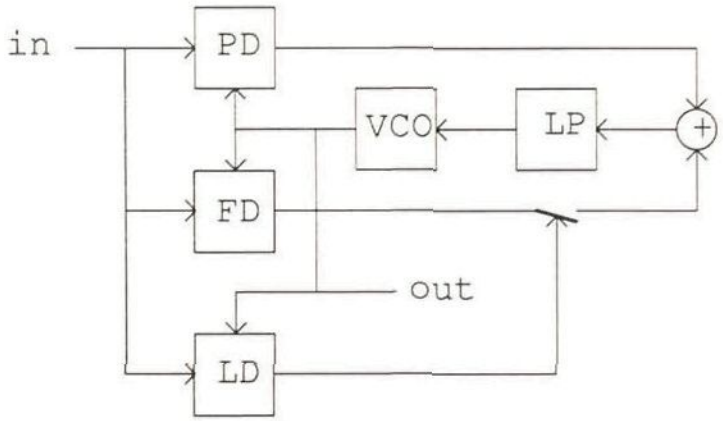


Fig. 3.22 Acquisition-aided PLL

Many authors have applied FD implementations to improve the acquisition properties of PLL's. Gardner [Gardner, 1979] has given an overview. One of the first was the original implementation of the so called quadricorrelator [Richman, 1954]. Other methods have been outlined in [Messerschmidt, 1979] and [McGeehan, 1980]. Many later implementations were essentially identical to the quadricorrelator.

However, generally applicable design information seems to be insufficient, especially on the selection of the most effective topology and implementation of an acquisition-aid under specific signal-to-noise conditions. To obtain design rules for acquisition-aids, more insight is required of the frequency detection behavior under conditions with input noise.

Theory frequency detection: The theory for frequency detection was developed from the early fifties till the seventies by scientists as Rice, Blachman, Axelson and Middleton. This was required for the purpose of modeling FM demodulation.

The requirements for the detection of a frequency difference by a frequency detector of an acquisition aided PLL, depend on the frequency detection properties of the PLL itself. If we neglect the auto acquisition

(pull-in) of the unlocked PLL, the frequency detector operation will be as Fig. 3.23 shows, in which a Frequency-Lock Loop (FLL) is drawn. The difference with the previously presented PLL Frequency Model from section II.1.B is clear: this detector is a genuine frequency difference detector with transfer factor K and the integration has disappeared.

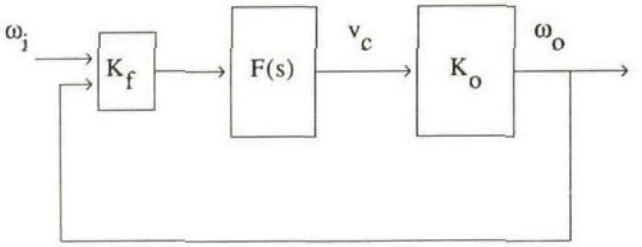


Fig. 3.23 Frequency-Lock Loop (FLL)

The transfer function is $\dfrac{\omega_o(s)}{\omega_i(s)} = \dfrac{K_f F(s) K_o}{1 + K_f F(s) K_o}$.

The transfer function from input frequency to control voltage is

$$\frac{v_c(s)}{\omega_i(s)} = \frac{K_f F(s)}{1 + K_f F(s) K_o}.$$

If a loop filter is applied with $F(s)=1/s\tau_f$, a detection bandwidth B_d is obtained proportional to $1/\tau_f$. This is equivalent to the standard frequency demodulator with a detection noise-bandwidth $B_{dn} = K_f K_o/4\tau_f$.

The frequency estimation problem for the FD of acquisition-aided PLL's is then transferred to the FM demodulation problem of a carrier that is 'modulated' with a DC signal. In combination with the PLL for the purpose of PLL acquisition enhancement, the error of the frequency detection should be smaller than the direct-lock range $\Delta\omega_L$ of the PLL.

The theoretical analysis of FM demodulators is well covered in literature by many authors. Two types of demodulators are abundantly used: the momentary frequency demodulator, and the zero-crossing counter. It has been shown in [Axelson, 1976] that both methods can be seen as equivalent, except that for the counter approach, the quantizing effect has to be taken into consideration.

For PLL acquisition-aiding we have to distinguish two errors of the frequency estimation, namely fluctuations and offset from the FLL. The fluctuations can be characterized by the output variance of the frequency estimation. This is equivalent to the linear noise transfer of the PLL.

The variance of the frequency estimate depends on the SNR_i, the input bandwidth B_i, and the detection bandwidth B_d. The bias term depends on the input SNR_i (called ρ_i from here), and on the input noise bandwidth B_i.

In other words, the variance can be kept arbitrarily low by choosing a suitably low detection bandwidth B_d (it takes a proportionally long time to find the estimate), but the bias term of the frequency estimation causes a lower bound for the application of FD-aided acquisition for low ρ_i. This bias term is related to the afore mentioned clicks. This term becomes significant under $\rho_i \approx 10$ dB. Moreover the clicks also cause an additional variance term in the output signal.

According to Rice [Rice, 1963] the power density spectrum of the frequency fluctuations can be rewritten as:

$$\Phi_f(f) = \frac{8\pi^2 f^2 N_0}{V_i^2}$$

For a first order detection bandwidth B_d, the variance is then approximated as

$$\overline{\sigma_f^2} = \int_0^\infty \Phi(f)\,|H(j\omega)|^2 df \approx \frac{N_0 B_d^2 B_i}{V_i^2} = \frac{B_d^2}{2\rho_i}$$

If the clicks have to be considered for $\rho_i < 10$ dB, the frequency estimate becomes biased and an additional variance term is introduced.

Click noise: According to literature, the clicks have to be considered as frequency pulses with energy content 2π in the output signal of a frequency demodulator. The average click frequencies are denoted as N_+ and N_-, for extra zero-crossings and missing zero-crossings, respectively. The bias of the frequency estimate can be expressed as

$2\pi(N_+ - N_-)$,

and depends on the difference of the considered frequency and the center frequency of the input filter, on the shape of transfer characteristic of

B_i, and on the signal-to-noise ratio ρ_i.

For a rectangularly shaped filter curve, calculations of the bias of the frequency estimate suggest to yield a bias equal to:

$$\mu_f = (\omega_c - \omega_i).e^{-\rho_i}$$

Measurements [Boere/Wolvers, 1988] showed that this relation is in good correspondence with practice, provided that special attention is given to implementation of the circuitry.

The variance of the frequency estimate due to clicks can be calculated by assuming that the clicks occur at random time intervals, such that the clicks can be represented by two independent Poisson processes, with total power spectral density

$$\Phi_{f,c}(f) = 8\pi^2(N_+ + N_-)$$

We have to know expressions for N_+ and N_- for employing this power density in the calculation of the output variance of the frequency estimator due to click noise. Rice determined very complex expressions for N_+ and N_-, that can be replaced for a rectangular bandwidth by

$N_+ + N_- = r.(1 - \mathrm{erf}(\sqrt{\rho_i}))$, in which $r = B_i/\sqrt{12}$ and erf(.) is the well-known error function.

If $(1 - \mathrm{erf}(\sqrt{\rho_i}))$ is approximated by $e^{-\rho_i}.(\pi\rho_i)^{-1/2}$, the variance due to click noise in a bandwidth B_d can be expressed as:

$$\overline{\sigma_{f,c}^2} = \frac{B_i B_d}{\sqrt{12}}\, e^{-\rho_i}.(\pi\rho_i)^{-1/2}$$

The output variance of a frequency detector can be written as the sum of the considered variances:

$$\overline{\sigma_{\Delta f}^2} = \frac{N_0 B_d^2 B_i}{V_i^2} + \frac{B_i B_d}{\sqrt{12}}\, e^{-\rho_i}.(\pi\rho_i)^{-1/2} = \frac{B_d^2}{2\rho_i} + \frac{B_i B_d\, e^{-\rho_i}}{\sqrt{12\pi\rho_i}}$$

Over a signal-to-noise ratio $\rho_i > 10$ dB, the second term of the expressions can generally be neglected.

Application to PLL acquisition-aiding: If we neglect the auto-acquisition of the PLL, the RMS errors of the frequency estimate have to be smaller than the direct lock-range of the PLL. Under this condition the PLL can take over control from the FLL as fast as possible. For a general analysis we will apply the design formulas of a loop with sinusoidal phase detector, although the conditions with varying input signal levels for the PLL quantities have not been taken into consideration.

The direct lock-range must be larger than the FD errors:

$$\Delta\omega_L > \mu_f + \sigma_{\Delta f} \Rightarrow \Delta\omega_L - \mu_f > \sigma_{\Delta f}$$

The RMS error is always > 0, so

$$\Delta\omega_L > \mu_f \Rightarrow \Delta\omega_L > (\omega_c - \omega_i).e^{-\rho_i}$$

The maximum bias can be expressed as $\pi B_i.e^{-\rho_i}$.

For a second-order, type 2 PLL the direct lock-range can be expressed in terms of loop noise bandwidth: $\Delta\omega_L = \dfrac{4B_L}{1 + \dfrac{1}{4\zeta^2}}$.

We have a specific bound for the usefulness of FD acquisition aiding:

$$\frac{4B_L}{1 + \frac{1}{4\zeta^2}} > \pi B_i.e^{-\rho_i} \Longrightarrow \frac{B_i}{2B_L} < \frac{2\,e^{\rho_i}}{\pi\left[1 + \frac{1}{4\zeta^2}\right]}$$

The PLL design question with respect to the applicability of frequency-detection for PLL acquisition-aiding has been answered. Under the condition that PLL auto-acquisition is neglected, the upper bound for the bandwidth ratio for useful FD aiding is approx.:

$$\frac{B_i}{2B_L} < .424\ e^{\rho_i} \qquad \text{for sinusoidal PD and } \zeta = .707$$

This means that for bandwidth ratios higher than 1, the signal-to-noise ratio ρ_i (in dB) has to be higher than given in the following table.

bandwidth ratio	minimum ρ_i
1	-.67 dB

2	1.9
5	3.9
10	5
100	7.3
1000	8.9

The foregoing discussion shows that the derived results from FM theory can be fruitfully applied.

Application to (Adaptive) Phase-and-Frequency Detectors:

These detectors, with the exceeding of the linear phase range as a criterion for acquisition enhancement, are inherently sensitive for missing and extra zero-crossings. From theory is known that the number of crossings depends on the noise spectrum and the signal-to-noise ratio.

> "If the number of crossings departs from the signal frequency, a PFD acts as though the loop is out of lock and tries to slew the VCO frequency to bring the loop back to 'lock'. At the very least, the wrong number of crossings will cause an additional bias of the PD output and, if the number of crossings is sufficiently wrong, tracking will fail entirely."

This quotation from [Gardner, 1979, p.131] shows that only qualitative statements have been given thus far.

The expected number of clicks is

$$N_+ + N_- = r\left[1 - \mathrm{erf}(\sqrt{\rho_i})\right] \approx r.\ e^{-\rho_i}.(\pi\rho_i)^{-1/2}.$$

The parameter r may be regarded as either the "radius of gyration" (Rice) about its axis of symmetry at $f = f_c$ or as the 'representative frequency' of the signal. For a rectangular shaped filter r is equal to $B_i/\sqrt{12}$. For a normal- law (Gaussian) filter shape ($\sigma = s_b$) with a noise bandwidth of $s_b\sqrt{(2\pi)}$, the parameter r is s_b, or in other words $B_i/\sqrt{(2\pi)}$.

The number of clicks appears to be independent of the center frequency of the signal, only the signal-to-noise ratio determines the number of clicks with a proportional factor which depends on the bandwidth and on the shape of the input filter. For the two given filter shapes the

difference is a factor √2.

For obtaining design information with respect to the applicability of PFD's, an other approach will give more insight into these facts. If we relate the amplitude of a sinusoidal signal (V_i) and the rms-value of the noise (σ) to the signal-to-noise ratio (ρ_i) as follows:

$V_i = \sqrt{2}\sigma \qquad \rho_i = 1 \quad (0\ dB)$
$V_i = 2\sigma \qquad \rho_i = 2 \quad (3\ dB)$
$V_i = 3\sigma \qquad \rho_i = 4.5 \quad (6.5dB)$
$V_i = 4\sigma \qquad \rho_i = 8 \quad (9\ dB)$
$V_i = 5\sigma \qquad \rho = 12.5 \quad (11\ dB)$

and calculate then the probability that the noise is larger than the signal amplitude, this yields:

$\sqrt{2}\sigma \qquad P(|x|>V_i) = 1.615\ 10^{-1}$
$2\sigma \qquad P(|x|>V_i) = 4.55\ 10^{-2}$
$3\sigma \qquad P(|x|>V_i) = 2.7\ 10^{-3}$
$4\sigma \qquad P(|x|>V_i) = 6.334\ 10^{-5}$
$5\sigma \qquad P(|x|>V_i) = 5.73\ 10^{-7}$

The expected number of clicks divided by the parameter 'r' from the formula of Rice shows for the different ρ_i:

$\rho_i = 1 \quad (0\ dB) \quad (N_+ + N_-)/r = 2.08\ 10^{-1}$
$\rho_i = 2 \quad (3\ dB) \quad (N_+ + N_-)/r = 5.4\ 10^{-2}$
$\rho_i = 4.5 \quad (6.5\ dB) \quad (N_+ + N_-)/r = 2.95\ 10^{-3}$
$\rho_i = 8 \quad (9\ dB) \quad (N_+ + N_-)/r = 6.69\ 10^{-5}$
$\rho_i = 12.5 \quad (11\ dB) \quad (N_+ + N_-)/r = 5.95\ 10^{-7}$

Apparently, the conclusion may be drawn from these figures, that the statement is true: Under the condition of a signal-to-noise ratio equal to 4.5, in a number of 10^4 cycles of a signal with frequency ω_c, probably 27 clicks are generated by the fact that the noise amplitude is larger than the signal amplitude.

Then we can follow a similar approach as in case of the frequency detector. To assess the disturbances of a PLL with PFD quantitatively, the bandwidth B_i and ρ_i determine the number of clicks equivalent to the FD case.

A closer look at the operation of this sequential phase detector, shows that the clicks can be considered as phase steps $\pm 2\pi$. An extra edge of the input signal causes the PFD to jump from a phase error of e.g. $-.1\pi$ to $+1.9\pi$. A missing edge causes a phase step from e.g. $+.1\pi$ to -1.9π.

The repetition time of the disturbances should be smaller than the lock time, in other words the click frequency must be smaller than the direct lock-range of the PLL. The direct lock-range of a second-order type 2 PLL with PFD (see also section II.2.C) is equal to $4\pi\zeta\omega_n$.
For a normal-law filter shape the click rate is

$$e^{-\rho_i} . (\pi\rho_i)^{-1/2} . B_i / \sqrt{(2\pi)}.$$

Obviously the conditions for the inequality

$$e^{-\rho_i} . (\pi\rho_i)^{-1/2} . B_i / \sqrt{(2\pi)} < 4\pi\zeta\omega_n$$

are *nearly always fulfilled.*

We have to discover a more restricted condition, because we know from experience that the conditions for application are very tight.

The average number of zero crossings per second N_n of *gaussian noise* that pass through an ideal band pass filter whose pass band extends from f_a to f_b , is:

$$2\left[\frac{1}{3}\,\frac{f_b^3 - f_a^3}{f_b - f_a}\right]^{1/2}$$ [Rice, 1945, form.(3.3-12)]

When f_a is zero this becomes $1.155\ f_b$ and when f_a is very close to f_b it approaches $(f_b + f_a)$.
For a rectangular shaped band pass filter B_i centered on f_c it is equal to

$$N_n = 2\ (f_c^{\,2} + B_i^{\,2}/12)^{1/2}.$$

This is equal to $2f_c$, only if $B_i \to 0$. For $B_i = f_c/2$, the number of zero crossings deviates 1%.

For the average number of zero crossings N_u per second of *a sine wave and noise*, Rice derived a complex expression in [Rice, 1948, form.(2.8)]. The expression shows that for signal-to-noise ratios ρ_i smaller than approximately 10 dB, the ratio of the signal frequency and the number of zero-crossings divided by 2, departs from one, depending on the offset from the center frequency and on the relative bandwidth.

Concluding remarks: The discussions about noise and acquisition, show that the design questions and the answers for the phase-and-frequency detectors, have been partly obtained. The sequential phase detectors have memories and consequently a missing or extra zero-crossing of the input signal will have an influence on the loop operation during several periods of the input signal. The analysis is therefore still unfinished and thus some of the designer's uncertainty whether to choose such a topology or not is still present.

The analysis of zero crossings must be extended further, applying the theory to obtain useful design information and perhaps new circuit configurations.

The phase detectors used in the frequency-lock (FLL) part of frequency-and-phase-lock loops, make use of the complete waveform of the input signal (multiplicative PD) instead of the zero-crossings only (sequential PD). In this case design information about the applicability of frequency detection for PLL acquisition-aiding has been established. The FD design however, cannot be close to ideal, due to the phase detector ripple of conventional phase detectors mostly used in the FLL part of frequency-and-phase-lock loops.

In section VI.12 a new multiplicative phase detection method is presented. The phase detector ripple is canceled. The principles of the compensation method are discussed, and the implementation possibilities are given together with some preliminary experimental results. This method offers many possibilities for a considerably improved performance. Especially the simple implementation of the multiplicative PD principle, combined with a very low ripple is very useful under conditions with excessive input noise.

The implementation of loop components is a dominant factor in the total design cycle. Until now digital circuitry has been preferred to improve PLL performance. The phase information, however, is still processed as time-continuous. An important design compromise has been ignored, thus far, namely considering the fully digital processing of the phase information, i.e. taking a sample and quantizing the information. In the following, the fundamental measures for digitizing will be discussed briefly.

III.3.D Digital design

References to digital circuit techniques were thus far assumed for simple implementation purposes. The present trend to digitizing cannot be denied.When the phase information will be digitized, characterization in terms of the principal measures, sampling frequency and quantization, is required.

In section VI.9 the concept of 'harmonic mixing' frequency conversion has been presented to link the baseband and the bandpass sampling theorems. The frequency conversion characteristic indicates spectral folding (aliasing) and inversion cases and leads to generally applicable theoretical minima and maxima for the sub-Nyquist sampling frequency. The determination of whether or not phase-lock sampling is required is straightforward.

The question of quantization is related to the problem of sampling-frequency determination. Phase information is a relative quantity and can be measured periodically. It can only be measured at certain instants of time, if the sampling time is harmonically related with the frequency of the input signal. The phase detector transfer characteristic then becomes quantized in phase and in output voltage. This non-linear operation can disturb system operation.

In section VI.10 an example is presented of a system function that was considered as phase detection. The despreading operation of direct-sequence spread-spectrum signals is commonly seen as the correlation of a local replica with the incoming signal. This was considered as a phase-tracking loop, in which a special phase detection function is implemented. This phase detection function was described in terms of sampling despreading. The sampling frequency has to be non-synchronous with the input frequency to prevent interference problems and to obtain a high phase-tracking resolution. Furthermore the sampling and despreading operation was combined into one circuit.

The approaches to digital design will ultimately result in configurations in which phase processing, with or without phase-tracking,

will be carried out in numerical form. Also all-digital PLL configurations in hardware are very promising design alternatives. In the next chapter all-digital PLL's will be considered

Summary of Chapter III

Given that the linear and non-linear model approaches to a standard single loop indicate that one or more design objectives cannot be met, single loop improvements become a natural choice of the designer. These improvements are most generally concerned with the phase detection function. A sample-and-hold circuit is shown to improve the loop performance with respect to ripple suppression. A phase-and-frequency detector improved both the ripple suppression and the acquisition performance. Moreover, the circuit can be built with simple digital circuits. If some specifications remain unmet the designer has to resort to a multi-detector topology.

Details inherent in the structure of the input signal may imply a multi-detector topology. A multi-detector topology is shown to be conceptually equivalent to a single loop with a special phase detector. It is not obvious if this is the ultimate choice the designer has to make.

The generalized design model was extended in section III.3 in order to explore practical design compromises. The adaptive phase detector and lock detection were examined with respect to design compromises concerning tracking and acquisition. Rate multiplier loops were introduced to illustrate the design dilemma existing between switching speed and spurious suppression in frequency synthesis. Finally design constraints in the presence of excessive input noise were considered, and proposals were considered for digital design.

It should be noted that, although much design information has been extracted thus far, further investigation will be necessary for validating topology choice under the influence of noise.

CHAPTER IV ALL-DIGITAL PLL DESIGN

Digital PLL's have been in use since the early sixties, if not before [VanDenBerg, 1988]. An overdriven vectorial multiplier phase detector functioning as a switching phase detector, may be considered to be a digital circuit.

PLL performance improves in the main when replacing loop components by digital circuits. This was first observed by *Westlake* in 1960, who converted the output signal of the loop filter into a control signal for a digital oscillator by means of a sample-and-hold circuit. His intended purpose was to profit from the better stability and linearity of a digital oscillator compared to an analog steerable oscillator, either of the sine-wave or multivibrator type. In 1962 *Byrne* described a PLL using a digital phase detector, nowadays a standard phase detector, the SR flip-flop. His design aim was a linear phase transfer characteristic. It was not until 1968 that *Gupta* replaced Byrne's last functional block, namely the loop filter, by a digital implementation.

A PLL in which one or more parts are implemented by a switching or digital circuit is termed *Digital Phase-Lock Loop (DPLL)*. When the PLL is realized with digital circuits only, it is termed an *All-Digital PLL*

(ADPLL). The first ADPLL was presented in 1967. *Drogin* realized a fully digital 'VHF omnidirectional range finder (VOR)'. In this navigation system the PLL had to track a slowly varying 30 Hz signal. The fast development of IC technology has increased the interest in the ADPLL. The ADPLL is perfectly suited for integration in large systems.

The use of digital circuits in PLL's may improve the performance, but the applicability and validity of the models used requires verification. For PLL's with analog circuits only, the linear models used are more or less implementation-independent.

As to DPLL's, the mostly implicit *time-continuity* conditions of the models of Chapter II have to be investigated. This will probably mean that the analysis should consider the hardware implementation. In almost all reported cases, models of the DPLL were developed using the waveform of the input signal and the specific implementation as a starting point. This design method is 'bottom-up' in nature. This results in models whose use is limited to a single specific application.

An early contribution to DPLL characterization was that by Lindsey and Chie [Lindsey/Chie, 1981]. We have also chosen to characterize DPLL's by their type of phase detector, keeping in mind that form of switching action is of fundamental interest. We will particularly emphasize the realization of the oscillator. Our main aim is to present a design approach in which the designer can decide whether a digital topology is practical.

To this end a brief survey will be given of the implementation of digital oscillators for use in all-digital PLL's. A number of new All-Digital PLL topologies, implementations and applications will also be presented.

A general implementation-independent model for ADPLL's will be initiated. In this model the fundamental relation between sampling frequency and resolution will be examined, because of its important role in the application of PLL's. The model can be used to decide whether an ADPLL can replace a common PLL.

The examples have been chosen to demonstrate how the electronics designer is able to improve the overall design of a spread-spectrum receiver or any other telecommunication system implementation in which the phase-lock principle is used.

IV.1 DIGITALLY CONTROLLED OSCILLATORS

Modeling: A review of PLL modeling, especially for oscillator models leads to the fundamental statement that an oscillator produces an additional amount of phase $\Delta\phi$each time interval Δt, which corresponds to the frequency of the oscillator. An oscillator yields a phase angle per time period or, in other words, rotating a vector with a specific speed. When the oscillator delivers an analog, sinusoidal waveform with a fixed frequency, the quantity $\Delta\phi/\Delta t$ is time-continuous and constant. If the phase information of an oscillator is only available on certain *sampling* time instants, as is the case for digital or switching oscillators, sampling theorems have to be used to analyze the behavior. Piece-wise linear waveforms such as sawtooth and triangular, may also be considered as sampled signals.

Strictly speaking only sinusoidal waveforms are generated by an oscillator, all others being waveform generators. However, the term oscillator is used because this is common practice.

Digitally controlled oscillators (DCO) to be used in All-Digital PLL's must be based on the 'addition' of a quantity of $\Delta\phi$ phase units at predefined time intervals Δt. These time intervals are derived from a clock signal. To generate a total cycle, a digitally controlled oscillator must either produce 'controlled parts of phase' each time interval, or a fixed quantity of phase per 'controlled number of time units'. In other words, to obtain a controlled frequency it is possible to count a variable number of clock periods or to accumulate a variable quantity of phase.

If every cycle must have a constant period time, the oscillator frequency and the sampling frequency should have a common divisor to which they are harmonically related. In PLL's this cannot be true mostly, because a PLL is intended to track the input phase precisely. Consequently, the successive periods of the oscillator will fluctuate and the spectral purity can be rather low, due to frequency components on the common divisor frequency distance.

Various DCO implementations for ADPLL's will now be characterized, together with their main performance.

Counters: Frequency division with digital counters is based on *phase counting* in terms of 2π of the input signal with frequency f_{ck}.

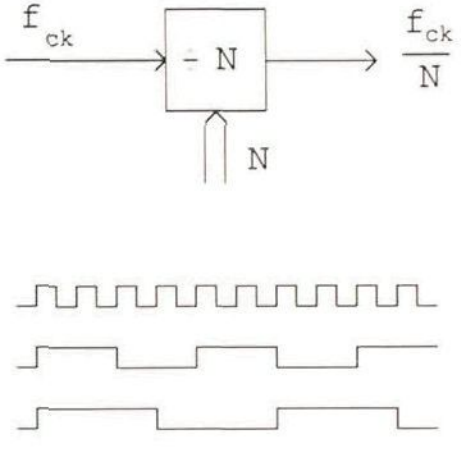


Fig. 4.1 Digital counter and waveforms

The contents of the counter are equal to fractional phase steps of $2\pi/N$ of the output signal. When the output frequency has to be controlled the division factor N has to be varied, so, the capacity of the counter must be variable.

The transfer characteristic (i.e. the output frequency as a function of the division factor) is non-linear.

The maximum frequency of a variable counter is three to four times lower than the toggle frequency of the flip-flops. If only a part of the total counter capacity can be used for the control range a faster counting scheme can be used, the so called *swallow counting* scheme. The swallow counting scheme is based on one fast dual-modulus swallowing counter (M,M+1), which is controlled by two slower variable counters A and B [Regenbogen, 1980]. The division factor is equal to (M.B + A), provided that B > A.

The side step programming scheme is the same as swallow counting for a factor B higher output frequency. The effective division factor is equal to (M + A/B), for B > A. In this case the distribution of the swallow actions over the repetition period determines the spectral purity. This counting scheme is a fractional one, because the output is not taken from

the output of the swallow counter, but from the swallowing counter.

For any counter scheme the control input must be supplied as a *digital word.*

Phase Shifters: As frequency is by definition the derivative of phase, *symmetric frequency steps can be generated by phase-modulating a carrier* frequency by means of a triangular waveform. When we increase the phase of a signal by 2π each second, the average frequency is 1 Hz higher. Based on this principle various topologies can be used:

□ As stated before in the Quadrature PLL section, we can generate four signals with $\pi/2$ difference by a 2 bit Johnson counter.

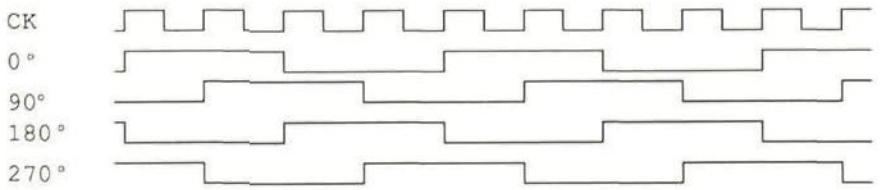


Fig. 4.2 Two-bit Johnson counter waveforms

If we choose a $\pi/2$ earlier version of the signal by means of a multiplexer every second, the average frequency will be increased by 1/4 Hz.

□ The Add/Delete or Increment/Decrement scheme is based on *repetitive phase shifting* of the idle output frequency with steps of magnitude π. In Fig. 4.2 the waveforms for incrementing and decrementing are shown. The *frequency of a fixed clock frequency signal is divided by two by suppressing* every other pulse. In incrementing, the empty place is filled (waveform b) and in decrementing the empty place is repeated (waveform c), thus creating phase steps of π. If the average output frequency has to be controlled, the repetition frequency of the phase steps must be varied.

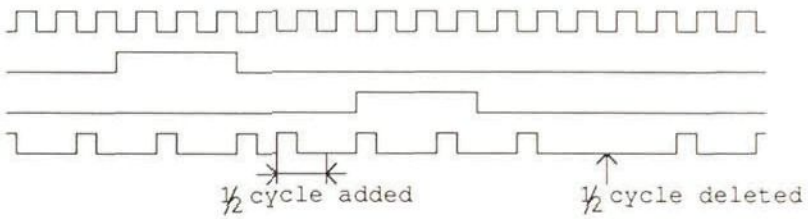


Fig. 4.3 Add/Delete waveforms

To control this kind of repetitive phase shifting, the total oscillator has to be extended by some form of timing device, because the average frequency deviation is the amount of phase per time unit. Repetitive phase shifting should be seen as frequency addition of the variable, controlled frequency to a fixed frequency or subtraction from it. As will be shown below the variable frequency can be generated by a counting scheme again.

Rate multiplier: Rate multiplication can be based on pulse pattern combination or on repetitive phase addition of fractions of 2π of the desired output frequency (Chapter III). In a rate multiplier based on repetitive phase addition the two mechanisms of phase shifting and variable counting are combined, so this circuit is perfectly suited to be used as a digitally controlled oscillator in a ADPLL.

When the output frequency has to be controlled, the fractions must be variable and again the control input format appears to be a digital word.

Controllability

The properties of the above given methods will now be compared in summary. The method for controlling the frequency (control), the maximum operation frequency (max.freq.), the maximum modulation frequency (mod.freq.max), the frequency resolution (freq.res.) and the frequency variation or the transfer factor (freq.dev., K_o) will be compared.

	divider	shifter	rate multiplier
control	word	via counter	word
max.freq.	$f_{toggle}/3$	f_{toggle}	$< f_{toggle}/3$
mod.freq.max.	f_{out}	f_{out}	f_{out}
freq.res.	$f_{ck}/N_{1\to2}$variable	any	f_{ck}/Q
freq.dev.,K_o	$\frac{\Delta f}{\Delta N} = \frac{f_{ck}}{N(N-\Delta N)}$	$\Delta f = \Delta\phi.f_{rep}$	$\Delta f = \frac{\Delta P}{Q}.f_{ck}$

The aspect of frequency that has to be considered, is the average frequency. This implies that the phase errors relative to a desired, regular-spaced frequency are averaged. The peak-to-peak phase errors are:

	divider	shifter	rate multiplier
$\Delta\phi_{e,pp}$	$\frac{2\pi}{N/\Delta N}$	$\frac{2\pi}{N}$	$\frac{(P-1)2\pi}{Q}$

This phase error can be lowered by dividing the output signal again. This implies that the output frequency also decreases. This is an important property of nearly all digitally controlled oscillators. The phase resolution is determined by the clock frequency. In any digital system only complete clock pulse periods are available.

Therefore, the irregularity of all clocked systems for frequency generation is essentially equal to the period time of the master clock. Division does not alter the time error, but it is now related to a larger period time and so the phase jitter has been decreased

The foregoing description of digitally controlled oscillator principles, illustrates for the implementation-independent modeling of these oscillators, that the phase resolution is quantized at a sampling frequency, which is equal to the master clock. This will be applied to derive an implementation-independent model of digital PLL's.

First we will concentrate on the application of loop components described thus far, leading to different possibilities for implementation of all-digital PLL's.

IV.2 ALL-DIGITAL PLL CIRCUITS

So far, we have used the term 'digital' in a general sense for switching circuits, as is common practice. For the digital controlled oscillators a clocked behavior is assumed to determine the minimum deviation from an ideal frequency. These statements are given to connect the concepts of digitally controlled oscillators and the digital phase detector circuits from Chapter II and Chapter III. A multivibrator-type variable oscillator circuit is a digital circuit (it produces a binary signal), but it is controlled by means of an analog signal. In this sense it is not a digitally controlled oscillator.

A first order All-Digital Phase-Lock Loop can be obtained using any combination of a digital phase detector circuit and one of the above mentioned digital oscillator principles. The output signal of digital phase detectors is a binary signal, the duty cycle of which is considered as a measure for the phase difference. This duty cycle signal can be employed to control a digitally controlled oscillator. This will be shown in the following, together with a new approach to second-order implementations and by presenting special all-digital phase detectors for demodulation of BPSK.

IV.2.A All-digital PLLs based on modulated rate multiplication

All-digital PLL configurations will be presented that are based on an accumulator type rate multiplier (ATRM) acting as a digitally controlled oscillator. As was described in Chapter III, ATRM circuits, used as a fast switching frequency source, can be cascaded to produce a high frequency resolution. The rate-output is an optimally spaced pulse pattern with average frequency:

$$\omega_o = \frac{P}{Q}.\omega_{ck} = \frac{P_k Q_{k-1} Q_{k-2} \cdots Q_0 + P_{k-1} Q_{k-2} \cdots Q_0 + \ldots + P_0}{Q_k Q_{k-1} Q_{k-2} \cdots Q_0}$$

for n-cascaded circuits (n = 0,1,2,3....k).

If we consider the numerator as the digital control input, the circuit behaves as a Digitally Controlled Oscillator (DCO) with an output

frequency of $\omega_o = K_o.P$, in which the DCO transfer factor $K_o = \omega_{ck}/Q$. If the static 'control voltage' is a digital word, the frequency of the DCO ranges from zero up to the clock frequency. However, if P is periodically switched between two values P_0 and $P_0 + \Delta P$, we can control the average output frequency by means of the time intervals of P_0 and $P_0 + \Delta P$. The *duty cycle* E $(0 \leq E \leq 1)$ of the time intervals determines the average output frequency as follows:

$$\omega_o = (P_0 + E.\Delta P).K_o \text{ ,in which } E = \frac{t_{P_0+\Delta P}}{t_{P_0+\Delta P} + t_{P_0}}$$

If $\Delta P = 1$, we can choose between either switching the least significant bit (LSB) of P, or switching the carry input CI of the modulus-Q adder, which will result in a DCO with two independent control input ports.

It should be noted that $t_{P_0+\Delta P} + t_{P_0} = T_S$ should be smaller than the sequence length of the ATRM signal. Since an ATRM yields the best digital approximation of a regular signal, there will always be a residual phase jitter equal to $\Delta\phi_{e,p\text{-}p} = 2\pi(P\text{-}1)/P$. Practical tests and simulations [VanderCammen, 1983] proved that this will be maintained if $\Delta P \ll P_0$ and the switching period that must be used to define the duty cycle as the controlling variable is smaller than the cyclic length. Otherwise an increase of the phase jitter is to be expected.

Finally, duty cycle *conversion* should be mentioned as being a most useful property of the ATRM. The duty cycle of the carry output (CO) is equal to ω_o/ω_{ck}. If two non-coherent duty cycle signals with E_1 and E_2 are applied to the carry input (CI) and the LSB of the numerator, with all remaining bits of P put back to zero, the output frequency will be $\omega_o = \omega_{ck}(E_1 + E_2)/Q$. The duty cycle of the carry output will be $E_o = (E_1 + E_2)/Q$. This additional property of duty cycles turns out to be very useful indeed for the realization of higher order loops.

First-order ADPLL: In Fig. 4.4 the block diagram is given of a first order ADPLL based on modulated rate multiplication. First-order ADPLL's will easily be implemented with the ATRM used as a DCO and a phase detector like an XOR. The phase detector translates the phase error information to the duty cycle of its output signal. In the PLL's used thus

far this signal is averaged in the loop filter. In an ADPLL this duty cycle signal E can directly serve as a 'control voltage' for the DCO. If the duty cycle increases, the ATRM average output frequency will also increase, which in its turn reduce the phase difference and vice versa. The loop will stabilize at the fixed phase difference that causes the same output as the input frequency.

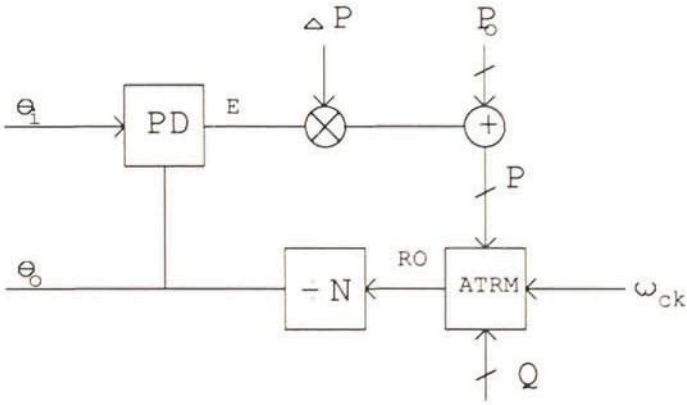


Fig. 4.4 ADPLL based on modulated rate multiplication

In the block diagram the adder and multiplier are only symbolic. A loop with $\Delta P = 1$ can simply be realized by connecting the phase detector output directly to the LSB of the numerator input, or to the carry input of the ATRM. The divider N in the loop is given to decrease the phase error of the DCO.

Loop analysis: Analysis by means of z-transforms appears to be impossible, since phase error variations (represented by the duty cycle) E are not expressed as binary numbers that are available each clock period, but as a sequence of ones and zeros. Only if the duty cycle repetition-rate is assumed to be small compared to the loop relaxation time, we can approximate E by a numerical value between zero and one. In that case the loop can also analyzed in the s- plane. This is mainly in accordance with Chapter II. We find a hold range $\Delta\omega_H = \Delta P\omega_{ck}/2QN$ and a -3dB bandwidth equal to $K_d\Delta P\omega_{ck}/2QN$. Only the phase detector transfer factor K_d could influence the loop bandwidth, but this is fixed for one PD type only.

Loop extensions: If a phase-and-frequency detector (PFD) is employed in a first-order loop based on modulated rate multiplication, the normal frequency detector action is lost, since in a normal second-order loop this action is based on the accumulation of the detected 'frequency-error voltage'. In a first order loop this is not possible. The PFD only increases the phase error range. A realization example with the common three-cell PFD is shown in Fig. 4.5.

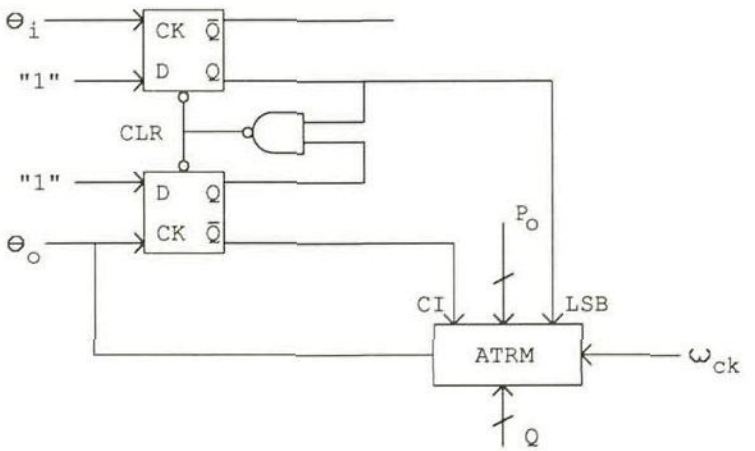


Fig. 4.5 Realization of a ADPLL with a three-cell PFD

A phase-and-frequency detector can be seen as an up-down counter (UDC) with three cells (see also Chapter III). If the number of cells is increased, the linear phase error range grows accordingly. The limit is reached when the number of cells equals the number of bits of the numerator of the ATRM. In Fig. 4.6 an ADPLL is shown with an UDC as a phase detector. The hold range covers the whole frequency range of the DCO from zero to the clock frequency.

This loop realization is still a serial type, as the numerator when it is in lock will be switched between two values that differ $\Delta P=1$. This loop is in fact a PFD loop with automatic center frequency adjustment. Loops with UDC's and RM's are known as 'calculating circuits' [Summers, 1974]. Analyzing them as a PLL gives a better understanding of the operating principles.

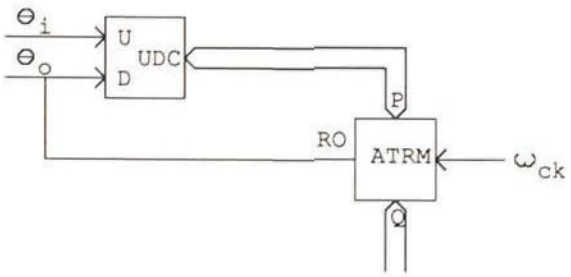


Fig. 4.6 ADPLL with up-down counter

Serial and parallel type: For the sake of completeness, the difference between serial and parallel type ADPLL's will be examined. A real parallel type DPLL, in which the phase error is expressed by a digital word rather than by a duty cycle signal has been realized by using a sampling phase detector. Fig. 4.7 shows an example in which the rate output of the ATRM is fed into the clock input of an n bit counter.

The output phase is then defined in steps of $2\pi/2^n$ for an output frequency represented by the MSB of the n bit counter. In the free running mode the counter contents change according to a sawtooth function. Digital phase samples are taken by the positive edges of the input signal with the help of a register that functions as a sample-and-hold phase detector. These phase samples, which are now in a numerical format (digital words), control the DCO and consequently the first-order loop is of the parallel type.

The hold range is equal to $\Delta\omega_H = \frac{P_0 + 2^n}{Q.2^n}.\omega_{ck}$, in which $Q \geq P_0 + 2^n$.

This 'digital phase sampling' technique was first proposed in 1980 to realize an arbitrarily-shaped phase detector transfer characteristic. Investigations showed [VanderCammen, 1982] that by using a ROM between the counter and the register with the required address-in/data-out code conversion, almost any phase transfer characteristic may be realized. Constant and variable digitally controlled phase shifts between input and output of the loop can be realized by incorporating a full adder. Cahn and

Leimer employed the phase sampling technique in an open-loop form, for carrier acquisition and coherent tracking in a processor of a spread-spectrum navigation receiver [Cahn/Leimer, 1980].

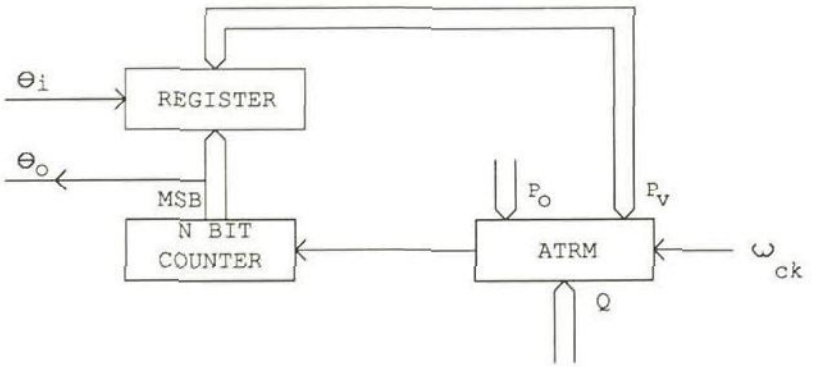


Fig. 4.7 Example of a parallel-type ADPLL

Concluding remarks: To determine the merits of the proposed ADPLL's based on modulated rate multiplication, several loops have been designed and realized for comparison with commercially available integrated ADPLL circuits. The design constraints of the proposed configuration with respect to operating ranges, are more flexible and the spectral purity is better especially close to the end of the hold range.

IV.2.B All-digital PLL IC xx297

This ADPLL circuit may be considered to be a serial type loop. Also here the phase detector produces a duty cycle proportional to the phase error. In this case the duty cycle controls a DCO which is based on the principle of repetitive phase shifting. A block diagram of a ADPLL based on this principle is given in Fig. 4.8.

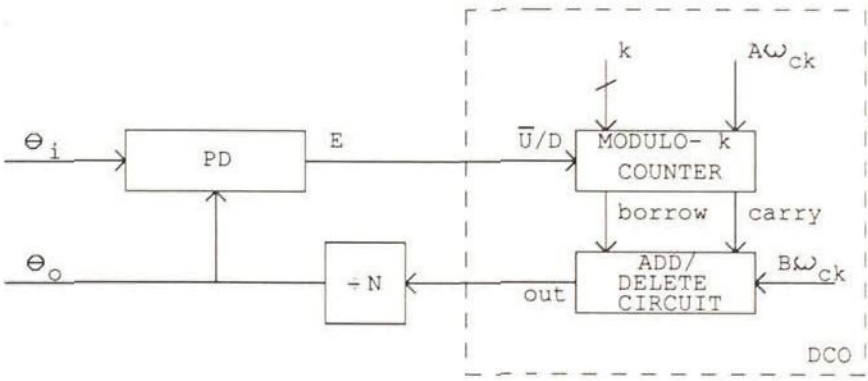


Fig. 4.8 ADPLL based on increment/decrement DCO principle

The duty cycle phase error E controls the counting of two up-counters, with programmable maximum capacity k, labeled as up-counter and down-counter. The duty cycle determines which counter is clocked with the external clock signal $A\omega_{ck}$. In case of overflow of one of the counters, a signal is generated that adds or deletes one half clock period of the same or another clock signal $B\omega_{ck}$. As we found in section IV.2.A, the phase shift steps are equal to $\pm\pi$ and the repetition difference-frequency is proportional to the phase error. The increment/decrement circuit operates together with the modulus-k counters as a DCO with a transfer factor $K_o = A\omega_{ck}/2k$.

When the ATRM is used as DCO, the phase error was added to a fixed value and converted into a frequency. When the combination of the modulus-k counters and the add/delete circuit is employed as DCO, the phase error is accumulated in the modulus-k counters and converted into a phase shifting frequency.

For a duty cycle of 0.5 the ATRM generates a frequency with a lower phase error value than the add/delete scheme. The k-counters give in each overall cycle time at least one retard and one advance command that (on the average) cancel each other. The momentary phase error may be large, however. In general this results in a larger spectral impurity.

IV.2.C All-digital Costas PLL and higher-order loops

Higher order loops: The behavior of the first order ADPLL's is equivalent to a first order continuous-time PLL. The noise bandwidth is determined by the loop gain, whereas the hold range is determined by both the maximum phase range and the loop gain. Hold range and noise bandwidth can therefore not be chosen independently. In order to create independent loop parameters a higher order ADPLL is needed.

The implementation of digital loop filters, that, in this case, would filter the duty cycle, is difficult. It is customary to create higher order ADPLL's by cascading first-order loops. Some dynamic properties are still determined by the 'first' first-order loop.

In section VI.11 a novel configuration for a second-order loop is presented. This configuration shows an almost identical behavior as the second-order type-2 continuous time PLL. The hold range may be designed independently of the noise bandwidth and the acquisition behavior is quite similar to a second-order loop with perfect integrator, except for the implied quantization effects.

Costas loop: The novel second-order ADPLL is perfectly suited for a Costas PLL carrier synchronizer and data demodulator for BPSK demodulation, because no static phase error exists in lock. In the section VI.11 also a new all-digital special phase detector is presented that is required for BPSK modulated carrier tracking.

This phase detector configuration is based on the simplified view on BPSK demodulation that, the loop gain of the normal, single loop PLL has to be inverted by the data synchronically. In combination with the divider of the loop, this operation has been performed in an elegant way.

The proposed loop can give information about the phase and frequency estimate of the input signal in a numerical format.

IV.3 AN IMPLEMENTATION INDEPENDENT MODEL FOR DIGITAL PLLs

The usual approach to DPLL modeling takes the continuous-time models as a starting point. The model to be proposed, is derived from the

essential DPLL quantities, i.e. the loop phase-quantization and the sample frequency or, the step size and the rate at which the output phase can change.

Lindsey and Chie distinguished in their survey four classes, depending on the implementation of the phase detector in the DPLL [Lindsey/-Chie, 1981]. Generally, the DPLL is modeled from a MAP-estimation point of view, resulting in stochastic equations that are solved by using the Markov-chain theory, Also the z-transform is used to analyze the acquisition behavior of the loop for various input transients. The complex models do not give much insight into the fundamental properties of the DPLL, such as loop step size and sampling frequency. These models do not tell the designer whether he can employ a DPLL. The model approach to be described here is intended to give an insight into the basic DPLL operation, and thus making the application limits of a DPLL explicit.

The DPLL is characterized by the fact, that the output phase can only change a discrete quantity of ε at discrete time intervals T. As usual a loop will be considered to be digital if either $\varepsilon \neq 0$ and/or $T \neq 0$.

We will restrict our analysis to DPLL's that can be seen as All-Digital (ADPLL). The input signal of the loop is a signal with a fixed amplitude, for example, as produced by a hard limiter, having a continuous phase and frequency. We will assume that the incoming signal is sampled at almost discrete time intervals in the phase detector. The phase of the signals is determined by a subtraction operation at certain time intervals, producing a duty cycle that represents the phase error of the loop.

The phase error is averaged in either the loop filter or in the DCO, depending on the implementation of the loop. This must be conceived as determining the average over a certain time interval. For 'phase' as a quantity this 'averaging over a certain time interval', produces consequently an average difference frequency, because frequency is $\Delta\phi/\Delta t$. So the phase error is converted to a frequency error by accumulating the phase error samples until one period can be generated.

From the input signal (phase as a quantity), with bandwidth B_i, the output phase θ_o is subtracted and (non uniformly) sampled at f_{si}, being the output frequency of the loop. In general this phase difference will be

quantized in steps ε of a cycle and accumulated with a frequency f_{sL}. This resembles delta modulation (Fig. 4.9).

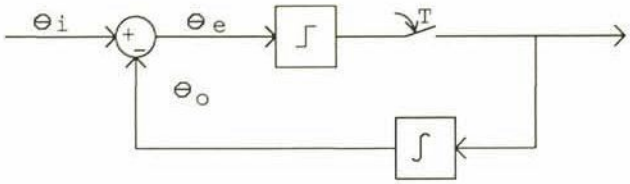


Fig. 4.9 Linear delta modulator

Preliminary experimental results show a noteworthy correspondence of the noise behavior of ADPLL's and the results from investigations of delta modulation with respect to the sampling frequency and the quantization step. These two fundamental aspects of the ADPLL determine the application properties.

This will be illustrated by examining the design formulas of the xx297 ADPLL as is shown in Fig. 4.8. With an XOR as a phase detector and a divider N, the following parameters can be derived for a first order loop:

- hold range $\Delta f_H = \frac{A f_{ck}}{2kN}$ [Hz]

- center frequency $f_c = \frac{B f_{ck}}{2N}$ [Hz]

- loop gain $K_v = \frac{2A f_{ck}}{kN}$ [rad/s]

In all expressions N is present in the denominator. This means that the phase has been quantized in steps of $2\pi/N$. One cannot straightforwardly determine what the sampling frequency of the loop will be.

The factor Af_{ck}/k in the loop gain expression represents the accumulation of the phase error. It is possible to keep the loop gain constant by decreasing A and k simultaneously. However, the phase error is then accumulated much slower and the fluctuations of the phase error cannot be tracked properly. The frequency Af_{ck} should be considered as the sampling frequency of the loop, which should be related to the input

frequency and bandwidth (sampling theorems). This is an important design conclusion, so far not mentioned in literature. This is especially important when first order loops are cascaded to obtain higher order ADPLL's.

Conclusions

The implementation of digitally controlled oscillators — and not of phase detectors as normally done in the literature — was used to distinguish DPLL configurations and thusly obtain more insight into the operation of ADPLL's.

Several new basic ADPLL configurations were presented and serial type and parallel type ADPLL's were defined on the basis of modulated rate multiplication.

A new configuration was proposed for a second-order ADPLL, that extends the application possibilities considerably by providing additional degrees of freedom for the design.

A novel all-digital quadrature loop configuration for implementing a Costas loop to be used for BPSK demodulation and carrier recovery was presented, which can also be applied with commercially available all-digital integrated PLL circuits.

An approach was started with an implementation-independent DPLL model, which resembles delta modulation. A noteworthy correspondence of the noise behavior of ADPLL's with results from delta modulation has already been shown in preliminary experiments.

CHAPTER V PLL DESIGN OVERVIEW

An overview will be given of the design questions and specifications that are related to the design and the implementation of phase-lock configurations. The topological approach to PLL design leads to a structured and hierarchical design strategy.

The design cycle is exemplified with common specifications for phase-lock configurations with use being made of a recently presented design-aid. Based on the input/output considerations of Chapter II additional questions have been formulated with respect to important application areas. The approach taken in Chapter II is summarized with respect to the specifications of main application areas.

This leads to a design strategy for PLL's that is based on the generalized design model of Chapter I and in which the extant design-aids can continue to be applied.

V.1 A PRIORI PLL DESIGN INFORMATION

In most cases the application of a PLL will not be dictated by the systems designer, but will be proposed by the electronics designer. The

specifications of the system designer must be carefully examined to find the simplest electronic implementation. Specifications and questions will guide the user by means of a checklist that contains items that must be analyzed before any attempt will be made to design the electronic realization.

V.1.A Specifications

Possible specifications will be presented as a checklist for main application areas. Each of these aspects can play an important role for the design and implementation. Without complete specifications, the PLL designer is unable to make the right choice of the configuration to be used.

Checklist phase-lock frequency synthesis e.g.:

- Output frequency range
- Output frequency resolution, number of channels
- Output signal spectral purity
  - spurious, Carrier-to-Spurious Ratio (CSR), dB, distance
  - phase noise, Carrier-to-Noise Ratio, ε dB/$\sqrt{Hz}$, distance
- Settling time, overshoot /channel /max, criterion $f < \chi$ Hz, $\phi < \vartheta^{\circ}$
- Modulation possibilities, with/without spectral purity demands
- Lock detection
- Power consumption

Checklist phase-lock signal processing e.g.:

- Modulator function,
- Frequency deviation,
- Phase deviation,
- Modulation frequency, -bandwidth
- Distortion

Checklist phase-lock signal tracking / carrier recovery e.g.:

- ☐ Input noise bandwidth
- ☐ Input frequency range
- ☐ Input signal modulation
  settling time, modulation/carrier tracking, distortion
- ☐ Input signal level, variations, dynamic range
- ☐ Input noise level
- ☐ Loop noise bandwidth, output variance, b.e.r.
- ☐ Tracking errors, type and order of loop
- ☐ Acquisition range, -time
- ☐ Lock detection

These specifications do imply the choice of a configuration. The designer will most likely choose a familiar topology and the component values to obtain an acceptable solution will be calculated. If a single loop is chosen on the basis of the main dynamic parameters ω_n and ζ, the dimensioning procedure can be guided through a questionnaire.

V.1.B Questions

This questionnaire is used in the dimensioning procedure of a fixed, single loop configuration to gather the specific values. An example of an interactive questionnaire for the utilization of an integrated PLL circuit is illustrated below.
Some additional remarks are given in italics.

Interactive design-questionnaire [Philips,1989]

- ☐ Give the input frequency of the PLL
  If FM modulated then give the mid frequency.
  (This is the center frequency of $2\Delta\omega_H$*)*

- ☐ Give expected maximum drift from mid frequency (in %).

- Do you wish a divider in the feedback ? Y/N.
  (This defines an input/output configuration)
  Do you want N to be variable ? Y/N. *(This defines a specific function)*
  Give value*(s)* for N. *(N_{ave})*

- Give VCO-center frequency f0 (= $N f_i$)
  Give 2fR *(= f_{max} - f_{min}, N times the total hold range $2\Delta\omega_H$)*

- Is the input modulated ? Y/N. *(This defines a specific function)*

- Give Vcc (in V).

- -Phase comparator type:
  1- PC1 *(XOR)*
  2- PC2 *(PFD)*
  3- PC3 (4046A only) *(SRFF)*
  4-

- -Filter type:
  1-Passive filter *(τ_2>0)*
  2-Active filter
  3-No filter
  4-Charge-Pump *(voltage-pump, passive filter)*

- -VCO type
  1- VCO 4046A/7046A
  2- *Other VCO type*

  Give VCO input voltage range (in V). *(=control voltage)*
  Give part-to-part spread (in %).

- 1-Set up overshoot and settling time.
  2-Set up zeta and settling time.
  Give value for zeta.
  Give value for settling time (in ms).

- Type of modulation:
  1 - frequency sinusoidal (FM)
  2 - frequency step (FSK)
  3 - phase sinusoidal (PM)
  4 - phase step (PSK)

- (default = 1), your value : 1 *(FM)*
  Give peak frequency deviation (in kHz).
  Give modulation frequency (in kHz).

  (default = 1), your value : 2 *(FSK)*
  Give peak frequency deviation (in kHz).
  Which of the following parameters do you want to set up ?
  1-Set up overshoot and settling time.
  2-Set up zeta and settling time.
  Give value for zeta.
  Give value for settling time (in ms).

  (default = 2), your value : 3 (PM)
  Give peak phase deviation (in degrees).
  Give modulation frequency (in kHz).

  (default = 3), your value : 4 *(PSK)*
  Give peak phase deviation (in degrees).
  (default = 9.000E+01), your value :
  Which of the following parameters do you want to set up ?
  1-Set up overshoot and settling time.
  2-Set up zeta and settling time.
  Give value for zeta.
  (default = 7.420E-01), your value :
  Give value for settling time (in ms).

Although the questions have a fixed order, it is possible to return to previous questions. The answers that are given may result in messages, warnings and indication of errors, resulting from certain alterations made

during a calculation, problems that may arise with the current values of parameters, or the fact that the loop will fail to operate with the current values of parameters, respectively. The final result is the following display of a 'result window' with the calculated component values for the voltage controlled oscillator, for the loop filter, and the dynamic loop properties.

```
                          INPUT PARAMETERS
PC      :  2      fin  (Hz) :  1.563E+04     Spread input freq.  (%) :  0.0
N       :  1.0    2fR  (Hz) :  1.563E+04     Part-to-part spread (%) :  0.0
Filter  :  2      f0   (Hz) :  1.563E+04     Vcc                (Volt) :  5.0

                       VCO and FILTER PARAMETERS
T1 (sec) :  6.3E-04        T2 (sec) :  3.6E-04        T3 (sec) :  3.7E-05
f1  (Hz) :  2.5E-03        f2  (Hz) :  4.4E+02        f3  (Hz) :  4.3E+03
R1 (Ohm) :  3.0E+04        R3 (Ohm) :  4.2E+02        R4 (Ohm) :  2.4E+02
R2 (Ohm) :  2.3E+05        C2 (Far) :  1.5E-06        C3 (Far) :  1.5E-07
C1 (Far) :  1.2E-08                                   Rp (Ohm) :  5.3E+05
                          DYNAMIC PARAMETERS
Wn/2π              (Hz) :  7.5E+02  pull-in time        (sec) :  7.1E-04
W_0dB/2π           (Hz)    1.4E+03  pull-in range       (Hz) :  7.8E+03
zeta                    :  0.71     pull-out range     (Hz) :  7.8E+03
overshoot          (%)  :  20.61    hold range         (Hz) :  7.8E+03
Kv                      :  1.4E+04  settling time      (sec) :  2.3E-04
Winput/W_0dB            :  11.3     lock-in range      (Hz) :  6.7E+03
phasemargin with C3 (deg) :  56     ripple suppr. with C3 (dB) : -56
           without C3 (deg) :  72                 without C3 (dB) : -56
W-3dB/2π closed loop (Hz) :  1.5E+03
                                                  Philips Components
```

OPTIMIZE ? (Y/N): Y

If this option is chosen, a window will be given for choosing loop properties which can be changed. It should be noted that explanations about the interrelations and dependency must be given in each modification

display. If one decides to try another loop filter or phase detector, the procedure has to be repeated.

```
IF YOU WANT TO OPTIMIZE, CHOOSE AN OPTION :
1  - VCO frequency range (2fR)
2  - hold range
3  - phase margin
4  - ripple suppression
5  - settling time
6  - lock-in range
7  - pull-in time
8  - pull-in range
9  - pull-out range
10 - set own values for filter components
11 - damping ratio (zeta)
12 - natural frequency (Wn)
13 - W_0dB (open loop)
14 - overshoot
15 - W-3dB (closed loop)
16 - No changes
```

The user obtains the results of the calculations by means of a display of the loop properties in the 'result window' and can try to find an acceptable set of specifications by trial and error.

V.1.C Additional questions

The preceding questions do not emphasize the function of the PLL in a specific application. Therefore additional questions have been formulated, on the basis of the examination of the input/output relations of the PLL as a black box (Chapter II).

- Input conditions with noise?
  - Give input noise bandwidth B_i($\neq$ input frequency range!) and SNR_i or signal power and spectral noise power density N_o

- Give loop noise bandwidth B_L or $\overline{\theta_{no}^2}$

- Give ripple suppression for unwanted VCO side bands or distortion

- Modulation in loop?
  - FM? Give modulation index, or modulation frequency μ and frequency deviation $\Delta\omega$. (N.B. $\omega_n << \mu$).
  - FSK? Give frequency step, steepness, data rate
  - PM? Give modulation index, or modulation frequency μ and phase deviation $\Delta\phi$. (N.B. $\omega_n >> \mu$).
  - PSK? Give phase step, steepness, data rate

  * For distortion specifications examine PD-type
  * If modulation frequency μ does not match ω_n, use combined FM/PM.†
  * If BPSK use balanced modulator or EXOR instead of PLL.

- Demodulation in loop?
  - FM? Give modulation index, or modulation frequency μ and frequency deviation $\Delta\omega$. (N.B. $\omega_n >> \mu$).
  - FSK? Give frequency step, steepness, data rate
  - PM? Give modulation index, or modulation frequency μ and phase deviation $\Delta\phi$. (N.B. $\omega_n << \mu$).
  - PSK? Give phase step, steepness, data rate

  * If distortion specifications, examine PD-type or linearity K_o

For the I/O function with respect to measurement in the single loop PLL, the questioning procedure can be extended by adding questions about post-detection filter properties etc.

V.2 DESIGN PROCEDURE CHARTS

From the a priori design information (the specifications and design questions), the designer may follow any route for the specific analysis of

---

† *see also [Underhill/Scott,1979]*

the specifications and questions.

In our view, however, the simplest model of the PLL, the linear phase model, has to be used first to examine specifications of an application with respect to the required small-signal dynamic properties. Then the non-linear model should be used to investigate specifications in relation to the operating ranges. If this standard analysis fails to meet certain design aims, the more sophisticated loop implementations must be tried. This path is summarized in the following under a), b) and c). The analysis starts with a simple PLL model and ends with complex, multi-detector loops.

a) Fundamental linear design

□ *linear, small signal, time-continuous;* the specifications must be met with respect to the following dynamic properties:
- Settling time, overshoot
- Bandwidth, order, type

b) Non-linear design

□ *standard non linear for operating ranges;* the requirements must be fulfilled with respect to one or more of the operational limits:

- hold range
- max. phase step
- max. frequency step, pull-out range
- max. frequency sweep
- pull-in range, pull-in time
- lock-in range
- noise dynamic range
- phase detector ripple
- spurious suppression

c) Advanced design

- *high performance single loops*

Phase-and-Frequency Detectors (PFD) with or without Charge-Pump widen the phase range, speed up frequency acquisition and minimize static phase error in comparison to the design with standard phase detectors.

- *multi-detector loops*

When lock detection is required, cycle slip detection can be adequate under conditions of low noise. A quadrature topology may be necessary because of the structure of the input signal.

- *specific design goals*

In Chapter III.3 special approaches were given for design compromises for the tracking and acquisition mode, the switching speed and spurious suppression, and for acquisition under conditions of noise.

A closer look at the a priori design information and at the total design procedure results in a general design strategy, in which every design aspect has a *hierarchical* place. This hierarchical design procedure may be seen as the final result of our approach. It shows similarity to the investigations of Chapter III.3. There the approach was already illustrated in a simple form.

V.3 PLL DESIGN STRATEGY

The above mentioned specifications, questions, and procedures were employed to present the general PLL design strategy. The following scheme can be used for a quick determining of the feasibility.

PLL design

- Define function of PLL, I/O topology,
- Define loop bandwidth, order/type,
- Define K_d and K_o, choose loop filter,
- Verify operating ranges, ripple/spurious, time-continuity,
- Extend ordinary loop, if necessary.

In more detail, the design scheme can be divided into the following steps:

- DEFINE FUNCTION OF PLL, I/0 TOPOLOGY,
  see I/O tables of Chapter II.

- DEFINE LOOP BANDWIDTH, ORDER/TYPE, preliminary on the base of the second-order loop design formulas of the linear phase model,
  see noise bandwidth, modulation frequency or settling time/overshoot.
  If more requirements are given, they can be dealt with in the verification step, in which operating conditions will be examined.

- ANALYZE PHASE DETECTOR SIGNALS,
  (frequency range, amplitude, noise, required phase range)
  one or both signals can be a switched waveform (binary),
  i.e input limiter permitted/required?
  sequential phase detector permitted?
  see noise/clicks (III.3.C)
  phase detector ripple

- CHOOSE PHASE DETECTOR TOPOLOGY
  see sections II.2 and III.1

- DEFINE K_d and K_o,
  (from preliminary orders of magnitude of input signal frequency, amplitude, supply and control voltage range)

- CHOOSE ULTIMATE LOOP FILTER TOPOLOGY
  for active and passive loop filter, see noise bandwidth, time and frequency responses of section II.1

- DIMENSIONING OF THE LOOP FILTER TIME CONSTANTS τ_1 AND τ_2,
  see section II.1

- VERIFY OPERATING RANGES, RIPPLE/SPURIOUS, TIME-CONTINUITY,
  see non-linear model of section II.2.

- **IF ALL REQUIREMENTS HAVE BEEN MET, THEN END, ELSE**

- CHOOSE ADDITIONAL PERIPHERAL CIRCUITS, ANOTHER LOOP FILTER, PHASE DETECTOR OR MULTI-DETECTOR TOPOLOGY.
  see sections III.2, III.3, and chapter IV.

- END Decide whether or not a standard PLL IC can be used.

Discussion: Let us briefly examine the steps of the analysis. This general PLL design strategy starts with a part of the specifications, the dynamic parameters ω_n and ζ, and ends in examining the operational limits of an equivalent, single loop. When the order of magnitude of K_o and K_d has been established, the operating ranges can be preliminary calculated, and the loop filter and the phase detector can be chosen. Most likely, conflicting requirements will remain from the acquisition and tracking requirements (with or without noise), or from the settling time, spurious suppression, and VCO noise attenuation requirements. Several remarks need to be made at this point.

Apparently, the analysis of the phase detector signals is an important step. It is to be expected that the strategy can be widened for application-specific choices of the phase detector. The calculations in the steps of this strategy will be simplified by using existing design-aids.

However, the balance of the relative importance of the specifications has not yet been incorporated. From the many specification requirements, the designer makes a choice in practice, which aspects are to be selected as the most important. Furthermore, the sequence of the questions is not fixed, but depends on the requirements of a specific application. Very often the specifications of an application will not be completely defined, and consequently the designer must estimate the relevance of their properties.

One might say that the criterion with the smallest degree of freedom separates the first design attempt from the total multi-dimensional design space. If this is the case the uncertainty bounds for the PLL properties must already be known explicitly. It is only from experience that a designer chooses a topology, which will probably meet the most important requirements. The application of the PLL for a specific function, specifies a set of requirements generally. The criterion with the smallest degree of freedom is not necessarily equal to the most important requirement.

In view of these considerations, the conclusion may be drawn that particularly, the design steps from specifications to configuration will be enhanced by the future development of 'expert system' fashioned programs. Many questions can be handled in a variable sequence, and justified estimations can be made for conditions with incomplete specifications.

V.4 EXAMPLES OF PLL DESIGN APPROACHES

In the course of time specific PLL design-aids have been published. They characteristic of either analysis or dimensioning algorithms.These results can be incorporated into the PLL design strategy since these are complementary. Therefore, a brief summary will be given.

□ Several articles describe specific dimensioning problems of PLL's particularly for phase-lock frequency synthesis.

Przedpelski described programmable calculator programs for stability analysis, optimization (tradeoffs between spurious and VCO noise reduction), and additional filtering for spurious suppression of type-3, third-order PLL's in [Przedpelski, 1978a, 1978b, and 1979] respectively.

Fadrhons gave a stability analysis program for a programmable calculator that can be utilized to investigate the effects of various loop filter tradeoffs for frequency synthesis. [Fadrhons, 1980] As special features of his program, he incorporated parasitic effects such as limited gain and bandwidth of active filters, VCO modulation bandwidth, and the effects of current-source charge-pumps.

Przedpelski calculated the noise spectral density and short-term frequency stability in a phase-lock synthesizer and he varied parameters to trade off the noise/functional performance requirements.[Przedpelski, 1981]. As an example a fifth-order loop was analyzed to determine the noise.

□ The first flow diagram for designing PLL's was published by Best. [Best, 1984, p.112-3]. The crucial (topological) step in the design process of choosing a configuration was not incorporated. Moreover he made an unjustified distinction between linear and digital phase detectors or loops. PLL's with sinusoidal phase detectors were considered as linear loops. A better distinction was proposed by Gardner, who made a distinction between loops with multiplicative and those with sequential phase detectors [Gardner,1979].

□ Dimensioning programs made by Przedpelski were published in [Rhode,-1983]. In the same book a BASIC program listing is given to analyze the stability of a third-order type 2 loop.

□ For HCMOS integrated PLL circuits of the series 74 HC/HCT 4046 A & 74 HC/HCT 7046 A, a design diskette was released by Philips Components, Nijmegen [Philips,1989]. In the latter stage of the development contributions were made by the author [DenDulk, 1989].

Unfortunately, the final version (1.1) can only deal with a limited part of the PLL applications for these circuits. For commercial reasons only the 'high-gain' dimensioning of the PLL with the standard digital phase detectors is well covered. Real Charge-Pump loop filters are mainly approximated and no applications are given in which the PLL IC can be used in a topology with other peripheral circuits. The approach is not as yet very user-friendly and can be characterized as an interesting, but still incompletely defined first attempt. The user should be protected from circular reasoning and the utilization of extended configurations should be better defined. Further investigations should result in a more structured design approach, together with new proposals for integrated circuits in the PLL field.

This recent development shows that commercial interest in this field is indeed growing.

CHAPTER VI CASE STUDIES

Introduction

The approach to systematic design of phase-lock loops for different applications was based on the PLL analysis, modeling, questions and specifications, acquired in several case-studies. This chapter consists of the publications of these case-studies.

First operating conditions will be examined in sections VI.1 and VI.2. Second, proposals will be given for circuit implementation with improved PLL performance based on cycle-slip detection (sections VI.3 to VI.7). The rate multiplier implementation appears to be very useful in frequency synthesis and for all-digital phase-lock loop implementation (section VI.8).

Studies of the digital implementation of the phase-lock principle will be given in sections VI.9 to VI.11. Finally, the investigations of a charge-pump PLL that can be used in the presence of excessive input noise, yield a new method and circuit implementation of multiplicative phase detection (section VI.12).

PHASE-LOCK-LOOP OPERATING RANGES MEASUREMENT

Indexing terms: Signal processing, Phase-lock loops, Spectrum analysers

A measurement method is presented that quickly displays the operating ranges of phase-lock loops (PLLs) and acquisition aids under various input conditions such as noise and interference. The PLL measurement set-up is based on the use of normally available spectrum analyser/tracking generator equipment rather than on the common display of the control voltage of the oscillator. It is shown that in case of a narrow-band PLL the spectrum-analyser display can be more easily interpreted than the control-voltage display.

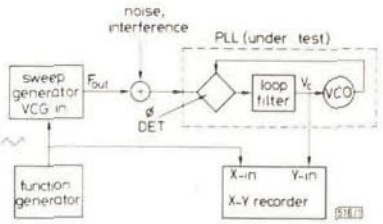


Fig. 1 *Measurement set-up commonly used*

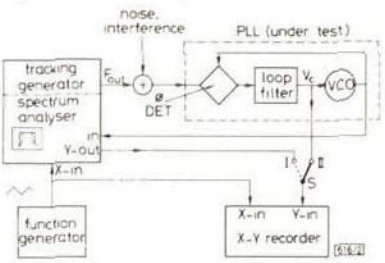


Fig. 2 *Selective measurement set-up*

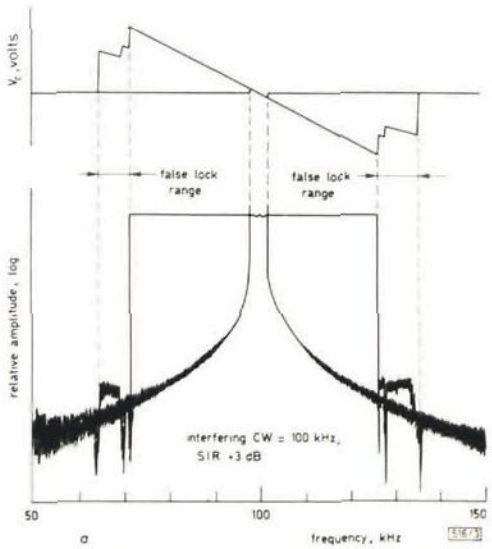


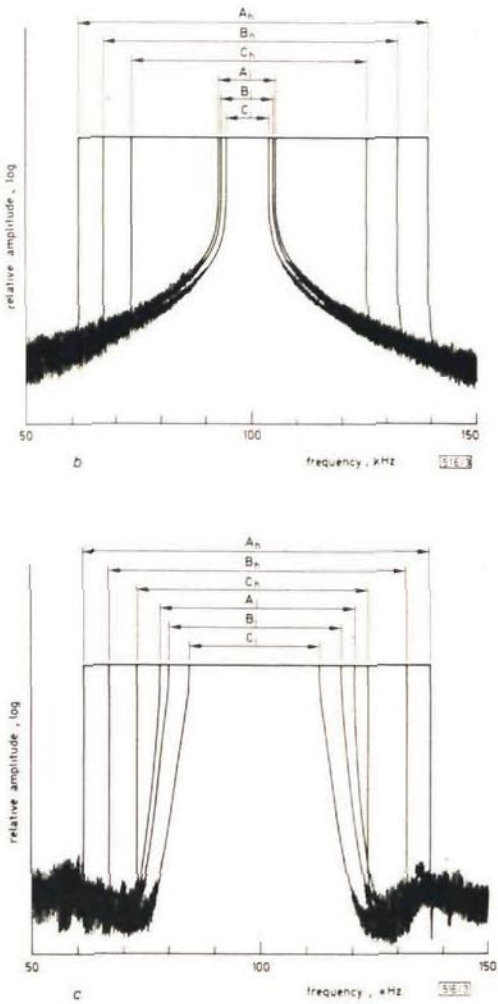
Fig. 3 *Examples of measurement results. Control voltage display and spectrum analyser display of:*

a Lock range and hold-in range in case of an interfering CW signal
b Lock range and hold-in range for different signal/noise ratios
A: S/N ≫ +30 dB
B: S/N = +3 dB
C: S/N = −3 dB
c Operating range of an acquisition-aided PLL under the same condition as in *b*

Introduction: Phase-lock loops (PLLs) are used widely in modern communications, radar, telemetry, command, time and frequency control, and instrumentation systems. Because of the importance of the application of PLLs, there has been a considerable amount of work done in this area. There are several books[1-3] which look into the analysis, design and application of the PLL in one way or another. However, little attention has been paid to the measurement of the basic PLL properties. The primary reason for this is that the PLL applications were traditionally left to the above areas. Integrated-circuit technology, however, has spawned a number of monolithic circuits,[4-6] including low-power medium-scale integration (MSI) and large-scale integration (LSI) chips, that have and will stimulate PLL applications in many other areas.

The design engineer has to optimise one or more of the following design goals:[1] static phase error; noise bandwidth; hold-in range; lock-in range; pull-in range; pull-in time. The noise bandwidth has a strong impact on nearly all of the other properties. The requirements of fast signal acquisition and good synchronous-mode performance are in conflict. The designer must find as good a compromise between both requirements as possible, although he can decide to use some form of acquisition-aid circuitry.

The acquisition range, however, depends strongly on both the input SNR conditions and the electronic implementation. Measurements in this area are very extensive, owing to the number of parameters that influence the PLL performance: noise bandwidth, acquisition-aid bandwidth, signal/noise



ratio, signal/interference ratio, parasitic PLL pole location, parasitic acquisition-aid pole location, VCO centre frequency, loop-filter implementation, VCO modulation bandwidth, phase-detector implementation etc.

Measurement set-up: The pull-in performance of a PLL, in the case of disturbing input signals such as noise and interference, is hardly predictable owing to the nonlinear PLL behaviour and the earlier-mentioned parasitic elements. The performance nearly always has to be measured. Moreover, these measurements provide insight into the relations between the theoretical PLL models and the electronic implementation. A measurement set-up commonly used to determine the PLL operating ranges is shown in Fig. 1. The averaged control voltage of the VCO is plotted as a function of the input frequency. In the case of additional input noise and interference the results are hard to interpret because the control-voltage variation is too small and/or too much disturbed.

The interpretation is made much easier if selective measurement equipment is added. It is possible to use a low-index FM-modulated signal source as input frequency and selectively measure the control voltage of the oscillator. However, the frequency modulation can disturb the measurement because the PLL cannot distinguish it from the input noise. In Fig. 2 a measurement set-up is shown that does deliver the right information. The tracking generator generates the input frequency, and the spectrum-analyser section selectively monitors the output frequency of the PLL.

By using a plot of the control voltage as well, all information about the operating ranges under various conditions can be found if some restrictions are borne in mind.

As is known from the PLL theory, restrictions have to be made with respect to the maximum sweep speed. This has to be smaller than $\frac{1}{2}\omega_n^2$ (ω_n = natural loop frequency) because otherwise the PLL cannot acquire the input signal. In the case of acquisition-aid circuitry it is possible to obtain some information about the order of the 'main time constant' of the acquisition aid by varying the sweep speed. The bandwidth of the spectrum-analyser section can play a governing role in these experiments. It should be noted that, because the main carrier component of the VCO signal is measured, difficulties can arise over the right bandwidth choice. It is beyond the scope of this letter to describe experimental measurement methods further than that given in the following Section.

Experimental results: These measurements are performed with sweep speeds smaller than half the squared natural loop frequency and with a spectrum-analyser bandwidth much smaller than the inverse sweep speed. In Fig. 3 some results are given of measurements on a PLL with a passive filter under various operating conditions. In Fig. 3*a* the lock-in range and the hold-in range are given in case of an interfering signal of −3 dB. These results are obtained from the control-voltage output and from the spectrum-analyser display. The same PLL is measured under various signal/noise ratios. The operating ranges are given in Fig. 3*b*. It is remarkable, but the conclusion that can be drawn from Figs. 3*a* and *b* is that interference affects the pull-in range more than noise does.

In Fig. 3*c* the measurement results are given for a PLL with some form of acquisition-aid circuitry under the same SNRs as in Fig. 3*b*. We see that the pull-in range is considerably enlarged.

Conclusions: A measurement method for quickly determining the operating ranges of a PLL under various input conditions is given. This method is applicable with commonly available laboratory equipment measuring the performance of PLLs and acquisition aids. However, the acquisition time, an important design parameter, cannot be measured with the proposed method, although an indication can be obtained by varying the sweep speed and the spectrum-analyser bandwidth.

Further information on the PLL performance can possibly be extracted with the proposed method by displaying the spectrum-analyser output in the linear mode, because VCO modulation voltage affects the magnitude of the main carrier component. It is left to the reader to explore the proposed method further.

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FALSE-LOCK SOURCES IN CHARGE-PUMP PHASE-LOCK LOOPS

Indexing terms: Circuit theory and design, Phase-locked loops

In spite of assumptions to the contrary, charge-pump phase-lock loops (CPPLL) with a phase-and-frequency detector can, in practice, stay in false lock, in the case of certain electronic implementations. False-lock sources are analysed for a CPPLL with a passive filter, and as a result design rules are given to prevent CPPLLs from false locking.

Introduction: Nowadays a special kind of phase detector, the phase-and-frequency detector (PFD), is often used in PLLs in integrated circuits. Together with a so-called charge-pump (CP), often implemented in the same circuit, a charge-pump phase-lock loop (CPPLL) (Fig. 1) can be built which has advantages for certain applications: a pull-in range equal to the hold-in range and a static phase error of almost zero, even with the use of a passive filter. It is commonly taken for granted that a CPPLL cannot be in false lock, but in practice this has proved not be be the case. Tal and Whitaker[1] have analysed this effect, but their results are limited to a very special configuration; this letter provides a more general treatment of the problem.

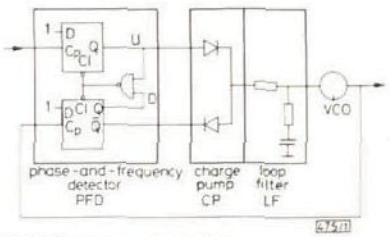

Fig. 1 *Charge-pump phase-lock loop*

False-lock sources: Gardner[2] has analysed the behaviour of a CPPLL as a time-continuous linearised model, assuming the output current of the CP to be $I_p \operatorname{sgn} \theta_e$ during the active state of the PFD, where I_p is fixed value of the pump current and θ_e is the phase error between the input signals at the beginning of an active period. In this letter the behaviour of the PFD with CP is discussed according to the model of Fig. 2, in which all possible shunt and source resistances which can be of influence in the implementation are incorporated.

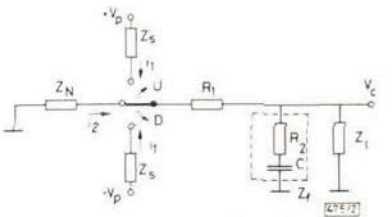

Fig. 2 *Model of charge pump and loop filter*

To allow a linearised, time-continuous treatment of the PFD behaviour, the ripple due to the resistor R_2 in Z_t is *ignored. The loop bandwidth is small compared to the signal* frequency, so that the active state current i_1 and the neutral state current i_2 of the filter capacitor C are also asumed to be time continuous when the loop is locked. Then the average active period $\bar{T}_1$ and the average neutral period $\bar{T}_2$ are related as

$$i_1 \bar{T}_1 = i_2 \bar{T}_2 \tag{1}$$

The phase error θ_e can be expressed as

$$\theta_e = \frac{T_1}{T_1 + T_2} 2\pi \tag{2}$$

so

$$\theta_e = 2\pi (1 + i_1/i_2) \quad \text{rad} \tag{3}$$

To use this result for false-lock determination it is necessary to take a closer look at the PFD transfer function in the case of a *frequency difference.*

A frequency difference between the two input signals can be seen as a continuous accumulating positive or negative phase error. This results in the phase-transfer characteristic passing through one of two directions, as is shown in Fig. 3a.[3]

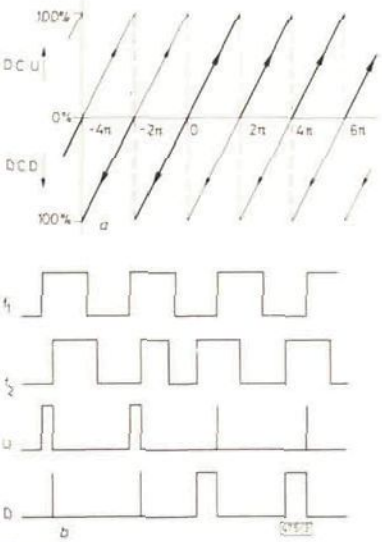

Fig. 3
a Transfer function
b Waveform examples of phase-and-frequency detector (PFD)

Consequently, the duty cycle of the output signal of the PFD in this case is either greater than or equal to 50%.[3]

This also implies, in a normal locking loop, that false locking can occur when

$$\theta_e \geq \pi \quad \text{rad} \tag{4}$$

From eqns. 3 and 4 it follows that $i_1 \leq i_2$.

For the model of Fig. 2 this implies in terms of VCO control voltage that if

$$|V_c| > V_p \{1 + (R_1 + Z_S)/(R_1 + Z_N) + 2(R_1 + Z_S)/Z_t\} \tag{5}$$

false locking can occur, on account of the shunt resistances. If a configuration is used with $Z_N \to 0$,[1] this implies that false locking will take place if $|V_c| \geq V_p 2$. Thus, for designing a false-lock-free loop, one has to make Z_S small compared to R_1

and Z_N has to be large compared to R_1. The input impedance Z_I of the VCO can be easily made very large.

A second false-lock source is created by the switch-off pulses of the PFD (Fig. 3*b*). During the internal propagation delay, labelled τ_p, both the U (up) and D (down) outputs are simultaneously active. This forces the output of the CP to a fixed voltage during τ_p, as long as the switches in the CP are fast enough. This is the case in an often-used PLL-IC such as the MC4044; but the 4046, a CMOS PLL-IC, has got two complementary MOS-transistors as output-switches, which are probably too slow to respond to the switch-off pulses. These switch-off pulses cause a phase error by discharging the filter capacitor C. Assuming identical switches in the CP, the output is forced to zero volts during τ_p and is active during $T_1 = \theta_e T/2\pi$.

With the model of Fig. 2, eqn. 4 and also under the condition $Z_N \to 0$ during τ_p and $Z_N \to \infty$ during the rest of the period, false locking can take place when $f \geq (V_p - V_c)/2V_c\tau_p$.

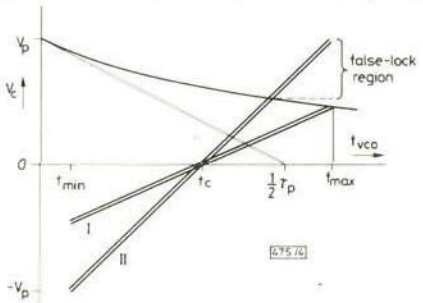

Fig. 4 *Voltage/frequency characteristics for determining false lock due to switch-off pulses*

I: high modulation sensitivity K_0
II: low K_0

By using the voltage/frequency characteristics of the VCO, the false-lock range can easily be displayed. When a loop has to be designed to operate at high frequencies, a high modulation sensitivity K of the VCO is necessary. In Fig. 4 it is shown how a too small VCO-gain will give rise to false locking at the higher frequencies (see the voltage/frequency characteristic II in Fig. 4). An active filter can also be used, but then, to obtain a discharge current as small as possible, care must be taken to make the switches symmetrical.

Experimental results: To verify the foregoing, we built two loops: one for measuring the influence of the parasitic impedance Z_N and one for studying false-locking due to the delay time τ_p. The loops are realised with a PFD built up by logic TTL-blocks; two MOS switches are used as a charge pump. For studying the influence of Z_N, an adjustable resistor is connected to zero volts during the neutral state. The reference frequency is slowly swept and the VCO voltage is examined to see false locking appear. Fig. 5*a* shows the results with $Z_N \to 0$ and $Z_N \to \infty$ (dotted line). It can be seen that false locking takes place for $|V_c| \geq V_p/2$.

For studying τ_p we forced the delay time to be longer by clearing the flip-flops of the PFD (see Fig. 1) by two monostable multivibrators. Using an input frequency of 200 kHz, locking of the loop with $\tau_p = 0{\cdot}5$ μs (dotted line) and $\tau_p = 2$ μs is also shown in Fig. 5*b*. We see that the internal delay can considerably influence the false-lock region. To prevent false locks, phase-and-frequency detectors without anticoincidence circuits can only be used safely far below their logical speed.

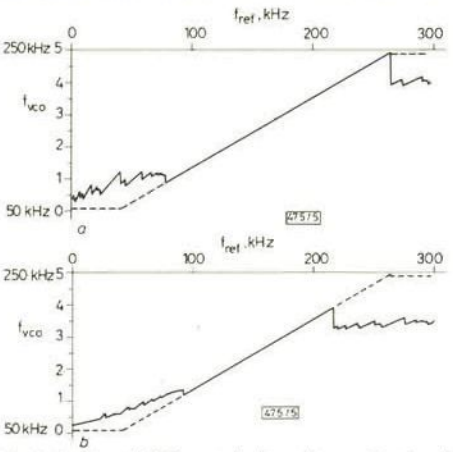

Fig. 5 *Experimental VCO control voltage plots as a function of input frequency sweep*

a False lock due to finite source impedance
b False lock due to switch-off pulse width

Conclusions: In this letter the important influence of such parasitic effects as shunt resistance and switch-off pulses on false locking, which is modelled as unwanted discharging of the filter of a CPPLL, is shown. If these effects are taken into account in the loop design, a second-order phase-lock loop having superior acquisition features can be built by using a passive filter. Its behaviour can be fully analysed according to Gardner's time-discrete analysis.[2]

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DIGITAL PLL LOCK-DETECTION CIRCUIT

Indexing terms: Phase locked loops, Detector circuits, Digital circuits

A digital lock detection circuit is described which can be used in combination with all known sequential phase detectors. The principle of operation is based on the detection of cycle slips, which is one of the possible unlock definitions of a PLL. Therefore definitions of phaselock are reviewed. The proposed circuit acts also in combination with the built-in phase detectors of a widely used PLL integrated circuit as a reliable lock detector.

Introduction: Phase-lock loops (PLLs) are widely used in modern communications, radar, telemetry, command, timing and frequency control, and instrumentation systems. There are several books,[1-3] which look into the analysis and the design of the PLL in one way or another. However, little attention has been paid to the implementation of the electronic circuitry, especially for a major design compromise of the PLL: considerations for the synchronous and acquisition modes.

A method to separate the acquisition mode and the synchronous mode is the application of the adaptive phase comparator.[4-6] In many application areas the implementation of this sequential phase detector is not straightforward. This is partly due to the lack of a suitable definition of the locked, synchronous state of the PLL and partly by the various demands on the properties of the auxiliary circuits. One has to distinguish circuits that detect the unlocked state and circuits that support the autoacquisition of the PLL for various application areas. Also, the circuit complexity has to be given attention. Particularly for the design of general-purpose PLL integrated circuits, the versatility of lock detection and acquisition-aiding circuits is of crucial importance.

In this letter a new digital lock detection circuit is proposed that can easily be incorporated into an integrated PLL circuit.

Definitions of phaselock: The purpose of lock detection is to give the state of the PLL and the validity of the output information and/or to deliver out-of-lock rate information to switch the bandwidth of the PLL. Generally, the design of a lock detection circuit depends heavily on the definition of phaselock. In Fig. 1 the block diagram is given for a PLL with

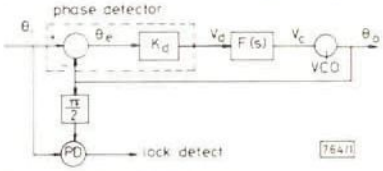

Fig. 1 *General PLL block diagram*

the most important signal names. Definitions of phaselock and the related lock detection circuits are based on:

(i) the time derivative $d\theta_e/dt$ and the noise bandwidth B_L: detectable by measuring the voltage across the 'zero' resistor in the loop filter

(ii) the average value and the variance of the phase error: detectable by an extra quadrature phase detector

(iii) Cycle slips: detectable by means of observing the periodicity of the phase detector output signal v_d (beat-note).

Each of the above-mentioned definitions is used in different application areas, and mostly implemented with complex special purpose analogue or mixed analogue/digital circuits. A lock-detector circuit which can be applied in a digital circuitry environment is found in the general purpose CMOS integrated circuit 4046.

Lock detection in a standard PLL IC: For the CMOS general-purpose PLL IC 4046 data sheets claim that lock detection is possible by using the so-called 'phase pulses'. In Fig. 2 the

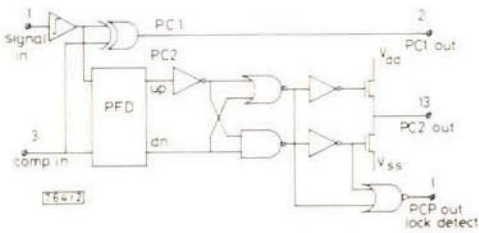

Fig. 2 *Extended block diagram (PD part) of general-purpose PLL IC*

extended block diagram is given of the phase detector circuitry of this component. For those who are not familiar with the three-state phase-and-frequency detector (PFD), the phase pulses on PCP can be thought of as simply the addition of both the pulses of an up S/R flip-flop phase detector and a down S/R flip-flop phase detector. They deliver information about the momentary positive and negative phase error in the form of the pulsewidths.

Discrimination of the widths of the phase pulses alone can give some information about the momentary phase differences, but does not give a reliable lock-detection criterion. Also, this method is strongly dependent on the input frequency and the static phase error of the loop. Of the above-mentioned definitions of phaselock only some form of (ii) can be approximated. The phase pulse energy content is averaged by a filter and the resulting DC level is used by a Schmitt trigger to give out-of-lock indication. One IC manufacturer has added this circuitry to the standard IC version in the 74HC/HCT7046A.

However, fully digitally implemented lock detection can be achieved by detecting cycle slips (CS) in the loop. Cycle slip occurrence used as definition of phaselock is given by Gardner (Reference 1, Chapt. 6) as an important phenomenon to determine the nonlinear behaviour of PLLs, and can be easily implemented in general purpose PLL ICs.

Proposed lock detector circuits: In Fig. 3 an equivalent circuit[8,9] of a sequential PFD is given as is applied in the 4046

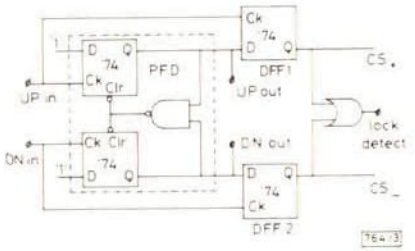

Fig. 3 *Proposed circuit as extension of common phase-and-frequency detector*

and as is available as a single IC,[10] with the proposed digital circuitry to detect cycle slips easily. A cycle slip occurs when two successive active edges are applied to one of the two inputs of a sequential PD. In DFF1 the information of the positive cycle slip (CS_+) is present and in DFF2 a negative cycle slip (CS_-). For the PLL IC of Fig. 2 the same operation can be realised by connecting DFF1 directly and DFF2 via an inverter to PCPout. The proposed circuit delivers out-of-lock information that is independent of the static phase error. At the same time the output pulsewidth is always greater than or equal to the period time of the input signal.

The statistics of cycle slip occurrence play an important role in the nonlinear behaviour of PLLs, or, in other words, determine the nearly unlocked state of the PLL. To get exact unlock information the given method can be easily extended by cascading the cycle slip DFFs. The contents of the thus created up (CS_+) and down (CS_-) cycle slip registers can be inspected and conclusions about the synchronous state of the PLL can be determined.

Conclusion: A simple digital lock detection circuit is given that can be used to detect the unlock state of a PLL. It uses a sequential phase detector, such as the S/R flip-flop phase detector or the three-state phase-and-frequency detector.

For the commonly used standard PLL IC 4046 the proposed circuit can also detect unlock in the case of using the other (multiplying) XOR-phase detector, because the occurrence of cycle slips is used as a definition of phaselock. This is probably the most useful definition of phaselock because cycle-slipping certainly indicates that the PLL is sometimes out-of-lock and definitely gives a situation in which the common linear approximated PLL model is not valid.

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Improved Phase-Locked Loop Performance with Adaptive Phase Comparators

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A major problem in phase-locked loop (PLL) design is to meet the requirements of both fast signal acquisition and good synchronous mode performance. This relation is reviewed for different types of phase comparators. As a result a new phase-and-frequency comparator is proposed. This comparator is based on an up-down counter principle and can be considered as an adaptive acquisition control circuit. The analysis of a PLL with the proposed phase comparator is based on an exact calculation method for the pull-in time. It is shown that fast signal acquisition is possible without affecting the filtering properties of the loop. Experimental results are given of the acquisition behavior of a second-order type-2 loop which show a good correspondence with the theoretical analysis.

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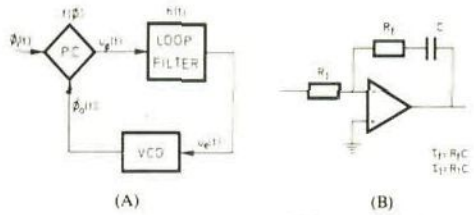
I. INTRODUCTION

Digital phase comparators (PC) have found wide application in phase-locked loop (PLL) configurations in frequency synthesizers [1-5], in synchronizing digital signals [6-8], and in motor speed-control systems [9, 10]. The use of digital circuits offers an easy way to realize phase comparators [11-12]. Several authors have described the performance of PLLs with digital phase comparators, but little attention has been paid to the separation of the two basic operation modes of the PLL, the synchronous (filtering) mode, and the acquisition mode. Byrne [13] and Goldstein [14] have analyzed the properties of PLLs with a sawtooth phase comparator, which is realized with a reset/set flip flop flip-flop. Compared to the use of a sinusoidal PC, this device delivers a better pull-in performance of the loop because of the full linear range. The acquisition properties, however, are still limited by the periodic nature of the transfer function of the sawtooth PC. A considerable number of papers on the PLL subject deals with the acquisition and pull-in subject [13-17].

This problem can be relieved by employing frequency acquisition aids such as frequency sweep, frequency discrimination [18-23], or feed-forward control [24]. However, the acquisition aids require much additional hardware, and feed-forward control assumes that a priori knowledge of the disturbance is available. Nearly all papers describe aided-PLLs with arbitrary periodic phase comparators. Oberst [25] has shown that a digital phase comparator can easily be modified into a phase-and-frequency comparator (PFC) by adding few logic gates, thus resulting in a nonperiodic, but repetitive transfer function. In his paper he summarized the implementation of several pulse-type phase comparators and phase-and-frequency comparators. Several other authors described phase-and-frequency comparators [25-31]. They are available in several versions as a single-chip integrated circuit [8, 27]. These PFCs make it possible to aid frequency acquisition without additional circuitry. The PLL acquisition performance with phase-and-frequency comparators is stated to be improved significantly.

However, no full separation of the two basic operation modes of the PLL can be realized. Only the sign of the frequency difference during acquisition is added; the maximum obtainable control voltage is still defined by filtering parameters. The requirements for both fast signal acquisition and good synchronous mode performance are in conflict. Fast signal acquisition requires a large loop bandwidth which conflicts with a good jitter and sideband suppression. The designer must find as good a compromise between both requirements as possible.

In this paper a class of integrable phase-and-frequency comparators which significantly separate both modes is presented. These adaptive comparators,



(A) (B)

Fig. 1. (A) General PLL block diagram. (B) Loop filter configuration.

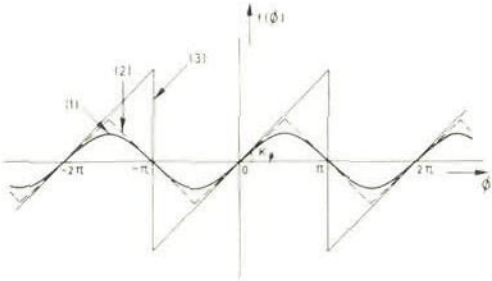
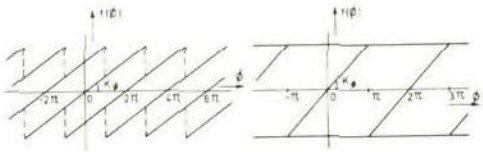


Fig. 2. Transfer function of different types of phase comparators: (1) sinusoidal type, (2) triangular type, (3) sawtooth type.



(A) (B)

Fig. 3. Transfer function of different types of phase-and-frequency comparators: (A) Bidirectional shift register. (B) Three-cell asynchronous delay line.

which are based on the up-down counting principles, are investigated in a commonly used second-order PLL with a perfect integrator.

The general block diagram of a PLL is shown in Fig. 1A. The input phase $\phi_i(t)$ is compared with the voltage-controlled oscillator (VCO) phase $\phi_o(t)$ in the phase comparator. Any difference between these two quantities results in a control signal $u_\phi(t)$, which is filtered and applied to the VCO.

This process is defined by the following relations [2]:

$$\phi(t) = \phi_i(t) - \phi_o(t)$$

$$u_\phi(t) = f\{\phi(t)\}$$

$$u_c(t) = \int_{-\infty}^{t} u_\phi(t)\, h(t - \tau)\, d\tau$$

$$d\phi_o(t)/dt = \omega_c + K_{vco}\, u_c(t)$$

where $f(\phi)$ is the PC transfer function, $h(t)$ is the impulse response of the loop filter, K_{vco} is the modulation sensitivity of the VCO in radians per volt per second, and ω_c is the quiescent frequency of the VCO in radians per second.

In the case of a linear PC transfer function with sensitivity K_ϕ (in radians per volt) and a proportional-plus-integral loop filter [see Fig. 1(b)], this results in the basic loop equation

$$d^2\phi/dt^2 + 2\zeta\omega_n\, d\phi/dt + \omega_n^2\,\phi = d^2\phi_i/dt^2 \qquad (1)$$

where

$$\omega_n^2 = K_\phi K_{vco}/\tau_1 \quad \text{and} \quad 2\zeta\omega_n = K_\phi K_{vco}\,\tau_f/\tau_1.$$

The natural frequency ω_n and the damping factor ζ are important design parameters for the filtering mode.

In the following section a review of some existing comparators (PCs and PFCs) is given and a criterion is derived for an adequate separation of the two modes. The adaptive phase comparator, in which this separation can take place fully automatically, is described.

In Section III the acquisition properties of PLLs, which employ the proposed phase comparator, are investigated. A design philosophy is given, based on the expected maximum initial frequency difference and the required filtering parameters.

II. FREQUENCY ACQUISITION

Since the frequency acquisition phenomenon is characterized by the occurrence of large phase errors, the acquisition performance of a PLL depends for the better part on the complete shape of the phase comparator transfer function. Fig. 2 gives the transfer functions of the RS flipflop (sawtooth), the exclusive-OR (triangular), and a sinusoidal comparator, all with equal sensitivity K_ϕ.

In the presence of a large frequency detuning the pull-in time of PLLs employing these kinds of phase comparators increases exponentially as this detuning increases. Because the frequency difference is equivalent to an accumulated phase difference, the output voltage of the comparators of Fig. 2 alternates between positive and negative values. In conjunction with the feedback these PCs deliver only a small dc voltage component (pull-in voltage) for decreasing the frequency difference [2].

A PLL employing a PFC instead of a PC does not suffer from this phenomenon. Some examples of PFCs are the bidirectional shift register (BSR) and the three-cell asynchronous delay line (ADL), whose transfer functions are shown in Fig. 3. The comparator output voltage contains a distinct dc voltage component, which is either positive or negative, depending on the sign of the frequency difference. Fundamentally these phase comparators can be

thought of as up-down counters [25] and a closer study of the up-down counting concept will be useful.

With an up-down counter (UDC) a variety of transfer functions can be realized, owing to the simple fact that several output signals can be combined [31]. One of the simplest members of the UDC family is the three-cell UDC with two outputs, each producing opposite values in the active state. This phase-and-frequency detector is available in several equivalent versions as a single-chip integrated circuit. The combination of both output signals gives the transfer function $f(\phi)$ of the circuit (Fig. 4) and a closer examination demonstrates the PFC character of the three-cell UDC.

To show the relation between the synchronous mode (natural frequency ω_n) and the acquisition mode an approximation of the pull-in time T_p of PLLs with the abovementioned phase comparators is now given following Meer's quasi-stationary approach [15]. This assumes a large frequency detuning $\Delta\omega$ in relation to ω_n, i.e., many cycle slips. In the case of a perfect integrator in the loop, it is found for phase comparators having equal sensitivity that

$$\omega_n T_p = c(1/2\zeta)(\Delta\omega/\omega_n)^2$$

with $c = 1$ for sinusoidal, $c = 6/\pi^2$ for triangular, and $c = 1.5/\pi^2$ for sawtooth-shaped transfer functions.

For phase-and-frequency comparators it is found that

$$\omega_n T_p = c\,\Delta\omega/\omega_n$$

with $c = 1/\pi$ for BSR and three-cell UDC and $c = 1/2\pi$ for three-cell ADL. In fact, the acquisition mechanism of PLLs employing PFCs can be considered as a frequency sweep of the VCO with rate $\pi\omega_n^2$ or $2\pi\omega_n^2$ (rad·s^{-2}).

Nevertheless, the pull-in time of these PLLs is merely specified through filtering parameters, with the result that synchronous and acquisition modes are highly dependent. This implies that the design possibilities are rather restricted. Only with mode separation can this restraint be attacked. The separation can be obtained from the phase error information.

The fact that the phase error exceeds the monotonic range of the PC transfer function, i.e., for a sawtooth PC the passing of a discontinuity reveals the information that the loop enters the acquisition mode in order to acquire lock during the subsequent cycles. In the case of a digital three-cell VDC, the mode information is readily available in the circuit itself. For a phase error that is a fraction smaller than 2π rads, the active cell of a three-cell UDC produces an output pulse train with a duty ratio of nearly one. On the other hand, this cell generates a signal with a duty ratio of nearly zero for a phase difference somewhat larger than 2π rad.

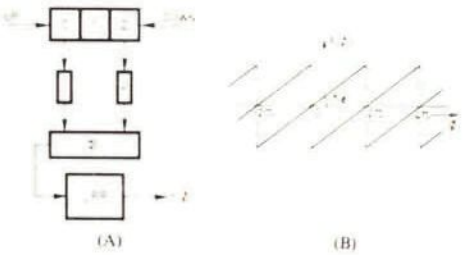


Fig. 4. (A) Diagram of counter. (B) Transfer function of three-cell up-down counter.

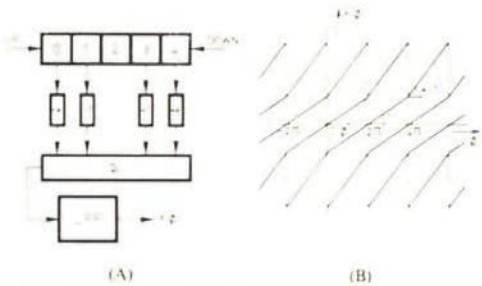


Fig. 5. (A) Diagram of phase comparator. (B) Normalized transfer function of five-cell adaptive phase comparator.

If a three-cell UDC is extended by two extra cells at both ends (Fig. 5), these cells will become active as soon as the phase error exceeds 2π rads. Hence these cells automatically contain the PLL operating mode information. This information can be used to make the filter and acquisition properties less dependent by attaching weight factors to the outermost cells. When high weight factors are attached to the outer cells, the acquisition performance can be greatly improved. A design philosophy can be developed which is based on direct synchronization (phase acquisition) rather than on the "flickering" approach (frequency acquisition). As will be explained in the following section the phase range extension of the comparator makes it possible for the loop to respond adaptively to input frequency steps.

III. LOOP PROPERTIES WITH ADAPTIVE PHASE COMPARATORS

A. Transfer Function

The transfer characteristic of the adaptive phase comparator can be obtained from the duty cycle analysis of the combined output signals. In the synchronous mode the phase comparator alternates between states 1 and 2 or states 2 and 3, depending on the sign of the instantaneous phase error. Suppose that the phase error grows a little over 2π rads; then the loop leaves the synchronous mode. In the case of

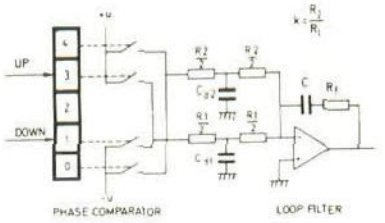


Fig. 6. Realization example of adaptive phase comparator and loop filter combination.

a positive frequency difference states 3 and 4 of the comparator are alternately active, thus producing a pulse train with a duty ratio of nearly one at output 3 and a pulse train with an almost zero duty ratio at output 4. The combination of the output signals with different weight factors, having ratio k, results in the general transfer function of the adaptive phase comparator, which is shown in Fig. 5(B).

Due to the alternation between states 3 and 4 for phase errors between 2π and 4π rads, the effective weight factor ratio is k-1. This ratio characterizes the independence of synchronous and acquisition modes. Theoretically, if the time-continuous character of the loop is preserved, any weight factor may be chosen, but in practice, the weight factor is only limited by physical constraints such as the maximum resistor ratio in the circuit of Fig. 6.

B. General Loop Analysis

Since the adaptive phase comparator performs repeating piecewise linear characteristics, loop equations describe the loop for only certain intervals of the phase error ϕ. In the case of the five-cell UDC it is sufficient to derive two equations for the interval $(-4\pi, 4\pi)$.

In this interval the transfer function is piecewise linear and is given by

$$f(\phi) = \begin{cases} K_\phi \phi, & \text{for } -2\pi < \phi < 2\pi \\ K_\phi^* \phi^* & \text{for } -4\pi < \phi < -2\pi,\ 2\pi < \phi < 4\pi \end{cases}$$

where

$$K_\phi^* = K_\phi (k - 1)$$

$$\phi^* = \phi - \phi'$$

$$\phi' = 2\pi[(k - 2)/(k - 1)] \operatorname{sign}(\phi).$$

This leads to (1) for the interval $(-2\pi, 2\pi)$ and to

$$d^2\phi/dt^2 + 2\zeta\omega_n(k - 1)(d\phi/dt) + \omega_n^2(k - 1) \cdot (\phi - \phi') = d^2\phi_i/dt^2 \qquad (2)$$

for the intervals $(-4\pi, -2\pi)$, $(2\pi, 4\pi)$.

The pull-in behavior of the PLL can be analyzed by inspecting phase plane plots of (1) and (2). In Fig. 7 the normalized phase-plane plots (ϕ, $\dot{\phi}/\omega_n$) are given of both a PLL with a three-cell and one with a five-cell UDC ($\zeta = 0.7$, $k = 5$) for several initial frequency steps. They are obtained from the numerical solution of (1) and (2). A comparison of these plots shows that for a large input frequency steps the number of cycle slips is considerably reduced by employing a five-cell UDC with suitable weight factors in the loop. A decrease in the acquisition time occurs, which will be more significant if the loop would normally have slipped more cycles.

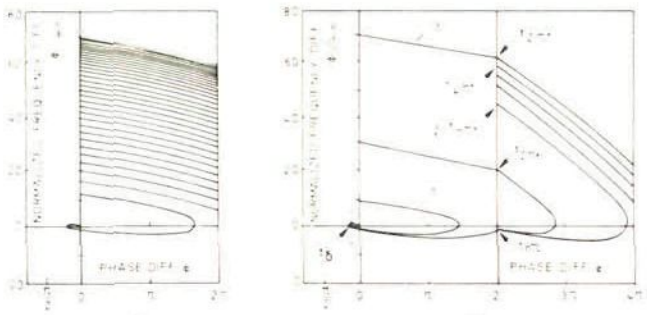
C. Acquisition Analysis

To judge the expected speed improvement more definitely, the pull-in time as a function of the initial frequency offset will be calculated for employing three-cell and five-cell UDCs for different k ratios.

Two different approaches are possible to calculate pull-in times. One of them is an exact calculation of the pull-in time using loop equations (1) and (2). The other is the quasi-stationary approach [15], an assessment based on the driving dc voltage component, which is produced by the phase comparator as a result of cycle slips during pull-in. Owing to the many cycle slips the latter already shows a good correspondence with exact calculations as far as the three-cell UDC loop is concerned. A quasi-stationary approach for the five-cell UDC loop [26] will not be very successful, because generally there are not many discontinuities involved and an exact pull-in time calculation becomes necessary. This exact method is described in the Appendix with the arbitrary definition of pull-in time as the time beyond which the absolute phase error $\phi(t)$ is less than $\pi/10$ rad.

The results of both approaches are shown in Fig. 8, in which the normalized pull-in time is presented as a function of the normalized initial frequency offset for several values of k and zero initial phase shift. The difference between the quasi-stationary approach as characterized by the dashed lines and the exact curves is significant. The former delivers very optimistic values in the case of the five-cell UDC loop, so that this approach is not very useful for the designer. Exact calculation of the pull-in time, however, results in a stepwise shape for the higher frequency offsets this due to the occurrence of cycle slips. To get an overview the results of the exact pull-in time calculation for this part are represented by the worst case envelopes. The pull-in time increases dramatically for increasing frequency offsets in this area, which is characterized by large discontinuities during pull-in. This is referred to as frequency acquisition.

Phase acquisition, on the other hand, is characterized by synchronization actions without the occur-



(A) (B)

Fig. 7. Phase plane trajectories of PLL for $\zeta = 0.7$ and $k = 5$. . (A) Employing a three-cell UDC. (B) Employing five-cell UDC.

rence of discontinuities. For a five-cell UDC loop this implies that the absolute phase error will be less than 4π at all times. The maximum input frequency step that maintains the phase error within the bounds $(-4\pi, +4\pi)$ is defined as the phase acquisition range and can be calculated using the method described in the Appendix. The result is shown in Fig. 9 and an increased phase acquisition range with increasing weight-factor ratio k is noticed. This implies that the appearance of discontinuities is delayed, so that the pull-in time is minimal for a certain set of initial conditions. In other words, for a certain initial frequency offset there is a minimum k value that satisfies phase acquisition conditions. The designer must apply a weight-factor ratio k that is large enough to guarantee phase acquisition for all expected initial frequency offsets in order to obtain minimum pull-in times.

IV. PRACTICAL RESULTS

A value higher than the minimum k value for a certain initial frequency step that maintains the phase error within the bounds $(-4\pi, +4\pi)$ provides no practical pull-in time improvement. This is caused by the automatic proportional enlargement of $\zeta^{\star}$, the damping factor for the extreme intervals with increasing k ratio. This results in a fast frequency error decrement with small overshoot, but also in a relatively slow phase error reduction towards $(\phi', 0)$. However, as soon as the phase error becomes smaller than 2π, the new equilibrium point becomes (0, 0) and yet another 2π rad phase error reduction has to be accomplished. This is illustrated by the phase-and-frequency step response of Fig. 10, in which the increase of k in the case of phase acquisition appears to have little influence on both frequency-and-phase response time. One could consider decreasing the damping factor $\zeta^{\star}$ independently. Although a little speed improvement may occur, this method is not recommended as the phase acquisition range and loop stability are affected.

In view of these considerations the experiments have been carried out with zero initial phase shift, while attention has been paid to the realization of the time-continuous character of the loop by means of suitable low-pass filters. The experimental results for

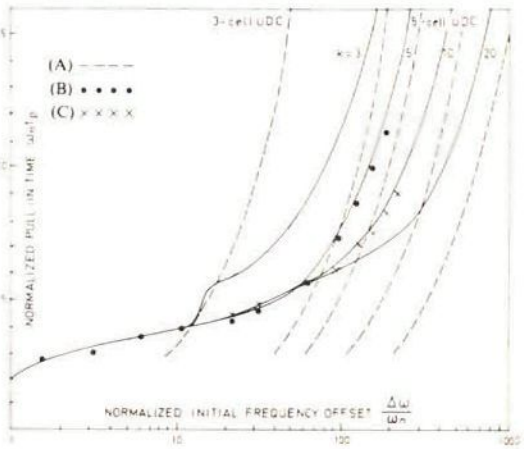


Fig. 8. Normalized pull-in time versus initial frequency offset of PLLs employing a three-cell comparator and different five-cell adaptive phase comparators for $\zeta = 0.7$. (A) --- quasi-stationary approach. (B) ... measured for $k = 5$. (C) xxx measured for $k = 10$.

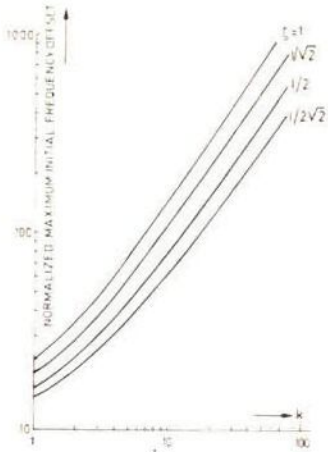


Fig. 9. Normalized maximum initial frequency offset versus k for different values of ζ in case of phase acquisition.

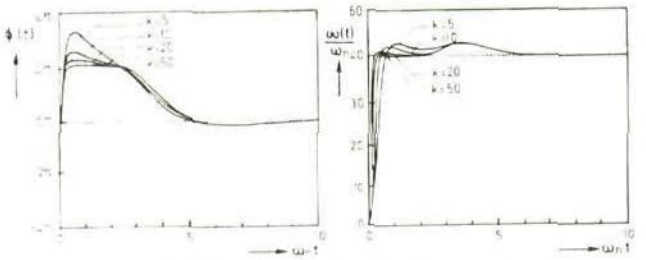
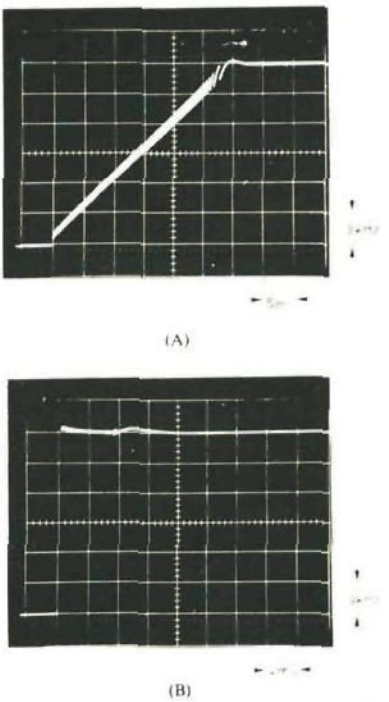


Fig. 10. Transient response of a PLL employing a five-cell UDC for $\zeta = 0.7$ and different k values.



(A)

(B)

Fig. 11. Frequency step responses of PLL for $\zeta = 0.7$ and $\omega_n = 1000$. (A) with three-cell phase comparator. (B) with five-cell adaptive phase comparator ($k = 20$).

loops operating in the 40-120 kHz range are also depicted in Fig. 8 and they show a good correspondence with calculated values. For a normalized frequency offset $\Delta\omega/\omega_n = 100$ it is seen from Fig. 9 that a k-value of minimally 10 is sufficient to guarantee phase acquisition. This results in a normalized pull-in time of $T_p = 7/\omega_n$, as is noted from Fig. 8. In Fig. 11 the frequency step responses of a loop with a three-cell and a loop with a five-cell UDC with $k = 20$ are compared. It is noted that the application of a five-cell adaptive phase comparator decreases the frequency acquisition time in this case by at least a factor 50. Phase acquisition is obtained with a speed improvement of a factor 5-10.

It should be noted that in practice the use of conventional up-down counters has some restrictions, because of their vulnerability to simultaneous input pulses, which can result in a wrong counter state. This deranges the control action of the loop. This defect, inherent in conventional UDCs, can be avoided by gating both input signals (causing a dead phase zone), or by employing a different concept of up-down counting, e.g., the use of two independent ring counters, one of which counts up pulses and the other of which counts down pulses. The state information is obtained from the combination of the contents of the individual counters in a decoding circuit. To prevent overflow the ring counters are only gated, when an outermost state is active. This indeed introduces a dead phase zone, which, nevertheless, is shifted to the extreme parts of the transfer characteristic. Hence this will not affect the synchronous mode performance, although theoretically the acquisition behavior is affected. In practice, however, the influence is negligible.

V. CONCLUSION

The properties of commonly used second-order loops that employ the adaptive phase-and-frequency comparator based on up-down counting techniques have been discussed. Pull-in behavior has been emphasized and a comparison has been made with other phase comparators. Numerical results, both theoretical and experimental, have been given for the situation of high signal-to-noise ratios. They show a considerable speed improvement for high initial frequency detunings with regard to the loop bandwidth, so that it is possible to choose the loop bandwidth a lot smaller than normal, based upon the conventional compromise, without affecting the acquisition properties. The proposed phase comparator can be thought of as an acquisition aid that is implemented together with the phase comparison function in one circuit. This adaptive five-cell phase-and-frequency comparator, used instead of a three-cell comparator, can deliver an easy design procedure for many PLL application areas.

APPENDIX

In this Appendix a method of exact calculation of the pull-in time of second-order PLLs with adaptive

TABLE I
General Solutions of Loop Equations for Both Phase Intervals

Interval	Damping Factor	Equation		
$(-2\pi, +2\pi)$	$\zeta < 1$	$\phi(t) = (1/\alpha)\exp(-\beta t/\alpha)[(y_0 + \phi_0)\sin(\beta t) + \alpha_1 \phi_0 \cos(\beta t)]$	(A2)	$\alpha = \sqrt{1-\zeta^2}/\zeta$; $\beta = \omega_n\sqrt{1-\zeta^2}$
$(+2\pi, +4\pi)$ and $(-4\pi, -2\pi)$	$\zeta^* > 1$	$\phi(t) = (1/2\alpha^*)\exp(-\beta^* t/\alpha_1)[(y_0^* + \phi_0^*(1+\alpha^*)]\exp(\beta^* t) - [y_0^* + \phi_0^*(1-\alpha^*)]\exp(-\beta^* t)] + \phi$	(A3)	$\alpha^* = \sqrt{\zeta^{*2}-1}/\zeta^*$; $\beta^* = \omega_n^*\sqrt{\zeta^{*2}-1}$

phase comparators is described. The procedure is based on the solutions of loop equations (1) and (2) for different phase intervals.

A. General Solution

The initial conditions consist of a constant phase and/or frequency difference, which leads for an input frequency step to

$$d^2\phi_i/dt^2 = 0, \qquad \text{for } t > 0$$

and

$$\phi(0) = \phi_0$$

$$\dot{\phi}(0) = \omega_0.$$

Defining

$$\sqrt{\zeta^2 - 1}/\zeta = \alpha$$

$$\omega_n\sqrt{\zeta^2 - 1} = \beta$$

$$\omega_0/\zeta\omega_n = y_0$$

the general solution of loop equation (1) for $t > 0$ becomes

$$\phi(t) = (1/\alpha)\exp(-\beta t/\alpha)\{(y_0 + \phi_0) \cdot [\exp(\beta t)/2 - \exp(-\beta t)/2] + \alpha\phi_0 \cdot [\exp(\beta t)/2 + \exp(-\beta t)/2]\}. \tag{A1}$$

Loop equation (2) can be rewritten to the form of (1) with

$$\omega_n^* = \sqrt{k-1}\,\omega_n$$

$$\zeta_n^* = \sqrt{k-1}\,\zeta.$$

Then the general solution of (2) is equal to (A1) with α, β, ϕ, and y_0 replaced by α^*, β^*, ϕ^*, and y_0^*.

Useful solutions of (A2) and (A3) are shown in Table I for common values of $\zeta(0 < \zeta < 1)$ and for weight factors that vary in such a way that $\zeta^* < 1$. These solutions are used for determining the loop behavior. Depending on initial conditions there are three different possibilities for achieving phase lock:

1) First-cycle pull-in: The complete synchronization problem is bounded to the interval $-2\pi < \phi < 2\pi$.
2) Second-cycle pull-in: Synchronization takes place in the interval $-4\pi < \phi < 4\pi$.

These phenomena are considered as phase acquisition because there are no discontinuities involved and there is an unequivocal relation between phase and PC output voltage during pull-in.

3) Frequency acquisition: The phase error exceeds 4π rad and the loop slips one or several cycles resulting in discontinuities in the PC output voltage.

The conditions required for the abovementioned pull-in cases will be determined. For given loop parameters and initial phase the maximum initial frequency offset will be calculated for which the particular phenomena appear.

B. Phase Acquisition Conditions

1) First-Cycle Pull-In Conditions

Generally, the initial conditions originate from a step change of the input frequency Ω_0. Asynchronous reference switching introduces an input phase step ϕ_0, which causes a step change of frequency of the VCO. So the net initial frequency offset if $\omega_0 = \Omega_0 - 2\zeta\omega_n$ ϕ_0. Hence, for the initial phase and/or frequency step, (A2) (see Table I) is modified to

$$\phi(t) = (1/\alpha)\exp(-\beta t/\alpha)[(y_0 - \phi_0)\sin(\beta t) + \alpha\phi_0\cos(\beta t)]. \tag{A2a}$$

The first extreme value of $\phi(t)$ determines the boundary of the first-cycle pull-in. This value amounts to [See Table I for (A3)]

$$\phi_{e1} = 2\pi. \tag{A4}$$

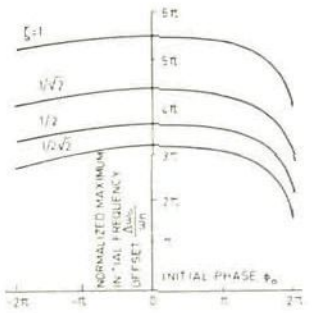


Fig. 12. Normalized maximum initial frequency offset versus initial phase for different values of ζ in case of first-cycle pull-in.

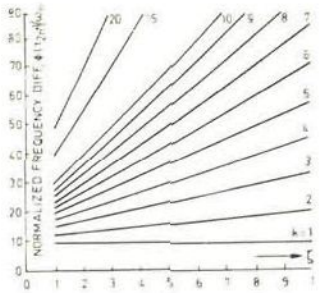


Fig. 13. Normalized maximum frequency difference versus ζ for $\gamma_0 = 2$.

The value ϕ_{e1} is given by the smallest positive value of t satisfying the relation $\dot{\phi}(t) = 0$.

It is found that

$$t_{e1} = (1/\beta)\left(n\pi + \tan^{-1}\{\alpha(y_0 - 2\phi_0)/[y_0 + \phi_0(\alpha^2 - 1)]\}\right) \quad \text{(A5)}$$

where

$$n = \begin{cases} 0, & y_0/\phi_0 > 2 \\ 1, & y_0/\phi_0 \leq 2. \end{cases}$$

The first extreme value of $\phi(t)$ is then given by

$$\phi_{e1} = \sqrt{[(y_0 - \phi_0)^2 + \alpha^2\phi_0^2]/(1 + \alpha^2)}\ \exp(-\beta t_{e1}/\alpha). \quad \text{(A6)}$$

Now ϕ_0 is fixed and the maximum normalized initial frequency offset $\hat{y}_0$ is solved from (A4) with (A5) and (A6). The solutions are shown in Fig. 12 as a function of the initial phase ϕ_0 for several values of ζ. It should be noted that this is equivalent to the direct capture range for a three-state PFC.

2) Second-Cycle Pull-In Conditions

A similar procedure is used for obtaining the boundary for second-cycle pull-in. This boundary is determined by the relation

$$\phi_{e1} = 4\pi \quad \text{(A7)}$$

where ϕ_{e1} is the first extreme value of $\phi(t)$ given by (A3). It is found that

$$\phi_{e1} = \sqrt{[(y_0^* + \phi_0^*)^2 - \alpha^{*2}\phi_0^{*2}]/(1 - \alpha^{*2})} \cdot \exp(-\beta^* t_{e1}^*/\alpha^*) + \phi' \quad \text{(A8)}$$

where

$$t_{e1}^* = (1/2\beta^*)\ln\{[(1 + \alpha^*)/(1 - \alpha^*)] \cdot [y_0^* + \phi_0^*(1 - \alpha^*)]/[y_0^* + \phi_0^*(1 + \alpha^*)]\}.$$

From (A8) the maximum normalized frequency offset $\hat{y}_0^*$ that satisfies second-cycle pull-in conditions is solved for $\phi_0^* = 2\pi$. The results are given in Fig. 13.

The maximum normalized initial frequency offset $\hat{y}_0$ for second-cycle pull-in is now obtained from (A2) with the boundary conditions

$$\phi(t_{2\pi}^+) = 2\pi$$

$$\dot{\phi}(t_{2\pi}^+) = (\beta^*/\alpha^*)\,\hat{y}_0^*.$$

For $\phi_0 = 0$ it is found that

$$\hat{y}_0 = \sqrt{(\hat{y}_{2\pi}' + 2\pi)^2 + 4\pi^2\alpha^2}\ \exp\{(1/\alpha)\tan^{-1} \cdot [2\pi\alpha/(\hat{y}_{2\pi}' + 2\pi)]\}$$

where

$$\hat{y}_{2\pi}' = (\alpha/\beta)(\beta^*/\alpha^*)\,\hat{y}_0^*.$$

The normalized function is plotted in Fig. 9 as a function of k for several values of ζ. This can be approximated by the expression

$$\Delta\omega/\omega_n = 4\pi\zeta k.$$

The initial phase ϕ_0 appears to have very little influence on the maximum initial frequency offset for second-cycle pull-in.

C. Pull-in-Time Calculation

For initial values that satisfy first-cycle pull-in conditions the pull-in time T_p is, according to Fig. 7(B), given by $T_p = t_\delta$ in which t_δ is the largest value of t

that satisfies the relation $|\dot{\phi}(t)| = \delta$ where $\dot{\phi}(t)$ is given by (A2a).

For initial values that satisfy second-cycle pull-in conditions the pull-in time is given by $T_p = t_{2\pi^-} + t_{2\pi} + t_\delta$.

1) The value of $t_{2\pi^-}$ can be obtained from (A2a) for $\phi(t) = 2\pi$, after which the frequency difference at this moment is given by $\dot{\phi}(t)_{2\pi^-}$).

2) The value of $t_{2\pi}$ is determined from the solution of (A3) for $\phi(t) = 2\pi$ with $y_0 = (\alpha/\beta)\,\dot{\phi}(t_{2\pi^-})$ as a starting value. The frequency difference at this moment is again obtained from the first derivate of $\phi(t)$.

3) The value of t_δ is determined by the earlier mentioned relation $|\dot{\phi}(t)| = \delta$, with $\phi_0 = 2\pi$ and $y_0 = (\alpha/\beta)\,\dot{\phi}(t_{2\pi^-})$ as starting values. Since the initial conditions do not originate from a step change of phase or frequency, (A2) is now used.

For initial values that do not satisfy phase acquisition conditions at least one discontinuity occurs which can be considered as a step change of 2π rad. This causes a net change of frequency of $2\zeta\omega n(k-1)\,2\pi$. The pull-in time is given by $T_p = t_{2\pi^-} + t_{4\pi^-} + \cdots + t_{n\pi^-} + t_{n\pi} + t_\delta$.

a) According to 1) above, the values of $t_{2\pi^-}$ and $\dot{\phi}(t_{2\pi^-})$ are determined.

b) The value of $t_{4\pi^-}$ is obtained from the solution of (A3) for $\phi(t) = 4\pi$ with $y_0^* = (\alpha^*/\beta^*)\,\dot{\phi}(t_{2\pi^-})$ as a starting value. The frequency difference $\dot{\phi}(t_{4\pi^-})$ is obtained by differentiation and substitution.

c) Considering the effects of the discontinuity stated above, the starting values for the adjacent phase region are

$$\phi_0^* = 2\pi/(k-1)$$

$$y_0^* = (\alpha^*/\beta^*)\,\dot{\phi}(t_{4\pi^-}) + 4\pi.$$

d) Another discontinuity will occur at the end of this cycle when $y_0^* > \hat{y}_0^*$ where $\hat{y}_0^*$ is given in Fig. 13.

e) In that case a procedure similar to that stated above under b) and c) follows until the final discontinuity occurs at $t = t_{n\pi^+}$. The terminal cycles are reached and the values of $t_{n\pi^-}$ and t_δ are determined according to the method described in 2) and 3) above.

In the case of many cycle slips the pull-in time can be approximated following Meer's method [15]. This method can be applied if $y_0 \gg 4\pi$. In terms of the weight factor k, it is necessary that $\omega_0 \gg 4\pi k\zeta\omega_n$.

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NOVEL CIRCUIT DESIGN AND IMPLEMENTATION OF ADAPTIVE PHASE COMPARATORS

Index ng terms: Circuit theory and design, Phase comparators, Phase-locked loops

A novel circuit implementation for an adaptive phase-frequency comparator, which can be conceived of as a 5-cell up-down counter, is proposed. This circuit can handle coinciden: input signals and has no dead phase zone or intermediate states. These properties greatly improve the performance of a phase-locked loop.

Introduction: The performance of phase-locked systems is highly dependent on the phase-comparing circuit used. The conversion factor K_d (V/rad) of the phase comparator influences important loop parameters in both the synchronous mode and the acquisition mode.

To optimise both filter and acquisition behaviour, the phase comparator should have independent conversion factors in the synchronous and acquisition modes. These comparators are called adaptive phase comparators,[1] and are an extension of the phase-frequency detectors (PFDs) commonly applied in integrated circuits, such as the 4046 and 4044. The desired transfer characteristic of the adaptive PFD is depicted in Fig. 1.

Common PFDs can be considered as 3-cell up-down counters. Adaptive phase comparators can be realised with a 5-cell up-down counter (UDC), with outputs weighted by a certain gain factor. However, circuit implementation is quite difficult owing to coincidence problems.

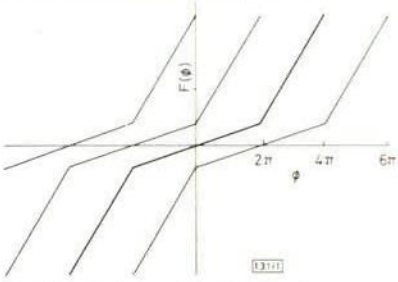

Fig. 1 *Transfer characteristics of adaptive phase comparator*

Coincident input signals: When a UDC is applied as a generalised phase-frequency comparator, special attention must be paid to the processing of coincident signals. For a certain phase difference the UDC jumps between two adjacent positions. If the phase difference between the two input signals is an integer times 2π, up and down pulses occur simultaneously and the position of the UDC may not change.

In general, a UDC consists of a series of sequential elements (flip-flops and/or latches), the state being determined by the input pulses. The outputs of these elements form the outputs of the UDC. Therefore the state of the sequential logic directly determines the position of the UDC. If up and down pulses occur simultaneously certain sequential elements must process set and reset actions at the same time.

As conventional UDCs cannot handle coincident signals, gating is normally applied to avoid the coincidence of signals. However, this introduces dead zones in the transfer function of the phase comparator, which means increased jitter in the phase-locked loop.

To avoid gating, a separation must be made between the state of the sequential elements and the position of the UDC itself. The up and down signals may never act on the same sequential element, but must always excite two different elements during successive or simultaneously arriving pulses. As a consequence, the sequential part has to change its state when up or down pulses occur, even when they occur simultaneously. To determine the position of the UDC, the sequential part is followed by a decoding circuit. This combinational circuit converts the output signals of the sequential elements into output signals of the UDC. Coincident input signals will cause a change in the state of the sequential part, but because of the decoder the outputs of the UDC will not alter.

Bounding: In the outermost positions (for the adaptive phase comparator the positions ± 2) special measures must be taken to prevent the UDC from jumping into the wrong position, because this will cause the sign of the phase error information to be lost. After the UDC has reached an outermost position, the leading signal must be suppressed. If the leading pulse occurs before the lagging signal, the leading pulse will be ignored and a cycle slip will result. However, the sign of the phase error is maintained.

Two propagation delays in the UDC are important with respect to the bounding action. First, the delay from the leading signal up to the activation of the bounding circuit must be considered. During the interval formed by this delay no leading pulses may occur, because the bounding is not yet active and the unsuppressed pulse would push the UDC into a wrong position. This would result in the loss of the sign information of the phase error.

Fig. 2 *Delay representation in phase transfer characteristic*

The second important propagation delay is measured from the lagging signal to the deactivation of the bounding action. During this interval, leading pulses are still suppressed. This delay time τ_b determines at what phase difference a cycle slip will occur; see Fig. 2 ($\phi_{cycle\ slip} = 4\pi - \omega\tau_b$). Because τ_b is fixed, the phase range of the adaptive PFD decreases with increasing frequency. If $\omega\tau_b = 2\pi$, the 5-cell UDC has degenerated into a 3-cell UDC.

The bounding signals can simply be derived from the outputs of the decoder, indicating the highest and lowest positions of the UDC. Because the delay through the decoder is included in τ_b, the logic depth of the decoder determines the maximum frequency of the detector.

Circuit implementation: To combat the coincidence problem, the design concept of the UDC discussed here offers various circuit options. First, the sequential elements can be connected to each other as in a chain. The up signals are fed into one side of the chain, and the down signals into the other. The up and down information asynchronously ripple to each other. Examples of this approach are the asynchronous delay line[2,3] and the digital phase-frequency comparator.[4] However, these designs have intermediate positions which occur when the UDC jumps from one stable position to another, introducing spikes. These have a deteriorating effect on the performance of the PLL.

Our new design has no intermediate positions and can handle coincident input signals. When the UDC is constructed with two identical counters (both counting in the same direction), the up and down signals can activate two distinct counters. The overall position of the UDC is obtained from the difference in position between the two counters. Intermediate positions are avoided, when the two counters are producing a progressive code. This can be accomplished by applying Johnson counters.

Only the difference in the contents of the two counters is a measure for the position of the UDC. For a 5-cell UDC, each counter must be able to take on five different positions relative to an arbitrary position of the other counter. Therefore each counter minimally requires three sequential elements. When three flip-flops are connected in series and the inverted output of the last section is fed back to the input of the series, a Johnson counter results. Special measures must be taken to prevent the counters from entering into one of the forbidden states (010 and 101).

This design can be further simplified, because of the presence of redundant states. The sequential part of the above-described UDC contains $6 \times 6 = 36$ states. However, for a 5-cell UDC operating on the proposed difference principle, only 25 states are required. Consequently, five sequential elements should be sufficient. To construct such a circuit, let us return to a UDC containing two counters with two flip-flops each. The differences that can be determined are: 0, +1, −1 and 'difference of 2'. In the last position the sign is unknown. However, because position +2 must always be preceded by +1 (the same reasoning is valid for the positions −2 and −1), the sign of the position 'difference of 2' can be determined by including the former position. The sign can be stored in a latch (Fig. 3). An additional advantage of this simplified detector is the absence of forbidden states in the two-flip-flop Johnson counters.

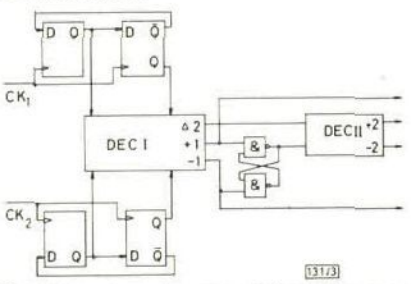

Fig. 3 *Two-counter implementation of adaptive phase comparator*

Analogue output: To complete the PFD circuit the digital output signals of the UDC should be combined into one analogue output signal. In addition, weight factors must be assigned to the outputs in order to obtain different comparator conversion gains for different phase ranges.

A very simple way to combine the UDC outputs is to use an operational amplifier. With the proper feedback configuration adding and subtracting the four outputs of the UDC can easily be accomplished. The weight factors can be added by assigning different values to the gain fixing resistors.

If a charge pump filter is used, the analogue output must float when no UDC outputs are activated. In that case the circuit should be constructed with current sources as depicted in Fig. 4. The weight factors can be set with current strengths I_1 and I_2.

Conclusions: Coincidence problems in up-down counters can be solved by separating the state of the sequential part and the actual position of the UDC. The relation between state and position is regained by a decoding circuit. After simultaneous input pulses, the state of the sequential circuit changes; however, due to the decoder the position of the UDC remains unaltered.

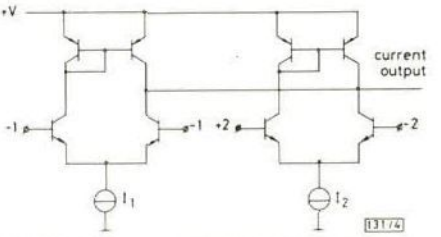

Fig. 4 *Weighted current sources for charge pump applications*

To avoid intermediate positions in the UDC the sequential circuit must produce a progressive code. For a PFD the UDC must be bounded in the outermost positions. The delay time needed to bound and debound the UDC determines the maximum frequency of the PFD.

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24th March 1987

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IMPROVED CIRCUIT IMPLEMENTATION OF ADAPTIVE PHASE COMPARATORS

Indexing terms: Comparators (circuits), Counting circuits

An improved implementation of an adaptive phase comparator circuit is presented. The adaptive phase comparator can be thought of as a five-cell up–down counter that is bounded in both the outermost cells. A new design concept leads to a circuit with a higher maximum operation frequency while maintaining the basic requirements of handling coincident input signals and absence of intermediate states. The circuit is based on the application of a number of identical logic elements, which are placed in a ring structure.

Introduction: The performance of a phase lock system is highly dependent on the applied phase comparator. To optimise both filter and acquisition behaviour, this comparator should have different conversion factors K_d (V/rad) in synchronous and acquisition mode. These comparators, indicated by adaptive phase comparators, can be realised with five-cell up–down counters (UDC), whose outputs are weighted by a certain gain factor.[1]

A problem in adaptive phase comparators (APC) is the occurrence of coincident signals. If $\Delta\phi = n \cdot 2\pi$, with n an integer, up and down pulses occur simultaneously and the position of the UDC may not change. This problem can be resolved by separating the state of the sequential part of the UDC and the actual position of the UDC.[2] In this way up and down pulses acting on one sequential element at the same time can be prevented. A decoding circuit converts the state of the sequential part into the position of the UDC.

The most obvious way to construct such an anticoincident sequential circuit is using a separate up and down section.[2] The maximum frequency of this configuration is limited by the bounding operation in the outermost positions, in which the decoder delay must be taken into account. This article describes a new APC, whose maximum frequency is only limited by the speed of the sequential elements themselves, offering a much faster circuit.

Bounding: In the outermost positions (positions ± 2) the UDC must be prevented from jumping into a wrong position. After the UDC has reached an outermost position the leading input signal must be suppressed. The lagging signal must deactivate the bounding action. However, owing to the time delay τ_b between the input and the bounding circuit, there is a small region in the phase characteristic ($\omega\tau_b$) where the leading signal is erroneously ignored and a cycle slip occurs (see Fig. 1). The phase range of the APC decreases with increasing frequency.

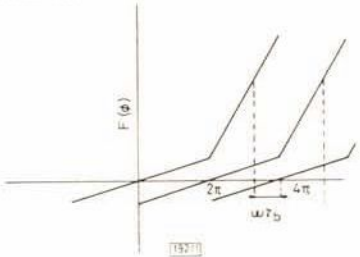

Fig. 1 *Cycle slip at $\phi = 4\pi - \omega\tau_b$*

In an APC containing a separated up and down section, the bounding information can only be obtained from the outputs of the decoder. So the time delay τ_b includes the propagation delay through the decoder. This global bounding method uses the outputs of the APC to control its inputs and can therefore be quite slow.

A much faster bounding method results if the bounding signals are obtained directly from the outputs of the sequential elements. In this local bounding method the delay through the decoder is avoided. The maximum frequency of the circuit depends solely on the speed of the sequential elements. To implement this local bounding method a quite different sequential circuit is necessary.

Ring structure design: In the new sequential circuit, which applies local bounding, there are no separated up and down sections. The circuit consists of a number of identical sequential elements placed in a ring structure. Each element contains both an up and a down clock input. The outputs of an element are connected to the set-up inputs of its preceding and successive element, thus creating the ring. The element itself resembles a master/slave flipflop, except for the two separate clock inputs (see Fig. 2). The set-up signals of the element, derived from the neighbouring elements, determine whether it is sensitive to its up or down clock. For an m position UDC, $m + 1$ elements are required; hence, the APC requires a ring of six elements.

The position of the UDC is derived from the number of set elements in the sequential circuit, irrespective of the absolute position in the ring. The information processing within the ring is as follows. The ring contains a string of k consecutive 1s (indicating the elements which are set) with $1 \leq k \leq m$. On

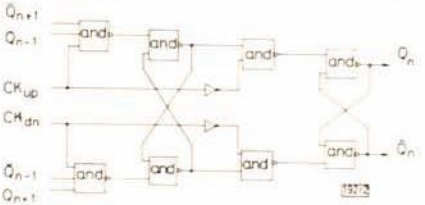

Fig. 2 *Sequential element for local bounding method*

successive up and down pulses the string circles in the ring structure in a fixed direction. Up pulses will add 1s at the front of the string, whereas down pulses will turn 1s into 0s at the tail of the string. Simultaneously occurring up and down pulses will both add a 1 at the front and remove a 1 at the tail of the string at the same time. The string has been shifted over one position. However, the number of 1s contained in the ring has not been altered, and neither has the position of the UDC. Because only one element changes after a clock pulse no intermediate states will occur. The ring code is progressive.

The set-up signals of an element are formed by the output signals of its predecessor and its successor. The following functions must be carried out by these set-up signals:

(i) If the predecessor is set to 1, the element must be sensitive to an up clock input.

(ii) If the predecessor is reset to 0, the element must be sensitive to a down clock input.

Because the predecessor can never be set and reset at the same time, an element will never be sensitive for both clocks.

The operation of the ring can only be satisfactory if $1 \leq k \leq m$; the ring must contain at least one 1 and one 0. Hence, if $k = 1$ or $k = m$, the outermost positions of the UDC have been reached. In that case the element containing the last 1 or 0, respectively, must be bounded to prevent a situation where all elements in the ring are set or reset. The bounding signals can be derived from the outputs of the successor of an element:

(iii) If the successor is set to 1, the element must be insensitive to the up clock input.

(iv) If the successor is reset to 0, the element must be insensitive to the down clock input.

Rules (iii) and (iv) must always be valid, whatever the state of the predecessor may be. Hence the set-up signals derived from the successor must have a higher priority than those of the predecessor. It can be shown that the element depicted in Fig. 2 satisfies all the rules (i)–(iv) just given.

In Fig. 3 an example of the ring operation is given. A six-element ring is depicted, in which the information shifts in a clockwise direction (Fig. 3*a*). We start with an arbitrary state consisting of a string with three consecutive 1s, as in Fig. 3*b*. According to rules (i) and (ii), elements 4 and 1 are sensitive for their up and down inputs, respectively. The other elements are also sensitive to one of the clock inputs, but this is not important, as an activation of this sensitive clock input will not alter their state. Bounding too is unimportant as $k \neq 1$ or 5. The bounding operation, which is always present, has no effect.

An up pulse will bring the state to the one shown in Fig. 3*c*. After the next down pulse the state depicted in Fig. 3*d* results. Comparing the states of Fig. 3*b* and 3*d* shows that the string of 1s has shifted over one position but the number of 1s remains the same. If the up and down pulses had arrived simultaneously the state of Fig. 3*c* would have been skipped.

After two more up pulses, the state of Fig. 3*e* occurs. Only one 0 at element 1 has remained. Because element 2 is set, the up clock of element 1 has been deactivated. So the next up pulse will not alter the state of the ring. Only after a down pulse has reset element 2 (its predecessor is reset, rule (ii)) can

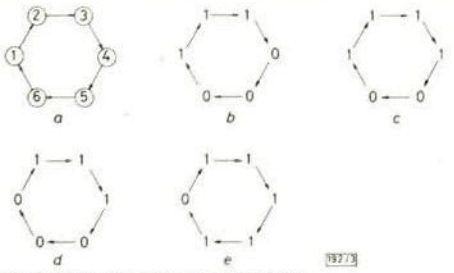

Fig. 3 *Information processing in ring structure*

element 1 receive up pulses again. The delay from a down pulse through element 2 to the set-up input of element 1 determines the time τ_b.

Processing fails if the 1s in the ring no longer constitute a consecutive string. If such a forbidden state arises the ring must be reset to a permitted state. A general reset is also required during starting up conditions. A special detection and reset circuit must be added for this purpose.

Decoder: The position of the UDC can be derived from the state of the ring by counting the number of 1s in the string. For a five-cell UDC the position is $k - 3$, when k is the length of the string.

This function can readily be achieved with a combinational circuit which converts the outputs of the sequential elements into four output signals $(-2, -1, +1, +2)$. The fan-in of the decoder should be as low as possible, as loading of the outputs of the sequential ring elements will slow down their operation and decrease the maximum frequency. After the decoder an analogue network is required to convert the ± 1 and ± 2 signals into a weighted output signal.

A faster and better method is the application of a decoder constructed with analogue electronic elements. If the input signals of the APC are nearly coincident, signals with very small pulse widths are generated in the decoder. If the pulse width gets beneath a certain minimum, the outputs of the decoder will no longer change. This phenomenon introduces dead zones in the phase characteristic around the points, where $\Delta\phi = n \cdot 2\pi$ with n an integer. The dead zone around $\Delta\phi = 0$ causes a jitter of the PLL frequency in the synchronous mode. With analogue circuits smaller pulses can be processed than with digital circuits.

Implementation: A complete APC, containing a six-element ring, a digital decoder and a fault detection/reset circuit was implemented on a PCF700 CMOS gate array from Philips. The FETs have a 4 μm gate length. The maximum operation frequency measured with this circuit was 3 MHz at a supply voltage of 5 V. The time delay τ_b of the bounding operation was found to be 160 ns.

Conclusions: The maximum frequency of adaptive phase comparators containing a five-cell UDC is determined by the bounding operation of the UDC in its outermost positions. In the UDCs using a separated up and down section the decoder delay is included in the bounding delay.

The speed can be increased considerably by deriving the *bounding signals from the outputs of the sequential part of* the UDC thus avoiding the time delay through the decoder. Thus the maximum frequency is determined by the speed of the sequential elements themselves. Such a sequential circuit can be constructed with identical elements placed in a ring structure. Set-up signals derived from adjacent elements determine whether an element is active or not.

The fan-in of the decoder should be as small as possible to keep the loading of the sequential element outputs to a minimum. In addition, attention must be paid to the processing of pulses of small width to minimise the dead zones.

A complete adaptive phase comparator containing a six-element ring, a digital decoder and a fault detection circuit was implemented in CMOS. The maximum frequency at 5 V was 3 MHz. The measured bounding delay τ_b was 160 ns. This rather low maximum operation frequency was caused by the loading of the sequential elements by the digital decoder and the added circuit to detect the forbidden states. Timing simulation of the ring structure alone showed a bounding delay of 70 ns and a maximum frequency exceeding 10 MHz.

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DIGITAL FAST ACQUISITION METHOD FOR PHASE-LOCK LOOPS

Indexing terms: Phase-locked loops, Digital circuits, Digital control

A method for enhancing the frequency-acquisition performance of phase-lock loops (PLLs) is presented, which can be used in all PLLs that employ sequential phase detectors. The proposed method always forces the PLL into the phase-acquisition mode by realising a phase detector transfer characteristic with a pseudolinear infinite phase range. Especially in the case of charge-pump PLLs the proposed method is very useful. Practical results show that the acquisition performance can increase by nearly two orders of magnitude.

Introduction: The availability of integrated phase-lock loop (PLL) circuits has broadened the application area of PLLs. In spite of the sometimes special properties of the electronic circuits in PLL ICs, the design procedure of PLLs more or less follows the common linear, time-continuous approximations. The interrelation of PLL system performance and considerations of the electronic implementation of the circuitry have been ill regarded.

The frequency acquisition performance of a PLL depends strongly on the applied phase detector circuit. The design considerations for the synchrone mode (= filter or tracking mode) and for the acquisition mode are in conflict. Often some form of acquisition-aiding is necessary. The problems can be relieved by using frequency acquisition enhancement such as frequency sweep and frequency discrimination. However, these acquisition enhancers require much additional circuitry.

Phase detectors (PD) with some form of built-in acquisition-aiding are classified by Gardner[1] as sequential PDs. The phase-and-frequency detector (PFD) is available in several versions as a single-chip IC (TTL and ECL 4044), and is available in a well-known PLL CMOS IC 4046. However performances of the synchrone and acquisition mode are still in conflict. If phase-lock system requirements demand some form of acquisition-aiding the designer has to make a choice between much additional hardware or the application of a phase and frequency detector. In the following, frequency acquisition performances are summarised and a new method is proposed and illustrated.

Frequency acquisition: The PLL frequency acquisition (pull-in) time strongly increases with the initial frequency difference. Even with a linear sawtooth-like phase detector transfer characteristic, such as the mentioned phase-and-frequency detector (PFD), the acquisition time is much larger than expected in terms of a linear model behaviour.

This is caused by the nonlinearities in the characteristic. This is inevitable because the phase error during pull-in is generally larger than the linear phase range of the PD. The acquisition time in the linear range (the phase-acquisition time) is approximately equal to $\omega_n T_p \simeq < 5\zeta$ for $\Delta\omega_0 < \pi \cdot 2\zeta\omega_n$ if the phase range is $(-\pi, +\pi)$. In Reference 2 an overview is given for acquisition with various phase detectors. The given quasistationary approximation gives, for a PLL with a perfect integrator in the loop and equal sensitivities

$$\omega_n T_p \simeq < c \cdot \frac{1}{2\zeta}\left(\frac{\Delta\omega_0}{\omega_n}\right)^2$$

$c = 1$ for sinusoidal

$c = 6/\pi^2$ for triangular

$c = 1{\cdot}5/\pi^2$ for sawtooth-shaped transfer functions

The normalised frequency acquisition time increases quadratically with the initial frequency difference $\Delta\omega_0$.

Phase detectors with a built-in acquisition aid such as the PFD have the sign of the frequency difference additionally to the control action during pull-in. The acquisition time in this case is:

$$\omega_n T_p = \frac{1}{\pi}\frac{\Delta\omega_0}{\omega_n}$$

Pull-in time is merely specified through filtering parameters. When *a priori* knowledge of the disturbance is available feed-forward control can be used.[3]

A method to separate acquisition and tracking performance into one circuit is the application of the adaptive phase comparator.[2] Adaptive phase comparators must be able to handle coincident signals. This results in a more complex circuit design[4,5] than that of the common phase-and-frequency detector.

Another approach is to examine the signals in a PLL during pull-in. This leads to the proposed 'pseudolinear' PD characteristic. In Fig. 1, phase-acquisition and frequency acquisition phase errors are illustrated in the sawtooth-like phase detector characteristic of the PFD. Phase acquisition

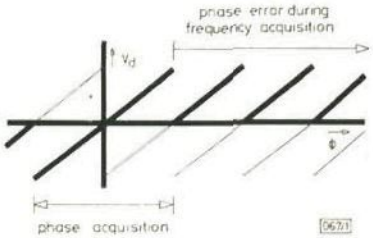

Fig. 1 *Phase acquisition and frequency acquisition depicted in phase detector transfer characteristic*

means that the absolute phase error always remains smaller than 2π. So, the linear model is applicable. During frequency acquisition the phase error increases in proportion to the frequency difference ($\theta_e \approx \Delta\omega_0 \cdot t$) and discontinuities are passed. So, the linear model is no longer valid. Also in terms of phase error the discontinuities are equivalent to phase steps. A phase step of 2π during the frequency acquisition process is a control action in the wrong direction and gives in a second order PLL with a PFD and an active filter a PD output voltage step equal to $V_{dd}/2$ and a control voltage step of $V_{dd}/2 \cdot \tau_2/\tau_1$.

The output frequency steps in terms of loop parameters: $\Delta\omega = 2\pi \cdot 2\zeta\omega_n$. This frequency step is also in the wrong direction and the acquisition is considerably slowed down. If these steps are compensated a full linear characteristic is made and phase acquisition is always maintained with a much smaller acquisition time as a consequence.

Realisation: To compensate for the frequency steps in the wrong direction the loop filter charge has to be modified during and just after the step. This can be easily done by switching current sources connected to the filter capacitor (Fig. 2). The voltage difference at the output of the filter after a

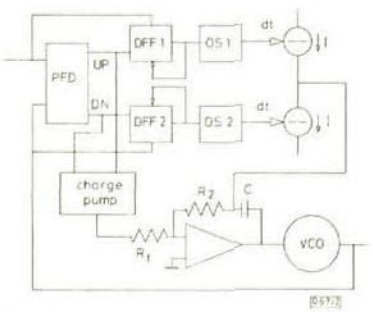

Fig. 2 *Diagram of realisation example*

current pulse I during Δt is equal to $I \cdot \Delta t/C$. The compensation has to be $V_{dd}/2 \cdot \tau_2/\tau_1$. Consequently $I \cdot \Delta t/C = V_{dd}/2 \cdot \tau_2/\tau_1$. The only question, however, is how to detect a discontinuity. In Reference 6 a digital lock detection circuit is given that is ideally suited for this purpose, if the unlock flip-flop operation is modified (self-clear) and followed by a monostable. In Fig. 2 a modified lock detector is given that detects each 2π discontinuity of the phase error characteristic. Consequently this circuit acts as a cycle slip detector.

Experimental results: The compensation results into the situation that after a cycle slip the loop has a phase difference of zero and a frequency difference

$$\dot{\phi}_{n+1} = \dot{\phi}_n + \Delta\dot{\phi}_{n+1}$$

The PLL synchronises from this new starting condition. This means that the PLL has not been out of the linear range. So the frequency pull-in time is approximately equal to the phase-acquisition time and has a magnitude of $5/\zeta\omega_n$.

In Fig. 3 the results are shown of a PLL with PFD and active filter, $\omega_n = 1000$, $\zeta = 0{\cdot}7$, $f_{min} = 400\,\text{kHz}$, $f_{max} = 600\,\text{kHz}$.

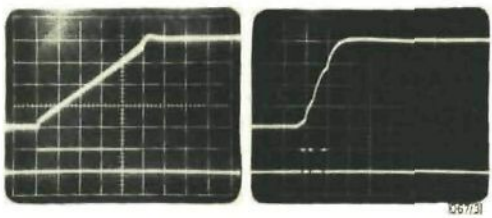

Fig. 3 *Frequency step responses with and without proposed 'pseudo-linear' acquisition method*

With an initial frequency difference $\Delta f_0 = 200\,\text{kHz}$, $T_p = 240\,\text{ms}$ with normal PFD operation and $T_p = 2{\cdot}5\,\text{ms}$ with pseudolinear phase transfer characteristic. This is a performance improvement of nearly factor 100.

Conclusions: A fast digital acquisition method is presented which is based on in-loop compensation of the phase transfer characteristic discontinuities. This can be simply determined from loop parameters and from the time instants on which compensation takes place. These are detected with a modified lock detector used as a cycle slip detector. The compensation results in a infinite range 'pseudolinear' phase transfer characteristic and consequently in a very short acquisition time. The method is shown to be applicable to integrated PLLs with phase detector transfer characteristics showing step discontinuities, such as SR-flip-flop and phase-and-frequency detector.

Experimental results show an acquisition-time improvement of nearly two orders of magnitude.

Acknowledgment: The author is very indebted to Prof. Ralph H. J. M. Otten for his encouragement and the colleagues and research students for their support. He especially thanks Ir. Joep Eijselendoorn for his stimulating discussions and Ir. Alexander Loontjens for working out the measurements.

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18th July 1988

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A Versatile CMOS Rate Multiplier/Variable Divider

RICHARD C. DEN DULK AND JAN J. STUYT

Abstract—A versatile CMOS rate-multiplier/variable-divider integrated circuit that delivers an optimally spaced output signal is presented. The paper includes a comparison of the commonly used rate-multiplication scheme and the accumulator rate-multiplier principle. It is shown that this principle always delivers the best possible digital approximation of a regular signal, but it is inherently slower. The design considerations for speed improvement are described, together with a scheme that leads to the special feature of a programmable denominator. In this case, the circuit can be used as, for example, a binary rate multiplier, BCD rate multiplier, and variable divider, etc. Cascading possibilities are shown, and some application areas are given. The circuit is ideally suited for use as a microprocessor compatible peripheral circuit in digital control systems.

I. Introduction

A RATE multiplier (RM) is defined as a digital circuit that multiplies an incoming frequency or rate by a digital number $K = P/Q$ (P, Q integer, $K \leqq 1$). In the field of phase-lock loop and frequency-synthesis electronics, the application and implementation of rate multipliers in low-power frequency synthesizers has been under investigation for quite some time [1], [2]. Rate multipliers have also found wide application in arithmetic and mathematical function generation [3]-[5], in power control systems [6]-[8], PCM systems [9], [10], motor control systems [11], [12], vector generation and interpolation [13]-[15], and general pulse-rate systems [16], [17], etc.

Commonly used rate-multiplier circuits have the property that only the numerator P can be programmed while Q is fixed to the value 10 (CMOS4527, TTL74167), the value 16 (CMOS-4089), or the value 64 (TTL7497). Cascades of these circuits may only be used for the realization of BCD or binary multiplier chains. Furthermore, as will be explained in this paper, the operating principle contributes to increased irregularity of the output signal. The rate-multiplier circuit to be described in all cases delivers the best possible digital approximation of a regular signal [18]. We have termed this an optimally spaced output pulse distribution. Moreover, the circuit has both numerator P and the denominator Q programmable.

It should be noted that there is a distinction between rate multiplication and division: in dividers the numerator P is always equal to one. Rate multiplication can be thought of as deleting one or more periods out of a group of periods of the incoming signal. If, for example, a multiplication factor $K = \frac{1}{2}$ is required, one can, in principle, carry out several deletion schemes. A simple flip-flop can be implemented in such a way that pulses are regularly deleted so that the first pulse passes, the second is deleted, and so on.

One may also perform the deletion in this way: of each group of six pulses, the first three are passed and the remaining three are deleted. Obviously, this deletion scheme gives a highly irregular signal and is not used in practice. However, if a rate multiplication factor of $K = \frac{2}{3}$ is required, the pulses are always irregularly distributed. The background, IC design, and results of a versatile rate-multiplier circuit that was realized in cooperation with Philips IC Development Laboratories, Nijmegen, The Netherlands, are described in this paper.

II. Commonly Used Rate-Multiplier Principle

Up to now, rate-multiplier integrated circuits have been based on the priniciple of a combination of internally generated noncoincident pulse sequences. In Fig. 1(a), the block diagram is given. For the case of a BCD rate multiplier ($Q = 10$), four basic rates are generated, namely $\frac{1}{10}$, $\frac{2}{10}$, $\frac{4}{10}$, and $\frac{8}{10}$. In Fig. 1(b), all possible waveforms are given for a standard BCD rate multiplier. For a multiplication factor of $\frac{5}{10}$, we see that the output signal is formed in the gate network from basic rates $\frac{1}{10}$ and $\frac{4}{10}$. Consequently, the resulting waveform is far from regular, in spite of the fact that this waveform could be regular. This pulse sequence combination scheme does not deliver the best possible pulse distribution. When more IC's of this type are cascaded, the irregularity can increase substantially. Not only is the spectral purity affected, but also the momentary time error can grow very quickly. In Fig. 1(c), an example of the frequency spectrum of the output signal of three cascaded BCD rate multipliers for a multiplication factor $K = 0.345$ is given. We see that the desired frequency component is very small compared to the adjacent components. For frequency synthesis this signal is not directly applicable. For other applications the momentary time error may in many cases be excessively large.

III. Accumulator Rate-Multiplier Principle

The accumulator principle for rate multiplication is depicted in Fig. 2(a) [19], [20]. This principle always delivers the best possible digital approximation of a regular signal. The programmed number P is added to a register with capacity Q each clock period. On overflow a clock pulse is passed. It is intuitively clear that this principle must deliver an optimally spaced output pulse pattern because upon overflow the remaining value is still stored in the register. The next overflow condition is biased with this value.

In Fig. 2(b), the possible waveforms of a BCD accumulator rate multiplier ($Q = 10$) are given. In contrast to Fig. 1(b), we see that, for instance, rate $\frac{5}{10}$ is perfectly regular. Consequently,

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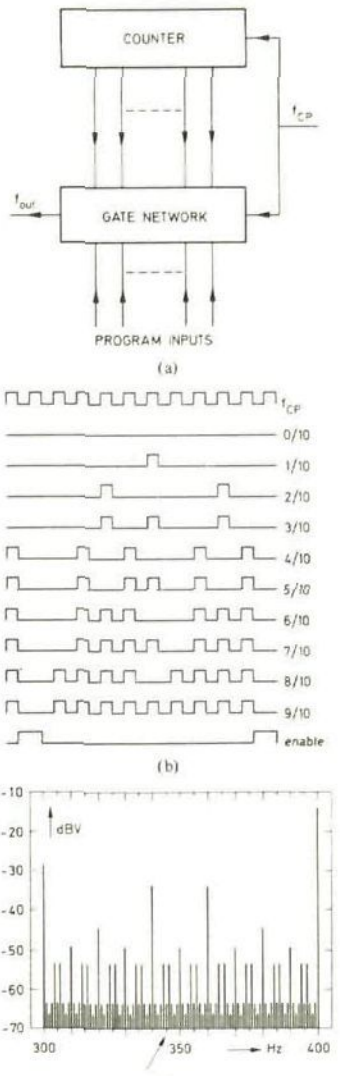

Fig. 1. (a) Common rate-multiplier principle. (b) Waveforms of a BCD rate multiplier (e.g., HEF 4527). Rate $\frac{5}{10}$ is not regular. (c) Output frequency spectrum of three cascaded BCD rate multipliers for $K = 0.345$.

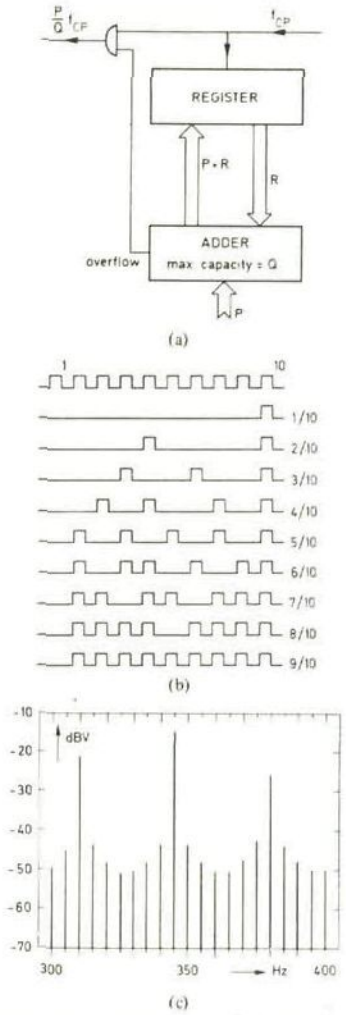

Fig. 2. (a) Accumulator rate-multiplier principle. (b) Waveforms of an accumulator rate multiplier for $Q = 10$. Rate $\frac{5}{10}$ is perfectly regular. (c) Output frequency spectrum of three cascaded BCD accumulator rate multipliers for $K = 0.345$.

the frequency spectrum of the output signal of an accumulator rate multiplier shows a considerable improvement. In Fig. 2(c), the frequency spectrum is given for a rate multiplication factor of 0.345. The desired frequency component has a magnitude roughly 30 dB greater than the adjacent components.

The principle is illustrated using an example in which $K = \frac{3}{10}$, and a comparison is made for a regular waveform, an optimally spaced pulse pattern, and a pulse sequence combination pattern. In the case of $K = \frac{3}{10}$, the maximum accumulator capacity is equal to 10 and the programmed number that is added each clock period is equal to 3. A really regular signal has a period time of $3\frac{1}{3}$ clock pulse period. However, in a digital system only whole clock pulse periods are available. Therefore, for a multiplication factor of $\frac{3}{10}$ it is impossible to generate a really regular signal. In Fig. 3, the phase values as a function of time of a regular signal and the best approximation are depicted. The accumulator rate multiplier acts as a "phase accumulating device." Each clock period, a value of 3 is added to the register. On overflow (≥ 10), an output pulse is passed. (This is comparable to a phase value of $\geq 2\pi$.) Assuming that the first pulse is on time, we see that the second one is $\frac{2}{3}$ of a clock period too late, while the third one is only $\frac{1}{3} T_{CK}$ too late. At the bottom of Fig. 3 the three waveforms are compared. The accumulator principle always delivers a peak-peak momentary time error smaller than $T_{CK} \cdot (P-1)/P$ for which the fraction P/Q must be simplified as far as possible.

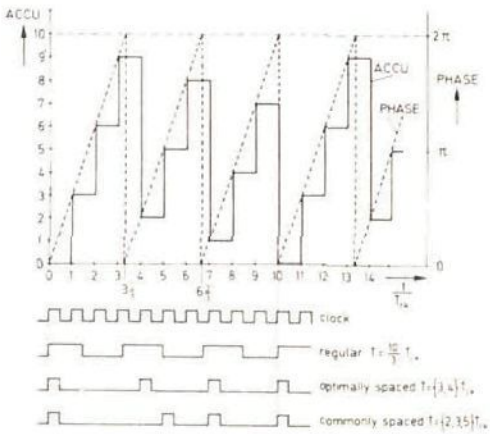

Fig. 3. The accumulator rate multiplier as a "phase accumulating device" that delivers the best possible digital approximation of a regular waveform with frequency $\frac{3}{16} \cdot f_{CK}$.

Only one disadvantage is connected with the accumulator scheme: it is inherently slower than the aforementioned pulse-sequence combination scheme. The IC design has been focused on speed improvement. In addition, as described in the following section the accumulator scheme can potentially broaden the range of applicability considerably.

IV. Circuit Design

The accumulator scheme for rate multiplication can easily be implemented as given in Fig. 2(a). However, for a symmetrical clock pulse the main speed restriction is formed by the propagation delay of the overflow signal. To prevent race conditions, this carry propagation delay has to be smaller than $\frac{1}{2}$ of a clock period. If the carry signal is resynchronized with one additional flip-flop, a speed improvement of at least a factor of 2 is gained. Further speed improvements are possible by extending the pipeline technique for every bit section. If the register is initally reset, this technique does not affect the optimality of the output pattern because only the output sequence is delayed one clock period. A fully pipelined structure can deliver only a denominator $Q = 2^N$. We have made a compromise to restrict one pipeline section to 4 bits because the circuit is not slowed down too much and versatility can be gained if binary and BCD rate multiplication can be combined into one circuit. In this case, available rate-multiplier IC's can be replaced by one new type.

The capacity of an N-bit accumulator can be artificially restricted to Q by an extra addition of 2^N-Q in case of overflow. For the BCD mode, a 4-bit accumulator capacity of 10 can be realized by adding $P + 6$ in the case of overflow, instead of P. This can be implemented as given in Fig. 4. The operating-speed-limiting propagation delays consist of two parallel paths: the register-adder path and the carry flip-flop multiplexer-adder path.

Because the main design goal was speed improvement, simulations were carried out with respect to the logic, transistor, and layout implementations. A standard cell approach had

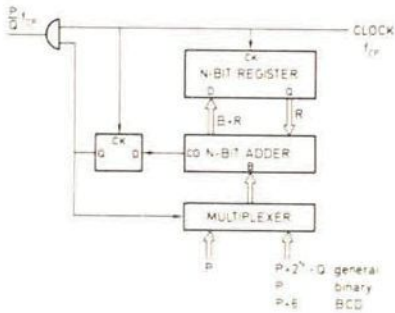

Fig. 4. Block diagram of an accumulator rate multiplier that gives speed improvement by pipelining and accumulator capacity restriction by using a multiplexer.

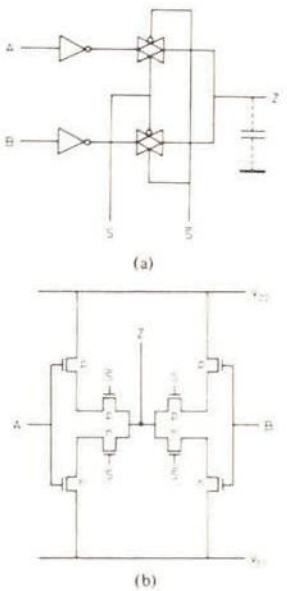

Fig. 5. Logic diagram (a) and transistor diagram (b) of a 1-bit multiplier section that is glitch-free.

limited applicability due to its inherently larger silicon area requirement. The only way to achieve speed in the logical configuration was to use a hand layout method with extensive application of transmission gate logic.

Transmission gate logic can also support the design in an other way. If the multiplexer circuitry is glitch-free, the binary mode can be faster because the multiplexer delay can be ignored, a switching action in case of overflow has to result in the same programmed number P. In Fig. 5, one section of the glitch-free multiplexer is given. Transmission gates (TG's) lead to a very simple transistor configuration. They can also be used to speed up the full adders [21].

The carry propagation delay plays an important role in the propagation delay paths. A main part of this study was related to the simulation and analysis of cascaded transmission gates

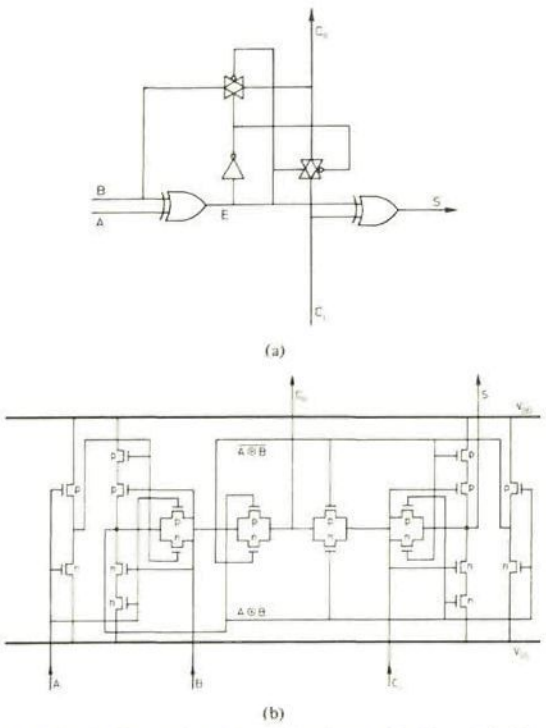

Fig. 6. Logic diagram (a) and transistor diagram (b) of one full-adder section of the accumulator.

for carry generation. As a result, in Fig. 6 the logic diagram and the transistor configuration of one full-adder section are given. When more full adders are cascaded, a chain of transmission gates will arise in which the carry signal can propagate very fast, for $V_{DD} = 15$ V, the propagation delay of a chain of four TG's is about 15 ns. The delay of a chain of TG's is found to be proportional to $N \cdot (N+1)$, in which N is the number of TG's. When the TG chain becomes too long, buffers have to be inserted to restore the signal. A simple optimization can be carried out to determine in which case a buffer is profitable. In our case (4 bits), it was not necessary to use a buffer in the carry chain.

The method described to limit the capacity of the accumulator also offers facility in the design of a general mode switching circuit that can deliver a programmable denominator Q for the rate multiplier. In this case, the other input of the multiplexer must be fed with the number $P + 2^N - Q = P + \overline{Q} + 1$ (mod 2^N). It is beyond the scope of this paper to describe this circuit in detail.

V. Product Definition

The design process might be one of continuous consultation in which thorough analysis of the various simulations led to the choice of a definitive configuration. In particular, restraints imposed by the pin requirements proved most educative.

A programmable denominator Q can broaden the application

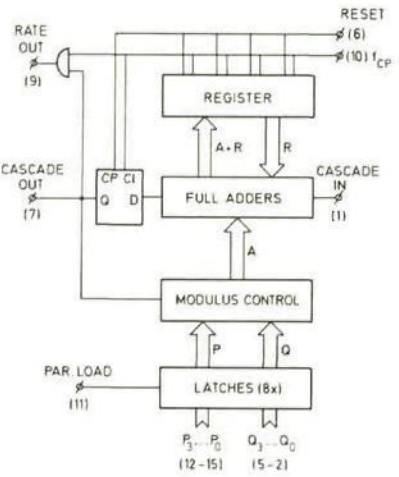

Fig. 7. Block diagram of the realized universal 4-bit rate multiplier/variable divider.

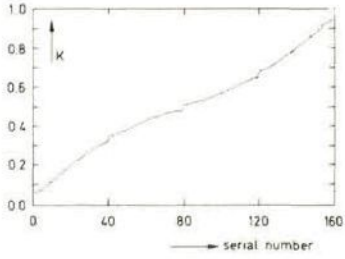

Fig. 8. Graphical representation of the multiplication factors of one rate-multiplier circuit with programmable P and Q.

area considerably. We have chosen the product definition given in Fig. 7. Both the numerator P and the denominator Q are programmable via transparent latches for compatibility in the microprocessor environment. The integrated circuit can be used as the following:

1) binary rate multiplier	$P = 0 \cdots 15$	$Q = 16$
2) BCD rate multiplier	$P = 0 \cdots 9$	$Q = 10$
3) variable divider	$P = 1$	$Q = 1 \cdots 17$.

Furthermore, the denominator Q can be programmed as, for example, $Q = 13$. Research has also been carried out for values $P \geq Q$. In this case, the extra addition in case of overflow takes place modulo 16. Then, the value of the denominator is equal to $Q + 16$. As a result, it appears that it is possible to generate 161 different rate-multiplication factors with one 4-bit unit. These are given in Fig. 8.

VI. Practical Results

The chip is realized using an industrial polysilicon gate CMOS process with a 4 μm gate length and local oxidation. The properties of the circuit can be summarized as follows:

1) optimally spaced output pulse distribution,

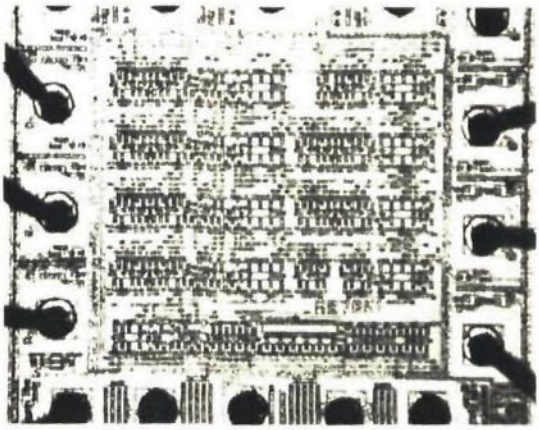

Fig. 9. Microphotograph of the rate multiplier.

2) both numerator P and denominator Q programmable via transparent latches,

3) easy cascading without any speed degradation,

4) *TTL compatible outputs (fan-out 5 LS-TTL loads),*

5) high clock frequency (typically 25 MHz, V_{DD} = 15 V), and

6) package 16-pin DIL, chip area 1.76 mm^2.

As an illustration, a micrograph of the chip is given in Fig. 9. The hand layout method and the transmission gate logic have resulted in a relatively high package density of 450 transistors/mm^2. Compared to standard gate logic, this corresponds to a high functional density. The circuit probably will become a member of the standard HEF 4000 series.

VII. Application

In Fig. 10, the cascading possibilities of the integrated circuit are depicted. There are two different cascading modes, namely the add mode and the multiply mode. It should be noted that the multiply mode does not deliver an optimally spaced output pulse pattern. In the add mode, the output pulses are always distributed in time as regularly as possible. Furthermore, we see that the denominator is always a product term. This results in the restriction that a prime number as denominator *is not possible. However, if we use the cascade input* of the first block we can realize a product term minus one. Other feedback methods to realize prime numbers are possible too. We call this the circular add mode.

Finally, some additional applications will be discussed. The realized rate-multiplier IC can be used as a frequency-synthesis system component. Both direct and indirect frequency synthesis systems are possible. The irregularity inherent to rate multiplication can be decreased by the well-known method of dividing the rate-multiplier output signal, or the signal can be used as input for a phase-lock loop (PLL) or frequency-locked loop in which the irregularity is averaged.

Since the programmed fraction P/Q is directly proportional to the dc value of the output signal, D/A conversion can be established by low-pass filtering. In this case, resolution can be exchanged for conversion speed.

The above-mentioned applications are now under investigation to realize PLL and frequency-synthesis systems in which full scope is given to the special features of the realized chip.

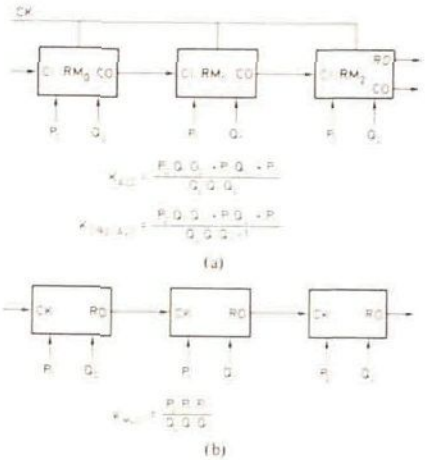

Fig. 10. Rate-multiplier circuits cascaded in the add mode (a) and the multiply mode (b). The circular add mode arises by connecting the cascade output of the last stage (CO2) to the cascade input of the first stage (CI0).

VIII. Conclusion

An integrated circuit for fast rate multiplication which delivers an optimally spaced output pulse distribution is described. This is the best possible digital approximation of a regular signal. The circuit is based on the accumulator principle. In addition, it is also possible to program the denominator Q of the rate-multiplication factor, broadening the application area considerably.

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A2.4

WELL-DEFINED SUB-NYQUIST SAMPLING-FREQUENCY RANGE LIMITS

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The concept of "harmonic mixing" frequency conversion of sample-and-hold circuits is presented to link the baseband and the bandpass sampling theorem. The frequency-conversion characteristic indicates spectral folding and inversion cases and clearly yields generally applicable theoretical minima and maxima for sub-Nyquist sampling frequencies as is used in modern analog and digital electronic systems. Moreover, the determination of whether or not phase-lock sampling is required is straightforward.

1. INTRODUCTION

Modern advanced phase-lock communication systems often employ digital-computer signal-processing, necessitating the conversion of modulated (bandpass) waveforms into a proper format for numerical processing with the help of some form of sampling. In sampled phase-lock systems a variable sampling frequency is used very often. In the case of the electronic implementation of these mixed analog/digital systems, it is important to make a proper selection of the sampling frequency and/or the frequency limits needed to obtain the desired sampled replica of the input signal.

The well-known baseband sampling theorem is easily understood: two points per shortest cycle are neccessary and sufficient for reconstruction. The bandpass version, or in other words the sub-Nyquist sampling theorem, however, is more difficult to comprehend and is usually applied straightforwardly without much insight into the theory behind it. In many textbooks (e.g. [1,2]) the baseband theorem is treated in a very comprehensive manner, however the bandpass version receives concise attention. Consequently there is a widely accepted rule-of-thumb for the minimum required bandpass sampling frequency, namely

$2B \leq f_s \leq 4B$.

The presentation of the "harmonic-mixing" frequency-conversion characteristic in terms of the minimum baseband sampling frequency $f_s = 2B$ allows one to get a better grip on this process basical to the general telecommunications properties of sampling circuits.

2. FREQUENCY-CONVERSION CHARACTERISTICS OF SAMPLE-AND-HOLD (SH) CIRCUITS

The frequency-conversion characteristic which depicts the input frequency versus the output frequency of a SH is given in Fig. 1 for a minimum baseband sampling frequency $f_s = 2B$. The bandpass sampling theorem as well as the baseband version is clearly illustrated; the input pass bands B0, B1 and B2 are converted to baseband on one of the slopes without aliasing, but the conversion of B1 delivers an inverted baseband spectrum (not allowed for e.g. SSB).

The input band B0 corresponds to the case of baseband sampling whereas the frequency bands B1 and B2 are located at sub-Nyquist sampling positions, in which the minimum sampling frequency 2B can be used. However for the input pass bands B3 and B4 aliasing occurs, so in these cases the sampling frequency has to be increased. It can easily be understood that, to prevent aliasing and spectrum inversion, for some locations of the input passband determined by the harmonic number, the minimum sampling

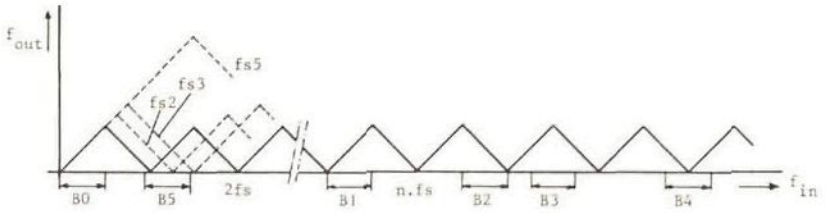

Fig.1 Frequency-conversion characteristics of a sample-and-hold circuit.

frequency must have a value higher than 2B.
The absolute position of the input pass band rather than the relative bandwidth determines whether or not the minimum baseband sampling frequency has to be increased. In Fig.1 also the characteristics for higher sampling frequencies fs2 and fs3 are partly given. To prevent aliasing the discontinuities have to remain ouside the passband to be converted.
A remarkable result of the proposed approach is that fs has to be larger than 2B in the case of spectral inversion as well, which cannot directly be concluded from the theories presented in the literature. As will be explained in the next section the upper and lower limits of the sampling frequency can be *exactly determined in terms of the minimum* baseband sampling frequency.

3. COMBINED BASEBAND AND SUB-NYQUIST SAMPLING RATE LIMITS

From the frequency-conversion characteristic it can be determined which requirements are *necessary to obtain the desired sampled replica* of the input spectrum. In accordance with the literature, the LOWEST sampling frequency for preventing spectral folding (or aliasing) can be formulated as

$$fs/B >= 2(1 + fo/B)/(INT(fo/B) + 1) \qquad (1)$$

in which fo is the lowest frequency of the input pass band and INT(fo/B) is the LARGEST positive integer, which satisfies the relation smaller than or equal to fo/B.
However, there exist also local MAXIMUM sampling frequencies for a given input pass band. Although this is not mentioned in the literature, it can be a serious source of trouble in practice. From Fig. 1 one can conclude that for the exact minimum sampling frequency of the input pass band B1 an increase of the sampling frequency can cause either folding on another slope or even inversion of the baseband spectrum. For a non-folded sampled replica, conversion must take place on just one slope of the characteristic.
A non-folded sampled replica can be obtained if the sampling frequency satisfies fo>= Mfs/2 and fo + B < (M +1)fs/2, in which M = INT(fo/B). This results in the following constraints for the sampling rate:

$$2(1+fo/B)/(M+1) < fs/B <= (2/M)(fo/B) \qquad (2)$$

If the sampled spectrum is not allowed to be inverted, the constraints for the minimum sampling frequency are more severe. If M is odd *the input spectrum is converted to an inverted* baseband spectrum. The above derived results are complementary to results presented in the literature.
Minimum and local maximum sampling frequencies in accordance with Eq.(2) are plotted in Fig.2 against the normalized lowest frequency of the input pass band. Usually the parts of Fig.2 with the bold lines, which represent the left part of the expression (2) derived, are given. As can be seen only the shaded areas correspond to this expression.
Even the widely accepted rule for the minimum sub-Nyquist sampling frequency, which states that fs must have a value between 2B and 4B, is not generally true; a spectrum (see B5 in Fig.1) with a lowest frequency fo just under the baseband sampling frequency which has to be converted non-folded and non-inverted, requires a minimum sampling rate of at least 6B !

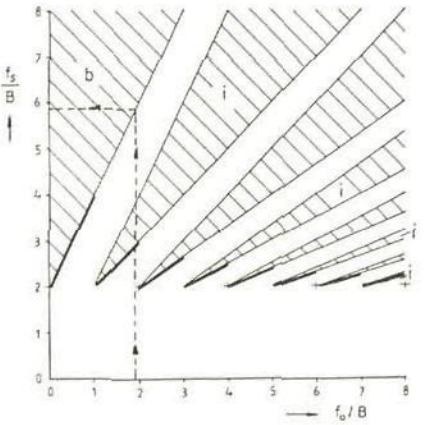

Fig.2 Sampling frequency range limits for a band of width B.

It should be noted that if the sampling frequency is varied for a specific input pass band, spectral inversion alternates with non-inversion. Obviously the permitted ranges of the sampling frequency decrease with larger values of M. For high ratios of fo/B the limits for a minimum sampling rate require at least some form of frequency-lock. In many cases, especially in satellite communication systems in which Doppler shifts occur, sampled phase-lock systems with a variable sampling frequency are required by virtue of the above-described reasons only.

4. CONCLUSIONS

With the concept of the harmonic-mixing frequency-conversion characteristic of the sample-and-hold circuit it is demonstrated why the common sub-Nyquist sampling rule-of-thumb does not yield the correct results for every input pass band. For input pass bands (fo+B) with a lowest frequency (fo) located slightly under the minimum baseband sampling frequency (2B), it has been found that the sampling rate

has to be at least 6B instead of the commonly assumed value of 4B. For input spectra located far above the minimum sampling frequency the necessary requirements for the sampling frequency in terms of magnitude and stability *can be exactly determined.*

The proposed concept covers baseband as well as sub-Nyquist (or bandpass) sampling and reveals directly the shortcomings of the standard approximations. The method can be applied in both industrial and academic research areas where the choice of a sampling frequency influences the system properties as well as in textbooks which treat electronic communications engineering.

In [3] the proposed concept of using the harmonic-mixing frequency-conversion characteristic in relation to the sub-Nyquist theorem is applied to the new design of correlation loop components of a direct-sequence spread-spectrum receiver.

5. ACKNOWLEDGEMENTS

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A2.6

A NEW DESPREADING METHOD BASED ON SUB-NYQUIST SAMPLING

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This paper describes a new despreading method, based on sub-Nyquist sampling, for a direct sequence spread spectrum receiver. It is theoretically proved that with one or two sample-and-hold circuits a despreader can be realized, having correlation properties approximately equal to those of an ideal despreader, if certain conditions are met. The proposed method can be very useful for the design of new silicon integrated phase-lock communication system components in which a conversion to numerical processing is necessary.

1. INTRODUCTION

The incoming signal of a direct sequence spread spectrum receiver consists of an information bearing digital data signal and a (spreading) pseudo-random noise sequence, BPSK-modulated onto a carrier. The most important part of such a receiver is the correlator loop which despreads the incoming signal. Since the fundamental aspect of despreading is correlation and since correlation is based on integration after multiplication, common despreaders have a multiplier (or mixer) as central component.

Three basic despreading methods can be distinguished [1]: heterodyne, in-line and baseband correlation. Baseband correlation can be accomplished if the BPSK signal can be coherently demodulated (with some sort of phase-lock loop) before being correlated, which is only possible with relatively high input signal-to-noise ratios. The difference between heterodyne and in-line correlation is that with the former the signal, besides being correlated with the reference signal, is also converted to another frequency band, whereas with the latter it is not (see also Fig. 1).

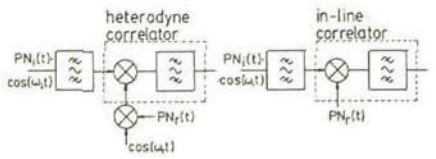

Figure 1

The correlator is the point in the receiver where process gain is achieved and where potential jammers are suppressed. Therefore, it is essential that jammers cannot reach parts of the receiver behind the correlator. Every correlation mixer, however, has some stray coupling from its input to its output. Consequently, if a (strong) jammer is present at the input of the correlator, an attenuated part will be coupled to the output of the correlation mixer. If in-line correlation is used, a jammer which is coupled to the output of the correlation mixer, although attenuated, can nevertheless interfere with the correlated (wanted) signal, since they are in the same frequency band. This obviously degrades the anti-jamming capability and can even make correct operation impossible. If, on the other hand, heterodyne correlation is used, the bypassed (attenuated) jammer will be in another frequency band than the correlated (wanted) signal and will therefore be strongly suppressed by the correlation band-pass filter.

2. SAMPLING DESPREADING.

Modern advanced phase-lock communication systems often employ digital signal processing, where it is necessary to convert input (band-pass) signals into a proper format for numerical processing, using some form of sampling. The possibility of despreading with sample-and-hold (SH) circuits would simplify the interface to a digital signal processor and would allow time-multiplexing of separate channels. However, the SH circuit can only "multiply" by "one" and "zero", whereas the common correlation mixer can multiply by positive as well as negative values. Therefore, the SH circuit has to be modified. Analogously to heterodyne correlation, any modification should obey the rule that input and output frequency bands of the correlator are different. Two configurations having the required properties have been found; they are based on sub-Nyquist sampling.

3. THE DOUBLE-SH DESPREADER.

The modification consists essentially in enabling the SH circuit to sample with delta functions with either positive or negative coefficients. With this in mind, the following basic principle was found: the modified SH circuit should sample the non-inverted incoming signal whenever the reference pseudo-noise code is equal to "1", and it should sample the inverted incoming signal whenever the reference pseudo-noise code is equal to "-1".

This can be realized with the circuit given in Fig. 2, which contains two SH circuits in the sub-Nyquist sampling mode, ending in one hold capacitor. Since sub-Nyquist sampling is used, the input and output frequency bands of the double-SH despreader are different. The *incoming and reference maximal length pseudo-*noise codes (henceforth: PN codes) are defined as

$$PN_i(t)=\sum_{j=-\infty}^{\infty} c[j]\,\mathrm{rect}\{(t-(j+1/2)T_{ci}-\tau_i)/T_{ci}\} \quad (1)$$

$$PN_r(t)=\sum_{k=-\infty}^{\infty} c[k]\,\mathrm{rect}\{(t-(k+1/2)T_{cr}-\tau_r)/T_{cr}\} \quad (2)$$

where $\mathrm{rect}(x)=1$, $-1/2<x<1/2$

$=0$, $|x|>1/2$ (3)

$f_{ci}=1/T_{ci}$ and $f_{cr}=1/T_{cr}$ are the clock frequencies of the PN codes. Furthermore,

$$c[j]=c[j+L]=\pm 1 \quad (4)$$

where L is the code length.

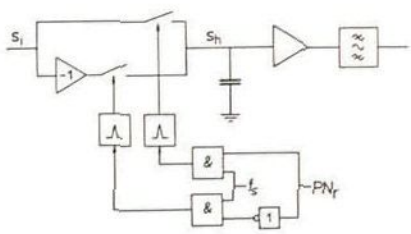

Figure 2 : Double-SH despreader

The incoming signal is modelled as a carrier BPSK-modulated by a PN code. Hence

$$s_i(t)=PN_i(t)\cos(\omega_i t+\phi_i) \quad (5)$$

The sampling function is defined as

$$\Delta(t)=\sum_{n=-\infty}^{\infty}\delta(t-nT_S-\tau_S) \quad (6)$$

where $f_S=1/T_S$ is the sampling frequency and $|\tau_S|<T_S$.

With (1-6) and using some elementary sampling theory we finally arrive at an expression for the signal across the hold capacitor (* stands for convolution)

$$s_h(t)=\mathrm{rect}\{(t-T_S/2)/T_S\}*\{s_i(t)PN_r(t)\Delta(t)\} \quad (7)$$

From (5-7) we find

$$s_h(t)=\sum_{n=-\infty}^{\infty} PN_i(nT_S+\tau_S)PN_r(nT_S+\tau_S)\cos(\omega_i nT_S+\omega_i\tau_S+\phi_i)\,\mathrm{rect}\{(t-(n+1/2)T_S-\tau_S)/T_S\} \quad (8)$$

Confining ourselves to the case $f_{ci}=f_{cr}=f_c=1/T_c$ and defining $\tau=\tau_i-\tau_r$, we have with (1-4)

$$PN_r(t)=PN_i(t+\tau) \quad (9)$$

Furthermore, for simplicity we will restrict ourselves to synchronous sampling, i.e $\omega_i=N\omega_S$ and $\cos(\omega_i\tau_S+\phi_i)=1$. Then we find

$$s_h(t,\tau)=\sum_{n=-\infty}^{\infty} PN_i(nT_S+\tau_S)PN_i(nT_S+\tau_S+\tau)\cdot\mathrm{rect}\{(t-(n+1/2)T_S-\tau_S)/T_S\} \quad (10)$$

The common auto-correlation function, $R(\tau)$, of $PN_i(t)$ is [2]

$$R(\tau)=\frac{1}{LT_c}\int_0^{LT_c} PN_i(t)PN_i(t+\tau)dt \quad (11)$$

The pseudo auto-correlation function is now defined as

$$R_{ps}(\tau)=\frac{1}{LT_c}\int_{\tau_S}^{\tau_S+LT_c} s_h(t,\tau)dt \quad (12)$$

which depends on τ_S. Substituting (10) in (12) we find

$$R_{ps}(\tau)=\sum_{n=0}^{M} PN_i(nT_S+\tau_S)PN_i(nT_S+\tau_S+\tau)(T_S/LT_c)\cdot+PN_i\{(M+1)T_S+\tau_S\}PN_i\{(M+1)T_S+\tau_S+\tau\}\cdot\cdot(LT_c-MT_S)/LT_c \quad (13)$$

where $M=\mathrm{int}(LT_c/T_S)$ (14)

Without loss of generality we now choose $\tau_i=0$. Since $\mathrm{rect}\{(t-(j+1/2)T_c)/T_c\}=1$ only if $jT_c<t<(j+1)T_c \Rightarrow j=\mathrm{int}(t/T_c)$, we have with (1)

$$PN_i(t)=c[\mathrm{int}(t/T_c)] \quad (15)$$

Finally, from (1,13-15) we obtain

$$R_{ps}(\tau)=\sum_{n=0}^{M} c[\mathrm{int}\{(nT_S+\tau_S)/T_c\}]c[\mathrm{int}\{(nT_S+\tau_S+\tau)/T_c\}]T_S/LT_c+c[\mathrm{int}\{((M+1)T_S+\tau_S)/T_c\}]c[\mathrm{int}\{((M+1)T_S+\tau_S+\tau)/T_c\}]\cdot\cdot(LT_c-MT_S)/LT_c \quad (16)$$

So far no answer has been given to the question of how large the sampling frequency should be in relation to the code clock frequency. When we reconsider (7), we see that the mathematical description of the double-SH despreader is the

same as that of the circuit in Fig. 3, where $s_{dsp}(t)=PN_r(t)s_i(t)$.

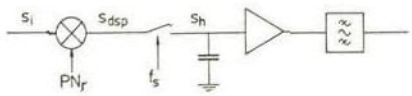

Figure 3

The only criterion to be met is that no significant aliasing errors may occur in that part of the spectrum of s_h that is passed by the correlation filter. In deriving Eq.(16) the correlation bandwidth was chosen infinitesimally small, since only the DC-component of s_h was of interest. In a practical despreading stage the correlation bandwidth is determined by the carrier frequency uncertainty of the incoming signal.

In accordance with [3], the upper limit of the minimum sampling frequency (f_{smin}) is determined by not allowing any aliasing errors in s_h. This means that f_s has to be related to the bandwidth and carrier frequency of s_{dsp}.

Holmes [2] analyzed the spectrum of the despread waveform (s_{dsp}), for baseband correlation and for the noise-free situation. Roughly interpreting his results, we have:

(i) For $|\tau|\leq T_c$ almost all power of s_{dsp} is concentrated in a (two-sided) bandwidth of approximately $2f_c$.

(ii) For $T_c<|\tau|<LT_c-T_c$ almost all power of s_{dsp} is concentrated in a (two-sided) bandwidth of approximately $4f_c$.

However, since R_{ps} is small anyway in case (ii), aliasing errors in this range are not important for a despreading stage.

Therefore, for the case of synchronous sampling (according to [3]) we have $f_{smin}<2f_c$. The lower limit of f_{smin} is f_c since every code chip has to be sampled at least once. It must be stressed that these considerations only apply to the noise-free case. In the presence of noise f_{smin} will be larger.

Eq.(16) has to be evaluated numerically. However, one simple case can be solved analytically: the case in which $f_s=f_c$. The resulting pseudo auto-correlation function for $\tau_s=T_c/2$ together with $R(\tau)$ is given in Fig. 4.

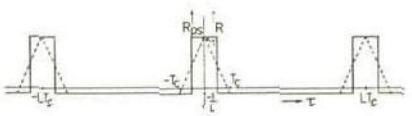

Figure 4

In this case every code chip is sampled exactly once at exactly the same position after the beginning of each chip. However, if $f_s=rf_c+\Delta f$ (where $0<\Delta f<f_c$), each code chip is sampled "r" times at different moments after the beginning of each chip, and a smoother pseudo auto-correlation function will result. In other words, if we avoid synchronous relations between f_s and f_c, the auto-correlation function will be approximated more closely.

This is demonstrated by Figs. 5-7, which are computer evaluations of Eq.(16), and which also show that the resemblance to the auto-correlation function improves with larger code lengths *and larger f_s. Moreover, they show that for* larger code lengths f_{smin} has to be only slightly larger than f_c (for the noise-free case).

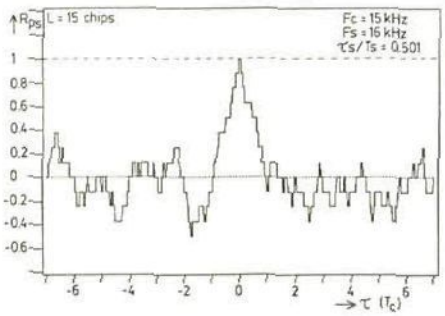

Figure 5 : Double-SH despreader

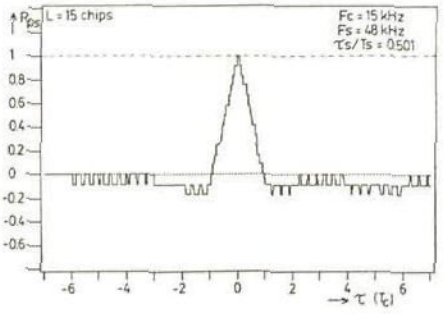

Figure 6 : Double-SH despreader

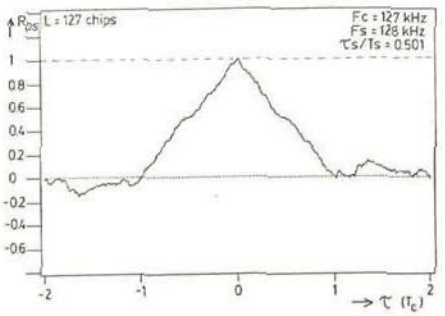

Figure 7 : Double-SH despreader

4. THE SINGLE-SH DESPREADER.

The double-SH despreader described in the previous section contains two SH circuits and two sampling pulse generators. In view of an economical electronic implementation it would be preferable if a sampling despreader containing only one SH circuit and only one sampling pulse generator could be realized .

In that situation the only possibility left in processing the incoming signal would be to delay the sampling pulses as a function of the reference PN code.

Delaying the sampling pulses over one half of the carrier period will result in an inverted sampled signal with respect to the sampled signal with no time delay. This being so, the function of the single-SH despreader can be defined as follows: the incoming signal is to be sampled by the non-delayed sampling pulses if the reference PN code is equal to "1", and by time-delayed sampling pulses if the reference PN code is equal to "-1". The time-delay has to be one half of the carrier period, i.e. $T_d=T_i/2$. If the carrier frequency can be considered practically constant, a constant time delay can be used. The resulting single-SH despreader is given in Fig. 8.

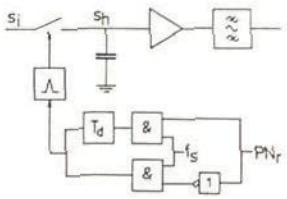

Figure 8 : Single-SH despreader

Keeping (1-6) in mind, we find for the sampling moments of the single-SH despreader

$$t[n]=nT_S+\tau_S+[1-PN_r(nT_S+\tau_S)]T_i/4 \qquad (17)$$

Analogously to the mathematical description of the double-SH despreader we arrive at

$$s_h(t)=\sum_{n=-\infty}^{\infty} s_i(t[n])\,\mathrm{rect}\{(t-(t[n+1]+t[n])/2)/(t[n+1]-t[n])\} \qquad (18)$$

Confining ourselves to the case of synchronous sampling, i.e. $\omega_i=N\omega_S$ and $\cos(\omega_i\tau_S+\phi_i)=1$, we have

$$s_i(t[n])=PN_i(t[n])PN_r(nT_S+\tau_S) \qquad (19)$$

Furthermore, we will restrict ourselves to the case of the code clock frequencies being equal, i.e. $f_{ci}=f_{cr}=f_c=1/T_c$, and we define $\tau=\tau_i-\tau_r$. Finally, analogously to (12) and with (14), we find

$$R_{ps}(\tau)=\frac{1}{LT_c}\int_{t[0]}^{t[0]+LT_c} s_h(t,\tau)dt$$
$$=\frac{1}{LT_c}\{\sum_{n=0}^{M} PN_i(t[n])PN_r(nT_S+\tau_S)\cdot$$
$$\cdot(t[n+1]-t[n])+PN_i(t[M+1])\cdot$$
$$\cdot PN_r((M+1)T_S+\tau_S)(LT_c-t[M])\} \qquad (20)$$

Eq.(20) has to be evaluated numerically.

By comparing (13) and (20) it can easily be verified that in cases where $T_i \ll T_S$, the single- and double-SH despreader give the same results. On the other hand, if T_i is of the same order of magnitude as T_S the performance of the single-SH despreader is somewhat less than that of the double-SH despreader, as is shown by Fig. 9 (which should be compared to Fig. 7).

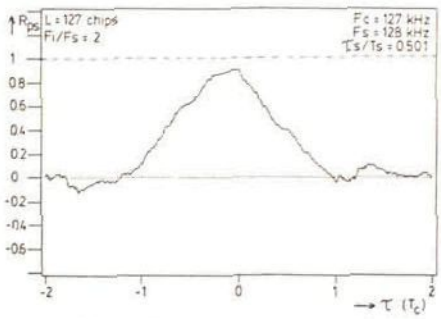

Figure 9 : Single-SH despreader

5. CONCLUSIONS

With the concept of sampling despreading of direct sequence spread spectrum signals, new receiver architectures are possible. It can be shown that the correlation properties of the single- and double-SH despreader approximate those of an ideal despreader if the code length is sufficiently large and if the sampling frequency is asynchronous to the code clock frequency. The single-SH despreader can only be used if the time-delay can be related accurately enough to the carrier frequency of the incoming signal.

The proposed method is to be used for the design of new generally applicable integrated circuit components for spread spectrum systems.

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A NEW SECOND ORDER COSTAS DPLL CONFIGURATION

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A new second-order all digital phase-lock loop is described that can be applied in a BPSK carrier synchronizer and data demodulator. The proposed loop configuration allows the lock range to be designed independently of the noise bandwidth , unlike common (cascaded first order) loop configurations. The proposed loop can give information in a numerical format on the phase and frequency estimate of the input signal. Moreover, the configuration is ideally suitable for integration in silicon.

1. INTRODUCTION

Phase-lock loops play an important role in communication systems. With the development of large-scale integrated circuitry, there is a trend toward digital phase-lock loops (DPLL's). Some advantages of the DPLL's are their entirely digital design, programmable bandwidth and center frequency, and an accuracy that is not affected by temperature and supply voltage variations.

The errors associated with digital systems, such as quantization, round off and overflow are minor compared to the advantages.

Lindsey and Chie [1] categorize the different DPLL implementations into four classes, based on the mechanization of the phase detector (PD):
1) Lag/Lead DPLL in which the PD determines at each cycle whether the input leads or lags behind the Digital Controlled Oscillator (DCO);
2) Zero Crossing DPLL in which the loop tries to sample at the zero crossings of the incoming signal;
3) Nyquist rate DPLL in which the input is sampled at the Nyquist rate; and
4) Duty Cycle DPLL in which the phase detector delivers a duty cycle proportional to the phase error. Possible phase detectors are the EXOR and the Set Reset Flip Flop.

This article concentrates on the duty cycle DPLL. Advantages of this type of DPLL are its linearity, its relatively easy implementation and its resemblance to the analog implementation of a PLL.

2. FIRST-ORDER DUTY CYCLE DPLL

A first-order duty cycle DPLL can be implemented as is depicted in Fig.1 with a commercially available integrated circuit such as 74LS297 OR 74HC/HCT297. The DCO consists of a modulo-K counter and an Increment/Decrement (I/D) circuit [2] and is controlled by the output of a duty cycle phase detector. The K-counter consists of an up-counter and a down-counter with respectively carry and borrow outputs. The Up/Down input controls which part (up or down) of the K-counter is in operation at a particular instant. The frequency of the carry pulses minus the frequency of the borrow pulses is proportional to the duty cycle from the phase detector. The I/D circuit produces an output frequency equal to one half I/D clock frequency when no carry or borrow is in process (Fig.2 waveform b). Carry pulses will be added to half the clock frequency (waveform c), while borrow pulses are subtracted from half the clock frequency (waveform d). The I/D output frequency varies linearly with the input duty cycle.

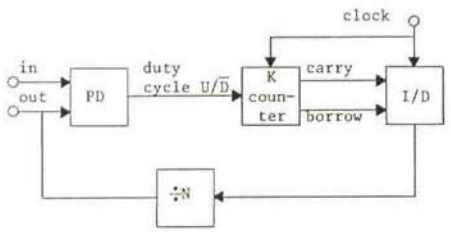

Fig.1 First-order DPLL

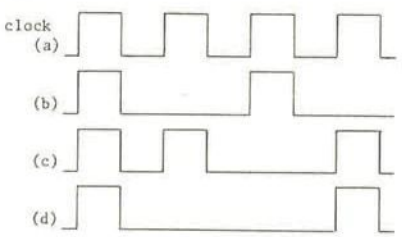

Fig.2 I/D circuit waveforms

Since the output transitions of the DPLL are synchronous with the clock used, the output phase is quantized. The ratio of the clock frequency and the output frequency, fixed by the divide by N-counter behind the DCO, determines the phase resolution.

The behavior of the first order DPLL is equivalent to a first-order analog PLL with a linear PD characteristic. The noise bandwidth is determined by the loop gain, while the lock range is determined by both the maximum phase error and the loop gain. Lock range and noise bandwidth can therefore not be chosen independently. Since the first order DPLL proposed by Iritani [3] uses an edge triggered PD with a linear range modulo $N \cdot \pi (N>>2)$ the noise bandwidth can be chosen regardless of the lock range. However, a disadvantage of a PLL employing an edge triggered PD is its degraded noise performance.

In order to create independent loop parameters as in the analog case, a higher order loop is needed.

3. HIGHER ORDER DPLL's

Digital loop filters in this category cannot be implemented easily. It is difficult to realize a digital integrating filter using duty cycles as input and output signals. It is therefore customary to create higher order loops by cascading first-order loops. In the literature all the possible ways of cascading first order loops to create a second-order DPLL are shown [3]. By cascading two first-order DPLL's and controlling the free running frequency of one DCO by the other phase error a second-order DPLL is constructed.

Although a perfect second-order loop can be created, the lock range is still determined by a first-order loop, and as a consequence the noise bandwidth and lock range can not be chosen independently.

4. THE NOVEL SECOND ORDER DPLL

The proposed perfect second-order loop consists of only one loop. As is known a loop filter can be realized by adding a proportional and integrating path [4]. In our configuration (see Fig.3) the proportional path consists, as in the first-order configuration, of Fig.1, of the modulo-K counter and the I/D circuit. The integrating path is formed by the modulo-K counter, Up/Down Counter (UDC) and the rate multiplier (RM). A rate multiplier is a digital circuit that multiplies an incoming frequency by a digital number $K=P/Q$ (P,Q integer, $K \leq 1$) [5]. The integral and proportional path are added in the I/D circuit after they have been converted to frequencies.

The operation can be explained as follows: Assume a step function behind the phase detector (the control duty cycle changes from 50 to 100 percent). At a 100 % duty cycle the K-counter counts up only, generating carry pulses. These pulses have two disjoint effects:
-The carry pulses are added in the I/D circuit to half the fraction (P/2Q) of the clock frequency, generating a DCO frequency step (proportional path of the loop filter).
-The Up/Down counter counts up every carry pulse, so the rate multiplier will generate a frequency ramp (integrating path of the loop filter).

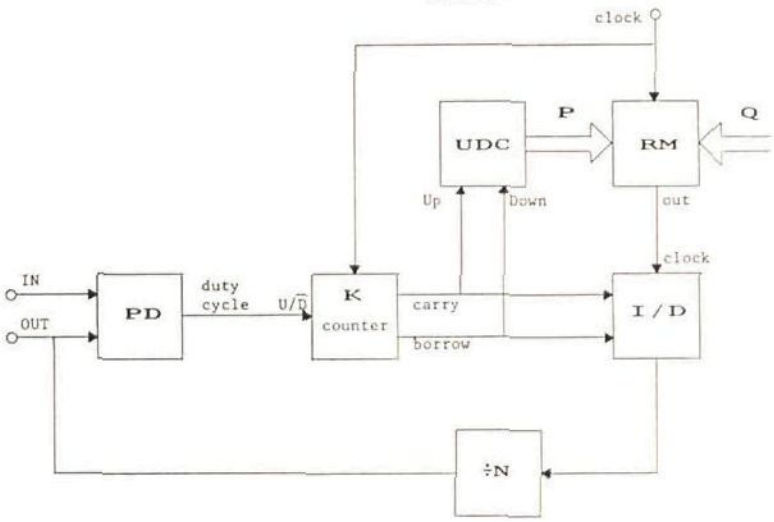

Fig.3 Proposed second-order DPLL

The behavior of the proposed second-order loop is equivalent to a perfect second-order analog PLL. The lock range theoretically lies between Fclock/2N and zero. The lock range can be limited by using an Up/Down counter with limitations. The noise bandwidth can be chosen by varying the proportional and integral gain. The lock range and noise bandwidth can be chosen fully independently, unlike the cascaded first-order configurations.

4.1 Acquisition of second-order duty cycle DPLL's

The acquisition behavior is quite similar to that of a perfect second order analog PLL. For small initial frequency errors the loop will lock within one phase transient (phase acquisition). *This phase aquisition range is determined* by the proportional loop gain.

For larger initial frequency errors the loop can also reach phase lock after skipping some cycles (frequency acquisition). The frequency difference results in a beat note behind the PD. The controlled oscillator will be phase modulated by this beat note. In the analog case this results in a pull-in voltage and in the digital case a pull-in duty cycle. The pull-in range is limited by the phase quantization: The DCO phase modulation must exceed this quantization to deliver the pull-in duty cycle.

4.2 Phase jitter of duty cycle DPLL's

The DCO output signal will show phase jitter, even if the input signal is noise free. The zero crossings of the DCO are always synchronous with the clock transitions. For an optimally spaced output signal the time jitter amounts to + or - 1/2 clock period, while the phase jitter is determined by the ratio of the clock frequency and the output frequency.

The output signal of a first order DPLL can be optimally spaced. However the output signal of a second order DPLL is more badly spaced since there are always two independent quantizations.

For our DPLL this results in a time jitter of + or - 1 clock period if the loop is locked on to the upper lock range limit (F-upper = Fclock/N). For lower input frequencies the time jitter will increase since the I/D clock frequency is reduced, so that the quantizations in the proportional path are magnified (see Fig.3). To minimize this additional jitter the I/D clock frequency has to be chosen as high as possible: This implies a divide by N-counter as large as possible. At F-upper/2 the time jitter already amounts to + or - 1.5 clock period.

5. NEW COSTAS DPLL APPLICATIONS

DPLL's can only handle input frequencies an order of magnitude lower than the clock frequency used. However, if bandwidth and carrier/sample frequency requirements can be fulfilled [6] input frequencies much higher can also be applied, because the digital equivalent of the S&H circuit mentioned in [6] can be used as a "harmonic mixer". However, the common baseband Nyquist applications are FSK detection, transition tracking clock synchronizers [7], motor speed control, noise filtering, tone recognition, frequency synchronization and multiplication.

The proposed loop is ideally suitable for a Costas loop carrier synchronizer and data demodulator for BPSK detection because in lock no static phase error exists. The fundamental difference between a Costas PLL and a conventional PLL in the analog case is the PD characteristic. This characteristic is periodic, recurring every 180 degrees, thereby wiping out *the effect of the BPSK modulation. By multiply*ing the outputs of two quadrature phase detectors a 180 degree periodic PD characteristic is created (see Fig 4).

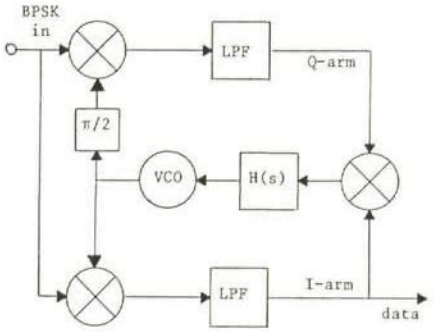

Fig.4 Analog Costas implementation

A simpler Costas implementation uses a hard limiter in the I-arm [8]. The limiter signal only decides whether the loop gain of the loop formed by Q-arm PD the loopfilter and the VCO has to be reversed. This configuration has been implemented digitally (see Fig.5). The loop gain reversals are realized by inverting the

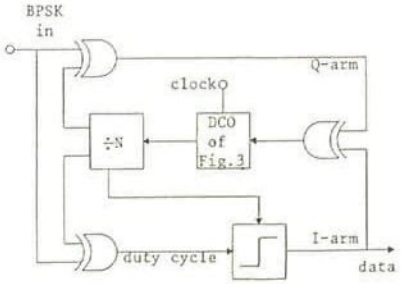

Fig.5 Digital Costas implementation

Q-arm duty cycle in the third EXOR. Since arm filters using duty cycles as input and output signals can hardly be implemented, the input noise bandwidth has to be determined by a band-pass filter.

Special attention must be paid to the I-arm hard limiter: This limiter has to determine whether the I-arm duty cycle is greater or less than 50 %, so a duty cycle hard limiter is required. This limiter can be implemented by (see Fig.6):

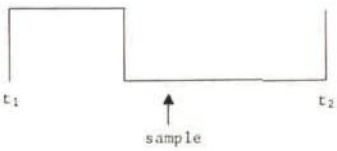

Fig.6 output signal of I-arm phase detector

-Integrate and dump. The interval t_1-t_2 is known since this is half a output period. During this interval the duty cycle can be integrated in an Up/Down counter. At t_2 a decision is made and the counter will be reset for the next cycle. A fast Up/Down counter is needed.
-Assume the duty cycle has only one transition during t_1-t_2 (see Fig.6). As long as this assumption is valid the duty cycle can be hard limited by sampling in the middle of the interval t_1-t_2. This Costas implementation uses only two EXORs and a D type flip-flop in addition to our proposed normal second-order DPLL.

6. CONCLUSION

With the configuration described the lock range and noise bandwidth of all-digital phase-locked loops can be designed independently. The analysis of the loop has shown that the acquisition is equivalent to analog PLL's and the residual phase jitter is inherent to the quantizations of time which exist in every digital mechanization of a PLL. A perfect second-order Costas loop can be implemented easily.

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A NEW MULTIPLYING PHASE DETECTION METHOD FOR CHARGE-PUMP PHASE-LOCK LOOPS

by Richard C. Den Dulk

Abstract

A multiplicative phase detection method for integrated Phase-Lock Loop (PLL) circuits is proposed. This method combines the low ripple of sequential Phase-and-Frequency Detectors (PFD) and the good noise performance of multiplicative phase detectors. The operating principle is described and electronic implementation examples are derived. The presented new phase detector circuits can be used in versatile, high- performance, integrated PLL circuits. These Charge-Pump PLLs with passive filter show good noise performance, zero static phase difference and low phase detector ripple.

Introduction

The availability of integrated phase-lock loop (PLL) circuits has broadened the application area of PLLs. There are several texts, in which the analysis and the design of a PLL are examined in one way or another. The interrelation of PLL system performance and considerations of the electronic implementation of the circuitry have been paid little attention, especially in the case of major design compromises of a PLL, such as the considerations to design the tracking mode, the acquisition mode and the considerations for noise performance and phase detector ripple.

The performance of a Phase-Lock system depends strongly on the electronic implementation of the applied phase detector circuit.

In the following some Phase-Lock system properties are given in relation to phase detector circuits.

A new phase detection method is described and several electronic implementations are proposed.

System performance

In Phase-Lock Loop terminology, it should be common practice to distinguish between Multiplicative (MPD) and Sequential Phase Detectors (SPD) [1]. Both types have different characteristics.

MPDs can operate in PLLs for signals deeply buried in noise (for instance: SNR = –20 dB), whereas SPDs are generally very sensitive to noise.

MPDs have an output signal which has a second-harmonic ripple term, in addition to the desired DC-term. The ripple term of the phase detector output signal may cause serious trouble in frequency synthesis PLLs, because the ripple generates spurious signals.

The static phase difference of MPD-loops is always equal to $\pi/2$.

Three-output-state SPDs that are inactive in the case of zero phase difference mostly show a low ripple term.

SPDs may also act as a phase detector with built-in acquisition-aid (Phase-and-Frequency Detector) or be specially designed to improve the acquisition performance of a PLL considerably [2].

Moreover, three-output-state sequential phase detectors enable us to make use of charge-pump-type loop filters (zero phase error without active filters). Although it is claimed that MPDs with three-state-output exist [3,4], the fact that the output of these circuits remains active, for zero phase error, prevents the use of Charge Pumps (CPs) in this case, because of the high probability of false-locks [5].

In the following it is shown that the proposed phase detection method results in MPDs with a real Inactive State (MPDIS). The ripple term is also removed by applying a compensation method to the conventional MPD. We will discuss the principles of the compensation method, the electronic implementation possibilities of the MPDIS and some experimental results. The resulting MPDIS circuits offer many possible applications with a considerably improved PLL performance. With this MPDIS it is possible to realize multiplicative Charge-Pump Phase-Lock Loops (CPPLL) which show a good

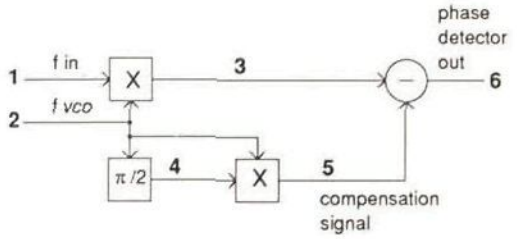


Fig. 1.
Operating principle of the multiplicative phase detector with an inactive state (MPDIS).

noise performance, together with zero phase error, obtained with a passive loop filter.

Operating Principle

The operating principle of the MPDIS is shown in Fig. 1. A compensation signal is subtracted from the output of a common MPD. This signal can be generated by multiplying the VCO output signal by a $\pi/2$ delayed version of itself.

The MPDIS output is inactive when the phase error is zero ($\equiv -\pi/2$ rad VCO phase). The signals for sliding phase errors ($-3\pi/2, +3\pi/2$) are shown in Fig. 2.

Although the phase detector transfer characteristic is not affected by the compensation method, we find that compensation only is effective for phase errors in the range ($-\pi/2, +\pi/2$). This means that ripple compensation is effective for the positive slope. Minimal ripple for the negative slope can be obtained by inverting the $\pi/2$ delayed version of the oscillator signal.

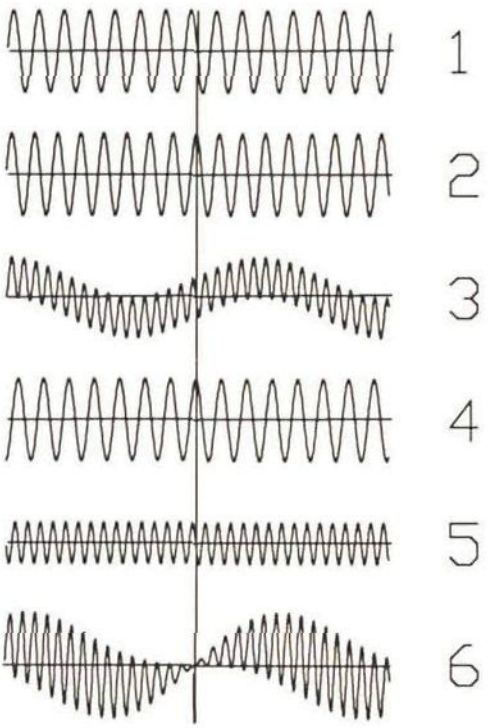


Fig. 2.
Waveforms of the proposed type of phase detectors for sliding phase differences.

Implementation of MPDIS

It is common practice to provide two output terminals which control current sources for Charge-Pump applications. In the inactive state both current sources are switched off. With our compensation method, this circuit can be realized by comparing the compensation signal with the normal MPD output instead of subtracting them. *If the signals are equal, both sources will be switched off.* A possible circuit implementation model is shown in Fig. 3a.

This model may be simplified because the compensation signal is identical to the frequency-doubled VCO signal, which leads us to the circuit of Fig. 3b.

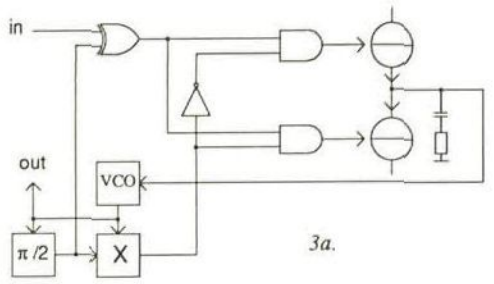
This phase detector circuit has no ripple for a 'VCO phase' of $-\pi/2$. Compensation for the negative slope can be obtained by exchanging the control signals of the current sources.

Using a double-frequency VCO and a toggle flip-flop, the phase detector circuit of Fig. 3b may be further simplified. This leads us to the circuit of Fig. 3c which shows unique features:

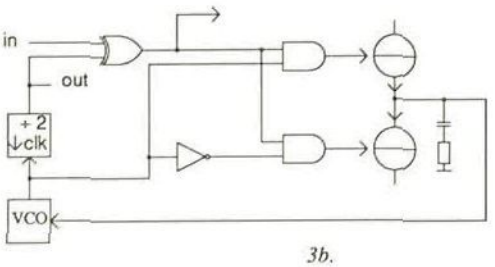
- it has a multiplicative charge pump phase detector
- the zero phase error is identical to zero phase difference (instead of the usual $\pi/2$ rad phase difference).

Experimental results

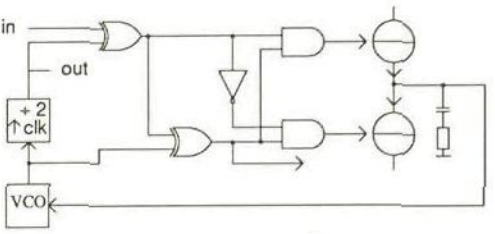
Practical Charge-Pump PLLs with the proposed phase detector circuits and passive filters have been built and are now being investigated to validate loop performance



3a.



3b.



3c.

Fig. 3.

Multiplicative phase detectors with an inactive state for charge-pump phase-lock loops.
a) circuit implementation model
b) simplification by using a double VCO frequency results in a static 'VCO phase' of $-\pi/2$.
c) further simplification results in a 'VCOphase' of zero

in conditions of excessive input noise.
Preliminary results in this respect show that our Charge-Pump PLLs, contrary to the usual PFD CPPLL, are only dependent on the noise within the loop noise bandwidth and stay in lock within the whole input frequency range while maintaining a mean static phase error of zero.

Detailed application results on the overall PLL performance (operating ranges, acquisition, tracking, etc.) will be reported as soon as possible.

Conclusions

It has been shown that with the proposed phase detection method it is possible to realize Multiplicative Phase Detectors circuits which show an inactive state for zero phase error and consequently a low phase detector ripple term.
Based on this principle it is also possible to implement a real charge-pump PLL with a passive filter that shows good noise performance (Multiplicative Phase Detector) and zero static phase error. Practical circuit implementations have been presented: a circuit for the usual static phase difference of $+\pi/2$ or $-\pi/2$ and a multiplicative phase detector circuit that shows the unique feature of choosing either zero or π static phase difference. So far this phase detector property could only be realized with sequential phase detectors.

Acknowledgements

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CHAPTER VII CONCLUSIONS

Design processes in several fields have been examined in brief. A route through the huge amount of material in the field of Phase-Lock Loops has been suggested. This route is based on the assumption, that design processes are composed of two basic steps: the choice of a topology and the calculation of its elements.

Investigation and analysis of the topological choices and basic design questions have led to the generation of an approach to systematic designing, required for automation. This approach has been applied to the field of PLL's, with initial attention being given to treating basic PLL properties.

Linear model equations ⇒ PLL remains in lock

The basic model assumes that the PLL is in lock. The output frequency of the loop is equal to the input frequency and only small variations are taken into consideration. The dynamic properties are determined by the small-signal transfer factors of the loop components: phase detector, loop filter, and oscillator. The dynamic requirements of the application are

specified in terms of response time or bandwidth. The topology and time constants of a loop filter of a PLL are the keys to controlling the dynamic performance. In the loop filter, dynamic parameters can be easily traded off to meet the requirements. The other loop components have values that cannot be changed so easily.

Loop filter topology: If no loop filter is applied the dynamic properties of a PLL are determined by the loop gain $K_o K_d$ that must be expressed as a function of angular frequency ω_L, independent of the units of K_o and K_d. This was established as the upper bound of the dynamic behavior, regardless of the passive loop filter topology.

The choice of a loop filter in order to obtain a specified time or frequency response was described in terms of undamped angular frequency ω_n and damping factor ζ. The requirements for ω_n and ζ are determined by the functional performance of the PLL. The single-input/single-output combinations were established in I/O tables.

Input/output topology: The application of a PLL and requirements on its dynamic properties were summarized for a single loop either with or without a divider.

The PLL-Frequency Model was introduced to examine the dynamic performance in the frequency domain. Examination of the basic function of the phase detector led to the non-linear model of the PLL

Non-linear model equations ⇒ operating ranges of a PLL

Phase detection implies non-linearity resulting in definitions for the operating ranges of a PLL in which the linear properties are valid. The topology of the phase detector implementation is the key to controlling the operating ranges. By choosing a phase detector and either an active or passive loop filter, operational parameters can be traded off to meet the requirements.

Phase detector topology ⇒ Basic design equations: The governing equations of the conditions of operation were given for standard phase detectors implemented in integrated PLL circuits. Unfortunately, the small phase error properties described by the linear model and some of the operating ranges appear to be inversely dependent. Moreover, phase detectors also

generate unwanted signal components: phase detector ripple.

Extended non linear analysis: Governing equations were also presented concerning Carrier-to-Spurious Ratio caused by the phase detector ripple for PLL's with standard phase detectors.

Limits on the operating ranges of a PLL were further restricted under the influence of noise. A quantitative explanation of the question — how a PLL is unlocked by noise — was given.

Design constraints

Usually a designer will first try to improve the chosen topology by considering other loop component implementations, hoping to better meet the conflicting requirements. The design compromises concern in the main acquisition performance and tracking bandwidth or phase detector ripple suppression and switching speed. Ripple suppression may be improved by a sample-and-hold phase detector and by a phase-and-frequency detector. Moreover, the phase-and-frequency detector will improve the acquisition performance. If conflicting requirements still cannot be met, multi-detector loops are indicated.

Multi-detector topology

Although it is possible to meet some requirements when a number of controlled oscillators operating in consort, we have limited the discussion to the use of multiple phase detectors controlling one oscillator. It was shown that multi-detector loops can be based on the quadrature principle. A summary was given of various quadrature configurations. Many quadrature configurations can be transformed into single loops with a special phase detector transfer characteristic.

As have been seen simple models become more and more complex. The more complex topology can be tailored to most applications, thereby illustrating a frequently observed design phenomenon: the higher the performance required, the more complex the circuit will become. Design information was, however, not complete. Another path has thus been followed, searching out suitable methods for simplifying implementation and fulfilling design compromises.

Design aims

Acquisition improvement and lock detection were shown to be realizable with simple implementations based on the detection of cycle slips. The adaptive phase detector was introduced to design the tracking and acquisition behavior independently.

To meet switching speed and spurious suppression the accumulator type rate multiplier was proposed for use with a digital harmonic mixer to control the frequency of a sampled PLL frequency multiplier.

A lower bound for the input signal-to-noise ratio in conditions of excessive input noise was found for cases in which frequency-detector aided PLL's are applicable. A route was given for further investigations to obtain topological design rules for acquisition-aided PLL's. The multiplying charge-pump phase detector was introduced to realize an independent design of the frequency and phase performance of Frequency-and-Phase-Lock Loops, that must operate under the condition of excessive input noise.

All-digital PLL's

All-digital PLL's were analyzed from the point of view that the characterization of the digitally controlled oscillator is the key to determining its applicability.

Configurations for all-digital loops were presented, based on modulated rate multiplication.

A new configuration was proposed for a second-order ADPLL that extended the application possibilities considerably by providing additional degrees of freedom in the design.

A novel all-digital quadrature loop configuration was presented for implementing a Costas loop for BPSK demodulation and carrier recovery. The principle of this configuration may also be used with commercially-available all-digital integrated PLL circuits.

It was shown that the fundamental properties of digital PLL's depend on sampling frequency and phase quantization. It was suggested that design information may be obtained by examining the DPLL as a delta-modulator.

Structured design approach

The given approach to systematic PLL-design resulted in a PLL design strategy, based on a PLL questionnaire about the designers's intentions in a specific application.

It was also established that there are still some 'white spots' left in the available design knowledge. In the future these will have to be investigated in more detail. To complete further research it will be necessary for a designer to determine uncertainty bounds for each topology. In order to choose the simplest implementation, the designer should be aware of the global design constraints governing any topology. Implicit in the process is the proper weighting of design aims.

A conclusion drawn from the generalized design model that was used in this thesis is that *dimensioning* may be performed by means of algorithmic programs, and the *topology* choice may be supported by knowledge-based programs. The requirements of an application category will determine the relevant questions. The answers to these questions should indicate promising configurations and exclude others. The uncertainty bounds must therefore be established in the knowledge base. The explicit weighting of design aims may become possible then.

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SAMENVATTING

Een Phase-Lock Loop (PLL) is een samenstelsel van elektronische circuits die zodanig met elkaar samenwerken dat een *regel*systeem ontstaat, waarin de *fase* informatie van een signaal wordt bewerkt. Omdat de tijdsafgeleide van de fase van een signaal wordt gedefinieerd als de frekwentie van een signaal, wordt ook de *frekwentie* van het signaal bewerkt.

PLL's worden gebruikt op uiteenlopende terreinen van de elektronica, zowel in de consumenten sector (audio, video) als in de professionele sector (telecommunicatie, computers, meetsystemen). De functie van een PLL is altijd die van het synchroniseren van twee grootheden. Dit geschiedt dan ten behoeve van de signaalverwerking, bijvoorbeeld demodulatie van de informatie die gemoduleerd is op een drager die met ruis is belast, of ten behoeve van de signaalopwekking, bijvoorbeeld het genereren van een aantal afstemfrekwenties (kanalen) in een radio- of televisieontvanger. Steeds is er bij *phase-lock systemen* sprake van een relatie tussen de fase van een inkomend signaal en de fase van een lokaal-opgewekt signaal.

De hoeveelheid literatuur op het gebied van PLL's is overweldigend; het gebied is zeer interessant voor mathematische analyses vanuit de regeltheorie, de communicatie-, modulatie-, en informatietheorie. Phase-lock systemen werden altijd gebruikt door deskundigen, totdat echter de IC-techniek zijn intrede deed. Door het beschikbaar komen van geintegreerde PLL circuits (PLL IC's), werden de toepassingen sterk uitgebreid. De ontwerpkennis heeft hiermee echter geen gelijke tred gehouden. Het *ontwerpen* van phase-lock systemen is ook altijd het werk geweest van experts, die vaak op een ogenschijnlijk ongestructureerde manier te werk gingen.

Een gestructureerde aanpak van het ontwerpen is de laatste decennia op een groot aantal terreinen noodzakelijk geworden. Voor elektronische systemen komt dit voort uit de toenemende hoeveelheid componenten (VLSI), de toenemende mate van interactie tussen die onderdelen en de hiermee samenhangende complexiteit. Bovendien worden steeds hogere eisen gesteld aan de kwaliteit van de elektronica.

Phase-lock systemen zijn in het algemeen niet complex in opbouw, maar wel in gedrag. Daarom is ook voor het ontwerpen van PLL's een gestructureerde ontwerpmethode noodzakelijk. Dan is het uiteindelijk mogelijk gedeelten van het ontwerptraject te automatiseren.

Analyse van *het proces bij het ontwerpen* op diverse terreinen heeft geleid tot een aanpak op basis van de topologie. De topologie van een systeem bestaat uit de plaats (topos) en de beredeneerbare (logische) verbindingen van de systeemonderdelen teneinde een specifieke functie te kunnen verrichten. **Iedere ontwerper kiest op basis van zijn ervaring een samenstelling van het systeem, waarvan hij denkt dat het voldoet aan de eisen en gaat vervolgens dimensioneren en vormgeven.** Dan blijkt dat de gekozen topologie voor het systeem al of niet voldoet en moet eventueel een herhaling van de procedure plaats vinden.

In dit proefschrift wordt voor *het ontwerpen van phase-lock systemen* allereerst onderzocht wat de eigenschappen en beperkingen zijn van de bestaande PLL modellen die vrijwel altijd alleen voor *analyse* worden gebruikt. Voor de *synthese-stap* in het hier te behandelen ontwerpproces is het nodig deze kennis op een andere manier te ordenen dan gebruikelijk is. Vastgesteld is dat *ontwerp informatie* op hierarchische wijze kan worden verkregen als vanaf het begin een onderscheid wordt gemaakt tussen de lineaire en niet-lineaire eigenschappen van een PLL. Vanuit ontwerp-standpunt is dit duidelijk: Lineaire eigenschappen worden door de systeem-ontwerper gespecificeerd, terwijl de elektronische implementatie de niet-lineaire eigenschappen (o.a. werkgebieden, ruisgedrag) bepaalt.

Als de lineaire en niet-lineaire eigenschappen van de standaard "single loop PLL" niet tegelijkertijd kunnen worden bereikt, wordt de ontwerper met een probleem geconfronteerd. Dit verschijnsel heeft weliswaar ruime aandacht gekregen in de bestaande literatuur, maar er is vrijwel geen ordening aangebracht voor wat betreft ontwerpdoelen, zoals het kiezen van de eenvoudigste elektronische implementatie die kan voldoen aan de specificaties. Men kan zijn toevlucht nemen tot het modificeren van de lineaire eigenschappen teneinde de niet-lineaire eigenschappen aan te passen, of men kan een andere topologie kiezen door perifere circuits toe te passen, die bijvoorbeeld het in-lock komen van de PLL vergemakkelijken. Voor dit keuzeprobleem van de ontwerper worden oplossingen aangedragen.

Nieuwe keuzemogelijkheden wordt gepresenteerd in de vorm van nieuwe circuits. De ontwerper kan kiezen voor single-loop oplossingen, of voor multiple-detector oplossingen. Ook kan het digitaal implementeren in hard-ware of software een elegante oplossing vormen. Tenslotte wordt dit

ingepast in het uiteindelijk, ogenschijnlijk nog veraf liggende doel in dit proefschrift: een voorstel voor een systematische ontwerpstrategie.

In hoofdstuk II wordt eerst de bestaande praktijk gevolgd die uitgaat van het eenvoudige lineaire model van de PLL. Uit de beschouwingen m.b.t het *lusfilter* volgen bekende, specifieke dynamische eigenschappen van de verhouding: standaard uitgang/ingang. Ontdekt is dat de "high-gain" benadering voor 2^e orde lussen met passief filter onvolledig is gespecificeerd in de literatuur. Tevens worden de grenzen van de dynamische eigenschappen in relatie tot de overdracht van de fasedetector en oscillator expliciet gemaakt en wordt het *PLL-Frekwentie Model* gepresenteerd.

Uit de beschouwingen van de *ingang/uitgangsrelaties* volgen bekende beperkingen voor de dynamische eigenschappen, die nader zijn vastgelegd voor het geval een variabele deler in de lus is opgenomen.

Het tweede gedeelte van hoofdstuk II behandelt de functie van de *fasedetector*. Vastgesteld wordt dat fasedetectie essentieel een niet-lineair proces is en dat dus een niet-lineair model nodig is om de werking van een PLL te beschrijven. Dit houdt in dat voor elke standaardvorm van niet-lineairiteit er grenzen zijn voor de werking. *Ontwerp formules* worden gegeven voor de werkgebieden van PLL's met standaard fasedetectoren die in PLL IC's worden toegepast.

In het derde gedeelte van hoofdstuk II wordt het tot dan toe gehanteerde onderscheid lineair en niet-lineair model uitgebreid. Voor de verschillende input/output relaties werkt de niet-linairiteit op een andere manier. Ook moet de invloed van de ruis voor een niet-lineair model tot uiting komen in een equivalente beperking van het werkgebied. Tevens komt het echte (AC & DC) uitgangssignaal van de fasedetector hier aan de orde.

De vraag: Hoe raakt een PLL uit lock door ruis?, wordt op een nieuwe manier behandeld. Verder wordt een compleet overzicht gepresenteerd voor de Carrier-to-Spurious Ratio (CSR) voor de standaard fasedetectoren uit PLL IC's. Tenslotte volgt een beschouwing over de beperkingen van de tot hier toe gevolgde werkwijze, speciaal m.b.t. het gevolg van het schakelen in sommige fasedetectoren.

In hoofdstuk III worden voorbeelden gegeven van circuits en configuraties die gebruikt kunnen worden om een combinatie van lineaire en niet-lineaire eigenschappen te bereiken, die met een standaard, enkele lus niet

kunnen worden bereikt. De Sample-and-Hold (SH) schakeling en de *Phase-and-Frequency Detector* (PFD) met Charge-Pump (CP) worden beschreven als een verbetering van een standaard fasedetector voor een enkele lus. Gedeeltelijk is de nieuwe beschrijving van de werking van de PFD inmiddels algemeen geaccepteerd; helaas wordt in diverse boeken en "application notes" nog steeds een onjuiste en/of niet totale overdrachtskarakteristiek gegeven. Als een uitbreiding van de PFD wordt een *nieuwe methode voor lockdetectie* in een enkele lus gepresenteerd.

Onderzocht is wat de eigenschappen en beperkingen zijn van de topologie van Quadrature Loops. Gevonden is dat de speciale luseigenschappen kunnen worden gerealiseerd, mits de *juiste signalen* kunnen worden opgewekt. De consequenties van het niet precies in quadratuur zijn van de signalen, zijn buiten beschouwing gelaten.

Uit het eerste gedeelte van dit hoofdstuk kan als voorlopige conclusie worden gesteld dat, zowel bij de verbeteringen van de enkele lus, als bij de introductie van meervoudige detector lussen, de ontwerp compromissen blijven bestaan. Dit wordt veroorzaakt door de tegenstrijdige eisen voor de synchrone werking en bijvoorbeeld de spurious onderdrukking of de eisen voor de acquisitie tijd als ruis aanwezig is op het ingangssignaal.

Daarom worden in het volgende gedeelte van hoofdstuk III nieuwe configuraties gepresenteerd, die de ontwerper meer keuzevrijheid geven bij het dimensioneren. Vooral het onafhankelijk van elkaar kunnen dimensioneren van de lineaire- en de niet-lineaire luseigenschappen met behulp van zo eenvoudig mogelijke circuits staat centraal.

De *Adaptive Phase Detector* wordt gepresenteerd en de luseigenschappen worden onderzocht. Het blijkt dat met deze nieuwe fasedetector de acquisitie-eigenschappen vrijwel onafhankelijk van de tracking-eigenschappen kunnen worden gedimensioneerd. De circuit-implementatie vormt echter nog een probleem. Dit wordt opgelost door een circuitontwerp en realisatie van deze fasedetector in de vorm van *twee onafhankelijke tellers* met een begrenzingsnetwerk. De maximale frekwentie hiervan is echter beperkt. Een verbeterd circuit ontwerp en realisatie wordt gepresenteerd op basis van een *ring structuur*, die een maximale frekwentie toelaat die gelijk is aan de maximale frekwentie van de gebruikte sequentiële elementen. Het is echter gebleken dat het speciale circuitontwerp dat nodig is voor de introductie van deze nieuwe fasedetector een belemmering kan vormen voor

de ontwerper van toepassingen. Daarom wordt een nieuwe methode voor snelle *acquisitie* gepresenteerd op basis van het realiseren van een *pseudo-lineaire fasedetector karakteristiek met "oneindig" fase gebied.* Deze methode kan worden toegepast bij standaard fase detectors.

De *rate multiplier* wordt gepresenteerd als een goede hulp bij het instellen van de frekwentie van een frekwentie-synthesizer. De afhankelijkheid van de spurious onderdrukking en de omschakelsnelheid onderling kan hiermee worden geëlimineerd, zoals wordt aangetoond voor het ontwerp van een "fractional-harmonic frequency synthesizer". Tevens zal later blijken dat de rate multiplier ook met vrucht kan worden toegepast als digital controlled oscillator voor "All-Digital PLL's".

Als *ruis* bij het ingangssignaal aanwezig is, moeten speciale maatregelen worden genomen om het *tracking/acquisition* ontwerp-compromis te benaderen. Als er ruis bij het ingangssignaal aanwezig is kan een PFD niet goed werken. Dit blijkt een eigenschap te zijn van de PFD en niet van de Charge-Pump. Bij het niet-lineaire model kwam het uit lock gaan door ruis aan de orde, nu wordt dit verder geanalyseerd met betrekking tot de detectie van een frekwentieverschil. Een ondergrens is gevonden voor de toepassing van frekwentie detectie in *gecombineerde Frequency-and-Phase-Lock Loops (FPLL's)* met optimale tracking en acquisitie eigenschappen. Een nieuwe *vermenigvuldigende fasedetectie methode voor Charge-Pump PLL's* wordt gepresenteerd, die gebruikt kan worden als er ruis aanwezig is. Tenslotte wordt verwezen naar artikelen die voorwaarden geven waaraan het *digital design* van phase-lock systemen moet voldoen.

In hoofdstuk IV wordt een aanzet gegeven voor het ontwerp van PLL's die volledig kunnen worden opgebouwd uit digitale circuits en/of volledig geïmplementeerd kunnen worden in software. In plaats van een karakterisering op basis van fase detectoren, is een onderscheid gemaakt naar het principe van digitaal stuurbare oscillatoren. Vastgesteld is dat een rate multiplier goede diensten kan bewijzen voor een *nieuwe*, volledig digitale implementatie van een PLL.

De implementatie van een geheel digitale *nieuwe COSTAS PLL* voor carrier-tracking en data-demodulatie wordt gepresenteerd. Tevens wordt een nieuwe implementatie van een *digitale* 2^e *orde PLL* gegeven, die het mogelijk maakt, in tegenstelling tot de gebruikelijke hogere-orde lus

configuraties, om het vanggebied onafhankelijk van de dynamische eigenschappen te dimensioneren.

Tenslotte wordt een aanzet gegeven voor een *implementatie-onafhankelijk model voor digitale PLL's*, dat de ontwerper in staat moet stellen te beslissen of een geheel digitale topologie tot zijn keuze mogelijkheden behoort.

In hoofdstuk V wordt een overzicht gegeven van de stand van zaken met betrekking tot het ontwerpen van PLL's. Aanvullende *ontwerp informatie* wordt afgeleid uit vragen en specificaties o.m. afkomstig uit een recent verschenen ontwerp-programma. De gebruikte benadering van de *ontwerp procedures* uit dit proefschrift wordt samengevat. Dit leidt tot de systematische en hierarchische *ontwerp strategie* voor de implementatie van systemen, waarin het phase-lock principe wordt gebruikt. Voorbeelden worden gegeven van gedeelten uit het ontwerp traject die door anderen in het verleden zijn gepresenteerd.

In hoofdstuk VI worden case studies gegeven over werk-gebieden van PLL's, verbeteringen op basis van cycle-slip detectie en op basis van rate multipliers. Voorts worden benaderingen gegeven voor het digitale ontwerp. Tot slot wordt een nieuwe phase detector gepresenteerd, die gebruikt kan worden voor een Charge-Pump PLL, die moet werken onder omstandigheden met ruis.

In hoofdstuk VII worden conclusies gegeven. De gevolgde benadering van het ontwerp probleem van PLL's, samen met de gepresenteerde nieuwe circuits, geeft een goed inzicht in de keuze problemen van de ontwerper en leidt naar een gestructureerde ontwerpmethode. De vragen die hierin gesteld moeten worden, zouden in een vervolg onderzoek kunnen leiden naar kennis-gestuurde programma's (expert-systems) voor de topologie keuze en naar reken programma's (spread-sheets) voor het dimensioneren van de gekozen topologie.

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ABOUT THE AUTHOR

Richard C. den Dulk was born in Leidschendam, in 1945. He received his technician's certificate at the former UTS (now MTS), the Hague, an engineering degree in electrical engineering from the 'Haags Polytechnisch Instituut,' the Hague, and the ing. degree from the 'Hogere Technische Avond School,' Rotterdam, in 1964, 1969 and 1971, respectively. In 1978 he received the ir. degree in electrical engineering from the Delft University of Technology, Delft.

In 1964 he joined the Department of Electrical Engineering at Delft, where he worked on HF and VHF receivers, automatic tracking systems for meteorological satellites, and the implementation of frequency synthesizers. Since 1974 he has been a mentor for students who are working on the application of digital circuits in frequency synthesizers. Since 1980 he has been a member of the scientific staff at Delft, where he lectures and supervises student's work on electronic design of integrated PLL system components. His present research interest is in the design, implementation, and testing of electronics for communications application such as phase-lock loops and spread-spectrum system-components. As a matter of course his activities have grown to include education and courseware for effective study management.

He was a member of the Faculty Council of the Faculty of Electrical Engineering at Delft from 1983 till 1987. Since 1985 he has been a member of the board of State External Examiners for the department of electrical engineering of the 'Dag-HTS, Haagse Hogeschool,' the Hague. From 1986 he has been a lecturer and a supervising tutor part-time at the 'Avond-HTS, Haagse Hogeschool,' the Hague. He is a member of the 'Nederlands Elektronica- en Radio Genootschap' (NERG). In April 1989 he was appointed a member of the governing board of the NERG.

His extra-professional interests include sailing, surfing and league volleyball. Following up several private, non-profit and industrial activities on strategic planning he founded INNOMEC CONSULTANTS in 1986. INNOMEC® coordinates research in areas such as business planning in education.

14. Bij het lezen van artikelen in kranten en tijdschriften constateren deskundigen dikwijls onjuistheden over het eigen vakgebied. Hieruit moeten zij de conclusie trekken dat dit ook geldt voor artikelen op het vakgebied van anderen.

15. Een promovendus is een "kleine zelfstandige in wetenschap" en dient dus ook in aanmerking te komen voor overheids-stimulering ter bevordering van de "kleinschaligheid."

16. De ene ingenieur (ir.) is de andere niet (ing.).

17. Wie alles ernstig neemt, moet niet serieus genomen worden.

STELLINGEN

behorende bij het proefschrift
van
Richard C. den Dulk

Delft, 16 november 1989

1. Ontwerpen kan beschouwd worden als het kiezen van een configuratie en het vervolgens dimensioneren van de onderdelen.

Dit proefschrift: hoofdstuk I

2. De overdrachtskarakteristiek van de fase-en-frekwentie detector is door Gardner onvolledig en door Best onjuist weergegeven.

F.M. Gardner, *Phaselock techniques 2nd ed., Wiley, New York, 1979, p.124*
R.E. Best, *Phase-Locked Loops, McGraw-Hill, New York, 1984, p.8*

3. Hardy stelt een PLL-implementatie voor, die een oscillerende regeling tot gevolg heeft.

J. Hardy, *Electronic Communications Technology Prentice-Hall, Englewood Cliffs, 1986, p.301*

4. Maatschappelijke processen zijn te onderscheiden naar constructie- en groeiprocessen. Constructie-processen betreffen het samenvoegen van externe onderdelen; bij groeiprocessen is er sprake van interne, zelfregulerende delingsmechanismen. Op de fundamentele verschillen in externe beïnvloedbaarheid van deze processen wordt door de overheid geen acht geslagen.
Constructieve maatregelen, die het werkklimaat niet verbeteren, zijn contra-produktief als het gaat om de beïnvloeding van groeiprocessen, zoals het onderwijs.

5. Medische ontwikkelings-samenwerking dient uitsluitend door non-profit organisaties te worden uitgevoerd.

6. Privatisering sluipt het (technisch en wetenschappelijk) onderwijs in door de toenemende afhankelijkheid van de tweede en derde geldstroom. Het is wenselijk dat de overheid dit expliciet vermeldt en dat nagegaan en aangegeven wordt, welke onderwijskundige resultaten hiermee beoogd worden.

7. Bij het (leren) oplossen van problemen verschaft "een open deur intrappen" het besef, dat er minstens één deur is.

8. Er kan ernst worden gemaakt met de verhoging van het studierendement in de elektrotechniek door de invoering van colleges over de methodologie van studie en onderzoek in het algemeen, en over systematische benaderingen in de elektrotechniek in het bijzonder.

9. Computerprogramma's voor controle van de spelling dienen zodanig te worden uitgebreid, dat zij alle fouten ontdekken in zinnen zoals:
De zin: "Dit antwoordt betekend, dat we nu noch verder zijn verwijdert van het pijl dat in de simulatie wel goed berekent word," vertoond negen fouten.

10. De woorden "simuleren", "simulatie", "simulator" en "simulant", dienen in de volgende context te worden gebruikt:

- Een toestel (programma) dat iets kan *simuleren* (nabootsen) dient *simulator* te worden genoemd. Met deze inrichting kan men een *simulatie* uitvoeren.
- Degene die simuleert, dient in de techniek geen *simulator* of *simulant* te worden genoemd, maar simuleerder: Door simulatie kan de simuleerder veel leren.

11. Simuleren zonder experimenteren en verifiëren is verleren.

12. "Glasnost" en "perestrojka" stimuleren in de Sovjet-Unie ook de micro-elektronica, aangezien men daardoor het begrip "vrije lading" beter kan toepassen.

Vrij naar Cor Ridders (≈ 1980)

13. Toelichting door "deskundigen" in NOS-journaals draagt nauwelijks bij tot de informatie.