A Fully-Passive Noise-Shaping SAR for use in a Zoom ADC

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By

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Abstract

The ΔΣ analog-to-digital converter (ADC) is widely used in audio applications for its high resolution. However, it is less energy efficient compared to Nyquist Rate ADCs. The growing demand for portable and wearable devices poses a more stringent power-efficient requirement on the audio system, and the traditional ADCs architecture is hard to achieve both high linearity and high energy efficiency. Zoom ADC is a proven energy-efficient hybrid structure for high-resolution and high-linearity applications. It consists of a front-end successive approximation register (SAR) ADC as a coarse stage and ΔΣ modulator backend to take advantage of the energy efficiency of a SAR ADC and the high resolution of a ΔΣ.

However, the conventional zoom ADC suffers from distortion due to the input-correlated quantization error from the coarse stage. The tonal behavior (also known as “fuzz”) degrades overall linearity.

This thesis describes a low cost, calibration-free method to suppress the fuzz in the zoom ADC. It improves the SNDR by introducing a 1st order fully passive noise shaper with a dithering to the coarse SAR ADC, which reduces the correlation of its quantization error with the input.

A prototype ADC has been implemented in standard 160 nm CMOS process. It achieves 104.4dB peak SNR, 103.8 dB SNDR and 106.5 dB dynamic range (DR) in the audio band (20Hz~20kHz) at an oversampling ratio (OSR) of 62.5. The ADC consumes 317 μW from a 1.8V supply, thus resulting in a Schreier FoM of 185 dB.

Acknowledgements

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1 Introduction

Thanks to Moore's Law, the world has become increasingly digital. Analog-to-digital converters (ADCs) have thus become essential in an increasing number of applications to build bridges between the physical and digital worlds. The purpose of this work is to develop an ADC for audio applications that offers high resolution, linearity, and power efficiency.

1.1 Motivation

Audio applications require high SNR (>100 dB) and linearity (THD < -110dB). Traditionally, ΔΣ ADCs have been the workhorse in this application due to their high resolution and linearity. However, they require power-hungry amplifiers. On the other hand, SAR ADCs are very low power thanks to their mostly digital nature. However, their power efficiency degrades when targeting high resolutions.

The zoom ADC combines a low-resolution SAR and a ΔΣ, has emerged as a promising architecture[1, 2], where a SAR is used to significantly reduce the signal swing in the ΔΣ with negligible power overhead, thereby allowing substantial power savings. As shown in Fig. 1, the ADC survey suggests that zoom ADCs achieve state-of-the-art energy efficiency in high-resolution applications.

When a low-resolution SAR is used in a zoom ADC, its quantization error, which is highly correlated with the input, appears in the overall output and significantly degrades system linearity. Increasing the SAR resolution would significantly increase complexity and power [3]. This thesis proposed an architecture that employs a fully passive noise-shaping SAR[4] to boost the front-end's in-band performance without increasing its resolution. This thesis thus aims to improve the overall linearity of the zoom ADC by enhancing the performance of the conventional zoom ADC by applying a noise-shaping SAR front-end.

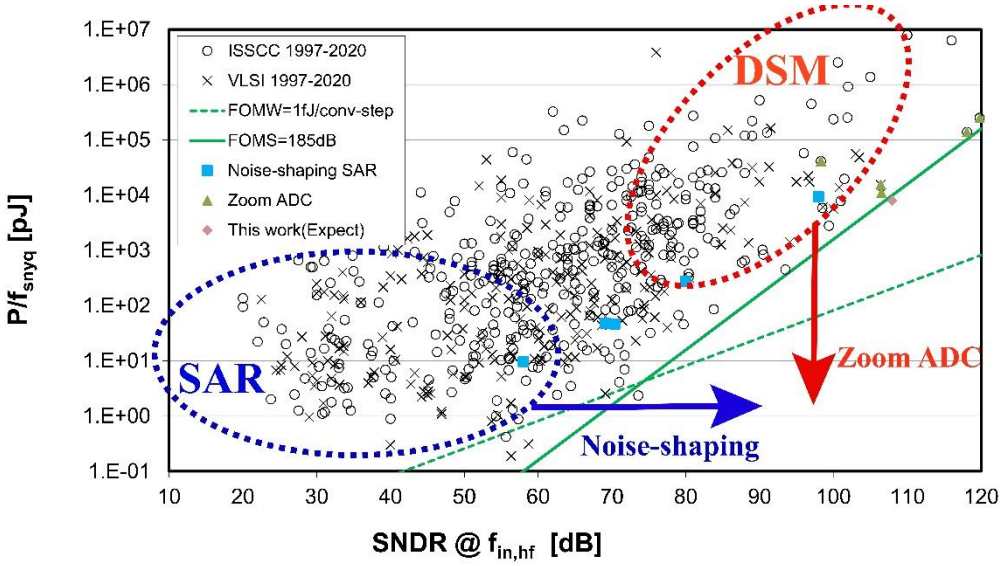


Figure 1.1: Survey on ADC performance in terms of energy efficiency and peak SNDR[5] .

1.2 Thesis organization

This thesis describes the architecture, circuit implementation, layout, and measurement results of the prototype ADC.

The thesis is organized as follows:

- **Chapter 2** gives an overview of conventional ADC structures including SAR and Delta-sigma ADCs. Furthermore, it introduces emerging hybrid ADC structures (e.g., noise-shaping SAR and zoom ADC). Finally, the limitation of the SNDR of the zoom ADC is analyzed and a new zoom ADC architecture is proposed to improve the linearity performance.

- **Chapter 3** describes a system-level design. The requirements and the feasibility of the NSSAR are justified for the use of a zoom ADC, and the proposed architecture is verified by MATLAB simulation.

- **Chapter 4** presents the details of the circuit design as well as the layout implementation. The performance of this design is supported by the circuit-level simulation results in CADENCE.

- **Chapter 5** shows the measurement results of the fabricated ADC prototype.

- **Chapter 6** concludes the thesis and suggests future works.

2 System-level overview

This chapter briefly introduces the theory of Nyquist and Over-sampled ADCs. The design trade-offs of SAR and Delta-Sigma ADCs are described. Furthermore, an overview of noise-shaping SAR and zoom ADC are introduced. Finally, the linearity of the zoom ADC is analyzed and a new zoom ADC architecture based on noise-shaping coarse SAR ADC is proposed and possible improvement to the linearity and SFDR are discussed.

2.1 Nyquist rate ADC and Oversampled ADC

The Nyquist theorem indicates that the sampling rate of an ADC should be higher than twice the input bandwidth to reconstruct a signal without aliasing [6], which is expressed as:

$$F_s \geq 2 \cdot F_{BW} \tag{2.1}$$

where Fs is the sampling rate of the ADC, and F_{BW} is the bandwidth of the input signal. The lowest sampling rate is recognized as Nyquist-rate ($F_{s,Nyquist} = 2 \cdot F_{BW}$).

Quantization is a critical step for an ADC to digitize the sampled signal. However, the quantization error is introduced after the digital code of the signal is generated. Assuming that the quantization error is uncorrelated to the input signal, the quantization error is uniformly distributed over the Nyquist bandwidth (DC to $\frac{Fs}{2}\ Hz$) [7]. The rms value of the full range input signal and the quantization error are shown in Equation 2.2 and Equation 2.3 respectively. Therefore, signal-to-quantization noise ratio (SQNR) can be expressed as Equation 2.4

$$V_{Fs,rms}^2 = \left(\frac{2^N \cdot V_{LSB}}{2\sqrt{2}}\right)^2 \tag{2.2}$$

$$V_{q,rms}^2 = \left(\frac{V_{LSB}}{\sqrt{12}}\right)^2 \tag{2.3}$$

$$SQNR_{Nyquist} = \frac{V_{Fs,rms}^2}{V_{q,rms}^2} = 10\log_{10}(2^{2N}) + 10\log_{10}(\frac{3}{2}) = 6.02 \cdot \mathrm{N} + 1.76\ \mathrm{dB} \tag{2.4}$$

For a sampling rate (F_s) higher than Nyquist rate ($F_{s,Nyquist}$), the ADC is operating in an oversampled mode, a factor of oversampling ratio (*OSR*) can be expressed as:

$$OSR = \frac{F_s}{2 \cdot F_{BW}} \quad 2.5$$

The total quantization noise power is only related to the resolution of the ADC (*N*), and the quantization error is spread from DC to $\frac{Fs}{2}\ Hz$. Therefore, a higher sampling rate results in lower in-band integrated quantization noise as shown in Equation 2.6.

$$V_{qos,rms}^2 = \left(\frac{V_{LSB}}{\sqrt{12}}\right)^2 \cdot \frac{1}{OSR} \quad 2.6$$

Equation 2.4 can be rewritten as equation 2.7, the SQNR of the ADC increases by 6dB (or 1 bit) by quadrupling the OSR.

$$SQNR_{Oversampled} = 6.02 \cdot N + 1.76dB + 10 \cdot log_{10}(OSR) \quad 2.7$$

2.2 Successive-Approximation Register (SAR)

In recent years, Successive-Approximation Register (SAR) ADCs demonstrated an excellent energy efficiency for moderate resolution of 9-10 bits [8, 9]. Figure 2.1 shows the block diagram of a SAR ADC. The input signal is first sampled by a sample-and-hold (S/H) circuitry. During the conversion phase, the SAR logic drives the DAC to null the comparator input, based on the comparator decisions after each DAC update. At the end of each conversion, an *N*-bit digital code is generated by the SAR logic. This structure is highly digital and does not require a power-hungry OTA, and has become very energy-efficient in modern CMOS processes.

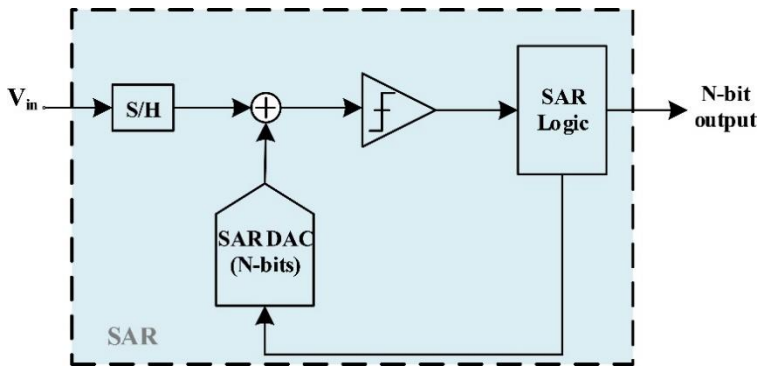


Figure 2.1: Block level diagram of SAR ADC.

However, for target resolutions beyond 12bits, the energy efficiency of the SAR ADC in Figure 2.1 is limited by its stringent requirement on comparator noise and DAC linearity [10]. As a result, SAR ADCs targeting resolution beyond 11-12 bits are less efficient.

2.3 Delta-Sigma Modulator (DSM)

The delta-sigma modulator (DSM) is widely used in high-resolution applications by combining oversampling and noise shaping. Figure 2.2 shows a simplified block diagram of a DSM. It includes an L^{th} order loop filter, an M-bit quantizer and an M-bit DAC. In this feedback loop configuration (Figure 2.2), the quantization error q(z) can be shaped out of the signal band. The out-of-band quantization error can then be easily filtered by a digital low pass filter afterwards [11]. The quantizer and DAC can also have a 1-bit resolution, which results in simple circuit implementations.

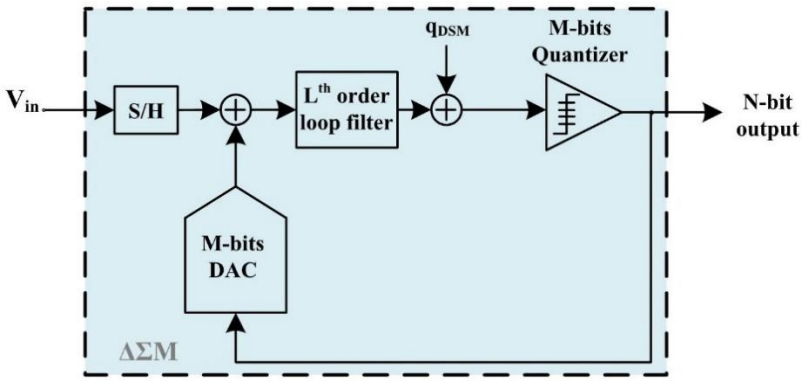


Figure 2.2: Block level diagram of DSM.

The signal-transfer function $STF(z)$ and the noise transfer function $NTF(z)$ can be described as:

$$STF(z)=\frac{Y(z)}{X(z)}=\frac{H(z)}{1+H(z)} \qquad 2.8$$

$$NTF(z)=\frac{Y(z)}{q(z)}=\frac{1}{1+H(z)} \qquad 2.9$$

where $X(z)$ is the sampled input, $Y(z)$ is the output, and $H(z)$ represents the transfer function of the loop filter. In the signal band, $H(z) \gg 1$. Therefore, the STF becomes close to 1, and the NTF can be approximated as $1/H(z)$.

In the case of a first-order DSM, for each doubling of the OSR, the SQNR improves by 9dB, which is more efficient than oversampling alone (3dB improvement) [11]. More aggressive noise shaping can be achieved by increasing the loop filter order. Signal to quantization noise ratio of an L^{th} order DSM can be expressed as:

$$SQNR_{DSM}(dB)=6.02dB\cdot N+1.76dB+10\log_{10}\frac{2L+1}{\pi^{2L}}+(2L+1)\cdot 10\log_{10}(OSR) \qquad 2.10$$

where L is the order of the loop filter, N is the resolution of the quantizer, and OSR is the oversampling ratio. As shown in Equation 2.10, the SQNR improves (2L+1)dB for each doubling of the OSR [11].

Through effective noise shaping, DSM can achieve resolution higher than 20-bits. However, high-order single-bit DSMs have a few drawbacks. First of all, high-order DSMs tend to be less stable than low-order DSMs due to quantizer saturation. As a result, the maximum stable input amplitude (MSA) of higher-order DSMs are limited. Designing a stable high-order DSM modulator requires extensive analysis on its stability which is often carried out by simulation aids.

Employing a multi-bit quantizer is another way to improve the SQNR, which is typically implemented with a flash architecture. By introducing 2^M comparators and feedback DAC elements, the quantization noise can be reduced by the same factor as 2^M, and the MSA is extended since the amplitude of shaped quantization noise at the quantizer input is reduced [11]. On the other hand, the flash quantizer results in significantly increased power and area. Moreover, mismatch in the multi-bit DAC introduces distortion. Therefore, techniques like dynamic element matching (DEM) are required to improve the linearity at the cost of circuit complexity and power [12].

2.4 NS-SAR ADC

The noise-shaping SAR ADC (NS-SAR) is an emerging hybrid data converter architecture. The motivation of the NS-SAR is to improve the SQNR of the SAR ADC. As addressed in Section 2.2, the kT/C and the comparator noise limit the SQNR performance of high-resolution SAR ADCs. Oversampling and noise shaping techniques are often employed to boost the SQNR without increasing the SAR ADC bits as described in [13].

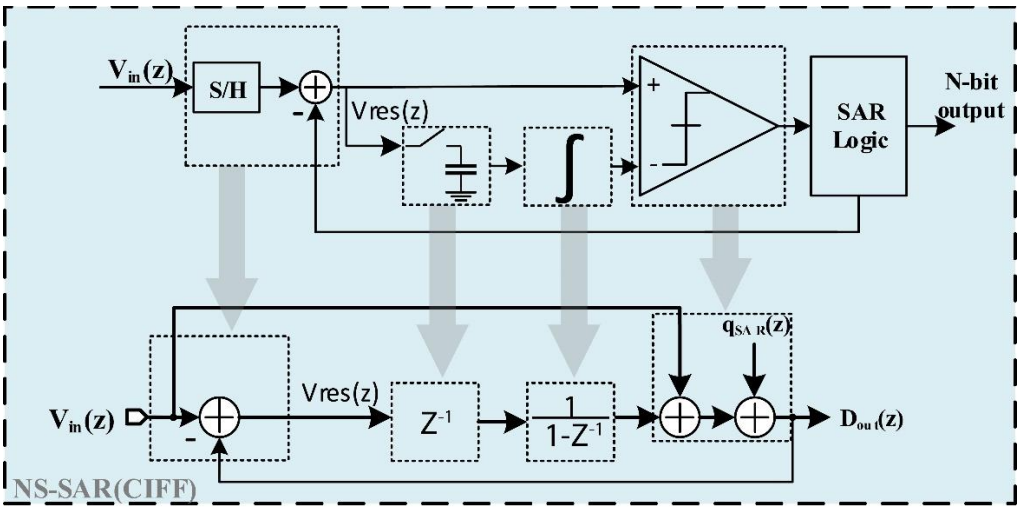


Figure 2.3: Block-level diagram of noise shaping SAR ADC (CIFF structure).

Figure 2.3 illustrates a block diagram and equivalent signal diagram of a cascaded-integrator-feedforward (CIFF) topology of an NS-SAR. Compared to a conventional SAR ADC as shown

in Figure 2.1, an NS-SAR simply adds a noise shaper to process the residue signal V_{res}, which is generated at the end of the SAR conversion. The residue signal can be expressed as:

$$V_{res}(\mathrm{z}) = V_{in}(z) - D_{out}(z) \tag{2.11}$$

The noise shaper in the example of Figure 2.3 integrates previous residue voltage. The processed residue signal and the input signal is being fed-forward and summed in a multi-path comparator [13]. The transfer function is therefore expressed as Equation 2.12.

$$D_{out}(\mathrm{z}) = V_{in}(z) + \frac{z^{-1}}{(1 - z^{-1})} \cdot V_{res}(z) + q_{SAR}(z) \tag{2.12}$$

$$D_{out}(\mathrm{z}) = V_{in}(z) + (1 - z^{-1}) \cdot q_{SAR}(z) \tag{2.13}$$

Equation 2.13 can be re-written as Equation 2.13, where the quantization error can be 1st order noise shaped. Note that, similar to 1st order DSM, this noise-shaping effectiveness is highly related to DC gain of the OTA based integrator, which might degrade energy efficient merit of SAR ADC.

2.5 Zoom ADC

Figure 2.4 shows a simplified block diagram of a zoom ADC [14]. It consists of an N-bit SAR ADC, an N-bit DAC, an L[th] order loop filter, and an M-bit quantizer. The output of the Zoom ADC $Y_{zoom}(z)$ is the sum of the digital output of SAR ADC (K) and the bitstream of the DSM (bs).

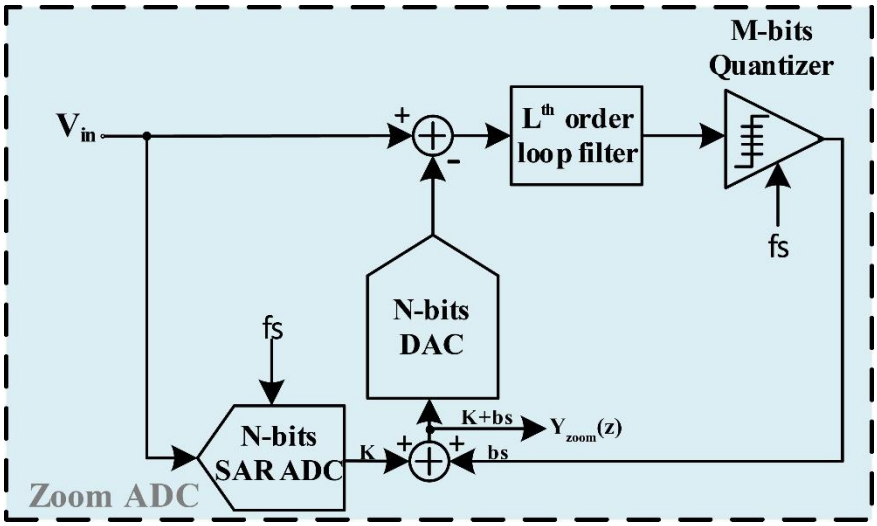


Figure 2.4: A simplified block level diagram of a Zoom ADC.

The operation principle of the Zoom ADC is as follows: First, the SAR ADC performs a coarse conversion, which determines the reference levels for the DSM. This coarse-fine operation

reduces the signal swings inside the DSM. Moreover, the Zoom ADC architecture avoids the need for multi-bit quantizers and achieves a similar resolution when compared to that of a multi-bit DSM. These architectural improvements enabled the zoom ADCs to achieve state-of-the-art energy efficiency [1, 2, 14, 15].

2.5.1 Incremental & Dynamic Zoom ADCs

For applications such as sensors targeting narrow bandwidths, an incremental Zoom ADC has been published in [14]. This ADC employs a 6-bit SAR ADC as a coarse converter and a 1-bit DSM operating sequentially. As a result, the ADC can only handle signal bandwidths up to 5 Hz which is considered as near DC.

For applications requiring more bandwidth (e.g, audio systems), the dynamic Zoom ADC [15] is proposed where the DSM and SAR operate in parallel. The SAR ADC updates the references of the DSM on-the-fly and the dynamic zoom ADC can track higher frequency input signals when compared to the incremental zoom ADCs.

However, the maximum input signal frequency reported in designs of [14, 16] is limited by the SAR ADC speed. For high-frequency input signals, the SNDR of the zoom ADC decreases since SAR ADC cannot track fast-changing input signals [2]. The dynamic zoom ADC with asynchronous SAR ADC improves its signal tracking ability and robustness to out-of-band interferers, which improves the maximum input signal frequency[2].

2.6 Error sources of the zoom ADC

2.6.1 Non-Idealities of SAR ADC

In a zoom ADC, since the SAR ADC's output defines the reference levels for the DSM, the SAR quantization levels should match the DSM DAC output levels for correct operation. A mismatch between the SAR ADC's DAC and the DSM DAC causes the input signal received by the DSM to fall in the wrong range and overload the DSM as shown in Figure 2.5a.

To overcome the overloading of the DSM due to SAR ADC's non-idealities, over-ranging can be used to relax the matching requirement between the SAR DAC and the DSM DAC. Figure 2.5b shows that with an over-ranging factor (OR), DSM no longer suffers from the overloading. Apart from the relaxed matching requirement, the over-ranging factor also relaxes the requirements of the SAR ADC, such as offset and noise. Therefore, the power and area of the SAR ADC can be reduced significantly. The reference level of the DSM can be expressed:

$$V_{ref-} = (K\text{-}OR)\cdot V_{LSB} < V_{in} < V_{ref+} = (K+1+OR)\cdot V_{LSB}, \quad K=0 \sim (2^N - 1). \qquad 2.14$$

where K is digital output code, N is the bit number of the SAR ADC and V_{LSB} is the step size of the least significant bit.

Increasing over-ranging factor to prevent overloading of the DSM increases its quantization error. For example, for an over-range factor of 1, the DSM DAC range increases from 1LSB to 3LSB. As a result, the quantization error power increases by 3 times, or 9 dB [1].

A multi-bit flash quantizer can be used to mitigate the SQNR loss due to the increased DSM DAC swing [1]. As shown in Figure 2.5c, the DSM can take advantage of the full DAC range by using a 2-bit quantizer and the DAC of the DSM only toggles ±1LSB. This effectively reduces quantization error from 3LSB to 1LSB. Therefore, the SQNR of the DSM can be improved by about 9dB [1].

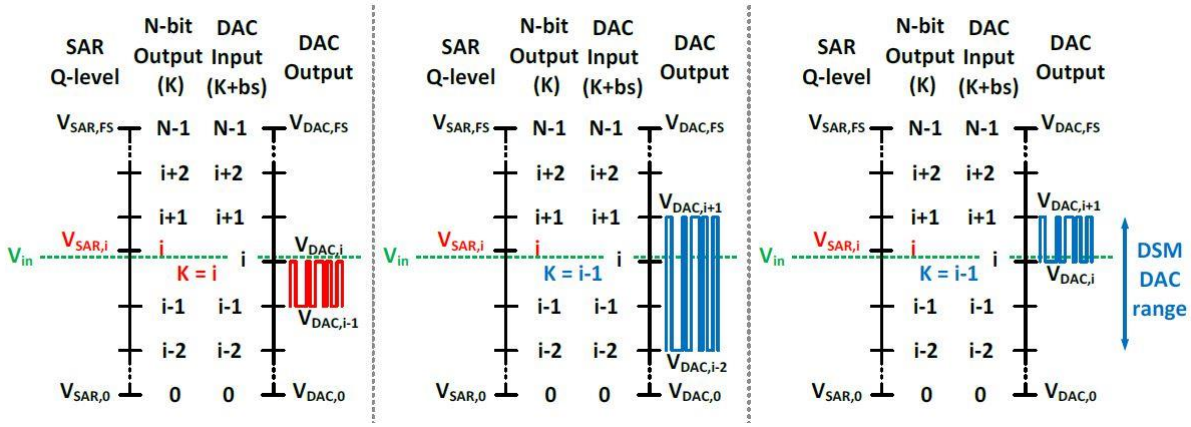


Figure 2.5: Fine reference set by DAC (a) without over-ranging, (b) single bit quantizer with over-ranging, (c) Multi-bit quantizer with over-ranging.

2.6.2 Non-Idealities of DSM

Mismatch of the DAC unit elements introduces nonlinearity in the DSM and the zoom ADC output. Therefore, dynamic element matching (DEM) is needed to ensure that the linearity of the DSM DAC will not limit the SNDR of the zoom ADC [1, 2, 14, 16]. However, DEM implementation increases digital power. DAC resolution or DEM should be carefully chosen to achieve a balance between energy efficiency and linearity.

The finite DC gain of the OTA of the DSM reduces the loop gain and results in a higher quantization noise level thus reducing the SQNR. Furthermore, due to the finite DC gain, the settling time of the OTA is degraded, which causes settling error and further degrades noise-shaping quality.

2.7 Tone leakage in the zoom ADC

2.7.1 Problem definition

Figure 2.6 depicts a simplified block diagram of a conventional zoom ADC. The transfer functions of the SAR, the DSM, and the Zoom ADC can be expressed as:

$$Y_{SAR}(z) = V_{in}(z) + Q_{SAR}(z) \tag{2.15}$$

$$Y_{DSM}(z) = -Q_{SAR}(z) \cdot STF + Q_{DSM}(z) \cdot NTF \tag{2.16}$$

$$Y_{zoom}(z) = V_{in}(z) + Q_{SAR}(z) \cdot (1 - STF) + Q_{DSM}(z) \cdot NTF \tag{2.17}$$

where Q_{SAR} and Q_{DSM} are the quantization error of the SAR ADC and the DSM, respectively. NTF is the noise transfer function of the DSM and STF is the signal transfer function of the DSM.

For a DSM with unity STF, the Q_{SAR} is completely cancelled from the output of the Zoom ADC as indicated in [1, 2, 16] to Equation 2.17. However, for implementation where the STF of the DSM deviates from unity at high frequencies, the Q_{SAR} is only shaped by the NTF where $NTF = (1 - STF)$. As a result, Q_{SAR} appears the output of the Zoom ADC and it limits the maximum achievable SQNR of the zoom ADC. Furthermore, Q_{SAR} is highly correlated with the input signal for quantizers with 1-5bits of resolutions.

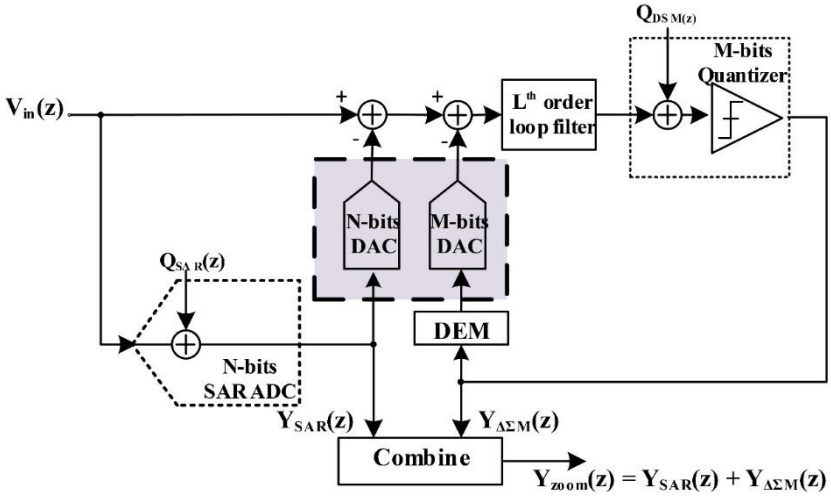


Figure 2.6: Simplified Conventional zoom ADC block diagram.

Figure 2.7 shows the output spectrum for different resolutions of the SAR ADC. The Q_{SAR} of a low-resolution SAR is highly correlated to the input signal and exhibits harmonically related tones at its output [17]. A low-resolution SAR ADC is often employed as a trade-off between power efficiency and implementation complexity of the DEM algorithm [1, 2, 16]. However, due to the limited suppression provided by the NTF, harmonic tones generated by the SAR ADC can be observed at the output of the zoom ADC. In the next section, we will give an overview of the techniques published in the literature to solve the quantization noise leakage of the SAR ADC.

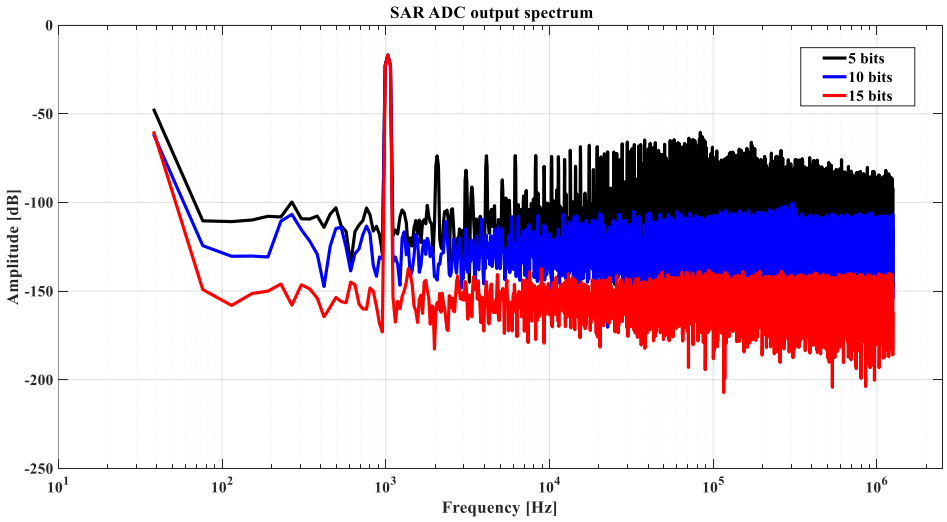


Figure 2.7: Output spectrum of SAR ADCs with different resolutions. The DAC of the SAR ADC is ideal without any mismatch and noise.

2.7.2 Overview of the prior art

Two solutions have been proposed to tackle the Q_{SAR} leakage of the zoom ADC [1, 2].

Ref. [2] suggests filtering the coarse ADC output before combining it with the DSM output. The SAR quantization error can be completely removed if the digital filter's transfer function matches the DSM's STF. In practice, circuit nonidealities (e.g., mismatch and finite DC gain) cause the actual STF to vary, thus limiting the efficiency of this technique.

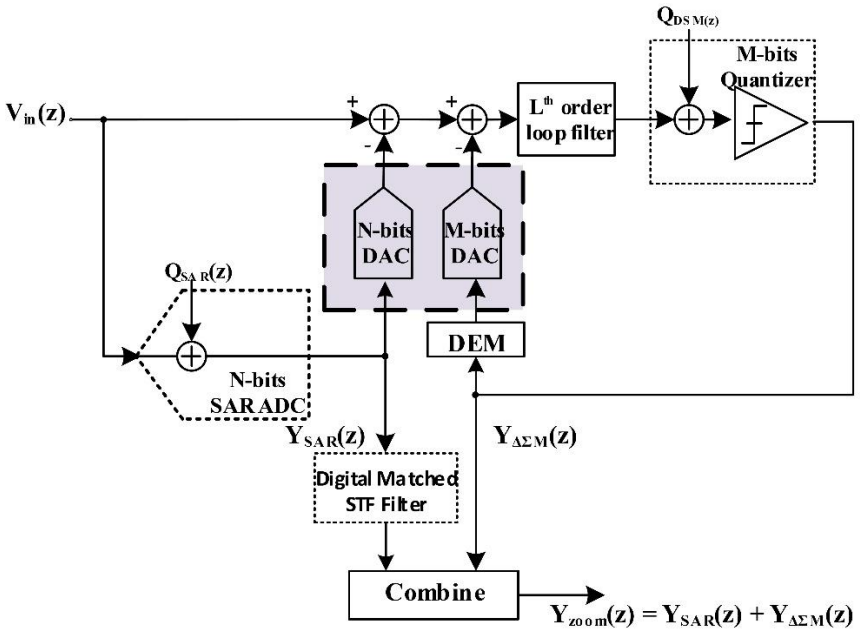


Figure 2.8: Digital filter method.

Ref. [1] proposes an on-chip, analog method to cancel the tone leakage of the zoom ADC. A replica DAC is used for obtaining a copy of the Q_{SAR}, which is directly fed to the DSM's quantizer input, making its STF equal to 1 across all frequencies. However, due to the mismatch between the replica DAC and the SAR DAC, the Q_{SAR} still leaks to the output, and limits the SNDR.

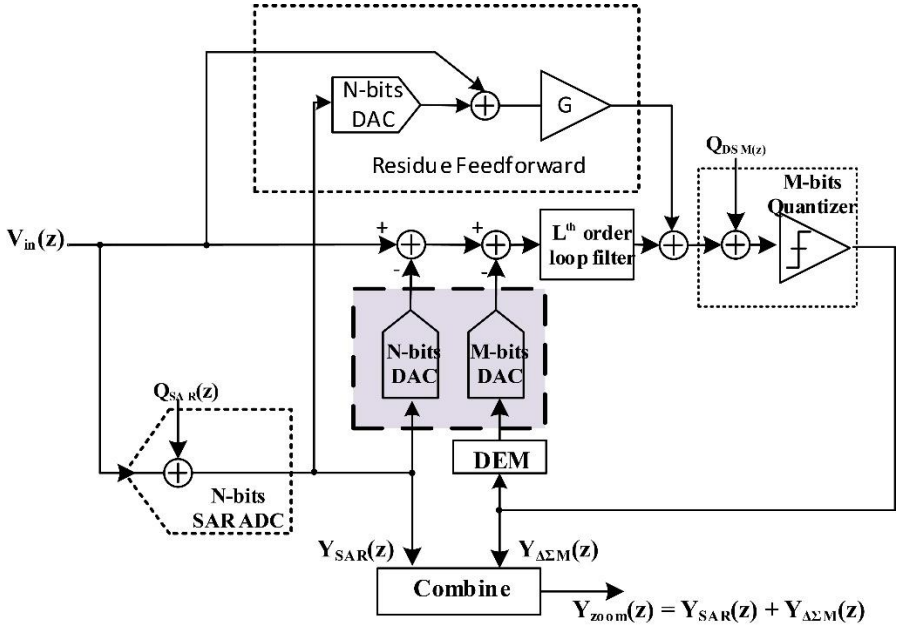


Figure 2.9: Residue feedforward method.

2.7.3 Proposed solution

Figure 2.10 illustrates a simplified diagram of the Zoom ADC. The coarse ADC is implemented as a noise shaping SAR ADC whose quantization noise (Q_{SAR}) is shaped to out of band interest. The transfer function of the proposed Zoom ADC can be expressed as:

$$Y_{zoom}(z) = V_{in}(z) + NTF \cdot NTF_{SAR} \cdot Q_{SAR}(z) + NTF \cdot Q_{DSM}(z) \qquad 2.18$$

where NTF_{SAR} is the noise transfer function of the NS-SAR ADC, Q_{SAR} and Q_{DSM} are the quantization error of the SAR ADC and the DSM, respectively. The Q_{SAR} at the output of the Zoom ADC is shaped both by the noise transfer functions of the SAR ADC and DSM.

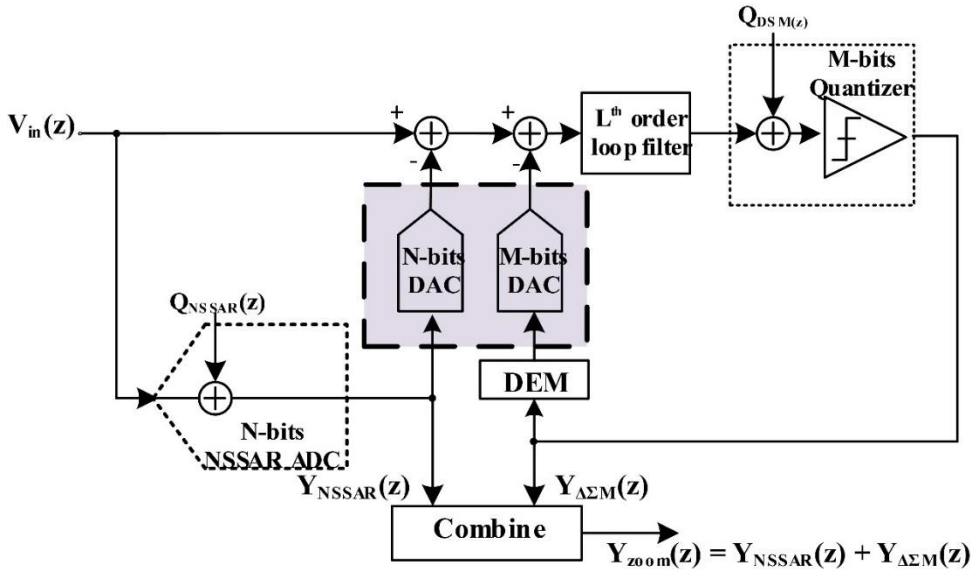


Figure 2.10: Simplified Proposed zoom ADC block diagram.

2.8 Goal of this work

This work aims to improve the SNDR of a previous zoom ADC [6], by using a noise-shaping SAR to implement its coarse ADC. In this way, the in-band quantization noise leakage caused by the coarse ADC will be suppressed below the thermal noise floor of the Zoom ADC. As a result, the SNDR of the Zoom ADC will not be limited by the coarse ADC related artifacts, leading to a significant improvement in its resolution and energy efficiency.

3 System-level design

This chapter describes the system parameters of this zoom ADC and the structure of the passive NS-SAR are discussed. Moreover, the requirements and the feasibility of the NSSAR are justified for the use of a zoom ADC, and the theory is verified by MATLAB simulation.

3.1 System-level parameters for zoom ADC

The system-level parameters of the zoom ADC are shown in Figure 3.1 in red. The coarse ADC bits (*N*), loop filter order (*L*), and sampling frequency (*fs*) should be determined such that the system achieves high resolution (SNR=108dB) while minimizing its power consumption. To obtain the target SNR, the SQNR of the system should reserve a 10dB margin, which is 118dB. Furthermore, the dynamic element matching (DEM) algorithm is required to ensure a low distortion level, and reach the target SNDR of 108dB.

Similar to a normal DSM, a higher-order loop filter (*L*) gives aggressive in-band noise suppression. However, a DSM with a high-order loop filter tends to exhibit instability and the additional integrators increases area.

To decrease the in-band quantization noise of the coarse ADC, its resolution (*N*) can be increased. However, increasing *N* results in higher digital power consumption, as the DEM block needs to operate at the same clock rate of the coarse ADC and process 2^N-1 levels. Moreover, higher *N* reduces the maximum tolerable input frequency since it results in overload issues in the zoom-ADC [2].

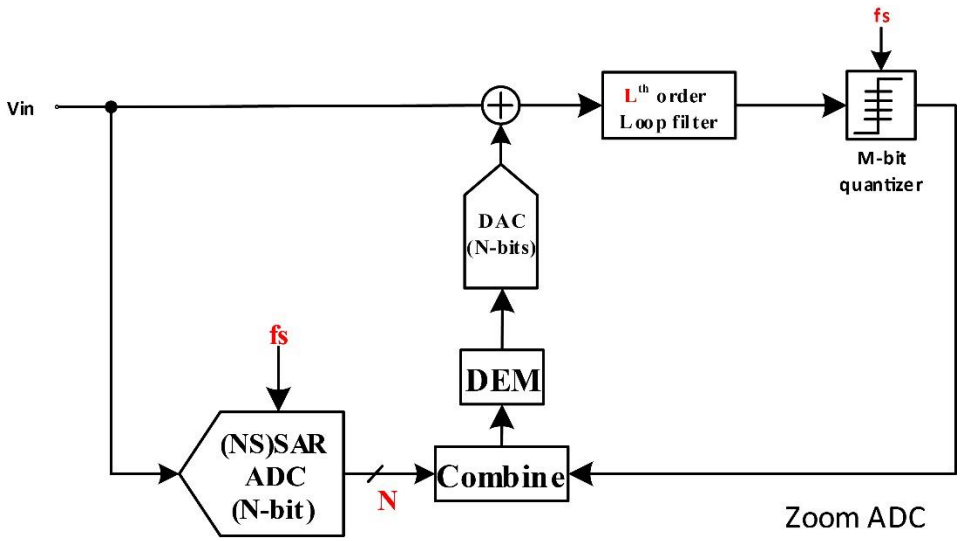


Figure 3.1: Block diagram of the zoom ADC.

Higher sampling rates (*fs*) help reduce the in-band noise by increasing the OSR and improves the maximum input frequency, as discussed in [2]. For an L^{th} order DSM, doubling the OSR improves the SQNR by$(2L+1)\cdot 6dB$ [11]. However, the digital power consumption which is proportional to the sampling rate also increases. Therefore, it is essential to minimize the sampling rate while meeting SQNR specifications.

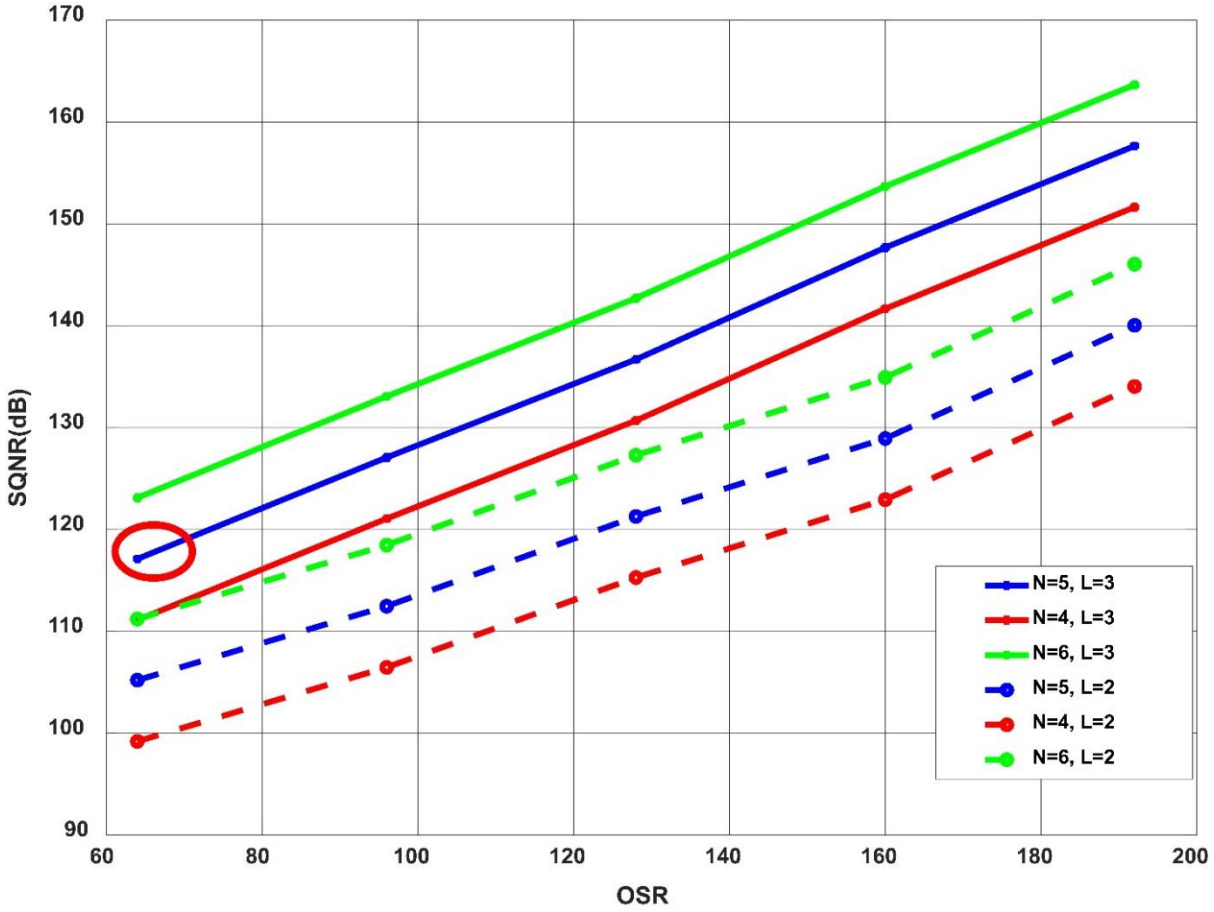


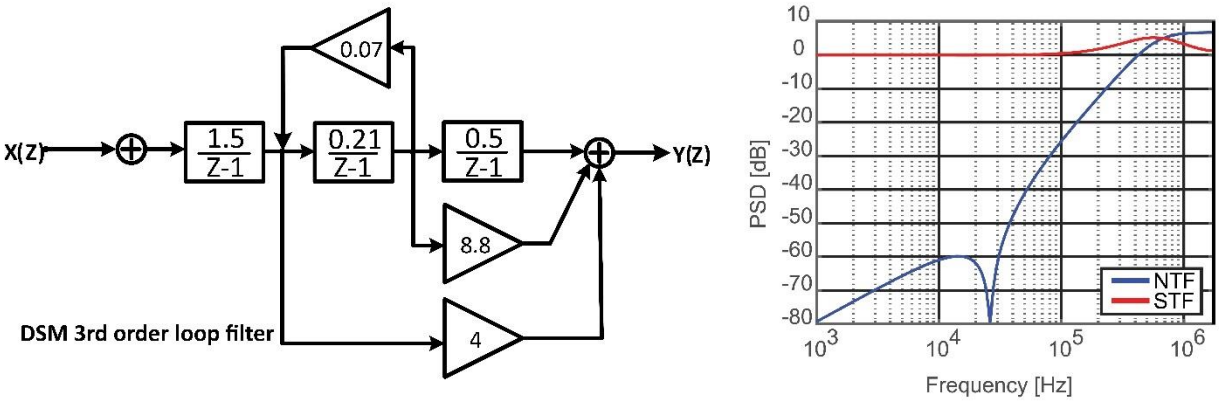
Figure 3.2: Peak SQNR vs OSR for different coarse ADC bits (N) and DSM modulator order (L).

Figure 3.2 illustrates the peak SQNR versus OSR for coarse ADC bits (N) and DSM modulator order (L). It can be seen that a 3rd order loop filter with a 5-bit coarse ADC meets the target SQNR of 118dB at the lowest sampling rate. For the same SQNR target, a higher *N* or a higher *fs* will result in unnecessary digital power consumption.

In this design, a 5-bit SAR, 3rd order DSM, and 2.5MHz sampling rate are chosen to achieve the target of SNDR =108dB with an SQNR = 118dB in a 20 kHz BW [1].

3.1.1 Loop filter coefficient

Figure 3.3a shows the block diagram of the loop filter and its coefficients. The 3rd order CIFF DSM loop filter with a notch around the signal bandwidth edge is inherited from [1]. Figure 3.3b shows the magnitude of the NTF and STF. The notch of the NTF is placed at 16kHZ for the optimal inband SQNR performance. The STF peaking can be observed at a high frequency. This causes Q_{SAR} leakage, as addressed in the previous chapter.



(a) *(b)*

Figure 3.3: CIFF DSM Loop-filter (a) block diagram (b) STF and NTF as illustrated in [1].

3.2 NS-SAR

There are a few requirements that should be considered for implementing an NS-SAR ADC as the coarse converter of the zoom ADC. First, the noise-shaping SAR ADC should suppress the in-band correlated quantization error below the thermal noise level. Second, the NTF of the NS-SAR should be stable. Furthermore, the NS-SAR must be energy efficient. Finally, the combination of the NS-SAR with a DSM should achieve > 118dB SQNR.

3.2.1 Fully passive NS-SAR

Figure 3.4 illustrates a simplified block diagram of an M^{th}-order CIFF NS-SAR with a different type of integrators. Compared to a SAR ADC, a NS-SAR ADC employs additionally an M^{th}-order loop filter and *M*-input comparator. Each integrator can be implemented by using active or passive circuitry. In an active NS-SAR, an OTA-based integrator is used to integrate a previous residue voltage and an *M* input comparator is employed to sum the outputs of the integrators and the input signal. As result, an active NS-SAR is less energy-efficient and requires additional area for the integrators and the multi-input comparator. Thus, the active NS-SAR is not the optimal structure to implement in a zoom ADC since high-order noise shaping is not required.

To obviate the need for a power-hungry OTA-based integrator in a CIFF NS-SAR ADC, recent works [4, 18-21] demonstrate possibilities to implement a fully passive noise shaper by only using switches and capacitors. As shown in Figure 3.4, the difference between fully passive NS-SAR and active NS-SAR is the type of integrator. The residue integration is done by charge sharing between the residue sampling capacitor and the residue integrating capacitor. Due to the charge sharing, the residue voltage suffers from an attenuation, this attenuation can be compensated by introducing a gain ratio between residue and signal input pairs of the *M*-input comparator [20]. Another side effect for charge sharing is that the charge cannot be fully integrated on the integrating capacitor. Therefore, a passive NS-SAR has a weaker in-band noise suppression compared to the active NS-SAR.

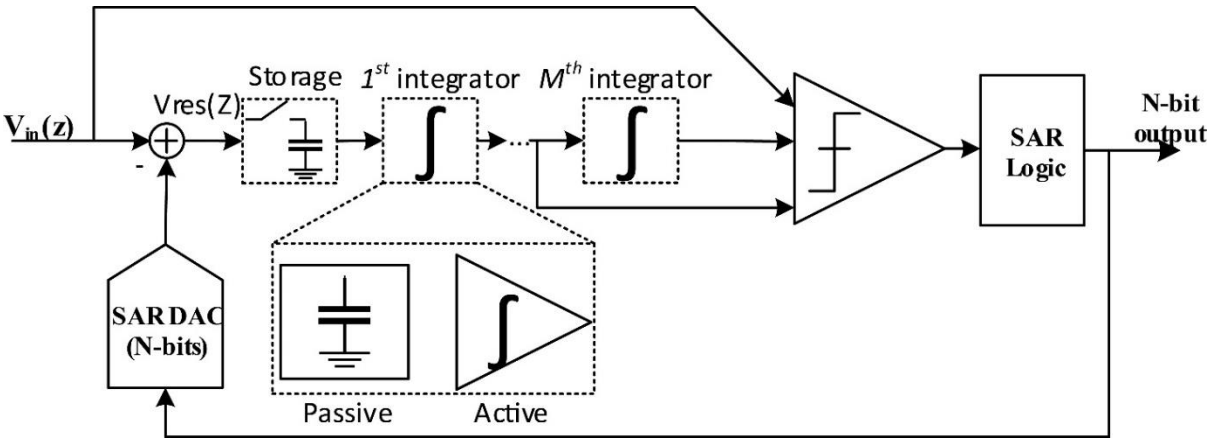


Figure 3.4: Block-diagram of an M^{th} order CIFF NS-SAR.

The in-band quantization error suppression of the NS-SAR relies on the design of the residue loop filter. Similar to a DSM, a higher-order filter embedded in NS-SAR enables more aggressive quantization noise suppression. In a fully passive NS-SAR, the order of the NTF can be increased by simply adding an extra integrating capacitor, and an extra path in the comparator to compensate for the residue attenuation due to the charge sharing [21].

Although the passive NS-SAR has a limited improvement on quantization error, its cost-efficiency and robustness suit well in the zoom ADC application. Figure 3.5 compares different NTFs of the active and passive NS-SAR ADCs at the oversampling ratio (OSR) of 62.5. The active first-order NS-SAR ADC achieves good noise suppression but results in lower energy-efficiency [13]. On the other hand, a passive NS-SAR can have over 24dB in-band noise suppression with second-order noise-shaping [21] and 10dB with first-order noise-shaping [4], while keeping the energy efficiency of the SAR ADC.

Figure 3.6 shows the pole zero locations of the NTFs implemented in Figure 3.5 [13, 20, 21]. The zero of the 1^{st} order active NS-SAR is placed on the unit circle, which is comparable to an ideal 1^{st} order DSM. Due to the charge sharing process in the residue integration, the zero of the 1^{st} order passive NS-SAR shifts within the unit-circle. The extra integrator in 2^{nd} order passive NS-SAR introduces an additional zero at the same NTF location, if the gain ratio of comparator inputs fully compensate the voltage attenuation due to the charge sharing.

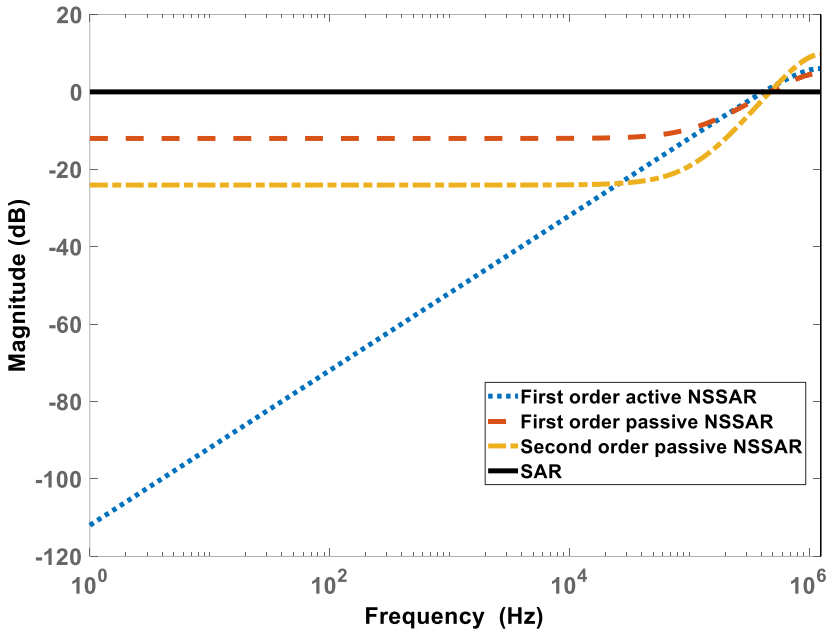


Figure 3.5: NTF of different NS-SAR architectures.

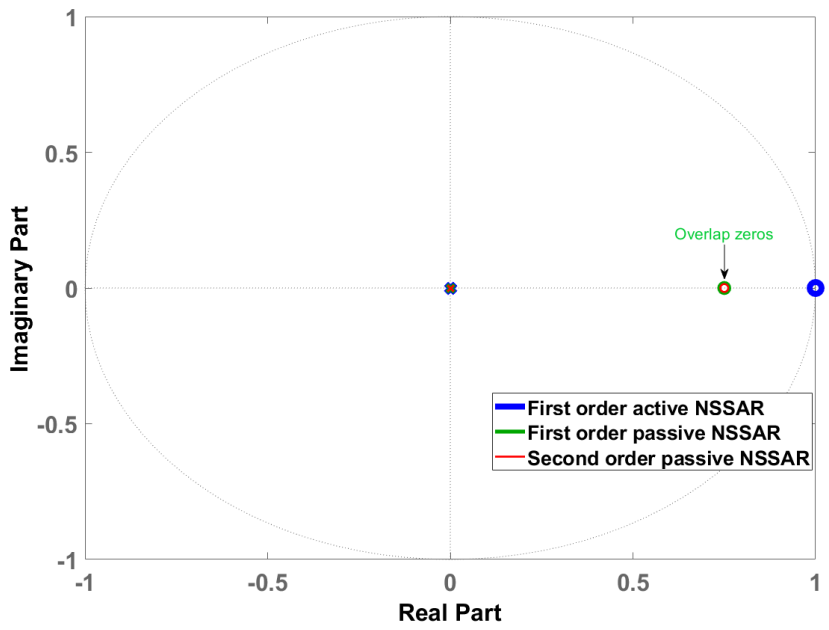


Figure 3.6: Pole-zero locations of different NS-SAR architectures.

Figure 3.7 compares different order noise-shapers attached to a conventional SAR ADC. The SAR ADC's SQNR can be improved by 10 dB and 24dB by employing a first-order and second-order passive noise shaping respectively.

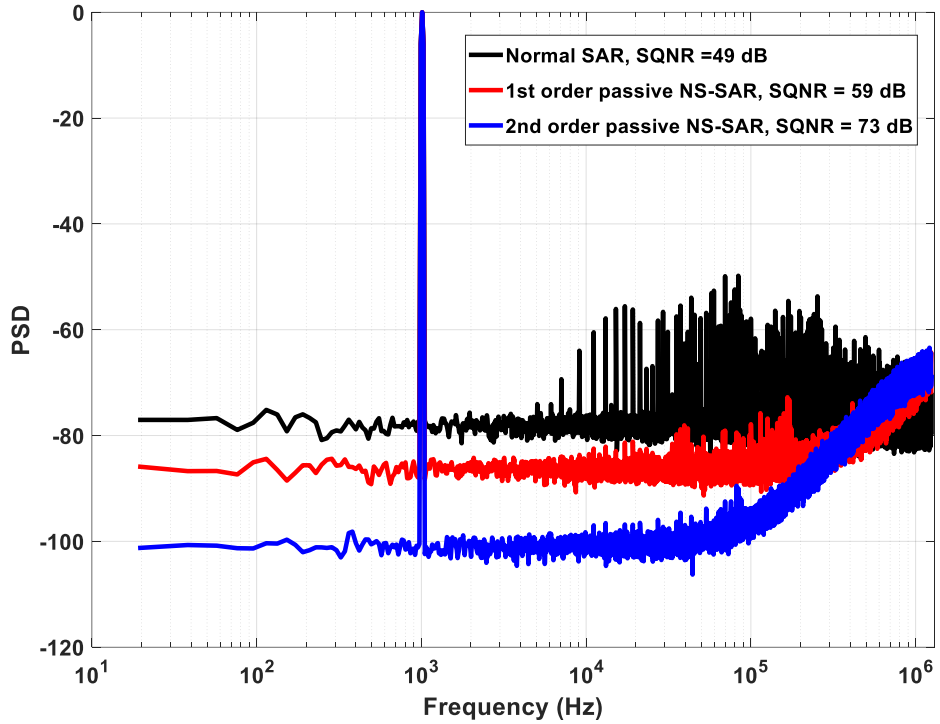


Figure 3.7: Output spectrum of different order passive NSSAR.

3.3 NS-SAR in Zoom ADC

Figure 3.8 shows the output of a regular SAR ADC and an NS-SAR. In a regular SAR ADC, the output level remains relatively static. On the contrary, the NS-SAR's output toggles between two levels ($K \cdot V_{LSB} \sim (K+1) \cdot V_{LSB}$), exhibit a behaviour similar to a delta-sigma modulator, which is because the residue voltage participates the SAR conversion. Note that, the NS-SAR only toggles at the edge transition, because the residue tends to be higher in this area, while the flat-level indicates that the NS-SAR make the same decision as SAR ADC because in this case, the residue is too small to cause the toggles on NS-SAR. This toggling can be tolerated by using minimal over-ranging ($(K-1) \cdot V_{LSB} \sim (K+2) \cdot V_{LSB}$) in the zoom ADC.

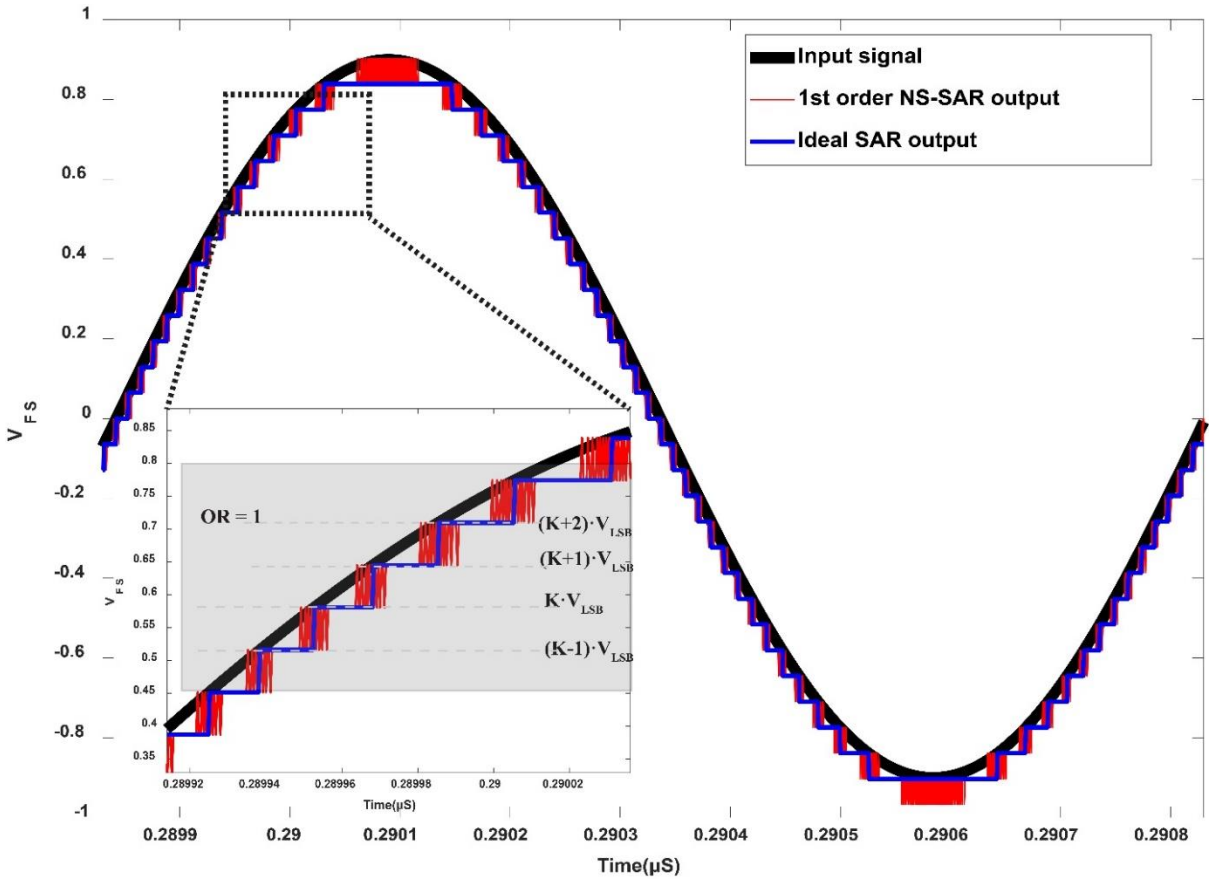
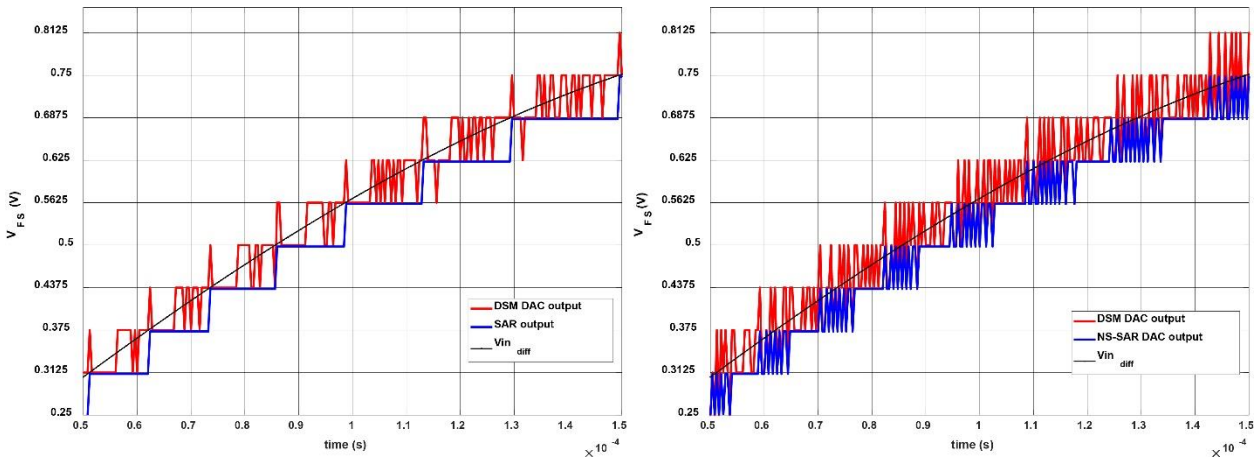


Figure 3.8: SAR output with/without a 1st order passive noise shaper.

Figure 3.9 describes the time domain output of the zoom ADC with SAR ADC or NS-SAR ADC. Compare Figure 3.9a with Figure 3.9b**,** both the *N*-bits conventional SAR ADC and the *N*-bits NS-SAR ADC defines 2^N reference levels for the DSM, under these circumstances, the SQNR of the zoom ADC will not be influenced by employing an NS-SAR as the coarse ADC.



(a) *(b)*

Figure 3.9: Time domain output comparison (a) Zoom ADC with Normal SAR ADC (b) Zoom ADC with NS-SAR

The noise-shaping of the SAR helps to de-correlate the in-band quantization error. This is shown in Figure 3.10, the SQNR of the zoom ADC improves from 106.7dB to 115.4dB by employing a passive noise-shaping SAR, which demonstrates a significant reduction in the Q_{sar}. Here, some harmonics from the SAR are still visible above the thermal noise level and degrade the linearity performance, because in a first-order passive NS-SAR, the residue voltage is still correlated to the input signal.

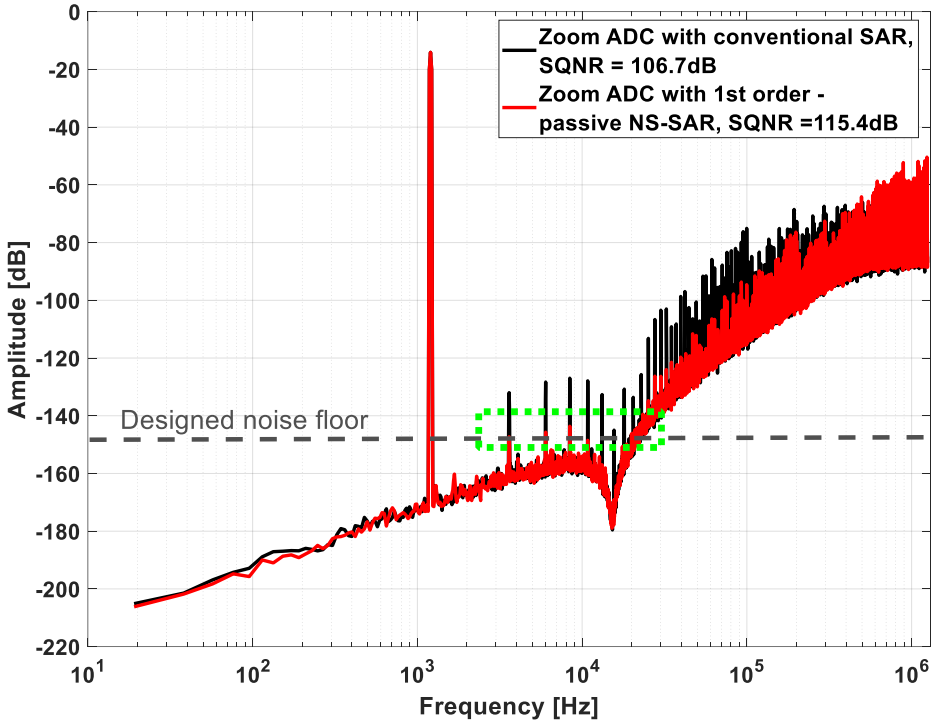


Figure 3.10: Output spectrum of a zoom ADC with a 1st order passive NS-SAR.

There are two ways to reduce these tones. The first method is to implement a second-order NS-SAR, which has a more aggressive NTF and a less correlated residue. This results in tones being fully suppressed, as seen in the output spectrum of Figure 3.11.

An alternative method is to apply dithering in a 1st order passive NS-SAR to decorrelate the quantization error. The implementation of the dithering will be discussed in the next section.

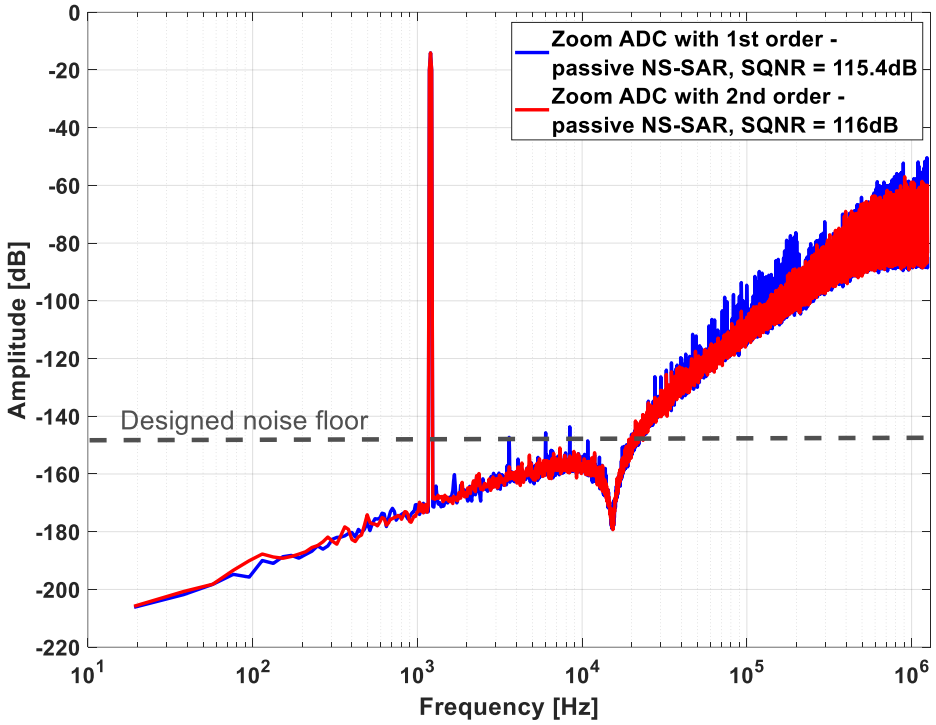


Figure 3.11: Output spectrum of a Zoom ADC with a 2nd order passive NS-SAR.

3.3.1 Dithering

Dithering is a well-known technique to improve the linearity of the DSM [22]. It can be used in the first-order NS-SAR to decorrelate the quantization error and reduce harmonic distortion.

However, introducing dither increases the noise floor. In this work, a small dither (1/4 LSB) is chosen to decorrelate the coarse ADC's quantization error. This comes at the cost of only a small SQNR loss of 0.4dB. A 1st order NS-SAR with a small dither can suppress the tones below the thermal noise level as depicted in Figure 3.12. The 1st order NS-SAR gives a similar SNDR improvement as a 2nd order NS-SAR, but it obviates the need for an extra path for the N-input comparator, and the area of the noise shaper is much less.

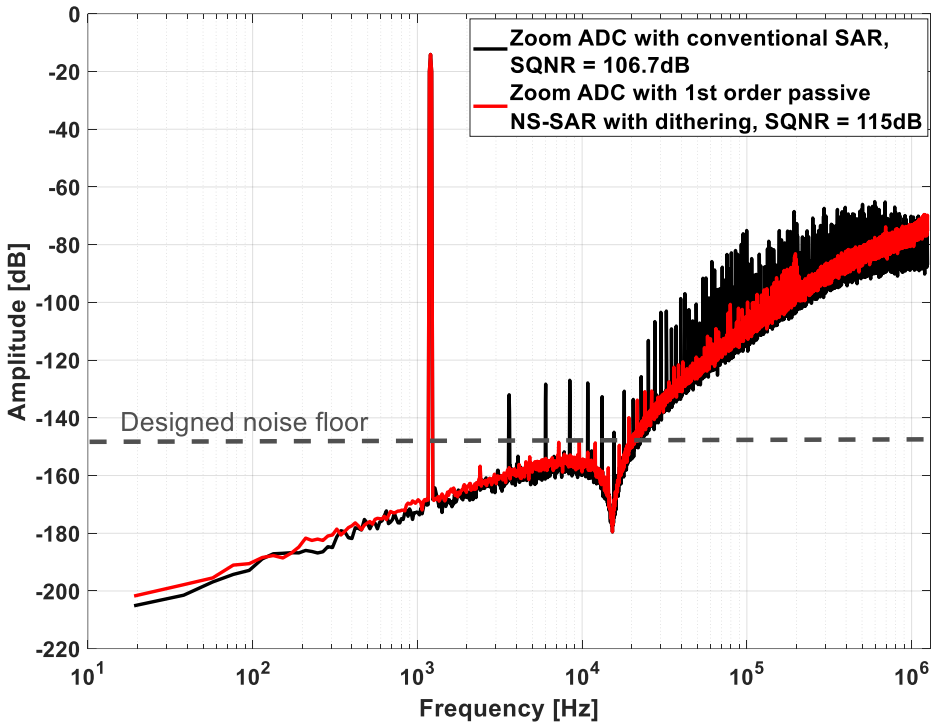


Figure 3.12：Output spectrum of Zoom ADC with 1st order passive NS-SAR(dithered)

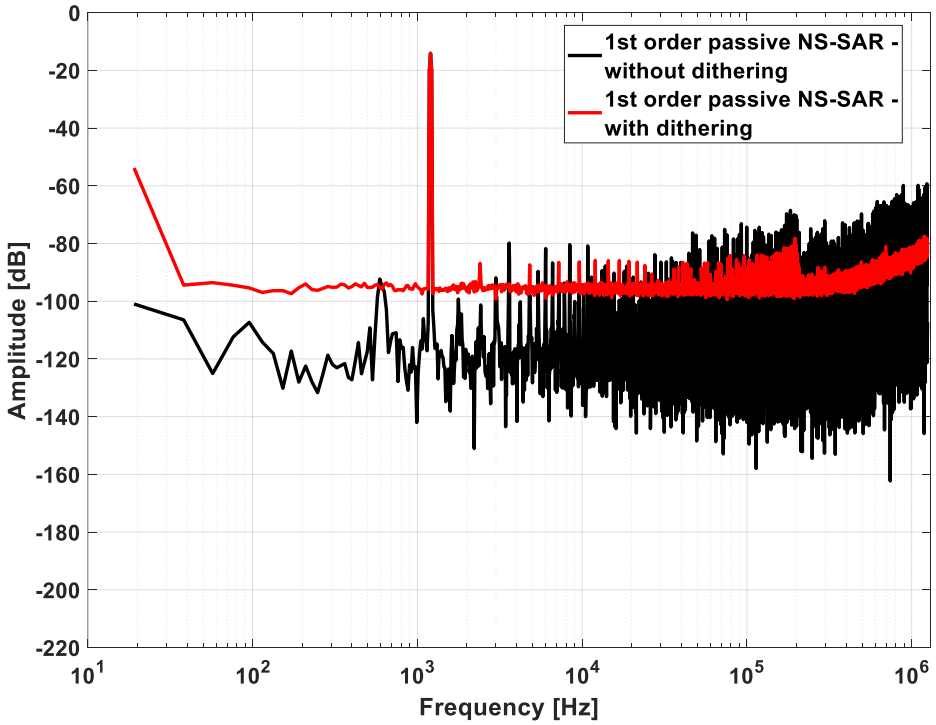


Figure 3.13：Output spectrum of 1st order passive NS-SAR with ¼ LSB dithering.

3.4 Error and Quantization Noise Leakage of NS-SAR ADC

In this zoom ADC, the noise-shaped quantization error ($NTF_{SAR} \cdot Q_{SAR}$) and harmonics of the NS-SAR ADC are processed by a CIFF DSM. The error and Quantization noise leakage of the NS-SAR ADC can be expressed as Equation 2.18.

Therefore, the NTF of the DSM defines the level of tones that leaks from the SAR ADC to the output of the zoom ADC. As shown in Figure 3.3b, the NTF of the delta-sigma modulator can suppress the errors introduced by the NS-SAR by around 60dB. This suppression would degrade as the frequency of error moves outside of the signal band. As also shown in Figure 3.12, there is almost no error suppression beyond 200KHz.

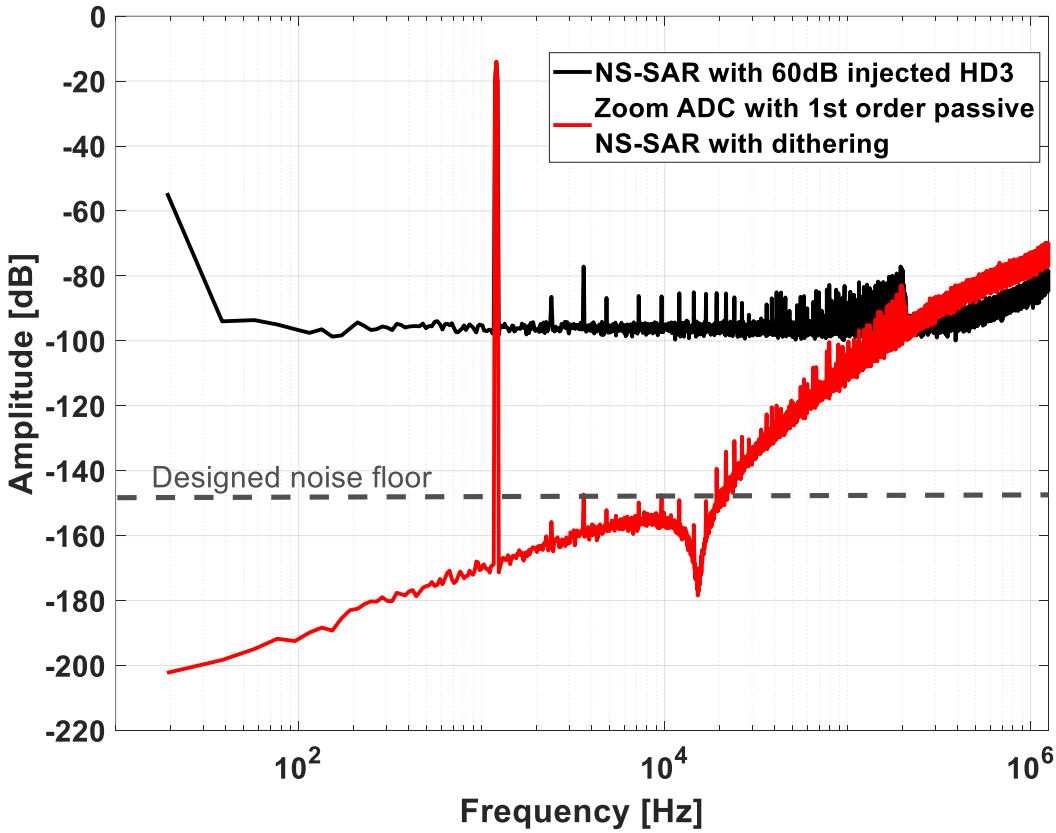


Figure 3.14: Tone tolerance for Zoom ADC with 1st order passive NS-SAR (dithered).

As shown in Figure 3.15, an HD3 of 60dB is better than what can be expected with a unit capacitor mismatch σ of up to 5%. This means that the required matching of the SAR DAC is quite relaxed.

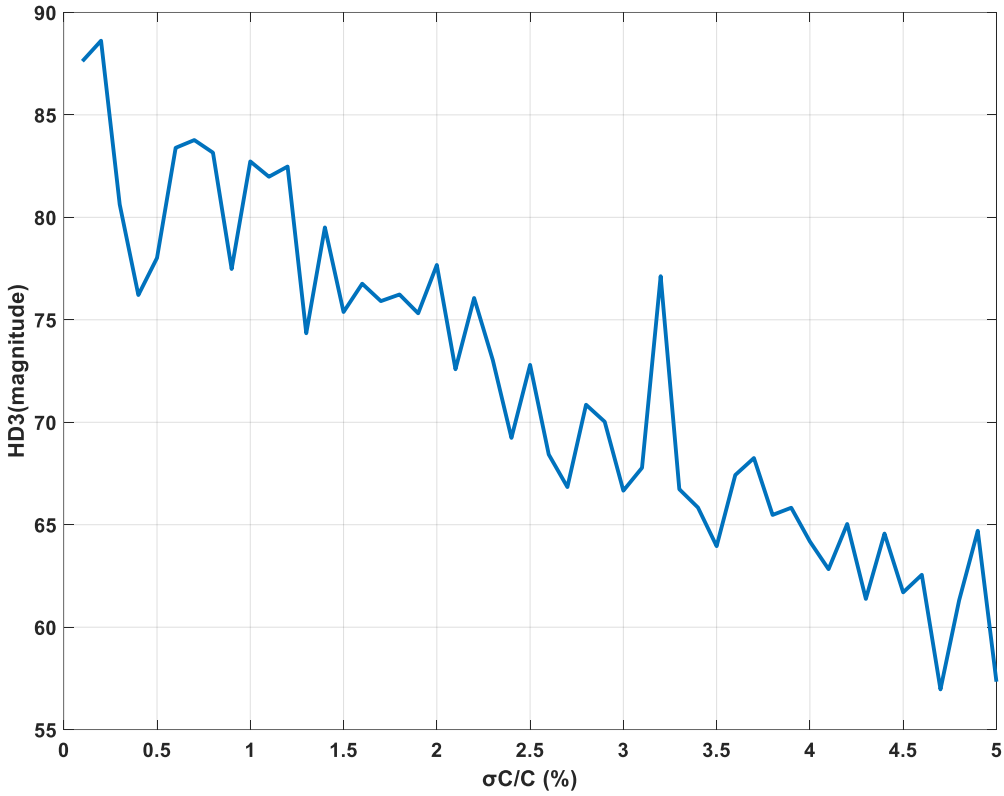


Figure 3.15: Unit capacitor mismatch vs. HD_3 of the SAR ADC.

3.5 Architecture summary

Figure 3.16 shows the complete zoom ADC. It is composed of a 1st order NS-SAR with dithering and a 3rd order DSM with a 2-bits flash quantizer.

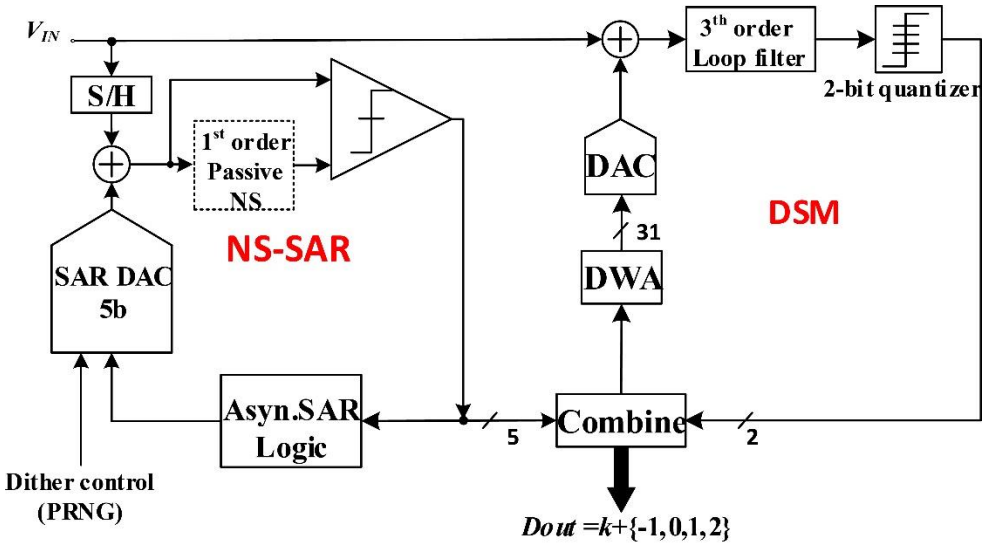


Figure 3.16: Implemented zoom ADC block diagram.

This architecture achieves 109 dB of DR and 108dB of SNDR within the audio bandwidth (20kHz), with a low sampling rate of 2.5MHz. Figure 3.17 shows the SNR and SNDR across input amplitude at 1 kHz. The SNDR is very close SNR, which means that the in-band error leakage of the NS-SAR is well below the thermal noise floor of the zoom ADC.

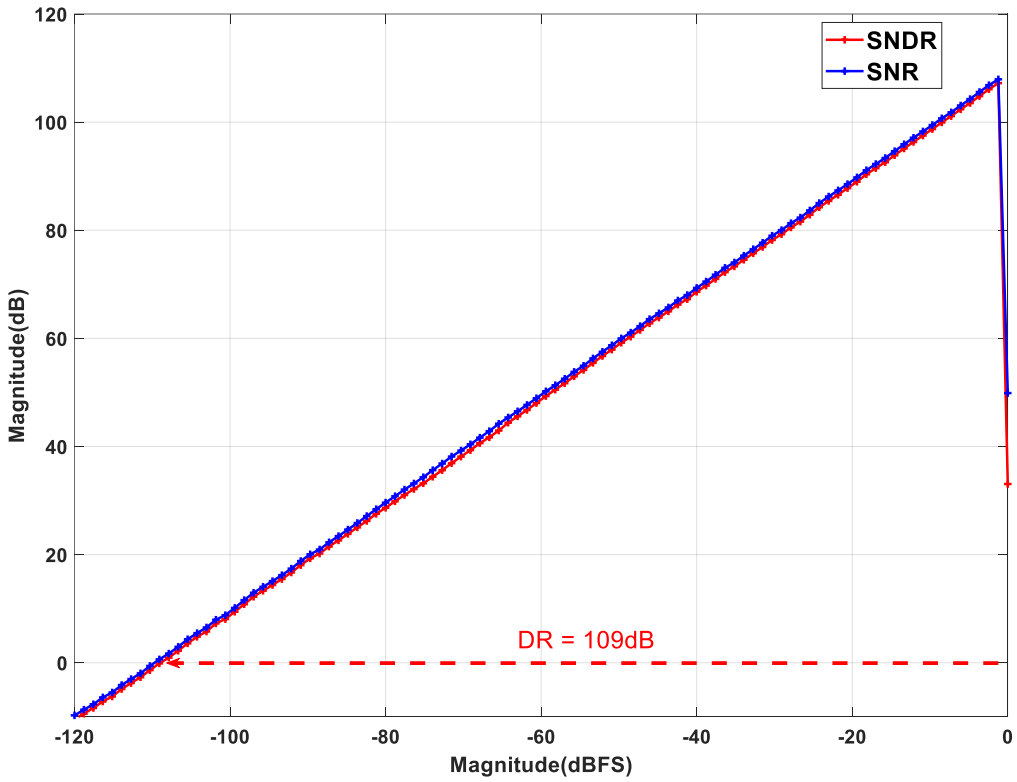


Figure 3.17: SNR/SNDR vs. an input signal amplitude (f_{in}=1kHz).

4 Circuit implementation

This chapter describes the circuit implementation and presents circuit simulation results of the proposed zoom ADC.

4.1 Asynchronous NS-SAR ADC design

As discussed in the previous chapter, a 5-bit NS-SAR ADC is used as a coarse ADC in parallel with a 3rd order DSM to obtain high SQNR with a low digital power [1]. The coarse ADC in this work uses the same asynchronous SAR logic as [2, 23]. A noise shaping function is introduced in the SAR ADC to reduce its quantization error leakage and achieve the target SNDR.

4.1.1 Noise shaper implementation

A Ping-Pong residue sampling NS-SAR is implemented in this zoom ADC [4]. In this architecture, a differential residue sampling technique is employed to compensate for the attenuation of V_{res} due to the passive residue integration.

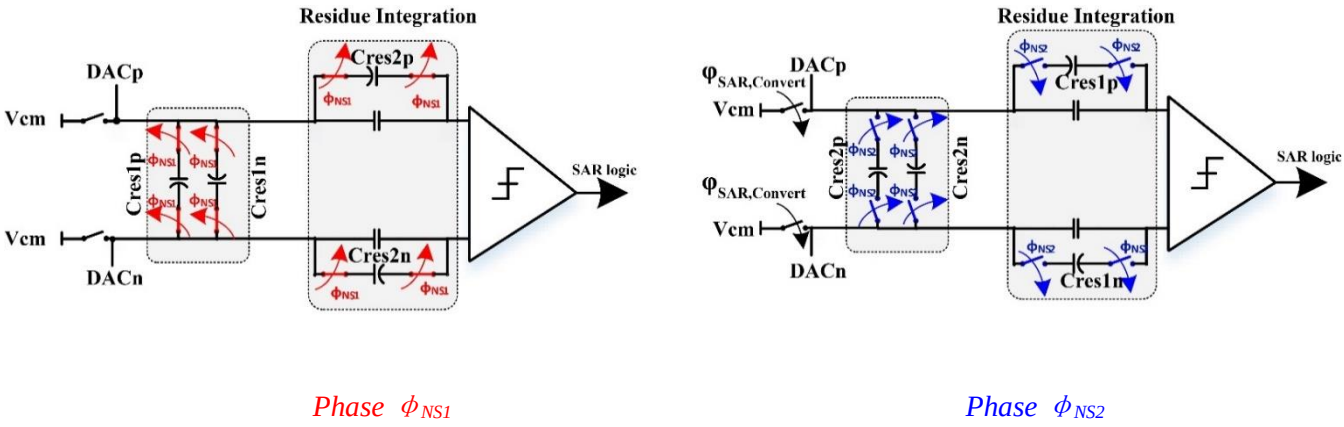


Figure 4.1: Ping-Pong operation of 1st order passive NS-SAR.

Figure 4.1 illustrates the two phases (Φ_{NS1} and Φ_{NS2}) of the Ping-Pong operation for the noise shaper. During the residue sampling phase (Φ_{NS1}), C_{res1p} and C_{res1n} sample the residue voltage that remains at the end of the SAR conversion. A passive gain of 2 is obtained through cross-differential sampling. During the residue integration phase (Φ_{NS2}), C_{res1p} and C_{res1n} are disconnected from the DAC and connected to the integration capacitor C_{intp} and C_{intn}. C_{res1p} holds the differential residue charge from the residue sampling phase and performs charge sharing with C_{intp}, while C_{res1n} holds the negative differential residue charge and performs charge sharing with C_{intn}. Simultaneously, C_{res2p} and C_{res2n} do the same as C_{res1p} and C_{res1n}, but at opposite phases.

4.1.1.1 Timing

The timing diagram of the zoom ADC is shown in Figure 4.2. At the beginning of the sampling phase φ1, the SAR DAC samples the input, and the residue from the previous conversion is integrated through passive charge sharing. A SAR ADC conversion then takes place, controlled

by asynchronous logic that is inherited from a previous design [1, 2], and takes ~30ns. Note that the conversion time should guarantee the residue settles on the residue sampling capacitors ($C_{res1p,1n}$ or $C_{res2p,2n}$).

At the end of sampling phase φ1, the input signal is sampled on the DSM sampling capacitors. Before $\phi 2$, the zoom ADC combines the SAR output and $\Sigma\Delta$ output.

The NS clock phase φ_{NS1} and φ_{NS2} are generated by a conventional non-overlapping generator [24].

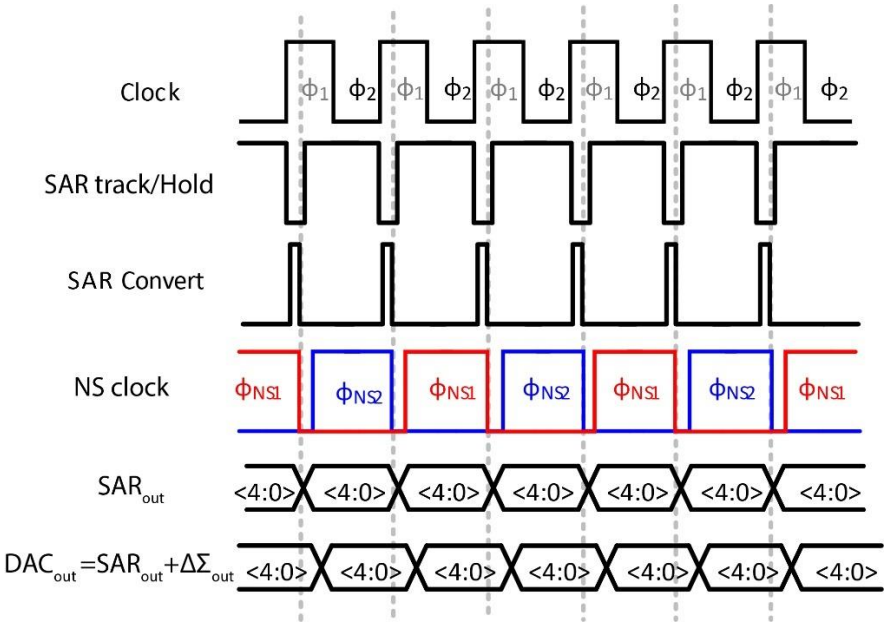


Figure 4.2: Timing diagram of the zoom ADC.

4.1.1.2 Noise shaping transfer function

Figure 4.3 shows a signal diagram of the Ping-Pong 1st order passive NS-SAR. The charge sharing attenuation factor α is compensated by the differential sampling factor g. The signal transfer function can be obtained as:

$$D_{out}(z)=V_{in}(z)+\frac{1-(1-\alpha)z^{-1}}{1-(1-\alpha-g\alpha)z^{-1}}\cdot(Q(z)+V_{n,comp}) \qquad 4.1$$

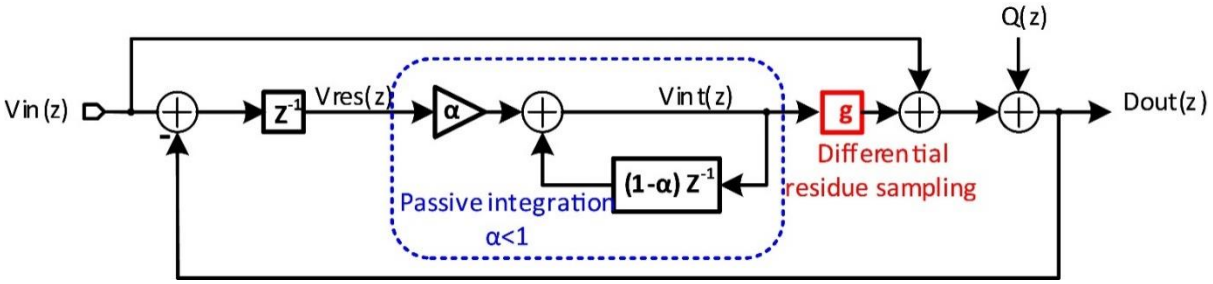


Figure 4.3: 1st order Passive NS-SAR signal diagram

The differential residue sampling factor g is 2, and the attenuation factor α, which is the ratio of the residue sampling capacitors and integrator capacitors ($C_{res1p,n}$ ($C_{res2p,n}$) and $C_{intp,n}$, respectively), is designed to be 1/2 and is described in Equation 4.2

$$\alpha = \frac{C_{int}}{C_{res} + C_{int} + C_{parasitic}} \tag{4.2}$$

The NTF shows that the pole and zero locations are only related to the attenuation factor α. For an attenuation factor of α = 0.5, the NTF has zero at 0.5 (z = 0.5) and a pole at -0.5 (z = -0.5).

$$D_{out}(z) = V_{in}(z) + \frac{1 - 0.5z^{-1}}{1 + 0.5z^{-1}} \cdot (Q(z) + V_{n,comp}) \tag{4.3}$$

4.1.1.3 Mismatch and parasitic effect

Capacitor mismatch and parasitic capacitor contribute to a shift in attenuation factor α, which causes the ratio to deviate from 0.5 and shifts the pole and zero locations.

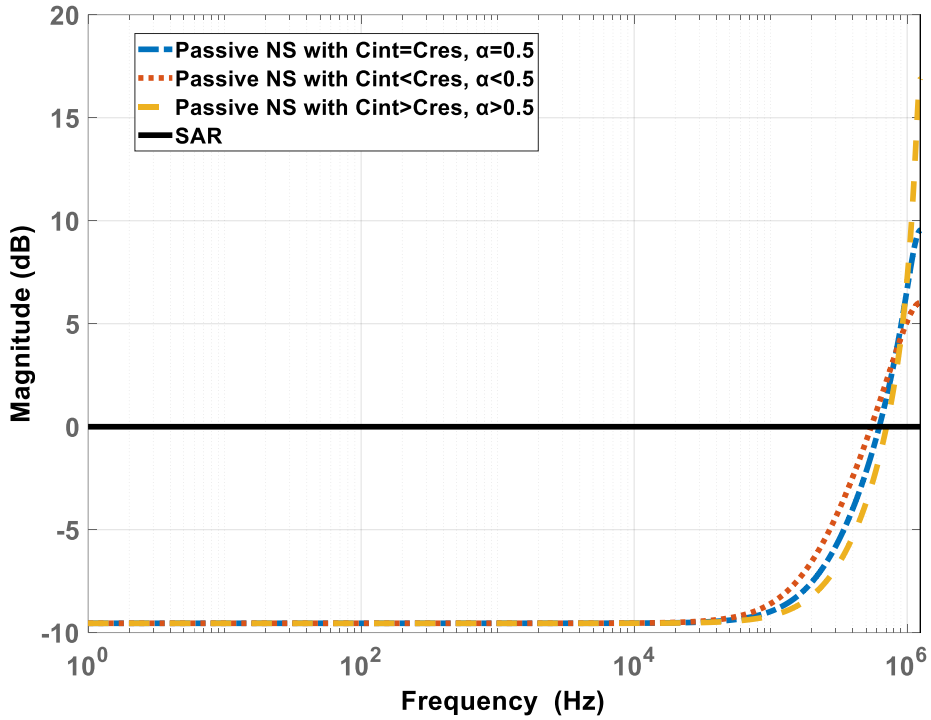


Figure 4.4: Magnitude of the NTF as a function of α

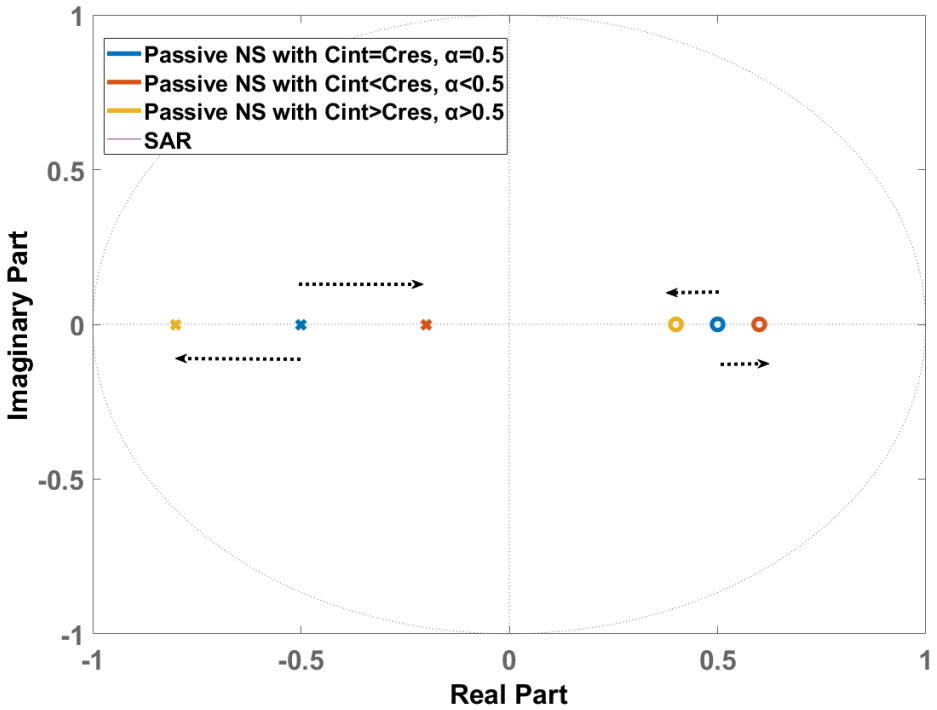


Figure 4.5: Pole-zero location of the NTF as a function of α

The change of the magnitude and pole-zero location of the NTF versus attenuation factor α is illustrated in Figure 4.4 and Figure 4.5. In Figure 4.5 when $\alpha = 0.5$, the zero is placed at 0.5, and the pole is placed at -0.5, rendering the standard NTF of the chosen architecture. If α increases, then pole moves to left and zero moves towards unit circle, causing higher peaking in the NTF. If α reduces, then pole moves to right and zero moves away from unit circle, causing a mild out of band peaking in the NTF.

In this structure, the change of the pole-zero location will not compromise the in-band quantization error suppression, as shown in Figure 4.4. However, at the case of C_{int}>C_{res}, the NS-SAR exhibit a higher out of noise as illustrated in Figure 4.4, which might challenge the minimal over-ranging setting in the zoom ADC. As shown in Figure 4.6, when $\alpha > 0.5$ the SAR ADC toggles aggressively, and the toggling range becomes more than 1LSB, which indicates the over-ranging cannot cover the error decision of the SAR ADC.

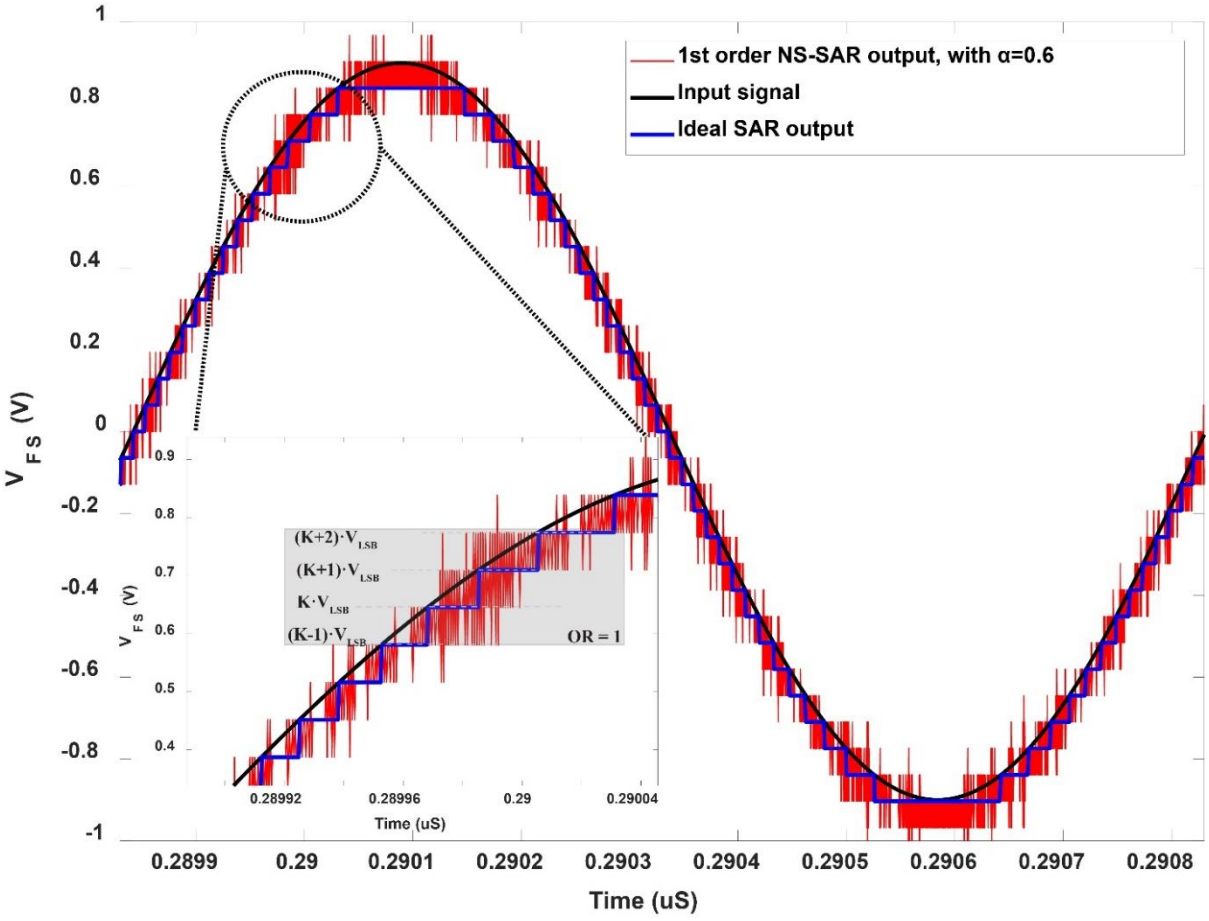
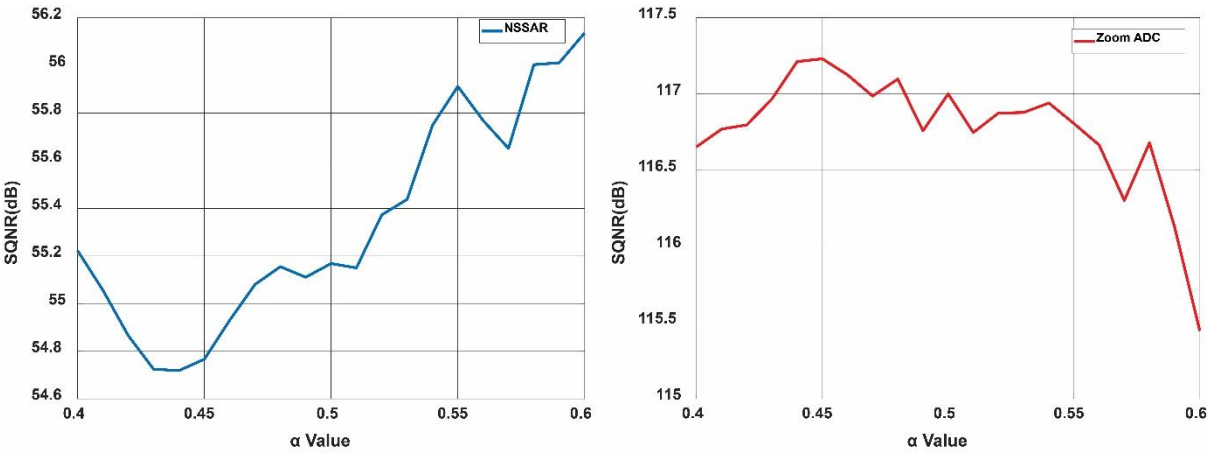


Figure 4.6: NSSAR output with $\alpha > 0.5$.

Figure 4.7 shows the simulated SQNR of the NSSAR and zoom ADC versus different attenuation factors α. As shown in Figure 4.7 (a), the SQNR of the NS-SAR ADC improves as α increases. However, as discussed previously, it will result in a higher out of band noise and NS-SAR output code exhibits values beyond over-ranging. Therefore, the SQNR of the zoom ADC degrades over the increased α as shown in Figure 4.7 (b). Thus, this design requires careful layout to avoid the SQNR degradation of the zoom ADC.



(a) *(b)*

Figure 4.7: Simulated SQNR versus attenuation factor α (a) NSSAR (b) Zoom ADC.

4.1.1.4 Excess noise contributions

In this passive CIFF NS-SAR structure, noise is sampled during the different phases.

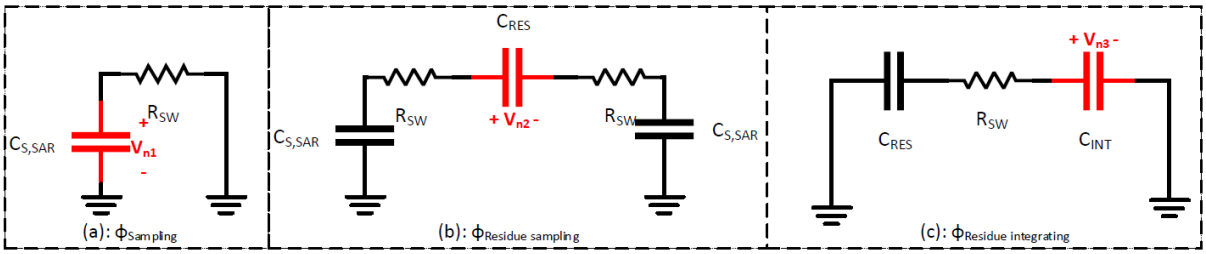


Figure 4.8: Primary noise sources from the NS-SAR.

Figure 4.8 explains the sources of sampled noise. Figure 4.8(a) shows sampled noise V_{n1} of the single-sided SAR DAC ($C_{S,SAR}$) during the SAR input sampling phase ($\Phi_{Sampling}$), where R_{sw} is the on-resistance of the sampling switch.

$$V_{n1}^2 = \frac{kT}{C_{S,SAR}} \qquad 4.4$$

Figure 4.8(b) and Figure 4.8(c) illustrate the noise contributions from the noise shaper. Extra noise is obtained during sampling of Φ_{NS1} and Φ_{NS2}. V_{n2} is introduced at the end of the residue sampling phase per C_{res}. Similarly, V_{n3} is sampled at the end of the residue integrating phase.

$$V_{n2}^2 \approx \frac{kT}{C_{res}} \quad 4.5$$

$$V_{n3}^2 \approx \frac{kT}{C_{res} + C_{int}} \quad 4.6$$

By combining Equation 4.4, 4.5, and 4.6, the corresponding total integrated noise for a differential implementation can be calculated as:

$$V_n^2 = 2 \cdot \left(\frac{kT}{C_{S,SAR}} + \frac{kT}{C_{res}} + \frac{kT}{C_{res} + C_{int}} \right) \quad 4.7$$

Table 4-1 summarizes the noise-budget of the NS-SAR. In a 5-bit conventional SAR, the quantization error dominates the noise source. However, in this NS-SAR, the thermal noise dominates due to the shaping of the quantization noise. As shown in Equation 4.7, the noise is limited by the C_{res}, C_{int}, and $C_{S,SAR}$. Hence, the size of the C_{res} and C_{int} should be large enough to ensure their noise contribution is insignificant. The capacitance of the C_{res} and Cint is chosen as 4x the unit capacitance (7.2fF) to meet the thermal noise requirement.

Table 4-1: The system level noise budget of the NS-SAR

SNR	SAR Value(dB)	NSSAR Value(dB)
SQNR	49	58
$SNR_{Thermal}$	70	55
SNR_{Total}	49	54.7

4.1.2 Dither implementation

The bottom plate sampling technique is used to optimize the linearity of the SAR ADC [25], and the dithering is used to de-correlate the quantization error of 5-bit SAR ADC. Figure 4.9 illustrates the sample & hold (S/H) network and the dithering implementation. Same as the S/H network, the dither switch is enabled by φSAR_{track} or $\varphi SAR_{convert}$. The only difference is that, the conversion of the SAR DAC is controlled by the Asynchronous SAR logic, and dithering switch is controlled by the external FPGA.

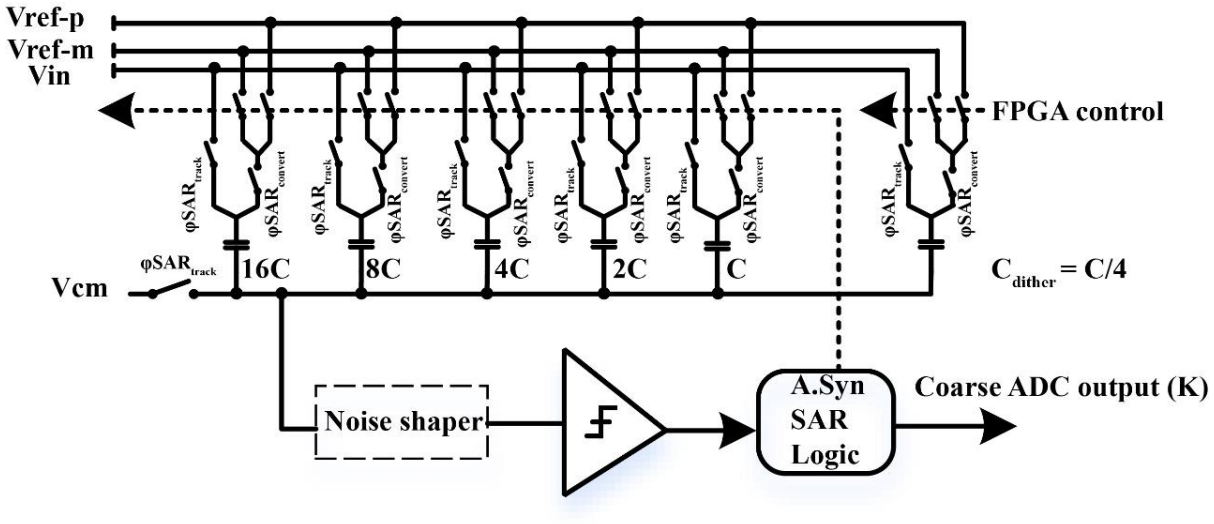


Figure 4.9: Sample & Hold network and dither implementation of the NS-SAR ADC.

4.1.3 DAC

The SAR DAC consists of 31 unit capacitors. Figure 4.10 shows the implementation of the capacitive DAC, which is a modified version of the previous work [1, 2]. The capacitance of each unit capacitor is 1.8fF, resulting in a total DAC capacitance of 55.8fF. Metal fringe capacitors are used for their area efficiency and proper matching. Dummy capacitors are placed next to the DAC to prevent the capacitor deviation due to edge effects. The edge of the dummy capacitors is used as the dither capacitors.

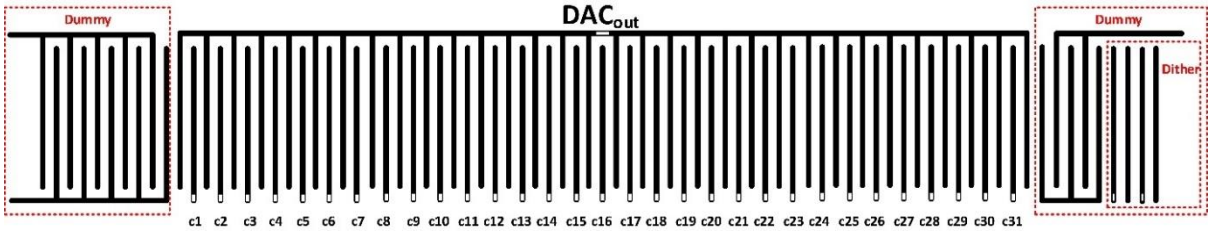


Figure 4.10: Layout of the SAR DAC

The noise shaping capacitors are implemented as illustrated in Figure 4.11. Since C_{res} and C_{int} only contain the residue value, the matching between the SAR DAC and noise shaping capacitors is not critical. Therefore, the noise shaper is implemented separately to simplify routing. Similar to the SAR DAC's implementation, dummy capacitors are used to minimize the edge effects and provide good matching for the noise shaper.

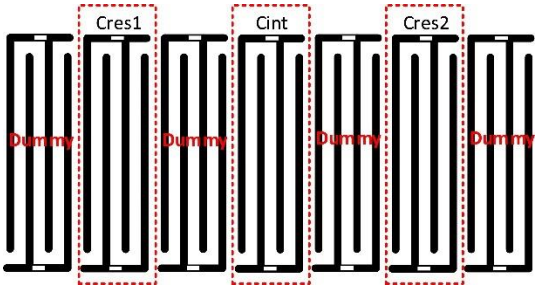


Figure 4.11: Layout of the noise shaper

4.1.4 Dynamic comparator

The dynamic comparator in Figure 4.12 is used in this NS-SAR ADC [2]. The circuit is composed of a pre-amplifier and a dynamic latch. A cascoded MOS is biased by Vb0 in the saturation region to keep the drain current constant to reduce the dynamic offset [9]. The input pair is cascoded to minimize the kick-back to the noise shaper and SAR DAC. The pre-amplifier is dynamic, which results in a low-power comparator.

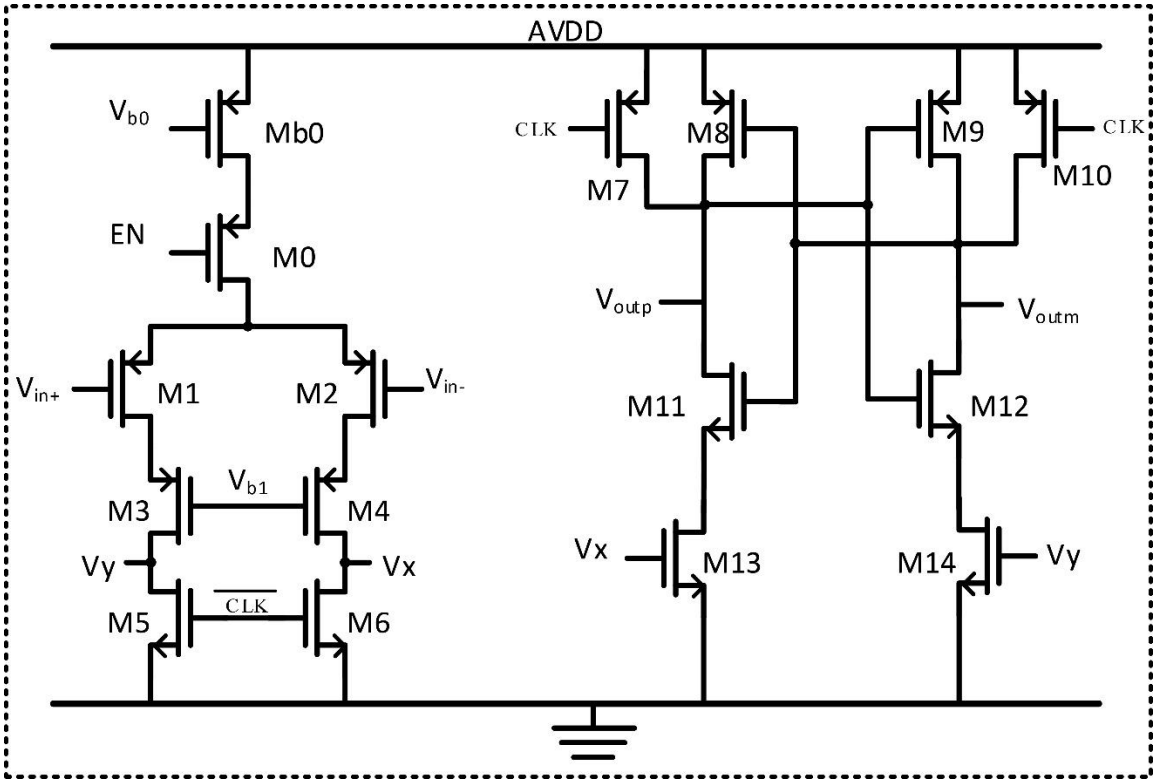


Figure 4.12: Dynamic comparator schematic.

4.2 Delta Sigma Modulator

The DSM in this design employs a discrete-time 3rd order CRFF loop filter with local feedback, where the NTF notch is placed at 16kHz for the optimum SQNR performance [1]. The coefficients of the loop filter are defined by the ratio between capacitors, and the size of the capacitor is determined by the noise and matching requirements. Moreover, a 4-level flash quantizer with a resistive ladder is used to retrieve the SQNR loss due to the over-ranging in the zoom ADC [1, 2].

4.3 Top-Level Simulation Results

Figure 4.13 shows the transient simulation result of the coarse ADC. By adding NS to the SAR ADC, its quantization noise is shaped, which results in around 14dB improvement on SQNR.

Figure 4.14 compares the zoom ADC's with noise shaping "ON" and "OFF". It can be seen that the tones caused by the SAR ADC are significantly suppressed by the NS-SAR. The SNR performance is expected to be limited by thermal noise to 108.5 dB.

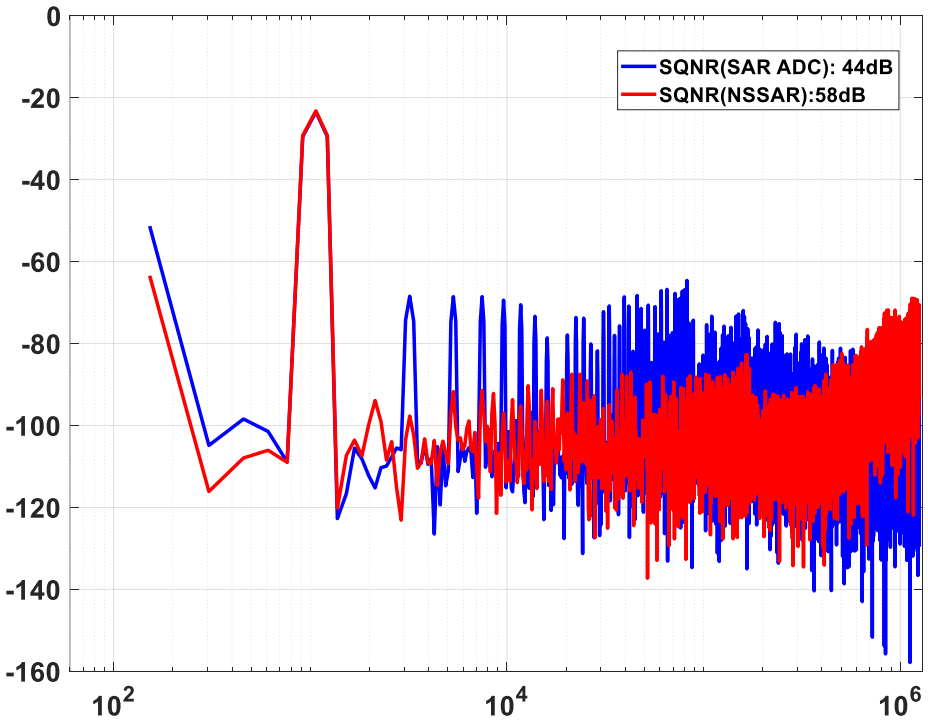


Figure 4.13: Output spectrum of coarse ADC

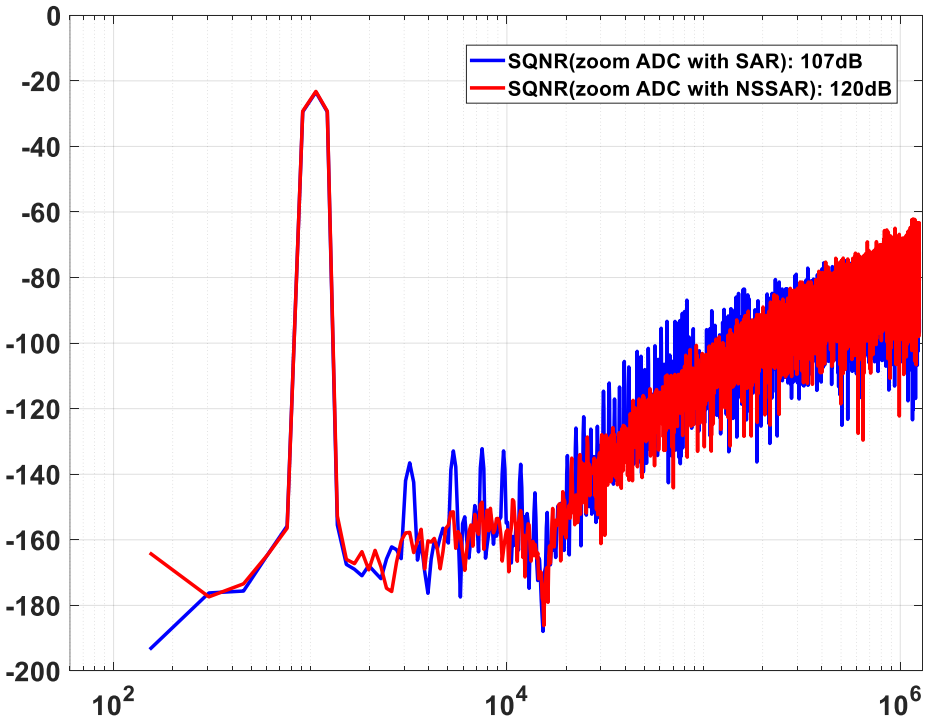


Figure 4.14: Effective tone suppression for zoom ADC with SAR and NS-SAR ADCs.

5 Measurement and evaluation

A chip micrograph of the fabricated ADC in a standard SSMC 160-nm CMOS process is shown in Figure 5.1. The ADC has an active area of 0.29 mm^2, and consists of 4 main blocks: Capacitive CDAC, 3rd order loop filter with quantizer, asynchronous NS-SAR (A.syn NS-SAR) and digital logic. The DSM occupies 0.24 mm^2, and the NS-SAR occupies 0.018 mm^2, with the noise shaper only accounting for 14% of the NS-SAR area.

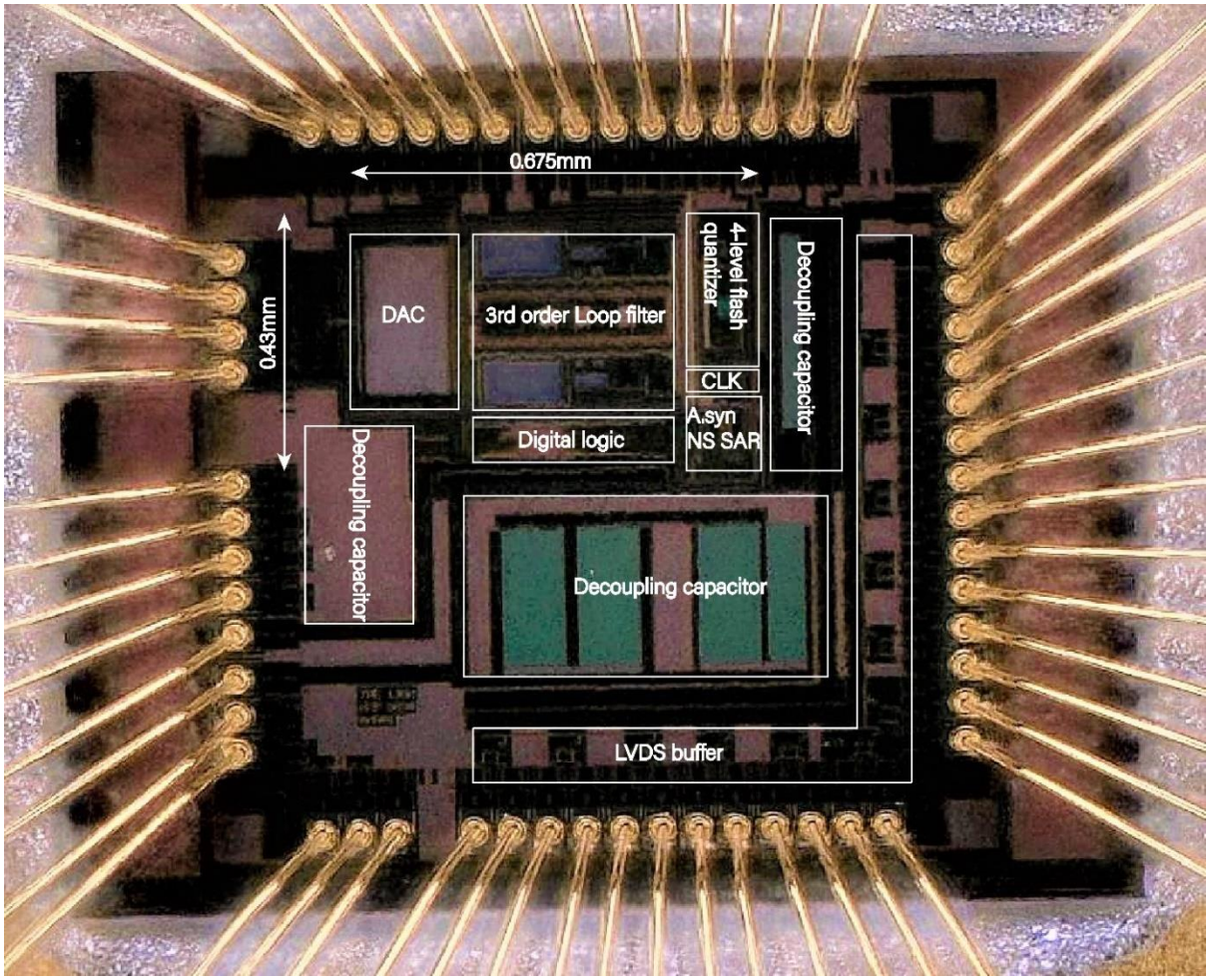


Figure 5.1: Chip micrograph of the prototype zoom ADC.

5.1 Measurement setup

The target of the measurement setup is to evaluate the performance of a high-linearity, high-resolution ADC. As shown in Figure 5.2, the PCB is separated into three supply and ground domains: analog, digital, and PC. Each supply/ground domain is powered by a different power supply to minimize the coupling effect.

The performance of the analog domain, which comprises the signal and reference paths, directly influences the performance of the ADC. Therefore, the PCB must be designed to achieve better performance than that of the ADC. The signal is generated by the audio precision analyzer (APx555) and its output is filtered and buffered before being entered to the ADC.

Similarly, the precision reference voltages are generated on the PCB, and fed to the ADC after being filtered and buffered. The requirements on the digital domain are relatively relaxed compared to those on the analog domain. The PCB should provide sufficient current to bias the low-voltage differential signaling (LVDS) buffers that drive the ADC. The requirements on the PC connection domain are the most relaxed. However, since the PCB and the PC are both connected to a data capturing block (DAQ), the ground bounce of the PC domain might couple to the digital ground on the PCB and degrade the measurement results. Therefore, an isolator is used to separate the digital ground of the PCB and the PC.

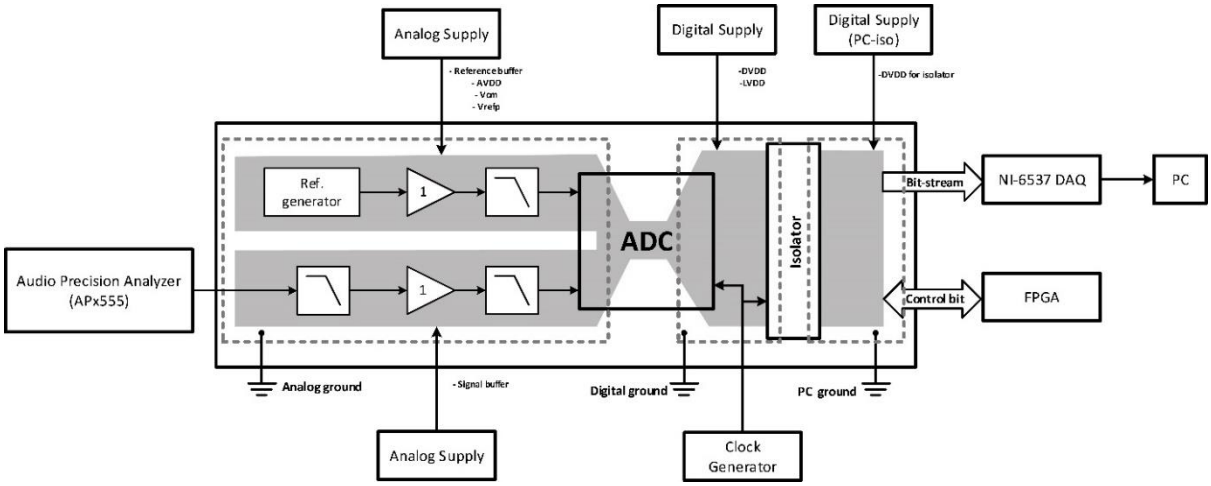


Figure 5.2: A simplified block diagram of measurement setup with star connection [1].

5.1.1 PCB layout

The signal routing is crucial in this mixed-signal PCB. The current return path should made as short as possible to avoid magnetic coupling [26]. A long current return path indicates a high ground impedance, which will increase the coupling between the different ground planes. A star-connection [1] is used to shorten the current return path, and the separated ground planes are connected in a small area located under the ADC.

The PCB employs a four-layer design. The signal tracks and component placements are placed on the top and the bottom layer, while the mid-layers are used for power and ground planes. This layout floorplan not only reduces the current return path but also minimizes coupling between different ground domains.

5.1.2 Signal generator, buffers and filter

The analog part of the ADC consists of the input signal and the reference signal as discussed in Section 5.1.1. The quality of the signal network should be better than our target specification (SNDR=108dB) for the ADC. The in-band integrated RMS noise of the prototype chip is calculated as $5.1\mu V_{rms}$ (SNR =108dB). In this discrete-time zoom ADC, the input and reference source might not be able to drive capacitive load and provide a sufficient settling and accuracy. Therefore, a buffer between the source signal and the ADC is required. The input is generated by an Audio Precision Analyzer and buffered by a low noise and high linearity buffer (OPA1611). The total integrated noise of OPA1611 is 156nVrms, which is considerably smaller than the noise floor of the zoom ADC. The same argument also holds for the reference

network. With the same noise contribution, the ADC performance will not be influenced by buffers in the signal network.

Wide-band white noise can fold-back and potentially increase the ADC's noise floor, so filters are required to limit the high-frequency noise of the signal generator. A 1st order RC low pass filter (LPF) is located at the output of the input and reference buffers to limit the noise bandwidth. However, the low bandwidth of the buffer will result in higher distortion due to the improper setting of the buffer. Hence, the trade-off should be considered between the noise folding and the linearity. Passive components are another potential source of non-linearity. Therefore, the RC filters were implemented with high-linearity components such as polypropylene dielectric capacitors and thin metal film resistors.

5.2 Measurement results

Table 5-1 lists the power breakdown of the zoom ADC with noise-shaping ON and OFF. The sampling rate is 2.5MS/s (OSR=62.5) and the zoom ADC with NS-SAR consumes 310 μW from a 1.8V supply. When the noise shaping mode of the SAR ADC is enabled, the power dissipation of the ADC increases to 316 μW from a 1.8V supply. The noise shaping function of the SAR ADC only consumes an extra 6 μW, which is less than 2% of the total power consumption of the ADC.

Table 5-1: Power breakdown

	NS-OFF	NS-ON
Power (Analog + reference) (μW)	191	192
Power (Digital) (μW)	119	124
Total power (μW)	310	316

5.3 Dynamic performance

5.3.1 NS-SAR ADC

Figure 5.3 shows the measured output spectrum of the coarse ADC with and without noise shaping function (with dithering disabled). The output spectrum shows a clear suppression of the in-band noise when the noise shaping is enabled. Tones are also shaped to a lower level as expected. The offset of the SAR ADC is also improved. Enabling the noise shaper improves the SNR, SNDR, and THD by about 7dB, 16dB, and 16dB, respectively.

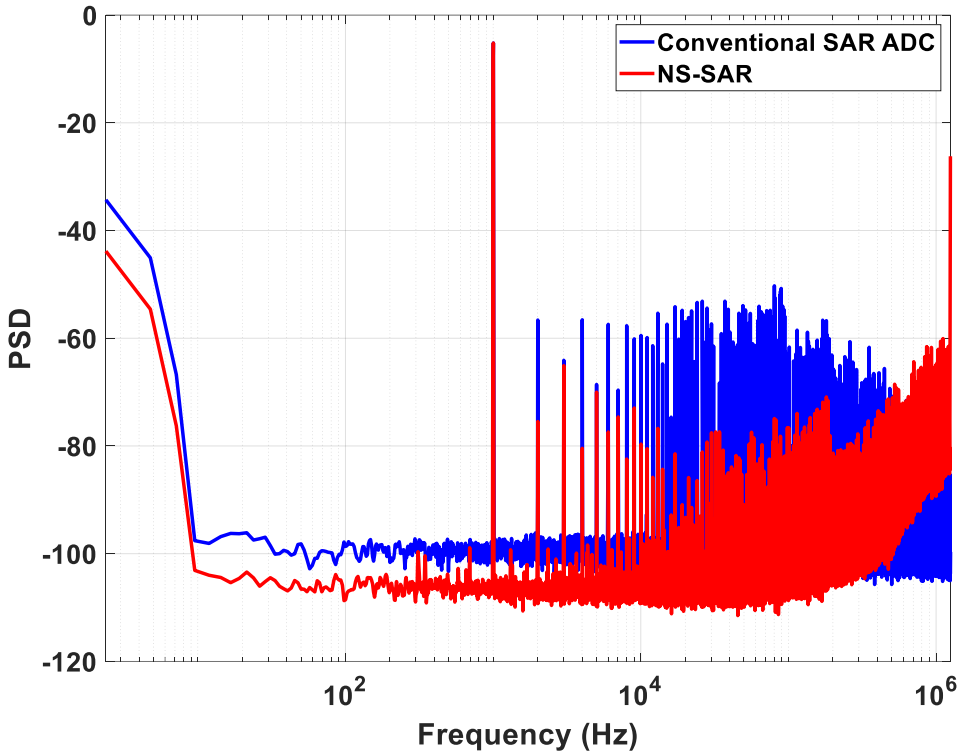


Figure 5.3: Measured SAR ADC output spectrum with noise shaping function enabled or disabled

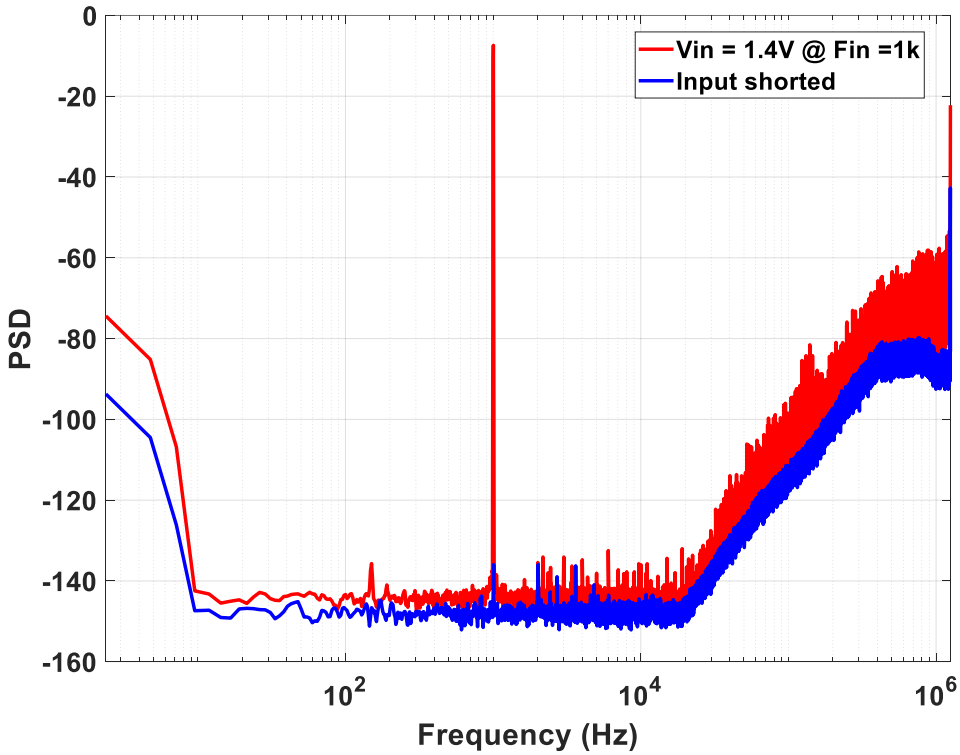


Figure 5.4: Measured zoom ADC output spectrum with peak SNDR and input shorted

5.3.2 Zoom ADC

Figure 5.4 shows the output spectrum of the zoom ADC with the NS-SAR on and with a full-scale input signal and with the ADC's input pins shorted together on the PCB. The corner frequency of the flicker noise is lower than 10Hz.

As shown in the Figure 5.5, by turning on the noise shaper of the SAR ADC, tones are greatly suppressed, the THD improves 5dB. However, more noise can be observed around the notch frequency of the DSM, which degrades the SNR of the zoom ADC. The reason is that the parasitic capacitor introduced by the layout causes aggressive toggling of the NS-SAR, and thus degrades the SQNR.

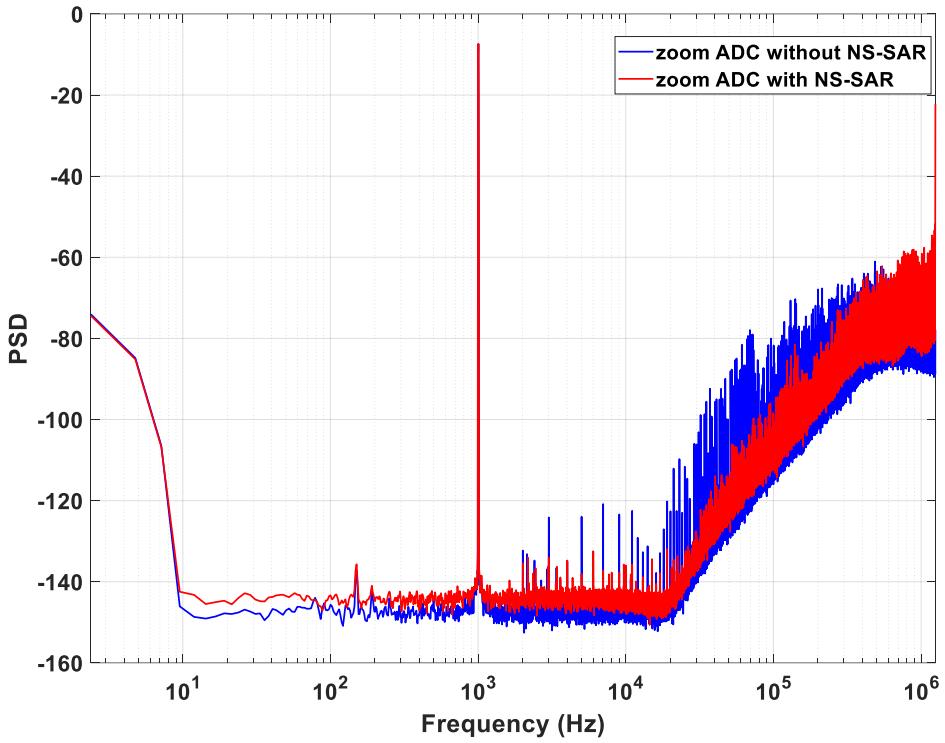


Figure 5.5: Measured zoom ADC output spectrum with noise shaping function enable/disabled

The measured output spectrum of the zoom ADC with dithering of the NS-SAR enabled is shown in Figure 5.6. The sampling rate is set to 2.5MHz. The SNR and SNDR increase by 0.7dB. The reason why the noise floor increases when dithering is enabled still needs to be investigated in the future. The measured peak DR, SNR and SNDR of the zoom ADC with NS-SAR are 106.5 dB, 104.4dB and 103.8dB respectively (see Figure 5.7).

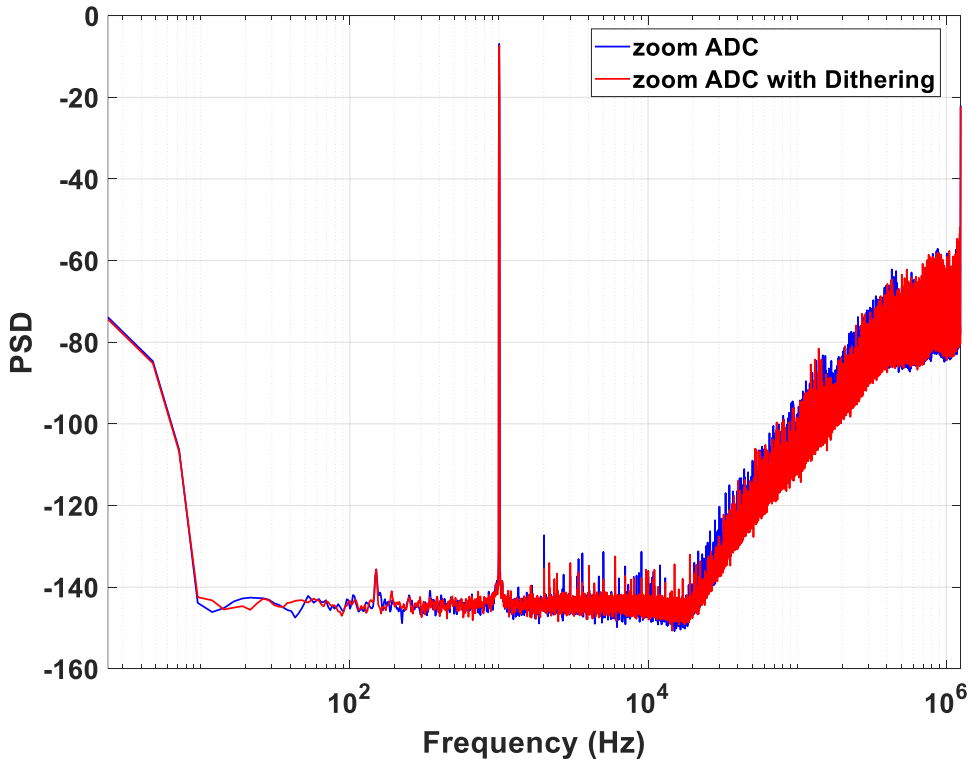


Figure 5.6: Measured output spectrum of the zoom ADC with dithering ON (red) and OFF (blue).

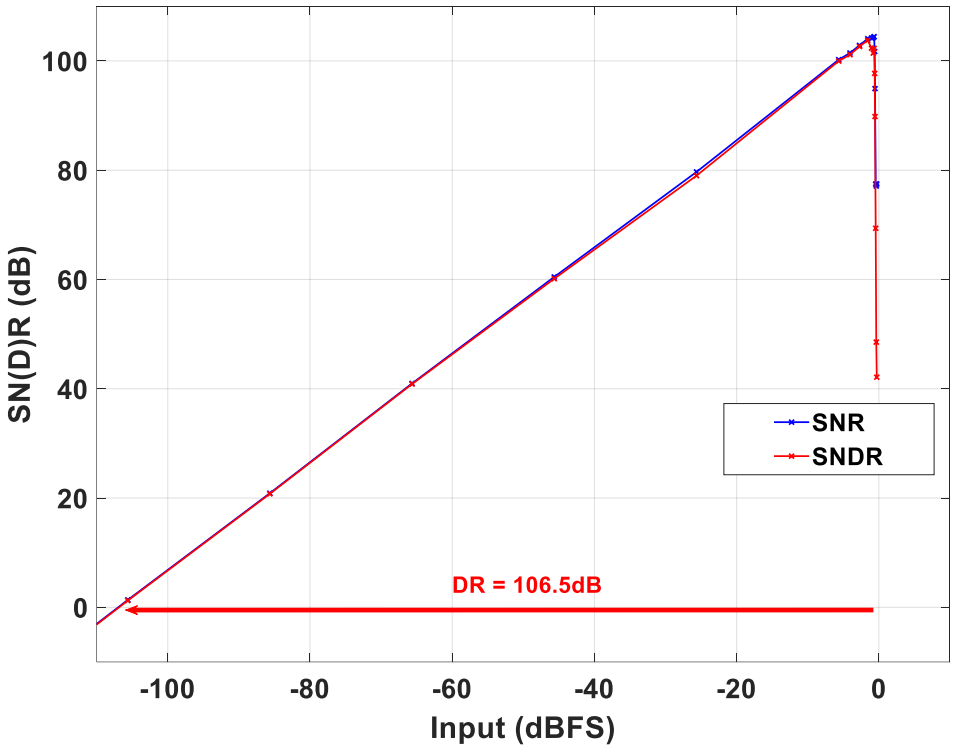


Figure 5.7: Measured DR/SNR/SNDR of the zoom ADC with NS-SAR across input signal magnitude.

Table 5-2 summarizes the performance of the zoom ADC with NS-SAR and compares it with that of state-of-the-art hybrid ADCs. This design is the first work that employs an NS-SAR as the coarse ADC of the zoom ADC architecture. The ADC achieves a 185dB FoM_S and a 182dB FoM_{SNDR}. The limitation of the FoM_S and FoM_{SNDR} is caused by the NS-SAR output codes switching beyond the pre-defined over-ranging, and limitations caused by the PCB. The SNR and SNDR can be further improved by optimizing the performance of the PCB.

Table 5-2: Performance summary and comparison with State-of-the-art hybrid ADCs

Specifications	This work	E.Eland [1]	S.Karmakar [2]	B. Gönen[27]	J.Liu [19]
Year	2020	2020	2018	2020	2020
Architecture	NS-SAR & DT-SD	SAR & DT-SD	SAR & DT-SD	SAR & CT-SD	NS-SAR
Technology [nm]	160	160	160	160	40
Active Area [mm^2]	0.29	0.27	0.25	0.27	0.061
Supply [V]	1.8	1.8	1.8	1.8	1.1
Power [μV]	317	440	280	618	67.4
Sampling rate [MS/s]	2.5	3.5	2	5.12	2
Bandwidth [kHz]	20	20	1	20	10
SNR_{peak}[dB]	104.4	107.5	119.1	108.1	96.1
$SNDR_{peak}$[dB]	103.8	106.5	118.1	106.4	95.3
DR [dB]	106.5	109.8	120.3	108.5	98.5
FoM_S* [dB]	185	186.4	185.8	183.6	180.2
FoM_{SNDR}** [dB]	182	183.1	183.6	181.5	177

FoM_S* = DR + 10log(BW/Power)

FoM_{SNDR}** = SNDR + 10log(BW/Power)

6 Conclusion & Future Work

6.1 Conclusion

This thesis demonstrates the feasibility of employing a NS-SAR ADC as the coarse ADC of an audio zoom ADC architecture.

With a low-cost, fully passive CIFF NS-SAR scheme, the proposed zoom ADC architecture improves the SNDR with a minimal modification to the original SAR ADC. The concept is verified by system-level simulation, and the resulting circuit is simulated at both schematic-level and after post-layout extraction. Finally, a high precision measurement setup was used to verify the prototype chip.

Measurement results support the expectation that employing a noise shaper in the SAR ADC can shape its quantization noise Q_{SAR} effectively out of band, thus solving the Q_{SAR} leakage issue in the zoom ADC. Although this tone suppression technique is promising, the prototype chip suffers from SNR loss after enabling the noise shaping function. Due to layout parasitics, the NS-SAR toggles more aggressively than expected, which leads to a larger DAC swing, that in turn, increases in the quantization noise of the zoom ADC.

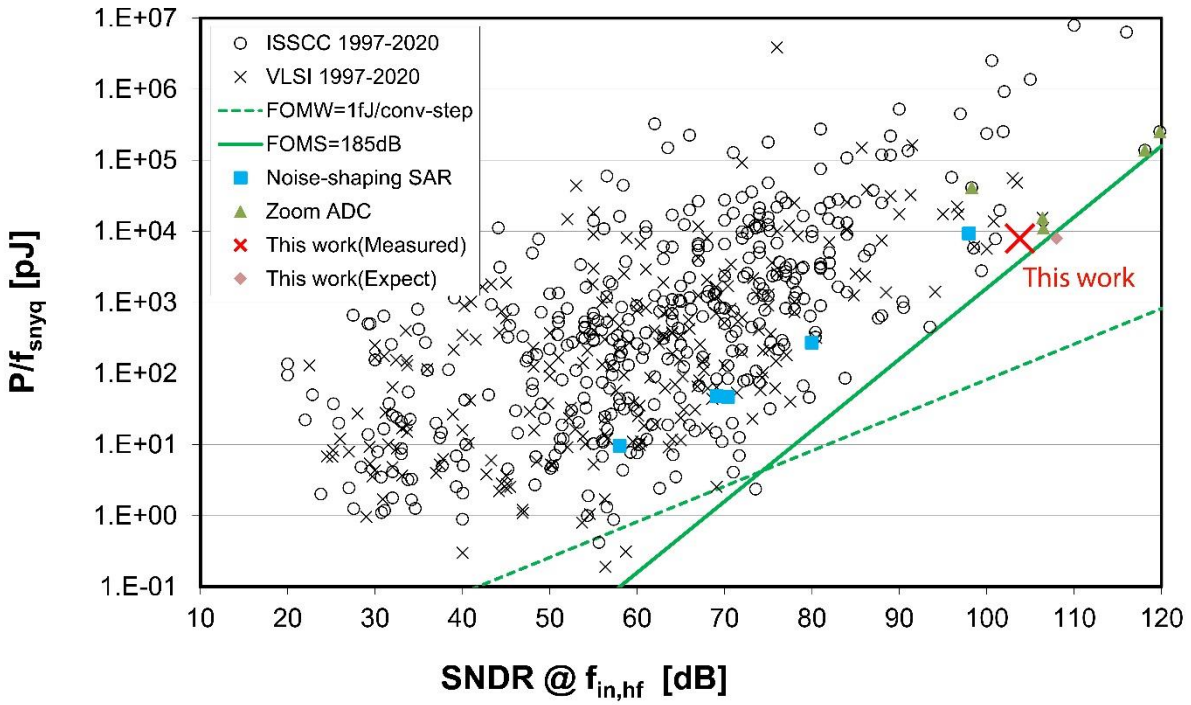


Figure 6.1: ADC survey on energy efficiency versus peak SNDR [5]

Figure 6.1 shows a survey of the energy efficiency vs. peak SNDR performance of published ADCs at VLSI and ISSCC. The green solid line represents an FoM of 185dB and represents the state-of-the-art ADC performance in recent years. As shown in the figure, this design is very close to the state-of-the-art FoM. By solving the limitations of the layout and the measurement setup, this design can be improved to approach the state-of-the-art work further.

6.2 Future work

This work has the potential to achieve state-of-the-art FoM and SNDR performance. However, the PCB board and chip layout of the NS-SAR limits the DR and SNR of this design. The PCB can still be improved by tuning parameters of the input filter and reference buffer with careful attention to the NS-SAR swing of the chip.

6.2.1 Linearized OTA

The analog circuits accounts for a great proportion of the power consumption of this zoom ADC. The main consumer is the 1st OTA because of its stringent linearity requirement. However, by using the newly developed tail-resistor-linearized OTA[28], similar linearity can be achieved with a significantly lower tail current.

6.2.2 Lower-bits NS-SAR

As discussed in chapter 3, the digital power consumption is proportional to the number of coarse ADC bits due to the logic needed for the DWA algorithm. Therefore, a lower resolution NS-SAR can be implemented in a future design to reduce the digital power consumption. The digital power consumption can be expressed as

$$P_{digital} = \mathrm{CV}^2 \cdot \mathrm{fs} \qquad 6.1$$

where C is the total capacitances, that processed by DWA algorithm, V is digital power supply, and fs is the sampling rate.

In the case of 4bits NS-SAR, the DWA logic will only need to handle half the elements, which will halve the digital power. Moreover, the parasitic capacitor will also halve. But the SQNR of the zoom ADC will also drops when the number of SAR ADC bits is decreased. This can be solved by increasing the sampling rate a bit, but the analog part will still have to burn more power to achieve the same performance, so it is not clear that the total power consumption of the ADC can be reduced by using this strategy.

6.2.3 Continuous-Time DSM

The thermal noise of the discrete-time delta-sigma modulator (DTDSM) is determined by the size of the sampling capacitors (k*T*/*C* noise). As a result, the switched-capacitor input network requires input buffers and reference buffers to deliver a high current, which compromises the energy efficiency of the total system. On the other hand, the input network of a continuous-time DSM (CTDSM) behaves like a simple resistor, which relaxes the buffer design. Since a previous work CTDSM used a higher fs (= 5.12M Hz) but still suffered from Q_{SAR} leakage [27], the use of a NS-SAR should enable comparable SQNR while using a much lower fs, which will also save the digital power.

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