2025 Conference on Lasers and Electro-Optics Europe & European Quantum Electronics Conference (CLEO/Europe-EQEC) | 979-8-3315-1252-1/25/$31.00 ©2025 IEEE | DOI: 10.1109/CLEO/EUROPE-EQEC65582.2025.11111507

Enabling micro transfer printable SNSPDs for fully integrated quantum photonic platforms

Linus Krämer
University of Heidelberg, KIP, Im Neuenheimer Feld 227, 69120 Heidelberg, Germany

R. Jaha[1], C. Graham-Scott[2], I. Luntadila Lufungula[3], L. Jin[4], S. Ferrari[1], W. Pernice[1]

1. University of Heidelberg, KIP, Im Neuenheimer Feld 227, 69120 Heidelberg, Germany
2. University of Münster, SoN, Busso-Peus-Str., 48149 Münster, Germany
3. Ghent University-imec, Technologiepark-Zwijnaarde 126, 9052 Ghent, Belgium
4. (previously at 1, now) Delft University of Technology, QuTech, Lorentzweg 1, 2628 CJ Delft, Netherlands

Micro-transfer printing (uTP) facilitates the integration of pre-characterized components from different substrates onto one common carrier die, enabling high-yield processes. Its highly parallel nature allows for exceptional throughput [1]. uTP has been successfully applied to III-V amplifiers, lasers [2], and quantum dot emitters [3], among others.

Our research focuses on fabricating transferrable devices containing waveguide-integrated superconducting nanowire single-photon detectors (SNSPDs) [4]. Thanks to their outstanding performance SNSPDs integrated on low-loss Silicon Nitride waveguides enable optical quantum computing [5] and quantum key distribution [6]. Transferring SNSPDs allows for precise on-demand detector placement while circumventing fabrication constraints that could compromise the quality of the superconducting film.

The fabrication process involves patterning nanowires, half-etched Si_3N_4 waveguides, and metal electrodes via electron beam lithography (EBL), followed by reactive ion etching (RIE), physical vapor deposition (PVD) or sputtering. To make the Si_3N_4 device freestanding and ready for transfer printing, the final step employs hydrofluoric acid etching to dissolve the SiO_2 layer (see Fig. 1a and b). Thereafter, a PDMS stamp is used to pick up the device, breaking its support structures and accurately place them on the dedicated carrier substrate.

Our photonic architecture is optimized for detecting photons at a 930 nm wavelength. For sacrificial test devices, grating couplers at both ends of the suspended structures facilitate integrity and functionality testing during fabrication, while metal contacts to the SNSPDs allow for electrical pretesting. This approach allows for a precise placement of pre-characterized waveguide-integrated SNSPDs on any substrate and thus the creation of hybrid architectures necessary for fully on-chip quantum photonic applications.

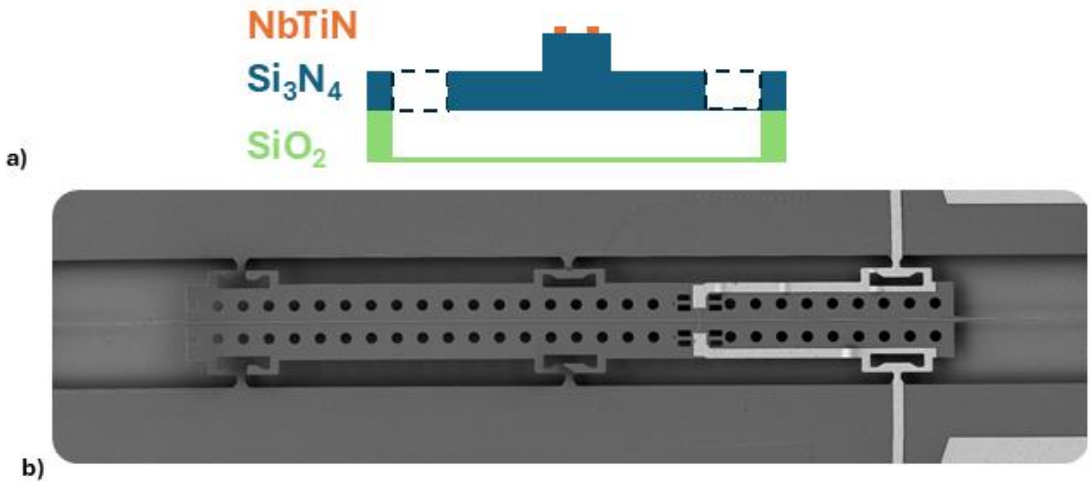

Fig. 1 a) Schematic sidecut view of a chiplet containing a waveguide integrated nanowire. b) SEM image of freestanding device.

Example References

[1] G. Roelkens et al., IEEE J. Select. Topics Quantum Electron., vol. 29, no. 3: Photon. Elec. Co-Inte. and Ad, pp. 1–14, 2023, doi: 10.1109/JSTQE.2022.3222686
[2] C. Op de Beeck et al., Optica, 7(5), 386-393, 2020, doi: 10.1364/OPTICA.382989
[3] R. Katsumi et al, in Yatsui, T. (eds) Progress in Nanophotonics 7. Topics in Applied Physics, vol 147 Springer, Cham, 2022, doi: 10.1007/978-3-031-16518-4_4
[4] S. Ferrari, Nanophotonics, vol. 7, no. 11, pp. 1725–1758, 2018, doi: 10.1515/nanoph-2018-0059
[5] J. O'brien, Optical quantum computing, Science, 318(5856), 1567-1570, 2007 doi: 10.1126/science.1142892
[6] J. P. Chen, Physical review letters, 124(7), 070501, 2020, doi: 10.1103/PhysRevLett.124.070501