Investigation of Pulse Current Capabilities of IGBTs and MOSFETs

By

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CONTENTS

ACKNOWLEDGEMENTS....................iii
LIST OF FIGURES....................viii
LIST OF TABLES....................x
ABSTRACT....................xii
1 INTRODUCTION....................1
1.1 RESEARCH OBJECTIVES....................2
1.2 THESIS STRUCTURE....................2
2 MOSFET....................4
2.1 MOSFET....................4
2.2 STRUCTURE....................4
2.3 WORKING PRINCIPLE....................5
2.4 MOSFET WORKING....................5
2.5 MOSFET SWITCHING....................8
2.6 MOSFET OPERATING LIMITATIONS....................11
3 TYPES OF MOSFET....................12
3.1 P-channel MOSFET....................12
3.2 N-channel MOSFET....................12
3.3 N-channel MOSFET vs P-channel MOSFET....................13
3.4 DEPLETION MOSFET....................13
3.5 ENHANCEMENT MOSFET....................14
3.6 E MOSFET vs D MOSFET....................14
3.7 SiC MOSFET....................14
3.8 SiC MOSFET vs Si MOSFET....................16
3.9 SUMMARY....................22
4 IGBT....................23
4.1 IGBT STRUCTURE....................23
4.2 IGBT WORKING....................24
4.3 IV CHARACTERISTICS....................25
4.4 IGBT LATCHUP....................25
4.5 IGBT SWITCHING....................27
4.6 IGBT LIMITATIONS....................28
5 TYPES OF IGBT....................29
5.1 PT-IGBT....................29
5.2 NPT-IGBT....................31
5.3 NPT-IGBT vs PT-IGBT....................32
5.4 SHORT CIRCUIT TEST....................33
5.5 TRENCH GATE FIELD-STOP IGBT....................34

6 OVERALL COMPARISON 37
6.1 OUTPUT CURRENT 37
6.2 LEAKAGE CURRENT 38
6.3 GATE CHARGE AND SWITCHING LOSSES 38
6.4 SWITCHING LOSSES 39
7 FACTORS AFFECTING DRAIN CURRENT 40
7.1 PULSE CURRENT TEST CIRCUIT 40
7.2 FACTORS AFFECTING PEAK DRAIN CURRENT ID 41
7.3 PEAK DRAIN CURRENT ID 45
7.4 FAILURE INVESTIGATION OF THE DEVICE 47
8 PULSE CURRENT TEST 49
8.1 SPICE MODEL OF DUT 49
8.2 PULSE CURRENT TEST SETUP 50
8.3 PULSE CURRENT TEST 53
9 CONCLUSION 61
9.1 RECOMMENDATIONS FOR FUTURE WORK 63
APPENDIX A 65
APPENDIX B 66
BIBLIOGRAPHY 77

LIST OF FIGURES

Figure 1-1 Structure of MMC [1] 1
Figure 1-2 Output voltage and Sub-Module current of MMC [1] 2
Figure 2-1 MOSFET symbol [2] 4
Figure 2-2 MOSFET Structure [2] 4
Figure 2-3 Transconductance $\boldsymbol{ID}$ vs $\boldsymbol{VGS}$ [2] 5
Figure 2-4 Formation of conduction channel [2] 5
Figure 2-5 MOSFET $\boldsymbol{VDS}$ vs $\boldsymbol{ID}$ [3] 6
Figure 2-6 Cut-Off region [6] 6
Figure 2-7 Ohmic region [6] 7
Figure 2-8 Quasi-Saturation region [6] 8
Figure 2-9 MOSFET Capacitances [3] 8
Figure 2-10 MOSFET Turn ON [3] 9
Figure 2-11 MOSFET Turn OFF [3] 10
Figure 3-1 P-channel MOSFET [7] 12
Figure 3-2 N-channel MOSFET [7] 12
Figure 3-3 Depletion MOSFET [7] 13
Figure 3-4 Enhancement MOSFET [7] 14
Figure 3-5 SiC MOSFET Structure [9] 14
Figure 3-6 Bandgap, Dielectric constant, Critical field strength comparison [10] 15
Figure 3-7 Advantages of SiC over Si [12] 16
Figure 3-8 $\boldsymbol{VDS}$ vs $\boldsymbol{ID}$ a Si MOSFET b SiC MOSFET [13] 16
Figure 3-9 a $\boldsymbol{RDS(on)}$ b $\boldsymbol{VGS}$ Si MOSFET vs SiC MOSFET [14] 17
Figure 3-10 Transconductance gfs a Si MOSFET b SIC MOSFET [14] 18
Figure 3-11 a Capacitances b Time delay Si vs SiC MOSFETs [14] 18
Figure 3-12 Switching transients a Si MOSFET b SiC MOSFET [14] 19
Figure 3-13 a Planar MOSFET b Trench MOSFET [15] 20
Figure 3-14 On-state Resistance $\boldsymbol{RDS(on)}$ Planar MOSFET vs Trench MOSFET [9] 20
Figure 3-15 SCWT a Planar MOSFET b Trench MOSFET [16] 21
Figure 3-16 Electric field distribution a Planar MOSFET b Trench MOSFET [16] 21
Figure 3-17 Flowchart - Types of MOSFET 22
Figure 4-1 IGBT Symbol [2] 23
Figure 4-2 Structure of IGBT [2] 23
Figure 4-3 Effective MOSFET and BJT portions [2] 24
Figure 4-4 a IGBT Equivalent circuit b Parasitic Elements of IGBT [2] 24
Figure 4-5 Conduction in IGBT [2] 24
Figure 4-6 IGBT IV Characteristics [2] 25
Figure 4-7 Equivalent circuit during IGBT conduction [3] 26
Figure 4-8 IGBT turn-on waveforms [2] 27
Figure 4-9 IGBT Turn-off waveforms [2] 27
Figure 5-1 PT-IGBT structure [3] 29
Figure 5-2 NPT-IGBT structure [3] 31
Figure 5-3 $\boldsymbol{VCE(sat)}$ NPT-IGBT vs PT-IGBT [17] 32
Figure 5-4 Switching Losses a Eon & b Eoff NPT-IGBT vs PT-IGBT [17] 33
Figure 5-5 Non-destructive Short circuit test PT vs NPT-IGBT [18] 33
Figure 5-6 Structure of Trench Field-Stop IGBT [19] 34

Figure 5-7 $\mathbf{p}+$ layer thickness optimization [20] 34
Figure 5-8 n-buffer layer thickness optimisation [20] 35
Figure 5-9 Flowchart - Types of IGBT 36
Figure 6-1 Output characteristics comparison [21] 37
Figure 6-2 Leakage current comparison [21] 38
Figure 6-3 Gate charge and Gate Energy comparison [21] 38
Figure 6-4 Switching Losses comparison [21] 39
Figure 7-1 Pulse current test circuit 40
Figure 7-2 $\boldsymbol{ID}$ for different $\boldsymbol{VGS}$; $\boldsymbol{VDS}$ = 800 V; $\boldsymbol{RG}$= 11 $\boldsymbol{ton}$ = 5 μ sec [23] 42
Figure 7-3 Resistances $\boldsymbol{RG}$' and $\boldsymbol{RG}$ in Gate circuit [23] 43
Figure 7-4 $\boldsymbol{ID}$ and $\boldsymbol{VDS}$ for different $\boldsymbol{RG}$ [23] 43
Figure 7-5 $\boldsymbol{VDS}$ vs $\boldsymbol{ID}$ for a constant $\boldsymbol{VGS}$ = 20 V $\boldsymbol{ton}$ = 4 μ sec [23] 44
Figure 7-6 Current and voltage waveforms for critical energy $\boldsymbol{Ecr}$ calculation at $\boldsymbol{VDS}$ = 800 V and $\boldsymbol{VGS}$ = 20 V [23] 45
Figure 7-7 Safe Operating Area of SiC MOSFET [23] 46
Figure 7-8 SiC MOSFET Failure investigation [23] 47
Figure 7-9 Energy band diagram SiC-$\boldsymbol{SO2}$ interface [10] 48
Figure 8-1 Pspice model of SiC MOSFET 49
Figure 8-2 Power Board of the Pulse Current test circuit 50
Figure 8-3 Gate Driver 51
Figure 8-4 Pulse Current Test circuit schematics 52
Figure 8-5 $\boldsymbol{VDS}$ Test – Simulation 53
Figure 8-6 $\boldsymbol{VDS}$ Test - Experimental results 55
Figure 8-7 $\boldsymbol{VGS}$ Test - Experimental results 56
Figure 8-8 Pulse Current comparison IGBT vs MOSFET 58
Figure 8-9 Pulse current comparison - IXGH24N170 vs IXBH20N300 59
Figure 8-10 Pulse Current Test of SiC MOSFET vs Trench Gate FS IGBT 60

Appendix A

Figure A-1 Pulse Current Test circuit 65

Appendix B

Figure B-1 Oscilloscope image VDS Test (C2M0160120D) 66
Figure B-2 Oscilloscope image VGS Test (C2M0160120D) 67
Figure B-3 SiC MOSFET - C3M0075120D 68
Figure B-4 SiC MOSFET - C3M0080120D 69
Figure B-5 Si CoolMOS - IPW90R120C3 70
Figure B-6 NPT IGBT – SGW25N120 71
Figure B-7 NPT-IGBT IXGH24N170 72
Figure B-8 NPT-IGBT IXBH20N300 73
Figure B-9 SiC MOSFET – C3M0016120D 74
Figure B-10 - TRENCH GATE FS IGBT - IHW40N120R5 75

LIST OF TABLES

Table 3-1 Electrical and Thermal properties of 4H-SiC vs Si [11] _______ 15
Table 8-1 SiC MOSFET used in simulation _______ 49
Table 8-2 Power Electronic devices used for Pulse Current Test _______ 52
Table 8-4 Statistical results $\boldsymbol{VGS}$ *constant, increasing* $\boldsymbol{VDS}$ _______ 55
Table 8-3 Statistical results $\boldsymbol{VDS}$ *constant, increasing* $\boldsymbol{VGS}$ _______ 57

ABSTRACT

TU Delft and KEMA laboratories are collaborating to create a Programmable high voltage test source by employing Modular Multilevel Converter MMC which can generate output voltage waveforms of any arbitrary shape. To produce an Impulse waveform of magnitude 250 kV across a capacitive load of 10 nF with a rise time of 1.2 μs as output voltage, each Power Electronic device incorporated into each Sub-Module of the MMC has to conduct pulse currents as high as 850 Amperes. Moreover, the Impulse Waveform has a very short time duration. Hence the Power Electronic devices need to conduct such high current magnitude only for a very short duration of time. This motivates this Master thesis to find out how many multiples of its rated current a Power Electronic device is able to conduct within such short time and what factor limits the peak current capability of the Power Electronic device. However, to produce an output voltage of any other waveshape each Power Electronic device of each Sub-Module of the MMC has to conduct only a few amperes of continuous current. Employing Power Electronic devices of current rating as high as pulse currents of Impulse waveform is not only uneconomical since other waveforms do not require such high continuous currents, but also such Power Electronic devices of high current rating would make the MMC bulkier.

To identify the Power Electronic device technology that is capable of conducting such high pulse currents, a literature review is conducted among IGBT, MOSFET and their types. Each device of IGBT and MOSFET is compared to one another. Finally, the most promising switching technology is chosen among MOSFET and IGBT based on three criteria namely, high peak current capability, high voltage blocking capability and high switching frequency.

A prototype of Pulse Current Test circuit is built to test the peak pulse current of the chosen switching technology. Then, the factors that can be utilized to achieve the peak pulse current are identified. Based on results of the pulse current test, the multiplication factor of the rated current of the Power Electronic device is identified. Switch technology for the MMC specifically for Impulse waveform is suggested.

1
INTRODUCTION

TU Delft and KEMA laboratories are collaborating to create a Programmable High Voltage test source by using Modular Multilevel Converter (MMC) as shown in **Figure 1-1**. The Programmable High Voltage Test Source is able to produce Output Voltage waveforms of various arbitrary shapes which also includes Impulse waveform.

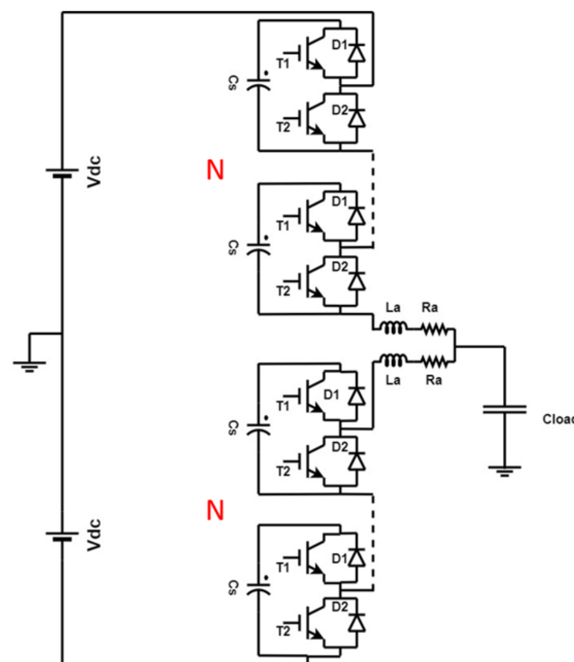

Figure 1-1 Structure of MMC [1]

Modular Multilevel Converter (MMC) has N Sub-Modules and each Sub-Module has two Power Electronic Devices and a Sub-Module capacitance C_s. To produce an Impulse waveform of magnitude 250 kV with a rise time t_r of 1.2 μs across the load capacitance C_{load} of the Modular Multilevel Converter (MMC), each Power Electronic device of every Sub-Module has to endure pulse currents of peak magnitude of the order of several hundred amperes for short pulse durations as shown in **Figure 1-2**. However, the Modular Multilevel Converter (MMC) does not demand such high switching currents to produce output voltages for other waveforms such as Sine, Cosine, Rectangular or Triangular.

Power Electronic devices of nominal current ratings as high as almost 1 kA is bulky and costly. Since, only the Impulse waveform demands very high switching currents, it is not economical to use such high I_{rated} Power Electronic switches to produce other waveforms that do not demand currents as high as Impulse waveform.

Generally, the datasheets of Power Electronic devices recognize Pulse Currents as high as only 2 times the Nominal rated current I_{rated}. Especially, for very short durations such as 1.2 μs, the applicable Pulse current rating is not mentioned.

Hence, this master thesis aims to explore the possibility of using Power Electronic devices of lower continuous current rating to achieve higher pulse currents of magnitude N x I_{rated} (Pulse current capability) for such short durations, by applying repetitive short current pulses and studying the performance, until the peak Pulse current of the device is achieved.

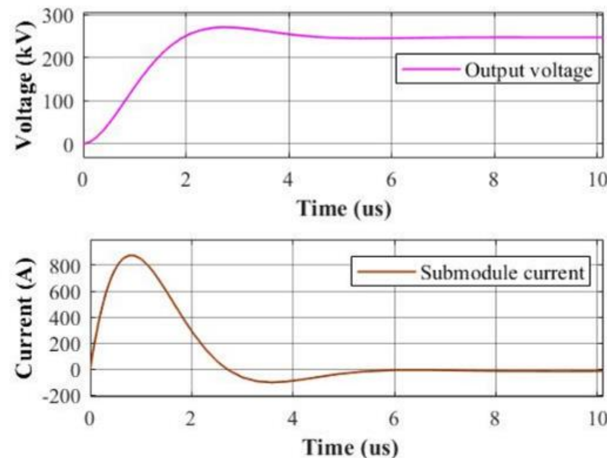

Figure 1-2 Output voltage and Sub-Module current of MMC [1]

1.1 RESEARCH OBJECTIVES

This thesis aims to explore various Power Switching semiconductor technologies and their Pulse Current capabilities to answer the following research questions:

1. Study the most promising Power Electronic device to achieve the highest multiple of its rated current.
2. What are the Parameters that determine the peak current obtained through a Power Electronic device?
3. How to verify practically the highest peak pulse current derived from theoretical understanding?

1.2 THESIS STRUCTURE

This thesis is comprised of following chapters:

Chapters from 2 to 6 form the literature review of the thesis. A significant amount of literature has been studied to summarise and serve as a guide to choose Power Electronic devices that could reach high pulse current capabilities. Chapter 7 provides adequate information on how to reach the peak pulse current capabilities. Chapter 8 elaborates on results from various Pulse current tests that were performed in the laboratory.

CHAPTER 2 describes structure of MOSFET in detail, its working principle, regions of operation, switching waveforms and limitations.

CHAPTER 3 lists out various types and characteristic features of MOSFET such as P-channel MOSFET, N-channel MOSFET, Enhancement MOSFET, Depletion MOSFET, Si MOSFET, SiC

MOSFET, Planar MOSFET and Trench MOSFET. Moreover, this chapter compares each type of MOSFET to one another to pick the most promising type of MOSFET that could deliver highest drain current, voltage blocking capability, and switching frequency.

CHAPTER 4 describes IGBT structure, its working, IV characteristics, IGBT latch up, switching waveforms and its limitations.

CHAPTER 5 compares various types of IGBT technologies such as Punch-Through IGBT, Non-Punch Through IGBT and Trench Gate Field-Stop IGBT. Finally, the most promising switching technology among types of IGBT is identified that has potential to deliver highest collector current, switching frequency and almost zero current tailing.

CHAPTER 6 performs an overall comparison of all Power Electronic devices together based on output current, leakage current, gate charge required to create conduction channel and switching losses.

CHAPTER 7 discerns the pulse current test circuit and lists out various factors of the switch that affect peak pulse current of the Power Electronic Device. Moreover, the critical energy that the semiconductor device can conduct before it fails and failure mechanism are clearly explained.

CHAPTER 8 explains the elements that make the Pulse Current Test setup are listed and procedure to build the Test setup is discussed. P-spice simulations and experimental results of both V_{GS} and V_{DS} tests are discussed. Based on results of these two tests, all the Power Electronic devices chosen are subjected to Pulse Current Tests. Finally, the switching technology among all types of MOSFET and IGBT that could deliver highest pulse current capability is determined by subjecting all types of IGBT and MOSFET to Pulse current test.

CHAPTER 9 summarises all the important research findings from this thesis. Research questions are answered and possible future work is discussed.

2

MOSFET

2.1 MOSFET

Metal oxide semiconductor field effect transistor is a power electronic semiconductor device which is used for high-frequency switching applications [3] where the switching frequency is usually in several kilohertz. MOSFET is a three-terminal device. The terminals are namely Gate, Source and Drain. The terminals are represented in the symbol of MOSFET from **Figure 2-1** [2].

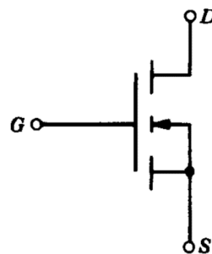

Figure 2-1 MOSFET symbol [2]

2.2 STRUCTURE

The structure of MOSFET is represented in **Figure 2-2**. A thin Gate oxide layer is formed over a p-substrate (p body region), on top of which metallic Gate terminal is placed. Two separate heavily doped n^+ layers are formed in the p-substrate below the Source terminal. Since there is no physical connection between the two n^+ regions and n^- drift region, a channel of free electrons has to be created beneath the oxide layer for the drain current i_D to flow from Drain to Source terminals. The channel in p body region has length L separated by n^+ region and n^- drift region. The MOSFET has a parasitic npn BJT which is maintained in cut-off region by body-source short. The integral diode is the body diode of the MOSFET which helps MOSFET to conduct during 3rd quadrant operations. This configuration of MOSFET is called as the N channel enhancement MOSFET and N channel represents formation of channel made of electrons [2].

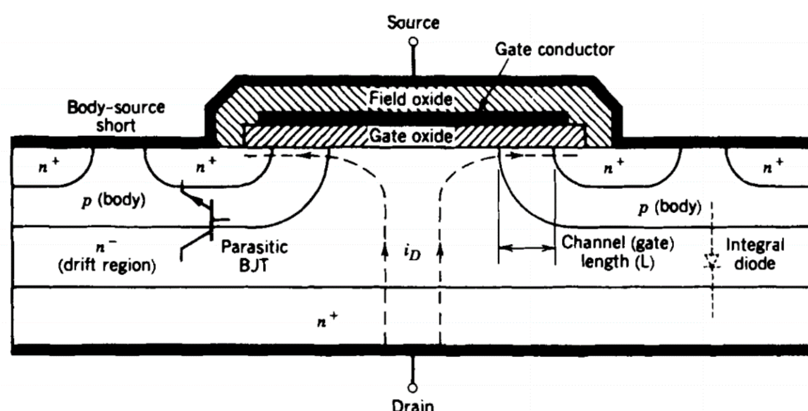

Figure 2-2 MOSFET Structure [2]

2.3 WORKING PRINCIPLE

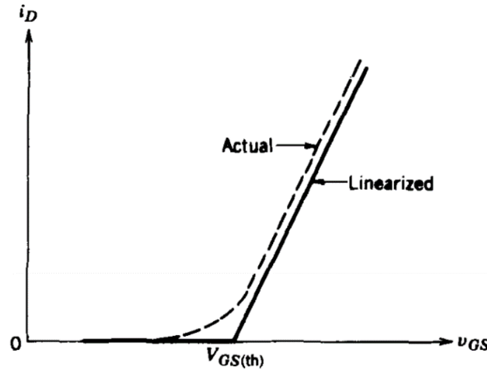

Figure 2-3 Transconductance I_D vs V_{GS} [2]

MOSFET works by the principle of Field Effect. When a positive voltage greater than Gate-Source Threshold voltage $V_{GS} > V_{GS(th)}$ as shown in **Figure 2-3** [2] is applied across the Gate and Source terminals, holes in the p-region experience a repulsive force and they moved away from the oxide region. As a result, the electrons are attracted to the surface of the silicon oxide forming a channel of electrons between heavily doped n^+ region and n^- drift region called as the inversion layer or conduction channel [5] represented by **Figure 2-4** [4].

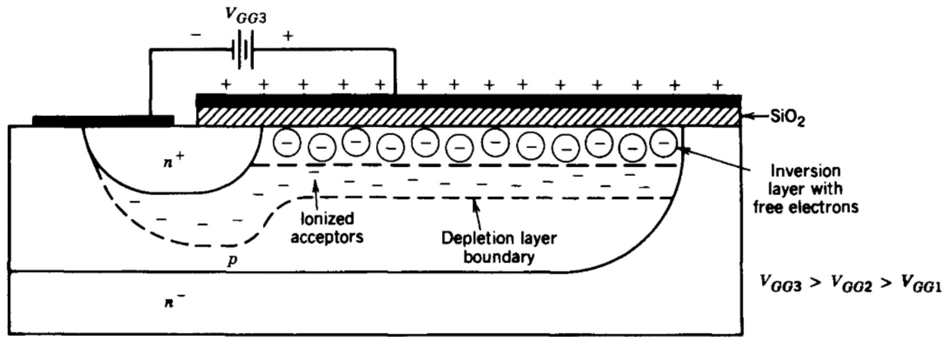

Figure 2-4 Formation of conduction channel [2]

As a result, this allows a current to flow from Drain to Source terminals called the Drain current $\boldsymbol{I_D}$. As a result, a layer is formed below the inversion layer which is devoid of mobile electrons called as the depletion layer. This layer contributes to the on-state voltage drop of the device during conduction [5].

2.4 MOSFET WORKING

MOSFET works in three states, namely,

1. Cut-off region
2. Ohmic region
3. Saturation region

The Drain Source Voltage $\boldsymbol{V_{DS}}$ vs Drain current $\boldsymbol{I_D}$ characteristics representing the operating states of MOSFET is shown in **Figure 2-5**.

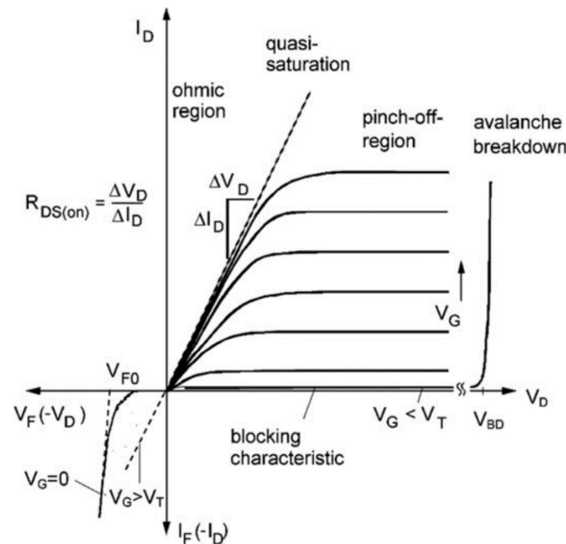

Figure 2-5 MOSFET V_{DS} vs I_D [3]

2.4.1 CUT-OFF REGION or BLOCKING STATE

When the applied Gate-Source Voltage V_{GS} is less than the Gate Threshold Voltage $V_{GS(th)}$ ($V_{GS} < V_{GS(th)}$), there is no conduction channel of electrons formed below Gate oxide layer, between Drain and Source terminals [3]. Hence there is no Drain current I_D flowing through the MOSFET, meaning MOSFET is in cut-off region or forward blocking state. MOSFET in cut-off region is represented in **Figure 2-6**.

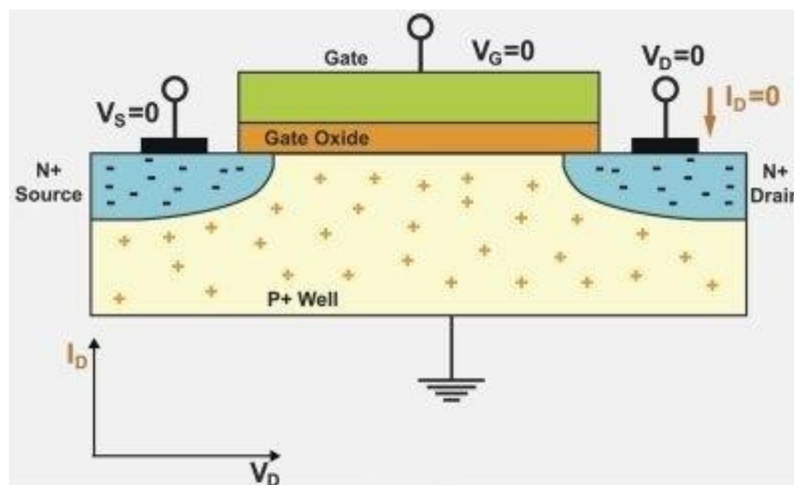

Figure 2-6 Cut-Off region [6]

2.4.2 OHMIC REGION

When $V_{GS} > V_{GS(th)}$ and applied V_{DS} is small, MOSFET is in Ohmic region (linear). A conduction channel is formed below the Gate oxide layer, between Drain and Source terminals. This conduction layer acts as purely resistive layer and hence the state of MOSFET is called Ohmic state [3]. A thin depletion region or space-charge region is formed below the conduction channel as a result of application of small V_{DS} shown in **Figure 2-7**.

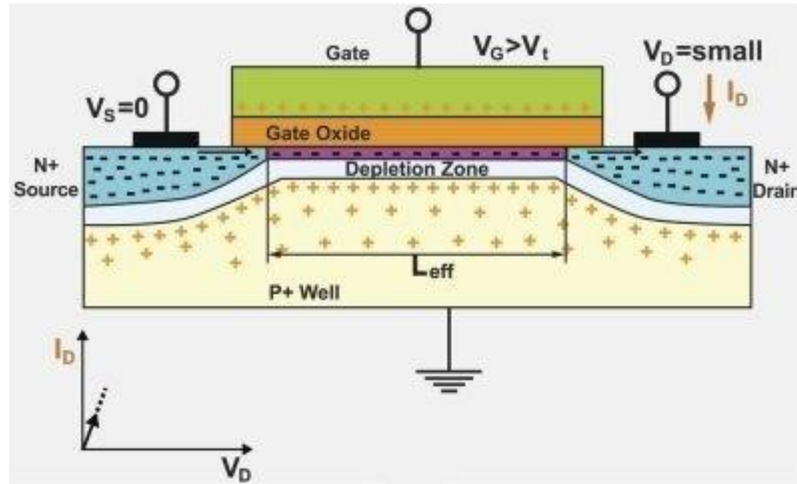

Figure 2-7 Ohmic region [6]

Resistance of the inversion layer is given by

$$R_{ch} = \frac{L}{W \mu_n Q_s} \quad \text{Equation (2.1)}$$

Where,

L is the length of the inversion layer

W is the width of the inversion layer

Q_s is the charge across the inversion layer

μ_n is the mobility of electrons

Since Inversion layer acts as a resistor in Ohmic region, drain current I_D rises linearly with V_{DS} through the MOSFET obeying $R_{DS(on)} = \frac{\Delta V_{DS}}{\Delta I_D}$. Drain current I_D in Ohmic region is given as

$$I_D = \frac{W \mu_n C_{ox}}{L} (V_{GS} - V_T) V_{DS} \quad \text{Equation (2.2)}$$

2.4.3 QUASI-SATURATION REGION

When $V_{GS} > V_{GS(th)}$ and $V_{DS} = V_{Dsat}$, the inversion layer of the MOSFET pinches-off represented by Figure 2-8 [3]. While the potential of Drain terminal increases equal to the potential of the Gate terminal and when the Source terminal is at lower potential, the electric field created between Drain and Source terminals sweeps away free electrons of the conduction channel formed by field effect. Hence the thickness of the conduction channel pinches-off near the Drain terminal. This process is called as pinch-off in MOSFET. As a result of increased Drain potential, the thickness of the depletion region under the conduction channel increases significantly. The extent of thickness of the depletion region determines voltage blocking capability of the MOSFET during cut-off state.

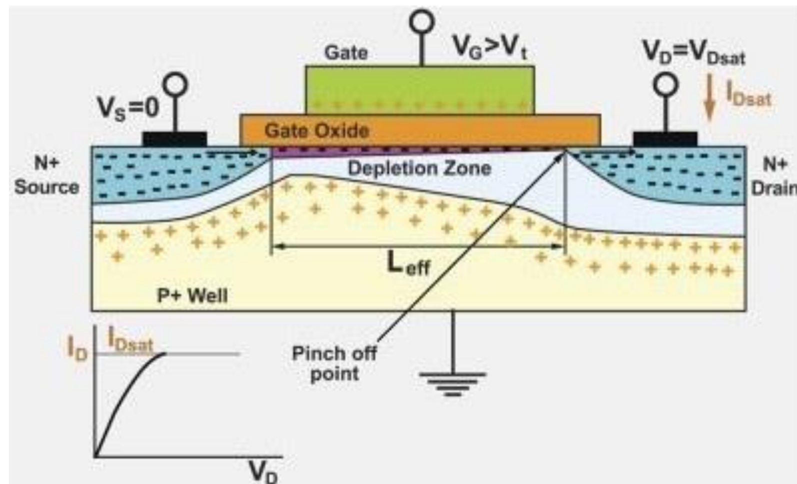

Figure 2-8 Quasi-Saturation region [6]

The channel resistance R_{ch} increases significantly as the width of the channel pinches-off. From this point the Drain current I_D attains saturation $I_{D,sat}$ and does not vary linearity with respect to Drain Source Voltage V_{DS} anymore.

Drain current I_D in Saturation region is given as

$$I_D = \frac{W\, \mu_n\, C_{ox}}{L} (V_{GS} - V_T)^2 \quad \text{Equation (2.3)}$$

2.5 MOSFET SWITCHING

MOSFET is either switched ON or switched OFF by either charging or discharging its intrinsic capacitances. The MOSFET capacitances are namely Gate Drain Capacitance C_{GD} or Miller Capacitance, Drain Source Capacitance C_{DS} and Gate Source Capacitance C_{GS} as shown by **Figure 2-9** [2].

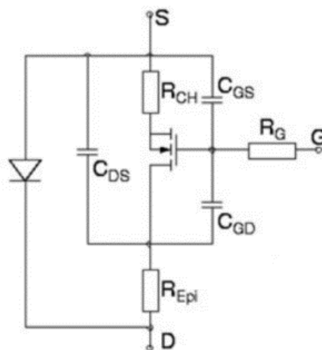

Figure 2-9 MOSFET Capacitances [3]

2.5.1 TURN-ON

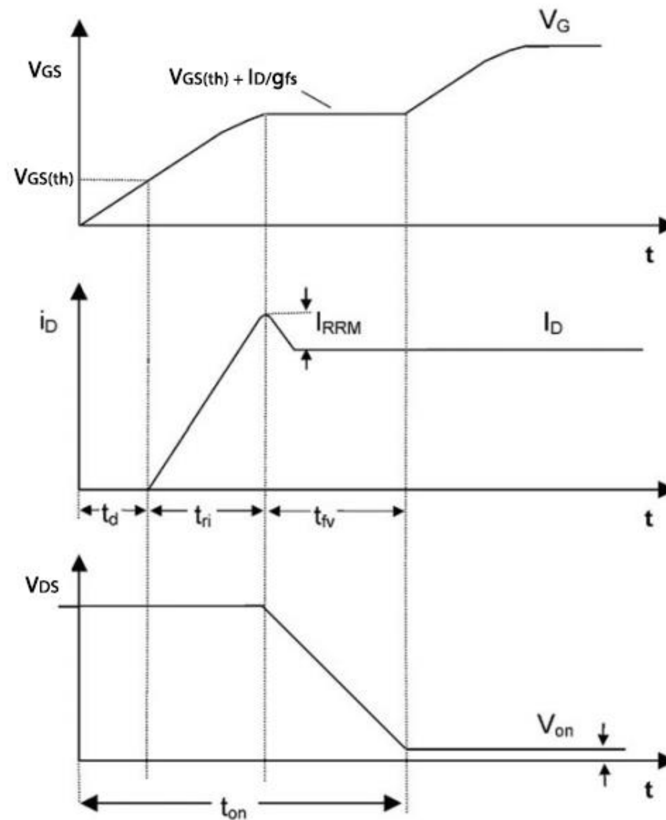

Figure 2-10 MOSFET Turn ON [3]

The turn ON characteristics of MOSFET is represented by **Figure 2-10**. It has three important timelines, the on-time delay $\boldsymbol{t_d}$, the Drain current rise time $\boldsymbol{t_{ri}}$ and the Drain Source voltage fall time $\boldsymbol{t_{fv}}$. During t_d MOSFET is in cut-off region, V_{GS} increases from zero to $V_{GS(th)}$ with a time constant τ $= R_G\ (C_{GD} + C_{GS})$ as gate current i_g flows through capacitances C_{GD} and C_{GS}. There is no conduction channel formed for Drain current i_D to flow and Drain Source voltage is at forward blocking voltage V_{DS} [3].

During t_{ri} MOSFET enters linear region as i_D increases linearly from zero to I_D+I_{RRM} when V_{GS} crosses $V_{GS(th)}$. I_{RRM} represents the reverse recovery current of the body diode as a result of inductive load. The Drain Source Voltage V_{DS} remains constant during this time interval [3].

During t_{fv} voltage across MOSFET falls to very low value V_{on} = $R_{DS(on)}\ I_D$. V_{GS} reaches a value $V_{GS(th)}$ + I_D/g_{fs} called Miller Plateau as C_{GD} is charged with time constant τ = $R_G\ C_{GD}$ where g_{fs} transconductance of MOSFET [3].

2.5.2 TURN-OFF

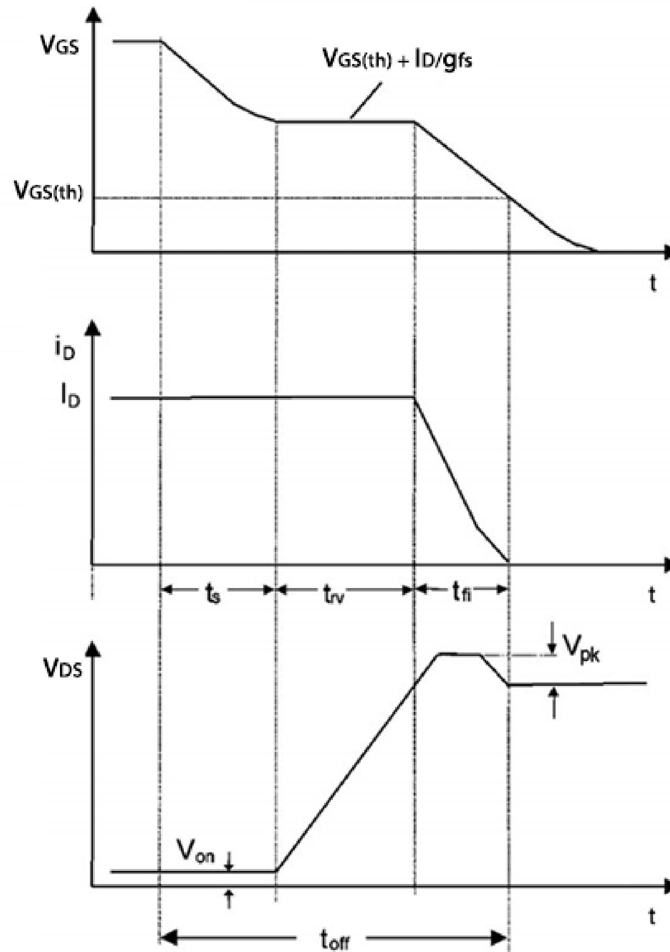

Figure 2-11 MOSFET Turn OFF [3]

Figure 2-11 shows the Turn OFF waveforms of the MOSFET and it is the exact inverse of the Turn ON waveforms of MOSFET. The turn OFF characteristics of MOSFET has three important timelines, the storage time $\boldsymbol{t_s}$, the voltage rise time $\boldsymbol{t_{rv}}$ and the current fall time $\boldsymbol{t_{fi}}$ [3]. During t_s charges present in C_{GD} & C_{GS} discharge at τ = $R_G\ (C_{GD} + C_{GS})$ as V_{GS} decreases to Miller Plateau $V_{GS(th)} + I_D/g_{fs}$.

During t_{rv} V_{GS} continues to remain in Miller Plateau while V_{DS} rises to its forward blocking voltage with a time constant τ = $R_G\ C_{GD}$ while Drain current I_D remains constant.

During t_{fi} gate capacitances C_{GD} & C_{GS} discharge as V_{GS} decreases from Miller Plateau to $V_{GS(th)}$ with time constant τ = $R_G\ (C_{GD} + C_{GS})$. As a result, the drain current I_D falls to zero. During this time interval, Drain Source voltage V_{DS} experiences an overshoot V_{pk} which has two reasons. The first reason is because of dI_D/dt inducing voltage drop across parasitic inductance of the MOSFET and the second reason is due to dynamic forward voltage V_{FRM} of the body diode.

Hence, $V_{pk} = L_{par}\frac{dI_D}{dt} + V_{FRM}$

2.6 MOSFET OPERATING LIMITATIONS

2.6.1 BREAKDOWN VOLTAGES

In MOSFET, V_{GS} and V_{DS} should not exceed $V_{GS(max)}$ and V_{BD} from **Figure 2-5** respectively [2]. If V_{GS} exceeds $V_{GS(max)}$ the gate oxide is broken down because of excessive electric field across the SiO_2 layer [2]. If V_{DS} exceeds V_{BD} the p-n junction of Drain-Body regions break down because of excessive electric field and goes into avalanche breakdown [2].

2.6.2 PARASITIC BJT

MOSFET has a parasitic BJT, since Drain of the MOSFET behaves as Collector, body region as base and Source as emitter of the BJT from **Figure 2-2** [2]. In order to keep this parasitic BJT at cut-off region, the body and source regions are shorted [2]. Since the base region of this BJT is connected through a Gate Drain capacitance C_{GD} to the Drain of the MOSFET, during fast turn-off of the MOSFET, a high $\frac{dv_{DS}}{dt}$ across Collector and Emitter terminals of the BJT will make it forward biased and the displacement current through the Base of the BJT are enough to turn ON the BJT [2]. This can be avoided by preferring lower switching speed and higher value of Gate resistance R_g [2].

3

TYPES OF MOSFET

Based on the type of charge carriers used for conduction, MOSFET can be classified into two types, they are namely

1. P-channel MOSFET
2. N-channel MOSFET

3.1 P-channel MOSFET

In P-channel MOSFET, the substrate material is n-type on which two heavily doped p^{+}regions are diffused. When a negative V_{GS} is applied, the electrons are repelled away from the Gate terminal attracting a channel of holes (minority charge carriers) between Drain and Source terminals as shown in the **Figure 3-1** [7]. Hence the Drain current I_D flows through a channel of holes. Hence the MOSFET is called as P-channel MOSFET [7].

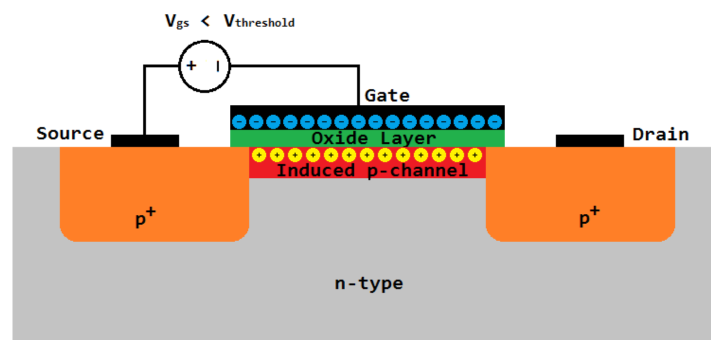

Figure 3-1 P-channel MOSFET [7]

3.2 N-channel MOSFET

When a positive $\boldsymbol{V_{GS}}$ is applied, the holes are repelled away from the Gate terminal attracting a channel of electrons (minority charge carriers) between Drain and Source terminals as shown in the **Figure 3-2** [7]. Hence the **Drain current $\boldsymbol{I_D}$** flows through a channel of electrons. Hence the MOSFET is called as N-channel MOSFET [7].

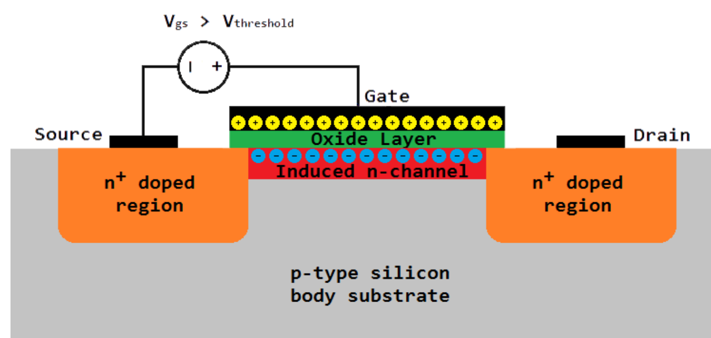

Figure 3-2 N-channel MOSFET [7]

3.3 N-channel MOSFET vs P-channel MOSFET

N-channel MOSFET is preferred over P-channel MOSFET since the mobility of electrons μ_n is greater than the mobility of holes μ_p [8].

Drain current I_D produced by the MOSFET is directly proportional to its charge carrier mobility. Since mobility of electrons μ_n is greater than mobility of holes μ_p, N-channel MOSFET can produce higher peaks of Drain current I_D compared to P-channel MOSFET. Also, N-channel MOSFET switches faster and hence has higher operating frequencies and compact in size [8].

From **Equation (2.1)** On-state resistance R_{on} of P-channel MOSFET is almost double that of N-channel MOSFET since μ_n is almost double that of μ_p and this difference is well pronounced especially in higher current applications. Hence P-channel MOSFET has higher conduction losses compared to N-channel MOSFET [8].

Thus N-channel MOSFET has above mentioned significant advantages over P-channel MOSFET especially for higher current applications and hence it is chosen over P-channel MOSFET.

Based on the presence of physical inversion layer, MOSFET can be classified into two types, they are namely

1. Depletion MOSFET
2. Enhancement MOSFET

3.4 DEPLETION MOSFET

In Depletion MOSFET or D-MOSFET, the Drain and Source regions are connected by a physical channel implanted into the p-substrate as shown by the **Figure 3-3** [5]. The D-MOSFET can operate either in Depletion mode or Enhancement mode based on the applied Gate-Source Voltage V_{GS}. When a negative V_{GS} is applied, the electrons are repelled away from the physical channel attracting a large number of holes. Hence the Drain current I_D across the channel is greatly reduced.

For a Gate-Source Voltage $V_{GS(off)}$, the channel is completely depleted of electrons and Drain current I_D across the channel is zero. This Gate-Source Voltage $V_{GS(off)}$ is called Gate-Source Cut-off voltage.

This mode of operation is called the Depletion Mode.

However, when a positive Gate-Source Voltage V_{GS} is applied, Drain current I_D through the channel increases. This mode of operation is called the Enhancement mode [5].

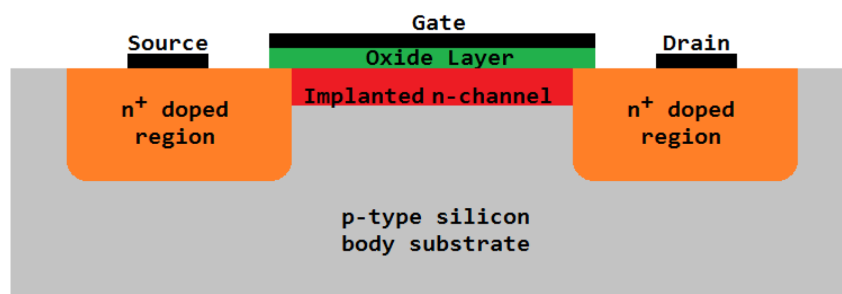

Figure 3-3 Depletion MOSFET [7]

3.5 ENHANCEMENT MOSFET

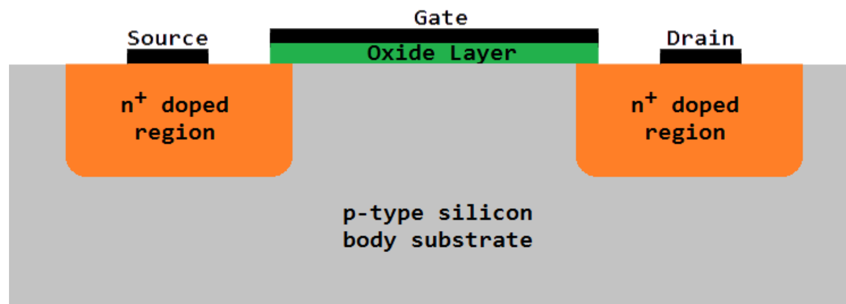

Figure 3-4 Enhancement MOSFET [7]

Figure 3-4 shows the construction of Enhancement MOSFET [7]. The Drain and Source regions are not connected by a physical channel. Hence the Enhancement MOSFET can be operated only in the enhancement mode but not in depletion mode [7].

When a positive $V_{GS} > V_{GS(th)}$ is applied, a channel of electrons or inversion layer is created and this increases conductivity of Drain current I_D through the inversion layer.

3.6 E MOSFET vs D MOSFET

Usually, Enhancement MOSFET is preferred over Depletion MOSFET since the Depletion MOSFET is more expensive because of implantation of Physical channel into the substrate [8].

Moreover, since the Depletion MOSFET has a physical channel, there is a possibility of leakage in Drain current I_D which is undesirable. Also, a negative Gate-Source voltage $V_T < V_{GS} < 0$, has to be applied to remove electrons from conduction channel to stop MOSFET from conducting. This increases complexity of the Gate circuit. On the other hand, because of the absence of a physical channel, the Enhancement MOSFET conducts only when a $V_{GS} > V_{GS(th)}$ is applied which is more controllable and reliable compared to the Depletion MOSFET [8].

Based on the type of substrate material, MOSFET can be classified into two types, they are namely

1. Si MOSFET
2. SiC MOSFET

3.7 SiC MOSFET

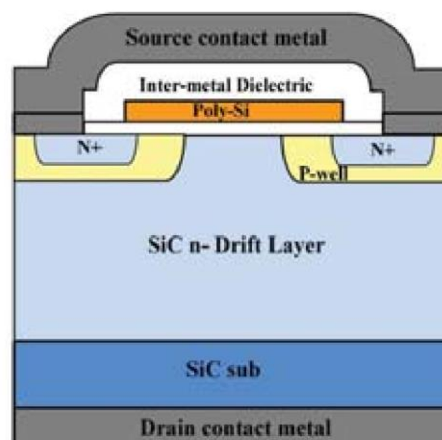

Figure 3-5 SiC MOSFET Structure [9]

Figure 3-5 shows the structure of a SiC MOSFET [9]. The SiC MOSFET is identical in structure to Si MOSFET except the substrate material alone is different which is Silicon Carbide. SiC MOSFET works exactly the same as that of the Si MOSFET. However, it has significant advantages over Si MOSFET because of its material properties.

3.7.1 SiC ADVANTAGES OVER Si

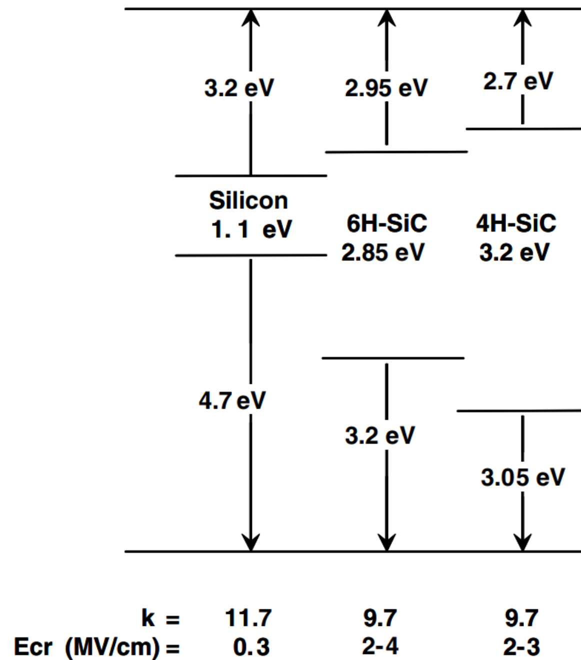

Figure 3-6 Bandgap, Dielectric constant, Critical field strength comparison [10]

Figure 3-6 compares Bandgap (eV), Dielectric strength k and Critical Field strength E_{cr} of Silicon with polymorphs of Silicon Carbide such as 6H-SiC and 4H-SiC. Silicon Carbide has a wider bandgap compared to Silicon.

The bandgap of Silicon is 1.1 eV whereas the bandgap of Silicon Carbide is 3.2 eV (4H-SiC) as shown in **Figure 3-6**. Wider the bandgap, higher potential has to be applied to remove electrons from the material. Hence higher is the breakdown field strength or Critical Field strength E_{cr} as listed in **Table 3-1**. Because of this, higher is the voltage blocking capability for the same thickness in SiC MOSFET.

Property	Si	4H-SiC
Bandgap (eV)	1.1	3.2
Critical Field E_c (MV/cm)	0.25	2-3
Thermal conductivity, κ (W/cmK)	1.5	5
Melting Point (°C)	1420	2830

Table 3-1 Electrical and Thermal properties of 4H-SiC vs Si [11]

SiC has higher thermal conductivity κ and higher melting Point (°C) mentioned in **Table 3-1** and hence better high temperature performance compared to Si devices [11].

The advantages in electrical and thermal properties of SiC over Si have been listed in above **Table 3-1**.

Because of better electro-thermal properties, SiC MOSFET has significantly lower switching losses. Hence it can achieve significantly higher switching frequencies compared to that of the Si MOSFET. Hence thickness of the SiC MOSFET is significantly lower [11]. Lower the thickness, lesser is the on-state resistance (Bulk resistance). Therefore, SiC MOSFET has higher current density and lower conduction losses compared to Si MOSFET [11].

From the website of Rohm, some of the advantages of SiC MOSFET over Si MOSFET is shown in **Figure 3-7** [12].

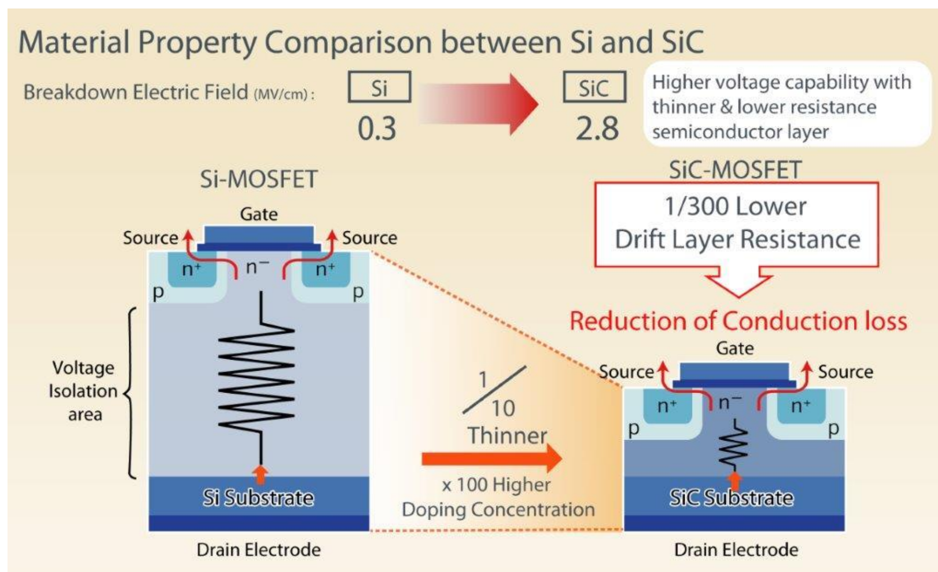

Figure 3-7 Advantages of SiC over Si [12]

3.8 SiC MOSFET vs Si MOSFET

3.8.1 OUTPUT CHARACTERISTICS

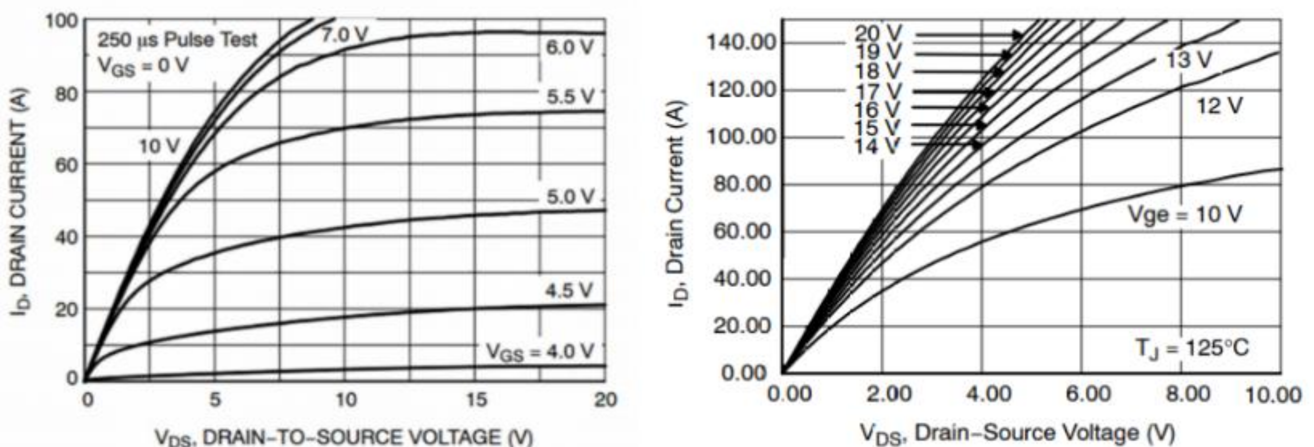

Figure 3-8 V_{DS} vs I_D a Si MOSFET b SiC MOSFET [13]

Figure 3-8 shows output characteristics of Si MOSFET vs SiC MOSFET. SiC MOSFET has lower transconductance compared to Si MOSFET and hence it has wider quasi-linear regions compared to Si MOSFET. Thus, the slope of the Drain current I_D increases throughout when V_{GS} is kept increasing until $V_{GS,max}$. On the other hand, due to abrupt change in quasi-linear regions, the slope of Drain current I_D stops increasing significantly beyond V_{GS} = 10 V. For this reason, SiC MOSFET can reach much higher Drain current I_D for higher V_{GS} compared to Si MOSFET. For the same reason lower Transconductance, knee points are less distinguishable in SiC MOSFET compared to Si MOSFET [13].

3.8.2 ON-STATE RESISTANCE AND THRESHOLD VOLTAGE

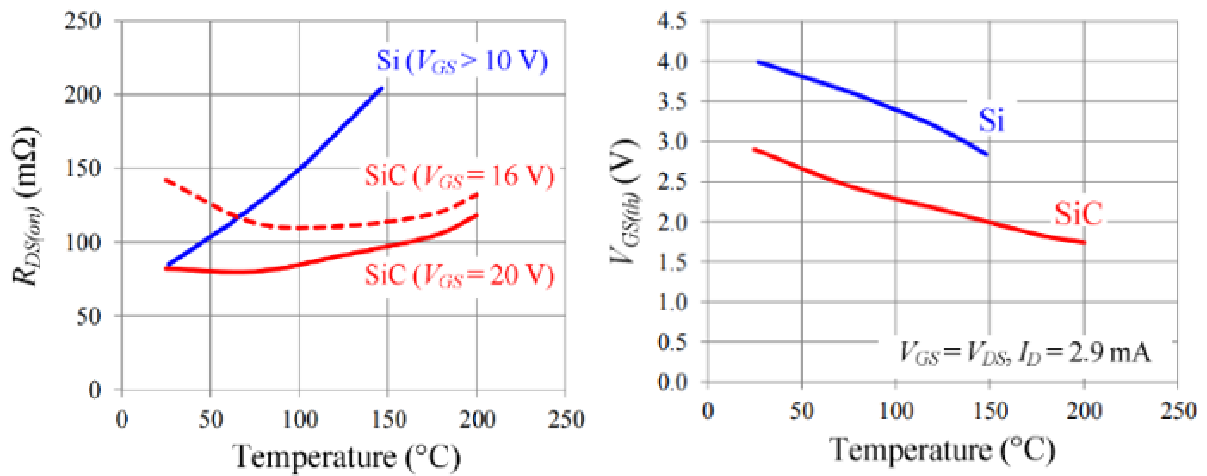

Figure 3-9 a $R_{DS(on)}$ b V_{GS} Si MOSFET vs SiC MOSFET [14]

Figure 3-9 a. shows the dependence of on-state resistance $R_{DS(on)}$ with respect to temperature of SiC MOSFET vs Si MOSFET at different V_{GS}. the $R_{DS(on)}$ of Si MOSFET increases linearly with rise in temperature even when V_{GS} is increased beyond 10 V. However, in SiC MOSFET, $R_{DS(on)}$ drops when V_{GS} is increased. Moreover, the conduction channel of the SiC exhibits unique property of negative temperature coefficient which is clearly visible at V_{GS} = 16 V.

At lower V_{GS}, the on-state resistance of MOSFET is dominated by the resistance of the conduction channel. When temperature increases, the channel resistance drops and compensates increase in on-state resistance of the bulk. Hence a drop in $R_{DS(on)}$ can be observed until when the resistance of the bulk becomes dominant. Thus SiC MOSFET has much lower $R_{DS(on)}$ compared to Si MOSFET [14]. Moreover, because of lower $R_{DS(on)}$, SiC MOSFET can accumulate more charges in the accumulation region below the oxide layer. Hence the threshold voltage $V_{GS(th)}$ needed for conduction of SiC MOSFET is lower compared to Si MOSFET [14].

3.8.3 TRANSCONDUCTANCE

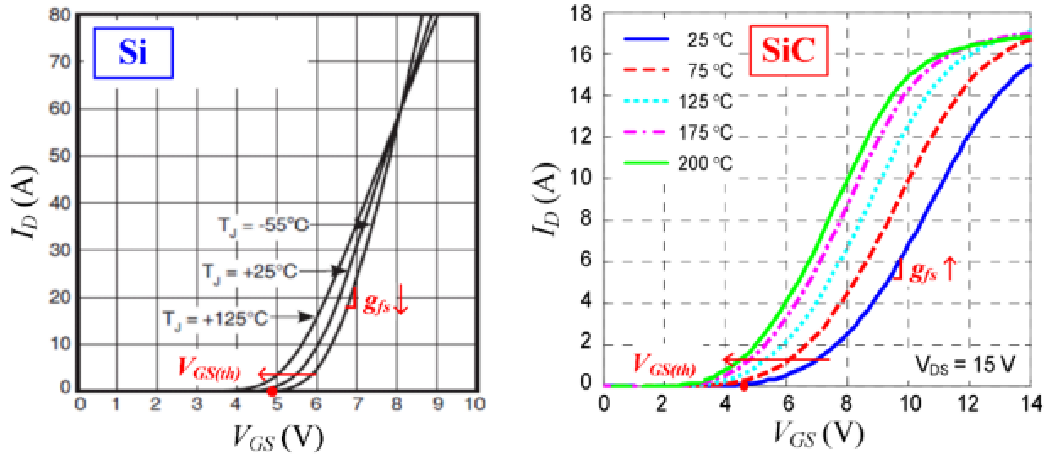

Figure 3-10 Transconductance gfs a Si MOSFET b SIC MOSFET [14]

Figure 3-10 a and b show Transconductance g_{fs} of both Si and SiC MOSFETs respectively. As a matter of fact, the g_{fs} of SiC MOSFET is lesser compared to that of the Si MOSFET. However, the g_{fs} of SiC MOSFET is special that it increases with increase in temperature whereas g_{fs} decreases with increase in temperature for Si MOSFET. This is attributed to the higher thermal conductivity of the SiC MOSFET bulk [14].

3.8.4 CAPACITANCE AND TIME DELAY

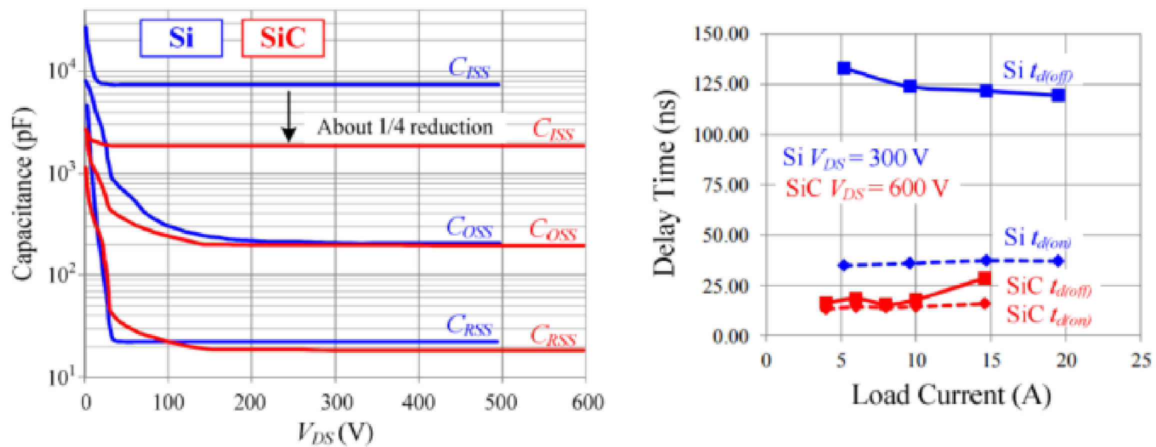

Figure 3-11 a Capacitances b Time delay Si vs SiC MOSFETs [14]

The input capacitance C_{ISS} of the SiC MOSFET is significantly lower than that of Si MOSFET ($^1/_4$ times) whereas capacitances C_{OSS} and C_{GSS} are of the same order. As a result, the charge required by Gate terminal to form conduction channel in the SiC MOSFET is only $^1/_4 th$ of that of the Si MOSFET. This results in quicker Gate charging time and hence lower time delay during turn-off and turn-on. Whereas the Si MOSFET has significantly longer time delays shown in **Figure 3-11** b. Moreover, because of lower Gate charging required, SiC MOSFET has lower switching losses compared to Si MOSFET. This contributes to much higher operating frequency of SiC MOSFET compared to Si MOSFET since time delay in SiC MOSFET is greatly reduced [14].

3.8.5 SWITCHING TRANSIENTS

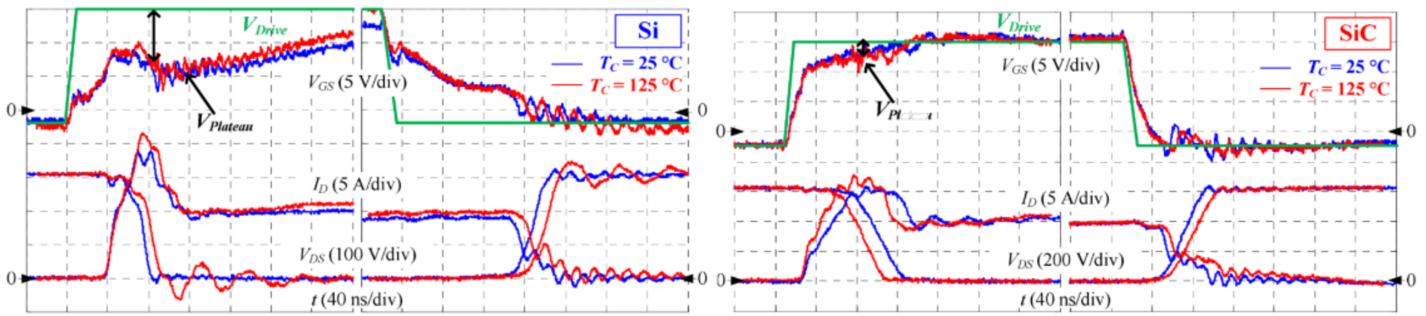

Figure 3-12 Switching transients a Si MOSFET b SiC MOSFET [14]

Figure **3-12** shows the comparison of switching transients between Si MOSFET and SiC MOSFET. During turn ON, SiC MOSFET exhibits lower voltage drop across Drain-Source terminals V_{DS} since it has lower $R_{DS(on)}$ compared to Si MOSFET which exhibits higher Voltage drop during t-ON [11].

During t-ON, there is a spike in Drain current I_D that has two reasons. Reverse-recovery current of the body diode and Drain-Gate Capacitance C_{gd} is being discharged. This spike is more dominant in Si MOSFET compared to SiC MOSFET indicating poor reverse recovery in Si MOSFET [11].

Gate Voltage V_{GS} of the MOSFET undergoes oscillations called Gate ringing. This happens because the $\frac{dI_D}{dt}$ of the Drain current I_D causing a Voltage surge (V_{pk} discussed in TURN-OFF of MOSFET) in V_{DS} reflected on V_{GS} through Gate Capacitances C_{gd}, causing transients in Gate Source Voltage V_{GS}. In SiC MOSFET the transients die out faster compared to Si MOSFET since it has lower C_{gd} (τ = RC) [11].

Thus SiC MOSFET delivers superior performance over Si MOSFET for following reasons namely, higher peaks of drain currents, same blocking capability for thinner device, lower $R_{DS(on)}$, higher current density, higher switching frequency and better switching transients.

Based on the structure of Gate terminal, MOSFET can be classified into two types, they are namely

1. Planar MOSFET
2. Trench MOSFET

3.8.6 PLANAR MOSFET vs TRENCH MOSFET

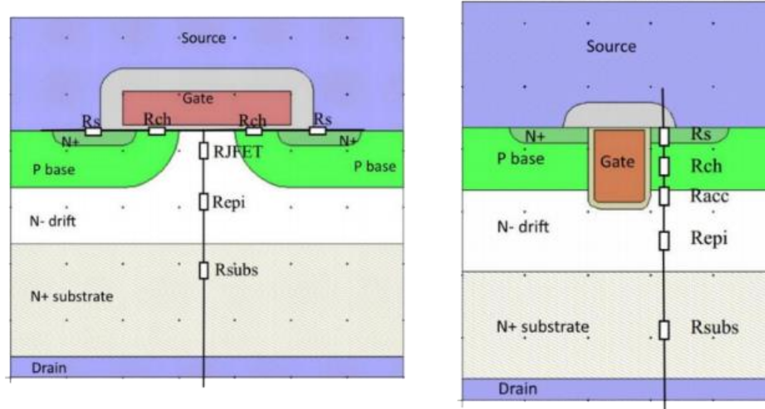

Figure 3-13 a Planar MOSFET b Trench MOSFET [15]

Figure 3-13 a shows Planar MOSFET and **Figure 3-13** b shows Trench MOSFET respectively. In Planar MOSFET, since the Gate terminal is horizontal to the bulk, an inversion layer is formed horizontally between heavily doped n^+ region and n^- drift region.

However, Trench Gate structure is formed by etching Gate terminal vertically and the conduction layer is formed vertically between heavily doped n^+ region and n^- drift region.

In Trench MOSFET, width W of the inversion layer is wider and length L of the inversion layer is shorter than in the Planar MOSFET to get lower channel resistance $\boldsymbol{R_{ch}}$ and hence a higher drain current $\boldsymbol{I_D}$. However, since n^- drift region is reduced in thickness in Trench MOSFET, the extent of depletion region within the n^- drift region is greatly reduced. Hence the voltage blocking capability of such a Trench MOSFET is drastically reduced for the same thickness compared to Planar MOSFET [15]. This limits the Trench MOSFETs from being used in high voltage applications [15].

In Planar MOSFETs, the Drain current flows from Drain terminal to JFET region vertically and from JFET region (n^- drift region) to Source (heavily doped n^+ region) horizontally which causes current crowding at the JFET region. This is because of the geometry of the conduction channel. The conduction channel has smaller width W and relatively longer length L thereby increasing channel resistance R_{ch} [15]. Also, the on-state resistance $R_{DS(on)}$ of the Planar MOSFET is higher compared to Trench MOSFET of the same rating since Planar MOSFET has JFET region resistance R_{JFET} which is absent in Trench MOSFET shown in **Figure 3-14** [15][9].

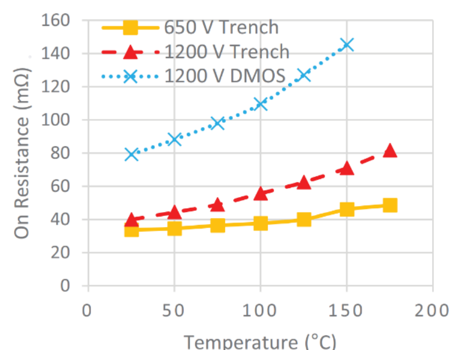

Figure 3-14 On-state Resistance $R_{DS(on)}$ Planar MOSFET vs Trench MOSFET [9]

Planar MOSFET and Trench MOSFET of similar ratings are subjected to Short Circuit Withstand test as shown in **Figure 3-15**. Ratings: Planar MOSFET (V_{DS} = 650 V, I_D = 29 A, $R_{DS(on)}$ = 120 mΩ, V_{GS} = 18 V) and Trench MOSFET (V_{DS} = 650 V, I_D = 21 A, $R_{DS(on)}$ = 120 mΩ, V_{GS} = 18 V). The active chip area: Trench MOSFET 0.021847 cm^2; Planar MOSFET 0.054941 cm^2 [16];

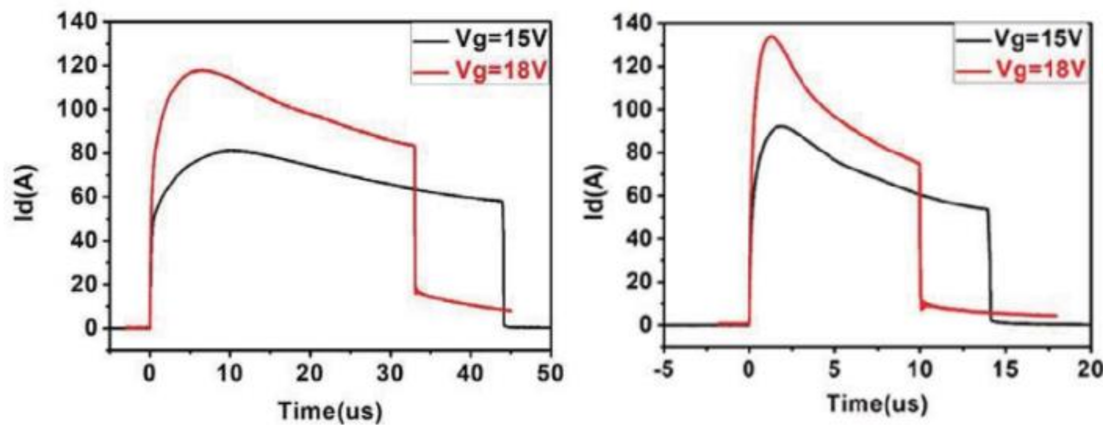

Figure 3-15 SCWT a Planar MOSFET b Trench MOSFET [16]

Even though the Trench MOSFET was able to achieve 13% higher Short Circuit current compared to Planar MOSFET at a current density of 2.85 times higher than Planar MOSFET, it has poor withstanding capability during the Short Circuit test because the Electric field intensity is very high at the corner of the Trench Gate structure as shown in **Figure 3-16**, which is the weakest portion of the Trench MOSFET structure. This leads to premature destruction of the Gate terminal of the Trench MOSFET during high voltages [16].

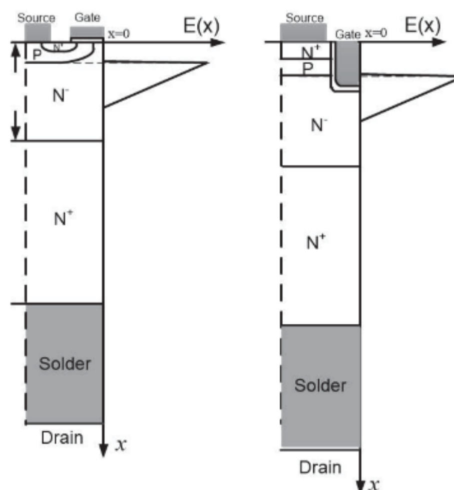

Figure 3-16 Electric field distribution a Planar MOSFET b Trench MOSFET [16]

Thus, Planar MOSFET is preferred over Trench MOSFET since Trench MOSFET has lower breakdown voltage strength compared to Planar MOSFET making Trench MOSFET comparatively less suitable for short circuit tests at high Voltages [16].

3.9 SUMMARY

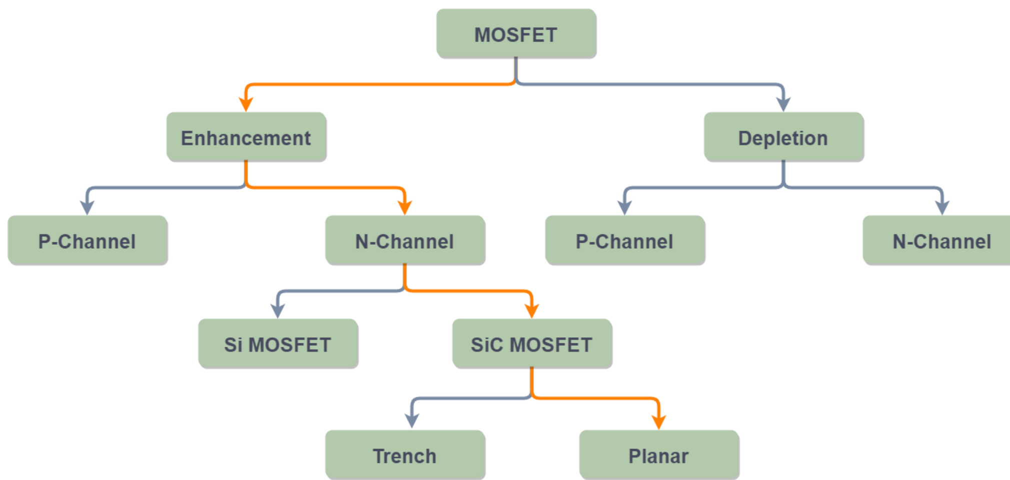

Figure 3-17 Flowchart - Types of MOSFET

In this chapter, MOSFET was classified based on physical implantation of inversion layer or conduction channel into Depletion and Enhancement MOSFETs. Enhancement MOSFET was preferred over Depletion MOSFET for its simplicity, reliability and low cost. Based on the types of charge carriers, MOSFET was classified into P-channel and N-channel MOSFET. N-channel MOSFET was preferred over P-channel MOSFET for its higher charge carrier mobility μ_n. Based on material of the substrate used, MOSFET was classified into Si and SiC MOSFET. Because of advantageous material properties, SiC MOSFET was preferred over Si MOSFET. Finally, based on structure, MOSFET was classified into Planar and Trench MOSFET. Even though Planar MOSFET was able to conduct lower Drain current I_D, it is preferred over Trench MOSFET since Planar MOSFET has higher blocking capability making it more feasible to operate at higher voltages during short circuit test.

Thus from **Figure 3-17,** Planar SiC MOSFET is identified as the potential switching technology among MOSFETs that could deliver highest drain current, blocking voltage and switching frequency.

4

IGBT

Insulated Gate Bipolar Junction Transistors is a power electronic device technology that combines the best qualities of BJT and MOSFET such as high current conducting capability and high switching speeds respectively [2]. IGBT is a three terminal device namely Gate, Collector and Emitter as shown in **Figure 4-1** [2]. It resembles the symbol of an npn-BJT as it has Collector and Emitter terminals. However, in place of a Base terminal of a BJT, IGBT has a Gate terminal like a MOSFET [2]. Since, the structure of IGBT is almost identical to that of the MOSFET, the circuits often express IGBT with MOSFET terminals such as Gate, Source and Drain [2].

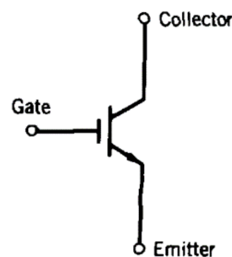

Figure 4-1 IGBT Symbol [2]

4.1 IGBT STRUCTURE

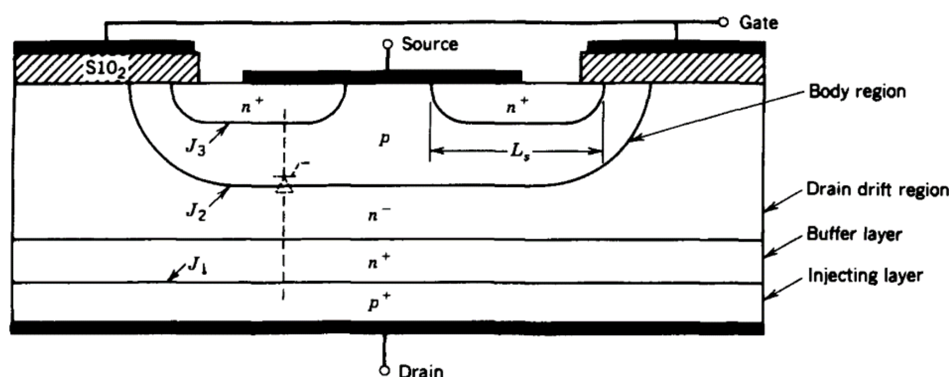

Figure 4-2 Structure of IGBT [2]

Figure 4-2 shows the structure of IGBT which resembles MOSFET with addition of p^+ layer (injection layer) at the Drain terminal of the IGBT [2]. It has three Junctions formed between adjacent p and n layers namely J1, J2 and J3. The Body region is shorted to Source terminal to avoid possible turn ON of the parasitic thyristor shown in **Figure 4-2** [2]. The various layers of the structure of IGBT form effective n-channel enhancement MOSFET and pnp BJT as shown in **Figure 4-3**. p^+ injecting layer, n^- Drift layer and p Body region form Emitter, Base and Collector terminals of the pnp BJT. Layers n^+ pn^- n^+ which are above the p^+ injecting layer form an effective MOSFET within the n-channel IGBT structure.

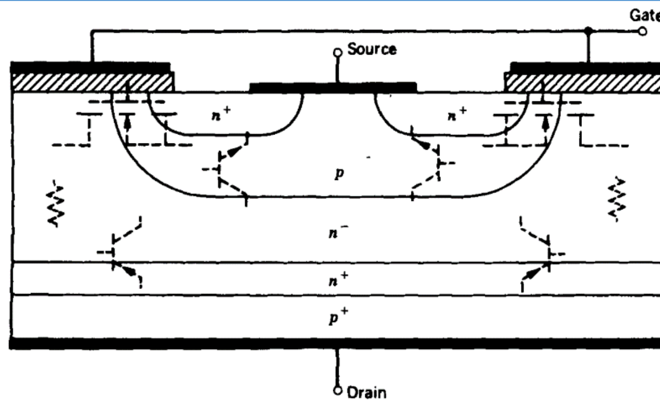

Figure 4-3 Effective MOSFET and BJT portions [2]

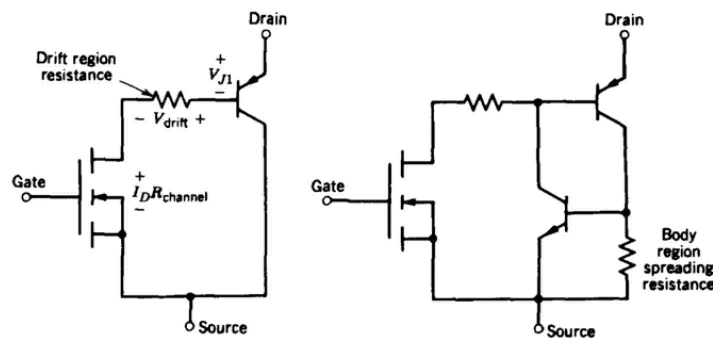

Figure 4-4 a IGBT Equivalent circuit b Parasitic Elements of IGBT [2]

Drift resistance of the n^- drift layer in **Figure 4-4** a is in between Base terminal of the pnp BJT and the Drain of the MOSFET [2]. Majority of the current flows through the MOSFET which is desirable as it avoids turning parasitic thyristor ON shown in **Figure 4-4** b [2].

Hence the on-state voltage drop across IGBT is expressed as

$$V_{DS(on)} = V_{J1} + V_{drift} + I_D R_{channel}$$

4.2 IGBT WORKING

Because of its construction similar to that of the MOSFET, IGBT essentially operates like a MOSFET based on Field Effect [2]. When a positive voltage across Gate-Source terminal $V_{GS} > V_{GS(th)}$ applied, a conduction channel is formed in the p-layer between n^+ and n^- drift region [2].

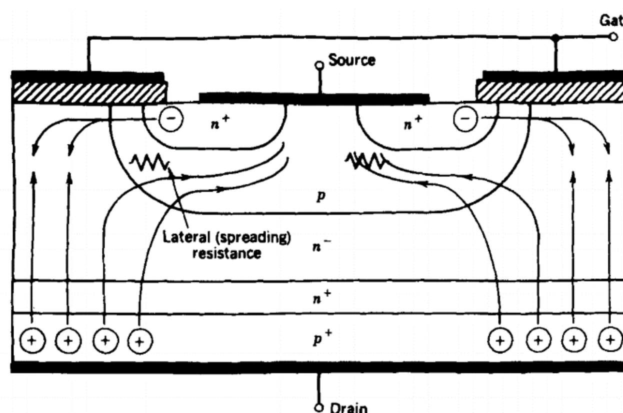

Figure 4-5 Conduction in IGBT [2]

Thus, electrons flow into n^- drift layer through the conduction layer as shown in **Figure 4-5** [2]. As a result, junction J_2 becomes forward bias. Because of this, a significant number of holes are injected from p^+ injection layer to the n^- drift region and thereby arrive at the p-region. This conduction of charge carriers called as conductivity modulation which significantly reduces the on-state resistance $R_{DS(on)}$ of the IGBT compared to a MOSFET [2]. The holes that arrive at the p-region reach the Source terminal contributing to the conduction of IGBT. Some of the excess holes recombine with the electrons in the n^- drift layer and some of the holes remain in the structure of IGBT. Thus, IGBT has current tailing during turn OFF [2].

4.3 IV CHARACTERISTICS

The IV characteristics of the IGBT shown in **Figure 4-6** resembles the IV curves of a BJT, however Gate-Source Voltage $\boldsymbol{V_{GS}}$ is the controlling parameter of IGBT. Since $\boldsymbol{V_{GS} > V_{GS(th)}}$ enables the device to conduct, IGBT is a voltage-controlled device [2].

Since n^+ buffer layer is used, blocking capability BV_{DSS} of the junction J1 of the device is reduced as a result of heavy doping. Moreover, this reduces the reverse-blocking capability V_{RM} of the IGBT significantly which is represented in **Figure 4-6** [2].

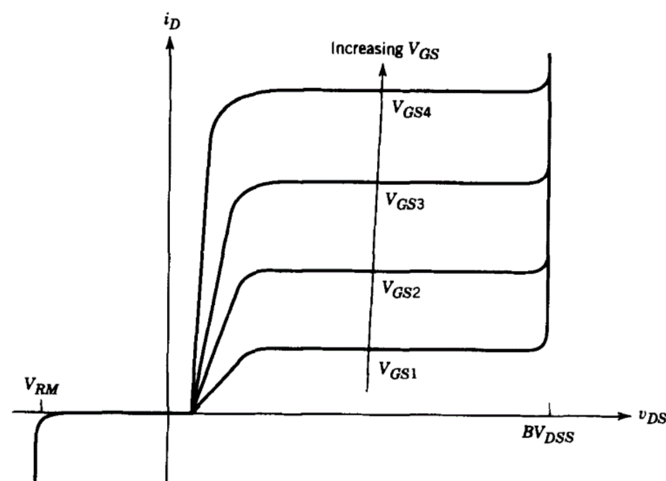

Figure 4-6 IGBT IV Characteristics [2]

4.4 IGBT LATCHUP

When a hole current laterally travels across the body region shown in **Figure 4-5**, it drops a voltage across the spreading resistance which makes the junction J_1 between n^+p layers forward bias [2].

If this voltage drop is high enough to attract electrons from Source to the Body region, the parasitic npn transistor shown in **Figure 4-4 b** is turned ON. This causes the parasitic thyristor shown in to latch **Figure 4-2** [2].

As a result, the Gate-Source Voltage $\boldsymbol{V_{GS}}$ loses its control over the Drain current $\boldsymbol{I_D}$. Hence the IGBT can only be turned off by forced commutation just like how a thyristor is turned off [2]. If the IGBT is not turned off after being latched, it is bound to dissipate excessive heat and lead to destruction [2]. The equivalent circuit during conduction of IGBT is shown in **Figure 4-7** below,

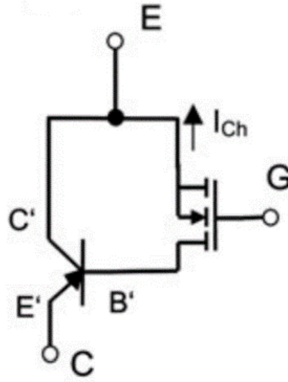

Figure 4-7 Equivalent circuit during IGBT conduction [3]

From the circuit of Figure **4-7**, the terminals of the pnp BJT are indicated as E' – Emitter, B' – Base and C' – Collector and terminals of IGBT as G – Gate, C – Collector and E – Emitter [3].

The collector current of IGBT is given as

$$I_c = I_{C'} + I_{CH} \qquad \text{Equation (4.1)}$$

$$I_{C'} = \beta_{pnp} I_{CH} \qquad \text{Equation (4.2)}$$

$$I_{C'} = \frac{\alpha_{pnp}}{1 - \alpha_{pnp}} I_{CH} \qquad \text{Equation (4.3)}$$

Where $\alpha = \frac{\beta}{\beta+1}$

$$I_c = \frac{\alpha_{pnp}}{1 - \alpha_{pnp}} I_{CH} + I_{CH} \qquad \text{Equation (4.4)}$$

To avoid latch-up, the current through Collector terminal C' should be as low as possible, hence from Equation **(4.3)** α_{pnp} must be as low as possible [3].

4.4.1 AVOIDING LATCHUP

One way of avoiding latch-up is to reduce the switching speed of IGBT during turn-off as it allows holes to recombine slowly. Hence minimising the lateral current across spreading resistance indicated in Figure **4-5**. This can be achieved by increasing the value of Gate resistance R_G thereby increasing time constant [2].

4.5 IGBT SWITCHING

4.5.1 TURN ON

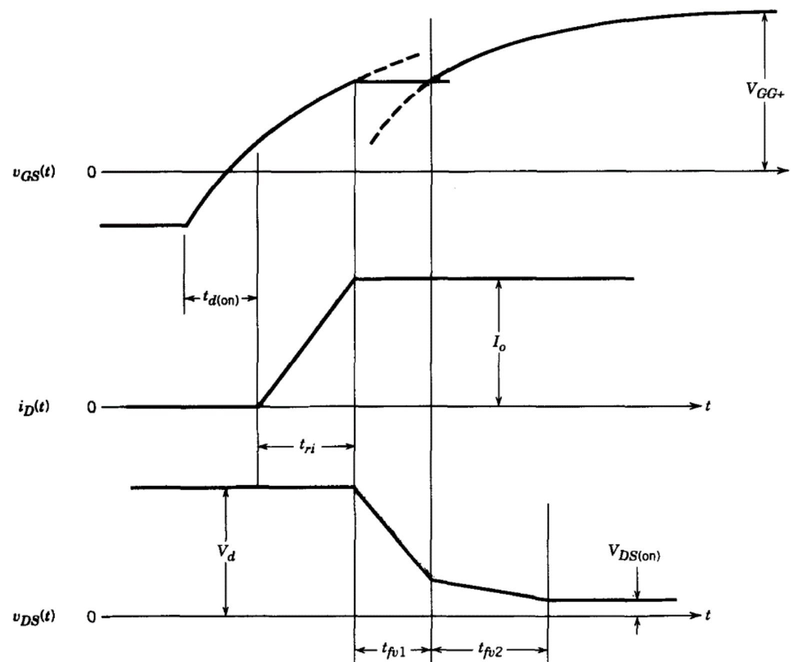

Figure 4-8 IGBT turn-on waveforms [2]

Since the IGBT is essentially behaving as a MOSFET, the IGBT turn ON characteristics is almost identical to that of the MOSFET. Moreover, Turn ON of IGBT can be understood with the same equivalent circuits as that of the MOSFET [2].

However, during t_{fv2} from **Figure 4-8**, V_{DS} does not drop to its final on-state value immediately since value of Gate-Drain capacitance C_{gd} increases in the MOSFET part of the IGBT and during this interval the pnp BJT is switching from its active state to hard saturation slowly [2].

4.5.2 TURN OFF

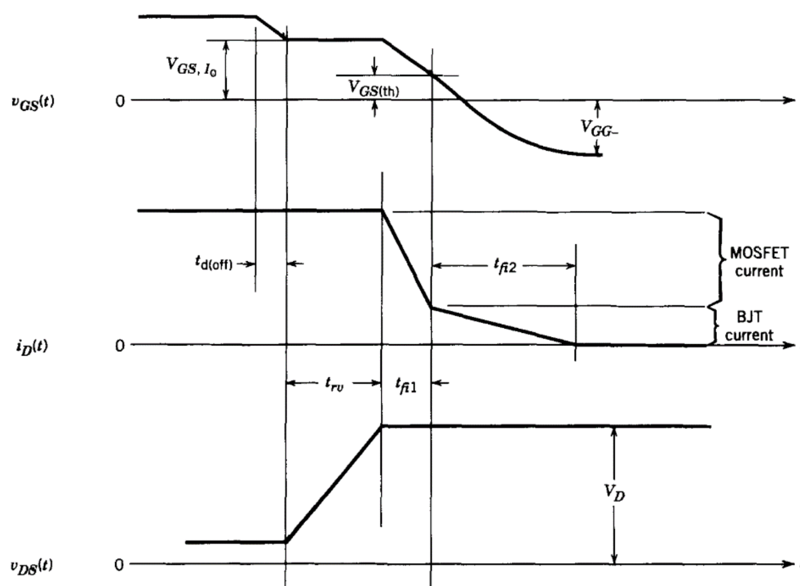

Figure 4-9 IGBT Turn-off waveforms [2]

The turn OFF characteristics of IGBT is shown in **Figure 4-9** [2]. By observing the figure, it can be stated that the only difference in turn-off transients between MOSFET and IGBT is observed in the Drain current $\boldsymbol{I_D}$ in two different time intervals $\boldsymbol{t_{fi1}}$ and $\boldsymbol{t_{fi2}}$ [2].

During $\boldsymbol{t_{fi1}}$, the Drain current $\boldsymbol{I_D}$ drops rapidly which corresponds to the turn-off of the MOSFET part of IGBT. During $\boldsymbol{t_{fi2}}$ the tailing of the Drain current $\boldsymbol{I_D}$ occurs since $\boldsymbol{n^-}$ drift region has stored charges that can only be removed by recombination within the structure of IGBT [2].

If $\boldsymbol{t_{fi2}}$ is long, the power dissipation across the IGBT is high since voltage drop across the Drain-Source region $\boldsymbol{V_{DS(on)}}$ is not the lowest. This can have degrading effects on IGBT [2].

4.6 IGBT LIMITATIONS

Maximum Drain current $\boldsymbol{I_{D(max)}}$ depends on the $\boldsymbol{V_{GS(max)}}$ applied across MOSFET part of the IGBT, which is the maximum voltage that can be applied across Gate-Source terminals without breaking down the Gate oxide layer [2].

Maximum $\boldsymbol{V_{DS(max)}}$ that can be applied across IGBT is determined by the breakdown voltage of pnp BJT $\boldsymbol{BV_{CBO}}$ which is determined by the breakdown voltage of Body-Drift regions [2].

During Reverse bias conditions, a too large $\boldsymbol{\frac{dv_{DS}}{dt}}$ can cause the IGBT latch-up. Hence to avoid too high $\boldsymbol{\frac{dv_{DS}}{dt}}$, proper Gate Source voltage $\boldsymbol{V_{GS}}$ and Gate resistance $\boldsymbol{R_G}$ must be selected [2].

5

TYPES OF IGBT

Based on the presence of n^+ buffer layer IGBT is classified into three types, they are namely

1. Punch-Through IGBT (PT IGBT)
2. Non-Punch-Through (NPT IGBT)
3. Field Stop IGBT (FS IGBT)

The Punch-Through IGBT (PT IGBT) has n^+ buffer layer and Non-Punch-Through (NPT IGBT) does not have n^+ buffer layer. However, the Field Stop IGBT has a lightly doped n^- buffer layer. The types of IGBT are discussed in detail in the upcoming sections of this chapter.

5.1 PT-IGBT

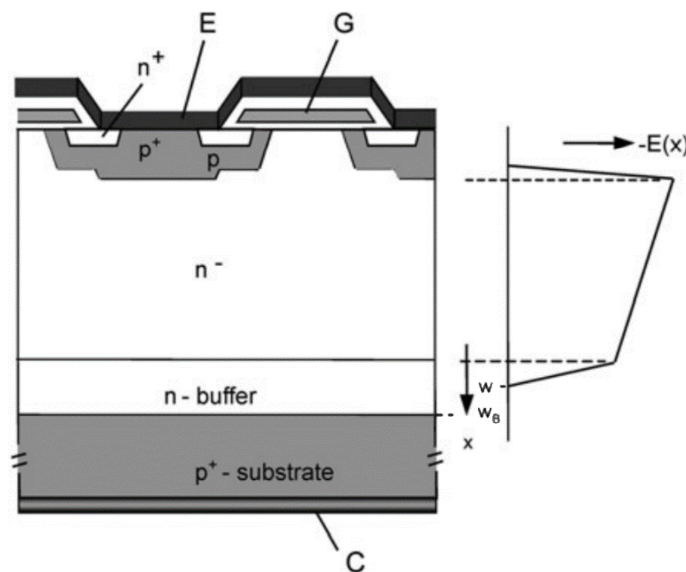

Figure 5-1 PT-IGBT structure [3]

Figure **5-1** represents the construction of a Punch-Through IGBT (PT IGBT) and its electric field distribution [2]. The most important feature of PT IGBT is the presence of heavily doped n^+ buffer layer sandwiched between n^- drift region and p^+ substrate [2].

From Figure **5-1**, the electric field is trapezoidal in shape and it crosses the n^- drift region and extends into the n^+ buffer layer and hence called as Punch-Through IGBT. Area under the curve E(x) gives the blocking capacity of the device [3].

Adding n^+ buffer layer in the bulk reduces the thickness of the n^- drift region thereby reducing $R_{CE(on)}$. Since n^+ buffer layer is heavily doped it significantly reduces $V_{CE(on)}$ during on-state and hence lesser on-state conduction losses compared to that of the NPT IGBT [2].

However, the blocking capability of the device is determined by how much the depletion region of junction J_2 can extend into the n^- drift region. Since the thickness of n^- drift region is reduced by adding n^+ buffer layer, the forward blocking capability of the device is significantly reduced for the same thickness compared to NPT-IGBT [2].

Moreover, the reverse blocking capability of the PT IGBT is only a few tens of volts since the breakdown voltage strength of n^+ layer is too small [2].

Because of unequal forward and reverse voltage blocking capabilities, PT IGBT is also termed as unsymmetric IGBT [3].

During turn-off of the IGBT, the MOSFET portion of the IGBT turns off even before the excess holes are removed from the n^- drift region of the IGBT leading to long current tailing shown in **Figure 4-9**.

Since n^+ buffer layer is heavily doped and has excess free electrons, this layer can act as sink for the excess holes during turn-off significantly reducing current tailing of IGBT [3].

From **Figure 5-1**, effective Base of pnp BJT starts at the end of space charge region between $x = w$ and $x = w_B$ [3]. Since the Base width w_B is very small and is inversely proportional to current gain β of the pnp BJT transistor, PT-IGBT is easily prone to latch-up [3].

High value of β_{pnp} leads to a high value of α_{pnp}

$$\alpha_{pnp} = \gamma \, \alpha_T \quad \text{Equation (5.1)}$$

Where α_T is called as the Transport factor and γ is Emitter efficiency of the pnp BJT [2].

$$\gamma = \frac{1}{1 + \frac{\mu_n}{\mu_p} \frac{N_{buf}}{N_{sub}} \frac{L_p}{L_n}} \quad \text{Equation (5.2)}$$

$$\alpha_T = 1 - \frac{w_B^2}{2\, L_p^2} \quad \text{Equation (5.3)}$$

$$L_p = \sqrt{D_p \, \tau_p} \quad \text{Equation (5.4)}$$

Where N_{buf} is the doping concentration of buffer layer, N_{sub} is doping concentration of substrate, L_p diffusion length, D_p diffusion co-efficient and τ_p lifetime of holes.

Latch-up can be avoided by heavily doping n^+ buffer layer, thus reducing lifetime τ_p of the holes by creating recombination centres of excess free electrons which leads to lower diffusion length L_p [3].

Lower diffusion length L_p of holes reduces the transport factor α_T thereby reducing Emitter efficiency γ of pnp BJT. Hence α_{pnp} is reduced thereby reducing the risk of latch-up of the PT-IGBT [3].

5.2 NPT-IGBT

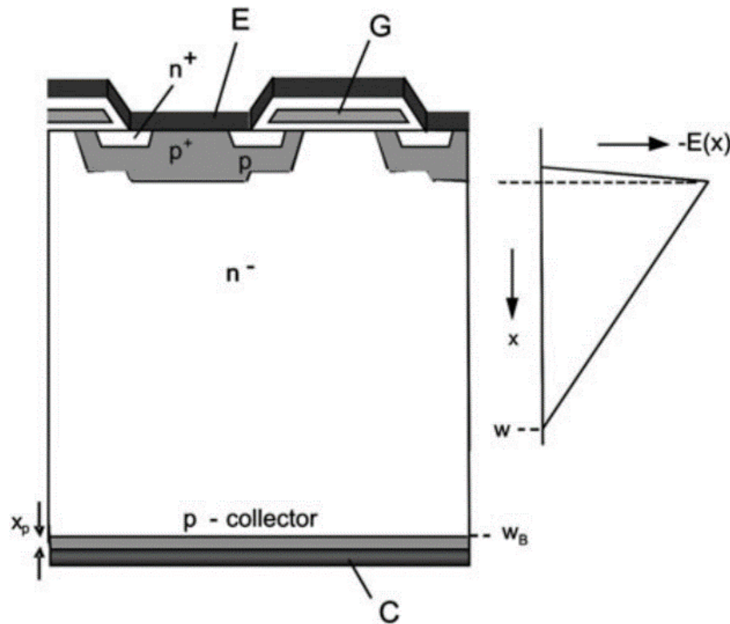

Figure 5-2 NPT-IGBT structure [3]

Figure 5-2 shows the structure of Non-Punch-Through IGBT and its electric field distribution [3]. The $\boldsymbol{n}^{+}$ buffer layer is absent in the NPT-IGBT and also the $\boldsymbol{p}^{+}$ injection layer is very thin compared to the PT-IGBT [3].

The electric field distribution E(x) is triangular and it does not enter into the thin $\boldsymbol{p}^{+}$ substrate region and hence called as Non-Punch-Through IGBT [3].

Since the $\boldsymbol{n}^{-}$ drift region is thicker in NPT-IGBT, the depletion region of junction $\boldsymbol{J_2}$ can extend into the $\boldsymbol{n}^{-}$ drift region much further than that of the PT-IGBT. Hence the voltage blocking capability of the NPT IGBT is significantly larger than that of the PT-IGBT [2].

Also, the reverse blocking voltage of the NPT IGBT is same as that of the forward blocking voltage. Hence it is termed as symmetrical IGBT [2].

Since $\boldsymbol{n}^{-}$ drift region is thicker in NPT IGBT, the on-state Resistance $\boldsymbol{R_{CE(on)}}$ and on-state forward voltage drop $\boldsymbol{V_{DS(on)}}$ across the NPT-IGBT is significantly higher [2].

Because of higher voltage drop $\boldsymbol{V_{DS(on)}}$ during on-state, NPT IGBT has more on-state conduction losses compared to that of the PT IGBT [2].

Since NPT-IGBT does not have $\boldsymbol{n}^{+}$ buffer layer, it suffers a long current tailing. However, the MOSFET part of IGBT is constructed in such a way that it conducts most of the current before it turns-off. Hence only a small proportion of current during IGBT turn-off period flow through the BJT part as current tail [2].

From the **Figure 5-2** the effective Base width of the pnp BJT transistor starts at the end of the space charge region between $\boldsymbol{x} = \boldsymbol{w}$ and $\boldsymbol{x} = \boldsymbol{w_B}$ [3].

Since NPT IGBT has thicker $\boldsymbol{n}^{-}$ drift region, it also has a wider Base region for the pnp BJT. As a result, NPT IGBT has intrinsically lower values of $\boldsymbol{\beta}$ compared to PT IGBT [3].

$$\alpha_{pnp} = \gamma\ \alpha_T \quad \text{Equation (5.5)}$$

$$\alpha_T = 1 - \frac{w_B^2}{2\ L_p^2} \quad \text{Equation (5.6)}$$

$$\gamma = 1 - q\ h_p\ \frac{p_L^2}{j} \quad \text{Equation (5.7)}$$

$$h_p = \frac{D_n}{p^+\ X_p} \quad \text{Equation (5.8)}$$

Where α_T is called as the Transport factor and γ is Emitter efficiency of the pnp BJT, w_B is width of Base region of BJT, L_p is diffusion length of holes and h_p is emitter parameter [3].

At low doping of p^+ and $x_p < 1$ µm, h_p emitter parameter is high. Therefore γ emitter efficiency is low. Hence α_{pnp} of the pnp BJT is lower naturally. Thus, NPT IGBT is intrinsically resistant to latch-up of the IGBT [3].

5.3 NPT-IGBT vs PT-IGBT

5.3.1 ON-STATE VOLTAGE DROP AND CONDUCTION LOSSES

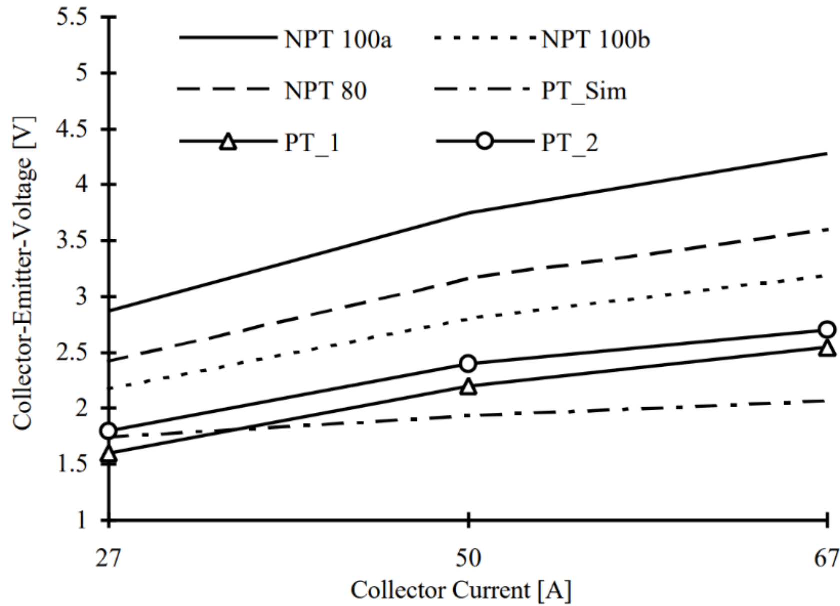

Figure 5-3 $V_{CE(sat)}$ NPT-IGBT vs PT-IGBT [17]

Because of the presence of n^+ buffer layer, the thickness of n^- drift layer is reduced in PT-IGBT. However, the NPT-IGBT does not have n^+ buffer layer and has thicker n^- drift layer. Because of this on-state resistance $R_{DS(on)}$ is lower in PT-IGBT and higher in NPT-IGBT. Thus, the voltage drop $V_{CE(sat)}$ and thereby conduction losses are lower in PT-IGBT compared to NPT-IGBT shown in **Figure 5-33** [17].

5.3.2 SWITCHING LOSSES

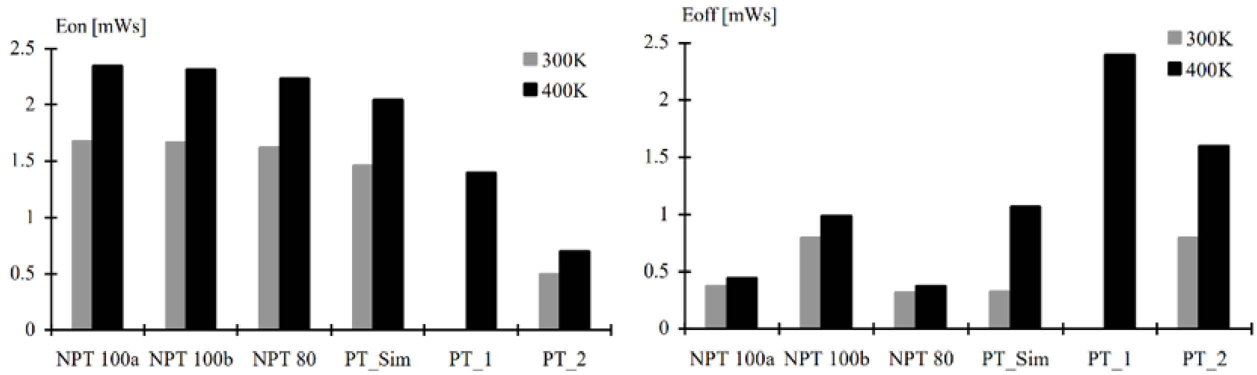

Figure 5-4 Switching Losses a Eon & b Eoff NPT-IGBT vs PT-IGBT [17]

Figure 5-4 a and b represent switching losses E_{on} and E_{off} respectively of NPT and PT IGBTs. Both NPT-IGBT and PT-IGBT have comparable losses during turn-on E_{on}. This turn-on losses E_{on} in both NPT-IGBT and PT-IGBT technologies are attributed to the poor reverse recovery of Collector current through the body diodes of the IGBTs. This turn-on losses are aggravated with increase in temperature [17].

During turn-off, IGBTs have current-tailing because of retention of holes in the n^{-} drift region [2].

During turn-off, the NPT-IGBTs have long current tailing because of the absence of n^{+} buffer layer. However the magnitude of Collector current is insignificantly low. On the other hand, PT-IGBTs have high magnitudes of Collector current during turn-off and a very short tail since they are recombined in n^{+} buffer layer [2].

This process is highly temperature sensitive in PT-IGBT whereas independent of temperature in NPT-IGBT. Thus PT-IGBTs have higher turn-off losses compared to NPT-IGBTs especially at higher temperatures [8]. Hence NPT-IGBTs have lower overall switching losses compared to PT-IGBTs.

5.4 SHORT CIRCUIT TEST

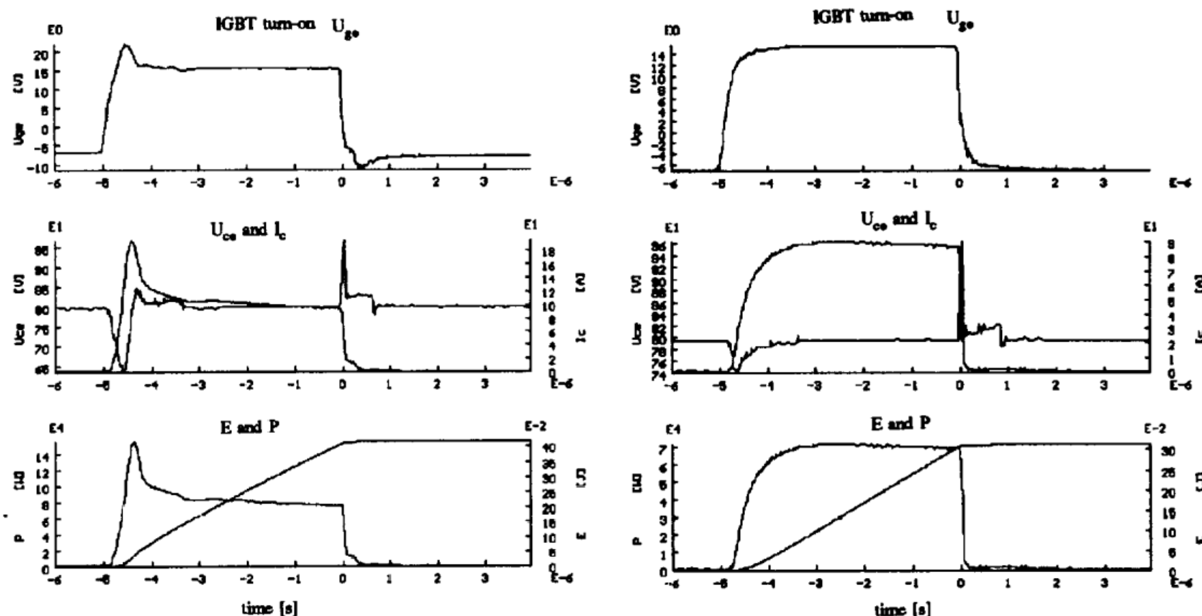

Figure 5-5 Non-destructive Short circuit test PT vs NPT-IGBT [18]

A non-destructive Short Circuit test for 5 μs is performed to compare short circuit bhaviour of PT-IGBT (TOSHIBA MG15Q6ES40 – 1200 V/15 A) and NPT-IGBT (SIEMENS BSMISGDIOOD – 1000 V/15 A). A short Gate pulse of 5 μs is applied for both the switching technologies. From **Figure 5-5,** for an applied Collector-Emitter voltage of 80 V, PT-IGBT technology conducted 18 A of Collector current I_c. On the other hand, the NPT-IGBT conducted peak current of 9 A, half the Collector current I_c as that of the PT-IGBT. This is attributed to higher transconductance g_{fs} of the PT-IGBT technology compared to the NPT-IGBT technology. Higher the transconductance g_{fs} of the device is, more Collector current I_c can be produced for the same Gate-Emitter voltage V_{GE} applied. Moreover, the PT-IGBT was able to produce 30% more Short Circuit energy than that of the NPT-IGBT [18].

5.5 TRENCH GATE FIELD-STOP IGBT

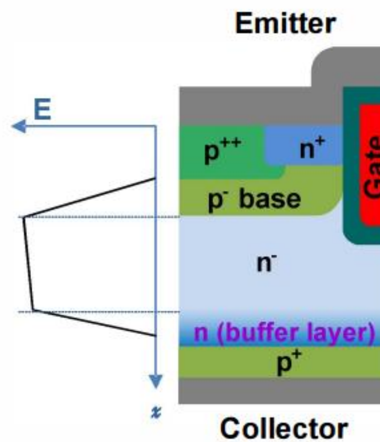

Figure 5-6 Structure of Trench Field-Stop IGBT [19]

Figure 5-6 shows the cross-section of the Trench Gate Field-Stop IGBT and electric field distribution across its cross section. The Field-Stop IGBT uses both Trench Gate structure and lightly doped Field stop layer (n-buffer layer) to achieve the advantages of both NPT-IGBT and PT-IGBT such as lowest on-state voltage drop $V_{CE(on)}$, high Collector current I_C, current tailing is almost eliminated, lower capacitances and hence higher switching frequencies and lower switching losses [19].

The electric field distribution in Field-Stop IGBT looks similar to that of the PT-IGBT. The Field stop layer (n-buffer layer) is doped high enough to stop the electric field from reaching the p^+ injection layer, but also not too heavily doped so that the emitter efficiency γ from **Equation (5.2)** is low. Hence the Field-Stop IGBT has higher resistance towards latch-up compared to PT-IGBT.

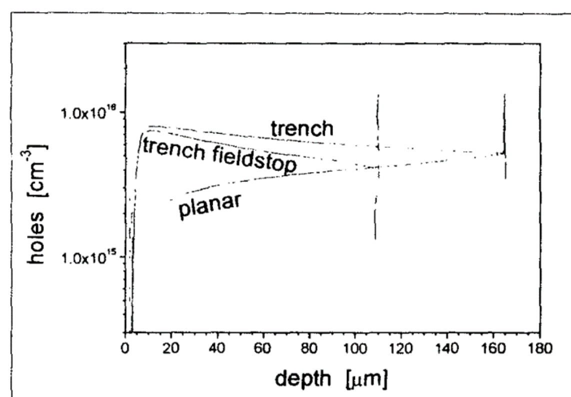

Figure 5-7 p^+ layer thickness optimization [20]

In the Field stop IGBT, thickness of p^+ injection layer is optimized to achieve lower concentrations of holes injected during IGBT turn-off as represented in **Figure 5-7** so as to match doping of n-buffer layer. Since the concentration of holes injected into the n^- drift layer is made almost equal to the concentration of electrons injected into the n^- drift layer, most of the holes recombine with free electrons and only a small fraction of holes remains in the IGBT structure, eliminating most of current tailing in IGBT [20].

When a positive Collector-Emitter Voltage V_{CE} is applied to a trench structure, the inversion channel formed in the p^- base (p-well) is vertical instead of being horizontal like in planar Gate structures. Inversion layer or conduction channel formed with Trench Gate structure has been designed to work with lower channel length L_{ch} and wider channel width W_{ch} and hence lower channel resistance R_{ch} compared to Planar Gate structure [15]. Moreover, the thickness of the n^- drift layer can be optimised to stop the Field at a particular Field-stop voltage thereby achieving lower overall on-state resistance $R_{CE(on)}$ as shown in **Figure 5-8**.

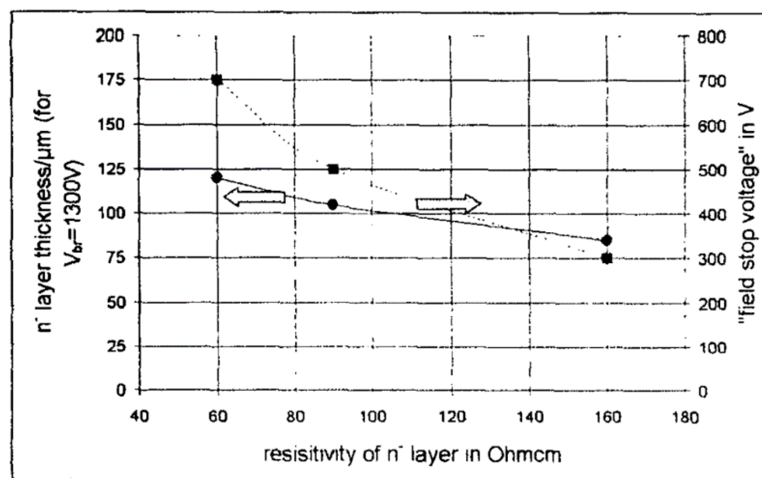

Figure 5-8 n-buffer layer thickness optimisation [20]

5.5.1 SUMMARY

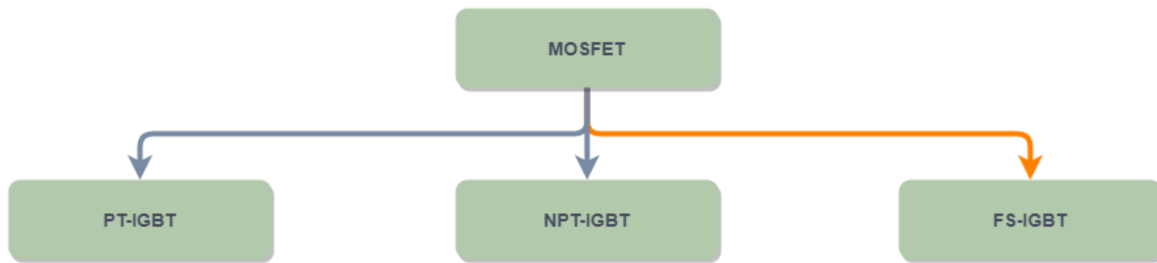

Figure 5-9 Flowchart - Types of IGBT

PT-IGBT has $\boldsymbol{n}^{+}$ buffer layer which has the advantage of lowest on-state resistance $R_{CE(on)}$, lowest on-state voltage drop $V_{CE(on)}$, eliminates current tailing of the IGBT and Highest peaks of Collector current I_c among IGBTs. However, because of the presence of $\boldsymbol{n}^{+}$ buffer layer, PT-IGBT has lower voltage blocking capability and has higher chances of latching. NPT-IGBT on the other hand, does not have $\boldsymbol{n}^{+}$ buffer layer. Hence NPT-IGBT has higher voltage blocking capability and resistant to latch-up. However, it suffers from higher on-state resistance $R_{CE(on)}$, higher voltage drop $V_{CE(on)}$, current tailing and lower peak Collector current I_c. Even though NPT-IGBT has current tailing, the overall switching losses is lower due to its significantly lower magnitude of tailing current. On the other hand, PT-IGBT has much shorter current tailing, however the magnitude of tailing current is significantly larger and hence higher is switching losses.

FS-IGBT is introduced which has a Trench Gate structure and lightly doped n-buffer layer which reduces the on-state resistance $R_{CE(on)}$ of the FS-IGBT. Lower the on-state resistance $R_{CE(on)}$, higher is the peak Collector current I_C. The thickness of the $\boldsymbol{n}^{-}$ region can be adjusted to have better Field Stop Voltage at lower resistance. Higher the field stop voltage, higher is the voltage blocking capability. Moreover, the depth of the $\boldsymbol{p}^{+}$ layer can be optimised to achieve lower concentration of holes remaining in bulk during turn OFF of IGBT this reduceing current tailing.

Among all IGBT technologies, the PT-IGBT has the best capability to achieve highest peak of Collector current I_C lowest on-state resistance and NPT-IGBT has the best capability to achieve highest blocking voltage for the same thickness. However, the Trench Gate Field Stop IGBT combines the advantages of both PT and NPT-IGBTs and hence it is determined as the most balanced switching technology among all IGBT technologies that could provide high Collector current I_C, high blocking voltage, high switching frequency as represented in the flowchart in **Figure 5-9**.

6
OVERALL COMPARISON

In the previous chapters, switching technologies such as MOSFET and IGBT and their types were discussed in detail. Planar N-channel Enhancement SiC MOSFET among all types of MOSFET and Trench Gate FS IGBT among all types of IGBT were considered to be the most promising switching technologies that could deliver high output current, voltage blocking capability and switching frequency. This chapter is dedicated to compare Planar N-channel Enhancement SiC MOSFET and Trench Gate Field Stop IGBT with the rest of IGBT and MOSFET technologies to illustrate the significant advantages of these two devices over the others.

[21] compares Planar SiC MOSFET and Trench FS IGBT with other types of MOSFETs and IGBT of comparable ratings. The ratings of the switches used in this comparison are as follows:

Si Super junction MOSFET (SJMOSFET) - IPW90R120C3 by Infineon – V_{DS} = 900 V, $R_{DS(on)}$ = 0.12 Ω, I_D = 36 A

Si Trench FS IGBT (TFS) - FGA20N120FGD by Fairchild - V_{CE} = 1.2 kV, I_{CE} = 20 A

Si NPT IGBT (NPT) - IRGP20B120U by International Rectifier - V_{CE} = 1.2 kV, I_{CE} = 20 A

SiC Planar MOSFET (SiC) - CMF20120D by Cree - V_{DS} = 1200 V, $R_{DS(on)}$ = 80 mΩ

Si MOSFET (Si MOS8) - APT34M120J by Microsemi - V_{DS} = 1200 V, $R_{DS(on)}$ = 0.3 Ω

6.1 OUTPUT CURRENT

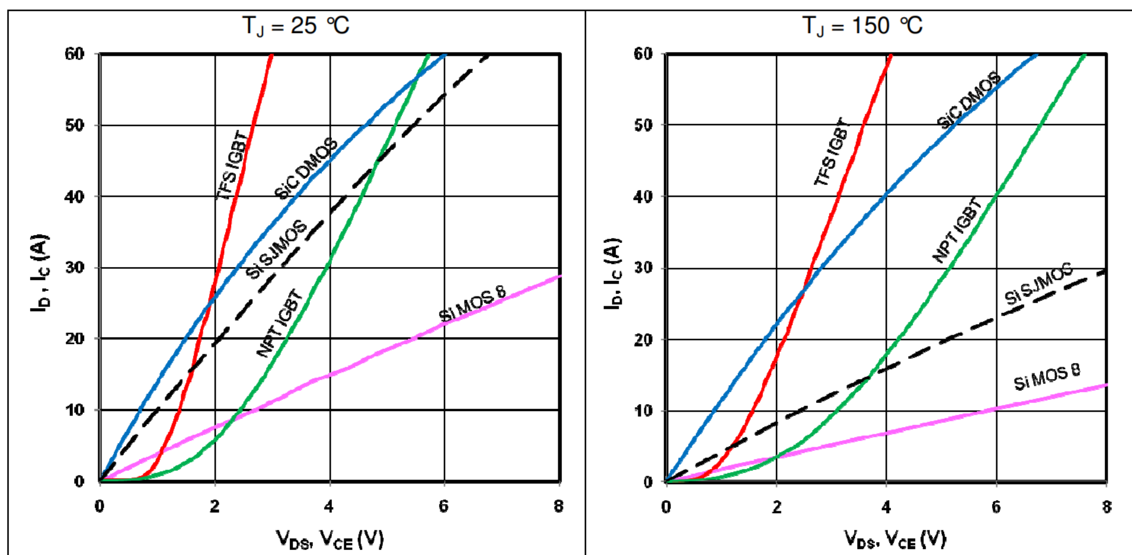

Figure 6-1 Output characteristics comparison [21]

From **Figure 6-1** TFS IGBT has the highest slope of I_C for respective voltage drop across the device during on-state among all the device technologies at both the temperatures (T_j = 25 °C & T_j = 150 °C &) due to its Transconductance. SiC MOSFET exhibits only a slight increase in Drain Source Voltage drop V_{DS} from T_j = 25 °C to T_j = 150 °C due to its excellent thermal properties since on-state resistance $R_{DS(on)}$ increases only 20%. Other devices exhibit fairly higher voltage drop with increase in temperature.

6.2 LEAKAGE CURRENT

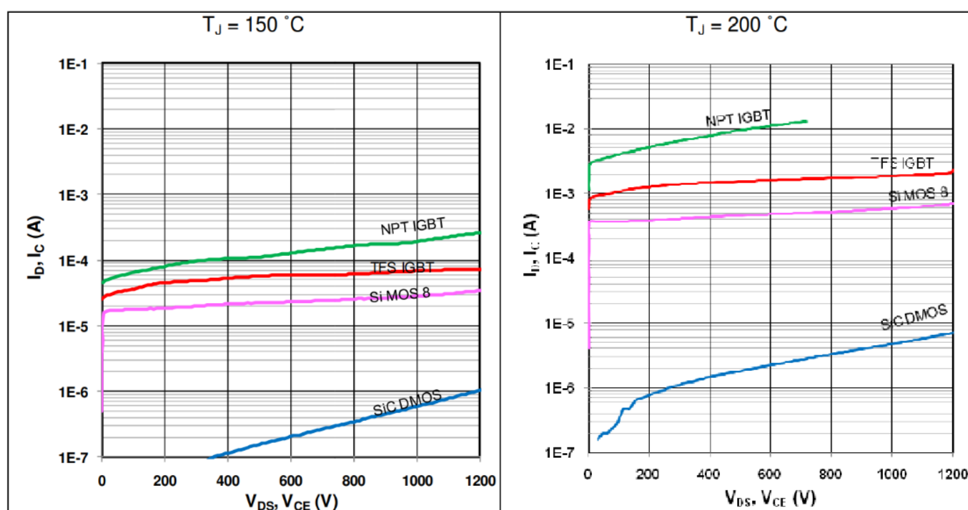

Figure 6-2 Leakage current comparison [21]

From **Figure 6-2** SiC MOSFET exhibits the least leakage current $I_{D,leakage}$ among all devices. This is attributed to its higher bandgap compared to other Si devices. At T_j = 150 °C, SiC MOSFET exhibits at least 20 times lower leakage current. However, at T_j = 200 °C, SiC exhibits at least 100 times lower leakage current compared to all other Si devices. Whereas the leakage currents of other Si Devices have increased dramatically to values that cannot be acceptable with increase in temperature.

6.3 GATE CHARGE AND SWITCHING LOSSES

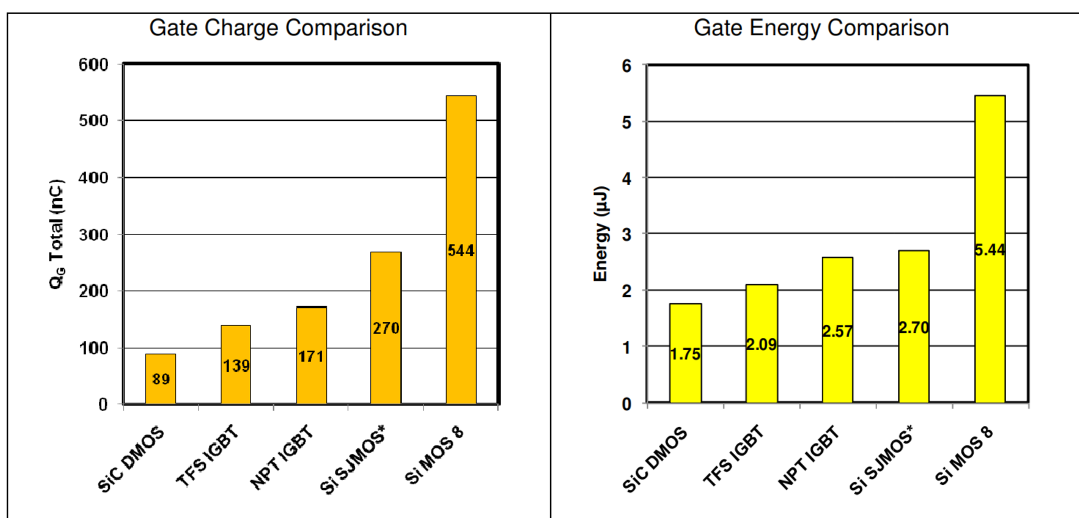

Figure 6-3 Gate charge and Gate Energy comparison [21]

From **Figure 6-3,** SiC MOSFET shows the least amount of Gate charge Q_G required (89 nC) and energy consumed (1.75 µJ) during charging the Gate Source terminals as the conduction channel is formed during this time interval. This is attributed to the lowest input capacitance C_{ISS} of the SiC MOSFET compared to all other Si devices. The second least amount of Gate charge Q_G required (139 nC) and energy consumed (2.09 µJ) is the Trench FS IGBT. Hence these two devices achieve least switching times and hence highest switching frequencies among all the devices.

6.4 SWITCHING LOSSES

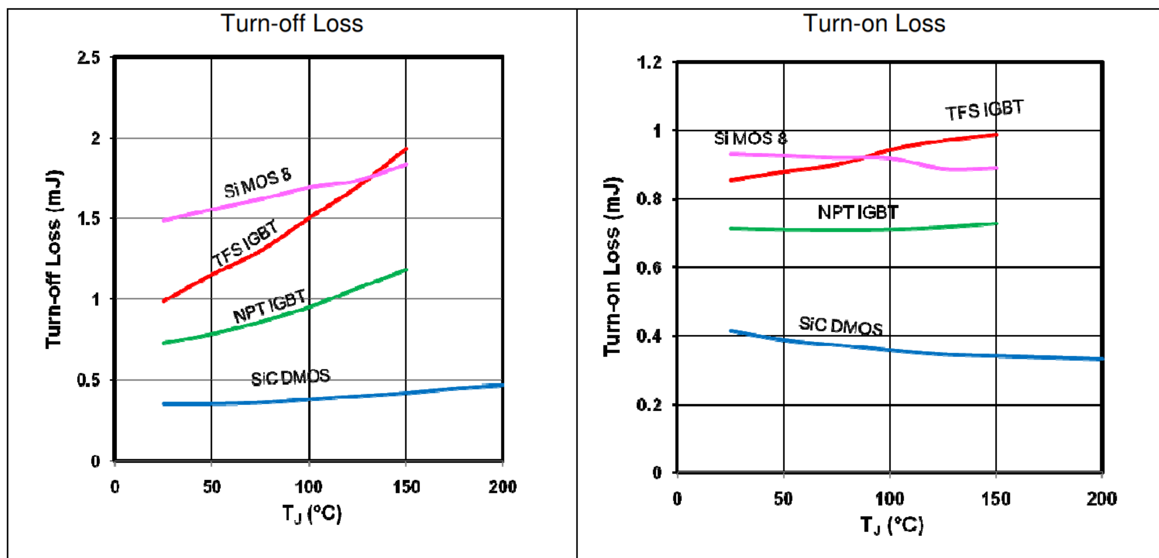

Figure 6-4 Switching Losses comparison [21]

From **Figure 6-4**, Turn-off losses of all the devices increase as the junction T_j temperature increases. TFS IGBT exhibit highest turn-off losses because of recombination of holes with electrons during turn-off to eliminate current tailing. Moreover, this process is temperature sensitive and as temperature increases, the losses increase significantly. However, the NPT IGBT has higher conduction losses compared to Trench FS IGBT as it has higher on-state resistance $R_{CE(on)}$ and voltage drop $V_{CE(sat)}$. SiC MOSFET exhibits the least switching losses among all the switching technologies.

7
FACTORS AFFECTING DRAIN CURRENT

7.1 PULSE CURRENT TEST CIRCUIT

From the previous section of the thesis, that is Literature review, working principle and functioning of various Power Electronic switching technologies such as MOSFET and IGBT and their types were thoroughly discussed. Each type of the switching technology was compared to the other types and N-channel Enhancement Planar SiC MOSFET among all MOSFET and Trench Gate FS IGBT among all IGBT were considered to be the promising switching technologies to produce very high peaks of output current, blocking voltage and switching frequency.

This section of the thesis elaborates the pulse current test circuit shown in Figure **7-1** and various factors that affects peak magnitude of drain current I_D and how they are manipulated to our advantage to extract highest output current from the Device Under Test.

TU Delft has built a test circuit of TO-247-3 package to investigate Pulse Current capabilities of Power Electronic devices under Short Circuit conditions which is shown in Figure **7-1**.

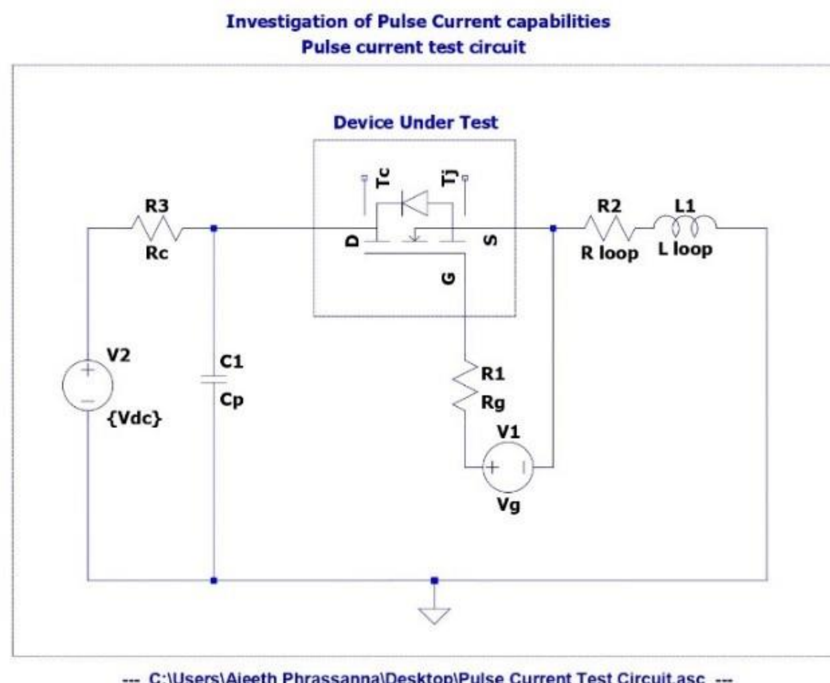

Figure 7-1 Pulse current test circuit

As represented in Figure **7-1**, the test circuit has a variable input DC supply voltage V_{DC}, Charging resistance R_c to charge the capacitor C_p, the auxiliary loop has the Device Under Test (DUT), since the test circuit short circuits the Device Under Test, it has very low values of loop resistance R_{loop} and loop inductance L_{loop} to generate pulse currents of very high magnitude. The DUT is driven by a Gate Source Voltage V_g and the Gate circuit has resistance R_g. The capacitor C_p is charged for

an initial voltage of V_{DC} while the MOSFET is blocking the voltage. When the Gate pulse of very short duration in order of few µs is applied to the DUT, the DUT starts to conduct and the capacitor C_p discharges short pulses of currents of very high magnitude into the auxiliary loop.

The equations regarding different loops of the pulse current test circuit can be given as follows:

The equation of capacitor charging loop can be given as,

$$V_{DC} = R_c i_c + \frac{1}{C_p}\int_0^{t_c} i_c \; dt \qquad \text{Equation (7.1)}$$

Where, i_c is the instantaneous charging current and t_c is the charging time. The equation of auxiliary loop can be given as,

$$V_{DC} = R_{loop} i_D(t) + V_{DS(on)} + L_{loop}\frac{di_D(t)}{dt} + \frac{1}{C_p}\int_0^{t_{on}} i_D(t) \; dt \qquad \text{Equation (7.2)}$$

Where $i_D(t)$ is the instantaneous drain current, t_{on} is the Gate pulse duration and $V_{DS(on)}$ is the on-state voltage drop across the DUT. The on-state voltage drop across the DUT $V_{DS(on)}$ is very low and hence it is neglected. Thus, the instantaneous drain current is obtained as,

$$I_D(t) = \frac{V_{DC}}{\omega L_{loop}} e^{-\gamma t \sin(\omega t)} \qquad \text{Equation (7.3)}$$

Where,

$$\gamma = \frac{R_{loop}}{2\, L_{loop}} \qquad \text{Equation (7.4)}$$

And

$$\omega = \sqrt{\frac{1}{L_{loop}\, C_p} - \frac{{R_{loop}}^2}{4\, {L_{loop}}^2}} \qquad \text{Equation (7.5)}$$

7.2 FACTORS AFFECTING PEAK DRAIN CURRENT I_D

The peak value of the drain current I_D is affected by various factors such as Gate Source Voltage V_{GS} and Drain Source Voltage V_{DS} directly. However, Gate circuit resistance R_g indirectly affects the rate of rise of drain current I_D (slope). Also, longer the Gate pulse duration t_{on} higher is the energy through the DUT and hence higher peak drain current I_D can be achieved [23].

7.2.1 GATE SOURCE VOLTAGE V_{GS}

The magnitude of Gate Source Voltage V_{GS} directly affects the conduction channel parameters such as width W and length L. Higher the V_{GS} wider is the channel width W and more volume of electrons can pass through the channel. Hence peak drain current I_D is very sensitive to any changes in Gate Source Voltage V_{GS}. Moreover, higher the Gate Source Voltage V_{GS} a greater number of free electrons are attracted at the accumulation region below the oxide layer which significantly drops the on-state resistance $R_{DS(on)}$. Hence higher magnitudes of drain current can be achieved. [23]

plots a graph of changes in drain current I_D with respect to changes in Gate Source Voltage V_{GS} in a 1.2 kV/180 A SiC MOSFET manufacture by Rohm at a constant Drain Source Voltage V_{DS} = 800 V and Gate circuit resistance R_g = 11 Ω in **Figure 7-2**.

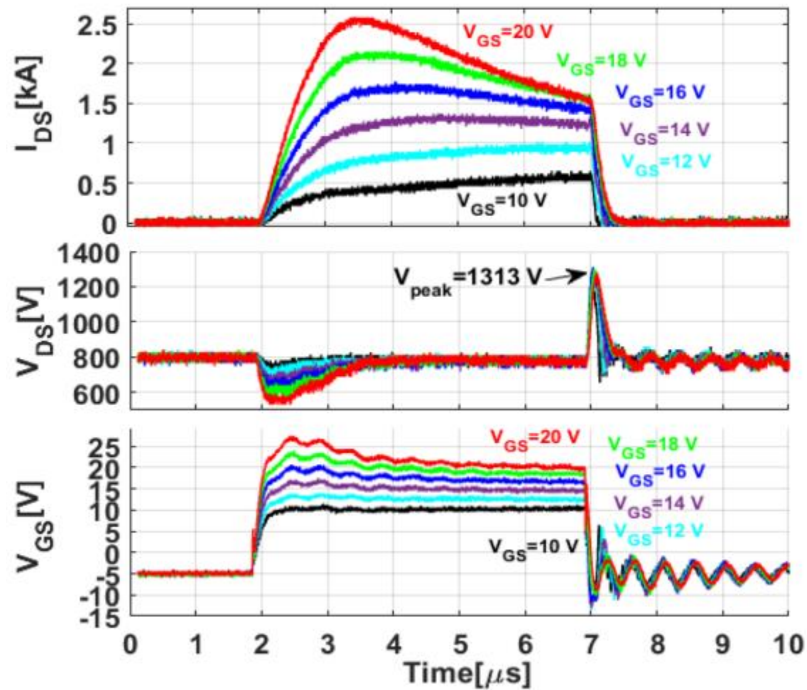

Figure 7-2 I_D for different V_{GS}; V_{DS} = 800 V; R_G= 11 t_{on} = 5 μ sec [23]

From **Figure 7-2**, it can be seen that for a $\boldsymbol{V_{GS}}$ = 10 V the conduction channel is not completely formed which reflects in the lower magnitude of drain current $\boldsymbol{I_D}$ however, because of high voltage applied across the bulk $\boldsymbol{V_{DS}}$, more energy is dissipated in the bulk. Thus, the mobility of electrons $\boldsymbol{\mu_n}$ increases as the temperature of the device increases. When $\boldsymbol{V_{GS}}$ is gradually increased to $\boldsymbol{V_{GS}}$ = 20 V, $\boldsymbol{I_D}$ can reach a peak value $\boldsymbol{I_D}$ = 2.5 kA meaning the conduction channel is completely formed.

However, higher the applied V_{GS} higher is the overshoot in turn-off voltage across Drain and Source terminals $V_{DS(off)}$. Higher V_{GS}, higher is $\frac{dI_D}{dt}$. Hence, according to Turn-off characteristics of MOSFET, high $\frac{dI_D}{dt}$ induces voltage drop across parasitic inductances of the circuit. For a V_{GS} = 20 V, the overshoot obtained is $V_{DS(off)}$ = 1313 V which is greater than the breakdown voltage of the device BV_{DSS} however it is momentary [23].

7.2.2 GATE RESISTANCE R_G

Gate resistance $\boldsymbol{R_G}$ is directly related to the time constant of the Gate circuit as $\tau = \boldsymbol{R_G\ C_{GS}}$. Lower the value of $\boldsymbol{R_G}$, faster is the time constant τ and hence the conduction channel formation is faster. Thus, steeper slopes of drain current $\boldsymbol{I_D}$ can be achieved. Despite the advantage of having steeper slopes of $\boldsymbol{I_D}$, lower values of $\boldsymbol{R_G}$ leads to higher overshoots of $\boldsymbol{V_{DS}}$ during turn-off. The reason behind this is, during Turn-off of MOSFET, $\boldsymbol{V_{DS}}$ increases with a time constant $\tau = \boldsymbol{R_G\ (C_{GD} + C_{GS})}$. Lower the value of $\boldsymbol{R_G}$, lower is the time constant τ and hence $\boldsymbol{V_{DS}}$ rises faster with a high overshoot. To tackle such an overshoot in $\boldsymbol{V_{DS(off)}}$, two different Gate resistances $\boldsymbol{R'_G}$ and $\boldsymbol{R_G}$ are employed in the Gate circuit as shown in **Figure 7-3** [23].

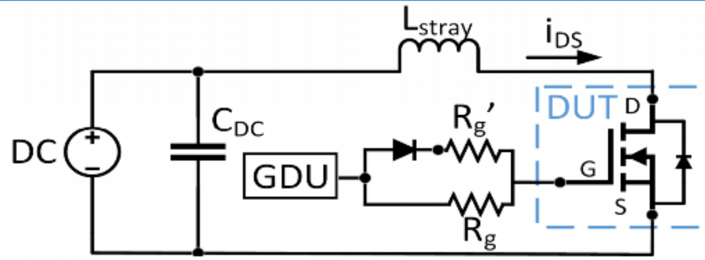

Figure 7-3 Resistances R_G' and R_G in Gate circuit [23]

From **Figure 7-3**, by adding a diode in the Gate circuit, a very low value of Gate resistance can be obtained during t_{on} as the diode is in Forward bias and the overall Gate resistance becomes the parallel combination of R_G' and R_G [23]. During t_{off} the Diode is in reverse bias and hence R_G' is cut-off from the Gate circuit thereby leaving a high resistance R_G during t_{off}. Thus, higher resistance R_G during t_{off} increasing the time constant τ of V_{DS} reducing overshoots. This can be understood better with the **Figure 7-4** [23].

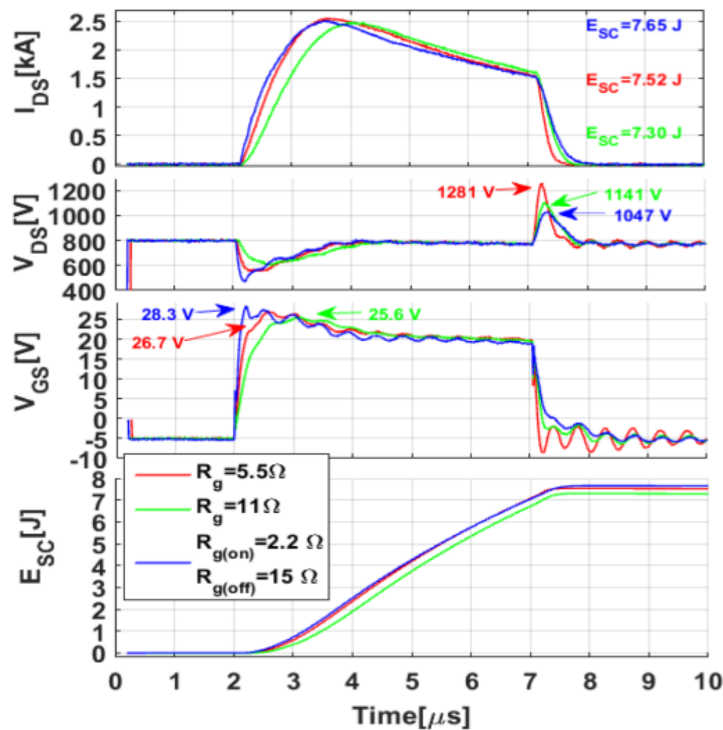

Figure 7-4 I_D and V_{DS} for different R_G [23]

From **Figure 7-4**, for a Gate resistance of R_G = 5.5 Ω, I_D peak value is achieved faster however because of steep slope of I_D, highest overshoots of V_{DS} occurs for 1281 V. However, for Gate resistance pair R_G' = 2.5 Ω and R_G = 15 Ω in figure, the resultant on-state and off-state resistances are $R_{g(on)}$ = 2.2 Ω and $R_{g(off)}$ = 15 Ω respectively in **Figure 7-4**. For such a resistance pair of R_G' = 2.5 Ω and R_G = 15 Ω, the slope of drain current is the fastest among all the Gate resistances R_G moreover, the overshoots of V_{DS} becomes the lowest at V_{DS} = 1047 V. However, the Gate Source Voltage V_{GS} attains the highest peak value of V_{GS} = 28.3 V. Care has to be taken that the Gate Source Voltage V_{GS} should not rise beyond maximum value $V_{GS(max)}$ [23]. Moreover, for the Gate resistance pair R_G' = 2.5 Ω and R_G = 15 Ω, the Short Circuit Energy E_{sc} conducted through the SiC MOSFET is the highest among all the resistance combinations. This happens because of the lowest

on-state resistance of $R_{g(on)}$ = 2.2 Ω, the Drain current I_D reaches peak faster and hence the area under Drain Current I_D is the highest among all resistance combinations.

Since Short Circuit Energy is related as,

$$E_{sc} = \int_0^{t_{on}} V_{DS}\ I_D\ dt \qquad \text{Equation (7.6)}$$

because of largest area under the current curve I_D, resistance pair of R'_G = 2.5 Ω and R_G = 15 Ω extracts highest Short Circuit Energy E_{sc} of 7.65 J from SiC MOSFET.

7.2.3 DRAIN SOURCE VOLTAGE V_{DS}

The magnitude of Drain Current I_D is directly related to Drain Source Voltage V_{DS} from **Equation (2.2**. However, when the SiC MOSFET is operating in linear region, it acts like a linear resistor of on-state resistance $R_{ds(on)}$. Hence the magnitude of Drain Current is given as

$$I_D = \frac{V_{DS}}{R_{ds(on)} + R_{Loop}} \qquad \text{Equation (7.7)}$$

The peak magnitude of Drain Current $I_{D,peak}$ is always achieved in the linear mode of operation since the on-state resistance $R_{ds(on)}$ is the lowest during linear mode. **Figure 7-5** represents how peak current I_D changes with respect to change in V_{DS}:

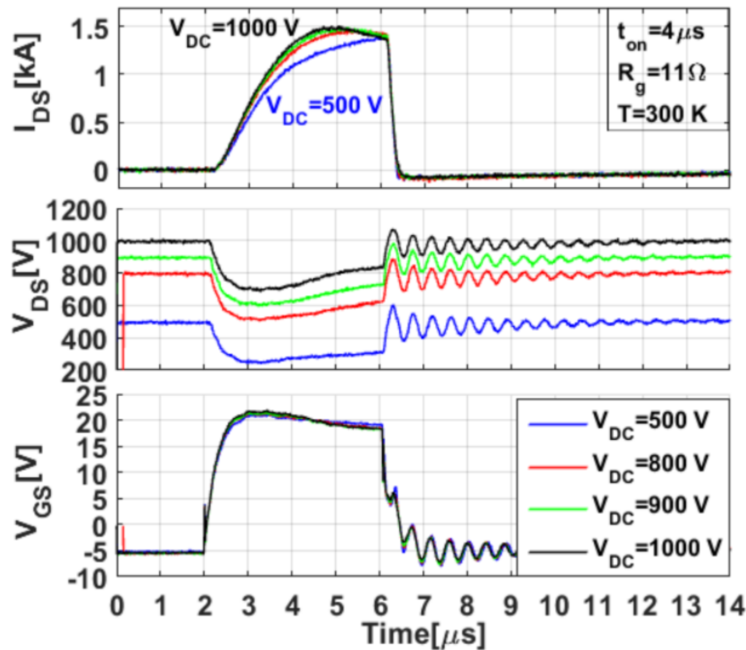

Figure 7-5 V_{DS} vs I_D for a constant V_{GS} = 20 V t_{on} = 4 μ sec [23]

From the **Figure 7-5**, for V_{DS} = 500 V, the Drain current I_D starts increasing gradually as the more energy is dissipated in the bulk of the device. The mobility of electrons μ_n increases until the peak current is reached. After the peak drain current is achieved, the channel mobility drops as the on-resistance of the device increases significantly.

For greater voltages such as V_{DS} 800 V, 1000 V the rate of rise in Drain current increases and the peak Drain current I_D is reached in much shorter time [23].

7.3 PEAK DRAIN CURRENT I_D

In the previous section, the Pulse Current test circuit and the factors affecting peak drain current $I_{D,peak}$ have been discussed. This section deals with how to utilize those factors such as Gate Source Voltage V_{GS}, Drain Source Voltage V_{DS} and Gate circuit resistance R_g to achieve peak drain current $I_{D,peak}$ of SiC MOSFET.

7.3.1 METHODS TO ACHIEVE PEAK DRAIN CURRENT I_D

The theoretical limit of peak drain current $I_{D,peak}$ of any power electronic device can be derived from its Critical Energy E_c. However, in reality, this theoretical limit of peak drain current $I_{D,peak}$ may not be achieved since the Drain current I_D could already be saturated well before the Critical Energy E_c of device is reached. Critical energy E_c of a Power Electronic device is the maximum amount of energy it can conduct before it fails.

Similar to Short Circuit Energy of **Equation (7.6)**, Critical Energy can be expressed as,

$$E_{cr} = \int_0^{t_{on}} V_{DS}\ I_D\ dt \qquad \text{Equation (7.8)}$$

$$E_{cr} = V_{DS}\ I_D\ t_{on} \qquad \text{Equation (7.9)}$$

From **Equation (7.9)** at a constant Gate Source Voltage V_{GS} and Drain Source Voltage V_{DS}, the pulse width t_{on} is increased until the Power Electronic device fails, marking its critical energy E_{cr}.

By substituting the found critical energy E_{cr} into the **Equation (7.9)**, for specific values of Drain Source Voltage V_{DS} and pulse width t_{on}, the theoretical limit of peak drain current $I_{D,peak}$ can be calculated.

This concept is well explained by **Figure 7-6** below:

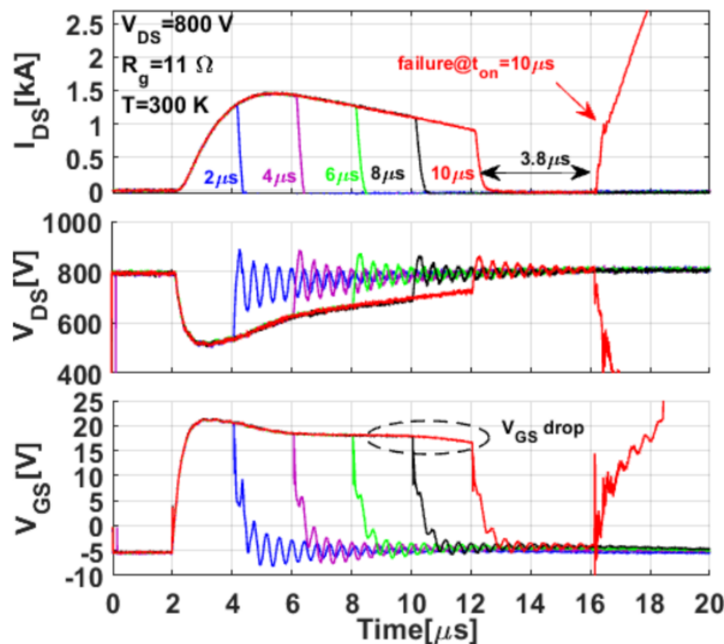

Figure 7-6 Current and voltage waveforms for critical energy E_{cr} calculation at V_{DS} = 800 V and V_{GS} = 20 V [23]

From **Figure 7-6**, at V_{DS} = 800 V and V_{GS} = 20 V, pulse width t_{on} is increased in steps of 2 μs. At 5 μs, peak drain current $I_{D,peak}$ of 1.47 kA was achieved. The pulse width t_{on} is increased further in steps until 10 μs and the Gate pulse is turned off at a drain current of I_D = 0.86 kA.

However, 3.8 μs after the Gate pulse is turned-off, Drain current I_D continues to rise uncontrollably and V_{DS} plummeting to zero even though no Gate pulse is applied to the Power Electronic device. This signifies that the SiC MOSFET was able to withstand a short circuit for 10 μs and after which it has reached its Critical Energy limit E_{cr}.

Before the occurrence of failure, from the **Figure 7-6**, a slight decrease of V_{GS} from 20 V to 18 V can be observed indicating leakage current in the Gate circuit. This is caused because of tunneling mechanism [10] of charge carriers (electrons) from SiO_2 to the Metallic Gate terminal causing Gate Oxide layer to breakdown resulting in short circuiting all the terminals together leading to thermal runaway [23]. Thus, the SiC MOSFET fails.

By substituting respective values of V_{DS}, I_D and t_{on} in **Equation (7.9)**, the Critical Energy E_{cr} of the SiC MOSFET is found to be 7.3 J. Thus, by substituting Critical Energy E_{cr} again in **Equation (7.9)**, for known values of V_{DS} and t_{on}, maximum achievable peak drain current I_D can be calculated for specific values of V_{GS} [23].

7.3.2 SAFE OPERATING AREA (SOA)

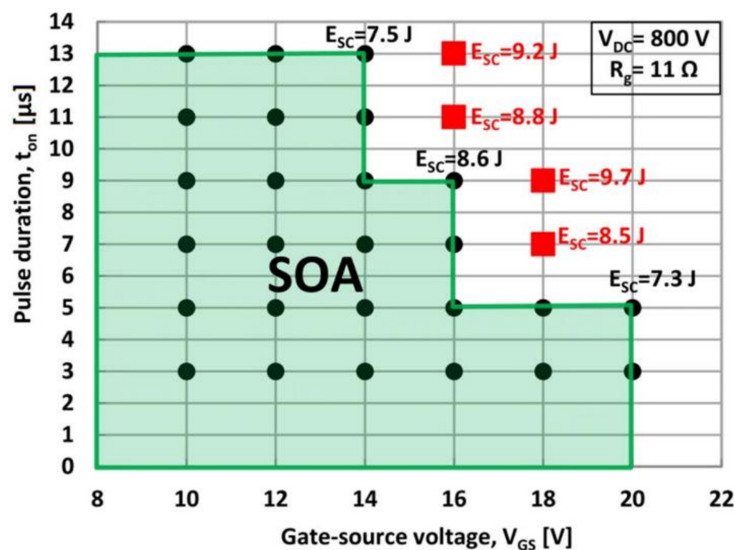

Figure 7-7 Safe Operating Area of SiC MOSFET [23]

Finally, Safe operating area is marked as shown in **Figure 7-7** for various values of Gate pulse width t_{on} and Gate Source Voltage V_{GS}. Pulse width t_{on} is gradually increased from 3 μs until 13 μ sec in steps of 2 μs while V_{GS} is varied between 10 V and 20 V. Black dots represent device passed the test while red squared represent device failed the test [23].

From figure, until t_{on} = 5 μs all the devices passed the test for a maximum V_{GS} of 20 V. It can be observed that when pulse width t_{on} is increased the maximum usable V_{GS} is decreasing marking the limits of Critical Energy E_{cr} of the device. At t_{on} = 9 μs and V_{GS} = 16 V, maximum Short Circuit Energy E_{cr} of 8.6 J for any values of t_{on} and V_{GS} was achieved. At maximum Short Circuit Energy E_{cr} of 8.6 J, for specific values of V_{DS} and t_{on}, maximum peak Drain current I_D that can be achieved for this particular SiC MOSFET [23].

7.4 FAILURE INVESTIGATION OF THE DEVICE

The Power Electronic devices that failed the test have been investigated for the reason of failure and the waveforms are analyzed from **Figure 7-8**. The most common failure process that were to be observed in SiC MOSFETs are thermal runaway.

From **Figure 7-8**, at the end of conduction of Drain current I_D, a small dip in the Gate Source voltage ΔV_{GS} at the end of each Gate pulse can be observed. This is caused due to Gate-Source leakage current causing the Gate oxide layer to degrade, leading to Gate-Source short circuit.

During the Gate-Source short circuit, a significant amount of leakage current flows between Drain and Source terminals leading to degradation of the bulk resulting in uncontrolled rise in Drain currents I_D shown in **Figure 7-8**. This results in thermal runaway of the SiC MOSFET. This failure mechanism is called as delayed failure.

The Gate-Source leakage current occurs due to tunnelling mechanism of electrons from the trap states at the interface between SiC and SiO_2 into metallic Gate terminal. This tunnelling mechanism is called as Fowler Nordheim tunnelling.

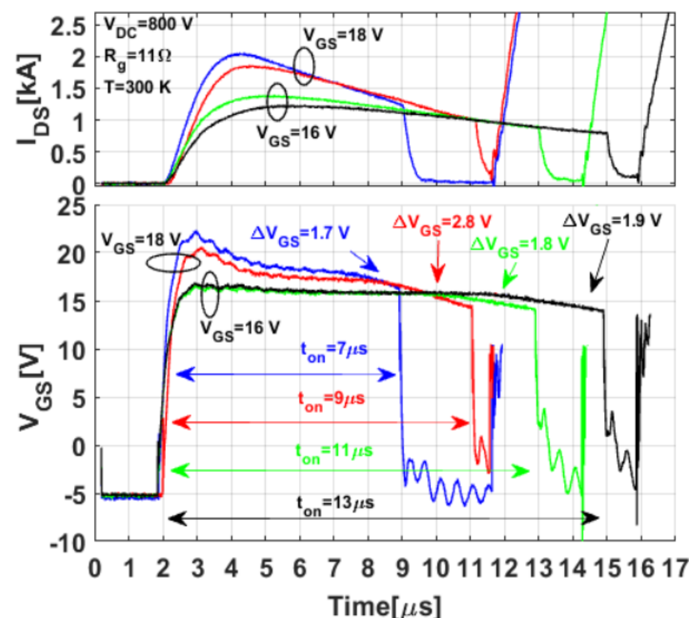

Figure 7-8 SiC MOSFET Failure investigation [23]

7.4.1 FOWLER NORDHEIM TUNNELING

Figure 7-9 explains how Fowler-Nordheim tunnelling works. **Figure 7-9** shows the energy band diagram at the SiC-SiO_2 interface. E_i represents intrinsic energy level, E_v represents energy level of the valence band and E_c represents energy level of conduction band. ⍰$_c$ is the barrier between the conduction band edges E_c of SiC and SiO_2 and ⍰$_F$ is the barrier between the fermi level E_f of SiC and conduction band E_c of SiO_2.

At the interface between SiC and SiO_2 materials, the density of trap states called the interface states is very high. When a positive Gate-Source voltage V_{GS} is applied, some of the electrons which are responsible for creating the conduction channel get trapped in these interface states. As a result, the barrier ⍰$_F$ between the fermi level E_f of SiC and conduction band E_c of SiO_2 shrinks to ⍰$_{eff}$.

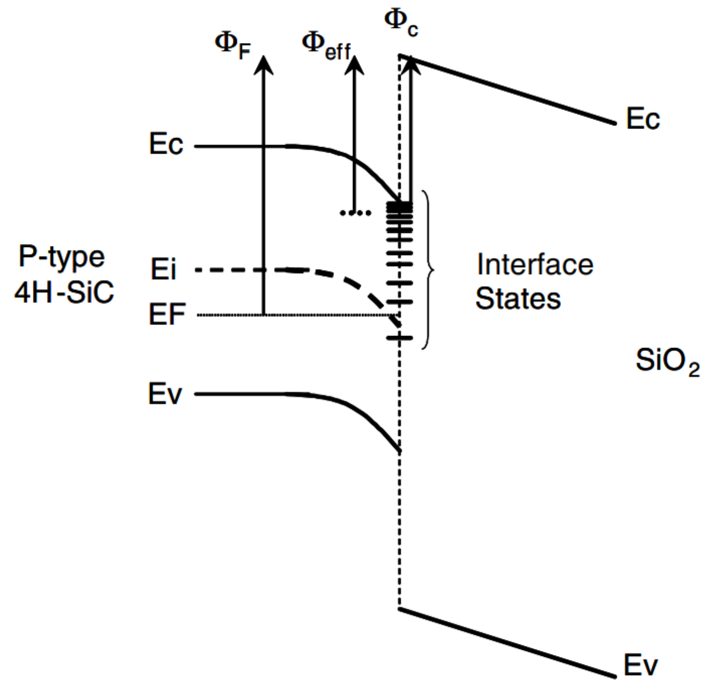

Figure 7-9 Energy band diagram SiC-SO_2 interface [10]

When the SiC MOSFET starts conducting high Drain currents I_D because of the application of large Drain Source voltage V_{DS}, the bulk reaches higher temperatures and the electric field intensity is very high near the conduction channel.

Because of high temperature and high electric field intensity at the SiC-SiO_2 interface, the electrons at the interface states gain energy and tunnel through the SiO_2 into the metallic Gate terminal overcoming the effective barrier Φ_{eff} between the fermi level E_f of SiC and conduction band E_c of SiO_2. This causes a large leakage current between Gate and Source terminals resulting in Gate-Source terminal short circuit leading to degradation of the SiO_2 dielectric material. This causes a voltage dip in Gate-Source voltage ΔV_{GS} as represented by **Figure 7-8**.

However, in Si device technologies such as IGBT and MOSFET, the density of interface states existing between Si substrate and SiO_2 dielectric is far lower compared to that of the SiC MOSFET. Hence delayed failure does not happen in devices with Si substrate as Fowler Nordheim tunnelling is nearly absent in Si devices. As the Si reaches its critical energy, the bulk degenerates leading to short circuit between Drain and Source terminals. This leads to uncontrolled rise in Drain current I_D resulting in thermal run-away of the device.

8

PULSE CURRENT TEST

8.1 SPICE MODEL OF DUT

From the above section, factors affecting peak Drain current $I_{D,peak}$, procedure to achieve peak Drain current $I_{D,peak}$, safe operating area and failure investigation were discussed. The most common mode of failure of SiC MOSFET was determined to be Gate terminal short circuit which leads to destruction of Gate terminal. During Gate Source short circuit, a significant leakage current flowing between Drain and Source terminals results in the thermal run-away of the MOSFET. This failure mechanism is called as delayed failure. However, in Si devices, the usual failure mechanism is Drain Source terminals short circuit without involving Gate Source short circuit, leading to thermal run-away.

Before performing Pulse Current test of the Power Electronic devices practically, the Pulse Current test circuit is simulated in Cadence P-spice simulation software along with Device Under Test to verify proper functioning of the built test circuit and to study the performance indices of the Device Under Test such as Peak Drain current $I_{D,peak}$, overshoot in Drain Source Voltage V_{DS} and corresponding waveform of Gate Source voltage V_{GS}. Hence the spice simulation model of Device Under Test is obtained from the website of manufacturer. The spice model shown in **Figure 8-1** SiC MOSFET C2M0160120D manufactured by Wolfspeed is obtained from the website for simulations and respective ratings of the device are listed in the **Table 8-1** as:

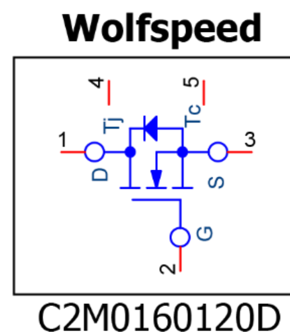

Figure 8-1 Pspice model of SiC MOSFET

Table 8-1 SiC MOSFET used in simulation

DEVICE	$I_{D,rated}$	$V_{DS,rated}$	$R_{DS(on)}$	$V_{GS(op)}$	$V_{GS(max)}$
C2M0160120D	18 A	1.2 kV	160 mΩ	-5/20 V	-10/25 V

8.2 PULSE CURRENT TEST SETUP

The key elements of the Pulse Current Test setup are namely;

1. Power Board
2. Gate Driver
3. Device Under Test (DUT)
4. Function Generator (FG)
5. Oscilloscope
6. Variable DC Power Supply V_{DC}
7. Measuring probes to measure V_{GS}, V_{DS} and I_D.

A step-by-step procedure to build up the Pulse Current Test Setup is elaborated in the sub-section below which begins with Power Board.

8.2.1 POWER BOARD

The Power board shown in **Figure 8-2**Error! Reference source not found. represents the Pulse Current test circuit. It has input supply terminals DC+ and DC- to which a variable DC voltage source is connected to power the test circuit. The Power board has 9 capacitances each of 22 µF and 198 µF on total connected across the input supply and Device Under Test (DUT). These capacitances produce the discharge pulse necessary to test the DUT. The Power board has a socket into which the Device Under Test is inserted, which is connected across the supply voltage and the capacitances. A 12 V input DC supply is given for the power board to function properly. The Power board has a slot across Gate and Source terminals into which the Gate driver is inserted.

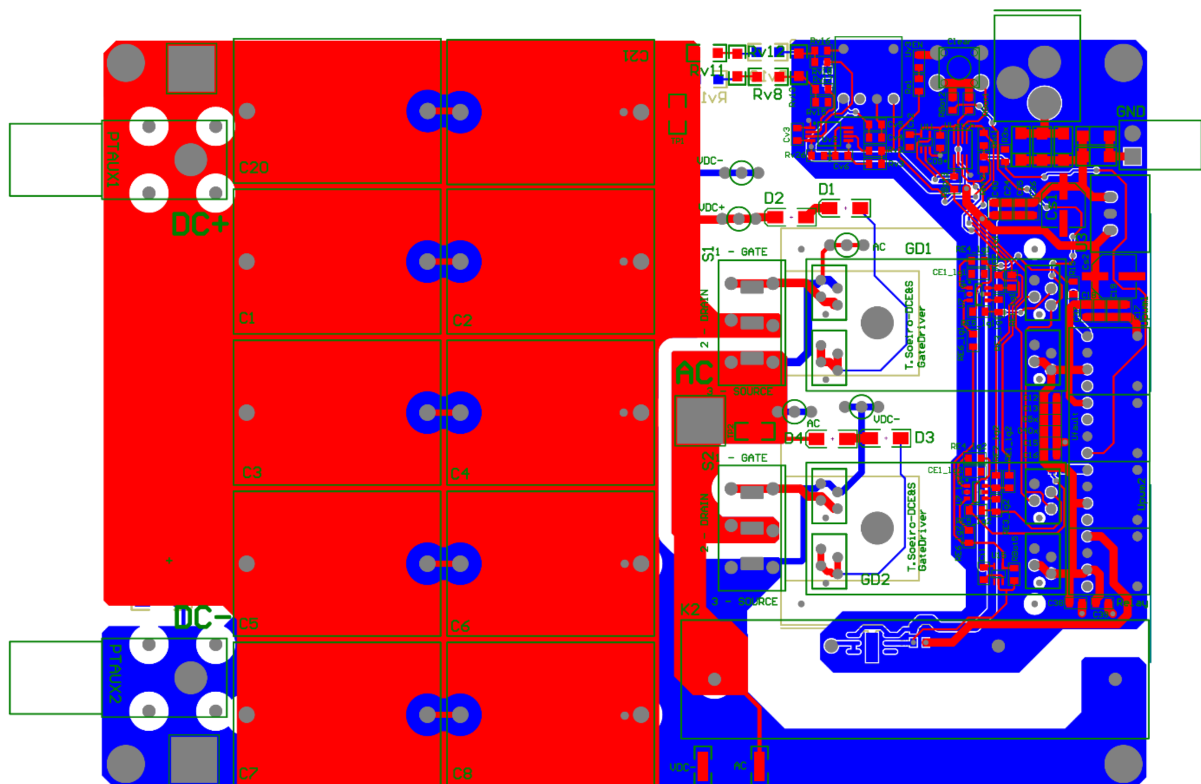

Figure 8-2 Power Board of the Pulse Current test circuit

8.2.2 GATE DRIVER

Figure 8-3 represents the Gate driver used in this Pulse Current Test. The Gate driver has a DC-DC converter which converts 5 V input DC voltage into Gate Source Voltage necessary to drive the DUT. The Gate driver is powered by ADuM4135 chip manufactured by analog devices. The most important feature of the ADuM4135 chip is the Desaturation pin. It is a short circuit protection feature that senses high Drain current I_D across Drain and Source terminals of the DUT during Short circuit conditions and trips the Gate Source Voltage V_{GS}. Disabling this desaturation protection allows SiC MOSFET to operate in high Drain current range. The Gate driver allows to use two different Gate resistances during on time and off time, R'_G and R_G respectively. Thus, the Gate driver helps to achieve both high peaks of Drain current I_D and lower overshoots in Drain Source Voltage V_{DS} during off time.

Figure 8-3 Gate Driver

8.2.3 TEST SETUP PROCEDURE

1. Insert the Gate driver into the Gate Driver slot of the Power board.
2. Insert the Device Under Test into the DUT slot.
3. Connect a variable DC source V across DC+ and DC- terminals of the Power board.
4. Connect the Gate driver input pin to the Function Generator.
5. The Function Generator is operated in Pulse mode (single pulse) with manual triggering of output voltage 5 V rms with a pulse width of $t_{on} = 4\ \mu s$.
6. Insert 12 V input supply to the power board which ensures proper working of the board.
7. Connect measuring probes to the Oscilloscope that monitor Gate Source Voltage V_{GS}, Drain Source Voltage V_{DS} and Drain current I_D of the DUT.
8. Check the following settings on the oscilloscope:
    a. Amplifications are set according to sensitivity of measuring probes and bandwidth for each channel.
    b. Trigger mode is set to manual and triggering channel is set to Gate pulse.
    c. Horizontal and vertical placement of each channel is adjusted so that all waveforms are clearly visible.

The Pulse Current Test Setup is complete as shown in **Figure 8-4** and is ready to perform Pulse Current Test. Various types of IGBT and MOSFET are subjected to Pulse Current Test. The performance of each device is studied and compared to one another to determine the device technology that delivers highest Peak pulse currents. The Power Electronic devices that are subjected to Pulse Current Test are listed in **Table 8-2** along with their ratings.

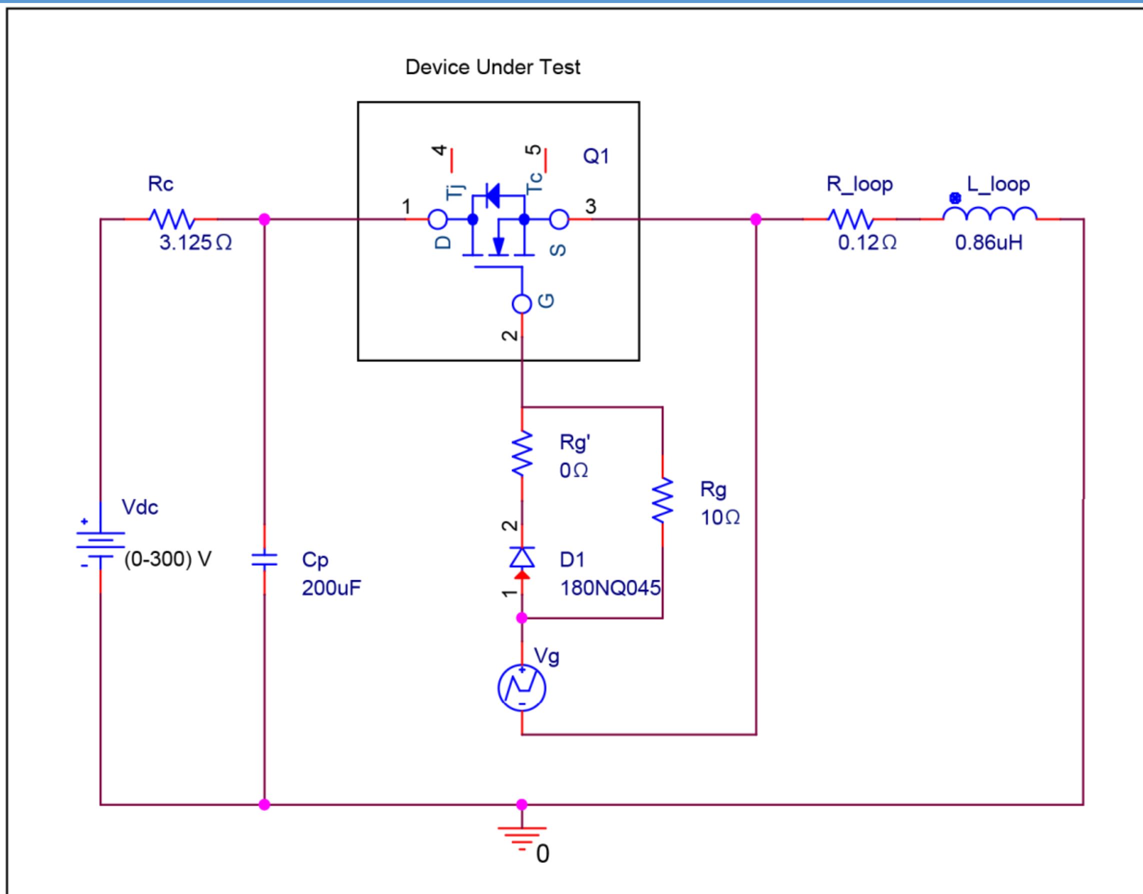

Figure 8-4 Pulse Current Test circuit schematics

DEVICE	TYPE	$I_{D,rated}$	$V_{DS,rated}$	$V_{GS(op)}$	$V_{GS(max)}$
C2M0160120D	SiC MOSFET	18 A	1.2 kV	-5/20 V	-10/25 V
C3M0075120D	SiC MOSFET	30 A	1.2 kV	-4/15 V	-8/19 V
C3M0080120D	SiC MOSFET	36 A	1.2 kV	-4/15 V	-8/19 V
IPW90R120C3	Si MOSFET	36 A	900 V	± 20 V	± 30 V
SGW25N120	NPT IGBT	46 A	1.2 kV	± 20 V	± 30 V
IHW40N120R5	FS IGBT	80 A	1.2 kV	± 20 V	± 30 V
C3M0016120D	SiC MOSFET	81 A	1.2 kV	-4/15 V	-8/19 V
IXGH24N170	NPT IGBT	50 A	1.7 kV	± 20 V	± 30 V
IXBH20N300	NPT IGBT	50 A	3 kV	± 20 V	± 30 V

Table 8-2 Power Electronic devices used for Pulse Current Test

8.3 PULSE CURRENT TEST

Pulse Current Test is performed by inserting Device Under Test in the circuit shown in **Figure 8-4**. As discussed earlier, when no Gate pulse V_g is applied to the DUT, the device is in cut-off region. It blocks the Supply voltage given across its Drain and Source terminals. The capacitor C_p is charged to V_{DC} through charging resistance R_c. When a Gate pulse V_g is applied across the DUT, it starts to conduct and the capacitor C_p discharges stored energy into the auxiliary loop. This test is called as Pulse Current Test and it determines the peak Drain current I_D that can be conducted by the DUT. The Power Electronic devices are brought to their Peak Pulse Current limits in two ways namely,

1. Increasing Drain Source Voltage V_{DS} and
2. Increasing Gate Source Voltage V_{GS}

8.3.1 SIMULATION

SiC MOSFET - C2M0160120D is simulated in Pspice software for Drain Source Voltage V_{DS} Test at constant Gate Source Voltage V_{GS} = 20/-5 V since thickness of conduction channel attains its optimal thickness at V_{GS} = 20/-5. Drain Source Voltage is increased to V_{DS} = 200 V. At Gate Source Voltage V_{GS} = 20/-5 V and Drain Source voltage V_{DS} = 200 V, the peak Drain current I_D reached by the SiC MOSFET is 123 A which is 6.83 times the continuous rated current of the device. The respective overshoot in Drain Source voltage is V_{DS} = 237 V. Following the simulation of V_{DS} test, SiC MOSFET - C2M0160120D is subjected to V_{DS} test in laboratory conditions at the same V_{GS} = 20/-5 V and V_{DS} = 200 V. The respective comparison between the simulation results and the oscilloscope image are shown in **Figure 8-5**. From the figure, the peak Drain current I_D reached by the SiC MOSFET in lab conditions was I_D = 130 A (Max C4) with overshoot in Drain Source voltage of V_{DS} = 242 V (Max C3). The simulations results are close to the Laboratory results. This verifies proper functioning of the Pulse Current Test circuit and hence the device under test can be subjected to V_{DS} and V_{GS} tests.

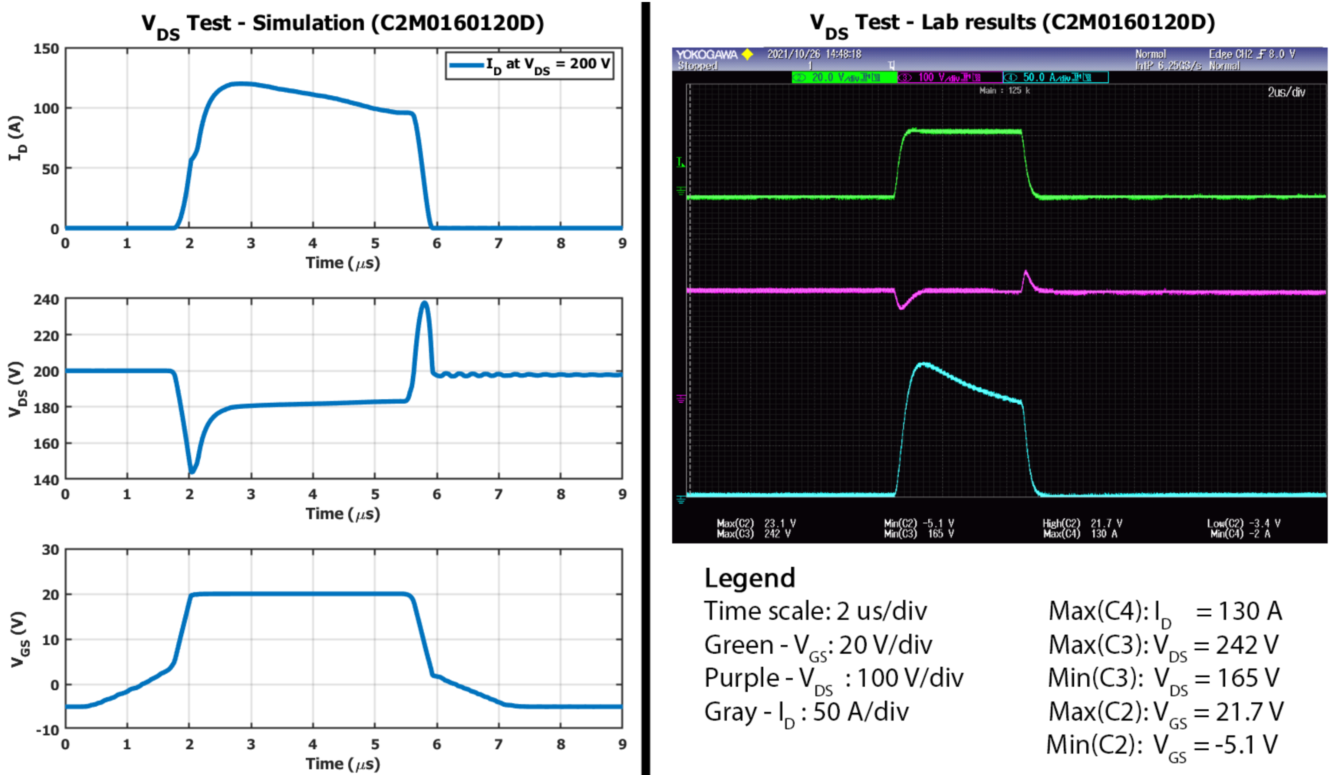

Figure 8-5 V_{DS} **Test – Simulation**

PULSE CURRENT TEST (V_{DS} TEST)

As discussed earlier, when Drain Source Voltage V_{DS} is increased, higher potential is applied across the bulk which results in conduction of a greater number of electrons through the device. As a result, drain current I_D conducted by the SiC MOSFET increases significantly. Moreover, when V_{DS} is increased, the peak value of Drain current I_D is achieved much faster as charge carrier mobility increases as a result of more energy dissipated across the bulk. At constant V_{GS}, increasing V_{DS} can bring the device closer to its Peak pulse current limits. Procedure for obtaining peak Drain current I_D by increasing Drain Source Voltage V_{DS} at constant optimal Gate Source Voltage V_{GS} is explained below.

1. Place the Device Under test in the DUT slot.
2. Operate Function Generator in Pulse mode with manual triggering. Configure Gate Pulse of 5 V rms and $t_{on} = 4\ \mu s$ in the Function Generator.
3. Bring the Gate Source voltage V_{GS} to -5/20 V which is the optimal V_{GS} of DUT.
4. Turn ON the Variable DC supply and gradually increase V_{DC} in steps of 20 V until 100 V.
5. Manually trigger the Gate pulse in the Function Generator.
6. Observe the behavior of Drain current I_D and Overshoot in Drain Source Voltage V_{DS}.
7. Note down Drain currents how many times the rated value is produced.
8. Repeat the same procedure by gradually increasing V_{DC} to 200 V and 300 V.
9. Observe the rise of Drain current I_D and Overshoot in Drain Source Voltage V_{DS}.
10. Note down Drain currents how many times the rated value is produced.

8.3.1.1 EXPERIMENTAL RESULTS (V_{DS} TEST)

SiC MOSFET - C2M0160120D is practically subjected to V_{DS} test by varying Drain Source voltage gradually from zero until V_{DS} = 100 V, V_{DS} = 200 V, V_{DS} = 300 V and V_{DS} = 400 V at a constant Gate Source voltage $V_{GS,optimal}$ = 20/-5 V. The experimental results of V_{DS} Test of SiC MOSFET - C2M0160120D are shown by **Figure 8-6**. At Gate Source $V_{GS,optimal}$ = 20/-5 V, the conduction channel is completely formed and hence Drain Source Voltage V_{DS} can be increased until the drain current saturates.

At V_{GS} = 20/-5 V, when V_{DS} is increased to V_{DS} = 100 V, the peak magnitude of Drain current through the MOSFET reaches I_D = 107 A which is almost 6 times the rated current of the device. At this point, the drain current is not saturated and hence more V_{DS} can be applied. When V_{DS} is increased to V_{DS} = 200 V, the Drain current increases only to 127 A which suggests that the drain current is closer to saturation. When V_{DS} is further increased to V_{DS} = 300 V, Drain current rises to I_D = 137 A. Finally, at V_{DS} = 400, Drain current reaches its highest value of I_D = 143 A which is almost 8 times the rated continuous current of the device with an overshoot in V_{DS} of 433 V during turn-off. The drain current I_D does not rise any higher even when more V_{DS} is applied. Increasing V_{DS} further causes more losses in the bulk of the SiC MOSFET.

6 SiC MOSFET - C2M0160120D devices are statistically subjected to V_{DS} test and the results obtained from the V_{DS} test is given by the **Table 8-3** below.

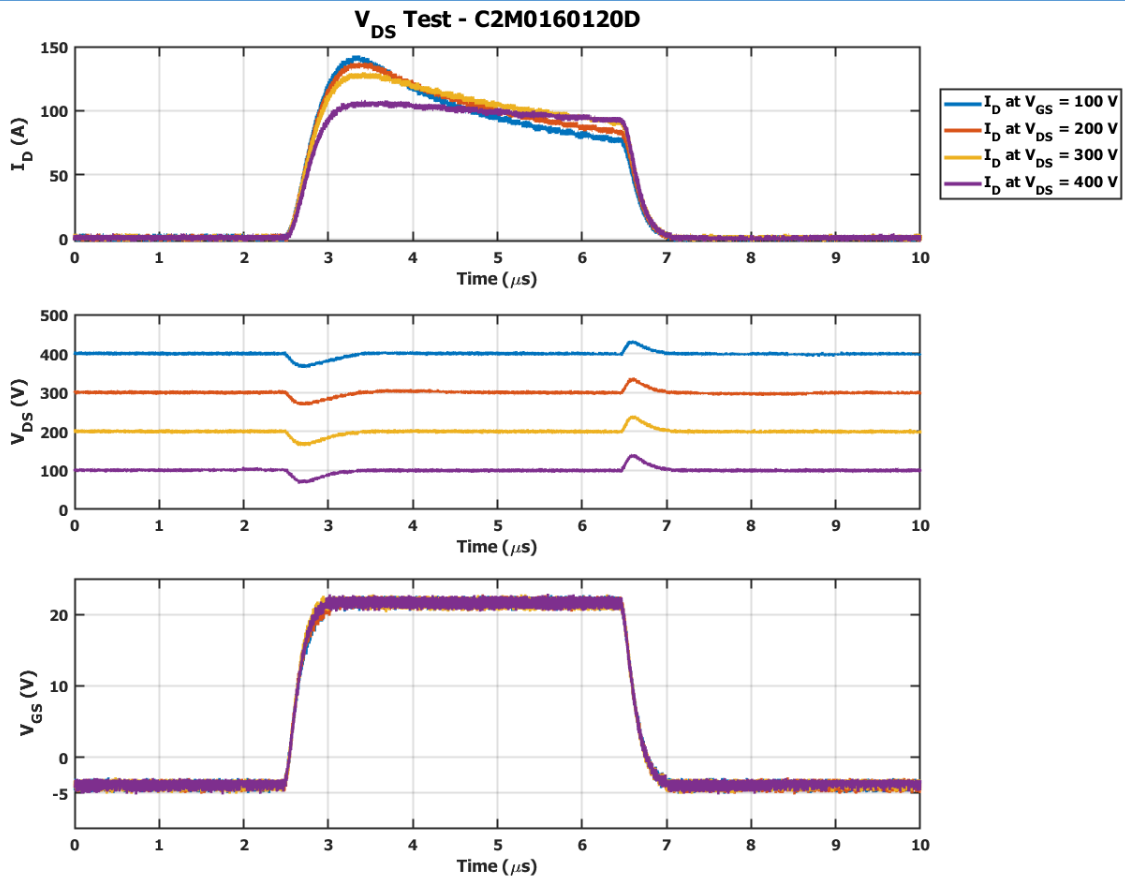

Figure 8-6 V_{DS} Test - Experimental results

8.3.1.2 STATISTICAL RESULTS (V_{DS} TEST)

SET	DUT	V_{DS} (V)	V_{GS} (V)	I_D (A)	$V_{DS,peak}$ (V)	$N = \frac{I_D}{I_{D,rated}}$
SET 1	DUT 10	100 V	-5/20 V	110	141	6.11
	DUT 11			108	142	6
	DUT 12			108	140	6
SET 2	DUT 13	300 V		140	338	7.77
	DUT 14			138	338	7.67
	DUT 15			139	337	7.72

Table 8-3 Statistical results V_{GS} constant, increasing V_{DS}

8.3.2 PULSE CURRENT TEST (V_{GS} TEST)

As discussed earlier, when Gate Source Voltage V_{GS} is increased, the thickness of the conduction layer increases which allows a greater number of electrons to pass through the conduction channel. As a result, drain current I_D conducted by the SiC MOSFET increases sharply. At constant V_{DS}, increasing V_{GS} can bring the device closer to its Peak pulse current limits. Procedure for obtaining peak Drain current I_D by increasing Gate Source Voltage V_{GS} at constant Drain Source Voltage V_{DS} is explained below.

1. Place the Device Under Test in the DUT slot.
2. Turn ON the Variable DC supply and configure $V_{DC} = 300\ V$.
3. Operate Function Generator in Pulse mode with manual triggering. Configure Gate Pulse of 5 V rms and $t_{on} = 4\ \mu s$ in the Function Generator.
4. Bring the Gate Source voltage V_{GS} to -5/15 V.
5. Manually trigger the Gate pulse in the Function Generator.
6. Observe the behavior of Drain current I_D and Overshoot in Drain Source Voltage V_{DS}.
7. Note down Drain currents of how many times the rated value is produced.
8. Repeat the same procedure for increasing values of V_{GS} = -5/20 V and V_{GS} = -5/24 V.
9. Note down Drain currents how many times the rated value is produced.

8.3.2.1 EXPERIMENTAL RESULTS (V_{GS} TEST)

SiC MOSFET - C2M0160120D is practically subjected to V_{GS} test in lab. Drain Source voltage is maintained at a constant V_{DS} = 300 V and Gate Source voltage V_{GS} is increased in steps from V_{GS} = 15/-5 V to V_{GS} = 20/-5 V and finally to V_{GS} = 24/-5 V. The experimental results of V_{GS} Test is shown by **Figure 8-7**. At V_{GS} = 15/-5 V and V_{DS} = 300 V, The MOSFET conducts a peak Pulse current I_D of magnitude 83 A which is 4.6 times the rated current of the device and the respective overshoot in Drain Source voltage V_{DS} is observed to be 334 V.

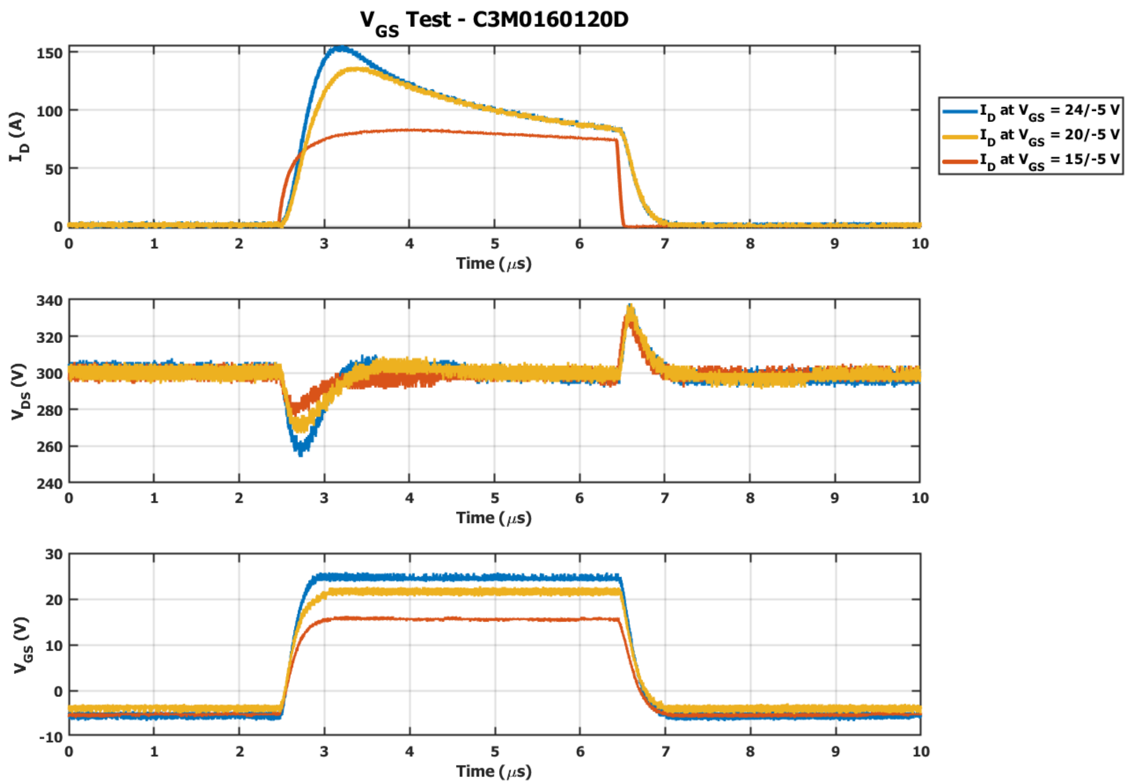

Figure 8-7 V_{GS} Test - Experimental results

When Gate Source voltage V_{GS} is increased to V_{GS} = 20/-5 V, peak Pulse current magnitude rises to 137 A which is almost 7.6 times the rated current of the device and the respective overshoot in Drain Source voltage V_{DS} is observed to be 338 V. Finally, at V_{GS} = 24/-5 V, the Peak pulse Drain current I_D attains a maximum value of I_D = 157 A which is almost 8.72 times the rated current of the device and the respective overshoot in Drain Source voltage V_{DS} is observed to be 338 V. 9 SiC

MOSFET - C2M0160120D devices are statistically subjected to V_{GS} test and the results obtained from the V_{GS} test is given by the **Table 8-4** below.

8.3.2.2 STATISTICAL RESULTS (V_{GS} TEST)

SET	DUT	V_{DS} (V)	V_{GS} (V)	I_D (A)	$V_{DS,peak}$ (V)	$N = \frac{I_D}{I_{D,rated}}$
SET 1	DUT 1	300 V	-5/15 V	83.6	335	4.64
	DUT 2			83.8	334	4.65
	DUT 3			79.9	334	4.43
SET 2	DUT 4		-5/20 V	140	338	7.77
	DUT 5			138	338	7.66
	DUT 6			139	337	7.72
SET 3	DUT 7		-5/25 V	158	337	8.77
	DUT 8			156	338	8.67
	DUT 9			157	338	8.72

Table 8-4 Statistical results V_{DS} constant, increasing V_{GS}

8.3.3 PULSE CURRENT COMPARISON OF DIFFERENT TYPES OF IGBT AND MOSFET

In this test, various types of switching technologies of comparable ratings are compared together and studied for their Pulse Current capabilities. A high Gate Source Voltage V_{GS} = 24/-5 V is applied to provide maximum volume to the conduction channel for the Drain current to flow and V_{DS} = 300 V is applied so that all the devices reach almost their peak output currents. The devices used in this test are listed below.

C3M0075120D – SiC MOSFET (3rd Gen): $I_{D,rated}$ = 30 A, $V_{DS,rated}$ = 1.2 kV, $R_{DS(on)}$ = 75 mΩ

C2M0080120D – SiC MOSFET (2nd Gen): $I_{D,rated}$ = 36 A, $V_{DS,rated}$ = 1.2 kV, $R_{DS(on)}$ = 75 mΩ

IPW90R120C3 – Si CoolMOS: $I_{D,rated}$ = 36 A, $V_{DS,rated}$ = 900 V, $R_{DS(on)}$ = 120 mΩ

SGW25N120 – NPT-IGBT: $I_{C,rated}$ = 46 A, $V_{CE,rated}$ = 1.2 kV

Figure 8-8 shows the experimental results of the Pulse current comparison of various switching technologies mentioned above.

From the figure, NPT-IGBT reaches peak Collector current of I_c = 574 A which is 12.48 times its rated continuous current which is the highest multiplication factor achieved among all the devices mentioned above. The overshoot in V_{CE} during turn-off was found to be 429 V. Si CoolMOS reached a peak drain current I_D = 297 A which is 8.25 time the rated continuous current with a peak overshoot of V_{DS} = 357 V. Both the 2nd Gen and 3rd Gen SiC MOSFETs were able to reach higher peaks of drain currents compared to Si MOSFET. SiC MOSFET (C3M0080120D – 2nd Gen) reached a peak drain current of I_D = 316 A with a multiplication factor of 8.78 times. However, the 3rd Gen SiC MOSFET reached 307 A which is 10.23 times its rated continuous current. The 3rd Gen SiC

MOSFET conducted a peak current 9 A lesser than 2nd Gen SiC MOSFET, however it produced better multiplication factor compared to 2nd Gen SiC MOSFET.

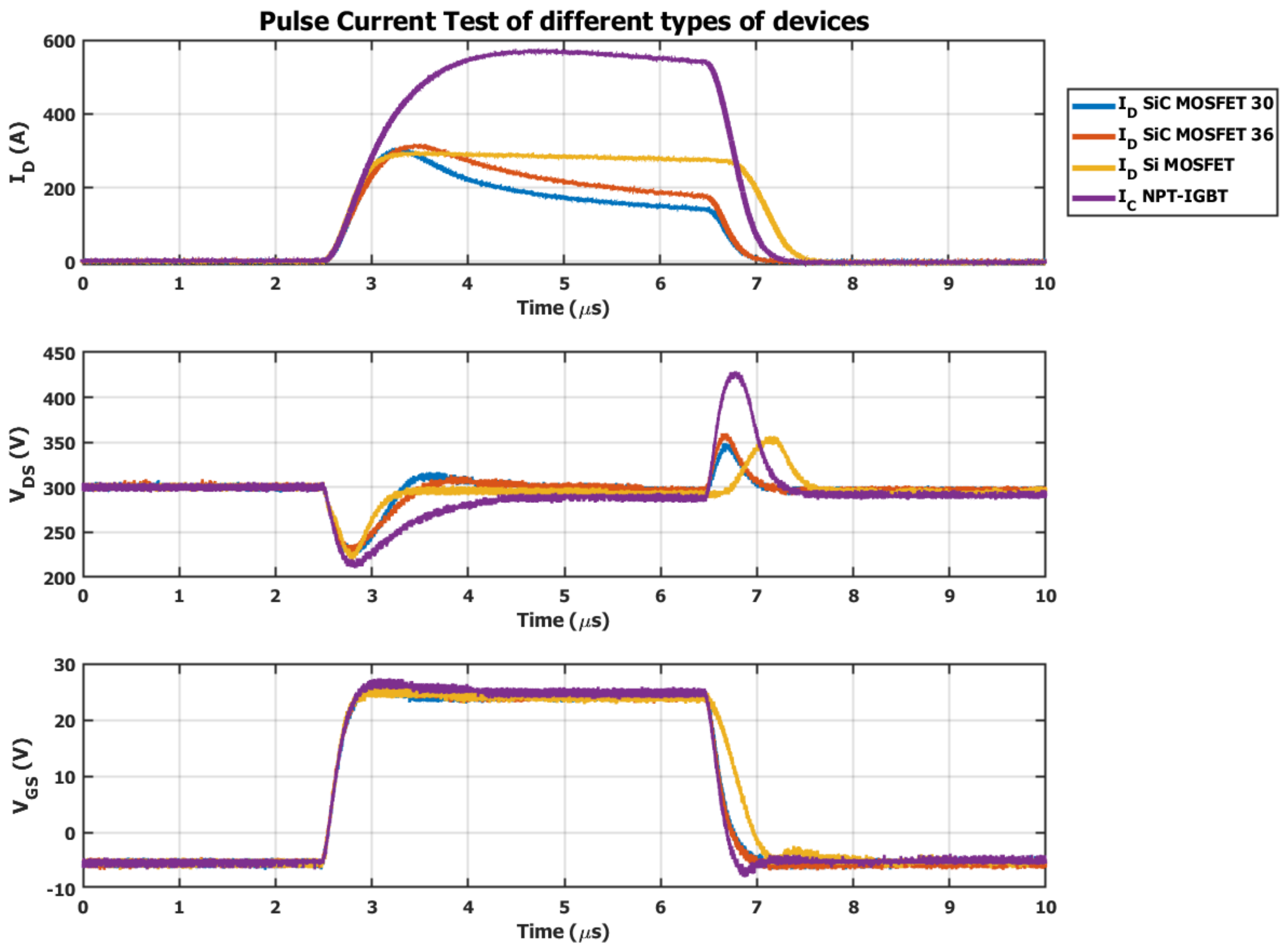

Figure 8-8 Pulse Current comparison IGBT vs MOSFET

8.3.4 PULSE CURRENT COMPARISON OF 1.7 kV vs 3 kV IGBT

A similar Pulse current test was conducted to compare two IGBT technologies belonging to different voltage ratings. The devices that are tested and their respective ratings are mentioned below.

IXGH24N170 – NPT IGBT: $I_{C,rated}$ = 50 A, $V_{CE,rated}$ = 1.7 kV, $V_{GE,max}$ = ± 30 V

IXBH20N300 – NPT IGBT: $I_{C,rated}$ = 50 A, $V_{CE,rated}$ = 3 kV, $V_{GE,max}$ = ± 30 V

Figure **8-9** represents experimental comparison of the two high voltage rating IGBT technologies IXGH24N170 and IXBH20N300. From the figure, IXGH24N170 conducts a Collector current I_C = 609 A which is 12.18 times the rated current of the device with an overshoot of V_{CE} = 409 V. IGBT IXBH20N300 conducts a peak Collector current I_C = 486 A which is 9.72 times the rated current of the device and overshoot of V_{ce} = 403 V. Since the IGBT are experimented at V_{GE} = ± 25 V, the conduction channels of both the devices still have more potential to conduct higher Collector currents I_C. Moreover, V_{CE} can be increased to achieve still higher Collector current I_C until the conduction channel is completely saturated. Also increasing V_{CE} can improve the rise time of the Collector current I_C further.

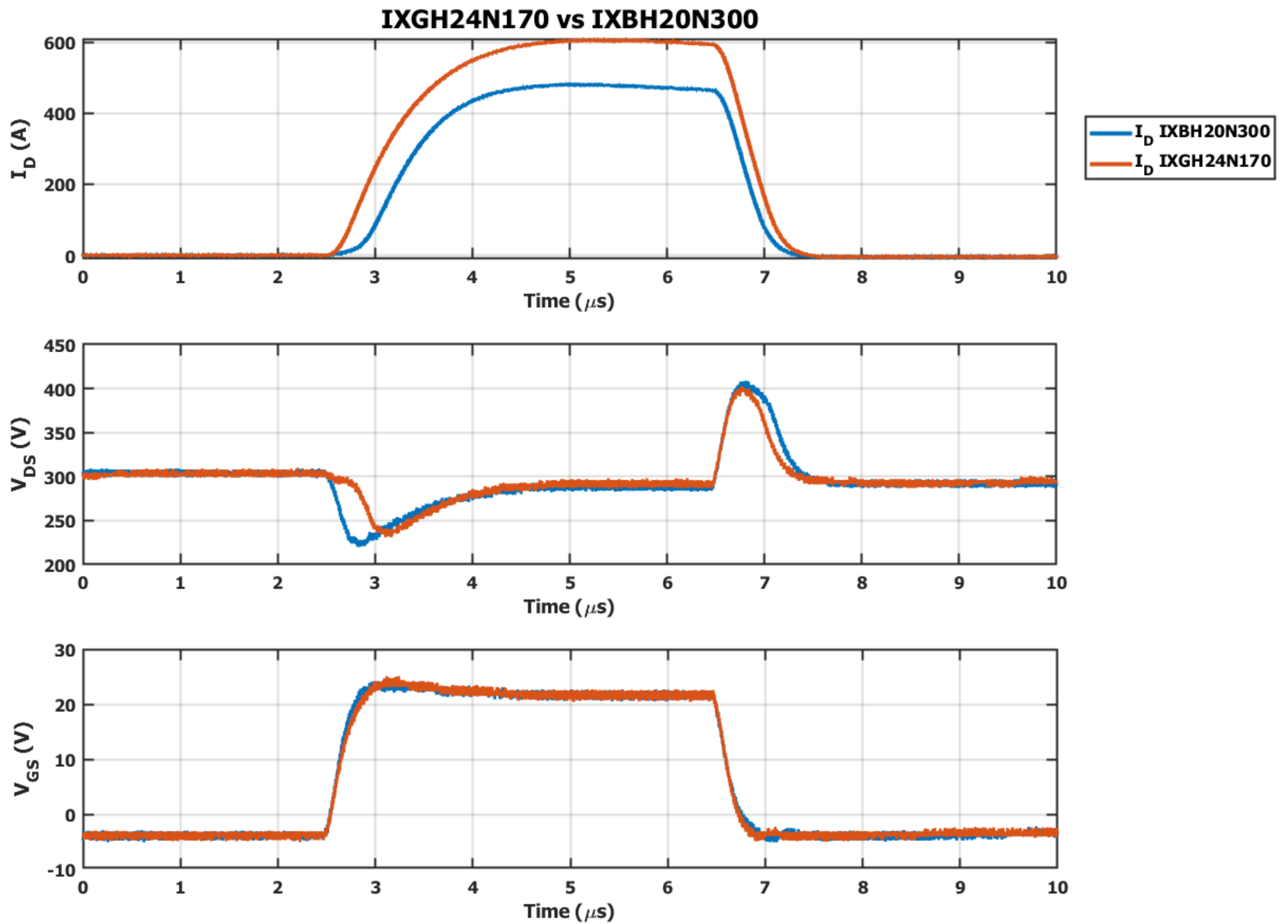

Figure 8-9 Pulse current comparison - IXGH24N170 vs IXBH20N300

8.3.5 PULSE CURRENT COMPARISON OF Planar SiC MOSFET vs Trench Gate FS IGBT

Finally, pulse current test was conducted to compare Planar SiC MOSFET with Trench Gate FS IGBT technology belonging to higher current ratings. The devices that are tested and their respective ratings are mentioned below.

Planar SiC MOSFET – C3M0016120D: $I_{D,rated}$ = 81 A, $V_{DS,rated}$ = 1.2 kV, $R_{DS(on)}$ = 16 mΩ

Trench Gate FS IGBT – IHW40N120R5: $I_{C,rated}$ = 80 A, $V_{CE,rated}$ = 1.2 kV

The devices are tested at V_{DS} = 300 V and V_{GS} = 24/-5 V and the corresponding experimental results are shown in **Figure 8-10**. At V_{GS} = 24/-5 V, the SiC MOSFET attains a peak Drain current I_D = 905 A which is 11.17 times its continuous rated current with an overshoot of V_{DS} = 389 V. On the other hand, the Trench Gate FS IGBT was able to conduct peak collector current I_D = 697 A. The multiplication factor obtained for such a high pulse current is 8.7 times which is 208 A lesser compared to SiC MOSFET. From the waveforms, it can be observed that the overshoot in V_{DS} during turn-off is related to the Drain current magnitude I_D at the falling edge of the Drain current curve.

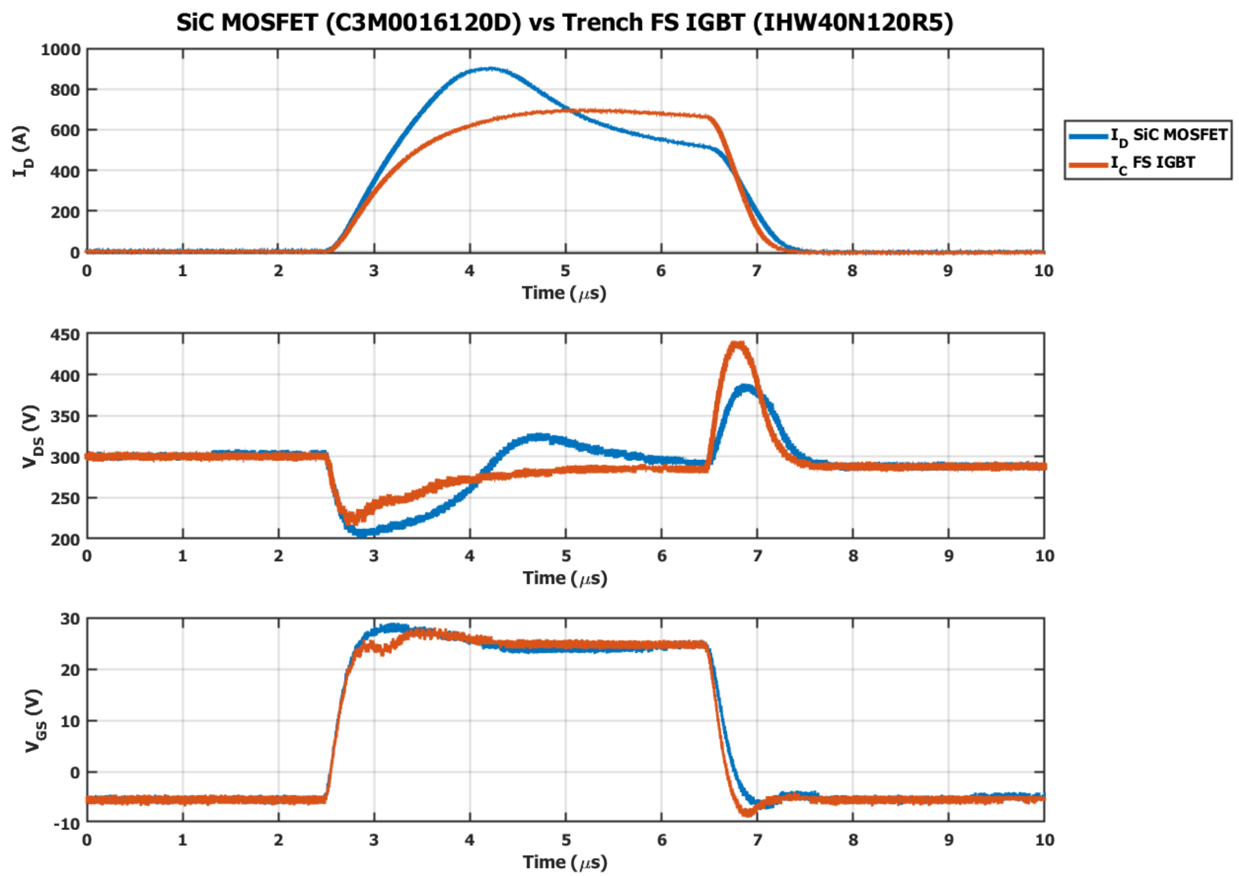

Figure 8-10 Pulse Current Test of SiC MOSFET vs Trench Gate FS IGBT

9
CONCLUSION

To generate an Impulse waveform of magnitude 250 kV with rise time of 1.2 µs by employing Modular Multilevel Converter (MMC), each Power Electronic device of every Sub-Module (SM) has to endure switching currents as high as 850 A. However, to generate other waveforms, the MMC generates switching currents of only a few Amperes. Also, implementing Power Electronic devices of current rating as high as 850 A is not only uneconomical, but also makes the system bulky. Hence this Master thesis explored the feasibility of using Power Electronic devices such as IGBT and MOSFET of lower current ratings to conduct high switching currents through following research.

- Preliminary research findings suggested N-channel MOSFET could reach higher current peaks compared to P-channel MOSFET as mobility of electrons is greater than holes. Further, MOSFET was classified into Enhancement and Depletion types. Enhancement MOSFET is easier to control compared to Depletion MOSFET. Further MOSFET was classified based on substrate material into Si and SiC MOSFET. SiC substrate had superior thermal properties resulting in lower on-state resistance and hence high peaks of Drain current. Based on literature, Planar MOSFET could exhibit better ability to withstand short circuit test at higher voltages compared to Trench MOSFET even though Trench MOSFET could conduct higher Drain currents.
- From literature, PT-IGBT has heavily doped n^+ layer which allows it to reach high Collector currents, very low on-state resistance, elimination of current tailing. However, very high turn-off losses due to recombination of holes during turn-off and prone to latch-up. NPT-IGBT because of absence of n^+ layer, has highest voltage blocking capability for same thickness among IGBTs, resistant to latch-up, lowest switching losses since holes are not recombined during turn-off. However, the on-state resistance of NPT-IGBT is high and as a result it suffers from high conduction losses. Moreover, it suffers from very long current tailing however the magnitude of tailing current is very low. Finally, Trench Gate Field Stop IGBT is introduced which combines the advantages of both PT and NPT-IGBTs such as higher Collector current, lower on-state resistance, resistance towards latching and high switching frequency.
- From literature, Trench Gate FS IGBT, NPT-IGBT, SiC MOSFET and Si MOSFET were compared together based on criteria namely output current, leakage current, charge required by the Gate terminal to create conduction channel and switching losses. Trench Gate FS IGBT reaches highest collector currents and exhibits lowest on-state voltage drop. SiC MOSFET exhibits least amount of leakage current. Both SiC MOSFET and Trench Gate FS IGBT requires least amount of Gate charge to create conduction channel. Finally, SiC MOSFET exhibited least amount of switching losses among all the devices.
- Pulse Current test circuit is defined and factors affecting peak value of Drain current were identified to be Gate Source voltage, Drain Source voltage and Gate resistance. Methods to

achieve peak drain current manipulating factors surrounding Drain current are discussed. Failure mechanisms of both SiC and Si devices are discussed.

- Elements of the pulse current test are defined and the procedure to setup the pulse current test is discussed. Power electronic device C3M0160120D undergoes V_{GS} and V_{DS} tests under laboratory conditions. Based on the results, various Power Electronic devices such as FS-IGBT, NPT-IGBT, SiC MOSFET and Si MOSFET are subjected to Pulse current test in lab. Respective multiplication factor delivered by each Power Electronic device is noted.

To conclude, from the results of Pulse current tests performed in the lab, it is clear that the main objective of this Master Thesis has been successfully accomplished. The SiC MOSFET - C3M0016120D achieved highest pulse current of magnitude 905 A which is which is greater than the pulse current requirement of the MMC of 850 A to produce an Impulse voltage of 250 kV across 10 nF capacitance. Moreover, NPT-IGBT displayed a promising multiplication factor of 12.48 times its rated current.

The research objectives are answered based on understanding developed from literature review and practical results obtained.

1. Study the most promising Power Electronic device to achieve the highest pulse currents.

   The switching technology that delivered highest peak of pulse current was SiC MOSFET. The SiC MOSFET – C3M0016120D was subjected to pulse current test at V_{GS} = 24/-5 V and V_{DS} = 300 V for Gate pulse duration of t_{on} = 4 µs. The ratings of the SiC MOSFET are: I_D = 81 A, V_{DS} = 1.2 kV and $R_{DS(on)}$ = 16 mΩ. The SiC MOSFET was able to conduct 905 A of peak pulse current at a multiplication factor of 11.17 with an overshoot of V_{DS} = 389 V during turn-off. SiC MOSFET when operated at high Gate Source Voltages V_{GS}, the on-state resistance $R_{DS(on)}$ across the bulk reduces. Moreover, quasi-linear regions are wider in SiC MOSFET unlike other Si devices due to its lower transconductance. Hence, when V_{DS} is increased beyond applied V_{GS}, the rate at which the pinch-off of the conduction channel occurs is lower. Also, when SiC MOSFET is operated in linear region, the on-state resistance $R_{DS(on)}$ of the device is dominated by the resistance of the conduction channel R_{CH}. The conduction channel of SiC MOSFET exhibits unique property of negative temperature co-efficient. Hence during linear region, as conduction current increases the temperature of the channel increases and channel resistance drops. These are the contributing factors that helped SiC MOSFET – C3M0016120D to reach highest pulse currents.

2. What are the parameters that determine the peak current obtained through a Power Electronic device?

   The parameters that decide the peak pulse current that can be conducted through a Power Electronic device are Gate Source Voltage V_{GS}, Drain Source Voltage V_{DS} and Gate resistance R_G. When V_{GS} is increased, the conduction channel accumulates a greater number of electrons. This enables a greater number of electrons to pass from Drain to Source terminals. The output current is very sensitive to any changes in Gate Source Voltage V_{GS}. When V_{DS} is increased, the potential applied across the bulk increases. In linear region, the Power Electronic device acts like a linear resistor. Hence, output current of the Power Electronic device is directly proportional to the voltage applied across the Drain and Source terminals. The conduction channel is formed with a time constant $\tau = R_G.C_{GD}$. Hence, lower the Gate resistance R_G lower is the time constant τ and

hence faster is the formation of conduction channel. Hence the rate of rise of output current increases.

3. How to verify practically the highest peak pulse current derived from theoretical understanding?

This can be well explained from V_{GS} and V_{DS} tests of SiC MOSFET – C2M0160120D. From V_{DS} test, when V_{DS} is increased beyond 20 V at V_{GS} = 20/-5 V, current magnitude starts to increase since the applied voltage across $R_{DS(on)}$ withdraws more current from the voltage source. On the other hand, increasing V_{DS} (greater than V_{GS}) beyond 20 V causes electrons that are responsible for the creation of conduction channel to drift into the Source terminal. This acts as a feedback mechanism for increasing drain current. However, since the DUT is under short circuit condition, more current flows through the conduction channel. This high current maintains the conduction channel as it compensates some of the loss of electrons from the conduction channel. As a result, at V_{DS} = 200 V, the Drain current reached I_D = 130 A as represented in **Figure 8-5** which is also verified by the simulation results. When V_{DS} is increased to V_{DS} = 400 V, the MOSFET reaches peak Drain current of I_D = 143 A and drain current does not increase further even when V_{DS} is increased. Thus, the SiC MOSFET has reached pinch-off and this verifies theoretical understand of peak pulse current that can be achieved practically.

9.1 RECOMMENDATIONS FOR FUTURE WORK

- Even though the SiC MOSFET – C3M0016120D was able to reach peak pulse current of 905 A with a multiplication factor of 11.17 times the continuous rated current, the NPT-IGBT technologies SGW25N120 and IXGH24N170 produced a multiplication factor of 12.5 and 12 times their continuous rated currents respectively. Hence, it is highly recommended to compare pulse current capabilities of SiC MOSFET – C3M0016120 to an NPT-IGBT and PT-IGBT of the same rating.
- This thesis mainly focussed on feasibility of achieving highest pulse current capabilities of IGBT and MOSFET. Hence, it is highly recommended to test the reliability and repetitive short circuit capability of IGBTs and MOSFETs

APPENDIX A

The Pulse current test circuit used to test pulse current capabilities of various Power Electronic devices in this thesis is shown in **Figure A-1** below.

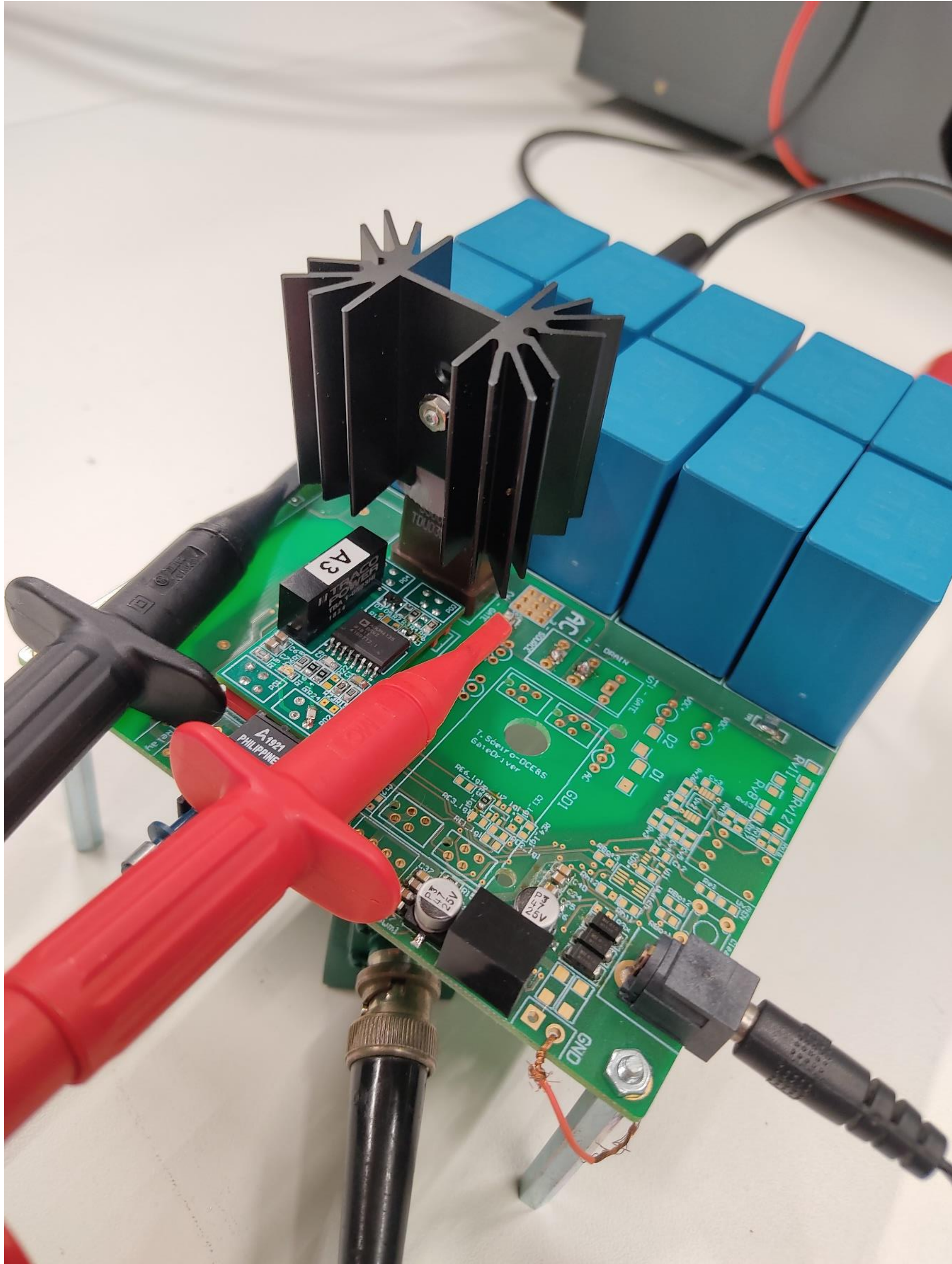

Figure A-1 Pulse Current Test circuit

APPENDIX B

The Appendix B section intends to include various oscilloscope images belonging to various Pulse current tests to authenticate the results and waveforms from **CHAPTER 8** of this thesis.

EXPERIMENTAL RESULTS (V_{DS} TEST)

The Oscilloscope image shown in **Figure B-1** corresponds to the waveform shown in **Figure 8-6** belonging to V_{DS} test of SiC MOSFET – C2M0160120D. Max(C4) displays peak pulse current achieved I_D = 143 A in the V_{DS} test at V_{GS} = 20/-5 V and V_{DS} = 400 V. Max(C3) denotes peak overshoot in V_{DS} during turn-off which is V_{DS} = 433 V.

Legend:

Time scale: 2 μs/div

Green: Gate Source Voltage V_{GS}: 20 V/div

Purple: Drain Source Voltage V_{DS}: 100 V/div

Gray: Drain current I_D: 50 A/div

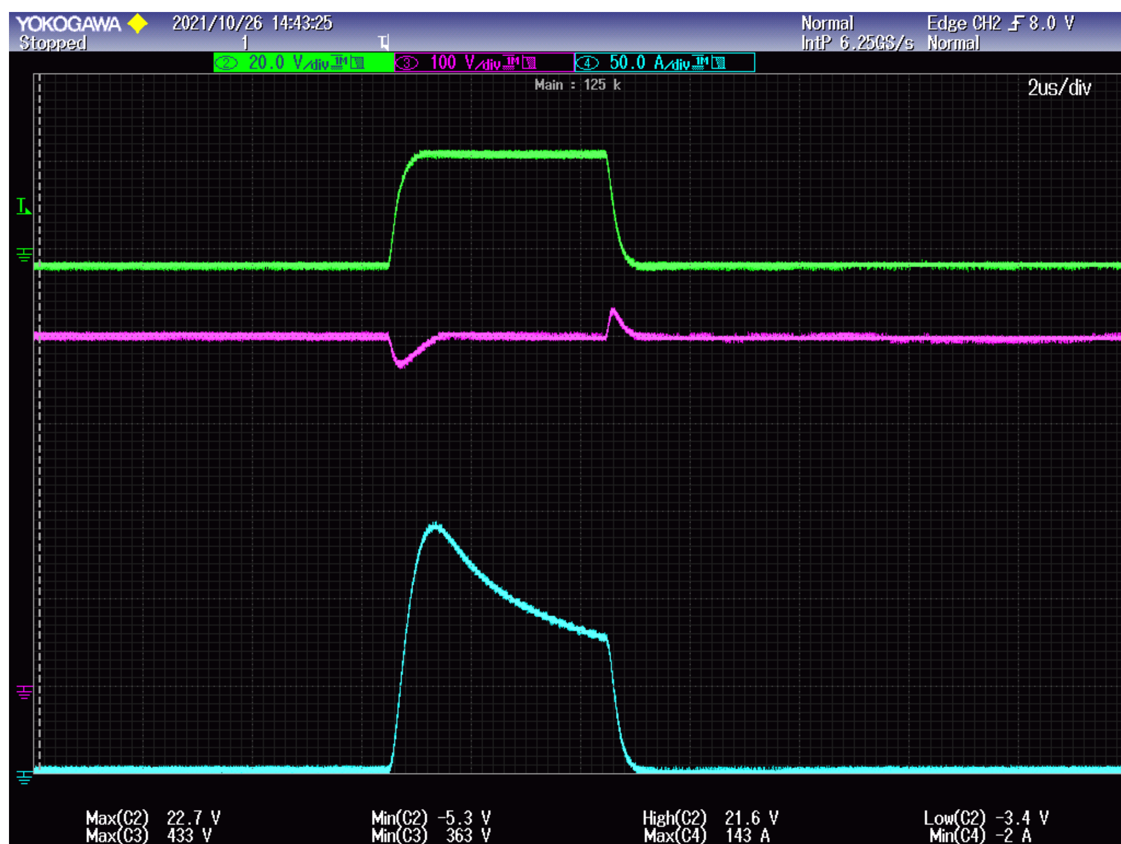

Figure B-1 Oscilloscope image V_{DS} Test (C2M0160120D)

EXPERIMENTAL RESULTS (V_{GS} TEST)

The Oscilloscope image shown in **Figure B-2** corresponds to the waveform shown in **Figure 8-7** belonging to V_{GS} test of SiC MOSFET – C2M0160120D. Max(C4) displays peak pulse current achieved I_D = 157 A in the V_{GS} test at V_{GS} = 24/-5 V and V_{DS} = 300 V. Max(C3) denotes peak overshoot in V_{DS} during turn-off which is V_{DS} = 338 V.

Legend:

Time scale: 2 µs/div

Green: Gate Source Voltage V_{GS}: 20 V/div

Purple: Drain Source Voltage V_{DS}: 100 V/div

Gray: Drain current I_D: 50 A/div

Figure B-2 Oscilloscope image V_{GS} Test (C2M0160120D)

PULSE CURRENT TEST OF POWER ELECTRONIC DEVICES $(30\ A - 46\ A)$ RANGE

SiC MOSFET - C3M0075120D

The Oscilloscope image **Figure B-3** corresponds to the waveform of SiC MOSFET C3M0075120D shown in **Figure 8-8** where it is compared to other devices at V_{GS} = 24/-5 V and V_{DS} = 300 V**.** Max(C4) displays peak pulse current achieved I_D = 307 A and Max(C3) denotes peak overshoot in V_{DS} during turn-off which is V_{DS} = 349 V.

Legend:

Time scale: 2 µs/div

Green: Gate Source Voltage V_{GS}: 20 V/div

Purple: Drain Source Voltage V_{DS}: 100 V/div

Gray: Drain current I_D: 100 A/div

Figure B-3

Figure B-3 SiC MOSFET - C3M0075120D

SiC MOSFET - C3M0080120D

The Oscilloscope image **Figure B-4** corresponds to the waveform of SiC MOSFET C3M0080120D shown in **Figure 8-8** where it is compared to other devices at V_{GS} = 24/-5 V and V_{DS} = 300 V**.** Max(C4) displays peak pulse current achieved I_D = 316 A and Max(C3) denotes peak overshoot in V_{DS} during turn-off which is V_{DS} = 361 V.

Legend:

Time scale: 2 µs/div

Green: Gate Source Voltage V_{GS}: 20 V/div

Purple: Drain Source Voltage V_{DS}: 100 V/div

Gray: Drain current I_D: 100 A/div

Figure B-4 SiC MOSFET - C3M0080120D

Si CoolMOS – IPW90R120C3

The Oscilloscope image **Figure B-5** corresponds to the waveform of Si CoolMOS – IPW90R120C3 shown in **Figure 8-8** where it is compared to other devices at V_{GS} = 24/-5 V and V_{DS} = 300 V**.** Max(C4) displays peak pulse current achieved I_D = 297 A and Max(C3) denotes peak overshoot in V_{DS} during turn-off which is V_{DS} = 357 V.

Legend:

Time scale: 2 µs/div

Green: Gate Source Voltage V_{GS}: 20 V/div

Purple: Drain Source Voltage V_{DS}: 100 V/div

Gray: Drain current I_D: 100 A/div

Figure B-5 Si CoolMOS - IPW90R120C3

NPT-IGBT – SGW25N120

The Oscilloscope image **Figure B-6** corresponds to the waveform of NPT-IGBT – SGW25N120 shown in **Figure 8-8** where it is compared to other devices at V_{GS} = 24/-5 V and V_{DS} = 300 V**.** Max(C4) displays peak pulse current achieved I_D = 574 A and Max(C3) denotes peak overshoot in V_{DS} during turn-off which is V_{DS} = 429 V.

Legend:

Time scale: 2 µs/div

Green: Gate Source Voltage V_{GS}: 20 V/div

Purple: Drain Source Voltage V_{DS}: 100 V/div

Gray: Drain current I_D: 100 A/div

Figure B-6 NPT IGBT – SGW25N120

PULSE CURRENT TEST (1.7 kV vs 3 kV IGBT)

NPT IGBT – IXGH24N170

The Oscilloscope image **Figure B-7** the waveform of NPT-IGBT – IXGH24N170 shown in **Figure 8-9** at V_{GS} = 24/-5 V and V_{DS} = 300 V**.** Max(C4) displays peak pulse current achieved I_D = 609 A and Max(C3) denotes peak overshoot in V_{DS} during turn-off which is V_{DS} = 409 V.

Legend:

Time scale: 2 µs/div

Green: Gate Source Voltage V_{GS}: 20 V/div

Purple: Drain Source Voltage V_{DS}: 100 V/div

Gray: Drain current I_D: 100 A/div

Figure B-7 NPT-IGBT IXGH24N170

NPT IGBT – IXBH20N300

The Oscilloscope image **Figure B-8** corresponds to the waveform of NPT IGBT – IXBH20N300 shown in **Figure 8-9** at V_{GS} = 24/-5 V and V_{DS} = 300 V**.** Max(C4) displays peak pulse current achieved I_D = 486 A and Max(C3) denotes peak overshoot in V_{DS} during turn-off which is V_{DS} = 403 V.

Legend:

Time scale: 2 µs/div

Green: Gate Source Voltage V_{GS}: 20 V/div

Purple: Drain Source Voltage V_{DS}: 100 V/div

Gray: Drain current I_D: 100 A/div

Figure B-8 NPT-IGBT IXBH20N300

PULSE CURRENT TEST (PLANAR SiC MOSFET vs TRENCH GATE FS IGBT)

PLANAR SiC MOSFET – C3M0016120D

The Oscilloscope image **Figure B-9 c**orresponds to the waveform of Planar SiC MOSFET – C3M0016120D shown in **Figure 8-10** at V_{GS} = 24/-5 V and V_{DS} = 300 V**.** Max(C4) displays peak pulse current achieved I_D = 905 A and Max(C3) denotes peak overshoot in V_{DS} during turn-off which is V_{DS} = 389 V.

Legend:

Time scale: 2 µs/div

Green: Gate Source Voltage V_{GS}: 20 V/div

Purple: Drain Source Voltage V_{DS}: 100 V/div

Gray: Drain current I_D: 100 A/div

Figure B-9 SiC MOSFET – C3M0016120D

TRENCH GATE FS IGBT - IHW40N120R5

The Oscilloscope image **Figure B-10** corresponds to the waveform of Trench Gate FS IGBT - IHW40N120R5 shown in **Figure 8-10** at V_{GS} = 24/-5 V and V_{DS} = 300 V**.** Max(C4) displays peak pulse current achieved I_D = 697 A and Max(C3) denotes peak overshoot in V_{DS} during turn-off which is V_{DS} = 441 V.

Legend:

Time scale: 2 µs/div

Green: Gate Source Voltage V_{GS}: 20 V/div

Purple: Drain Source Voltage V_{DS}: 100 V/div

Gray: Drain current I_D: 100 A/div

Figure B-10 - TRENCH GATE FS IGBT - IHW40N120R5

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