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Evaluating the High Temperature Reliability of Glass Encapsulant Packaged SiC Schottky Diodes with High-temperature Step Stress Aging Test

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***Abstract*—Silicon carbide (SiC) power devices exhibit superior thermal conductivity and excellent high-temperature stability, making them promising for high-power applications under extreme environments. However, ensuring long-term reliability, especially for devices packaged with glass encapsulant, remains a significant challenge. This paper introduces a high-temperature step stress aging test as a highly accelerated life testing method to evaluate the reliability of SiC Schottky diodes packaged with glass encapsulants compared to traditional plastic-packaged counterparts. In this test, diodes undergo incremental thermal stress from 50 ℃ to 300 ℃, increasing by 50 ℃ per step and held for 168 hours per step to simulate prolonged thermal exposure. Finite element simulations were also performed at 300 ℃ to analyze stress distributions in various packaging configurations. Post-aging results demonstrate the effectiveness of this accelerated method for rapidly assessing device degradation, providing valuable reliability insights for applications in extreme thermal environments such as aerospace power systems.**

Keywords*—*Power electronics; SiC schottky diodes; High-temperature step stress aging; Reliability evaluation; Glass encapsulant

I. INTRODUCTION

Power electronic devices, as the core of modern energy conversion systems, play a critical role in high-power applications including rail transportation, renewable energy, smart grids, and aerospace [1]. Their efficiency and reliability directly impact the overall system performance. Wide bandgap (WBG) semiconductor devices, particularly silicon carbide (SiC), exhibit superior breakdown field strength, excellent thermal conductivity, and high-temperature stability, significantly enhancing power density and efficiency, thus becoming a key alternative to traditional silicon-based devices [1]. However, the high-temperature (>200 ℃) and high-frequency operating characteristics of SiC devices pose severe challenges to packaging technologies. Traditional organic encapsulation materials (such as epoxy resin and silicone gel) are limited by their low glass transition temperatures (T_g) and thermo-mechanical degradation, resulting in delamination, electrochemical corrosion, and even "popcorn effects" at elevated temperatures, ultimately leading to device failure. Furthermore, issues such as interfacial stress induced by mismatched coefficients of thermal expansion (CTE), moisture penetration, and radiation-induced material aging further restrict the reliability of organic encapsulation materials under extreme conditions. Overcoming the high-temperature bottleneck of packaging materials has thus become crucial to unlocking the potential of SiC devices.

To address high-temperature packaging requirements, inorganic non-metallic materials (e.g., glass and ceramics) have attracted extensive attention due to their superior thermal stability, chemical inertness, and excellent insulation properties [2]. Research has demonstrated that glass encapsulation can optimize the CTE matching and encapsulation temperature by adjusting its composition (e.g., bismuth-based glass doped with BaO/ZnO) [3]. For example, East China University of Science and Technology achieved a low thermal resistance of 0.45 ℃/W by encapsulating SiC Schottky Barrier Diodes (SBD) using glass encapsulants at a process temperature of 450 ℃, maintaining stable performance over thermal cycling from -50 ℃ to 150 ℃ [4]. Similarly, Virginia Tech employed molten lead-glass encapsulation, demonstrating devices that maintained a high breakdown strength of 4.5 kV after continuous operation for 1000 hours at 250 ℃ [5]. Despite notable progress, glass encapsulation still faces significant challenges, including high-temperature processing (>450 ℃) that may damage chip oxide layers, interfacial microcracks caused by CTE mismatch reducing the partial discharge inception voltage (PDIV), and buffer layers (such as polyimide or nanocomposites) that, while alleviating stress, may compromise insulation or complicate fabrication. Current research primarily focuses on steady-state high-temperature performance, lacking systematic evaluations of failure mechanisms under realistic, dynamic temperature cycling and step-stress conditions. To

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[#] Both authors contributed equally to this work.

address these packaging reliability challenges under extreme high-temperature conditions, researchers propose a high-temperature step-stress aging test method, gradually increasing thermal and mechanical stress through incremental temperature steps with specific dwell times at each stage [6]. Compared with conventional steady-state aging, this approach, analogous to Highly Accelerated Life Testing (HALT), allows timely monitoring of soft and hard failures after each temperature step, identifying critical failure points, quantifying degradation processes, and providing crucial insights for subsequent material improvement and lifetime prediction [7].

To systematically evaluate the long-term reliability of glass-encapsulated SiC SBDs under extreme thermal environments, this study proposes a high-temperature step-stress aging test for comparative reliability assessment of glass encapsulation versus traditional plastic encapsulation. In the experimental setup, devices are subjected to temperature increments from 50 °C to 300 °C in steps of 50 °C, with each temperature step lasting 168 hours, thereby simulating prolonged thermal exposure. Concurrently, finite element simulations at 300 °C analyze thermo-mechanical stress distributions for different packaging configurations. Compared to conventional steady-state aging tests, the high-temperature step-stress approach rapidly reveals latent defects, providing critical reliability assessment benchmarks for practical applications in extreme environments such as aerospace.

II. EXPERIMENTAL SETUP AND METHODS

A. *TO-247 SiC SBD Sample Preparation*

Firstly, basic materials such as SiC chips (1200 V, 58 A, provided by SICHAINSEMI) and metal frames were prepared. Subsequently, die attachment was conducted using two different approaches: pressureless sintered silver or $PbSn_5Ag_{1.5}$ solder. For the pressureless silver sintering path, silver paste was printed onto the substrate using a printing device (Datacon 2200 evo), followed by die placement, and then sintered in a high-temperature furnace to form highly reliable interconnections. Alternatively, in the soldering path, solder bonding was completed using a pick-and-place machine (Jiafeng 380plus) combined with reflow soldering equipment. After die attachment, automatic wire bonding equipment was utilized to realize electrical interconnections between chips and leads, with bond quality verified through microscopic inspection.

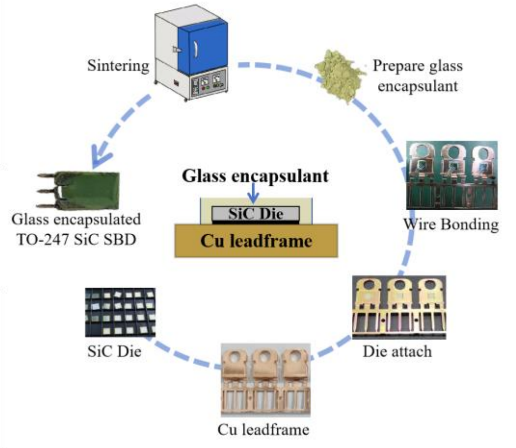

Fig. 1. Process flow of glass-encapsulated TO-247 SiC SBD.

The encapsulation stage included two schemes: the first was conventional plastic encapsulation, where plastic encapsulant material was heated, injection-molded, and shaped to improve the mechanical and environmental stability of the device. The second scheme employed a novel glass encapsulant material (provided by East China University of Science and Technology). The glass encapsulation was performed by placing the unencapsulated SiC SBD into a mold, adding the glass encapsulant powder, heating the assembly to 450 °C in a high-temperature furnace to melt and sinter the glass powder, and finally cooling naturally to room temperature to complete the encapsulation process. The detailed encapsulation process for the glass-encapsulated TO-247 packaged SiC SBD is illustrated in Fig. 1.

B. *High-Temperature Step-Stress Aging Test*

The high-temperature step-stress aging test was initiated by setting up an aging test platform and preparing test samples. Unlike traditional constant-temperature reliability tests, which operate at fixed temperatures typically aligned with silicon-based device limits (≤175 °C), the proposed method employs incremental temperature steps from 50 °C to 300 °C in 50 °C intervals, maintaining each step for 168 hours to simulate prolonged thermal exposure. This step-wise approach systematically explores temperature-dependent degradation mechanisms specific to wide-bandgap SiC schottky barrier diodes (SBDs), effectively revealing early-stage failures at intermediate temperatures, thus reducing the overall validation time compared to extended single-temperature tests. After each temperature increment, samples were cooled to room temperature for comprehensive static testing, capturing key parameter changes (e.g., reverse leakage current, forward voltage drop, and barrier height). Detected degradations were recorded and analyzed to plot detailed aging characteristic curves, facilitating accurate identification of critical failure thresholds. This methodology provides more granular and informative reliability data, significantly benefiting device design optimization and establishing rigorous operational benchmarks for high-temperature power electronics. The detailed procedure of the test is illustrated in Fig. 2.

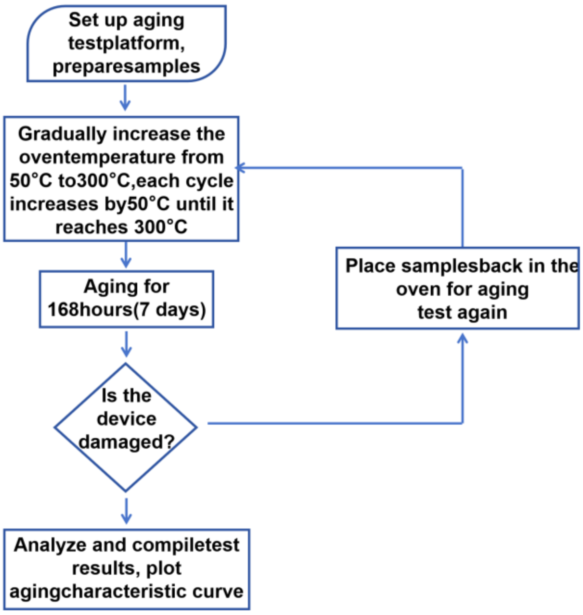

Fig. 2. High-temperature step-stress aging test flow.

III. RESULTS AND DISCUSSION

A. Static Performance Test Analysis

Firstly, devices assembled with different die-attach materials underwent static testing across various temperatures, and the results are illustrated in Fig. 3. Comparing the forward voltage drop (I-V) test results in Fig. 3(a) and 3(b), it can be observed that as operating temperature increased, the forward voltage drop (V_F) of devices bonded with either solder or pressureless sintered silver slightly increased. At a current of 10 A and temperature of 25 °C, the pressureless sintered silver exhibited a slightly lower V_F of 1.1 V compared to solder at 1.15 V, yet both maintained relatively low levels. As shown in Fig. 3(c) and 3(d), both device types demonstrated comparable reverse breakdown voltage (BV) performance, ranging consistently from 1620 V to 1680 V. Additionally, the Glass+Ag encapsulated devices similarly showed excellent static characteristics; further details can be found in the literature [4].

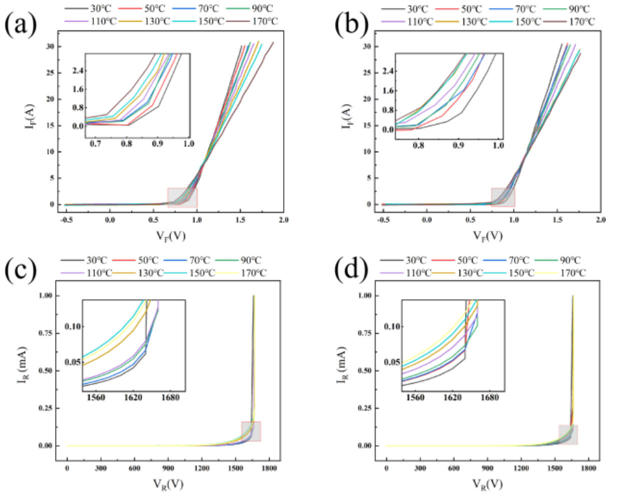

Fig. 3. Static tests at varying temperatures: Current-voltage (I-V) test results for (a) EMC+solder, (b) EMC+Ag; reverse breakdown voltage (BV) test results for (c) EMC+solder, (d) EMC+Ag.

B. Thermal Resistance Test Analysis

Fig. 4 illustrates the thermal resistance test results of the devices using the T3Ste method. The results indicate that the Epoxy Molding Compound (EMC)+solder devices exhibited the highest thermal resistance, approximately 0.56 °C/W (Fig. 4a). In comparison, the glass+Ag devices demonstrated improved sintering quality, resulting in a lower thermal resistance of 0.43 °C/W (Fig. 4c), thereby exhibiting superior thermal management performance. This difference primarily arises from the thermal conductivity of the packaging materials. Pressureless sintered silver possesses a thermal conductivity ranging from 200 to 400 W/(m·K), significantly higher than solder (approximately 50–60 W/(m·K)). Although the glass encapsulant material has a relatively lower thermal conductivity (~1 W/(m·°C)), it still surpasses EMC materials, whose thermal conductivity is generally below 1 W/(m·°C).

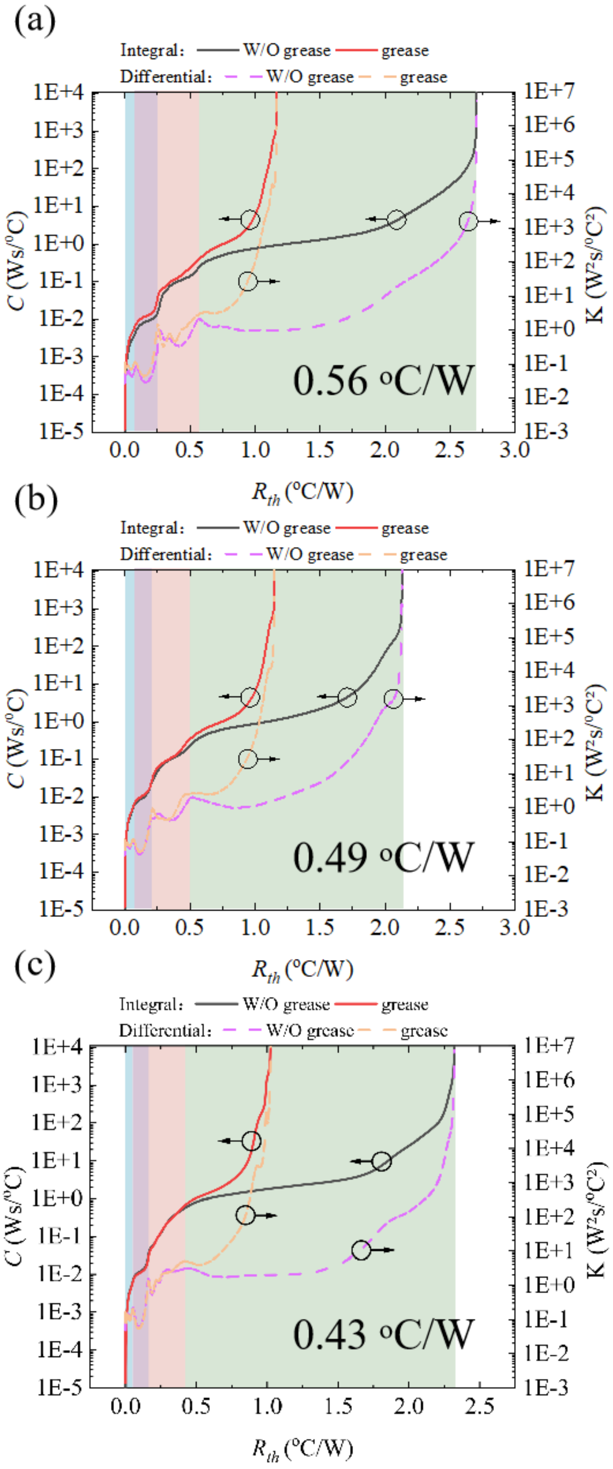

Fig. 4. Thermal resistance test results using T3Ste method: Thermal resistance measurements for (a) EMC+solder, (b) EMC+Ag, and (c) Glass+Ag devices.

To further investigate the influence of glass encapsulation materials on the thermal resistance performance of devices at different encapsulation temperatures, thermal resistance tests were conducted on devices prepared at three distinct encapsulation temperatures: 420 °C, 450 °C, and 480 °C. The results are presented in Fig. 5. The data indicate that as the encapsulation temperature increased from 420 °C to 450 °C, the thermal resistance significantly decreased from 0.8 °C/W to 0.325 °C/W. This reduction demonstrates that higher temperatures facilitate more complete glass melting, reducing internal porosity and consequently improving the overall encapsulation quality. However, when the encapsulation temperature further increased to 480 °C, the thermal resistance slightly rose to 0.4 °C/W. This increase is attributed to the formation of secondary bubbles due to overheating, negatively impacting the overall thermal conductivity of the glass encapsulation material and thereby increasing thermal resistance. This phenomenon underscores the importance of precisely controlling temperature during the encapsulation process to achieve optimal packaging quality and device performance.

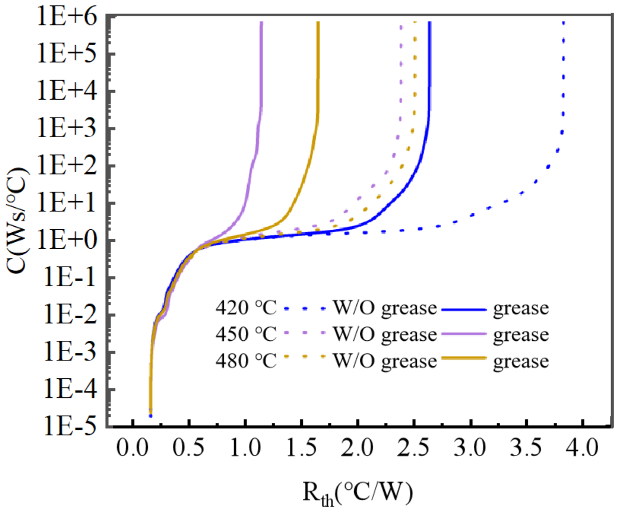

Fig. 5. Thermal resistance of glass-encapsulated SiC SBD at different encapsulation temperatures.

C. *High-Temperature Step-Stress Aging Test Result Analysis*

To evaluate the high-temperature stability of SiC SBD devices encapsulated with different materials, a high-temperature step-stress aging test was conducted. The devices were stored sequentially at temperatures of 50 °C, 100 °C, 150 °C, 200 °C, 250 °C, and 300 °C, with static performance measurements performed every 168 hours at each temperature, and an additional 168-hour aging at 300 °C. The stability of the forward voltage drop (V_F) is critical for assessing power device performance. Fig. 6 shows the changes in V_F for three types of devices after different aging periods. The results indicate that after 1176 hours of high-temperature testing, the V_F change for the glass+Ag encapsulated devices remained within 0.9%, satisfying standard performance requirements. In contrast, the EMC+Ag encapsulated devices exhibited a V_F change rate of 4.12% after a cumulative 840 hours at 250 °C. Furthermore, after an additional 168 hours at 300 °C, the V_F variation sharply increased to 74.4%, indicating potential device failure. Similarly, the EMC+solder encapsulated devices showed a V_F change of 51.4%. The test results clearly demonstrate that SiC SBDs encapsulated with glass-based materials have superior reliability at elevated temperatures compared to polymer-based encapsulation, highlighting the advantage of glass encapsulation in high-temperature applications, especially where long-term stability and reliability are required.

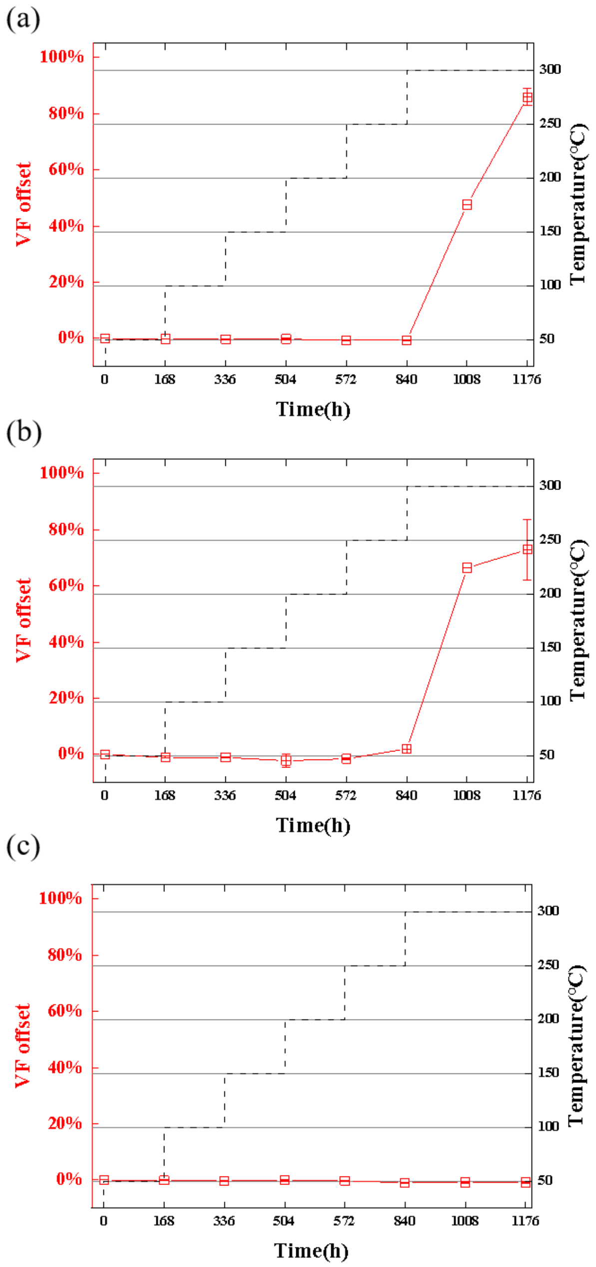

Fig. 6. Forward voltage (V_F) variation after high-temperature aging: V_F changes for (a) EMC+solder, (b) EMC+Ag, and (c) Glass+Ag devices over various aging durations.

D. *Finite Element Simulation Result Analysis*

To evaluate the effects of mismatched coefficients of thermal expansion (CTE) among different encapsulation materials on SiC SBD devices, finite element analysis (FEA) modeling and simulations were performed using ANSYS software for three types of encapsulated SiC SBDs. Fig. 7 and table I illustrate the finite element model developed based on the TO-247 package structure. Fig. 8 shows the equivalent stress distribution at 250 °C obtained from the simulation, revealing that the stresses were mainly concentrated at the interfaces between different materials. A refined mesh with high density was created around the chip wire bonding root and the interface between the glass encapsulation material and the lead frame to improve simulation accuracy.

TABLE I. FINITE ELEMENT SIMULATION PARAMETERS

Component	***Material***	***Thermal Conductivity (W/m·K)***	***Young's Modulus (GPa)***	***CTE*** $(\times 10^{-6}/°C)$
Chip	SiC	280	400	1.2
Bonding wire, frame	Copper alloy	401	110	18
Solder	Pb/Sn5	34	21.3	29
Pressureless Ag	Ag	320	15.11	20
Glass encapsulant	Glass	1.03	2.3	8.5
EMC	EMC	1.5	18	47

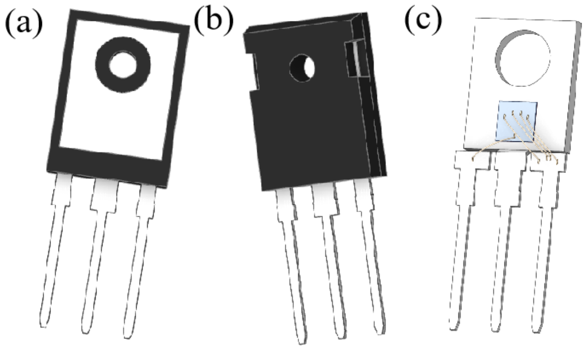

Fig. 7. Finite element model of glass-encapsulated SiC SBD (TO-247 Package): Views include (a) front view, (b) reverse view, and (c) model with encapsulant removed.

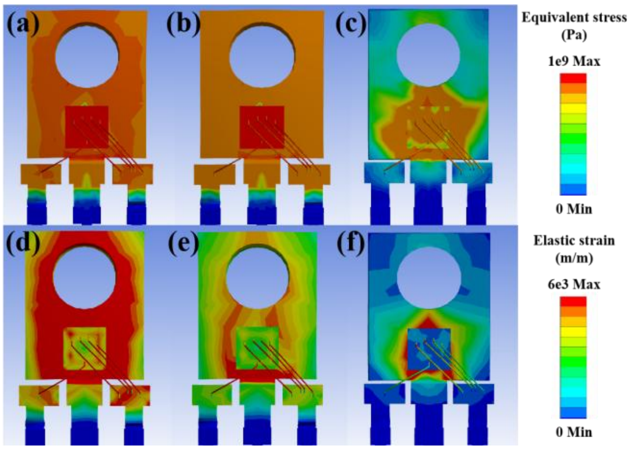

Fig. 8. Finite element simulation results: equivalent stress distribution cloud map for (a) EMC+solder, (b) EMC+Ag and (c) Glass+Ag; elastic strain distribution cloud map for (d) EMC+solder, (e) EMC+Ag and (f) Glass+Ag.

Finite element simulation results revealed that thermal stress within the device predominantly localized at interfacial regions between dissimilar materials, particularly at critical junctures such as the bonding interface between the SiC chip and solder layer, and the encapsulation interface connecting the chip surface to EMC (Fig. 8). Simulation results indicated that among the three packaging forms, the EMC+solder encapsulated devices exhibited the highest thermal stress at the SiC/solder interface, followed by EMC+Ag, while Glass+Ag had the lowest thermal stress. Thermal stresses primarily result from uneven expansion or contraction caused by CTE mismatch during temperature changes [4]. Since the glass encapsulation material has a CTE of approximately 8.48 ppm/°C, which is closer to that of the SiC chip (about 3.7 ppm/°C), materials with smaller differences in CTE experience more similar expansion or contraction rates during temperature variation, thus reducing stress induced by mismatch.

E. Failure Analysis

To assess pre- and post-aging integrity of the die-attach layer, scanning acoustic microscopy (CSAM) was conducted on the devices, with the results shown in Fig. 9. Comparing Fig. 9(a) and Fig. 9(c), obvious signs of melting, re-solidification, and crack formation are visible in the solder samples. In contrast, the sintered silver samples (Fig. 9(b) and Fig. 9(d)) exhibited no such phenomena. These findings indicate that when employing high-temperature resistant encapsulation materials like glass, it is crucial to use highly reliable die attach materials such as sintered silver to ensure overall packaging reliability.

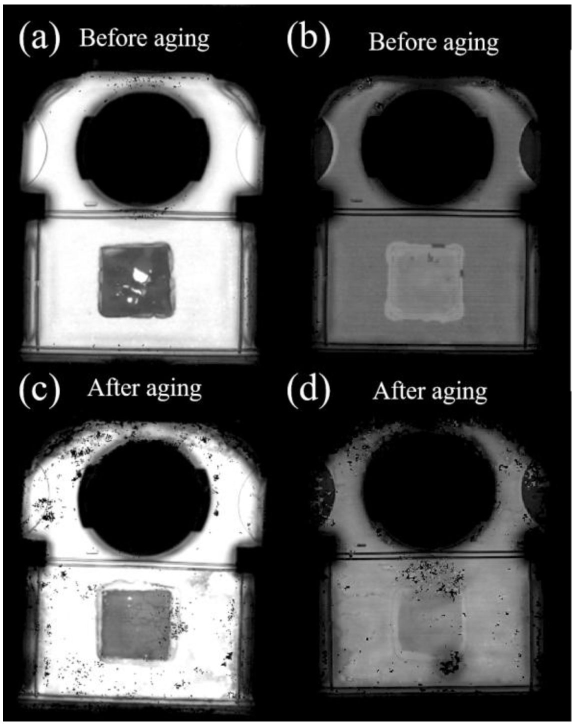

Fig. 9. CSAM analysis of die attach layers: comparison before aging (a) EMC+solder, (b) EMC+Ag and after aging (c) EMC+solder, (d) EMC+Ag.

IV. CONCLUSION

This study systematically investigated the high-temperature reliability of glass-encapsulated SiC Schottky diodes via a high-temperature step-stress aging test. By incrementally subjecting devices to thermal stress from 50 °C to 300 °C (with 50 °C steps maintained for 168 hours each) and integrating finite element analysis with comprehensive electrical characterization, the method effectively accelerated and revealed failure mechanisms under extreme conditions. The experimental results indicate that SiC schottky diodes fabricated using pressureless sintered silver for die attachment and a glass-based encapsulant exhibit significantly lower thermal resistance, reduced thermo-mechanical stress, and stable electrical performance compared to devices with conventional polymer encapsulation. These findings demonstrate the superior long-term reliability of the glass-encapsulation approach in high-temperature environments, thereby providing a robust pathway for optimizing power electronic packaging for applications in aerospace, nuclear, and other demanding sectors

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