On-chip Switched-Capacitor DC-DC converter for CMUT Biasing

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by

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for partial requirement to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Monday November 30, 2020 at 10:00 AM.

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TU Delft

Preface

I would like to place it on record that it would be near to impossible to complete the course without the constant support of my psychologist Dr. van der Knaap. I would also like to place my heartfelt gratitude to my supervisor Dr. Ir. Michiel A. P. Pertijs, for his constant support, guidance throughout the process of the thesis, and, more importantly, acknowledging my health issues and giving me the freedom to work at my own pace, especially during these extraordinary circumstances. If not for his support, I would have already packed my bags and kicking myself for not completing my masters. Also, special thanks to my daily supervisor Ir. Mingliang Tan for always being available when needed and motivating me to complete the thesis. Special thanks to Dr. Tiago Costa for being a part of the committee during these extraordinary circumstances. Preface would be not justified if I don't thank my friends Raghav, Blonde Arvind, Manoj, Karishma and Manojna from the bottom of my heart for all the support and dinners, which helped me with my panic attacks and often made me feel like I'm not alone. For all the weekend trips, doses of reality checks and so-called philosophical discussions ranging from Divya Spandana to Reema Sen. My sincere thanks to the support staff of Basic-Fit Sportschool Delft Leeuwenstein, who made me feel like home often at times when I felt alone.

Finally, I want to thank Joyce Siemers and my academic counsellors Mariëlle van Nijsten and Leonie Boortman for believing in me and sharing their enthusiastic energy and motivating me to complete my thesis. This journey wouldn't be possible without the moral and financial backing of my dad, mom, sister, brother-in-law, and my dear nephew Aarav. Also, for believing that I would graduate one day :).

Finally, I want to say to my friends (Raghav, Blonde Arvind, and Manoj) that "Let's party".

र्वधर्मान् परित्यज्य मामेकं शरणं व्रज ।
अहं त्वां सर्वपापेभ्यो मोक्षयिष्यामि मा शुचः ॥ ६६ ॥

A. Vijaykumar
Delft, November 2020

Abstract

CAPACITVE micromachined ultrasonic transducer (CMUT) technology has been considered as a promising alternative for the conventional piezo electric-based technology in ultrasound imaging systems. Its potential advantages include better image quality, higher operational frequency, and ease of fabrication and integration with CMOS read-out circuitry. However, CMUTs usually need high-voltage DC bias in order to transmit and receive acoustic waves.

This work presents the design of a DC-DC converter to bias a CMUT for ultrasound imaging systems. Two different cases have been investigated: biasing at 63 V from an input of 5 V using a fully-integrated converter realized in a 180nm BCD technology that can handle up to 65V; and biasing at 120 V by employing minimal off-chip components.

The proposed work explores the transient properties of a conventional on-chip switched capacitor DC-DC converter: the Dickson charge pump. A MATLAB model of the Dickson charge pump is developed to understand the relation between dynamic efficiency and the charge pump capacitor. Prior research works suggest that the dynamic efficiency of the Dickson charge pump is limited for a particular number of stages. However, the results obtained from the MATLAB model suggests that the dynamic efficiency can be improved by making the charge pump capacitor smaller. Various circuit simulations have been done to understand the results obtained from the MATLAB model. When the charge pump capacitor becomes very small, the parasitics start dominating and affect the overall efficiency of the Dickson charge pump. An optimization strategy is discussed to find the optimum number of stages and charge pump capacitor value to maximize the dynamic efficiency and minimize the circuit area. Based on the results obtained from this study, a DC-DC converter is designed to bias the CMUT at 63V, which consumes an estimated circuit area of 0.6586mm^2 and has a simulated efficiency of 0.752.

In addition, a new design idea that incorporates two DC-DC converters to bias the CMUT beyond the process voltage limitations is also discussed in this thesis. This hybrid converter involves the optimized DC-DC converter designed earlier to generate 63V from an input of 5V, a control unit circuit, and some off-chip components. The hybrid converter designed consumes an estimated circuit area of $0.842mm^2$ and has a simulated efficiency of 0.577.

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1 Introduction

1.1. Background

Capacitive micromachined ultrasonic transducers (CMUTs) have become a competitive alternative for next-generation ultrasound imaging systems. The CMUT is operated using electrostatic forces created by an applied DC bias voltage, which causes the membrane to deflect towards the substrate, as shown in Fig.1.1. The membrane is triggered by an AC pulse imposed on the bias voltage, coupling acoustic power to the surrounding medium to vibrate. However, CMUTs usually need high-voltage DC bias in order to transmit and receive acoustic waves.

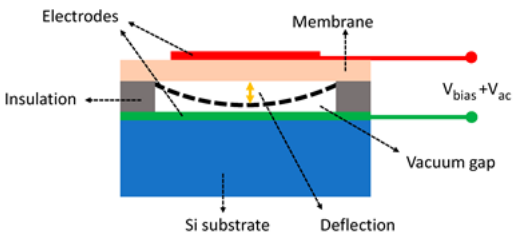

Figure 1.1: Typical structure of a CMUT in the cross-sectional view (reproduced from [1]

1.2. Prior art

Figure 1.2 depicts a simple block diagram of a transceiver for medical ultrasound imaging applications based on a CMUT [2]. In most cases, the biasing voltage V_B is provided externally for biasing the CMUT. It is applied to the CMUT via an RC-network that AC grounds the terminal of the CMUT to which the DC bias is applied. In the case of a transducer array consisting of many CMUT elements, the DC bias can be applied to a common electrode shared by all elements.

Only limited research work has been done to integrate the biasing network and CMUT transceiver unit. Such integration is crucial for battery-powered ultrasound imaging devices and requires that the biasing voltage is generated using a DC-DC converter. There are many challenges associated with designing the DC-DC converter on-chip. The converter should be compatible with process limitations and should preferably not rely on inductors, as these are hard to integrate on a chip.

The research work described in [4] uses an on-chip switched-capacitor DC-DC converter, which provides a DC bias of maximum 18.22V from an 5V input in 0.8m high-voltage technology. However, the DC bias obtained is too low for many CMUTs, and requires additional circuitry to provide high voltage bias. This thesis explores the on-chip switched-capacitor DC-DC converter and improves its conversion ratio and efficiency for CMUT biasing.

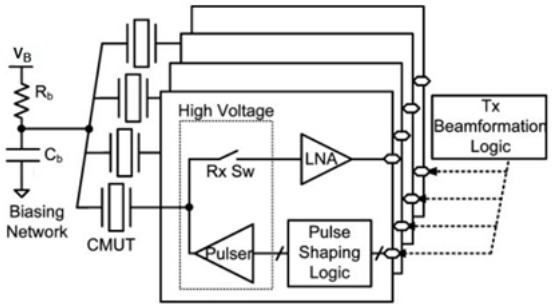

Figure 1.2: Simple transceiver block diagram for medical ultrasound imaging applications using a CMUT(reproduced from [2]

1.3. Design objectives

This project's primary goal is to design a DC-DC converter to bias a CMUT in a 180nm BCD technology that can handle up to 65V. The DC-DC converter designed aims at maximizing the efficiency during the conversion process and minimizing the circuit area. Two different cases are considered: generating a bias voltage of 63V from an input voltage of 5V without using off-chip components; and generating a bias voltage of 120 V. To bias the CMUT at 120V in 180nm BCD technology, which is beyond the process voltage limitation, an idea must be formulated that incorporates some components off-chip and an on-chip power converter that can generate up to the process voltage limitations. The blocking capacitor C_b as shown in Fig. 1.2, forms the main load that needs to be driven by the DC-DC converter. This is because the capacitor C_b is typically at least an order-of-magnitude larger than the capacitance of the CMUT (or the combined capacitance of the CMUT elements in a transducer array), in the order of few hundreds of nano Farad, so as to provide a proper AC ground. For this reason, the load for the DC-DC converter is chosen as C_{load} = 100nF.

1.4. Thesis organization

This report is divided into five chapters. Chapter 2 presents a review of the transient-mode Dickson charge pump. In chapter 3, a design for biasing the CMUT at 63V with a 1mm2 area budget is discussed. Chapter 4 describes a hybrid converter design idea for biasing the CMUT beyond the process voltage limitations. The hybrid converter's circuit schematic and simulation results are also discussed in this chapter. Finally, a conclusion is presented in Chapter 5.

2

Transient-mode Dickson charge pump

In this chapter, the transient mode of the Dickson charge pump is reviewed. It includes three main parts. The first part is an analysis of the conventional Dickson charge pump, which introduces the working principle and the dynamic properties. The key features and properties of the Dickson charge pump are presented in section 2.1. A MATLAB numerical model of the Dickson charge pump is shown in section 2.2. Based on the analysis of the Dickson charge pump, a variation compared to the conventional mode of operation is found and explained in section 2.3. Subsequently, an optimization strategy is discussed for designing the charge pump for biasing the CMUT at a required target voltage of 63V, which is explained in section 2.4.

2.1. Dickson charge pump

In this section, the working principle of the Dickson charge pump is presented. Following that, the dynamic properties and the fundamental limitations of the Dickson charge pump are discussed.

2.1.1. Single-stage Dickson charge pump

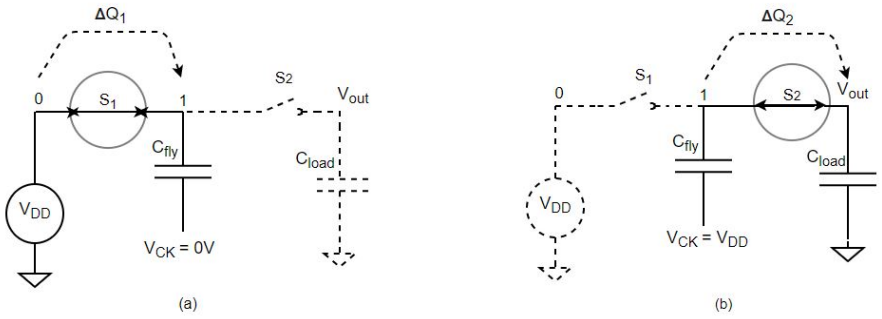

Figure 2.1: Single-stage Dickson charge pump during (a) VCK is Low (b) VCK is High

A simple one-stage topology is considered to demonstrate the working principle of an ideal Dickson charge pump [5] driving a capacitive load, as shown in Figure 2.1 . It consists of a single pumping capacitor (C_{fly}), two switches (S_1 and S_2) that are operating in two complementary phases, a clock signal (V_{CK}) with an amplitude equal to the power supply (V_{DD}) as shown in Figure 2.2, and a capacitive load (C_{load}).

Figure 2.2: Single-stage Dickson charge pump during (a) VCK is Low (b) VCK is High

During the first half cycle of V_{CK} (0 to T/2), S_1 is closed while S_2 is open. C_{fly} is charged to V_{DD} (2.1(a)) through S_1. Then, the switches change their state in the second half cycle (T/2, T), V_{CK} is switched to V_{DD} (2.2(b)), and part of the charge stored in C_{fly} is moved to C_{load} so that the output voltage is increased. The same charge transferring process repeats in every cycle so that the output voltage will continue to increase until it reaches the final steady-state value, $2V_{DD}$. The following recursive equation can describe this process:

$$V_{out}(j) = \frac{\left(2 \times C_{fly} \times V_{DD}\right) + C_{\text{load}} \times V_{out}(j-1)}{C_{fly} + C_{\text{load}}} \quad \text{where } j \geq 1 \tag{2.1}$$

where j represents the clock cycles. Several clock cycles are needed to reach $2V_{DD}$, and in each successive clock cycle, the step increase in the output voltage becomes smaller. Nevertheless, the output voltage will rise rapidly in the first part of the transient and gradually proceed to its final value, where there is preferably no charge redistribution. In conclusion, a simple single-stage Dickson charge pump takes charge from the power supply through the C_{fly} capacitor. It pumps this charge into the output capacitor C_{load}, increasing the output voltage to an ideal value twice the power supply.

2.1.2. N-stage Dickson charge pump

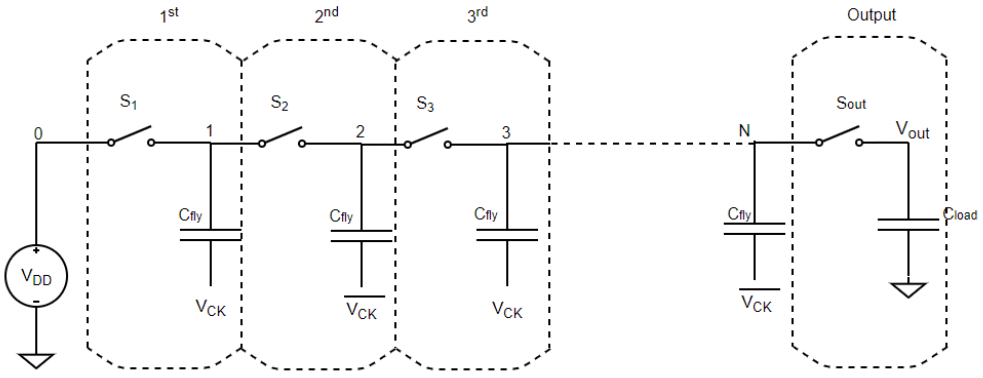

Figure 2.3: N-stage Dickson charge pump

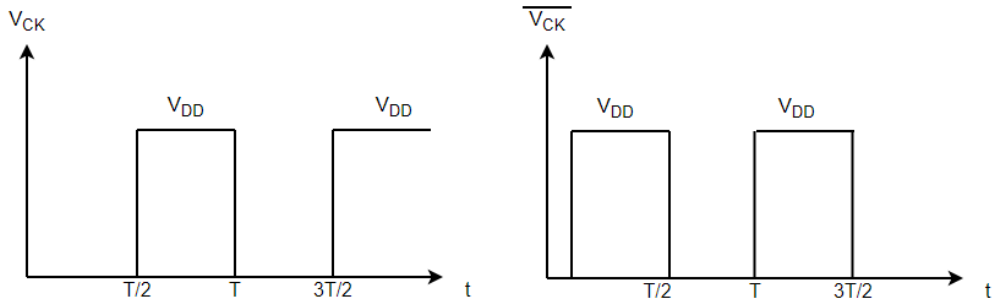

Figure 2.4: Waveform of the clock signals

The N-stage Dickson charge pump can be obtained by cascading a single-stage charge pump, as shown in 2.3. Each stage consists of a C_{fly} pumping capacitor and a switch. A two-phase clock is needed for the Dickson charge pump, and the final stage switch S_{out} is also required to connect the output load.

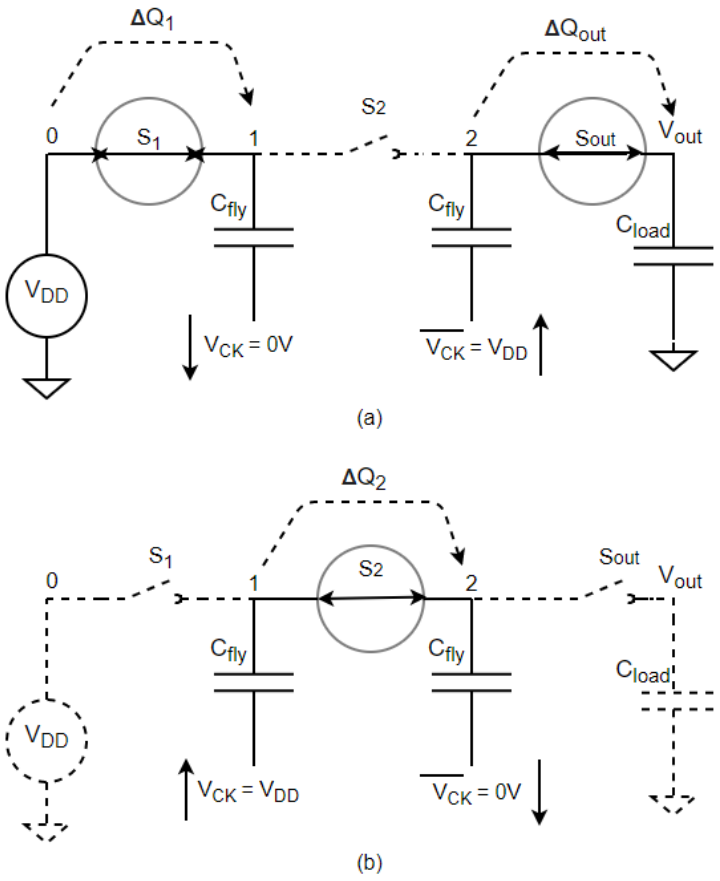

Figure 2.5: The schematic of charge transfer flow

The charge transfer behaviour of the Dickson charge pump with N stages is similar to that of a single-stage Dickson charge pump. V_{CK} is low, and only the odd-numbered switches are closed during the first half clock cycle, as shown in 2.5(a). Therefore, the first pumping capacitor is charged to V_{DD}, and all other pumping capacitors in the odd stages distribute the charge with the capacitor in the previous stage. In the second half clock cycle, the clock signal V_{CK} is equal to V_{DD}, and only the even-numbered switches are closed, as shown in 2.5(b). After that, all the capacitors in the odd stages distribute the charge with the capacitor in the even

stage. This charge redistribution process repeats until the charge pump reaches its steady state.

To summarize, each C_{fly} capacitor receives charge from the capacitor at its left side and gives a part of this charge to the capacitor at its right side in an entire clock period. Therefore, there is a charge transfer from the power supply to the output load in each period.

2.1.3. Dynamic properties

This section will briefly explain the dynamic properties of the Dickson charge pump. The instantaneous output voltage, rise time, and dynamic efficiency are the key dynamic parameters of the Dickson charge pump. The analytical results of these critical parameters have been derived in [6] and are discussed below. For an N-stage Dickson charge pump, the output voltage for the j^{th} cycle in the ideal case is given by

$$V_{\text{out}}(j) = (N+1) \times V_{DD} - \left(N \times V_{DD} \times \beta^j\right) \tag{2.2}$$

$$\beta = \left(1 + \left(\frac{\text{C}_{\text{fly}}}{N \times C_{OUT}}\right)^{-1}, \text{ where } \quad C_{OUT} = C_{\text{load}} + C_{PMP}\right. \tag{2.3}$$

$$C_{PMP} = A(N) \times C_{fly}, \quad \text{where} \quad A(N) = \begin{cases} \frac{4N^2+3N+2}{12(N+1)} \text{ when } N \text{ is even} \\ \frac{4N^2-N-3}{12N} \text{ when } N \text{ is odd} \end{cases} \tag{2.4}$$

C_{load} is the load capacitance, and C_{PMP} is the self-load capacitance of the charge pump. C_{PMP} is approximately one-third of the charge pump's total capacitance, which equals $\frac{NC_{fly}}{3}$, and its error is less than 3% for N>=4 and less than 7% for N>=5 [6]. During the steady-state where j tends to infinitity, β equals 0 and V_{out} equals (N+1)V_{DD} , calculated using equations 2.2 to 2.4.

In practice, the switches in a Dickson charge pump will introduce non-idealities, mainly the forward threshold voltage drop of the diodes. Besides, the flying capacitors will also be associated with parasitic capacitance [7]. Figure 2.6 shows a single stage of a multi-stage charge pump with parasitic capacitance C_T and the forward voltage drop of the diode V_T. Including these non-idealities, the output voltage for cycle j is given by:

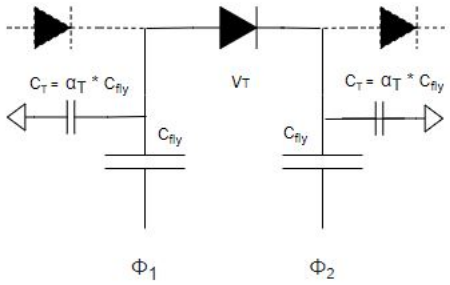

Figure 2.6: The schematic of a charge-pump stage with non-idealities

$$V_{\text{out}}(j) = N\left(\frac{V_{DD}}{1+\alpha_T} - V_T\right) + (V_{DD} - V_T) - N\left(\frac{V_{DD}}{1+\alpha_T} - V_T\right)\beta^j, \quad \text{where} \quad \alpha_T = \frac{C_T}{C_{fly}} \tag{2.5}$$

$$\beta = \left(1 + \left(\frac{(1+\alpha_T) \times C_{fly}}{N \times C_{OUT}}\right)\right)^{-1}, \quad \text{where} \quad C_{OUT} = C_{\text{Load}} + C_{PMP} \tag{2.6}$$

$$C_{PMP} = A(N) \times C_{fly}, \quad \text{where} A(N) = \begin{cases} \frac{4N^2+3N+2}{12(N+1)} \text{ when 'N' is even} \\ \frac{4N^2-N-3}{12N} \text{ when 'N' is odd} \end{cases} \tag{2.7}$$

The rise time T_R is defined as the time needed for the output voltage V_{out} to rise from V_g to V_{PP}, where V_{PP} is the required target voltage, and V_g is the initial output voltage. It can be obtained by solving equation

(2.5) with the boundary conditions.

$$V_g = V_{DD}$$
$$V_{out}(J) = V_{PP}$$
$$J = \frac{T_R}{T_0}$$

$$T_R = \frac{\ln\left(1 - \left(\frac{V_{PP} - V_g}{N \times V_g}\right)\right)}{\ln(\beta)} \tag{2.8}$$

The analytical results obtained from equations (2.5 and 2.8) agree with the simulation results within 10% for the rise time and output voltage [6]

Dynamic Efficiency η_{dyn} is the ratio between integrated energy delivered to the load and total integrated energy consumed by the input sources from the start-up to the J^{th} clock cycle. It is a crucial parameter involved in designing the Dickson charge pump for biasing the CMUT. Dynamic efficiency for an N-stage Dickson charge pump is given by [8]

$$\eta_{dyn}(J) = \frac{V_{out}(J) + V_{DD}}{2 \times (N+1) \times V_{DD}}, \text{For ideal case} \tag{2.9}$$

$$\eta_{dyn}(J) = \frac{V_{out}(J) + V_{DD} - V_T}{2 \times (N+1) \times V_{DD}}, \text{For non-ideal case} \tag{2.10}$$

Equations (2.5 and 2.8) estimate the output voltage $V_{out}(J)$ and rise time T_R for the J^{th} clock cycle. In section 2.3, these expressions will be compared with circuit simulation results.

2.1.4. Fundamental limitations

From equations (2.9 and 2.10), we see that the dynamic efficiency η_{dyn} or the efficiency during the transient phase for a Dickson charge pump is limited even for an ideal case. For a single-stage Dickson charge pump, the dynamic efficiency equals 75% during the transient phase for an ideal case and equals 66% for a two-stage Dickson charge pump. As the number of stages increases, the dynamic efficiency settles to approximately 50% at time T_R, calculated using equation 2.8. Table 2.1 summarizes the results obtained for dynamic efficiency η_{dyn} with the number of stages for the Dickson charge pump ranging from 1 to 16. Fig. 2.7 depicts the trend in efficiency for different stages of the Dickson charge pump. The target voltage V_{PP} is chosen as the steady-state value obtained using equation 2.2 for the ideal case, and for the non-ideal case using equation 2.5. Since we are interested in the transient behavior of the power converter for our application, the overall dynamic efficiency during the rise time is limited according to the equations derived in [6]. It becomes a very crucial performance metric to consider.

Number of stages (N)	Dynamic efficiency for an ideal case	Dynamic efficiency for the non-ideal case
1	0.75	0.72
2	0.66	0.64
3	0.625	0.60
12	0.538	0.517
14	0.533	0.512
16	0.529	0.508

Table 2.1: Dynamic efficiency at T_R for Ideal and Non-ideal case (V_T =0.2V)

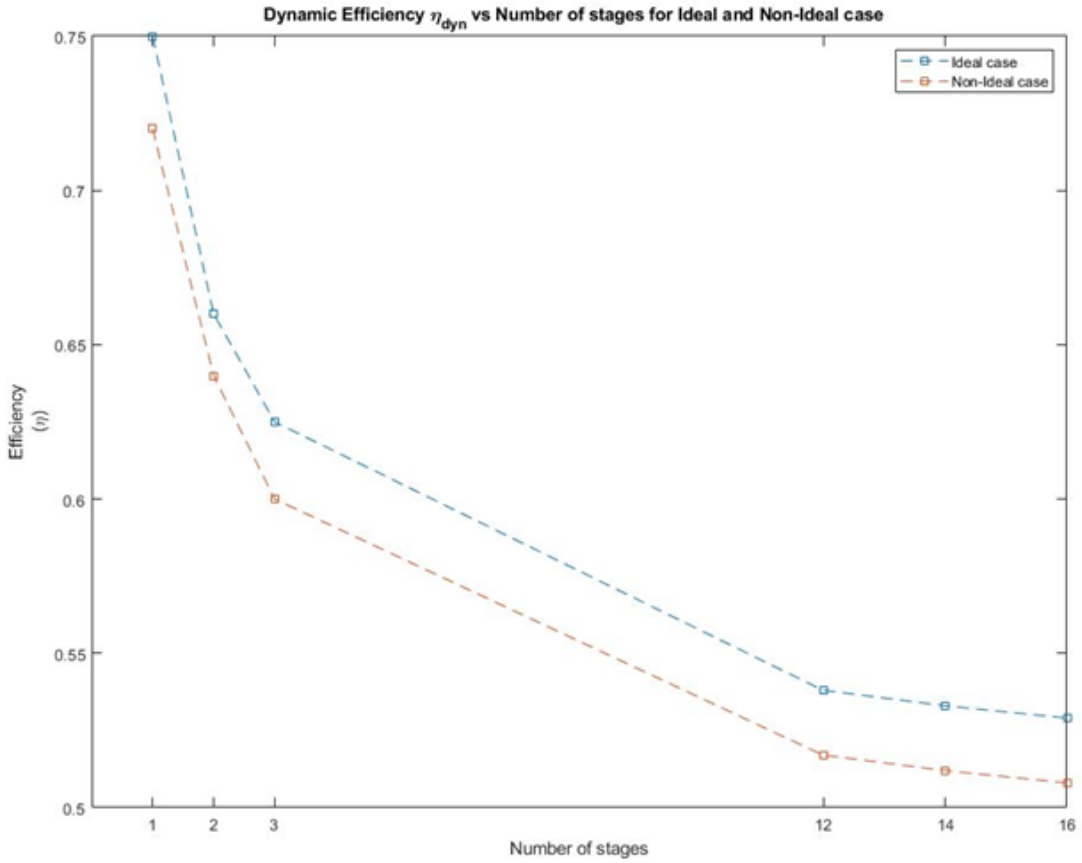

Figure 2.7: Dynamic efficiency for Ideal and Non-ideal case

2.2. MATLAB numerical model

To further analyze the dynamic efficiency, a numerical model of the Dickson charge pump is developed in MATLAB. The instantaneous output voltage, rise time, and dynamic efficiency are analyzed and compared with the theoretical expressions and circuit simulation results based on this model.

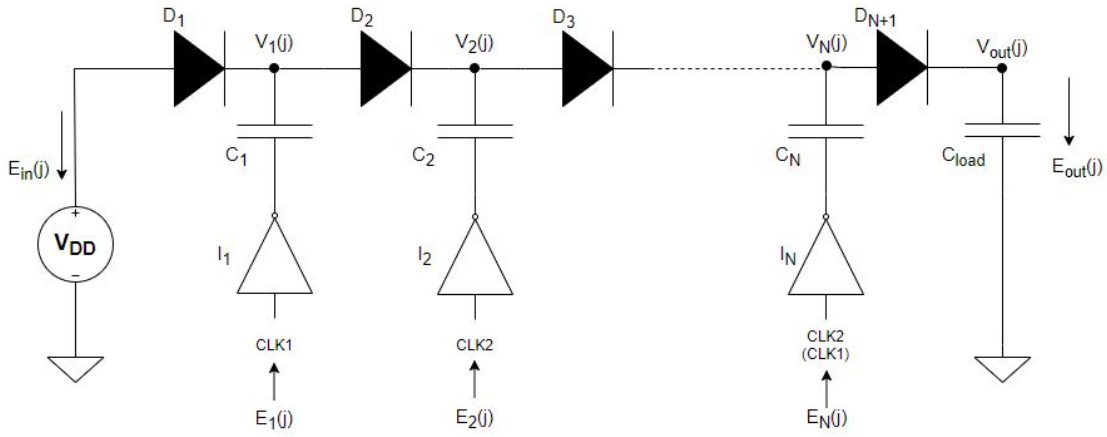

Figure 2.8: N-stage Dickson charge pump model

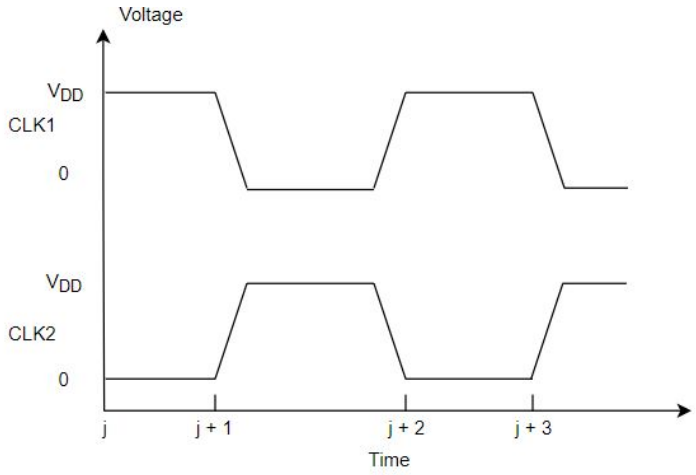

Figure 2.9: Timing diagram for clock signals CLK1 and CLK2

Fig. 2.8 illustrates the N-stage Dickson charge pump circuit. A charge pump with an even number of stages was considered for this analysis, while a similar approach can also be made for an odd number of stages. V_{DD} is the supply voltage. C_{fly} is the flying capacitor. D_i $(1 \leq i \leq N)$ is the diode. I_i $(1 \leq i \leq N)$ is the clock source driving each charge pump stage, and C_{load} is the load capacitor. $V_i(j)$ $(1 \leq i \leq N)$ is the instantaneous nodal voltage at each stage i during half clock cycle j. $E_{in}(j)$ is the instantaneous energy consumed by the input source V_{DD}. E_i(j) $(1 \leq i \leq N)$ is the instantaneous energy consumed by the clock sources driving the capacitor's bottom plate at each stage of the Dickson charge pump. E_{out}(j) is the energy delivered to the load capacitor.

The following assumptions were made for this analysis

1. Each charge pump capacitor has a constant value of C_{fly}, and the parasitic associated with each of them is negligible.
2. Each diode has a constant threshold voltage V_T, where for the ideal case V_T = 0V and for the non-ideal case VT = 0.2V.
3. Each flying capacitor C_{fly} and the load capacitor C_{load} are pre-charged to the supply voltage V_{DD}.
4. A capacitive load is considered, and parasitic capacitance associated with the load capacitor is negligible.

2.2.1. Instantaneous voltage expression

This section derives an expression for the instantaneous voltage at each node of the Dickson charge pump. Phase 1 and 2 combined results in one clock cycle (j=2).

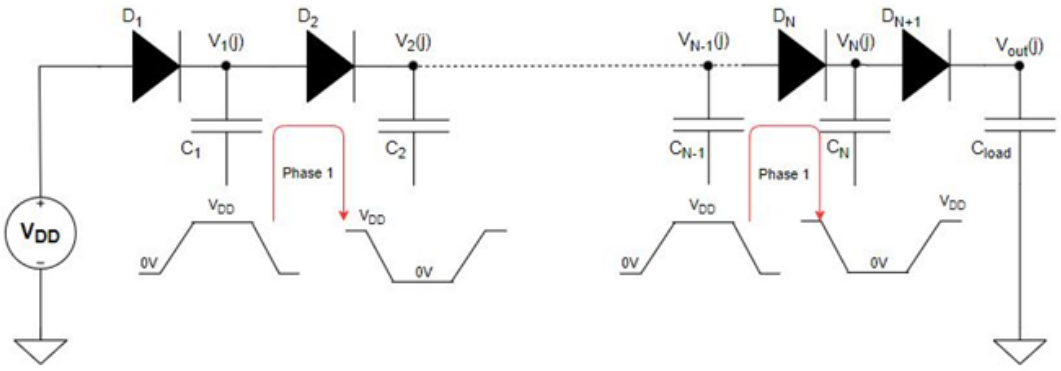

Figure 2.10: N-stage Dickson charge pump during phase 1

In phase 1, CLK1 is high (V_{DD}), and CLK2 is low (0). Therefore, the odd clock inputs I_1, I_3, I_5.....I_{N-1} drives the bottom plate of the charge pump capacitor of respective stages with the voltage of V_{DD}. As a result, charge redistribution happens between nodes 1 and 2, 3 and 4. . . .., N-1 and N, respectively, where the even-numbered diodes are forward biased, as shown in Fig. 2.10. Based on the charge redistribution principles, the final voltage expressions during phase 1 are:

$$V_n(j+1) = 0.5 \times \left(V_n(j) + V_{n+1}(j) + V_T\right) \tag{2.11}$$

$$V_{n+1}(j+1) = V_n(j+1) - V_T \tag{2.12}$$

where n ranges from 1 to N-1, the load capacitor is not involved in the charge redistribution during phase 1, as shown in Fig. 2.10

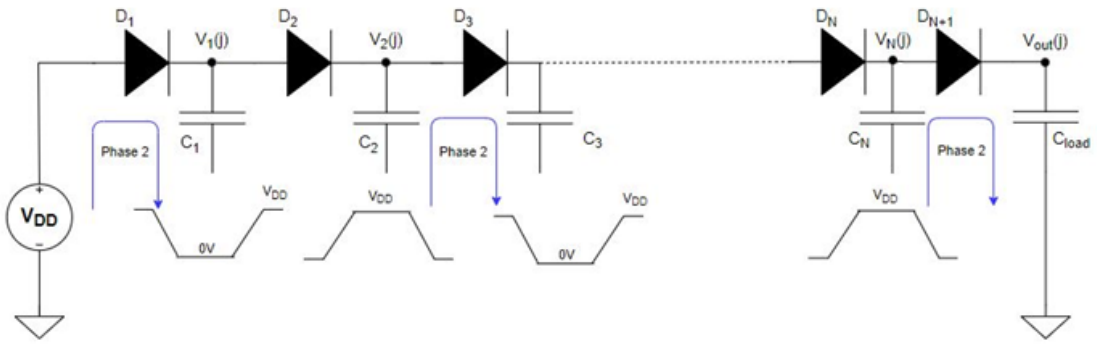

Figure 2.11: N-stage Dickson charge pump during phase 2

In phase 2, CLK2 is high (V_{DD}), and CLK1 is low (0). Thus the even clock inputs I_2, I_4, I_6.....I_N drives the bottom plate of the charge pump capacitor of respective stages with the voltage of V_{DD}. As a result, charge redistribution happens between nodes 2 and 3, 4 and 5. . . .., N and the output node, respectively, where odd-numbered diodes are forward biased, as shown in Fig. 2.11. Based on the charge redistribution principles, the final voltage expressions during phase 2 are derived as shown below,

$$V_1(j+2) = (V_{CC} - V_T) \tag{2.13}$$

$$V_{n+1}(j+2) = 0.5 \times \left(V_{n+1}(j+1) + V_{n+2}(j+1) + V_T\right) \tag{2.14}$$

$$V_{n+2}(j+2) = V_{n+2}(j+2) - V_T \tag{2.15}$$

$$V_N(j+2) = \frac{C_{\text{load}}}{C_{\text{load}} + C_{\text{fly}}} \times \left(\left(\frac{C_{fly}}{C_{\text{load}}} \times \left(V_N(j+1) + V_{DD}\right)\right) + V_{\text{out}}(j+1) + V_T\right) \tag{2.16}$$

$$V_{\text{out}}(j+2) = V_N(j+2) - V_T \tag{2.17}$$

where n ranges from 1 to N-3. As shown in Fig. 2.11, there is charge redistribution between node N and the output node reflected in equations 2.16 and 2.17. At node 1, the bottom plate of the capacitor C_1 is pulled down to 0V from V_{DD}, and the input V_{DD} charges the capacitor C_1 back to $V_{DD} - V_T$ where V_T is the threshold voltage drop of diode D_1 as shown in equation 2.13. Equations 2.14 and 2.15 follow the same principle discussed during phase 1, while in this phase, charge redistribution happens among the flying capacitors between nodes 2 and 3, 4 and 5. . . .., N and the output node, respectively.

A generic MATLAB model can be obtained for the Dickson charge pump's voltage expressions from 2.11 to 2.17. Similarly, the energy expressions are derived in the next section.

2.2.2. Energy expression

This section derives instantaneous energy expressions at each node of the Dickson charge pump in the presence of the clock inputs. Phase 1 and 2 combined results in one clock cycle (j=2).

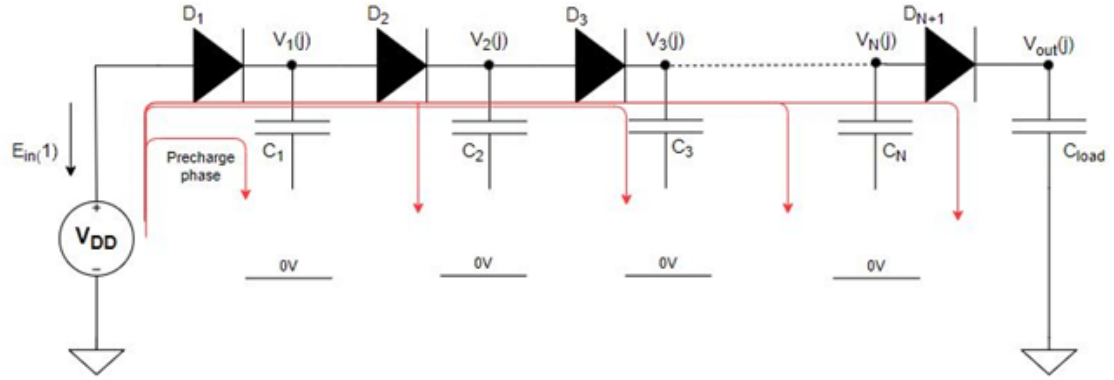

Figure 2.12: The schematic of the charge transfer flow during the pre-charge phase

During the pre-charge phase, $E_{in}(1)$ is the energy consumed during the pre-charging of all the capacitors present in the Dickson charge pump.

$$\mathrm{E_{in}}(1) = \left(N \times C_{fly} \times (V_{DD})^2\right) + \left(C_{\mathrm{load}} \times (V_{DD})^2\right) \tag{2.18}$$

Since all clock inputs are not provided during this pre-charge phase,

$$E_i(1) = 0 \quad \text{, where } 1 \le i \le N \tag{2.19}$$

The energy delivered to the load capacitor during this phase is calculated as shown below,

$$E_{\mathrm{load}}(1) = 0.5 \times C_{\mathrm{load}} \times (V_{DD})^2 \tag{2.20}$$

In phase 1, CLK1 is high (V_{DD}), and CLK2 is low (0). Thus the odd clock inputs I_1, I_3, I_5.....I_{N-1} drive the bottom plate of the charge pump capacitor of respective stages with the voltage of V_{DD}. As a result, charge redistribution happens between nodes 1 and 2, 3 and 4.....N-1 and N, respectively, where even-numbered diodes are forward biased, as shown in Fig. 2.13. As seen in this figure, there is no energy delivered to the load capacitor in this phase. Clock sources I_1, I_3, I_5.....I_{N-1} consumes energy while transferring the charge to the successive capacitors, represented by E_i(j) where $1 \le i \le N-1$ and 'i' take only odd values. The energy consumed by these clock sources is calculated using the following equation:

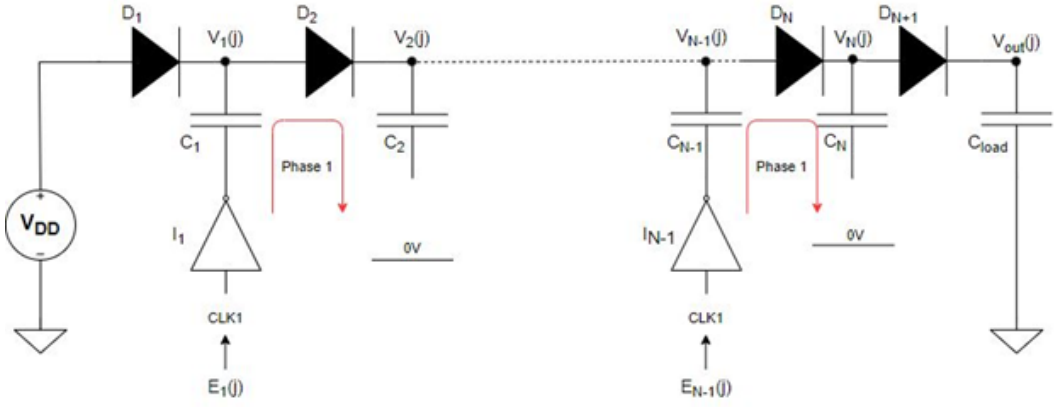

Figure 2.13: The schematic of the charge transfer flow during phase 1

$$E_i(j) = \frac{1}{2} \times C_{fly} \times \left(\left(V_{i+1}(j)^2 - \left(V_{i+1}(j-1) - 5\right)^2\right)\right) + \frac{1}{2} \times C_{fly} \times \left(\left(V_i(j) - 5\right)^2 - V_i(j-1)^2\right) + \frac{1}{2} \times C_{eff} \times \left(V_i(j) - V_i(j-1) + 5\right)^2 \tag{2.21}$$

The first term in 2.21 corresponds to the change in energy stored in the capacitor C_{i+1}, the second term in the equation corresponds to the change in energy stored in the capacitor C_i, and the third term in the equation corresponds to the energy consumed by the diode D_i for the clock source I_i. In this phase, there is no energy delivered to the load capacitor, and there is no energy consumed by the input source V_{DD} as well:

$$E_{out}(j) = 0 \text{ and } E_{in}(j) = 0 \tag{2.22}$$

In phase 2, CLK2 is high (V_{DD}), and CLK1 is low (0). Thus, the even clock inputs I_2, I_4, I_6.....I_N drives the bottom plate of the charge pump capacitor of respective stages with the voltage of V_{DD}. As a result, charge redistribution happens between nodes 2 and 3, 4 and 5.....N and the output node, respectively, where odd-numbered diodes are forward biased, as shown in Fig. 2.14. As seen in this figure, some energy is delivered to the load capacitor, and the input source V_{DD} consumes some energy in this phase. Clock sources I_2, I_4, I_6.....I_N consume energy while transferring charge to the successive capacitors, represented by E_i(j) where $1 \leq i \leq N$ and i takes only even values. Energy consumed by these clock sources is calculated as follows:

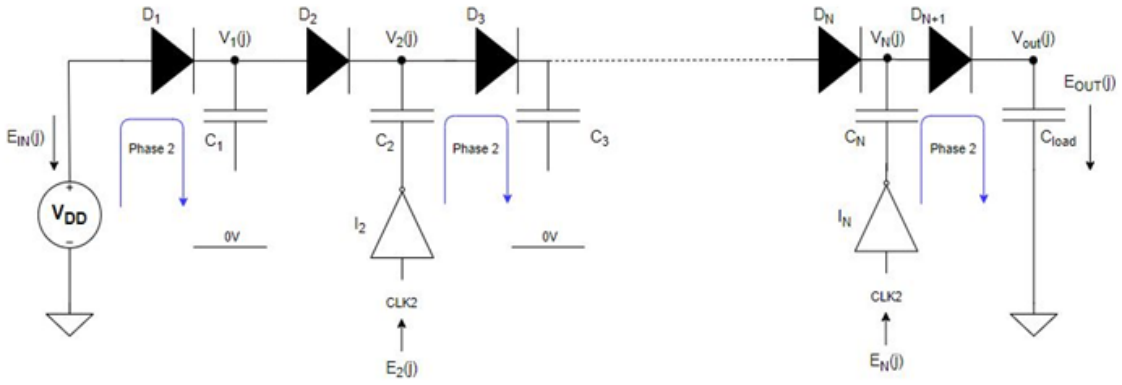

Figure 2.14: The schematic of the charge transfer flow during phase2

$$E_i(j) = \frac{1}{2} \times C_{fly} \times \left(\left(V_{i+1}(j)^2 - \left(V_{i+1}(j-1) - 5 \right)^2 \right) \right) + \frac{1}{2} \times C_{fly} \times \left(\left(V_i(j) - 5 \right)^2 - V_i(j-1)^2 \right) + \frac{1}{2} \times C_{eff} \times \left(V_i(j) - V_i(j-1) + 5 \right)^2 \tag{2.23}$$

Equation 2.23 is derived using the same principle as in equation 2.21. In this phase, some energy is delivered to the load capacitor, calculated by estimating the change in energy stored in the load capacitor after charge redistribution:

$$E_{out}(j) = \frac{1}{2} \times C_{\text{load}} \times \left(V_{\text{out}}(j)^2 - V_{\text{out}}(j-1)^2 \right) \tag{2.24}$$

At node 1, in this phase, the bottom plate of the capacitor C_1 is pulled to 0V from V_{DD} (previous clock cycle), and the input V_{DD} charges the capacitor C_1 back to $V_{DD} - V_T$. Energy consumed by source V_{DD} equals the change in the energy stored in the first flying capacitor after pulling the bottom plate of C_1 from 5 V to 0V:

$$E_{in}(j) = \frac{1}{2} \times C_{fly} \times \left(V_1(j)^2 - \left(V_1(j-1) - 5 \right)^2 \right) \tag{2.25}$$

However, in this equation, the energy consumed by the diode is neglected because the results do not vary much compared with the circuit simulation results for a large number of clock cycles. Dynamic efficiency during the transient period η_{dyn} (j) which is also explained in Section 2.1.3, can be calculated iteratively as shown in the equation below,

$$\eta_{dyn}(j) = \frac{\sum_{j=1}^{K} E_{out}(j)}{\sum_{i=1}^{N} \sum_{j=1}^{K} E_i(j) + \sum_{j=1}^{K} E_{in}(j)} \tag{2.26}$$

Where j is the half clock cycle number, K is the total number of clock cycles, N is the number of stages of the Dickson charge pump.

A generic MATLAB model can be obtained for the Dickson charge pump's energy expressions from 2.18 to 2.26 . With this MATLAB model, we can further investigate the dynamic energy efficiency η_{dyn} results compared to equations 2.9 and 2.10 and its validity compared with circuit simulation results.

2.3. Simulation results

In this section, results obtained from a MATLAB model based on the equations introduced in the previous section are compared to results obtained using a circuit simulator for different values of C_{fly} and different numbers of stages with the same C_{load}. It is done first for the ideal case, i.e., without parasitics and assuming ideal switches, and then for the non-ideal case with a diode having a threshold voltage drop. It allows us to understand the trade-off between the efficiency and design parameters, thus providing more clear design choices for a specific target.

2.3.1. Ideal case

2.3.1.1 Efficiency vs. C_{fly} from MATLAB model

This section shows the MATLAB model results of the ideal Dickson charge pump for different stages. The following assumptions were made for this analysis,

1. V_{DD} = 5V, where V_{DD} is the input source of the Dickson charge pump.
2. C_{load} = 100nF.
3. C_{fly} is varied from 2 pF to 120 pF with different discrete steps.
4. V_T =0 , since an ideal case is assumed for this section.
5. N is the number of stages and varies from 12 to 16 with a step size of 2.

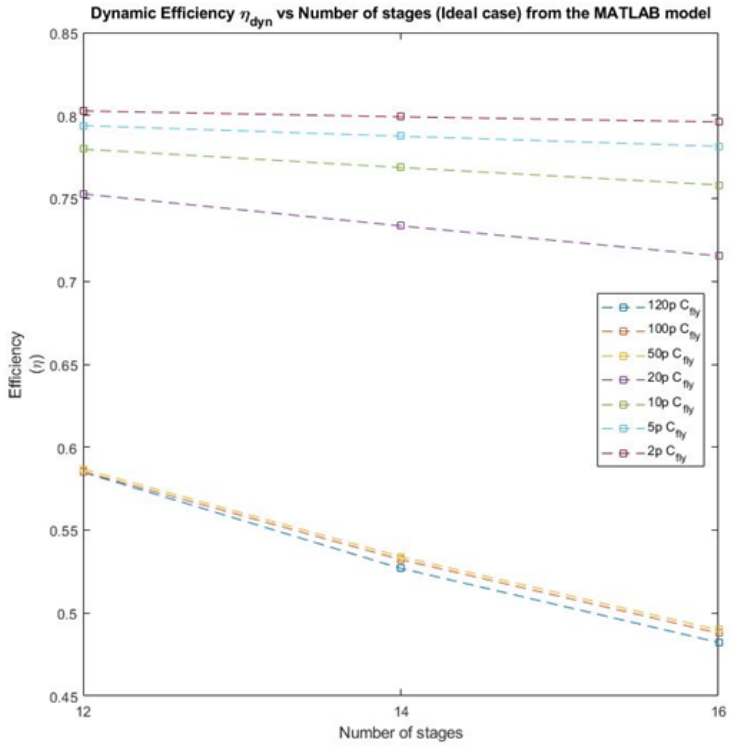

Figure 2.15: Dynamic efficiency vs. Number of stages (Ideal case) from the MATLAB model for different C_{fly}

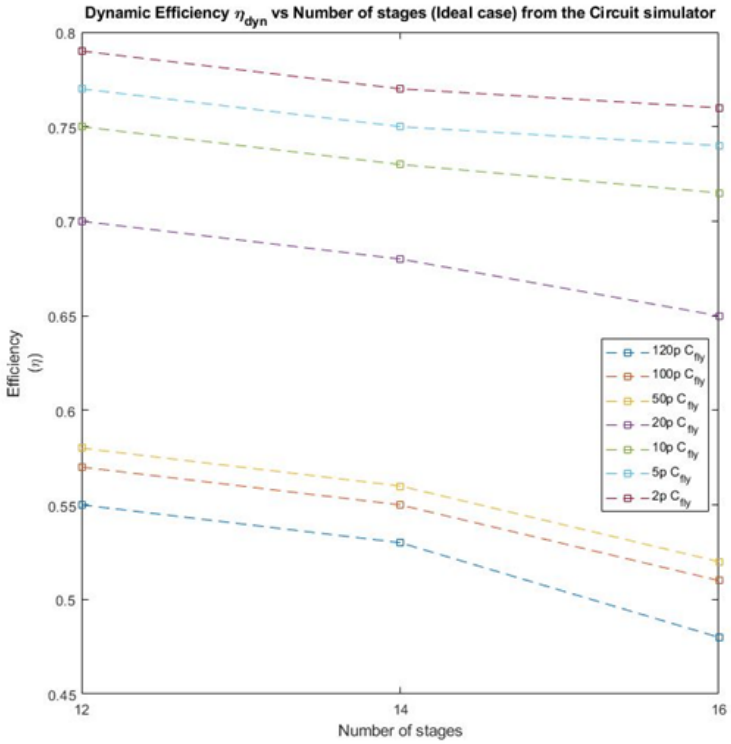

Figure 2.16: Dynamic efficiency vs. Number of stages (Ideal case) from the circuit simulator for different C_{fly}

	N=12	N=14	N=16
C_{fly}	η_{dyn}	η_{dyn}	η_{dyn}
2pF	0.8027	0.7992	0.7961
5pF	0.7939	0.7875	0.7814
10pF	0.7797	0.7686	0.7581
20pF	0.7527	0.7334	0.7153
50pF	0.5868	0.534	0.4898
100pF	0.5852	0.5332	0.4879
120pF	0.5849	0.5269	0.4823

Table 2.2: Dynamic efficiency vs. Number of stages (Ideal case) from the MATLAB model for different C_{fly}

Table 2.2 summarizes the MATLAB model results of the Dickson charge pump with C_{fly} ranging from 2pF to 120pF for the ideal case. Fig. 2.15 depicts the results obtained from the MATLAB model for N=12, N=14, and N=16, where 'N' is the number of stages. From this plot, we observe that the dynamic efficiency η_{dyn} varies with the charge pump capacitor C_{fly} for the same load capacitor value C_{load}, which contradicts the equation 2.9. Dynamic efficiency η_{dyn} is higher for smaller C_{fly} values, which vary from the values expected from this equation. However, for larger C_{fly} values, the dynamic efficiency η_{dyn} is similar to this equation's expected values. Hence, we can design a Dickson charge pump for a smaller charge pump capacitor C_{fly}, requiring a smaller area to achieve maximum dynamic efficiency. To further investigate this result, the same design setup was translated into a circuit simulator and analyzed.

2.3.1.2 Efficiency vs. C_{fly} from circuit simulations

This section shows the results obtained from the circuit simulator to compare the results obtained from the MATLAB model of the Dickson charge pump for an ideal case for a different number of stages. The same

parameter values have been used for this analysis.

	N=12	N=14	N=16
C_{fly}	η_{dyn}	η_{dyn}	η_{dyn}
2pF	0.79	0.77	0.76
5pF	0.77	0.75	0.74
10pF	0.75	0.73	0.715
20pF	0.70	0.68	0.65
50pF	0.58	0.56	0.52
100pF	0.57	0.55	0.51
120pF	0.55	0.53	0.48

Table 2.3: Dynamic efficiency vs. Number of stages (Ideal case) from the circuit simulator for different C_{fly}

Table 2.3 summarizes the circuit simulator results of the Dickson charge pump with C_{fly} ranging from 2pF to 120pF for the ideal case. Figure 2.16 depicts the results obtained from circuit simulations for N=12, N=14, and N=16, where 'N' is the number of stages. From this plot, we observe that the dynamic efficiency η_{dyn} varies with the charge pump capacitor C_{fly} for the same load capacitor value C_{load}, which coincides with the MATLAB model results for the Dickson charge pump as shown in Figure 2.15. Moreover, the same trend in dynamic efficiency η_{dyn} is observed for the circuit simulator results of the Dickson charge pump compared to the MATLAB model results. The dynamic efficiency η_{dyn} values vary within 1 percent compared to values found in the MATLAB model for the ideal case.

2.3.1.3 Summary

The results obtained from the circuit simulator and MATLAB model of the Dickson charge pump match well.

The following observations were made while comparing the results obtained from sections 2.3.1.1 and 2.3.1.2

1. We see that the dynamic efficiency η_{dyn} increases as C_{fly} becomes smaller from the MATLAB model, which is also seen from the circuit simulator for an ideal case but contradicts with the values obtained from equations (2.9) and (2.10) derived in the paper[]. These equations have been approximated using mathematical equations and fail to consider the complete dependence of the charge pump capacitor C_{fly}. However, the MATLAB model calculates the dynamic efficiency in each clock cycle and does not make any approximation.

2. We also observe that the dynamic efficiency decreases with an increase in the number of stages N for the same charge pump capacitor C_{fly} and load capacitor C_{load}.

2.3.2. Non - ideal case

In this section, the comparison between MATLAB simulation results and circuit simulation results is extended to the non-ideal case, i.e., including the diode with threshold, for different charge pump capacitor C_{fly} while maintaining the same load capacitor C_{load}, for a different number of stages. We could understand the trend in dynamic efficiency η_{dyn} and the MATLAB model's validity compared to circuit simulations with this analysis.

2.3.2.1 Efficiency vs. C_{fly} from MATLAB model

This section shows the results obtained from the MATLAB model of a non-ideal Dickson charge pump for a different number of stages. In this model, only the diode threshold drop is considered since it is challenging to include the other non-idealities in MATLAB. However, this analysis still analyzes dynamic efficiency trends and verifies the contradicting results seen in the Dickson charge pump's ideal case in section 2.3.1 The same assumptions made in section 2.3.1 applies for this case with the additional assumption V_T=0.2V.

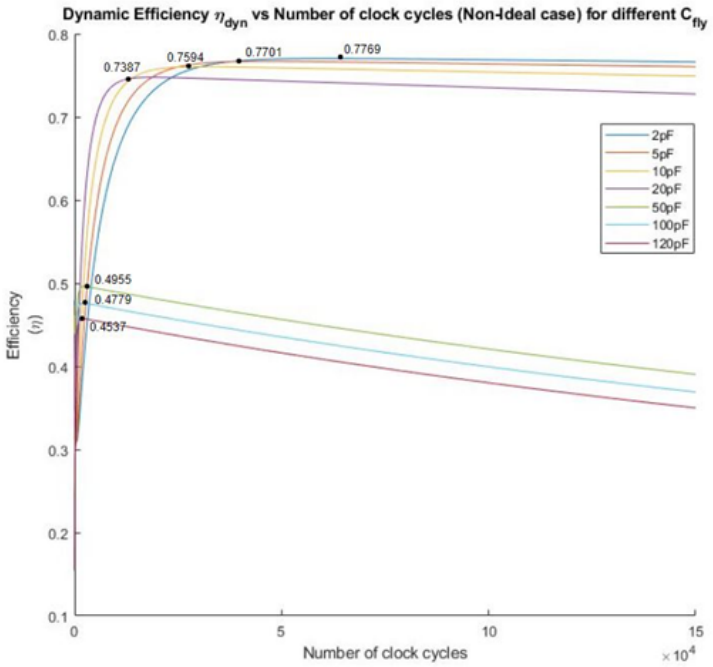

Figure 2.17: Dynamic efficiency vs. Number of clock cycles (Non-ideal case) from the MATLAB model for different C_{fly}, N=12

Fig. 2.17 depicts the results obtained from the MATLAB model of the Dickson charge pump for N=12, where 'N' is the number of stages, and the diodes in the model have a threshold voltage of V_T= 0.2V. We observe that for the non-ideal case after reaching a maximum voltage at the output, for a minimal increase in output energy delivered to the load capacitor, the input sources have to spend a considerable amount of energy as it still requires to conduct the diode during each clock cycle with constant threshold voltage drop. Therefore, the dynamic efficiency reaches a peak value $\eta_{dyn,peak}$, and degrades after the maximum output voltage is achieved for the non-ideal case of the Dickson charge pump.

	N=12	N=14	N=16
C_{fly}	η_{dyn}	η_{dyn}	η_{dyn}
2pF	0.7769	0.7751	0.7735
5pF	0.7701	0.7674	0.7646
10pF	0.7594	0.7544	0.75
20pF	0.7387	0.7301	0.7235
50pF	0.4955	0.4649	0.4378
100pF	0.4779	0.4487	0.4193
120pF	0.4537	0.4219	0.3943

Table 2.4: Peak dynamic efficiency vs. Number of stages (Non-ideal case) from the MATLAB model for different C_{fly}

Table 2.4 summarizes MATLAB model results of the Dickson charge pump with C_{fly} ranging from 2pF to 120pF for the non-ideal case. Figure 2.18 depicts the results obtained from the MATLAB model for N=12, N=14, and N=16, where 'N' is the number of stages. From this plot, we observe that the peak dynamic efficiency $\eta_{dyn,peak}$ for the non-ideal case, and the dynamic efficiency η_{dyn} for the ideal case described in section 2.3.1 vary in the same trend with respect to the charge pump capacitor C_{fly}. To further investigate this result, the same design setup was translated into a circuit simulator and analyzed.

2.3.2.2 Efficiency vs. C_{fly} from circuit simulations

This section shows the results obtained from the circuit simulator to compare the results obtained from the MATLAB model of the non-ideal Dickson charge pump for a different number of stages. The simulation parameters that were used in the MATLAB model are also used for this analysis. Since real diodes and ca-

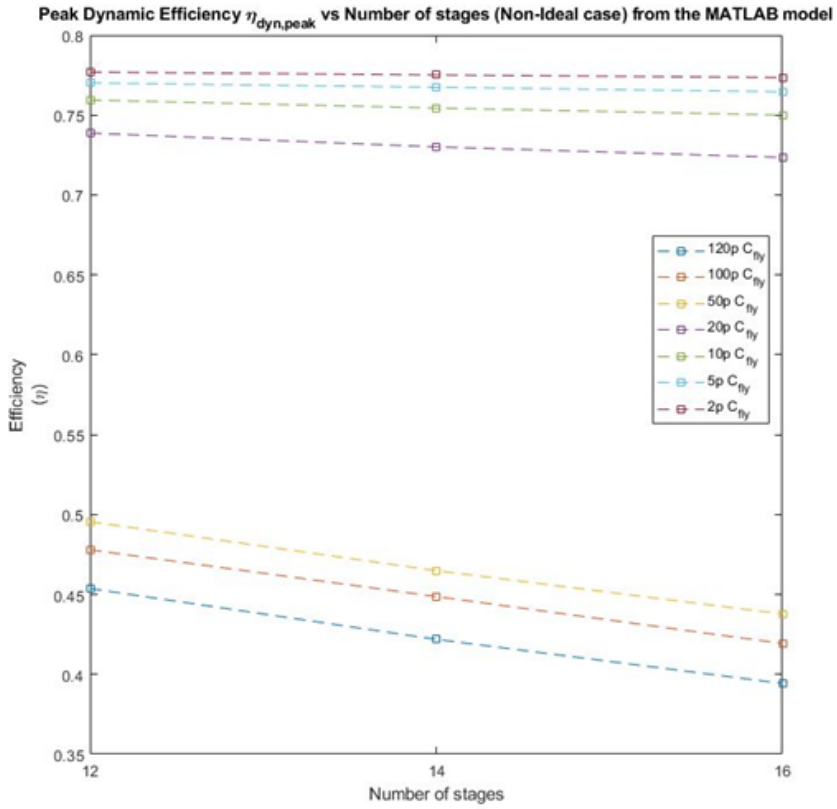

Figure 2.18: Peak dynamic efficiency vs. Number of stages (Non-ideal case) from the MATLAB model for different C_{fly}

pacitors are used, the non-idealities like threshold voltage drop and top plate parasitics of the charge pump capacitor as described in Fig. 2.6 might affect the results compared to that of the MATLAB model.

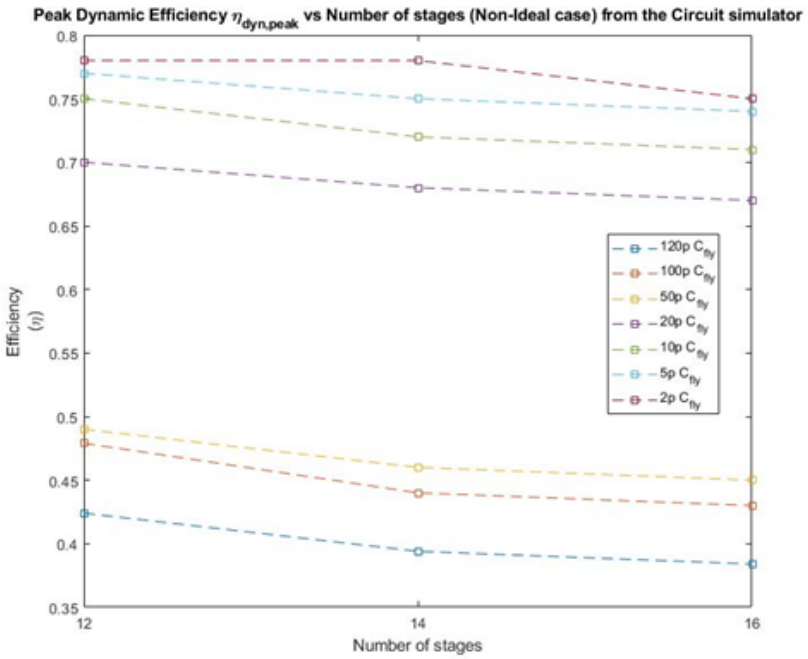

Figure 2.19: Peak dynamic efficiency vs. Number of stages (Non-ideal case) from the circuit simulator for different C_{fly}

	N=12		N=14		N=16	
C_{fly}	η_{dyn}	V_{PP}	η_{dyn}	V_{PP}	η_{dyn}	V_{PP}
2pF	0.78	34.9V	0.78	36.3V	0.75	38.5V
5pF	0.77	36.3V	0.75	39.4V	0.74	40.6V
10pF	0.75	39.15V	0.72	42.2V	0.71	44.2V
20pF	0.7	43.2V	0.68	46V	0.67	50.8V
50pF	0.49	47V	0.46	49.9V	0.45	56V
100pF	0.479	53.2V	0.44	56V	0.43	60.8V
120pF	0.424	58V	0.394	60.2V	0.384	63V

Table 2.5: Peak dynamic efficiency vs. Number of stages (Non-ideal case) from the circuit simulator for different C_{fly}

Table 2.5 summarizes the circuit simulator results of the Dickson charge pump with C_{fly} ranging from 2pF to 120pF for the non-ideal case. Figure 2.19 depicts the results obtained from the circuit simulations for N=12, N=14, and N=16, where 'N' is the number of stages. From this plot, we observe that the peak dynamic efficiency $\eta_{dyn,peak}$ varies with the charge pump capacitor C_{fly} for the same load capacitor value C_{load}, which coincides with the MATLAB model results for the Dickson charge pump as shown in Figure 2.18. Moreover, the same trend in peak dynamic efficiency $\eta_{dyn,peak}$ is observed for the circuit simulator results compared to the MATLAB model results for the non-ideal case of the Dickson charge pump. However, because of the domination of top plate parasitics, the maximum attainable output voltage V_{PP} decreases as C_{fly} decreases, which is also seen in equation2.5. As α_T increases, V_{PP} decreases. This trend is not observed in the MATLAB model since the top plate parasitics of the charge pump capacitor were not considered.

2.3.2.3 Summary

From the results obtained from the circuit simulator and MATLAB model of the non-ideal Dickson charge pump, the trend in the dynamic efficiency matches well.

The following observations were made while comparing the results obtained from sections 2.3.2.1 and 2.3.2.2

1. We see that the dynamic efficiency increases as C_{fly} becomes smaller from the MATLAB model and the circuit simulator for a non-ideal case but is not the same as predicted in the equations 2.9 and 2.10 derived in the paper[].

2. We observe a peak in dynamic efficiency after the maximum output voltage V_{PP} is achieved, since there is almost no charge redistribution happening with the load capacitor C_{load}. After reaching a maximum voltage, we need to spend more massive energy on the input sources for a minimal increase in output energy delivered to the load capacitor. It still requires to conduct the diode during each clock cycle, which has a constant threshold voltage drop.

3. We observe that the peak dynamic efficiency decreases with an increase in the number of stages N, for the same charge pump capacitor C_{fly} and load capacitor C_{load}.

4. We also observe that the maximum output voltage V_{PP} decreases as C_{fly} decreases for the non-ideal case from the circuit simulator because of the top plate parasitics of the charge pump capacitor. Therefore, to achieve the target voltage using a smaller C_{fly}, we might increase the stages. To achieve maximum dynamic efficiency and minimum area, we could make the charge pump capacitor C_{fly} smaller and increase the number of stages. There is an optimum number of stages and C_{fly} values resulting in higher efficiency and a smaller circuit area.

   Since there are many parameters involved, an optimization strategy must be formulated to find the optimum number of stages N and C_{fly} values. An optimization strategy has been discussed and planned for biasing the CMUT at a required target voltage, which will be discussed in the next section.

2.4. Optimization strategy

As discussed in the previous section, an optimization strategy is required for biasing the CMUT at 63V as there are so many parameters involved in designing it. From the previous sections, we concluded that as C_{fly} decreases, peak dynamic efficiency increases, but parasitic effects also increase. When the parasitic effects dominate, there would be a drop in the charge pump's maximum attainable voltage. In such cases, we have to

increase the number of stages to achieve the target voltage. Ideally, we would like to design the charge pump for a smaller area and better efficiency.

Therefore we need two analysis for designing the charge pump for biasing the CMUT:

1. Efficiency vs. C_{fly} for different number of stages

   From this analysis, we can obtain the value of C_{fly} and the number of stages that would achieve the maximum dynamic efficiency for an output voltage of 63V.

2. Area vs. maximum efficiency for different C_{fly}

   From this analysis, we can now estimate the area required for achieving maximum efficiency for each C_{fly}. With this result, we can design the charge pumps for the required target voltage while achieving maximum efficiency and minimum circuit area.

3

Charge pump prototype

In this chapter, the design of a prototype for biasing the CMUT at 63 V with a 1 mm^2 area budget is presented. It includes three main parts. The first part is the discussion of the design choices in a Dickson charge pump. The second part discusses the optimization of energy efficiency within certain area limitations. Finally, circuit implementation and simulation results of the finalized Dickson charge pump circuit are presented.

3.1. Design choices

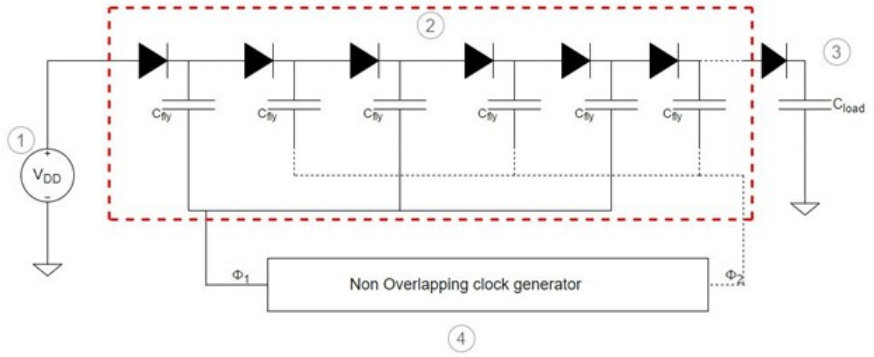

Figure 3.1: Dickson charge pump classified into blocks

The process available for designing the charge pump is the TSMC 180nm BCD technology. All the design choices made in this section are restricted to this technology. Although the results may vary with different processes, the design flow would be similar irrespective of the chosen process. For a typical Dickson charge pump, there are four significant blocks, as shown in Fig.3.1. The design choices chosen for these blocks will be described in detail below.

3.1.1. Input source

The charge pump aims to boost the battery voltage to 63 V for biasing the CMUT. The Li-ion battery operates between 3.0 V and 4.2 V [9]. In this prototype, we apply 5 V as the input source for simplicity. The design methodology will also apply to other battery voltages.

3.1.2. Intermediate stage

In this stage, several design choices have to be made, which are the realization of the diode, the value of the flying capacitors C_{fly}, and the number of stages *N*. To implement the diode realization of the Dickson charge pump, the voltage difference between the successive stages must be further examined. A simple 2-stage Dickson charge pump with ideal diodes driven by non-overlapping clock signals $\phi 1$ and $\phi 2$ is considered as shown in Fig3.2. In Fig.3.3, the simulated results for this ideal circuit are shown, and we can observe that the voltage

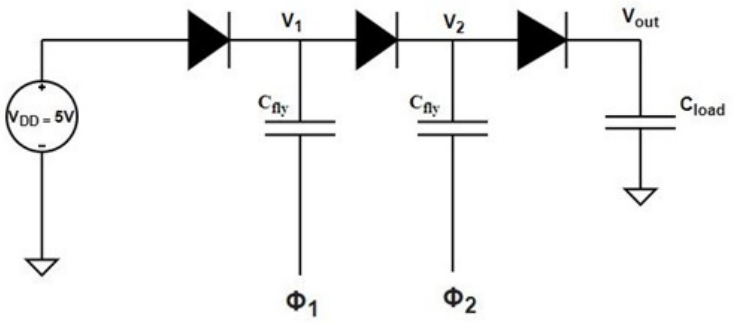

Figure 3.2: 2-stage Dickson charge pump

difference between V_1 and V_2 during the steady-state is 10V, which is twice the input voltage when $\phi 2$ is high, and $\phi 1$ is low. Therefore, when the diodes are realized using real components, it must withstand twice the input voltage (10V in our case).

In 180 nm BCD technology, the maximum achievable voltage is 65 V. In this technology, the diode can be implemented by MOSFET, BJT, or the Schottky diode. MOSFET used in this technology can only handle a V_{GS} of a maximum of 5V. If we use MOSFET for realizing diode in the Dickson charge pump as shown in Fig.3.4, we need a V_{GS} of 10V. The voltage difference between the Dickson charge pump's successive stages is twice as the input voltage, 2-V_{DD}=10V. Therefore, diode-connected MOSFET is not suitable for designing the charge pump because of the V_{GS} limitations. The V_{CE} of the BJTs can handle higher voltages. However, the substrate of the BJTs available in this technology can only handle a maximum of 40V, which is not desirable as we are planning to achieve a target voltage of 63V. Schottky diodes, which can handle a maximum of 63V and have a threshold voltage of V_T =0.2V, will be a suitable choice for the prototype. MOM capacitors are chosen in this design since they are the only capacitor type that can handle a high voltage of 63V in this technology. The choice of the capacitor size and the number of stages will be optimized for maximum efficiency within the targeted area, discussed in Sec.3.2.

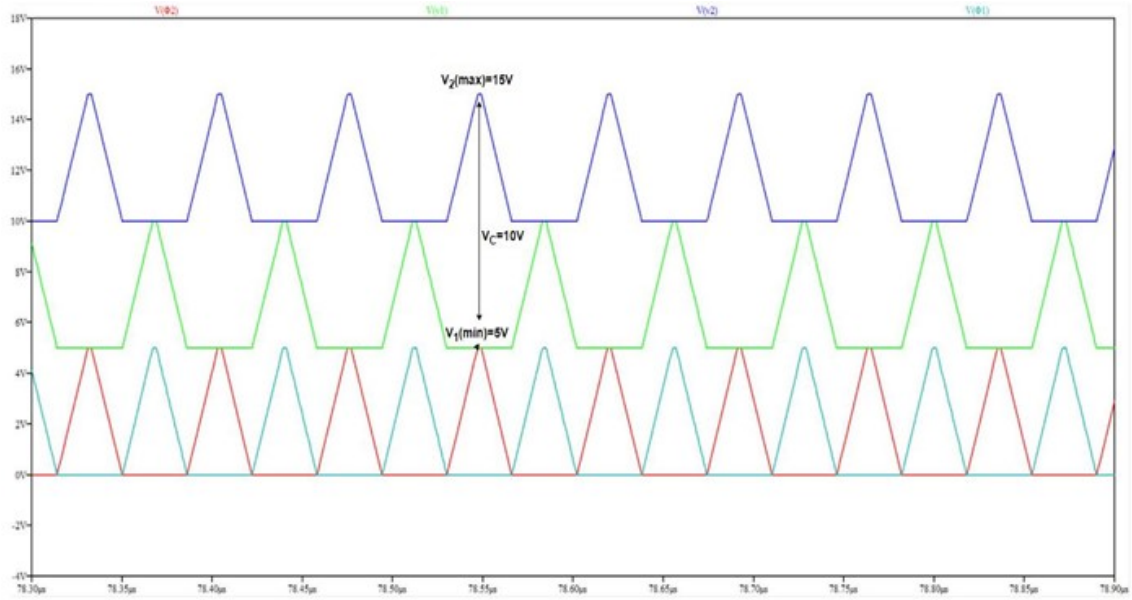

Figure 3.3: Circuit simulation results for 2-stage Dickson charge pump with ideal diodes

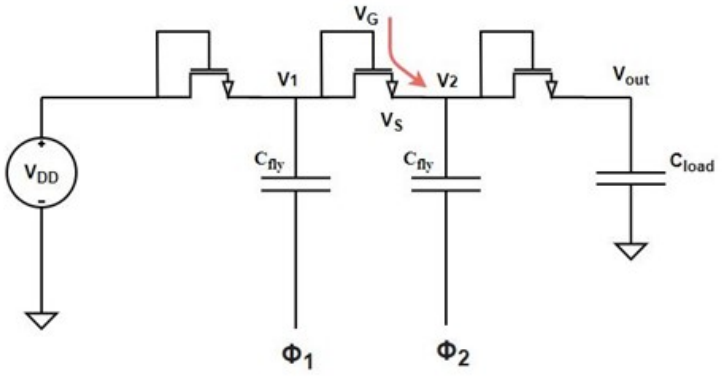

Figure 3.4: 2-stage Dickson charge pump with diode-connected MOSFETs

3.1.3. Load capacitor

The load capacitor will hold the charge for biasing the CMUT array. It needs to be large enough to avoid voltage drop when the CMUT is driven with a high-voltage pulse. The load capacitor C_{load} is chosen as 100nF, as explained in Sec1.3.

3.1.4. Non-overlapping clock generator

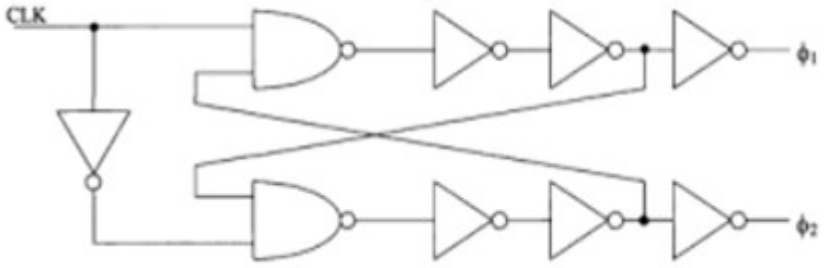

Figure 3.5: Non-overlapping clock generator circuit, reproduced from [3]

Two non-overlapping clock signals drive the bottom plate of the flying capacitors. The slew rate for the clock signals is designed in such a way that the peaking current I_{peak} while transferring the charge between the flying capacitors C_{fly} is given by

$$I_{peak} = C_{fly}\frac{\Delta V}{\Delta T} = C_{fly}\frac{5V}{T_r} \tag{3.1}$$

I_{peak} is small enough and should not exceed the Schottky diode's process limit, leading to a low slew rate for the clock signals. The non-overlapping clock signals with a low slew rate are shown in Fig.3.3. The non-overlapping clock generator is based on the NAND gate, as shown in Fig.3.5, which employs inverter chains to set the non-overlapping period [3]. Fig.3.6 shows the timing diagram of a clock signal. It consists of a rise time T_r, fall time T_f, on-time T_{on}, and period T_{period}.

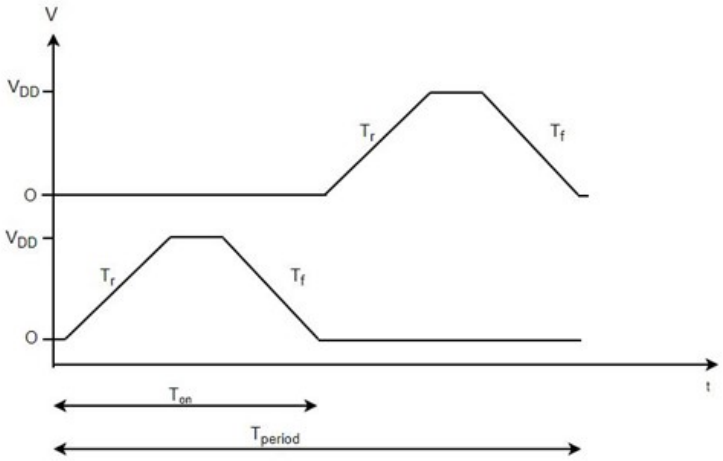

Figure 3.6: Timing diagram of a clock signal

3.2. Efficiency optimization

In this section, the dynamic efficiency for different charge pump capacitor C_{fly} is plotted based on the design choices made in Sec 3.1. From this plot, we can evaluate for which C_{fly} and N, the maximum efficiency $\eta_{dyn,peak}$ are obtained while achieving 63V at the output node.

The following conditions were made for this analysis

- All the capacitors used in the Dickson charge pump are empty initially.
- All the capacitors will be charged to 5V by the input source before the clock signals are applied.
- Non-overlapping clock signals are provided only after all the capacitors are pre-charged to 5V.

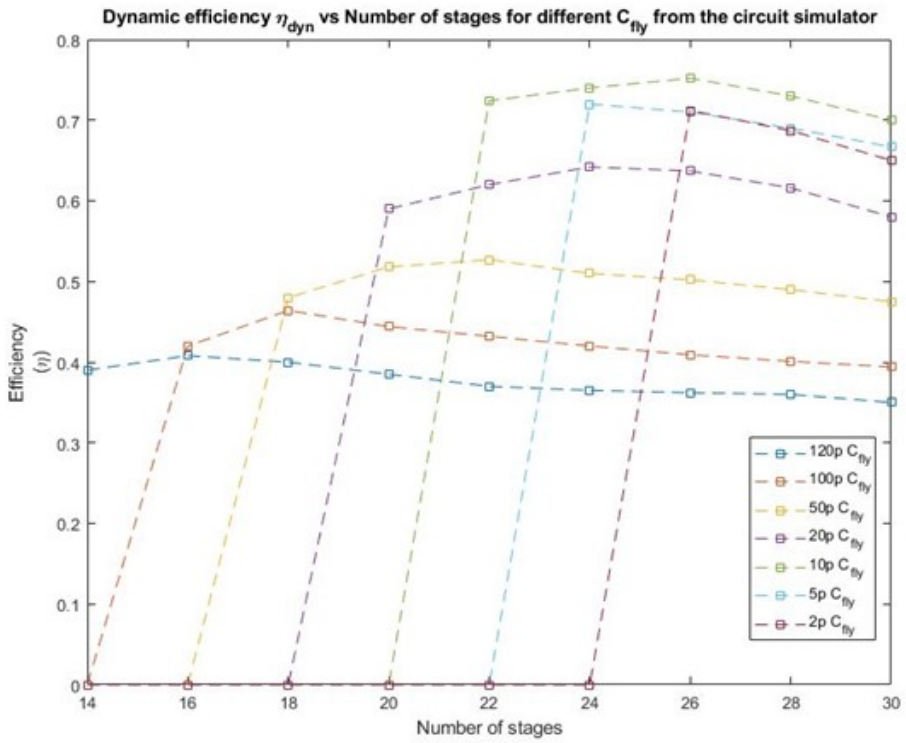

Figure 3.7: Dynamic efficiency vs. Number of stages for different C_{fly} from the circuit simulator

Fig.3.7 is obtained from the Dickson charge pump's circuit simulation results for a different number of stages and C_{fly}. In this plot, if the target voltage is not achieved for a certain C_{fly}, the efficiency is assumed to be 0. When the C_{fly} becomes smaller, the minimum number of stages required to achieve the target voltage also increases. As depicted in Figure 3.7, for C_{fly} equals 20pF, the minimum number of stages required to achieve the target voltage is 20. Likewise, for C_{fly} equals 10pF, the minimum number of stages required to achieve the target voltage is 22. From this plot, efficiency increases as the C_{fly} decreases, and after a certain C_{fly} (in this case, 10pF), the peak efficiency $n_{dyn,peak}$ will decrease since the parasitic losses start to dominate. We can also observe a local maximum in efficiency for a particular C_{fly} concerning the number of stages.

C_{fly}	Number of stages	Peak dynamic efficiency ($n_{dyn,peak}$)
120pF	16	0.408
100pF	18	0.464
50pF	22	0.527
20pF	24	0.642
10pF	26	0.752
5pF	24	0.72
2pF	26	0.712

Table 3.1: Peak dynamic efficiency vs. Number of stages for different C_{fly} from the circuit simulator

The peak efficiency values from this analysis are shown in Tab.3.1. The maximum peak efficiency is obtained for C_{fly} = 10pF and N= 26. Based on the design choices made in Sec.3.1, the circuit area for different charge pump capacitor C_{fly} where maximum efficiency is achieved, is plotted, as shown in Fig.3.8. The charge pump area is calculated from Layout XL software in cadence and is observed to be dominated by the flying capacitors.

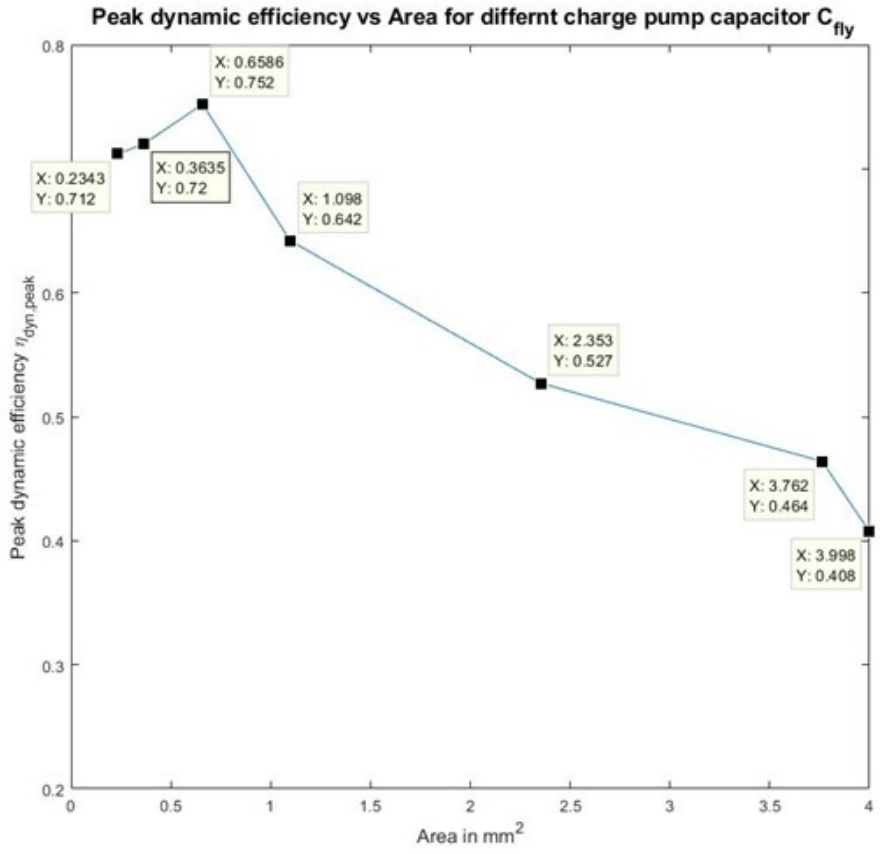

Figure 3.8: Peak dynamic efficiency vs. area for different charge pump capacitor C_{fly}

C_{fly}	Circuit Area in mm2	Peak dynamic efficiency ($n_{dyn,peak}$)
120pF	3.998	0.408
100pF	3.762	0.464
50pF	2.353	0.527
20pF	1.0980	0.642
10pF	0.6586	0.752
5pF	0.3635	0.72
2pF	0.2343	0.712

Table 3.2: Area vs. peak efficiency for different charge pump capacitor C_{fly}

Fig.3.8 shows the trend in the circuit area for different charge pump capacitor C_{fly} when peak dynamic efficiency is achieved, and these results are also tabulated, as shown in Tab.3.2. Our main goal is to obtain maximum efficiency without compromising the circuit area. Since this application's area budget is 1mm2, the last three values shown in Tab.3.2 are feasible. The Dickson charge pump with N=26 and C_{fly}=10pF is the best-case scenario, which leads to an efficiency of n_{dyn} = 0.752. However, a substantial area reduction can be obtained in a trade for a small reduction in efficiency if desired.

3.3. Simulation results

In Sec.3.2, the Dickson charge pump's best-case scenario for the given area budget was concluded. In this section, the circuit schematic and the simulation results for this Dickson charge pump scenario are presented.

Based on the design choices made in Sec.3.1 and the results obtained from Sec.3.2, the design of the Dickson charge pump is finalized for achieving a target voltage of 63V for biasing the CMUT in 180nm BCD technology. Fig.3.9, 3.10 and 3.11 are the simulation results for this schematic. In Fig.3.9, we observe the output voltage of the Dickson charge pump during the pre-charge phase. There are threshold voltage drops of the diode at each node in the Dickson charge pump, and if we wait for long enough with the diode still conducting in forward biased condition, we can reach the required 5V at each node of the Dickson charge pump. However, this is done to match the MATLAB model's initial conditions described in section 2.2 and does not affect the Dickson charge pump's design.

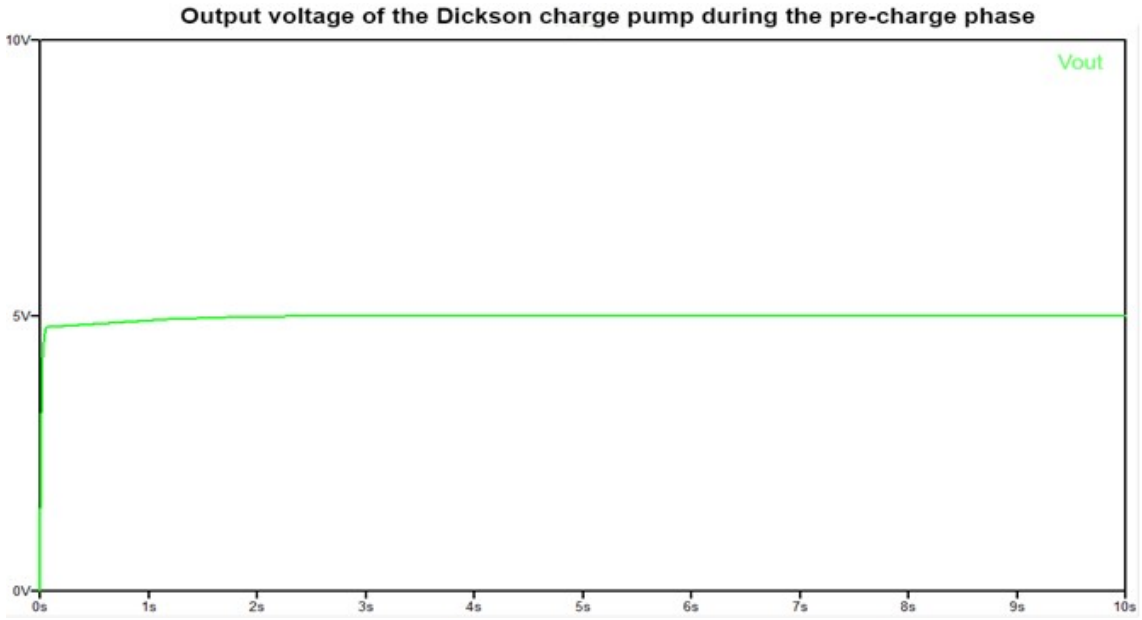

Figure 3.9: Output voltage of the Dickson charge pump design during the pre-charge phase

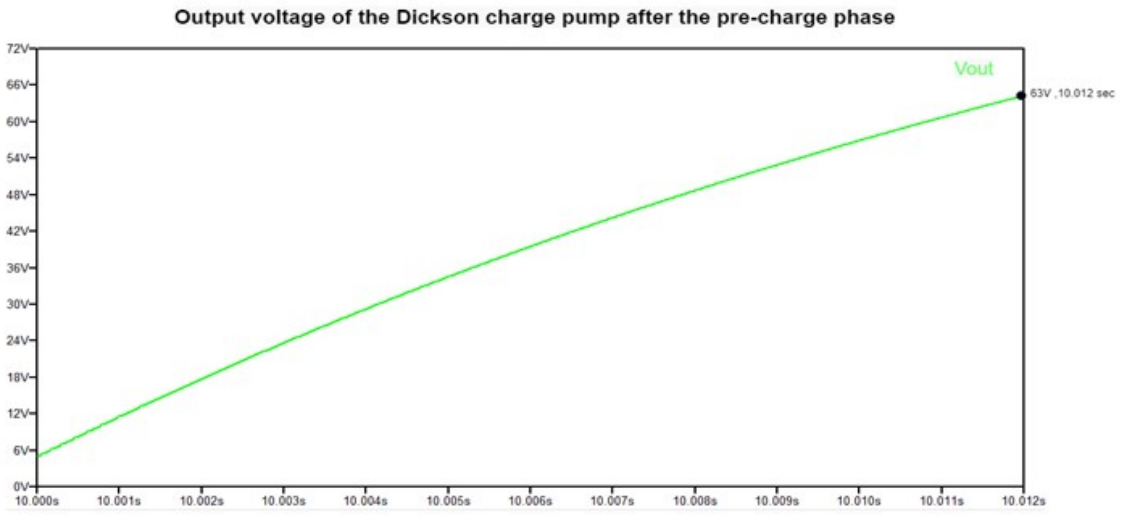

Figure 3.10: Output voltage of the Dickson charge pump design after the pre-charge phase

After the pre-charge phase, the non-overlapping clock signals are provided to the Dickson charge pump. During this phase, the voltage boosts up to the required target voltage of 63V at the output, as shown in Fig.3.10. The waveforms of the non-overlapping clock signals are shown in Fig.3.11, which is operated after a delay of 10 seconds (for the pre-charge phase). T_{on} = 36ns, T_{period} = 74ns, T_{rise} =17ns and T_{fall} = 17ns are the values of the clock signal parameters used for C_{fly} = 10pF based on the equation(3.1). Ideal non-overlapping clock sources are used in the simulation for this analysis. However, real non-overlapping clock sources can be developed, as shown in Fig.3.5

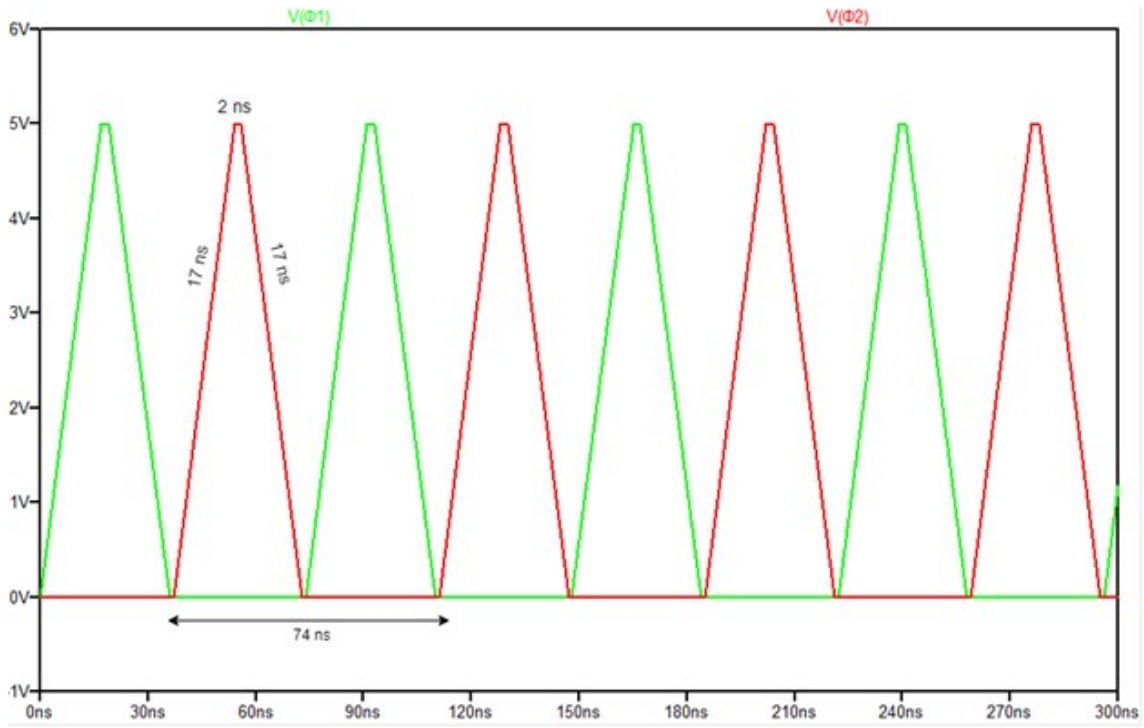

Figure 3.11: Output of the non-overlapping clock generator

We observe that it requires a rise time T_R of 12ms to achieve the target voltage of 63V, as shown in Fig3.10.The following are some design specifications achieved for this design.

Total rise time (T_R)	10.012 seconds
Number of clock cycles after the pre-charge phase	1.621 x 10^5
Clock frequency for $\phi 1$ and $\phi 2$	13.51 MHz
Total energy stored at the output	198.38 μJ
Total energy consumed by the input sources	263.81 μJ
Efficiency for the optimized Dickson charge pump (η_{dyn})	0.752
Circuit area	0.6586mm^2

Table 3.3: Design specifications obtained for the optimized Dickson charge pump

4

Hybrid Converter Topology

This chapter presents a design idea for biasing the CMUT at a higher voltage (120V) than supported by the 180nm BCD technology. First, the need for the concept is specified in Sec.4.1. Then, a hybrid idea for the charge pump circuit is presented in Sec4.2. Design considerations and the methods for designing the proposed concept are explained further in Sec.4.3 and Sec.4.4. The complete design of the hybrid converter and simulation results are discussed in Sec.4.5.

4.1. Need for a hybrid converter

Some CMUTs require a very high bias voltage [1], which can be beyond the process voltage limitations. To bias these types of CMUTs, an idea must be formulated that incorporates some off-chip components that can handle high voltages combined with an on-chip power converter that can generate up to the process voltage limitations. This combination of off-chip components and an on-chip power converter is discussed in detail in Sec. 4.2 .

4.2. Hybrid converter topology

In this section, an idea is proposed to bias a CMUT at 120V in a 180nm BCD technology that can handle 65V.

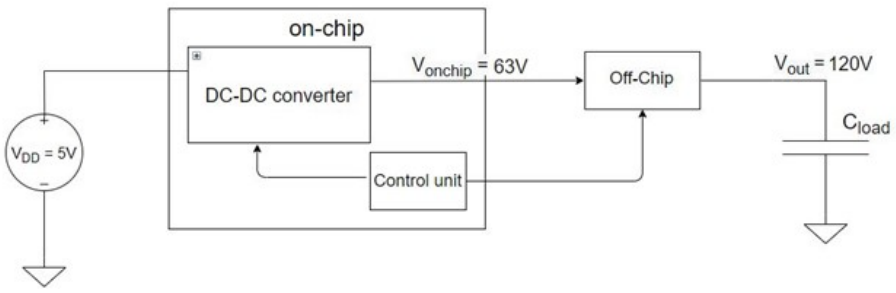

Figure 4.1: Block diagram of the hybrid converter

In Fig.4.1, the block diagram of the hybrid converter is presented. It combines 2 converters: the first converter is designed in a chip and boosts up to a maximum voltage that can be handled by the process technology used for fabricating the chip. The second converter incorporates some off-chip components to boost the voltage obtained from the first converter to the required target voltage. In our case, the first converter, namely the DC-DC converter shown in Fig.4.1, is designed in 180nm BCD technology and converts an input of 5V to 63V. The second converter, namely the off-chip unit, boosts this voltage to the target voltage of 120V to bias the CMUT. The charge-pump design presented in Sec.3.3 is considered for the on-chip DC-DC converter. This design was optimized for biasing a load capacitor of 100nF at 63V and will now be used to drive the off-chip unit. The charge pump's optimized design has fly capacitors C_{fly} = 10pF and consists of 26 stages

resulting in an efficiency of n_{dyn} = 0.752. The design of the off-chip unit and the control unit will be discussed in detail in Sec.4.3 and Sec.4.4, respectively.

4.3. Design of off-chip unit

In this section, the design of the Off-chip unit described in Sec.4.2 is examined. In Sec4.3.1, the constraints involved in designing the off-unit are explained, resulting in choosing the topology for the off-chip unit converter. In Sec4.3.2, an optimized design of the off-chip unit is presented

4.3.1. Off-chip converter topology

The off-chip unit is a voltage doubler which converts an input voltage of 63V to 120V at the output. The number of off-chip components involved should be minimized to optimize the overall size of the solution. These components should handle a high voltage of 120V, and the topology chosen for the off-chip unit should be compatible with the DC-DC converter presented in Sec.3.3. Similar to the on-chip converter, a Dickson charge pump topology is used for the off-chip unit. Only a single stage is used, so that only two high voltage diodes and one high voltage capacitor are required.

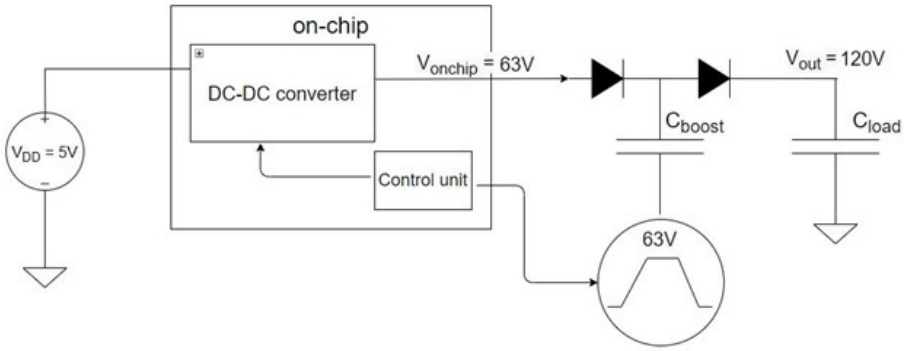

Figure 4.2: Block diagram of the hybrid converter with a Dickson charge pump as off-chip unit

Figure 4.2 depicts the resulting hybrid converter with a single-stage off-chip Dickson charge pump, where 'C_{boost}' is the flying capacitor for this converter. To drive the bottom plate of C_{boost}, a 63V pulse is required, which is also obtained from the on-chip unit's DC-DC converter with the help of the control unit.

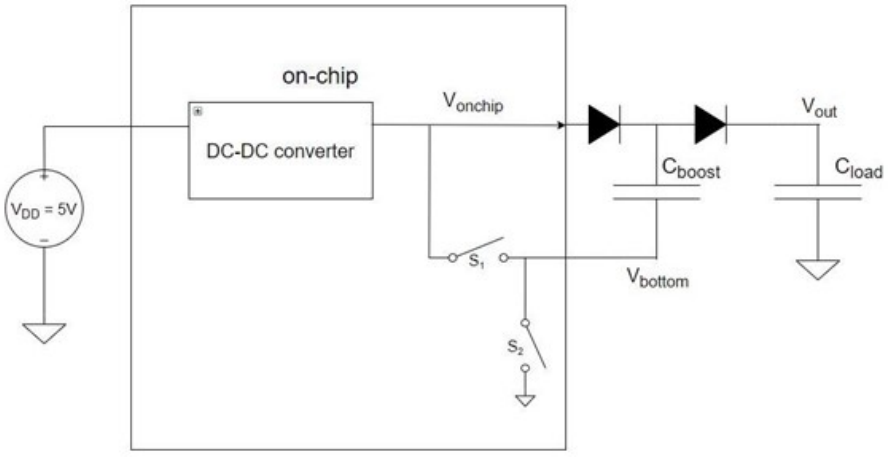

Figure 4.3: Hybrid converter with ideal switches as the control unit

A simple illustration to depict the concept of the control unit is shown in Fig.4.3. The control unit is replaced by ideal switches *S1* and *S2*. There are 3 phases: a pre-charge phase and two alternating phases: phase

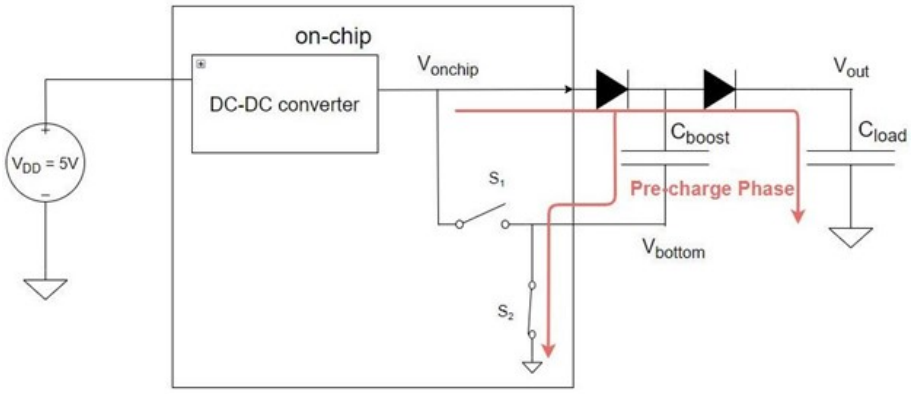

Figure 4.4: Hybrid converter with ideal switches as the control unit during the pre-charge phase

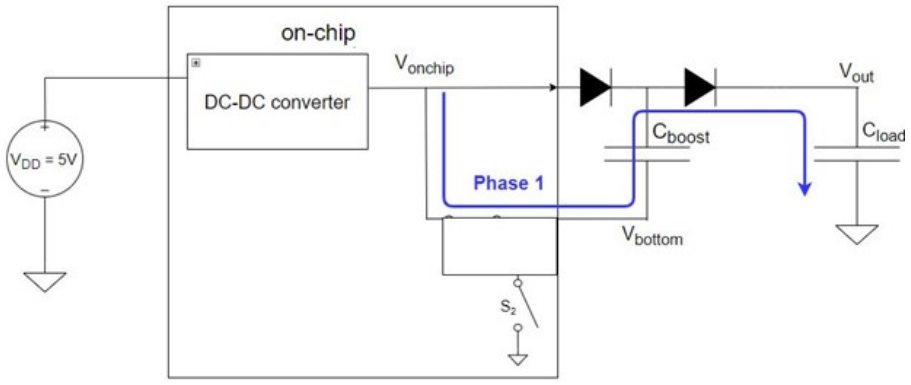

Figure 4.5: Hybrid converter with ideal switches as the control unit during phase 1

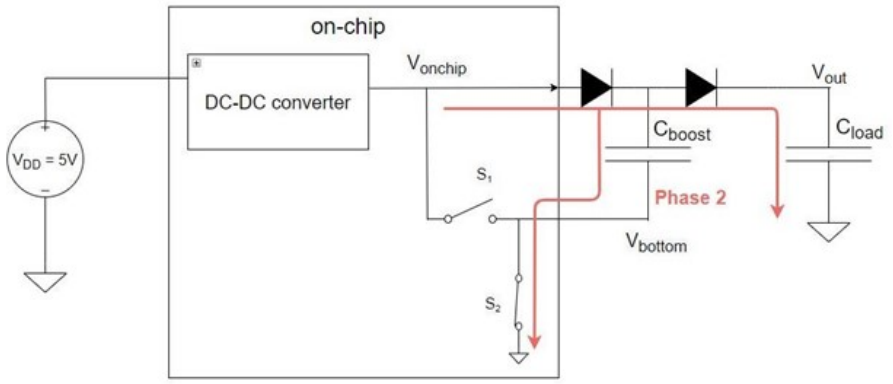

Figure 4.6: Hybrid converter with ideal switches as the control unit during phase 2

1 and phase 2 involved in the hybrid converter. In each phase, the load capacitor is different for the converter.

Switch *S1* is open, and switch *S2* is closed during the pre-charge phase, as shown in Fig. 4.4. In this phase, V_{out} and V_{onchip} are charged to 63V by the on-chip DC-DC converter. C_{boost} and C_{load} are connected in parallel, and thus the load capacitor C_L for this converter during this phase is:

$$C_L = C_{boost} + C_{load} \tag{4.1}$$

During phase 1, switch *S1* is closed, and switch *S2* is open, as shown in Fig.4.5. In this phase, V_{onchip} is connected directly to the bottom plate of the capacitor C_{boost}, and the connection exists until V_{onchip} and V_{bottom} are charged to 63V. C_{boost} and C_{load} are connected in series, as indicated by the arrow shown in Fig.4.5. Therefore the load capacitor C_L for this converter during this phase is:

$$C_L = \frac{C_{boost} * C_{load}}{C_{boost} + C_{load}} \tag{4.2}$$

During phase 2, switch *S1* is open, and switch *S2* is closed, as shown in Fig4.6. In this phase, the bottom plate of the capacitor C_{boost} is connected directly to the ground, and the load capacitor C_L is calculated using Eqn.4.1. Therefore, during phase 1, the bottom plate of the capacitor C_{boost} is driven by the on-chip DC-DC converter resulting in 63V. During phase 2, the bottom plate of the capacitor C_{boost} is grounded. Alternating between phases 1 and 2 results in pulses of 63V at the bottom plate of the capacitor C_{boost} and charge pumping from C_{boost} to C_{load}, eventually causing C_{load} to settle to approximately to $2 \times VC_{onchip}$. The design of the control unit using the real components will be explained in Sec.4.4.

4.3.2. Optimizing efficiency for different C_{boost}

The configuration with ideal switches for the control unit, as shown in Fig4.3, is simulated in a circuit simulator and analyzed for different C_{boost} values to observe which setting results in maximum efficiency. The load capacitor for this converter is chosen as 100nF in line with the AC coupling capacitor's value associated with the CMUT, as explained in Sec.1.3. The optimized design from Sec.3.3 is used as the on-chip DC-DC converter. Figure 4.7 depicts the resulting simulation setup for optimizing efficiency for different C_{boost}.

The on-chip DC-DC converter should reach 63V before driving the bottom plate of C_{boost} and acts as a pre-charge condition for this hybrid converter. During this pre-charge condition, switches *S1* is open, and *S2* is closed and resulting in V_{onchip} = V_{out} =63V. Since ideal diodes are used in the off-chip unit, no voltage drop is observed due to the diodes.

The value of C_{boost} determines the number of pulses that need to be applied to the bottom plate of C_{boost} to reach the target voltage on C_{load}. A larger C_{boost} requires a smaller number of pulses. The relationship between the C_{boost} and the number of pulses required to reach the target voltage can be found using the MATLAB model of the Dickson charge pump described in Sec.2.2.1. Based on the MATLAB model results, various simulations have been done for the hybrid converter in the circuit simulator, as shown in Fig.4.7, with values of C_{boost} ranging from 580nF to 2pF. In Sec.3.3, we observe that the non-overlapping clock signals are provided to the Dickson charge pump after a delay of 10s as an initial condition to maintain 5V at each Dickson charge pump node as shown in Fig. 3.9. However, this condition is ignored and does not affect the results obtained during this analysis.

Fig.4.8 depicts the simulated output waveforms of V_{out} and V_{bottom} for C_{boost} = 580nF. For C_{boost} = 580nF, it takes only one pulse at the bottom plate of C_{boost} to reach the target voltage of 120V. During the pre-charge phase, V_{bottom} is grounded, and V_{out} reaches 63V in 26ms for the load capacitance C_L = 680nF calculated using Eqn.4.1. During phase 1, V_{bottom} is charged to 63V. The duration of phase 1 is 13 ms calculated from the MATLAB model described in Sec.2.3.1 with a load capacitance value as C_L = 85.294nF calculated using Eqn.4.2. The overall efficiency of this converter is 0.289, calculated from the circuit simulator.

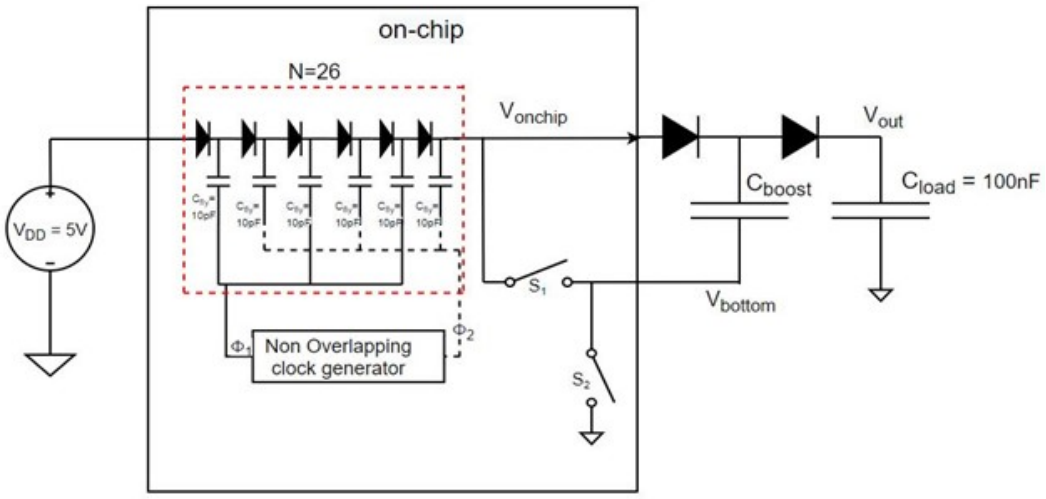

Figure 4.7: Hybrid converter with an optimized DC-DC converter and ideal switches as the control unit

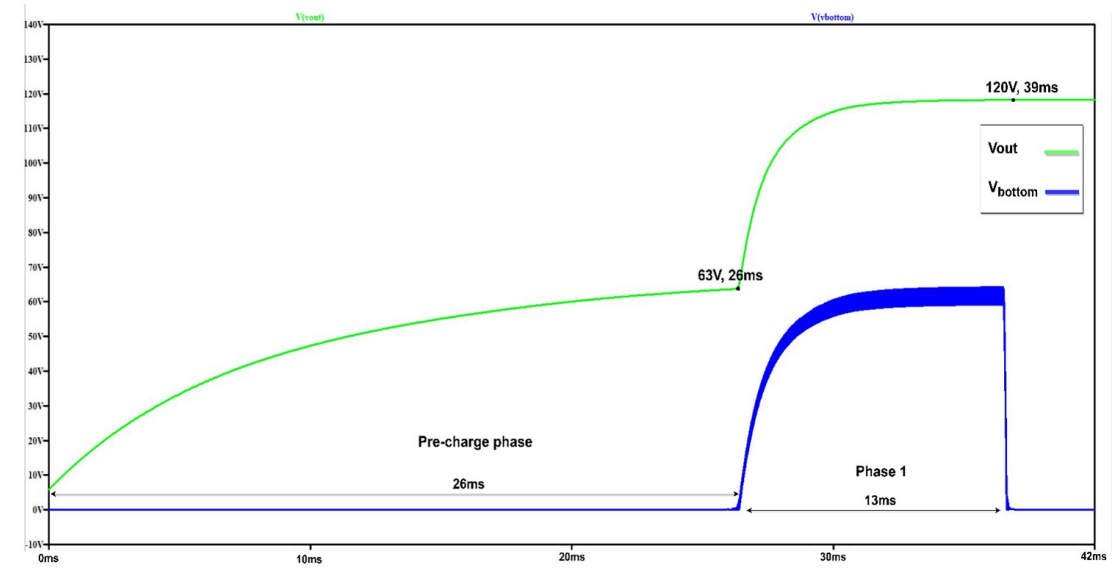

Figure 4.8: Simulated output waveforms for the hybrid converter of Fig.4.7 for C_{boost} = 580nF (1 pulse needed)

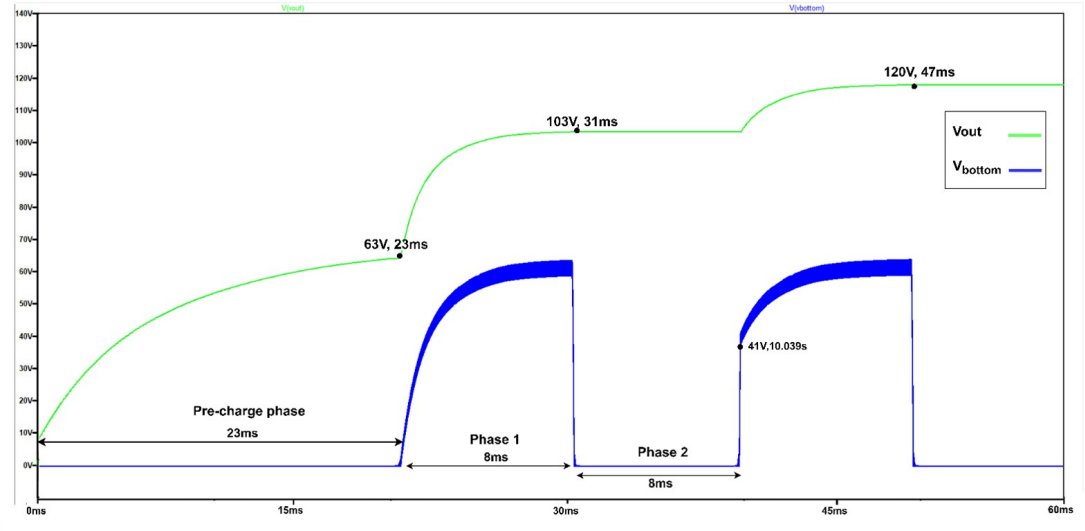

Figure 4.9: Simulated output waveforms for the hybrid converter of Fig.4.7 for C_{boost} = 160nF (2 pulses needed)

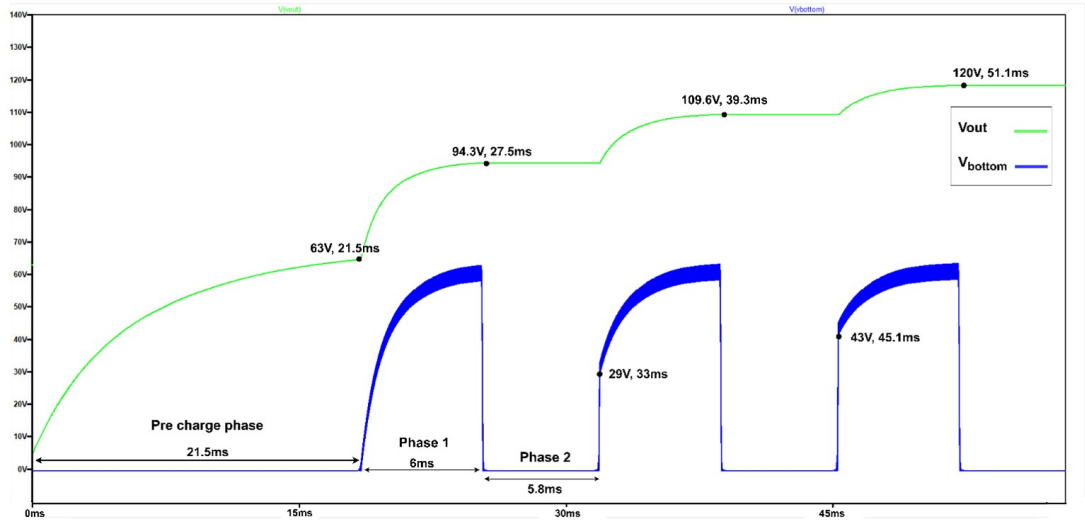

Figure 4.10: : Simulated output waveforms for the hybrid converter of Fig.4.7 for C_{boost} = 90nF (3 pulses needed)

Fig.4.9 and Fig.4.10 depict the waveforms of V_{out} and V_{bottom} for C_{boost} equal to 160nF and 90nF, respectively. For C_{boost} =160nF, it takes two clock cycles (i.e., two pulses at the bottom plate of C_{boost}), and for C_{boost} = 90nF, it takes three clock cycles (i.e., three pulses) to reach the target voltage 120V. During the pre-charge phase, V_{bottom} is grounded. V_{out} reaches 63V in 23ms and 21ms for the load capacitances C_L equals 260nF and 190nF calculated using the Eqn.4.1 for C_{boost} equals to 160nF and 90nF, respectively.

During phase 1, V_{bottom} is charged to 63V. As before, the duration of this phase is calculated as 8ms and 6ms from the MATLAB model described in Sec.2.3.1 with load capacitance values equal to 61.538nF and 47.368nF, calculated using equation 4.2 for C_{boost} equals to 160nF and 90nF respectively.

During phase 2, V_{bottom} is grounded, and the load capacitors for the converter equal 260nF and 190nF, calculated using equation 4.1 for C_{boost} equals to 160nF and 90nF, respectively. In the previous phase, V_{onchip} and V_{bottom} were connected. However, during this phase V_{onchip} is now connected to a different load capacitor with different charges stored in them compared to phase 1. As a result, the value of V_{onchip} is now different, and this effect propagates at each intermediate node of the on-chip Dickson charge pump, resulting in different voltage levels at each intermediate node. These values can be calculated using the MATLAB model

Efficiency η_{dyn}	**C**$_{boost}$	**No. of clock cycles**	**Rise time** T_R
0.289	580 nF	1	39 ms
0.302	160 nF	2	47 ms
0.316	90 nF	3	51.1 ms
0.339	60 nF	4	63 ms
0.375	10 nF	20	79 ms
0.418	1 nF	238	61 ms
0.532	100 pF	2346	62.4 ms
0.581	50 pF	4718	59 ms
0.609	10 pF	1.1 x 104	67 ms
0.594	5 pF	5.409 x 104	72 ms
0.512	2 pF	1.356 x 105	81ms

Table 4.1: Simulation results for the hybrid converter with an optimized DC-DC converter and ideal switches as the control unit for C$_{boost}$ ranging from 580nF to 2pF

described in section 2.2.1. The required duration of this phase is defined as the time taken by the converter to bring back these voltage levels to their steady-state values, where V$_{onchip}$ returns to 63V. Using the MATLAB model, this is estimated as 8ms, and 5.8ms for C$_{boost}$ equals 160nF and 90nF.

It is also noted that during the second clock cycle, V$_{bottom}$ starts at a different voltage level i.e., 41V and 29V for C$_{boost}$ equals to 160nF and 90nF, respectively, when compared to the previous clock cycle. In the previous clock cycle, V$_{bottom}$ was grounded, and in the second clock cycle, some charge is already stored in C$_{boost}$. As a result of charge redistribution, at this moment, V$_{bottom}$ is at a different voltage level. The total rise time and overall efficiency is 47ms and 0.302, respectively, for the hybrid converter with C$_{boost}$ equals 160nF to achieve the target voltage 120V. Likewise, the total rise times and overall efficiency is 51.1ms and 0.316, respectively, for the hybrid converter with C$_{boost}$ equal to 90nF to achieve the target voltage of 120V.

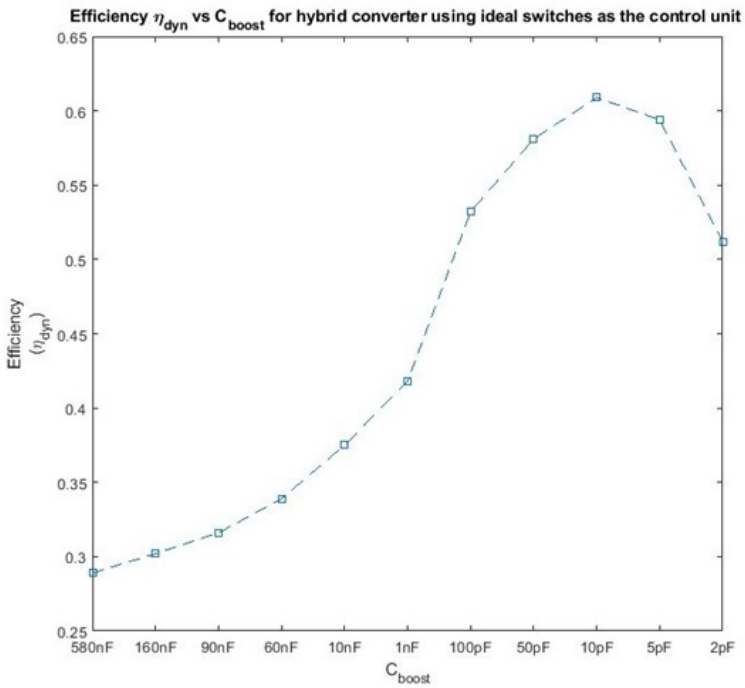

Figure 4.11: Efficiency vs C$_{boost}$ for hybrid converter using ideal switches as the control unit

Table 4.1 summarizes the simulation results obtained for the hybrid converter with C$_{boost}$ ranging from

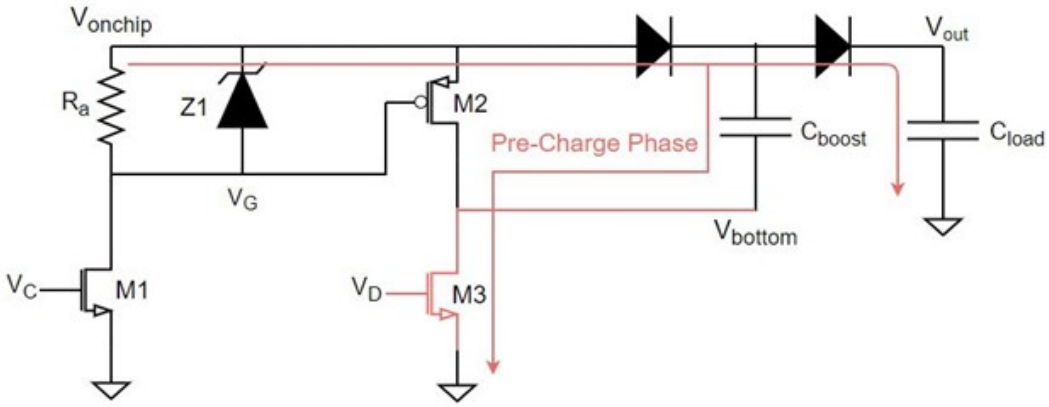

Figure 4.12: Control unit circuit during the pre-charge phase

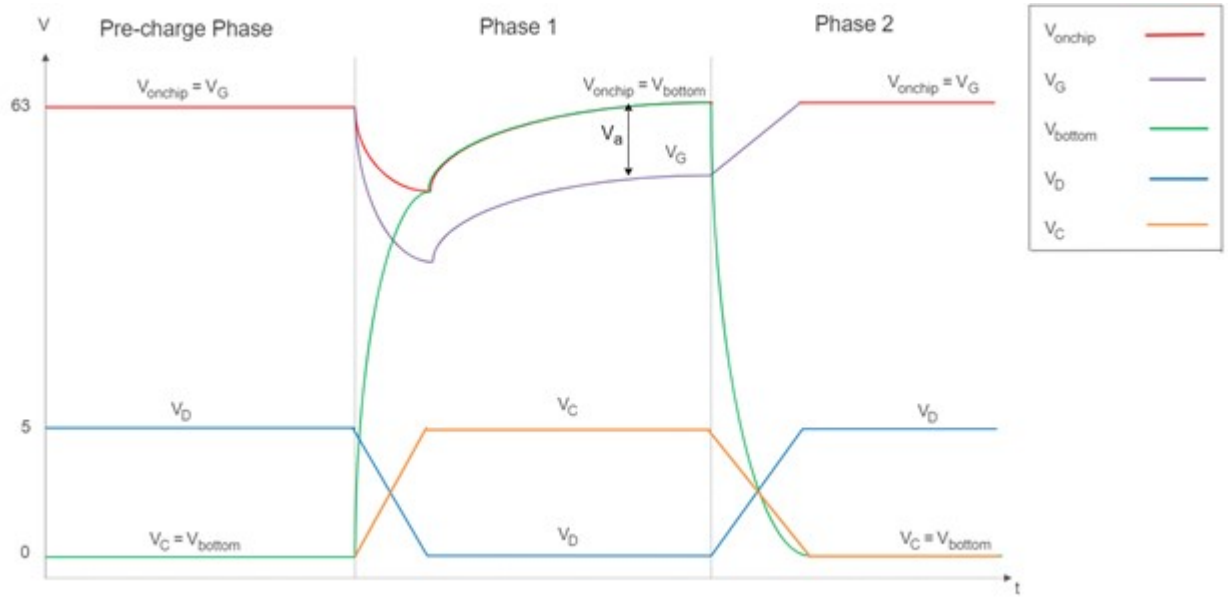

Figure 4.13: Timing diagram for the control unit circuit

580nF to 2pF. Fig.4.11 depicts the trend in efficiency as a function of C_{boost}. We observe that when C_{boost} becomes smaller, efficiency increases; however, the number of clock cycles needed to drive C_{boost} increases. The maximum efficiency of 0.609 is obtained to achieve the target voltage 120V at the output to bias the CMUT, for C_{boost} = 10pF with total rise time, T_R of 60ms. However, $1.1x10^4$ clock cycles are needed to drive the C_{boost} to achieve the target voltage.

4.4. Design of control unit

In Sec.4.3.1, the working of the control unit with ideal switches has been explained. In this section, the design idea and working of the control unit circuit is presented.

Fig.4.12 depicts the control unit circuit for the hybrid converter. This circuit consists of PMOS M2, NMOS M1, and M3, Zener diode Z1 and two control signals, namely V_C and V_D for transistors M1, M2, and M3, respectively.

During the pre-charge phase:

- V_D is set high (5V), and V_C is set low (0V).
- Transistor M3 is turned on, and as a result, there is a path between V_{bottom} and ground. The bottom

plate of the capacitor C_{boost} is grounded.

- Transistor M1, M2 is turned off. V_{onchip}, V_G, and V_{out} equal 63V, obtained from the DC-DC converter in the on-chip unit.

- The nodal voltages in this phase are shown in Fig.4.13 under pre-charge phase

During phase 1:

- V_C is high (5V), and as a result, transistor M1 is turned on.

- Current I_a flows through the transistor M1. R_a is biased so that the voltage drop V_a across the resistor R_a is more than the threshold voltage drop of the transistor M2, and as a result, transistor M2 is also turned on.

- There is a path formed between V_{onchip} and V_{bottom} during this phase, as shown in Fig. 4.14. The V_{onchip} obtained from the DC-DC converter, as shown in Fig.4.7, now drives the bottom plate of the capacitor C_{boost}.

- Zener diode Z1 is used to protect the transistor M1 from exceeding the maximum gate-source voltage limit of 5.5V in 180nm BCD technology.

- V_D is low (0V), and as a result, transistor M3 is turned off.

- The nodal voltages during this phase are shown in Fig.4.13 under phase 1.

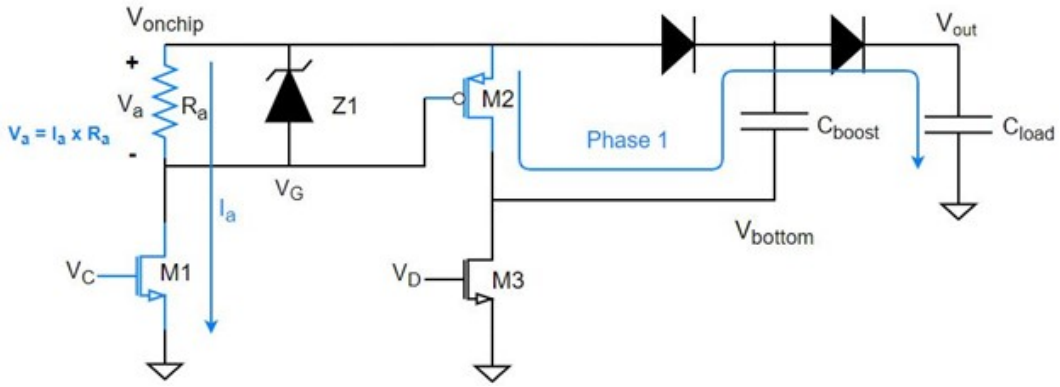

Figure 4.14: Control unit circuit during phase 1

During phase 2:

- V_D is high (5V), and as a result, transistor M3 is turned on.

- There is a path formed between the ground and V_{bottom} during this phase, as shown in Fig.4.15. The bottom plate of the capacitor C_{boost} is grounded during this phase.

- V_C is low (0V), and as a result, transistors M1 and M2 are turned off.

- The nodal voltages during this phase are shown in Fig. 4.13 under phase 2.

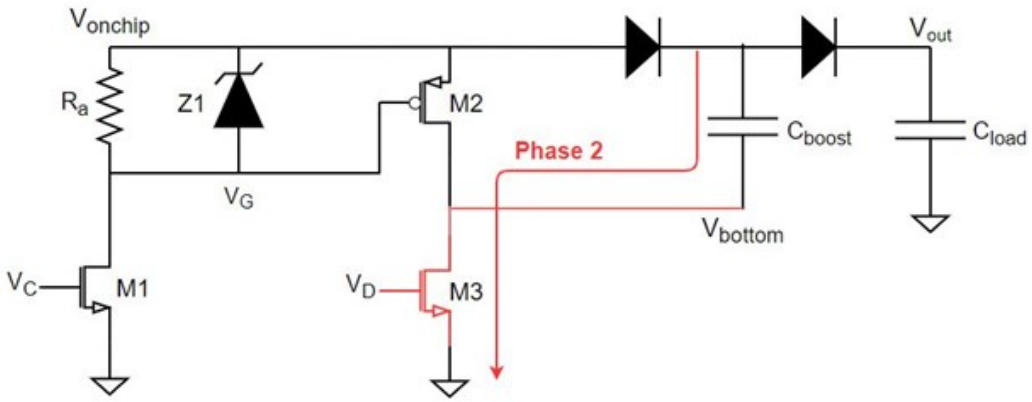

Figure 4.15: Control unit circuit during phase 2

From Fig. 4.13, we observe that V_{bottom} is at the ground during the pre-charge phase, and during phase 1, V_{bottom} raises to V_{onchip}. During phase 2, V_{bottom} reaches back to the ground resulting in a pulsated waveform of V_{bottom} with frequency same as the clock signals provided for V_C and V_D. This control unit circuit will be implemented with the optimized hybrid converter discussed in Sec.4.3.2, and the results will be discussed in the next section.

4.5. Circuit Schematic and simulation results

In this section, the circuit schematic and the simulation results for the complete hybrid converter are presented.

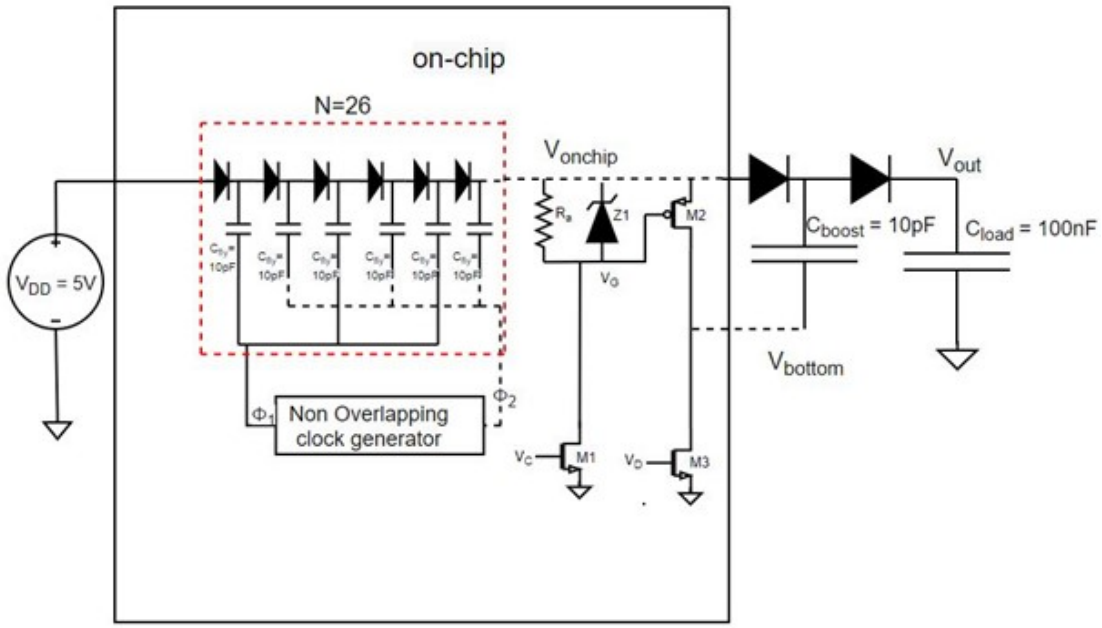

Figure 4.16: Circuit schematic of the optimized hybrid converter

Based on the design choices made in Sec. 4.3 and the results obtained from Sec. 4.4, the design of the hybrid converter is finalized for achieving a target voltage of 120V for biasing the CMUT in 180nm BCD technology. Fig. 4.16 shows the circuit schematic of the finalized version of the hybrid converter design, which contains an optimized on-chip Dickson charge pump with 26 stages, C_{fly} = 10pF based on the results from Sec. 3.3. Ideal clock signals are used for $\phi 1$, $\phi 2$, V_C, and V_D in this circuit simulation. Fig. 4.17, Fig. 4.18 and Fig. 4.19 are the simulation results obtained for this schematic.

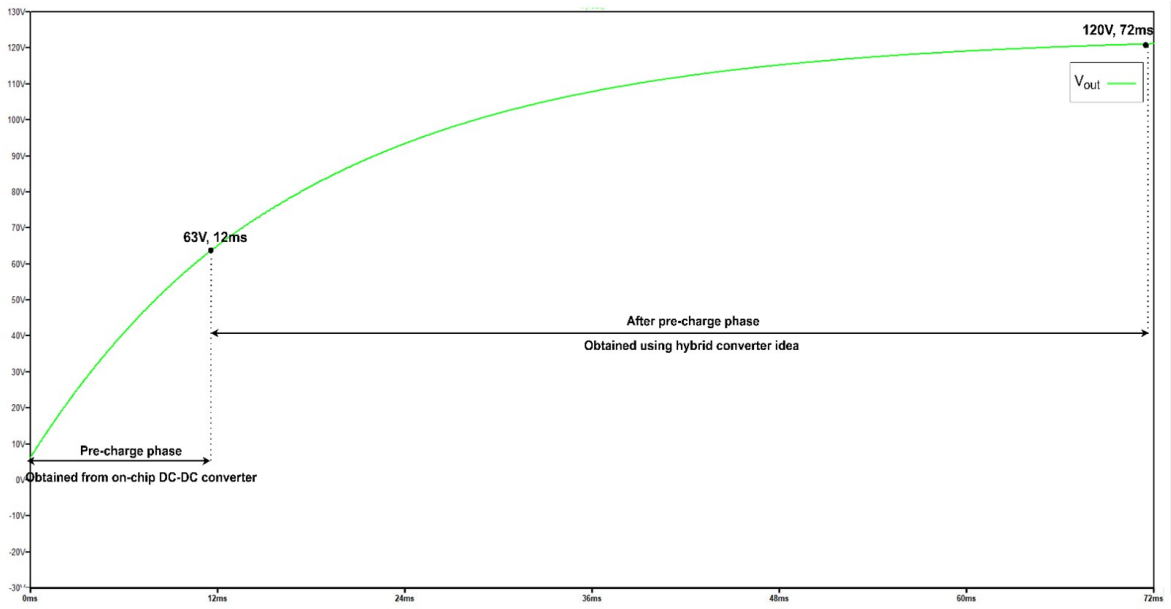

Figure 4.17: Output voltage of the hybrid converter design

In Fig. 4.17, we observe the output voltage of the hybrid converter. During the pre-charge phase, V_{out} reaches 63V in 12ms, obtained from the optimized on-chip Dickson charge pump design, and V_{boost} is grounded during this phase. After the pre-charge phase, the bottom plate of C_{boost} is driven by pulses of 63V, as shown in Figure 4.18. However, $1.1x10^4$ clock cycles are needed to drive C_{boost} to achieve the target voltage as explained in Sec. 4.3.2. Fig. 4.19 shows the control unit's timing diagram described in Sec. 4.4 for the hybrid converter during the three phases. The non-overlapping clock signals used for the Dickson charge pump are operated at 13.51 MHz with T_{period} = 74 ns, same as used in Sec. 3.3. The clock signals V_C and V_D used for the control unit are operated at 142.86 kHz with T_{period} = 7 µs. Table 4.2 summarizes the hybrid converter design's specifications to bias the CMUT at target voltage 120V. We also observe that the efficiency η_{dyn} for the hybrid converter is 0.577, which is lower than the values obtained in Sec. 4.3.2, which is 0.609. The drop in the efficiency is because real circuit components are used in this analysis and there is a continuous current flowing through the resistor R_a during phase 1 of the control unit. The hybrid converter's circuit area is calculated from Layout XL software in cadence and is observed to be dominated by the Dickson charge pump's flying capacitors.

Total rise time T_R	72 ms
Number of clock cycles for ϕ1 and ϕ2 during the pre-charge phase	1.621×10^5
Clock frequency for ϕ1 and ϕ2	13.51 MHz
Number of clock cycles for V_C and V_D after the pre-charge phase	1.5×10^4
Clock frequency for V_C and V_D	142.86 kHz
Total energy stored at the output	719.52 μJ
Total energy consumed by the input sources	1245.49 μJ
Efficiency for the hybrid converter design	0.577
On-chip circuit area	0.842mm2
Number of off-chip components	3

Table 4.2: Design specifications obtained for the hybrid converter with control unit circuit

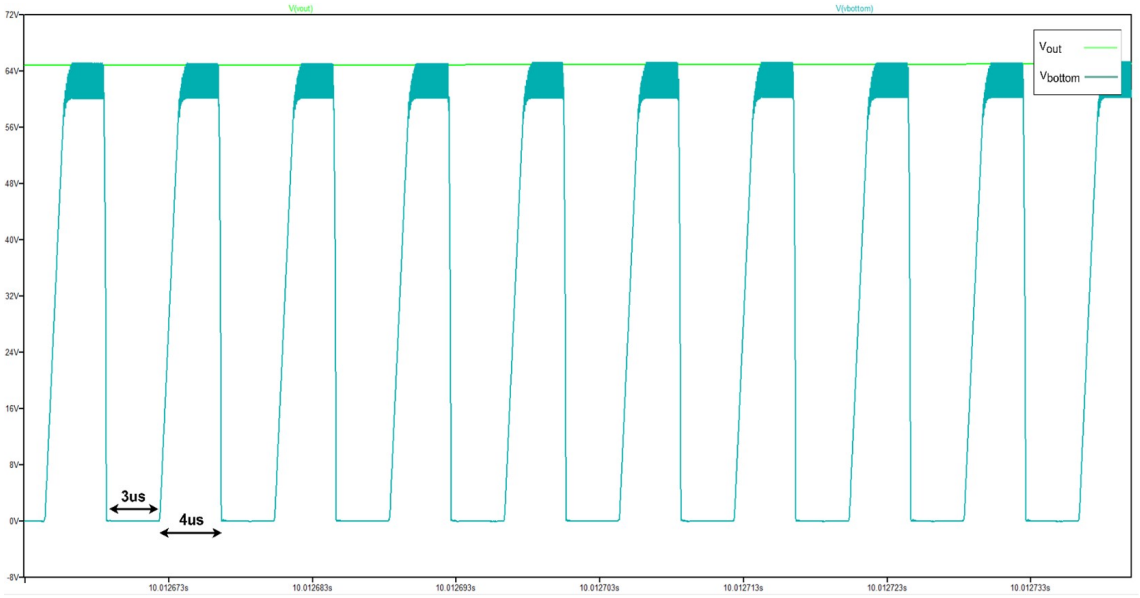

Figure 4.18: Voltage waveform of V_{bottom} in the hybrid converter design

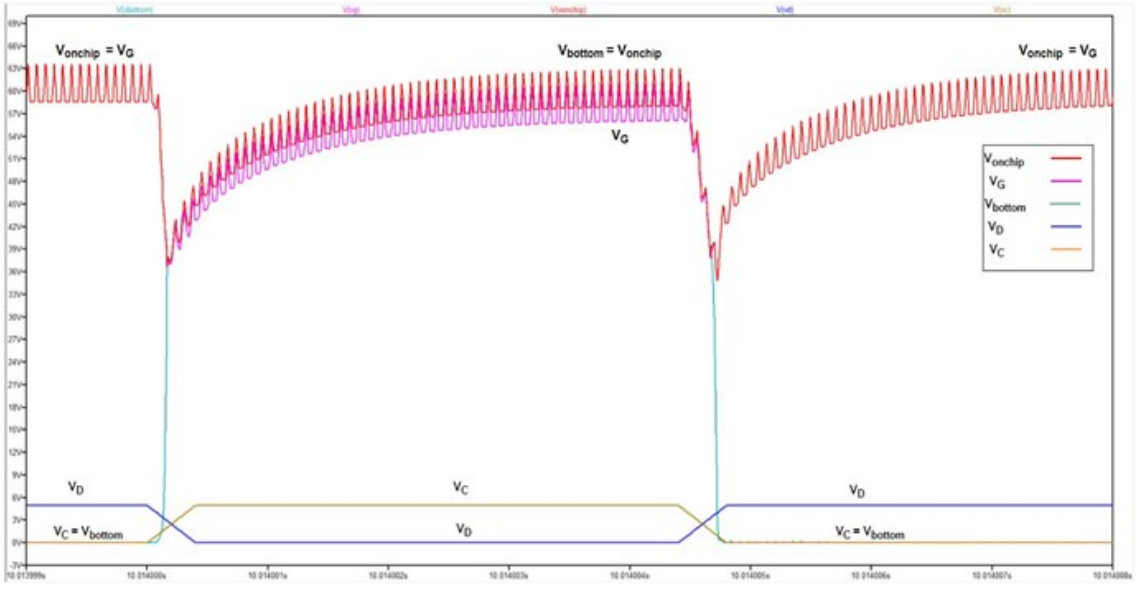

Figure 4.19: Timing diagram of the control unit circuit used in the hybrid converter

5

Conclusions

This thesis has shown the design of a DC-DC converter to bias a CMUT transducer. Two different cases have been investigated: biasing at 63V from an input of 5 V using a fully-integrated converter realized in a 180nm BCD technology that can handle up to 65V; and biasing at 120V by employing minimal off-chip components. In this chapter, we will discuss the conclusions and future work for this project.

5.1. General conclusions

Prior research work on the efficiency of Dickson charge pumps during the transient period is limited. The dynamic efficiency η_{dyn} described in equations 2.9 and 2.10 does not match with the circuit simulation results for the Dickson charge pump and seems to depend on the charge-pump capacitor C_{fly}.

A MATLAB model for the Dickson charge pump has been developed to support this observation. Based on the results obtained from this model, we observe that the dynamic efficiency increases as the charge pump capacitor C_{fly} becomes smaller. We also observe that the dynamic efficiency decreases with an increase in the number of stages N for the same charge pump capacitor C_{fly} and load capacitor C_{load}. As depicted in Fig. 2.16 and 2.19, these results provide an added advantage in minimizing the circuit area.

With the help of the results obtained using the MATLAB model, a DC-DC converter has been designed for biasing the CMUT at 63V in 180nm BCD technology with a simulated efficiency η_{dyn} of 0.752 and an estimated circuit area of 0.6587 mm^2.

A hybrid converter design idea to bias the CMUT beyond the process voltage limitations has also been discussed in this thesis. A DC-DC converter has been designed for biasing the CMUT at 120V in 180nm BCD technology with a simulated efficiency η_{dyn} of 0.577 and an estimated circuit area of 0.842 mm^2, using two high-voltage diodes and one high-voltage capacitor externally. This unique hybrid converter idea requires much fewer components than a conventional DC-DC converter and substantially minimizes the circuit area.

This research also suggests that the biasing circuit's energy consumption could be substantially larger than the total energy consumed by the transceiver components if the transducer is only pulsed a small number of times, given that the AC coupling capacitor that needs to be charged to the biasing voltage is much larger than the CMUT capacitance, and the AC biasing voltage is typically larger than the pulse voltage. Therefore, for battery-powered ultrasound imaging systems, it could be better to opt for PMUTs, if available, which do not require high voltage DC bias compared to CMUT.

5.2. Future work

The MATLAB model should also be developed for a generic switched-capacitor converter to investigate the relationship between the charge pump capacitor C_{fly} and the dynamic efficiency η_{dyn}. The Dickson charge pump should be replaced with a switched capacitor converter with a better conversion ratio resulting in fewer

components and a smaller circuit area.

The hybrid converter idea can be used in the on-chip DC-DC converter to reduce the number of components. A better control unit circuit that does not consume continuous current during phase 1, as explained in section 4.4, while driving the bottom plate of the off-chip capacitor C_{boost} should be developed for the hybrid converter.

We can now develop multiple converters on-chip and use the hybrid converter idea to integrate them into the final target voltage leading to a multilevel on-chip DC-DC converter to tune the center frequency of the CMUT by adjusting the bias voltage. We should further investigate a method to re-use the energy stored on the AC coupling capacitor of the CMUT swiftly by transferring the energy stored back to the battery or using that energy for other applications. Inductive DC-DC converters could help re-use the energy stored on the AC coupling capacitor of the CMUT.

Bibliography

[1] H. Wang, Y. Ma, H. P. Yang, H. Jiang, Y. Ding, and H. Xie, "MEMS Ultrasound Transducers for Endoscopic Photoacoustic Imaging Applications," *Micromachines*, vol. 11, pp. 928–969, Oct. 2020.

[2] K. Chen, H.-S. Lee, A. P. Chandrakasan, and C. G. Sodini, "Ultrasonic Imaging Transceiver Design for CMUT: A Three-Level 30-Vpp Pulse-Shaping Pulser With Improved Efficiency and a Noise-Optimized Receiver," *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 2734–2745, Nov. 2013.

[3] B. Nowacki, N. Paulino, and J. Goes, "A simple 1 GHz non-overlapping two-phase clock generators for SC circuits," in *Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2013*, pp. 174–178, 2013.

[4] P. Behnamfar and S. Mirabbasi, "A CMUT read-out circuit with improved receive sensitivity using an adaptive biasing technique," in *2011 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pp. 397–400, 2011.

[5] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, vol. 11, pp. 374–378, June 1976.

[6] T. Tanzawa and T. Tanaka, "A dynamic analysis of the dickson charge pump circuit," *IEEE Journal of Solid-state Circuits*, vol. 32, pp. 1231–1240, 1997.

[7] T. Tanzawa, "Dickson charge pump circuit design with parasitic resistance in power lines," in *2009 IEEE International Symposium on Circuits and Systems*, pp. 1763–1766, 2009.

[8] T. Tanzawa, "Design of DC-DC Dickson Charge Pump," in *On-chip High-Voltage Generator Design: Design Methodology for Charge Pumps* , pp. 67–122, Springer International Publishing , 2016.

[9] F. Farah, M. E. Alaoui, K. El Khadiri, and H. Qjidaa, "New analog li-ion battery charger using pulsed charging method," in *2018 6th International Conference on Multimedia Computing and Systems (ICMCS)*, pp. 1–4, 2018.