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A Novel Printed-Lookup-Table-Based Programmable Printed Digital Circuit

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***Abstract*— Advances in printed electronics (PE) enables new applications, particularly in ultra-low-cost domains. However, achieving high-throughput printing processes and manufacturing yield is one of the major challenges in the large-scale integration of PE technology. In this article, we present a programmable printed circuit based on an efficient printed lookup table (pLUT) to address these challenges by combining the advantages of the high-throughput advanced printing and maskless point-of-use final configuration printing. We propose a novel pLUT design which is more efficient in PE realization compared to existing LUT designs. The proposed pLUT design is simulated, fabricated, and programmed as different logic functions with inkjet printed conductive ink to prove that it can realize digital circuit functionality with the use of programmability features. The measurements show that the fabricated LUT design is operable at 1 V.**

***Index Terms*— Electrolyte-gated transistor (EGT), emerging technologies, Internet of Things (IoT), lookup table (LUT), low power, printed electronics (PE), security, yield.**

I. Introduction

PRINTED electronics (PE), as a complementary solution to the existing silicon-based technologies, has demonstrated tremendous potential in novel applications such as wearables, smart tags, and smart sensors requiring ultra-low-cost, on-demand fabrication, and mechanical flexibility [1]–[5]. Several PE transistor technologies have been proposed to implement functional circuits for PE applications [6], [7], [10]. However, high-volume fabrication of PE circuits suffers from several challenges.

Several printing techniques are used to fabricate PE circuits. Some of the printing techniques such as inkjet printing are low cost which enables users for low-volume point-of-use fabrication. However, these techniques have low resolution, high variation, and low yield, making them inefficient for mass production. On the other hand, expensive advanced printing fabrication techniques such as roll-to-roll processes with imprint lithography [20] can achieve down to nanometer resolution, low variation and high yield, resulting in high-performance printed circuits [18]. However, since these techniques use expensive tools and high-resolution masks for each design, they do not provide low-cost and on-demand fabrication. Therefore, one or multiple printing processes can be used depending on the target application.

The low resolution, low throughput, and high variation of low-cost fabrication printing processes, material-related limitations, and full-custom design methodology result in low-performance and low-yield PE circuits. Furthermore, low-cost but low-throughput fabrication printing processes such as inkjet printing that enables personalized fabrication are inconvenient for high-volume fabrication since it is incomparably slower than advanced fabrication processes for the mass production of printed circuits [18]. On the other hand, the advanced fabrication processes provide higher resolution and lower variation compared to low-cost fabrication processes resulting in better performance and higher yield in the exchange of expensive tools while restraining the on-demand and personalized fabrication.

The work in [19] presents a transistor level method utilizing functional transistors in a sea of transistors to improve the yield of printed circuits, but it requires a large amount of error-prone inkjet printing and transistor characterization effort to provide large-scale integration.

In this article, we propose the first one-time programmable printed lookup table (pLUT) design to implement virtually any printed digital circuits while addressing the aforementioned challenges. The pLUT can be fabricated using high-throughput advanced techniques in a production center to mitigate low performance and low yield, and to lower cost per printed circuit. Then, the pLUT can be programmed using printing conductive inks to corresponding connections based on user requirements using an inkjet printer so that users can realize any on-demand printed circuits with minimum effort.

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In addition, the programmability feature of this approach can also be used to mitigate failures by bypassing defective components through rerouting. The suitability of the existing and the proposed LUT implementations to the proposed split manufacturing scheme is reviewed and compared in terms of area usage, worst case delay, and power consumption. The proposed pLUT implementation is simulated and fabricated using inorganic electrolyte-gated printed transistors, and programmed with inkjet printed conductive ink as XNOR, XOR, and AND gate to prove the programmability of the proposed design. The characterization results show that the fabricated pLUT operates at 1 V. Furthermore, the usage cases of the proposed pLUT for several purposes are discussed.

The summary of the contributions of the work is as follows.

1) We propose the first one-time programmable pLUT design and compare it with existing LUTs in terms of area usage, worst case delay, and power consumption.
2) We present the efficient scaling of pLUT and chip architecture for complex circuit implementations.
3) We synthesize several benchmark circuits with pLUT cells and standard cells and present a comparison in terms of maximum frequency, area usage, and power consumption.
4) We provide fabrication and characterization results of 2-input pLUT (pLUT2), configured as AND, XOR, and XNOR gates.
5) We discuss the usage cases of the proposed design for yield improvement, performance improvement, and security solutions in PE.

The rest of this article is organized as follows. Section II introduces PE and technologies, while the proposed pLUT is presented in Section III. In Section IV, simulation and fabrication results are presented and discussed. Section V discusses the applications of proposed pLUT, and Section VI concludes this article.

II. Background on PE

PE is a complement to the existing technologies with its niche features of ultra-low-cost, disposability, mechanical flexibility, lightweight, large area, and on-demand/point-of-use fabrication enabling novel applications such as dynamic newspapers, smart labels, smart cards, health care diagnosis devices, energy harvesters, and smart clothing [28].

Various additive printing processes are used to manufacture PE circuits instead of photolithography-based subtractive processes that are complex, expensive, and environmentally hazardous. These additive printing processes are screen printing, flexography printing, offset printing, gravure printing, and inkjet printing [28]. Several materials are printed on a flexible substrate to construct PE circuits. Depending on the application, one or multiple printing processes can be used. Some of these processes, such as inkjet printing, enable a highly demanding feature: point-of-use fabrication [28], [29].

Several printed transistors such as p-type organic-based thin-film transistors (OTFTs) [7], organic field-effect transistors (OFETs) [6], and inorganic oxide semiconductor-based n-type transistors [10] are proposed to build functional PE circuits. Therefore, within one technology, only one type of transistor is possible which leads to transistor–resistor digital circuits. To demonstrate proposed circuits, we have used inorganic-based electrolyte-gated FETs (EGFETs) since they provide high intrinsic mobility and require low supply voltage ($\leq$1 V) when combined with electrolyte gate dielectric since EGFETs have high gate capacitance [10], [27]. In addition, EGFET possesses optical transparency and thermal stability. However, the lack of well-performing p-type EGFETs results in the circuits designed with n-type EGFETs in a pull-down network and a resistor as a replacement of p-type EGFETs [10].

As explained above, the research directions on PE circuits are mostly focused on printed transistors as well as other circuit elements [6], [7], [10]. However, there are few printed circuits in literature, and existing circuits such as inverters, latches and ring oscillators (ROs) contains limited numbers of elements [8], [9], [13]–[17], [22], [23]. The large-scale integration of printed transistors suffer extremely from the low yield and low performance of low-cost manufacturing printing processes such as inkjet printing. In addition, the performance of a functional circuit may not be sufficient for target applications since, to the best of our knowledge, the reported highest operation frequency of a printed RO in [9] is 1300 Hz.

III. Proposed pLUT

This section explains the motivation, the analysis of the existing LUT circuits in the context of PE, and the proposed pLUT design. Furthermore, the scaling of the design is elaborated to realize the high-volume production of the printed digital circuits with minimum overhead.

A. Motivation

In the supply chain of PE applications, which are ultra-low-cost devices in many cases, functional customization by end users or other parties in the supply chain is needed. Therefore, enabling such customization through programmability is desired. In addition, due to high intrinsic variations in this technology, manufacturing yield could be very low, especially for low-cost printing processes. (One-time) Programmable circuits can help to bypass defects to provide correct functionality despite the low manufacturing yield of the initial printing process.

Moreover, due to large feature sizes and rather simple circuit structures, counterfeiting is rather easy in PE applications. PE applications, especially for the medical field, have to be protected against counterfeiting since counterfeited products may lead to severe problems. For instance, inaccurate or wrong functionality of a medical sensor may lead to wrong diagnosis [5], [33], [34]. Therefore, countermeasures such as hardware watermarking and camouflaging should be considered in the design and fabrication flow of such applications. These countermeasures can be efficiently implemented using (one-time) programmable constructs and circuits.

For all these reasons, it is desired to have a (one-time) programmable building blocks for this technology. LUTs are common blocks to build programmable circuits. One-time

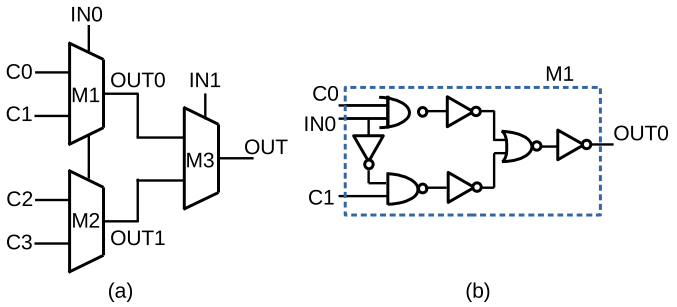

Fig. 1. LG-based LUT. (a) LUT2 implementation. (b) LG-based multiplexer implementation.

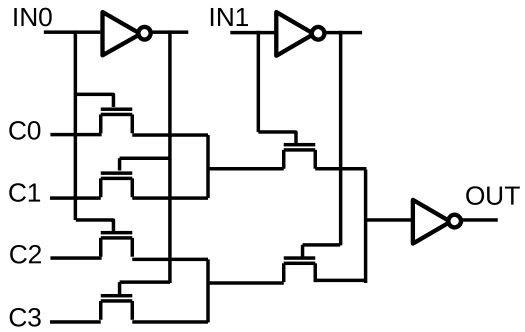

Fig. 2. PT-based LUT.

programmable LUTs are of interest in this article because of their efficiency.

B. Existing LUT Designs

In silicon technologies and for field-programmable gate arrays (FPGAs), three different LUT designs have widely been used [21]. The LUT2 circuits are revised according to one-time inkjet printing programmability and resistor—transistor logic in EGFET technology.

1) Logic Gate (LG)-Based LUT: The baseline implementation of LUT is based on logic gates as shown in Fig. 1. It has two inputs (IN0, IN1), four configurations (C0–C3) which can be connected to either VDD or GND to configure its functionality, and three 2-input multiplexers which contain two NAND, two INV, and one NOR gates as shown in Fig. 1(b). The disadvantage of this design is the large area usage.

2) Pass Transistor (PT)-Based LUT: This implementation, shown in Fig. 2, consists of two inputs (IN0 and IN1), four configurations (C0–C3) which can be connected to either VDD or GND to configure its functionality, six pass transistors (nMOS) to form the multiplexer, and an inverter to strengthen the signal quality. The PT implementation of multiplexers saves the area greatly. However, the PTs degrade logic-1 signals. Therefore, an inverter (or a half-latch) is required to improve the quality of logic-1 signals.

3) Transmission Gate (TG)-Based LUT: This design replaces PTs with TGs to improve the signal quality at the expense of pMOS transistors. However, due to the high area usage and the constraint of resistor–transistor logic, this structure cannot be realized in EGFET technology.

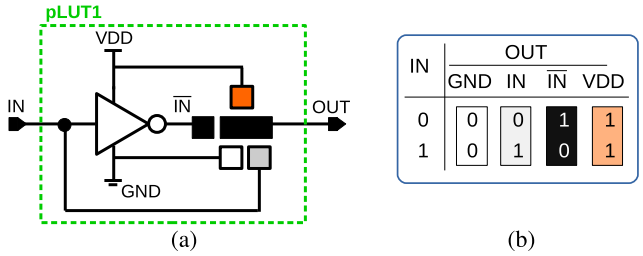

Fig. 3. (a) Proposed 1-input pLUT (pLUT1) in which functionality is set using inkjet-printed conductive inks. (b) Illustration of pLUT1 programmability in table form (pad colors indicate corresponding configuration in table).

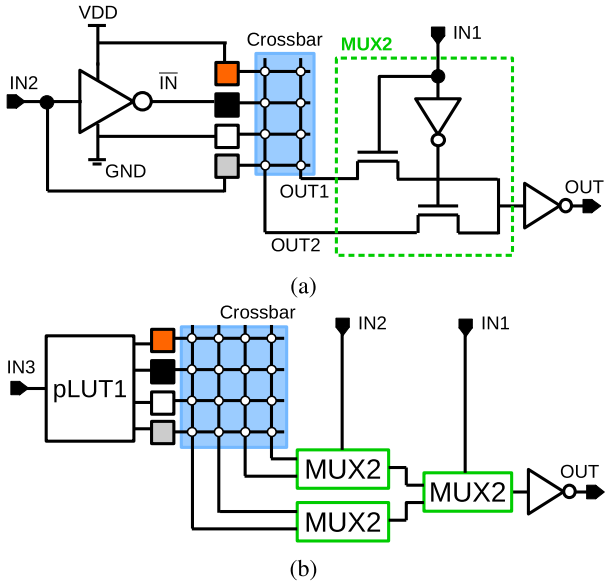

Fig. 4. (a) Proposed 2-input pLUT (pLUT2) containing multiplexer (MUX2). Crossbar is used to program LUT2 to desired functionality. (b) Proposed 3-input pLUT3.

C. Proposed pLUT Circuit

The core of the proposed LUT implementation is pLUT1 which is shown in Fig. 3(a). The proposed pLUT1 contains an inverter and wires to realize any 1-input/1-output functionality by printing conducting inks between the corresponding node and the output. The pads of ground (GND), input (IN), the inverse of input ($\overline{IN}$), or power supply (VDD) are placed close to the output pad of pLUT1 so that the output of pLUT1 can be easily connected to either GND, IN, $\overline{IN}$, or VDD using inkjet printed conductive inks to realize any functionality as illustrated in Fig. 3(b).

Using a pLUT1 and existing PT-based multiplexer (MUX2) consisting of an inverter and two PTs, N-input pLUT (pLUTN) can be constructed. Fig. 4(a) shows an LUT2 which is composed of a pLUT1, an MUX2, and an output inverter which improves the voltage level quality. A crossbar is used to connect pLUT1 signals to multiple intermediate outputs. As shown in Fig. 4(a), a pLUT1 and two intermediate outputs (OUT1 and OUT2) are used in the crossbar for LUT2 while for pLUTN, a pLUT1 and N intermediate outputs are used. Moreover, in this way, larger LUTs can be efficiently implemented as shown in Fig. 4(b). Therefore, the number of pLUT1 is constant for any input size LUT, which reduces complexity.

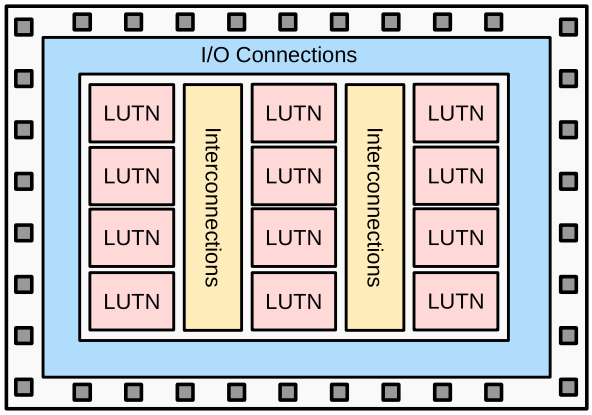

Fig. 5. Illustration of a programmable printed chip using N-input LUTs (LUTNs). Number of input, N, can be chosen based on requirements. Interconnections and I/O connections contains crossbars that are programmable and connects LUTNs and I/Os.

D. Overall System Architecture

The proposed pLUT implementation can be scaled to construct any LUT with pLUTN. Fig. 5 shows the system architecture of a programmable printed digital chip which is fabricated at the high-throughput fabrication center. I/O connections are to connect the input/output pad to pLUTNs and interconnections while pLUTNs are connected to each other through interconnections. I/O connections and interconnections are constructed using a crossbar so that the connectivity among pLUTNs and between pLUTNs and I/Os is programmed by inkjet printed conductive inks. Based on the placement and routing (P&R) of the hardware description language (HDL) design, the crossbars of I/O connections and interconnections are configured using inkjet printed conducting material inks (such as PEDOT:PSS) at the user site. It should be noted that the programmable circuit can be utilized in two ways. It can be some parts of a bigger PE design or complete programmable chip based on the usage scenario (see Section V).

E. Fabrication and Configuration Flow

The fabrication and configuration flow of pLUT-based programmable printed chip, to realize high volume and high throughput fabrication of PE circuits without sacrificing on-demand and point-of-use fabrication features, is illustrated in Fig. 6. In this flow, a programmable printed chip is fabricated using advanced high-throughput and high-yield fabrication techniques, which due to high costs, are only economical for high-volume production. In a subsequent step, end users are able to program it according to their specifications using low-cost processes such as inkjet printing. This way, the best of two worlds, high-throughput and high-yield fabrication as well as on-demand point-of-use customization, are achieved.

As illustrated in Fig. 6, the programmable printed chip is fabricated with advanced fabrication processes resulting in higher yield and better performance compared to low-cost fabrication processes (inkjet printing). At the point-of-use, the HDL (design.v) of the target design is synthesized using the standard cells used in the programmable printed chip (pLUT). The synthesized netlist (design_with_LUT.v)

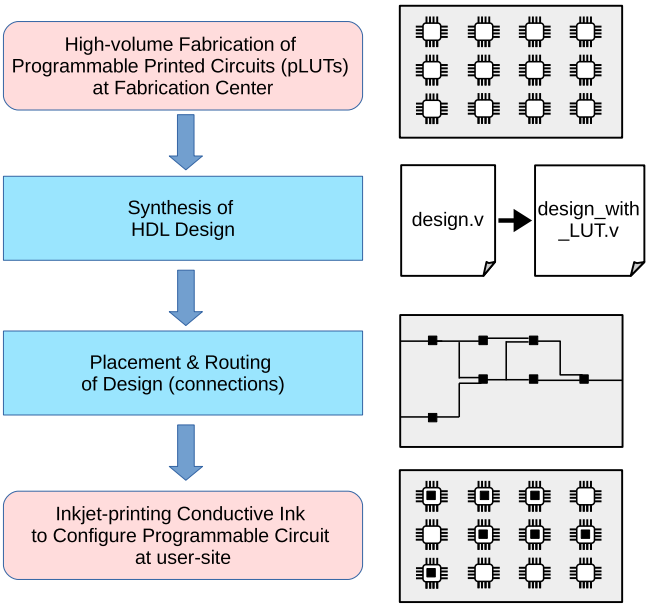

Fig. 6. Fabrication and configuration flow of pLUT-based programmable printed chip. A programmable printed chip is fabricated in high volume at the fabrication center. At the user site, the target design HDL is synthesized and then placed and routed (P&R) according to programmable chip. Finally, the programmable chip is configured using inkjet printing at point-of-use.

is converted into placement and routing file (P&R file) that contains the configuration information (configuration of LUTs and interconnections). Finally, the customization of the programmable printed chip is configured into desired functionality by inkjet printing conductive inks according to the P&R file. Therefore, the complex circuits can be easily implemented without dealing with the yield and performance issues.

IV. Experimental Results

In this section, we first provide a simulation-based analysis of the proposed pLUT and compare it with EGFET-based implementations of existing LUT designs. Afterward, we provide a fabrication-based evaluation of the proposed pLUT.

A. Simulation, Fabrication, and Characterization Setup

The simulation and measurement results presented in this section are based on the EGFETs which have the channel geometry of 200-μm width and 80-μm length, and the 100-kΩ resistors. We have employed the variation model of EGFET and process development kit presented in [11] and [12].

After the resistors, wires, and transistor electrodes are structured using laser ablation on a float glass substrate with 150-nm coated indium tin oxide (ITO), the substrates are cleaned with 2-propanol and acetone. The channel semiconductor material, indium oxide (In_2O_3) precursor, is inkjet printed with Dimatix 2831 inkjet printer between drain and source electrodes. Then, the substrates are annealed at 400 °C for 2 h. In the next step, composite solid polymer electrolyte (CSPE) is inkjet printed on top of the channel to cover it. After the CSPE is dried at room temperature, PEDOT:PSS is inkjet printed on top of electrolytes to form top-gate structure. In order to program circuits, PEDOT:PSS is inkjet printed

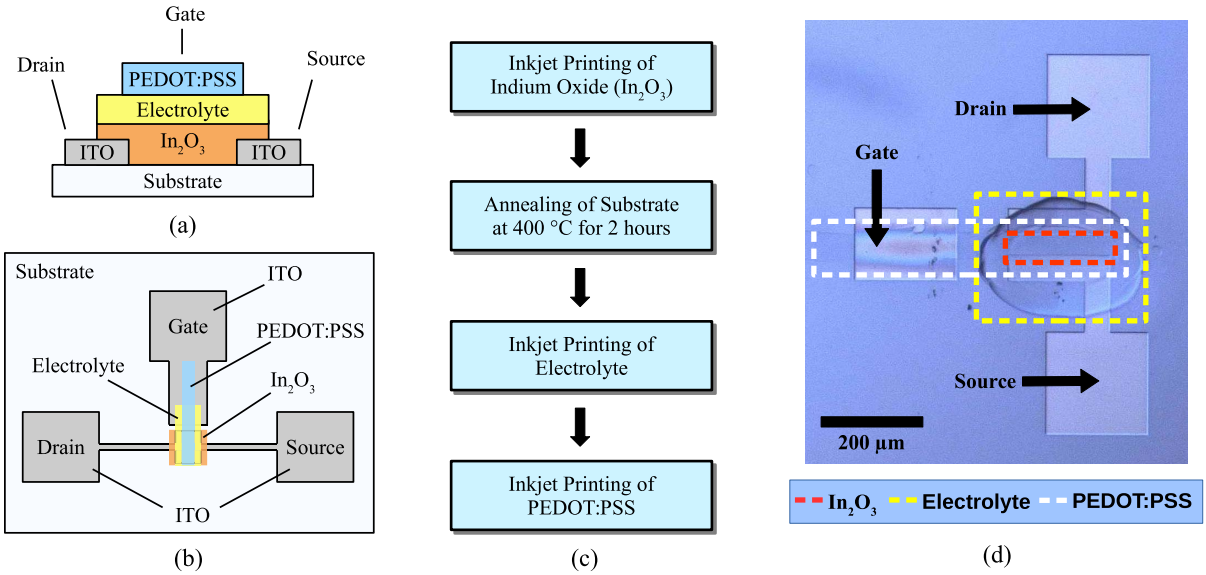

Fig. 7. Description of EGFET technology. (a) Cross-sectional view of EGFET [10]. (b) Top view of EGFET [10]. (c) Fabrication process of EGFET. (d) Optical image of a fabricated EGFET device.

TABLE I
COMPARISON OF VARIOUS LUT2 IMPLEMENTATIONS IN EGFET TECHNOLOGY IN TERMS OF AREA, DELAY, POWER, AND VOLTAGE LEVEL QUALITY AT 1 V

	LG-based	PT-based	pLUT
Area (mm^2)	120	28.2	17.4
Worst case delay (ms)	13.3	2.8	2.7
Average power consumption (μW)	192.561	29.661	24.717
Logic-1 level at output (V)	1	0.6	0.8

between the corresponding nodes. Fig. 7(a)–(c) shows the structure and the fabrication process of the EGFETs, and the optical image of a fabricated EGFET is shown in Fig. 7(d). It should be noted that the inkjet printed EGFET technology used in the fabrication of the proposed method is an emerging technology in which there are many challenges to be resolved for large-scale circuit fabrication. Moreover, due to our lab setup, we can only reliably fabricate and experimentally validate small-scale circuits. For this reason, we have only fabricated pLUT1 and pLUT2 to prove the concept.

The fabricated circuits are characterized and powered with Agilent 4156C semiconductor parameter analyzer and Yokogawa DL6104 digital oscilloscope. The input signals are generated with a Keithley 3390 arbitrary waveform generator. The measurements were carried out at room temperature and 70% relative humidity.

B. Simulation-Based Comparison of LUT Circuits

We have compared the EGFET-mapped LG-based, the PT-based, and the proposed pLUT implementations in terms of area, worst case delay, and average power consumption to strengthen different implementations. The comparison given in Table I is based on LUT2 implementation since it is the basic building block of the LUTs with more inputs. Moreover, the area, worst case delay, and average power consumption of various input-length LUTs (LUT1–LUT4) are shown in Fig. 8.

The results show that LG-based LUTs have much larger area usage, delay, and power consumption although it has high reliability as it has no signal degradation effect. The proposed pLUTs are better than PT-based LUTs in terms of area and delay since it reduces the number of PT levels using pLUT1 in the first level. Moreover, since the number of pLUT1 used in the pLUTs remains one as explained before, the average power consumption and the area usage of the pLUTs are increasing slower than the PT-based LUTs resulting in lower power consumption and less area usage while the number of inputs of pLUTs increases. The area usage of the proposed pLUT is 27%, 61%, 60%, and 53% of the area usage of PT-based LUT for the number of input of 1, 2, 3, and 4, respectively.

C. Circuit Synthesis Results With pLUT2

We synthesized various combinational circuits from ISCAS'85 [24] and École Polytechnique Fédérale de Lausanne (EPFL) [25] benchmarks using the proposed pLUT2 cells and compared with custom synthesis using EGFET standard cells (NOT, NAND, and NOR gates). The results are given in Table II. Since the pLUT2 has more area usage, latency, and power consumption than standard gates, it is expected that the synthesis results are worse than custom implementation using standard cells. However, such overheads are justified due to programmability features. This is the same in silicon-based technologies where FPGA-based implementations have higher area, delay, and power consumptions compared to full-custom application-specified integrated circuit (ASIC) implementations. Typically, for the implementation of complex Boolean functions such as XOR and XNOR, the pLUT2 is more efficient since only one pLUT2 cell is sufficient to realize these functions. For instance, c499, which is an XOR intensive circuit, has a higher maximum operating frequency ($F_{\max}$), less area usage, and less power consumption compared to custom synthesis.

TABLE II

COMPARISON OF SYNTHESIS RESULTS OF SEVERAL ISCAS'85 AND EPFL BENCHMARK CIRCUITS WITH STANDARD CELLS (NOT, NOR, AND NAND GATES) AND PROPOSED pLUT2 CELL

	F_{max} [Hz]			Area [cm^2]			Total Power [W]			Total Cells		
Circuit	Gates	LUT2	Diff	Gates	LUT2	Diff	Gates	LUT2	Diff	Gates	LUT2	Diff
c17	336.01	336.23	0.07%	0.55	1.26	129.14%	0.00067	0.000368306	-45.03%	9	8	-11.11%
c432	43.19	39.84	-7.76%	11.07	21.94	98.10%	0.003674	0.003936444	7.15%	183	133	-27.32%
c499	39.38	79.64	102.24%	33.06	32.66	-1.21%	0.016668	0.006743485	-59.54%	547	190	-65.27%
c1908	28.98	55.27	90.72%	29.02	37.32	28.60%	0.0110684	0.0012733049	-88.50%	475	216	-54.53%
c2670	32.40	41.83	29.10%	47.594	77.96	63.82%	0.0142332	0.004219984	-70.35%	824	609	-26.09%
c7552	20.52	21.96	7.04%	107.01	175.69	64.18%	0.02973	0.033540835	12.82%	1762	1146	-34.96%
adder	4.48	4.41	-1.57%	78.47	191.81	144.43%	0.015054	0.032469592	115.68%	1274	1194	-6.28%
barrel shifter	87.99	73.35	-16.63%	250.40	649.90	159.54%	0.117369	0.149192	27.11%	3741	3742	0.03%
max	2.07	1.87	-9.67%	222.35	504.91	127.08%	0.033004	0.078386967	137.51%	3643	3102	-14.85%
sine	5.60	7.71	37.68%	420.95	752.458	78.75%	0.086911	0.0237784098	-72.64%	6845	4651	-32.05%
Average			23.12%			89.25%			3.58%			-27.24%

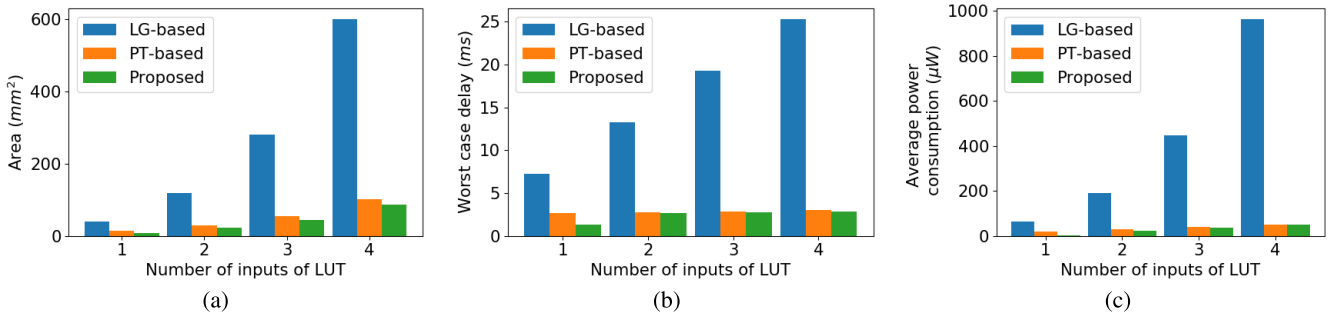

Fig. 8. Comparison of various LUT implementations with different number of inputs in terms of area, delay, and power.

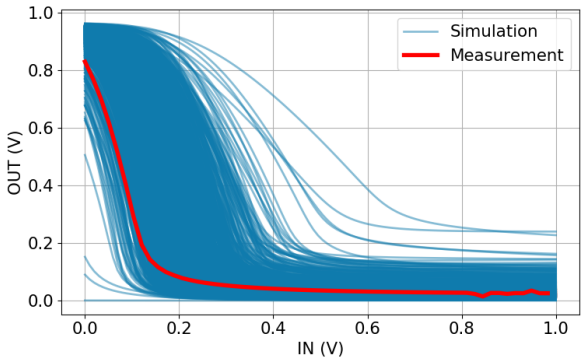

Fig. 9. Monte Carlo simulation and measurement of CLUT1 programmed as inverter ($\overline{\text{IN}}$).

The average improvement of the maximum frequency is 10.53% resulting from the efficient implementation of complex gates with the pLUT2 and the less delay overhead of the pLUT2. The average overhead of the area usage and the power consumption are 103.04% and 27.96% caused by the high area and power overhead of the pLUT2 compared to standard gates. Since the pLUT2 can implement complex Boolean functions with less number of cells, the average reduction of the number of cells is 22.82%.

D. Fabrication Results of Proposed pLUT

We have fabricated four pLUT1 and programmed them for four different configurations which are all-0 (GND), buffer (IN), inverter ($\overline{\text{IN}}$), and all-1 (VDD) as shown in Fig. 3(a) and (b). Fig. 9 shows that the dc measurement of a pLUT1 programmed for inverter functionality matches with the range of simulation results extracted from 100 Monte Carlo samples using the EGFET variation model [11]. The other three functionality measurements of pLUT1 are also as expected.

We have also fabricated multiple pLUT2s to demonstrate the preliminary results of the programmability of the proposed design. One of the pLUT2 is programmed as XNOR gate, while others are programmed as XOR and AND gates to construct half-adder. The images of pLUT2 programmed as XOR and AND are shown in Fig. 10. The programmed pLUT2s are characterized to prove their functionality at 1 V. Fig. 11 shows the behavior of three programmed pLUT2s in all input conditions at the supply voltages of 1 V. The level of logic-1 at the output does not reach VDD due to the PTs and resistor–transistor logic, as the PTs reduce the voltage level by threshold voltage (Vth), and the logic-0 for the inverters controlling the PTs is slightly more than 0 V (GND) resulting in higher leakage current in disabled PTs. For instance, as shown in the waveform of pLUT2 programmed as XOR, the output levels for "01" and "10" input values are 0.55 and 0.8 V. For "01," the PT transmitting the signal reduces 1 V (VDD) by Vth, whose mean value for EGFETs is 0.2 V, and the other PT disabled by above 0-V signal leaks more current resulting in low logic-1 (0.55 V). To solve this problem, an inverter or a half-latch can be used to improve the logic-1 voltage level. Note that the fabrication results of the pLUT2 do not contain inverter/half-latch at the output.

Moreover, the average power consumption of the fabricated pLUT2 is 25.12 μW while the worst case delay is 73.28 ms.

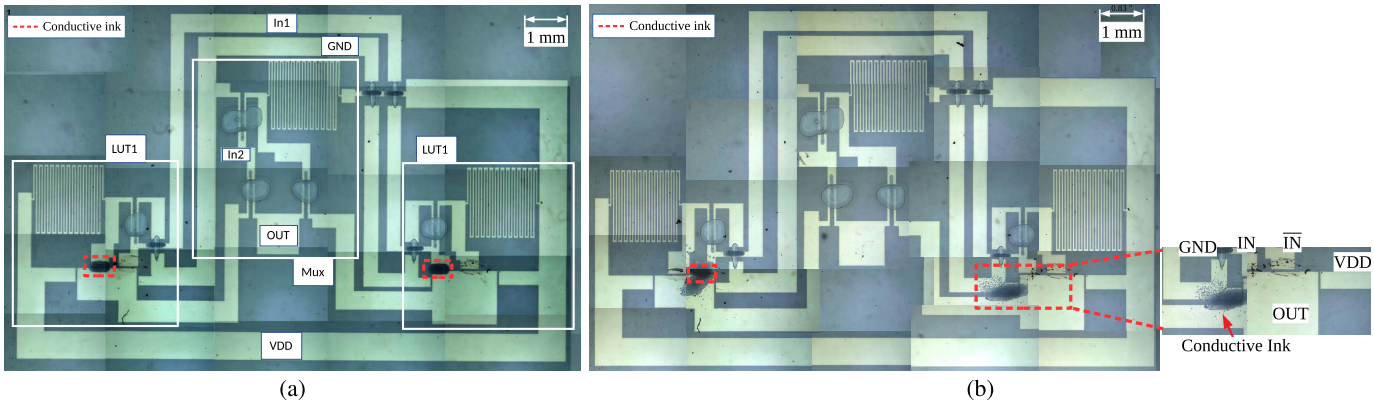

Fig. 10. LUT2s programmed with inkjet-printed conductive inks as (a) XOR gate and (b) AND gate.

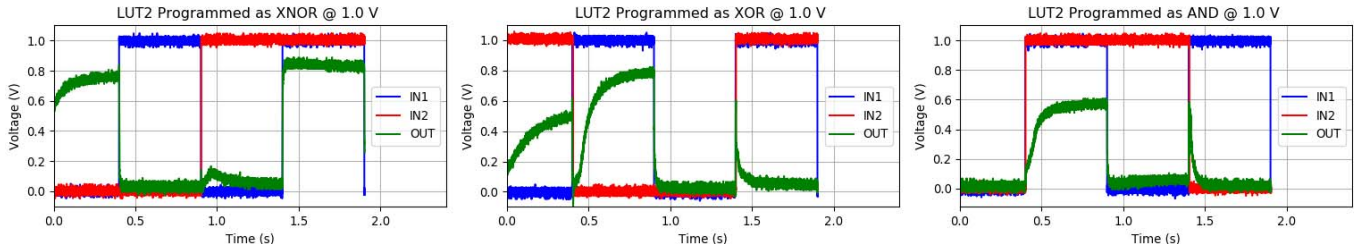

Fig. 11. Timing diagram of the fabricated programmable circuit. Left: LUT2 programmed as XNOR at 1 V. Middle: LUT2 programmed as XOR at 1 V. Right: LUT2 programmed as AND at 1 V.

In addition, the area usage of a pLUT2 is 60 mm^2 which is higher than the area usage value given in Table I due to the test pads and exaggerated wire widths for the prototype.

V. Programmable Components in PE Applications

The proposed programmable circuit can be utilized for different purposes. As explained before, since the yield of PE circuits fabricated with low-cost fabrication processes is low, the chip can be fabricated in an advanced production center resulting in high yield, and programmed using a low-cost and on-demand processes (e.g., inkjet printing). In addition, the failures can be mitigated bypassing defective parts of the circuit through rerouting. For instance, after the initial configuration is done, the defective parts are identified using digital testing methods. Then, these parts of the design are rerouted and configured into functional elements left in the neighborhood for this purpose. In this way, the yield can be improved while maintaining point-of-use functionality customization. This concept is similar to what has been done in the research direction of the defect and fault tolerance in FPGAs and reconfigurable computing in which several methods and defect-aware P&R have been proposed [35]–[37]. Moreover, in the context of high volume fabrication, this enables high throughput fabrication, which lowers the overall fabrication cost. Therefore, the proposed LUT-based printed digital circuit can be used to improve yield, performance, and fabrication throughput.

Another usage scenario of the proposed programmable circuit is that the end customers of the programmable circuit buy soft IPs (register transfer level (RTL) level) from a central IP provider, follow the fabrication and configuration flow in Fig. 6, to convert the IP into the configuration information of the chip, and then print the connections of programmable circuits in the point-of-use (user site). This allows the decentralized manufacturing of printed circuits. However, this scheme is vulnerable to IP piracy where one end customer share the IP with other unauthorized end customers. The countermeasure against IP piracy is hardware watermarking where IP owners introduce a watermark into their design at different levels to claim their ownership [30], [32]. In this scenario, the IP owner can constraint the IP at placement and routing level such that it uses certain different pLUTs in the chip for different end customers as a watermark, which allows tracing the source of IP piracy [31].

Last but not least, in the scenario where the entire design is manufactured in a fabrication center, the attacker can overproduce the circuit and sell it on the market or reverse engineer the design [26], [31]. To prevent this, the designer can use the programmable circuit to prevent this security threat using two separate manufacturing steps. At the fabrication center, programmable circuit is fabricated, and the configuration is implemented at point-of-use. Therefore, the fabrication center cannot overproduce or reverse engineer the design since there is no functionality implemented at this step, which will be performed by the designer at the point-of-use [31].

The above-mentioned security countermeasure is resulted from the intrinsic feature of programmable printed circuit and targets the attack performed at the production center. However, after the connections of the circuit are fabricated, one can buy the product, reverse engineer the design, and counterfeit it [26], [31]. Since the connections are optically visible, it is comparably easy to automatically reverse engineer design. To conceal the connections, a simple countermeasure is to fabricate a nonconductive ink, which looks

optically similar to the conductive one, to other nodes. In this way, the connectivity information is optically camouflaged, which dramatically increases the reverse engineering effort of the attacker.

VI. Conclusion

In this article, we proposed a pLUT which was suitable to combine advanced high-throughput and high-yield fabrication processes and low-cost inkjet printing for on-demand customization to realize high-volume printed circuits while improving performance and yield without sacrificing on-demand point-of-use customization. The proposed pLUT has been fabricated, programmed with inkjet printing, and characterized. The results show that the proposed circuit is programmable to realize any digital functionality, and operates at 1 V. Moreover, we discussed the pLUT utilization for yield, performance, and security purposes.

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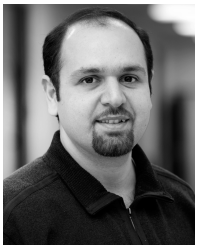

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