Dead Time Control Circuit in Monolithic GaN Class D Audio Amplifier

Master of Science Thesis

by

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Abstract

GaN transistors have advantages over conventional Si MOSFETs, such as lower on-resistance, lower parasitic capacitance, higher break-down voltage, etc. However, due to the lack of the body diode, when GaN transistors conduct reverse current during dead time, the source-drain voltage (V_{SD}) can be very large (up to 4-5 V, depending on the output current). High reverse conduction voltage leads to large power loss during dead time for the GaN class D amplifier. In this project, a dead time control circuit is proposed. With the dead time control circuit, the dead time can be reduced from a large default value to around 5 ns. The output power of the class D amplifier can be improved, and the third-order harmonic distortion can also be improved by 5-10 dB for different corners and temperatures.

Index items: Dead time control circuit; GaN class-D amplifier; monolithic GaN circuit

Acknowledgments

I never expected so many things to happen in the past two years. It was the first time I came to a place far from my hometown to go for a master's program. It was the first time I changed my major and the research field which I had worked for four years during my bachelor. It was the first time I lived totally on myself. Every day is challenging and exciting.

This thesis project is also the first project I have done with analog circuit design. The first time I heard about the topic of this program, I was attracted by its novelty. And through the project, I really learned a lot in terms of both circuit design and team collaboration. I would really say thanks to all the people who collaborated on this project: Pablo, Huajun, and Miao. More importantly, I would thank my supervisor Qinwen Fan. She is really responsible and always comes up with innovative ideas. She really gave me lots of help throughout the whole project. I would also thank Marco. He is a very experienced expert and also gave very helpful advice.

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Finally, I would say thanks to my parents and grandparents. They are all very supportive of my decision. And they give me huge energy when I face problems and feel upset. So do my best friends Hanwen and Mingyu. Hope to see everyone again soon!

Jing Pan

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Contents

Chapter 1 Introduction

1.1 Backgrounds of Class-D Amplifier

Class D amplifier is a good candidate to drive the load impedance of the loudspeakers, which can be modeled as an R-L series network with a few ohms resistance. Since the power transistors in class D amplifiers act like switches with a small on-resistance, compared with conventional class AB amplifiers, class D amplifiers have lower power dissipation and exhibit high power efficiency, which is typically larger than 90%. In this chapter, the basic working principle of the class-D amplifier is going to be introduced.

1.1.1 Pulse Width Modulation (PWM)

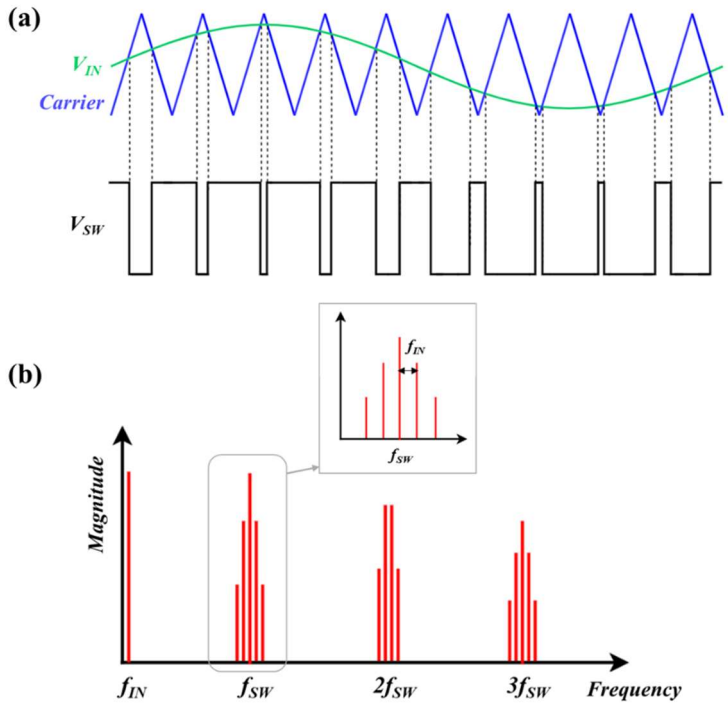

Figure 1.1 Natural sampling PWM in (a) time domain and (b) spectrum domain

To encode the input analog audio signal, pulse width modulation (PWM) is usually used. As shown in Figure 1.1 (a), a square waveform is generated by comparing the input V_{IN} with a triangle carrier signal, whose frequency f_{SW} is usually much higher than the highest audio frequency [1]. This procedure is called natural sampling PWM. The

output square wave carries the information of the input audio signal by varying duty cycles. Figure 1.1 (b) shows the spectrum of the PWM signal. By applying an LC low-pass filter, V_{IN} can be recovered from the PWM signal.

1.1.2 Class D Amplifier Output Stage

Figure 1.2 shows a Bridge-tied-load (BTL) class D amplifier output stage [1]. Power transistors in the class-D amplifier act like switches and operate in the linear region. The input audio analog signal is modulated by PWM into the digital domain. The signal at the switching node V_{SW} contains high-frequency components, which will be filtered out by the following LC filter. After the LC filter, the audio signal recovers back to the analog domain and drives a speaker.

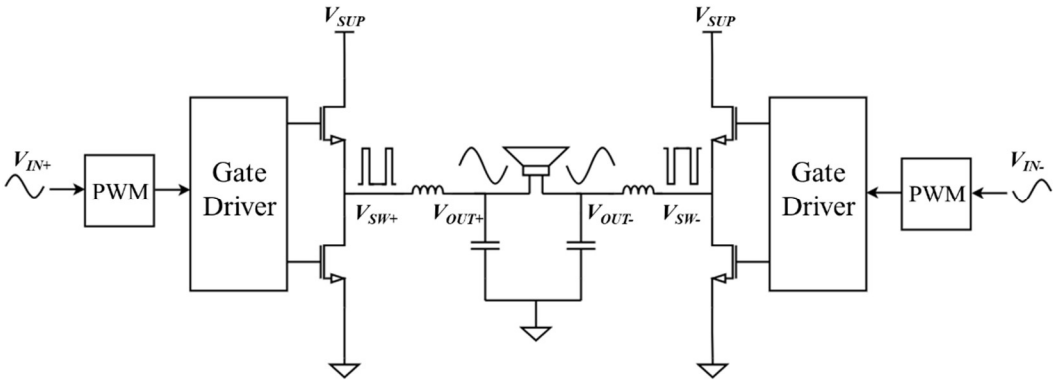

Figure 1.2 Bridge-tied-load (BTL) class D amplifier output stage

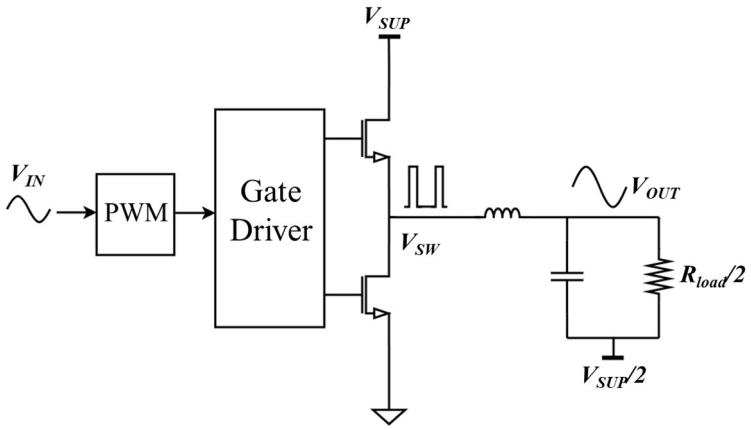

Figure 1.3 Equivalent half-bridge output stage

If the loudspeaker can be regarded as a resistive load, due to the symmetry of the BTL configuration, the voltage of the middle point of the resistive load R_{load} is always at the middle of the supply voltage V_{SUP} if the two sides are perfectly matched. Therefore, an equivalent half-bridge output stage can be used for simplicity, as shown in Figure 1.3.

1.1.3 Switching Node Behavior during Dead Time

In the class D output stage, high-side and low-side power transistors cannot be turned on at the same time, otherwise, the supply is directly connected to the ground, which is called cross conduction or shoot-through and will induce a huge current and damage the chip. Cross-conduction can be avoided by applying a break-before-make method [2]. This results in dead time, during which the high-side and low-side power transistors are both OFF.

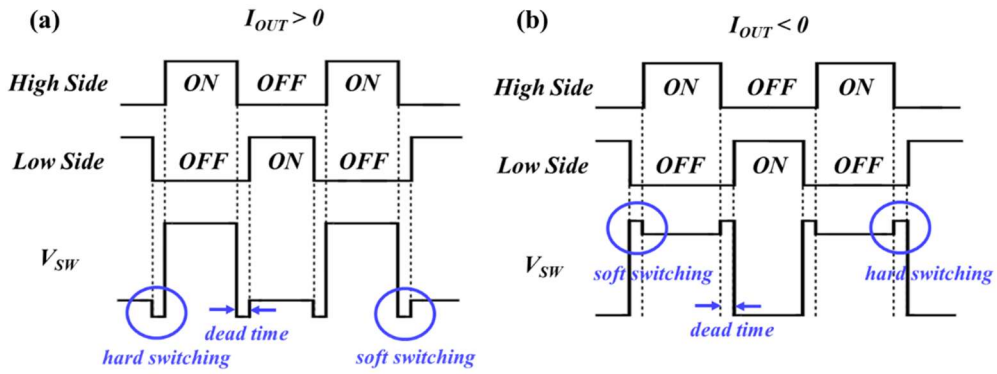

Figure 1.4 V_{SW} waveform for (a) output current flowing out of V_{SW}; (b) output current flowing into V_{SW}

Due to the inductive load, the output current still flows during dead time. In conventional CMOS technology, this current flows through the body diode of one power transistor, which induces one diode forward voltage drop added to V_{SW}, as Figure 1.4 shows. The reverse conduction principle in GaN technology is quite different, which is going to be discussed in Section 1.3.2. The transitions of the rising and falling edge of V_{SW} are not symmetrical. If the transition occurs after the dead time, e.g. the rising edge of V_{SW} when I_{OUT}>0, it is called hard switching; if the transition occurs before the dead time, it is called soft switching.

1.2 GaN Transistors and Monolithic GaN Class-D Amplifier

Compared with conventional silicon MOSFETs, GaN transistors have uniqueness in several aspects. This section starts with the comparisons of GaN and Si material properties. Then in Section 1.2.2, the conduction principle of GaN transistors and the device structure are introduced. Finally, the strengths of monolithic circuits over discrete circuits are demonstrated. This part gives explanations of why GaN is chosen to be explored with the class D amplifier, and why the monolithic circuit is chosen to be investigated.

1.2.1 GaN Material Property

Table 1.1 lists some material properties of silicon (Si) and Gallium nitride (GaN). Compared with Si, GaN has a larger bandgap E_g and higher critical electric field E_{crit}. A larger bandgap means a higher strength of the chemical bonds between atoms [3]. So GaN devices can operate under higher temperatures. With a higher critical electric field, GaN transistors have a larger breakdown voltage [3]. As a result, GaN devices have great potential in high-voltage applications and extreme-environment applications.

Table 1.1 Material properties of Si and GaN [3]

Parameter	Unit	Si	GaN
Bandgap E_g	eV	1.12	3.39
Critical electrical field E_{crit}	MV/cm	0.23	3.3
Electron mobility	$cm^2/V/s$	1400	1500
Hole mobility	$cm^2/V/s$	480	30

From Table 1.1, the electron mobility of GaN is larger than that of Si. Due to the two-dimensional electron gas (2DEG) formed in the GaN transistor, the electron mobility in the GaN transistor is even higher, which makes the on-resistance of GaN transistors lower than Si MOSFETs [3]. Section 1.2.2 will further explain this point.

Another thing that we can figure out from Table 1.1 is that the hole mobility of GaN is much lower than that of Si, so to make a symmetric inverter, the width of the p-type transistor should be >50 times larger than the width of the n-type transistor [10]. Therefore,

p-type GaN transistors are less promising in circuit design and are absent in the commercial GaN process.

Table 1.2 shows the comparison between the IMEC 200V GaN transistor and the Infineon 200V power MOSFET. To evaluate the switching behavior of a transistor, a Figure of Merit (FoM) is defined as follows [4]:

$$\text{FoM} = R_{DS,ON} \times (Q_{GD} + Q_{GS}) \qquad (1.1)$$

It can be discovered that the GaN transistor has much lower FoM compared with Si MOSFET, meaning a much lower transition loss for GaN transistors theoretically.

Table 1.2 Comparison between GaN transistor and Si MOSFET (200V power transistor)

	$R_{DS,ON}$	C_{ISS}	C_{OSS}	C_{RSS}	FoM
IMEC 200V GaN	6.3 mΩ	55 pF	35 pF	0.98 pF	3.66 p
Infineon power MOSFET IRFP4668PbF	8.0 mΩ	10.72 nF	810 pF	160 pF	856.3 p

1.2.2 Conduction Principle and Device Structure of GaN Transistors

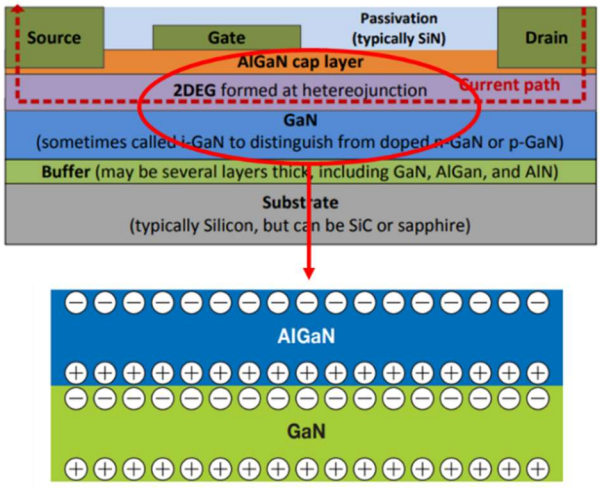

Figure 1.5 Typical structure of GaN transistor and 2DEG generation [3, 6]

The conduction of the GaN transistor is due to the 2-dimensional electron gas (2DEG) generated at the interface of the GaN/AlGaN heterojunction, as Figure 1.5 shows. Electrons are confined in a very small region at the interface of the heterojunction so they are named two-dimensional electrons. The 2DEG is generated by the piezoelectric effect

and spontaneous polarization induced effect, and can further increase the electron mobility in GaN transistors compared with unstrained GaN material [3, 5].

If an external voltage is applied to the GaN/AlGaN heterojunction as Figure 1.6 shows, then a large current is induced at the interface. This is the drain-source current formation principle in the GaN high electron mobility transistor (HEMT).

Because the 2DEG is automatically formed at the interface of AlGaN/GaN [6], to build an enhancement-mode transistor, an extra layer is needed to deplete out electrons when the gate voltage is zero, as Figure 1.7 shows. This layer is usually implemented by p-doped GaN or p-doped AlGaN.

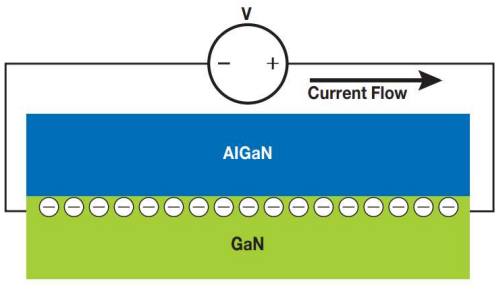

Figure 1.6 GaN/AlGaN heterojunction with an externally applied voltage [3]

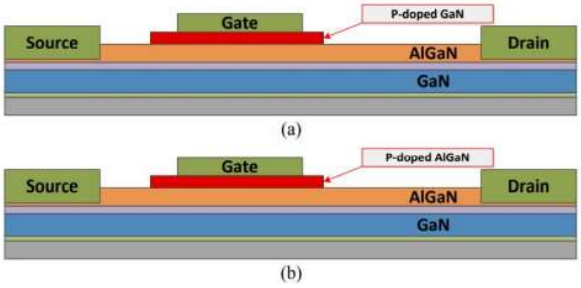

Figure 1.7 Structure of enhancement-mode GaN transistors [6]

For GaN transistors, there is no body diode formed inside the device. The lack of the body diode makes GaN transistors free from reverse recovery loss [3]. This phenomenon impacts the high-frequency performance of a circuit [7] and will not happen in GaN transistors.

1.2.3 Monolithic GaN Circuit

As Figure 1.8 shows, a monolithically integrated circuit integrates gate drivers, power transistors, etc. in a single chip, while in the discrete circuit, gate drivers and power transistors are separate, and bonding wires are needed to connect different parts. Compared with discrete circuits, monolithically integrated circuits have less parasitic inductance caused by bonding wires, PCB wires, etc., which leads to the two advantages listed below.

- The transient time of monolithically integrated circuits can be reduced, so circuits can operate at a higher frequency [9].
- It can prevent ringing at the gate of the power transistor [10].

In consideration of less propagation delay and less ringing, the monolithic GaN class D amplifier is chosen to be investigated in this thesis.

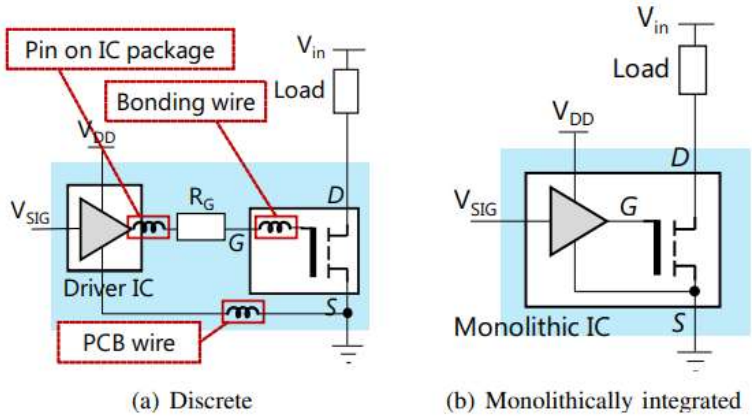

Figure 1.8 Discrete and monolithically integrated GaN circuit [8]

1.3 Problem Statement

In Section 1.2, we conclude that GaN devices have great potential in high-voltage applications. However, because of the absence of the body diode, GaN transistors suffer from larger V_{DS} voltage drops when they conduct reverse current compared with Si MOSFETs.

As the left figure in Figure 1.9 shows, for the Si MOSFET, when $V_{GS} < V_{th}$ and $V_{GD} < V_{th}$, body diode conducts the reverse current, which has the forward voltage of 0.65 V.

As the right figure in Figure 1.9 shows, for the GaN transistor, when $V_{GS} = 0$, $V_{SD} = V_{GD} - V_{GS}$ should be larger than the threshold voltage to turn on the transistor ($V_{GD} > V_{th}$ to form 2DEG). Since the threshold voltage is relatively high for GaN transistors, a larger voltage drop exists between drain and source (V_{DS}) for GaN transistors compared with Si MOSFETs during the dead time, which leads to larger power loss during the dead time [7].

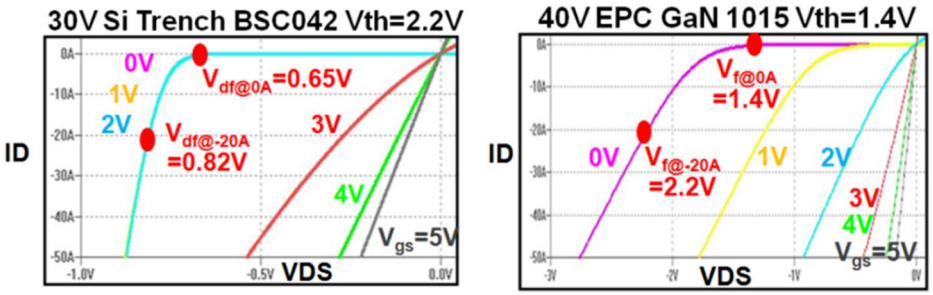

Figure 1.9 I_{DS} vs. V_{DS} curves for Si and GaN transistors in reverse conduction [7]

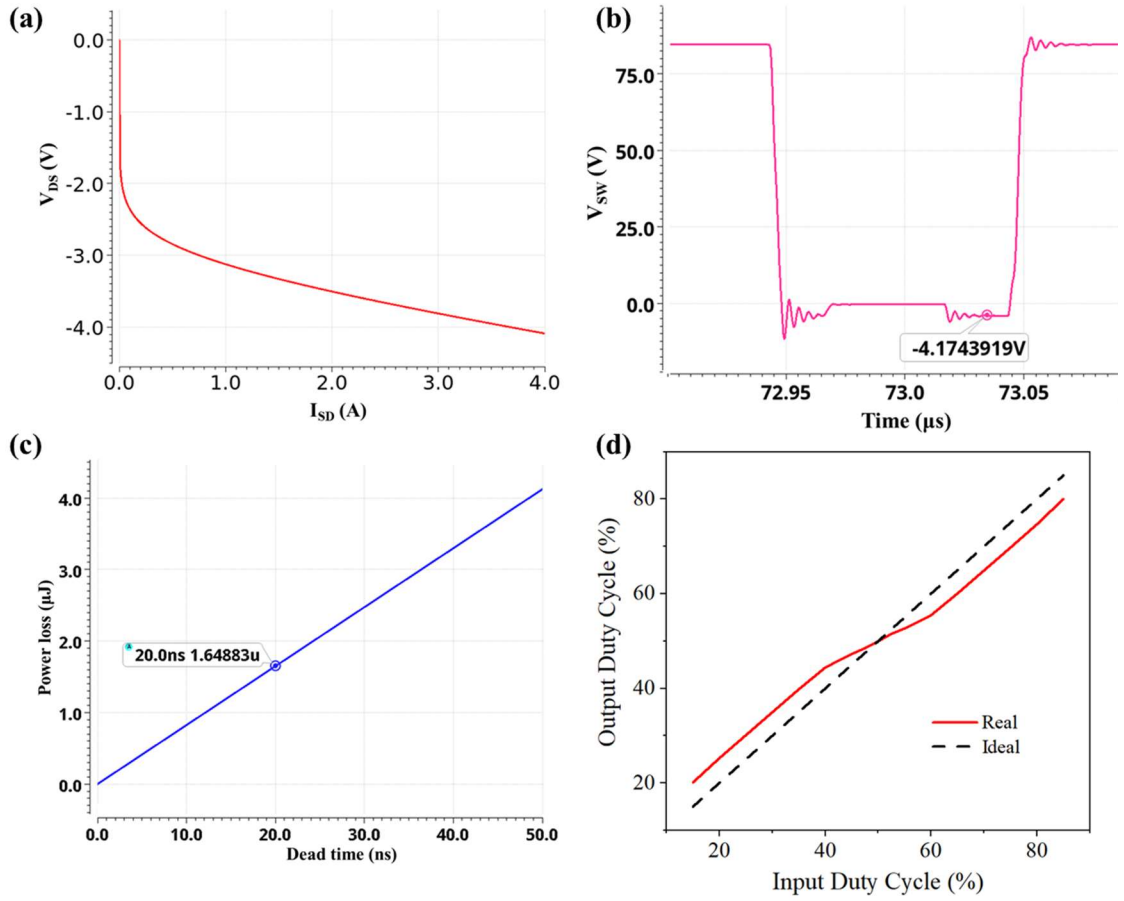

Figure 1.10 (a) V_{DS} vs. I_{SD} curve for a power transistor; (b) V_{SW} curve; (c) power loss vs. dead time; (d) Input duty cycle vs. output duty cycle

Figure 1.10 (a) shows a typical V_{DS} vs. I_{SD} for the IMEC 200 V GaN power transistor with $V_{GS} = 0$, and Figure 1.10 (b) shows the voltage at the switching node V_{SW} of a class D amplifier. It can be discovered that when conducting reverse current, $|V_{DS}|$ is dependent on the current flowing in the transistor. During dead time, when transistors conduct reverse current, V_{DS} can reach -4 V or even lower, which results in large power loss during dead time. Figure 1.10 (c) shows the power loss vs. dead time curve for a power transistor with 100 mΩ and 8 A output current. Considering 2 MHz switching frequency and 20 ns dead time, the conduction loss for each period is 40 nJ. The power loss due to dead time is 1.65 μJ, which is huge compared with the conduction loss. Furthermore, due to the dead time, the output duty cycle deviates from the input duty cycle, which results in distortion of the output signal, as Figure 1.10 (d) shows.

In order to reduce the loss during dead time and improve the distortion, one possible solution is to reduce the dead time. So a dead time control system is needed in the GaN class D circuit to lower the power loss during dead time and achieve better power efficiency for the circuit.

1.4 Literature Review

There are different ways to modulate dead time. In reference [11], a dead time control circuit is proposed to modulate the falling edge of V_{SW}. As Figure 1.11 shows, the dead time control circuit is used to add a delay time at the rising edge of the low-side input signal. The delay time is controlled by a voltage V_C. A sample and hold circuit is used to hold the voltage of V_{SW} at the time when the low-side power transistor is about to turn on (node B in Figure 1.11). Since the aim of the control is to achieve zero-voltage transition (ZVS), this voltage indicates whether the dead time is overlong or insufficient. An OTA is used to convert the sampled voltage to the control voltage V_C.

This circuit has pros and cons in the following aspects. One advantage is that the circuit is not “real-time”. It samples V_{SW} at one period and makes adjustments to the delay time for the next period. Therefore, the speed of the circuit is not demanding. The limitations of the circuit are that the circuit can only modulate the falling edge of V_{SW}, and is implemented by BCD technology. Without p-type transistors in GaN technology, it is difficult to implement the current mirror in Figure 1.11.

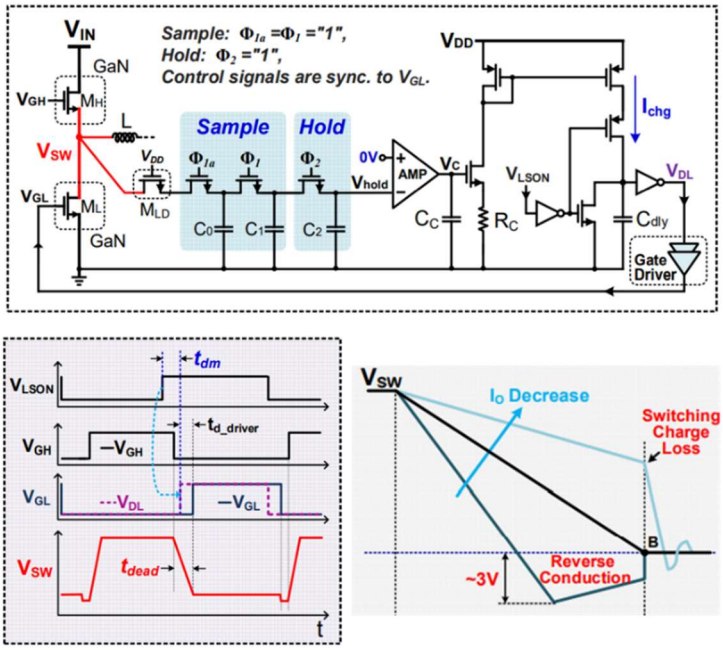

Figure 1.11 Single-edge dead time modulation [11]

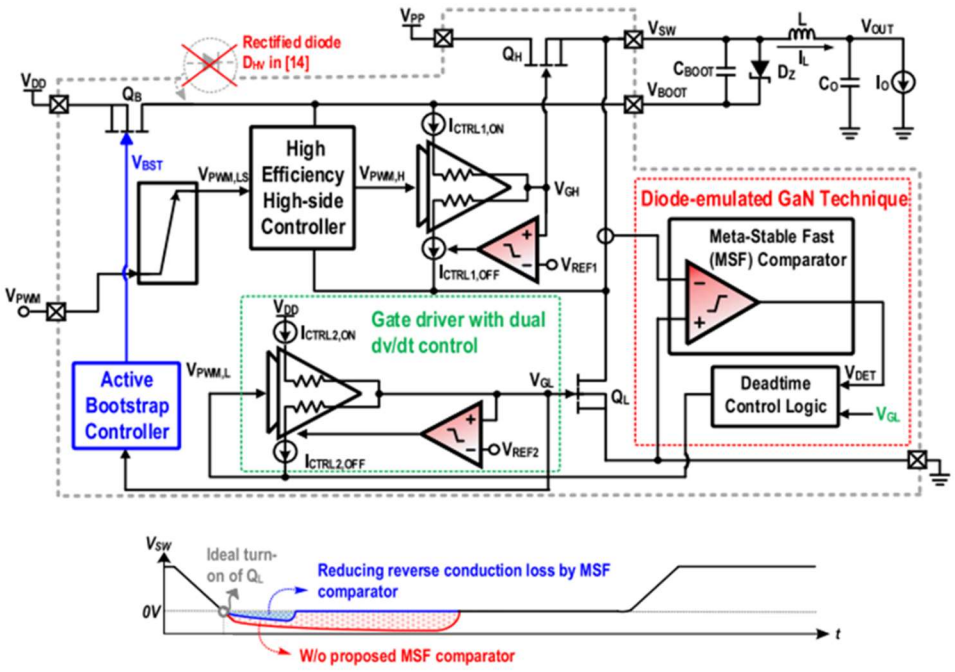

Figure 1.12 “Real-time” dead time modulation [12]

Another kind of dead time control circuit is proposed in [12]. As Figure 1.12 shows, the dead time control circuit is integrated with a monolithic GaN half-bridge circuit. In this circuit, a comparator is used to compare the source and drain voltage of the low-side power transistor. When the circuit enters dead time, the V_{DS} of the power transistor is

negative and the V_{GL} is low. A logic circuit is used to make judgments, and after the circuit enters dead time, this logic circuit can immediately flip and turn on the low-side power transistor.

Compared with the previous circuit, this circuit can realize "real-time" control of the dead time. By applying the circuit, the dead time can be reduced to <0.2 ns, which means the propagation delay time of the comparator, the logic circuit and the gate driver should be only hundreds of picoseconds. So the speed requirement of each block is very demanding. Besides, this circuit needs to use depletion-mode GaN transistors, which may not be available in other GaN processes.

For the dead time control circuits proposed in previous works, there are some common limitations. First, dead time control circuits can only work for single-edge modulation. Second, dead time control circuits are realized using BCD technology instead of integrating with GaN power transistors. Or they need depletion-mode devices, which is not available in some GaN process. Finally, they are used for fixed duty-cycle input signals. Regarding these limitations, the design targets of the proposed dead time control circuit in this project are discussed in the next section.

1.5 Design Targets

In Section 1.3, the significance of the dead time control circuit in a monolithic GaN circuit is emphasized. To integrate the dead time control circuit in the GaN class D amplifier, the following specifications should be achieved in the design of the circuit.

- The dead time control circuit should have the capability to handle a default dead time of 20 ns of the class D amplifier. The input PWM signals of the class D amplifier have initially 20 ns dead time to prevent shoot-through of power transistors. After applying the dead time control circuit, the dead time of both rising and falling edges should be reduced.
- The dead time control circuit should function well for the class D amplifier with a -3 dBFS sinusoidal input signal at a switching frequency of 2 MHz. This means the circuit can operate with signals with 15% to 85% of the duty cycle. Some margins are left because extreme duty cycles lead to very little time for one side power transistor, which can cause problems in modulating one of the two edges.

- The dead time control circuit should function well for all the process corners and temperatures from 25℃ (room temperature) to 100℃. Since the current in power transistors of the class D output stage can reach up to 8.5 A, the chip temperature will increase for a long working time. The proposed dead time control circuit should also operate well with high temperatures.
- To make sure no shoot-through after dead time modulation for all the process corners, temperatures and load current conditions, a residual dead time is desired and is set to be 5 ns. For the case shown in Figure 1.13, at the end of the dead time, it needs 3.25 ns for the gate driver to pull up the low-side V_{GS}. Therefore, the measured dead time is larger than the real dead time. In order to avoid the circuit ending up in negative dead time and suffering conduction for all the cases, the residual dead time is set to be 5 ns.

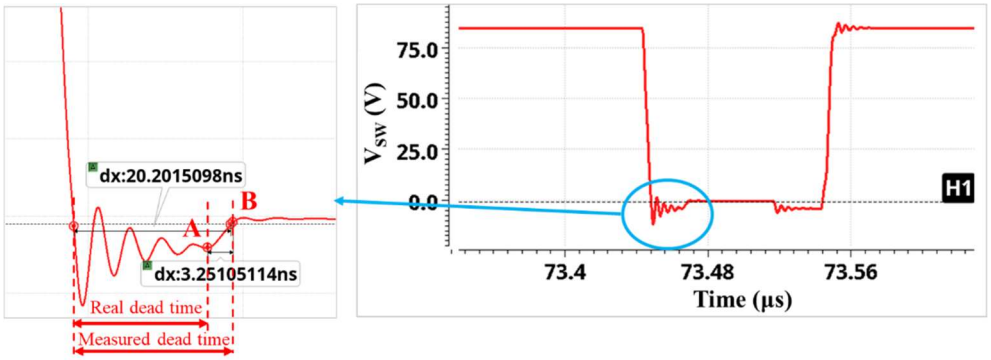

Figure 1.13 Measured dead time and real dead time (for the typical corner, 25℃)

- After applying the dead time control circuit, both output power and the distortion of the output signal should be improved, because the output duty cycle gets closer to the input duty cycle. If the dead time is assumed to be reduced from 20 ns to 5 ns, for 85% or 15% duty cycle input signals, the output power can be improved by 1.2 times theoretically.

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Chapter 2 Dead Time Control Circuit System-level Design

In Chapter 1, the significance of the dead time control circuit in monolithic class D amplifiers is analyzed. And the design targets of the dead time control system are listed. This chapter will focus on the system-level design of a proposed dead time control circuit. In order to meet all design targets suggested in Section 1.5, specific requirements for each circuit block are discussed.

2.1 Dead Time Control Circuit Structure

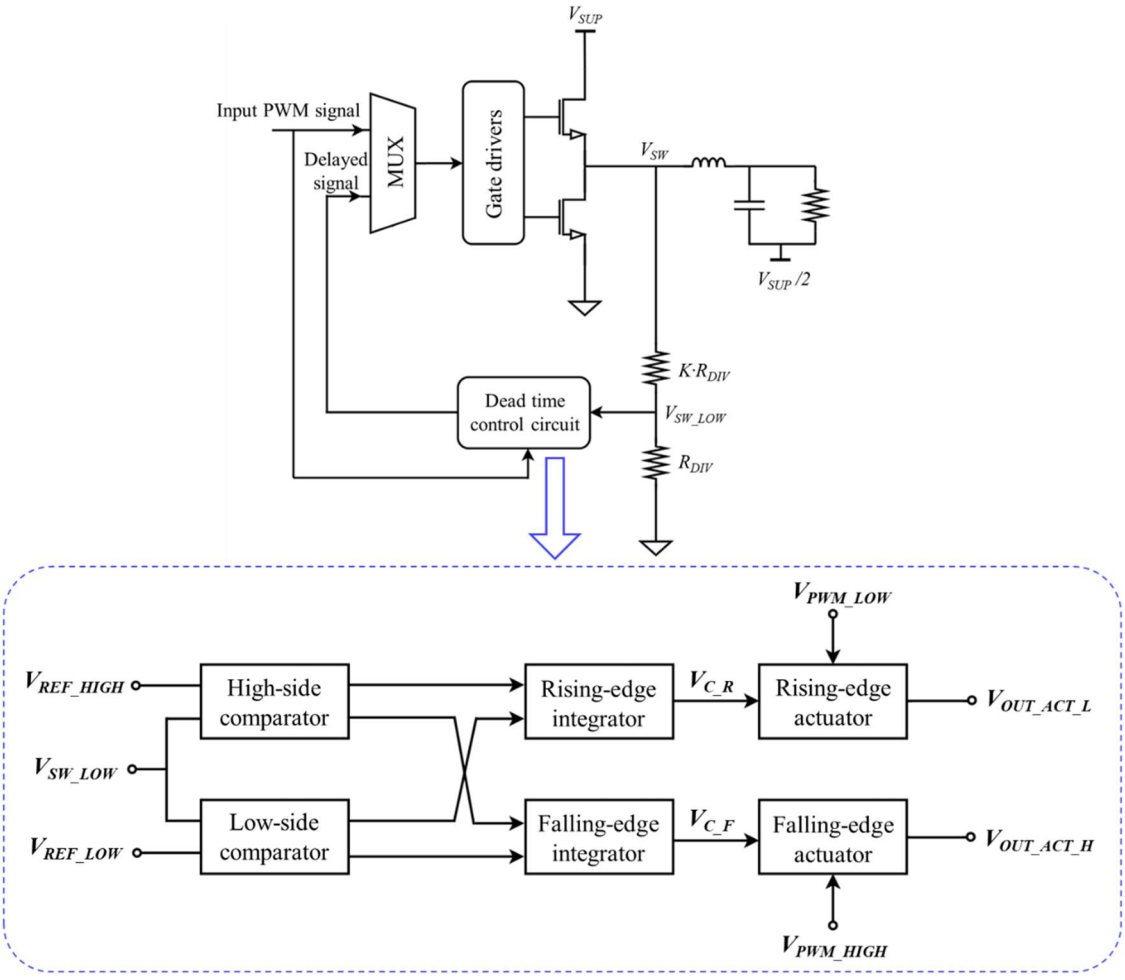


Figure 2.1 Circuit structure of the proposed dead time control circuit

In this thesis, a dead time control circuit is proposed, which is integrated with a half-bridge class D amplifier circuit, as Figure 2.1 shows. The function of the proposed dead time control circuit is to modulate the dead time at V_{SW} by modulating the dead time of the input PWM signals, as Figure 2.2 shows. A feedback loop needs to be involved to reduce the dead time from a large default value (20 ns dead time at the input PWM signals) to a small stable value.

For class-D amplifiers, the input signal varies over time, which means the duty cycle of the PWM signal varies all the time. To achieve dead time control in class D amplifiers, the feedback loop collects information at the switching node V_{SW} and modulates the dead time cycle by cycle. That is, collecting dead time information of one period and making adjustments in the next period.

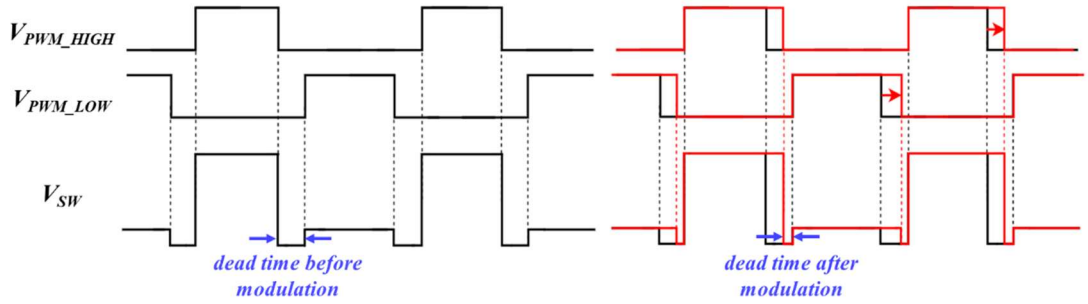


Figure 2.2 Dead time before (black curves) and after (red curves) modulation

The proposed dead time control circuit consists of three blocks: a comparator, an integrator and an actuator. The basic operation principle of the dead time control circuit is as follows:

- The inputs of the dead time control circuit are V_{SW_LOW}, V_{REF_LOW}, V_{REF_HIGH}, V_{PWM_LOW} and V_{PWM_HIGH}. V_{SW_LOW} is an attenuated version of V_{SW}, which is the input of the comparator and is the output of a voltage divider converting V_{SW} to a signal in the low-voltage domain. V_{REF_LOW} and V_{REF_HIGH} are comparators' reference voltages. V_{PWM_LOW} and V_{PWM_HIGH} are the two inversed PWM input signals to control low-side and high-side power transistors. The outputs of the dead time control circuit are $V_{OUT\_ACT\_L}$ and $V_{OUT\_ACT\_H}$, they are PWM signals with modulated falling edges.
- The comparator generates pulses during dead time. There are two comparators in parallel to cover all the output current conditions. If the output current flows out of V_{SW}, during dead time, V_{SW_LOW} goes below the low reference voltage V_{REF_LOW}, so

the low-side comparator generates pulses during dead time, as Figure 2.3 shows; if the output current flows into V_{SW}, the high-side comparator generates pulses. For each comparator, the two outputs separate pulses from rising edges and falling edges.

- The integrator is used to convert the information from the comparator to an output control voltage V_C. The integrator integrates pulses from the comparator. That is, during dead time, the output of the comparator is high and V_C increases. For the rest of the time, V_C always decreases. Therefore, the integrator needs to have two different time constants for both charge and discharge. There are two integrators in parallel. One is used to integrate pulses from rising edges while the other one is used for falling edges.

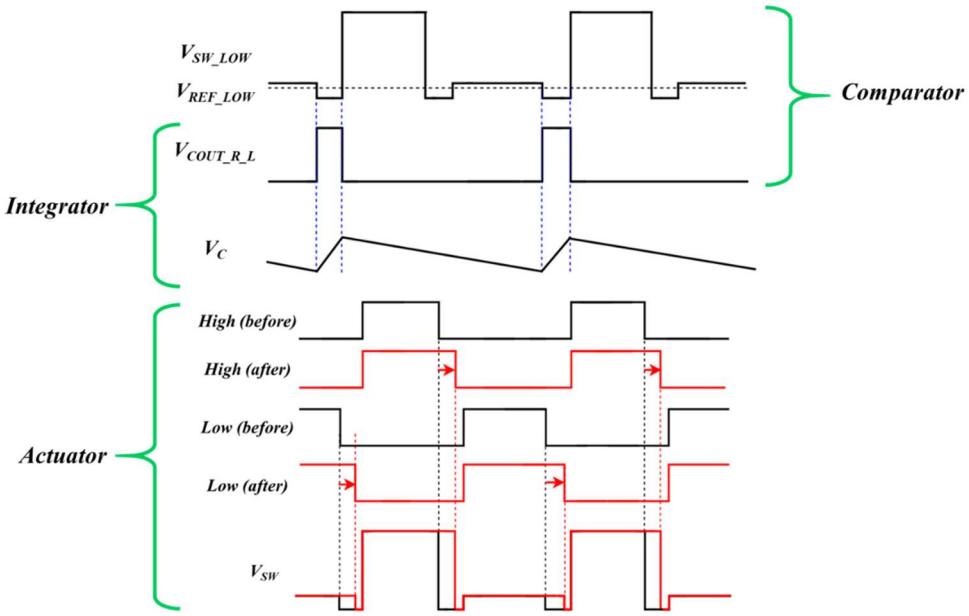


Figure 2.3 Operation principle of the comparator, integrator, and actuator

- The actuator is a voltage-controlled delay time generation circuit. It adds a delay time to the falling edge of the input signal. The delay time is positively related to the voltage V_C. That is, higher V_C corresponds to longer delay time, and thus smaller dead time.

From the above analysis, the proposed dead time control circuit is not a “real-time” system. If the comparator gives a sign telling that the dead time is too large at a certain time, despite real-time adjustment of V_C, adjustment of the input signal happens at the next period.

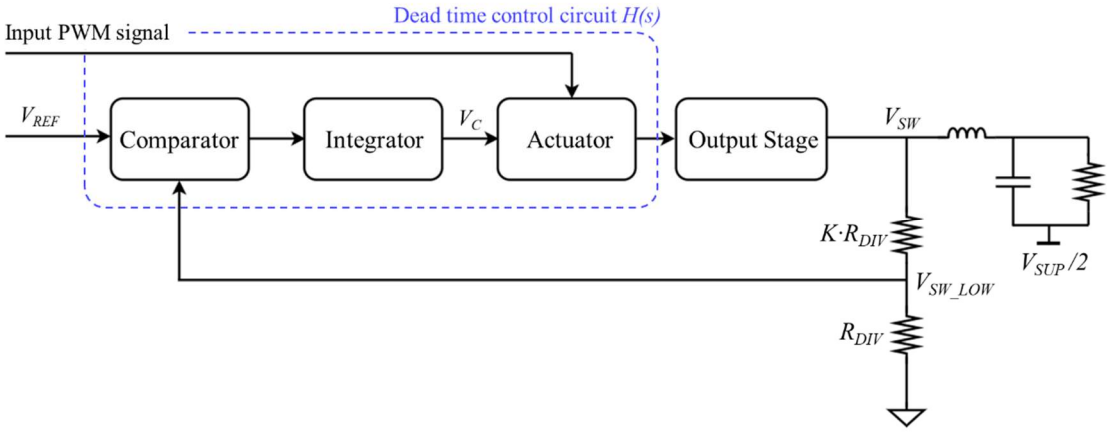


Figure 2.4 Block diagram of the dead time control circuit

The block diagram of the dead time control circuit is shown in Figure 2.4. The transfer function of each block can be calculated as follows.

- The transfer function of the comparator is calculated as Figure 2.5 shows. The input of the comparator is the voltage difference between V_{SW} and the reference voltage. So it can be seen that the input pulse width is equal to the length of the dead time. With the ideal comparator, it generates pulses during dead time. So the output pulse width is equal to the input pulse width and the transfer function of the comparator is ideally 1.

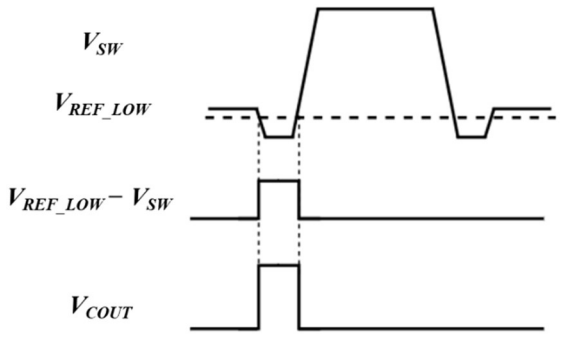


Figure 2.5 Transfer function of the comparator (input: V_{REF_LOW}-V_{SW}; output: V_{COUT})

- For the integrator, it integrates pulses from the comparator during dead time, and keeps decreasing for the rest of the period. The integrator transfers the pulse width t_{dead} to the voltage V_C with two steps. The input pulse width first modulates the current in a resistor. And then a capacitor C_{INT} is needed to convert the current to the voltage. Assume the current in the resistor is a constant value I_R and only flows during the

dead time, $I_R = C_{INT}\frac{dV}{dt}$. So the increase in V_C is $\Delta V_C = t_{dead}\frac{I_R}{C_{INT}}$. To make the circuit converge to a state with residual dead time t_{res} = 5 ns, the increase of V_C is equal to the decrease of V_C, which is $\Delta V_{C0} = t_{res}\frac{I_R}{C_{INT}}$. Since the decrease of V_C happens for the whole period, and the decrease speed of V_C is constant (also defined by a resistor), the decrease of V_C for one period is constant all the time and is equal to ΔV_{C0}.

- For the actuator, it provides a delay time at the falling edge $T_{d,falling}$ for every period. For simplicity, the delay time is linear with the input voltage V_C. Since V_C is changing all the time, for simplicity, V_C is sampled once for one period with the value which is used for the actuator. So it can be expressed as $\frac{T_{d,falling}}{V_C} = K\ (s/V)$.

In the following sections, each block is designed at the system level to illustrate the operation principle of the dead time control circuit in detail.

2.2 Comparator

As mentioned in Section 2.1, the comparator generates pulses during the dead time, indicating that the dead time is too large and needs to be reduced in the next period. During the dead time, the voltage of the switching node V_{SW} is determined by the direction and the value of the output current. To take all current conditions into consideration, two comparators are needed as explained below.

Figure 2.6 shows the design of the low-side comparator used for the case when the output current flows out of the switching node. The operating principle of the comparator is as follows.

- The two inputs of the comparator are V_{SW_LOW} and a reference voltage V_{REF_LOW}. V_{SW_LOW} is explained in Section 2.1. The reference voltage V_{REF_LOW} is from off-chip and is adjustable. V_{REF_LOW} is set to distinguish the negative V_{DS} of the low-side power transistor due to dead time. When the low-side power transistor is ON, V_{SW} is low with the value $-I_{out} \cdot R_{on}$ (R_{on} is the on-resistance of the power transistor). If the voltage divider reduces the value by K times, to generate pulses during dead time, the value of V_{REF_LOW} should be smaller than $-\frac{1}{K} \cdot I_{out} \cdot R_{on}$.

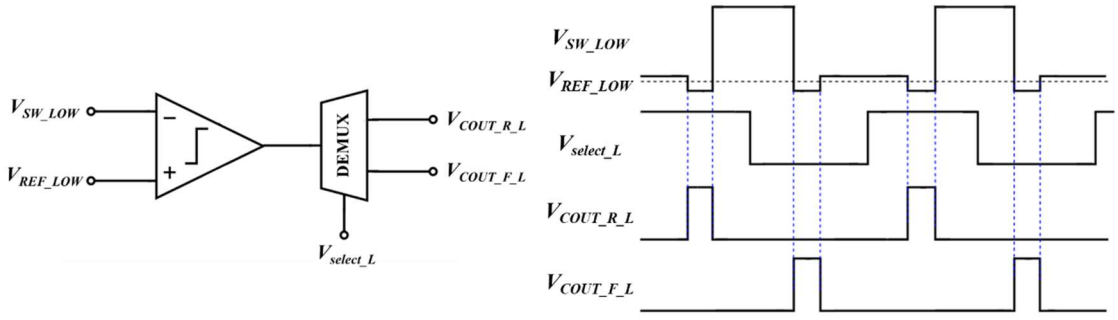


Figure 2.6 Low-side comparator

- The comparator compares V_{SW_LOW} with V_{REF_LOW} and generates pulses during dead time. A demultiplexer is connected to the output as a pulse selector. The select signal V_{select_L} switches at the middle of V_{SW}, so that one output signal $V_{COUT\_R\_L}$ contains the pulses generated at the rising edge of V_{SW}, while the other output $V_{COUT\_F\_L}$ contains the pulses generated at the falling edge of V_{SW}, as Figure 2.6 shows.
- The high-side comparator generates pulses when the output current flows into the switching node. The working principle of the high-side comparator is almost the same as the low-side comparator, as Figure 2.7 shows, except that V_{SW_LOW} is compared with a high reference voltage V_{REF_HIGH} in this case, which is also from external and is adjustable. V_{REF_HIGH} is set to distinguish the negative V_{DS} of the high-side power transistor due to dead time. Since V_{SW} is $I_{out} \cdot R_{on} + V_{SUP}$ when the high-side power transistor is ON, V_{REF_HIGH} should be higher than $\frac{1}{K}(I_{out} \cdot R_{on} + V_{SUP})$.

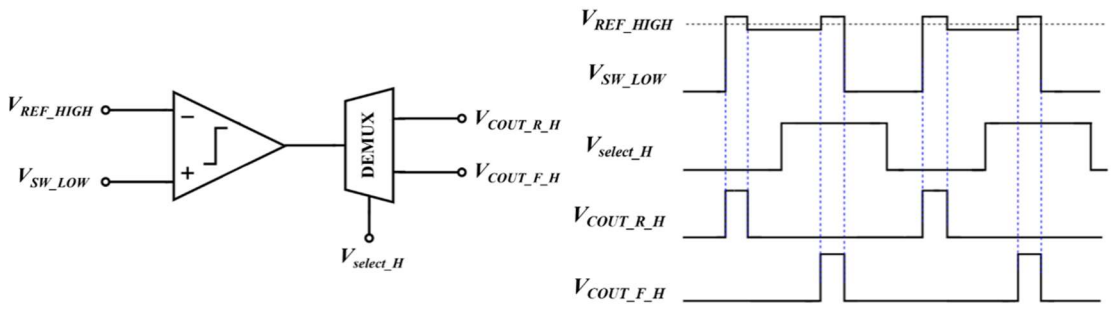


Figure 2.7 High-side comparator

For the class D amplifier with 85 V supply voltage and 100 mΩ power transistor on-resistance, if K is chosen to be 44 and the maximum current is lower than 10 A. V_{REF_LOW} should be lower than -22.2 mV, while V_{REF_HIGH} should be higher than 1.91 V.

From the above analysis, the requirements of the comparator are as follows.

- The input common-mode range of the comparator should be larger than -30 mV to 2 V. As analyzed before, the comparator needs to compare V_{SW_LOW} with both high and low reference voltages.
- The input-referred offset of the comparator should be low. When V_{SW} is reduced to V_{SW_LOW}, the V_{DS} of the power transistor during dead time is also reduced by K times. For example, if V_{DS} is -4 V and K is 40, then after the voltage divider, the difference between the two inputs of the comparator is 100 mV. To make the input-referred offset 10 times lower than this value, it cannot exceed 10 mV. On the other hand, the mismatch in GaN technology can reach hundreds of millivolts, which is very large compared with the desired offset. To achieve this goal, auto-zeroing can be used for the comparator.
- The comparator needs to have a large amplification to convert the small difference at the input to digital levels at the output. If the difference between the two inputs is assumed to be 100 mV, as analyzed above, to make the output reach V_{DD}, which is 6.3 V, the amplification cannot be lower than 63.
- The comparator needs to be able to handle 5 ns pulses, which corresponds to a desired bandwidth of 200 MHz. As mentioned in Section 1.5, the goal of the dead time control circuit is to reduce the dead time to 5 ns.

2.3 Integrator

2.3.1 Integrator Circuit Topology and Analysis

The function of the integrator is to generate a control voltage V_C according to the information from the comparator. During dead time, V_C gets higher because the integrator integrates pulses from comparators. For the rest time of the period, V_C is continuously decreased.

An integrator is a good candidate to realize the function mentioned above. Figure 2.8 shows a typical integrator.

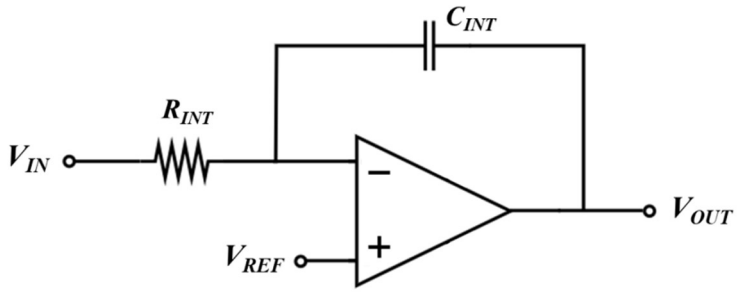


Figure 2.8 Typical integrator circuit topology

The ideal integrator has only one time constant: $\tau = R_{INT}C_{INT}$. However, according to the function of the integrator analyzed above, the integrator needs to have two different time constant values for charge and discharge. Furthermore, since the integrator is inverting, during dead time, V_{IN} needs to be connected to a low voltage to increase V_{OUT}; and when V_{IN} is connected to a high voltage, V_{OUT} will be decreased. Therefore, an integrator circuit is proposed in Figure 2.9. The operation principle is as follows.

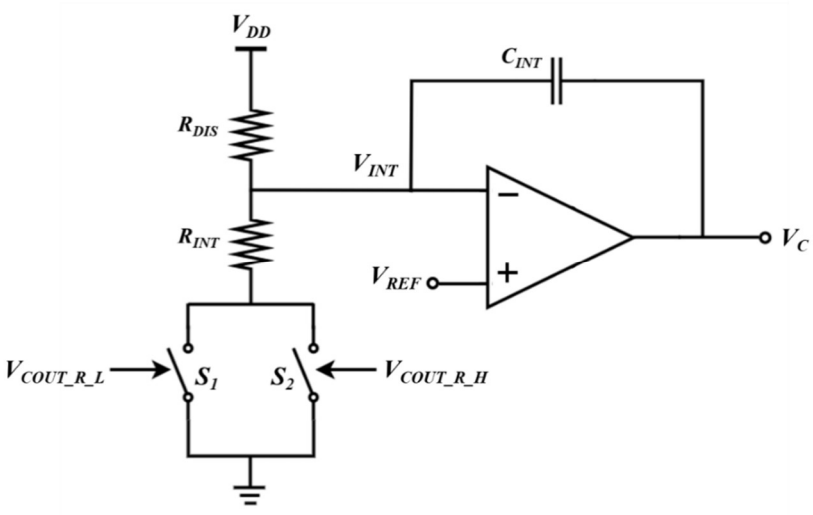


Figure 2.9 Proposed integrator circuit topology

- Switches S_1 and S_2 are controlled by the two outputs of the comparators. When there are no pulses from comparators, the two switches are both open, and no current flows through resistor R_{INT}. With an ideal amplifier, $V_{INT} = V_{REF}$, and the current flows in

the resistor R_{DIS} is equal to the current flowing through the capacitor C_{INT}. That is, $\frac{V_{DD}-V_{INT}}{R_{DIS}} = C_{INT}\frac{d(V_{INT}-V_C)}{dt}$. By solving the differential equation we can get the result:

$$V_C(t) = V_{C0} - \frac{V_{DD} - V_{REF}}{R_{DIS}C_{INT}}t \qquad (2.1)$$

, where V_{C0} is the initial voltage. Therefore, the capacitor is discharged by the resistor R_{DIS} and V_C is decreased when switches S_1 and S_2 are both open.

- During the dead time, one of the switches S_1 and S_2 are closed, and current flows through the resistor R_{INT}. If R_{INT} is much smaller than R_{DIS}, the current flowing in R_{INT} is $\frac{V_{INT}}{R_{INT}}$, which is approximately equal to the current flowing through C_{INT}: $C_{INT}\frac{d(V_{INT}-V_C)}{dt}$. By solving the differential equation $\frac{-V_{INT}}{R_{INT}} = C_{INT}\frac{d(V_{INT}-V_C)}{dt}$, we can get the results:

$$V_C(t) = V_{C0} + \frac{V_{REF}}{R_{INT}C_{INT}}t \qquad (2.2)$$

, where V_{C0} is the initial voltage. Therefore, the capacitor is charged and V_C is increased when one of the switches S_1 and S_2 are closed, so that pulses from comparators are integrated.

2.3.2 Residual Dead Time and the Choice of Reference Voltage

With the proposed integrator circuit, there is always a residual dead time. Considering a circuit starting with a large dead time, the dead time is first reduced as the increase of V_C. Then when the increase of V_C is equal to the decrease of V_C within one period (as Figure 2.10 shows), the circuit reaches a steady state, a small residual dead time remains and comparators still generate pulses during dead time. The existence of residual dead time can prevent the circuit from shoot-through.

The expression of the residual dead time t_{res} can be derived from Equations 2.1 and 2.2:

$$t_{res} = \frac{R_{INT}}{R_{DIS}}(\frac{V_{DD}}{V_{REF}} - 1)T \qquad (2.3)$$

From the above equation, the residual dead time decreases as the increase of the reference voltage V_{REF} (V_{REF} cannot be higher than V_{DD}), if the resistance of R_{INT} and R_{DIS} is fixed.

In order to make the residual dead time adjustable, the reference voltage is from off-chip, which is also adjustable.

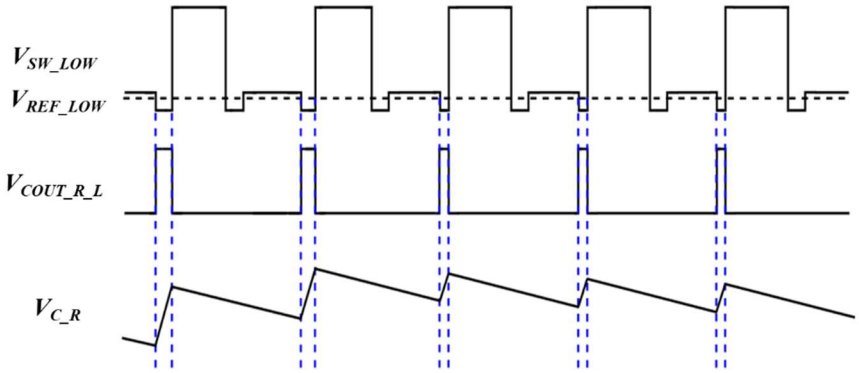


Figure 2.10 V_C is settled with a residual dead time

If the reference voltage is chosen to be $V_{DD}/2$ to achieve 5 ns residual dead time, then it can be calculated that $\frac{R_{INT}}{R_{DIS}} = \frac{1}{100}$, given the period T = 500 ns.

2.3.3 Requirements of the Integrator

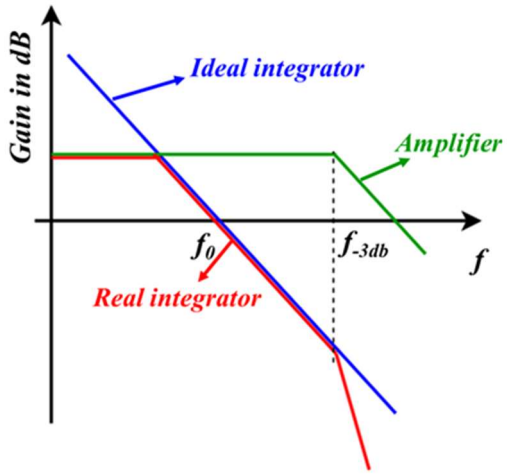


Figure 2.11 Bode plot of a real integrator

Because of the finite gain and bandwidth of the differential amplifier, the bode plot of a real integrator is shown in Figure 2.11. The gain of the amplifier is chosen to be 20 dB for simplicity (which can be achieved by one-stage amplifier). From theoretical analysis, the expected residual dead time is increased from 5 ns to 6.1 ns if V_C is settled to $V_{DD}/2$, because of the limited gain of the amplifier. In order to catch up with the audio signal

whose frequency is 20-20 kHz, f_{INT} should be at least 20 kHz, so that the unity gain frequency of the integrator f_0 is 200 kHz. To get >60° phase margin, the bandwidth of the amplifier should be at least 1.73 times larger than f_0, which is 346 kHz.

With the integrator proposed in Figure 2.9, it can be deduced that the formula of f_0 is:

$$f_0 = \frac{1}{4\pi R_{INT} C_{INT}} \qquad (2.4)$$

The derivation of the formula is presented in Appendix. The basic idea is as follows. Equation 2.3 can also be written as $V_{INT} = \frac{R_{INT}/D}{R_{DIS}+R_{INT}/D} V_{DD}$, where $D = t_{res}/T$ is the duty cycle. So R_{INT} is a duty-cycled resistor with equivalent resistance R_{INT}/D. The change in the input pulse width leads to the change in the equivalent resistance and thus the change of the output.

Another requirement for the integrator is that the amplifier should have a low input-referred offset. With a real amplifier, the expression of the residual dead time is:

$$t_{res} = \frac{R_{INT}}{R_{DIS}} (\frac{V_{DD}}{V_{INT}} - 1)T \qquad (2.5)$$

Due to offset, V_{INT} deviates from V_{REF}, resulting deviation of t_{res}. Despite of compensation by adjusting V_{REF}, several hundreds of millivolts input-referred offset is still not acceptable and is better to be compensated. By reducing the offset from 300 mV to 50 mV, the theoretical residual dead time can be reduced from 6.05 ns to 5.16 ns. Smaller error can be achieved by reducing the offset within 50 mV. So it is better to involve auto-zeroing technology.

2.4 Actuator

The function of the actuator is to add a delay time to the falling edge of the input PWM signal. As mentioned in Section 2.1, the delay time should be positively correlated to the input control voltage V_C.

Figure 2.12 shows the structure of a kind of actuator, which is based on the pulse-width adjustment circuit proposed in [1]. The operation principle of the actuator is as follows.

- At the rising edge of the *ON* signal, switch S_1 is closed and S_2 is open, the capacitor C_{ACT} gets charged and V_{CA} rises quickly. When V_{CA} goes higher than the threshold voltage of the first inverter $V_{TH,INV}$, the output voltage V_{OA} also flips from low to high.

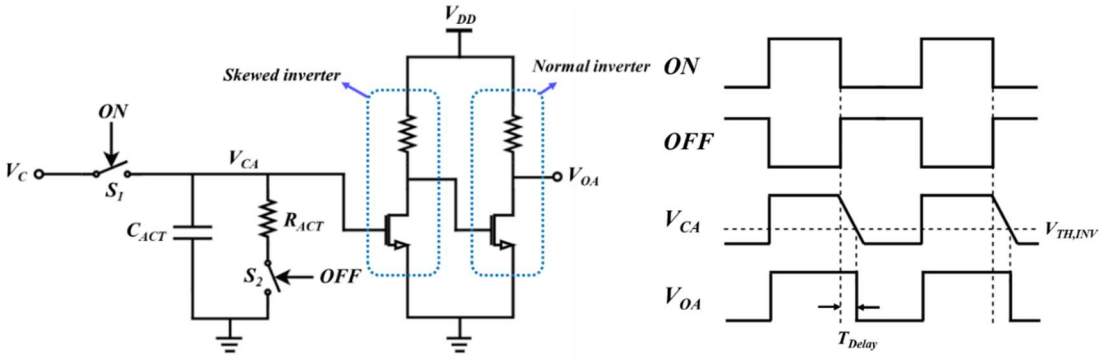


Figure 2.12 Actuator circuit topology

- The capacitor C_{ACT} starts to be discharged slowly at the rising edge of the *OFF* signal, at which time switch S_1 is open and S_2 is closed. The discharge speed is mainly determined by the resistor R_{ACT}. After V_{CA} is discharged to a value lower than $V_{TH,INV}$, V_{OA} goes low. As a result, V_{OA} follows the *ON* signal, except that a delay time is induced at the falling edge.

For this circuit, V_C cannot be lower than $V_{TH,INV}$, otherwise the output voltage V_{OA} will not flip. Since V_C cannot go higher than V_{DD}, the adjustment range of V_C is $V_{TH,INV} < V_C < V_{DD}$. To get a large adjustment range of V_C, the first inverter connected to C_{ACT} in Figure 2.12 is desired to be a skewed inverter with low inverter threshold voltage $V_{TH,INV}$. $V_{TH,INV}$ is designed to be the threshold voltage of a GaN transistor, which is around 2 V for typical corner.

For the circuit in Figure 2.12, when V_C is lower than $V_{TH,INV}$, output voltage V_{OA} will not switch. However, it is supposed that the output voltage follows the input voltage in this case. To overcome this problem, a logic circuit is added after V_{OA}, as Figure 2.13 shows. The function is to make the rising edge of the output signal follow the rising edge of the input signal, and is independent of the *ON* and *OFF* signals. As a result, the actuator only alters the falling edge of the input PWM signal. In this circuit, the falling edge of the *IN_PWM* signal is required to be aligned with the rising edge of the *OFF* signal. And the falling edge of the *OFF* signal (the rising edge of the *ON* signal) can be anywhere in one period.

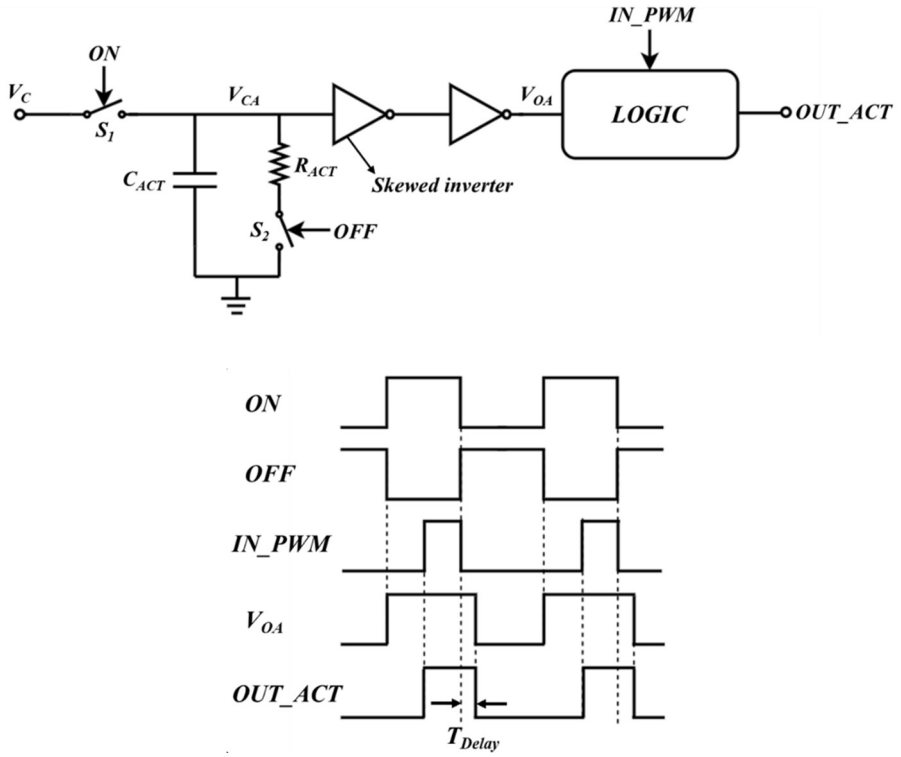


Figure 2.13 Proposed actuator circuit topology which only alters the falling edge of the input signal

As the delay time at the falling edge $T_{d,falling}$ is expected to be positively correlated with V_C, the maximum value is achieved when V_C is equal to V_{DD}, and the range of $T_{d,falling}$ is $0 < T_{d,falling} < T_{d,falling}$ (V_{DD}), which is also the adjustment range of the dead time. This range should be large enough to compensate for the dead time.

To conclude, the requirements of the actuator are as follows.

- $V_{TH,INV}$ of the skewed inverter should be designed ~2 V for the typical corner. No special requirements for other logic gates, so the threshold voltage is designed to be $V_{DD}/2$, which is 3 V for typical corner.
- $T_{d,falling}$ (V_{DD}) should be larger than the default dead time at the switching node for all the process corners and temperatures.

2.5 Conclusion

In conclusion, the proposed dead time control system can reduce the default large dead time. It consists of three blocks: the comparator, the integrator and the actuator. The comparators generate pulses during dead time. The integrators make adjustments

according to the pulses from comparators and provide a control voltage V_C to the actuator, which determines the delay time added to the falling edge of the input signal. After the dead time modulation, a residual dead time always exists and is adjustable, due to the structure of the integrator.

The specific requirements of each block are discussed in this section, and in the next chapter, each block is designed at the transistor level to fulfill the requirements.

Reference

[1] W.-H. Sun, S.-H. Chien, and T.-H. Kuo, "A 121dB DR, 0.0017% THD+N, 8× Jitter-Effect Reduction Digital-Input Class-D Audio Amplifier with Supply-Voltage-Scaling Volume Control and Series-Connected DSM," presented at the 2022 IEEE International Solid-State Circuits Conference (ISSCC), 2022.

Chapter 3 Dead Time Control Circuit Transistor-level Design

In Chapter 2, the system-level design of the circuit is discussed. According to the requirements of each block, in the chapter, the transistor-level design of the circuit is demonstrated. Sections 3.1 to 3.3 present the design of the comparator, integrator and actuator separately.

3.1 Comparator Simulation Results

In Section 2.2, the operation principle and the requirements of the comparator are demonstrated. In this section, the simulation results of the comparator are presented. The design of the comparator is originally from other's work.

The circuit structure is shown in Figure 3.1. In order to get a small offset and large amplification, the comparator is designed to be a two-stage auto-zeroing comparator. To handle -30 mV to 2 V common-mode input voltage, the ground of the first stage is connected to V_{EE}, which is -6.3 V.

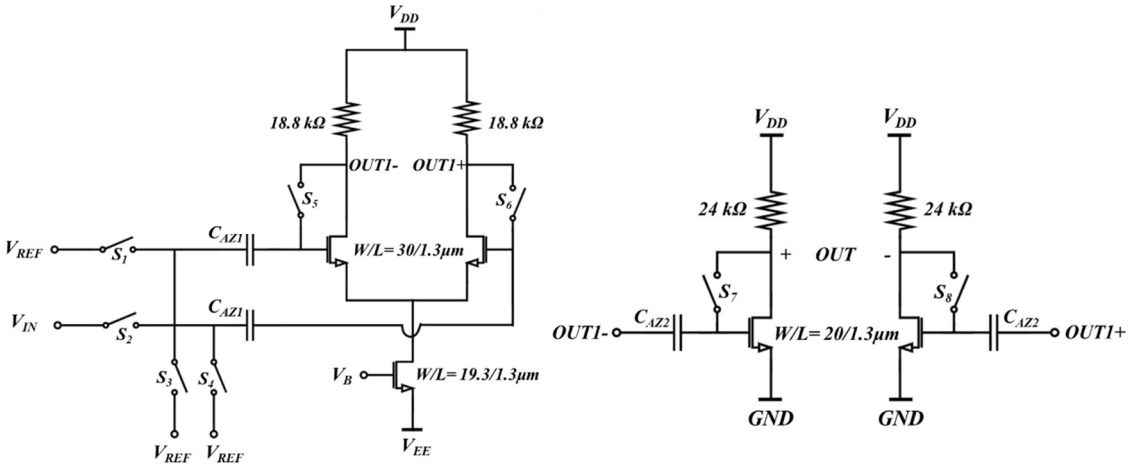


Figure 3.1 Implementation of the comparator

By running 100 Monte Carlo simulations, the input-referred offset of the comparator is listed in Table 3.1. After applying auto-zeroing, the standard deviation of the input offset is reduced from 253.0 mV to 2.8 mV at room temperature. The offset is small enough to

sense the voltage difference at the input of the comparator. The gain of the comparator is larger than the desired value for both 0 V and 2 V common-mode inputs.

Table 3.1 Monte Carlo simulation results of the comparator

		25 ℃		100 ℃	
		μ	σ	μ	σ
Input-referred Offset	No AZ	4.06 mV	253.0 mV	4.10 mV	252.9 mV
	With AZ	0.86 mV	2.8 mV	1.3 mV	2.7 mV
Gain	V_{CM} = 0 V	82.7	7.3	86.3	8.3
	V_{CM} = 2 V	83.2	7.2	86.8	8.2

Table 3.2 lists the simulation results of the bandwidth of the comparator for different corners and temperatures. Due to the auto-zeroing structure, the bandwidth is simulated with the two stages separately and added manually. It can be discovered that the bandwidth is lower than the requirement, which results in the deviation of the residual dead time and is going to be discussed in Section 4.5.

Table 3.2 Bandwidth of the comparator

	Bandwidth (MHz)
Typical corner, 25℃	148.5
Typical corner, 100℃	91.4
Slow corner, 25℃	112.4
Slow corner, 100℃	68.1
Fast corner, 25℃	219.6
Fast corner, 100℃	136.8

3.2 Integrator Design

This section will focus on the design of the integrator. The architecture of the integrator is proposed in Section 2.3.1. In this section, the specific implementation of the integrator is presented, which includes the following aspects.

- The implementation of the switches.
- The sizing of the resistors and the capacitor.
- The implementation of the differential amplifier.

3.2.1 Implementation of Switches

The two switches S_1 and S_2 in Figure 2.9 are implemented by transistors, as Figure 3.2 shows.

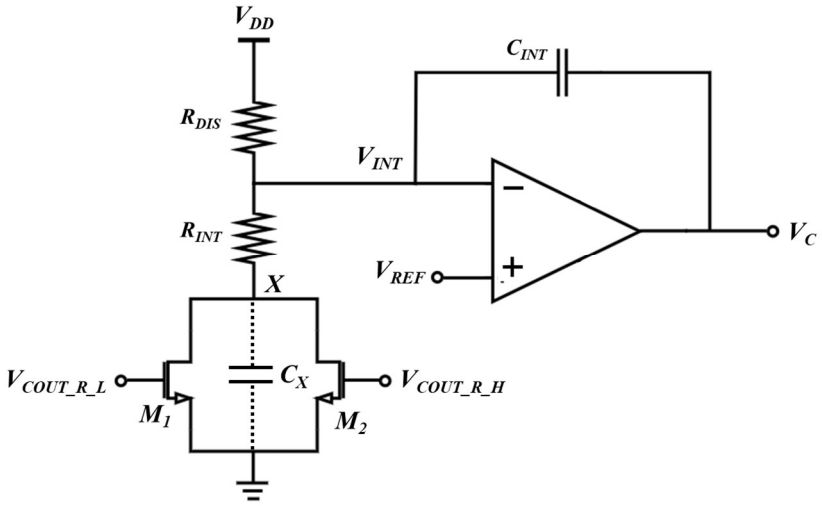


Figure 3.2 Integrator with switches implemented by transistors

This implementation introduces non-ideality to the circuit due to the parasitic capacitance at the drain of the transistor. If switches S_1 and S_2 are ideal, they can be turned on and off immediately. Considering the circuit is in a steady state with a small residual dead time, in one period, the charges through R_{DIS} should be equal to the charges through R_{INT} during dead time. That is, $Q_{R_{DIS}} = I_{R_{DIS}} \cdot T = \frac{V_{DD}-V_{REF}}{R_{DIS}} T = Q_{R_{INT}} = I_{R_{INT}} \cdot t_{res} = \frac{V_{REF}}{R_{DIS}} t_{res,i}$, where $t_{re\ ,i}$ is the ideal residual dead time.

However, when the switches are implemented by transistors, parasitic capacitance is induced in node X in Figure 3.2 (denoted as C_X). When one of the transistors is turning off, the current flowing in R_{INT} cannot be reduced to 0 immediately, since C_X needs to be charged up. So the expression of $Q_{R_{INT}}$ is changed into: $Q_{R_{INT}} = I_{R_{INT}} \cdot t_{res} + Q_{C_X} = \frac{V_{REF}}{R_{DIS}} t_{res,r} + Q_{C_X}$, where $t_{res,r}$ is the real residual dead time and Q_{C_X} is the amount of charge to charge up the parasitic capacitance at node X.

Since $Q_{R_{DIS}}$ is the same and not affected by the implementation of the switches, $t_{res,r}$ is smaller than $t_{res,i}$. And to minimize this effect, the size of the transistors should be as small as possible to minimize C_X, so that Q_{C_X} is also minimized. As a result, the size of the two transistors M_1 and M_2 are the minimum size with W = 2 μm and L = 1.3 μm. With this size, Q_{C_X} is 0.18 pC, and $Q_{R_{INT}}$ is 1.12 pC, which is around 6 times larger than Q_{C_X}, assuming V_{REF} is $V_{DD}/2$. If the size of transistors is increased by 5 times, then the residual dead time is reduced from 5.0 ns to only 1.5 ns, since Q_{C_X} takes a large part of $Q_{R_{INT}}$.

3.2.2 Resistor and Capacitor Sizing

Besides the non-ideality discussed in Section 2.3.4, the implementation of switches also causes another non-ideality due to the on-resistance of transistors R_{on}.

If R_{on} is taken into consideration, while charging the capacitor, resistor R_{INT} is actually $R_{INT} + R_{on}$. Therefore, the residual dead time is:

$$t_{res} = \frac{R_{INT} + R_{on}}{R_{DIS}} \left(\frac{V_{DD}}{V_{REF}} - 1\right) T \qquad (2.4)$$

From the above equation, for a fixed reference voltage, the real residual dead time is a bit larger than the calculation result. To minimize this effect, R_{INT} should be dominant over R_{on}. For transistors with the smallest size, R_{on} is around 1.6 kΩ when the transistor operates in the deep triode region. So R_{INT} is chosen to be 10 times larger than R_{on}, which is 16 kΩ. As calculated in Section 2.3.3, R_{DIS} should be 100 times larger than R_{INT}, which is 1.6 MΩ.

From Equation 2.4, the integrated capacitor C_{INT} is calculated to be 25 pF. In the design, C_{INT} is finally chosen to be 15 pF and the unity gain frequency of the comparator is adjusted to 332 kHz because of the following considerations.

- The size of the capacitor with 25 pF is 304 μm×304 μm, which is 1.7 times larger than the size of the capacitor with 15 pF. By reducing the size of the capacitor, the area can be effectively saved, regarding the situation that two capacitors are needed for the rising edge and falling edge integrators and the chip area is limited.
- In order to make V_C not be disturbed too much when charges are shared between C_{INT} and C_{ACT}, the capacitance of C_{INT} should be much larger than the capacitance of the capacitor in the actuator C_{ACT}. As C_{ACT} is 1 pF, this requirement can still be satisfied after reducing the size of C_{INT}. Further explanations will be given in Section 3.3.3.

Since the minimum value of f_0 is 200 kHz, f_0 = 332 kHz is also acceptable. And f_{-3dB} should be 1.73 times larger than f_0, which is now 575 kHz.

3.2.3 Differential Amplifier Implementation

As analyzed in Section 2.3.3, to achieve low input-referred offset, the differential amplifier is designed to be an auto-zero OTA (AZ OTA), as Figure 3.3 shows. The operation principle of the AZ OTA is as follows.

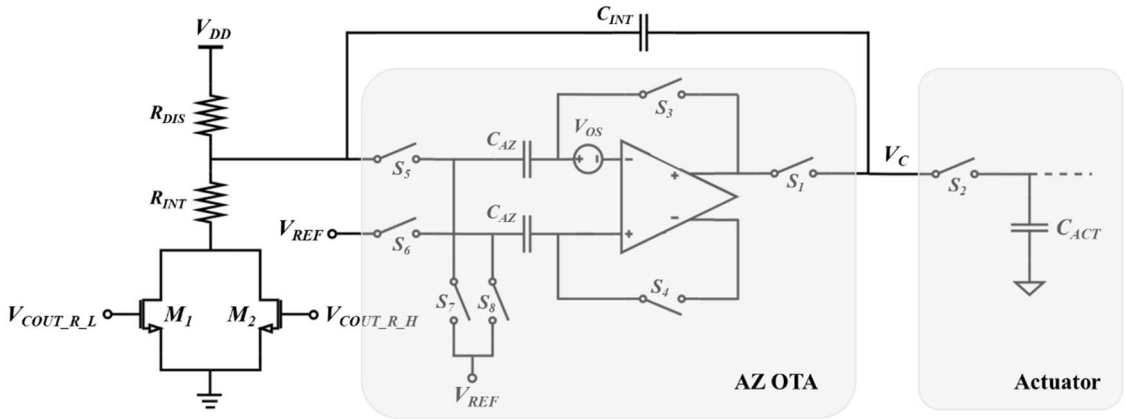


Figure 3.3 An AZ OTA is used to implement the differential amplifier

- For every period, there are two working phases: the auto-zeroing phase and the sensing phase.
- During auto-zeroing phase, switch S_3, S_4, S_7, S_8 are closed, switch S_5, S_6, S_1 are open. The inputs of the OTA are shorted to the outputs, and the input-referred offset is sampled on the input capacitors C_{AZ}.
- During sensing phase, switch S_5, S_6, S_1 are closed, switch S_3, S_4, S_7, S_8 are open. Since capacitors C_{AZ} holds the voltage, so the input of OTA can be compensated and get rid of the offset.

The signal to control auto-zeroing is designed as Figure 3.4 shows. Taking the rising edge as an example, V_{AZ_R} is the signal to enable auto-zeroing, and its inverted signal is used to enable the sensing phase. V_{AZ_R} is generated by V_{MTM_R} ***AND*** V_{HS_OFF}, where V_{MTM_R} is the middle-to-middle signal with transitions at the middle of V_{SW}, and that V_{HS_OFF} is the inverted signal of the high-side PWM signal. The design of the auto-zeroing signal takes advantage of the following aspects.

- The sensing clock is the inverted signal of the auto-zeroing clock. So they can make full use of the whole time of a period.
- In one period, the time for auto-zeroing is always shorter than half of the period since the duty cycle of the V_{MTM} signal is 50%. So the time for sense can be longer, which is desired.
- It guarantees that the OTA is always in the sensing phase when there are pulses from the comparator. The middle-to-middle signal separates the rising edge and falling edge, and AZ only happens in half of the period excluding the desired edge.
- For the extreme case, the time for auto-zeroing phase is 70 ns, which is enough for the input capacitor C_{AZ} to settle. From simulation results, the longest settling time needed is around 50 ns, which is for the slow corner at 100℃.

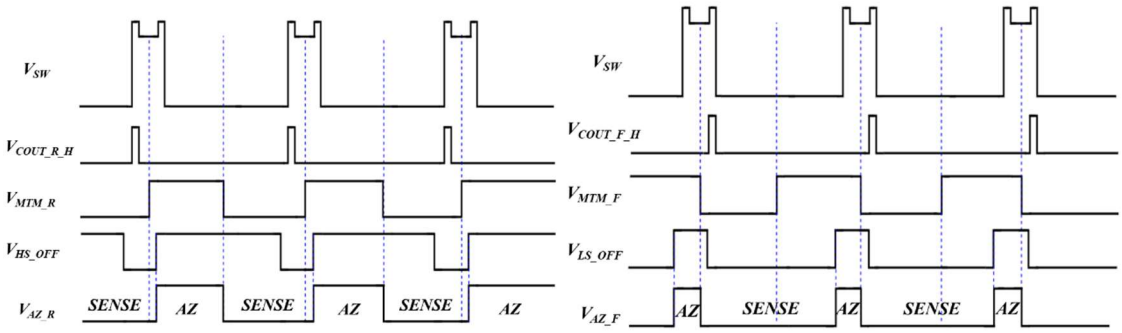


Figure 3.4 Sensing and auto-zeroing clock of AZ OTA for rising edge (left) and falling edge (right)

For the auto-zeroing circuit, switches S_3 to S_8 are all implemented by single transistors for simplicity. Switch S_1 is implemented by a bootstrapped switch, which is going to be discussed in Section 3.3.1.

Table 3.3 Bandwidth and gain of the OTA

	Bandwidth (MHz)	**Gain (dB)**
Typical corner, 25℃	234.7	19.2
Typical corner, 100℃	154.5	25.7
Slow corner, 25℃	183.1	25.8
Slow corner, 100℃	110.8	26.4
Fast corner, 25℃	391.5	23.9
Fast corner, 100℃	245.4	24.3

The design of the OTA is reused from other's work. The bandwidth and the gain of the OTA are listed in Table 3.3. It can be discovered that the gain can achieve the requirement mentioned in Section 2.3.3, and the bandwidth is much larger than the desired value.

3.3 Actuator Design

This section will focus on the design of the actuator. First, the implementation of the actuator is analyzed in Section 3.3.1. In Section 3.3.2, the simulation results of the actuator are shown to prove that the actuator can meet the requirements proposed in Section 2.4. Then in Section 3.3.3, the clock of the actuator is designed, considering the integrator auto-zeroing clock together.

3.3.1 Implementation of the Actuator

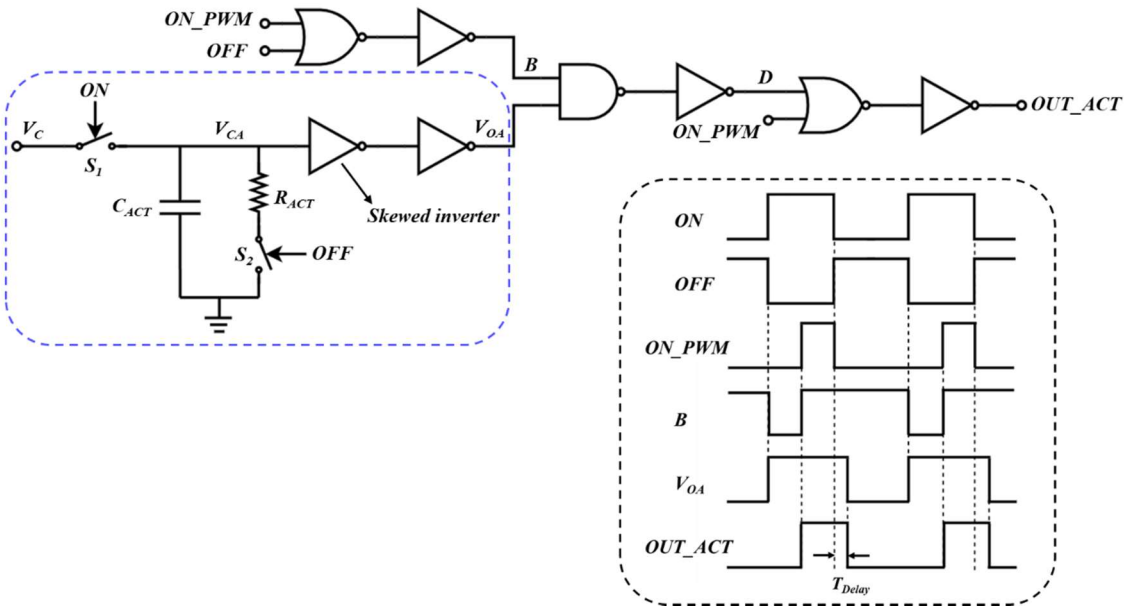


Figure 3.5 Proposed actuator circuit

Figure 3.5 shows the circuit topology of the proposed actuator. In this circuit, switch S_1 is implemented by a bootstrapped switch, so that V_{CA} can follow V_C when V_C varies between $V_{TH,INV}$ and V_{DD}. Switch S_2 is implemented by a transistor with minimum size.

The size of the capacitor C_{ACT} is chosen to be 1 pF. This value should be much smaller than the capacitor in the integrator C_{INT}, which is going to be explained in Section 3.3.3. On the other hand, C_{ACT} cannot be too small considering the parasitic capacitance in the

circuit. The resistor R_{ACT} is chosen to be 18 kΩ. It needs to be dominant over the on-resistance of switch S_2. Also, R_{ACT} controls the discharging speed of C_{ACT} and thus the delay time. By using 18 kΩ R_{ACT}, the largest delay time provided by the actuator is always larger than the default dead time, which is going to be shown in Section 3.3.2.

For the skewed inverter, the threshold voltage $V_{TH,INV}$ is desired to be ~2 V. The size of the resistor is designed to be 20 kΩ and the size of the transistor is W/L = 120µm/1.3µm. Figure 3.6 shows the voltage transfer curve for different corners and temperatures, and Table 3.4 lists the $V_{TH,INV}$.

For all the other logic gates, the size of the resistors is 12 kΩ, and the size of the transistors is W/L = 10µm/1.3µm. The threshold voltage of other inverters in the circuit is around V_{DD}/2 for the typical corner, which is also listed in Table 3.4.

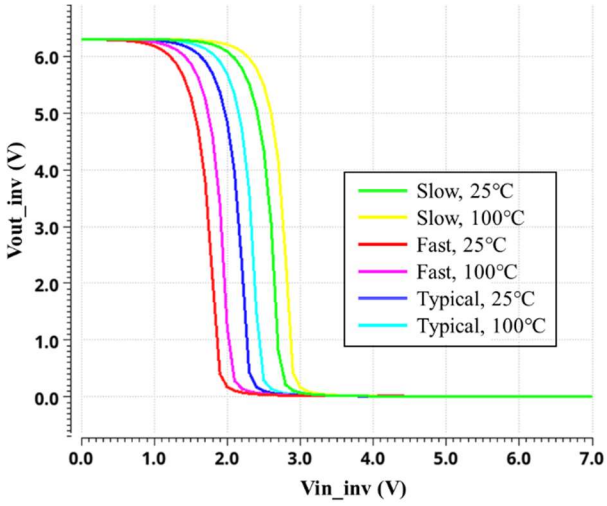


Figure 3.6 Voltage transfer curve of the skewed inverter

Table 3.4 Threshold voltage of skewed inverter and other inverters in the circuit

$V_{TH,INV}$ (V)	Skewed Inverter	Other Inverters
Typical corner, 25°C	2.16	3.07
Typical corner, 100°C	2.33	3.21
Slow corner, 25°C	2.60	3.46
Slow corner, 100°C	2.77	3.62
Fast corner, 25°C	1.75	2.73
Fast corner, 100°C	1.92	2.86

3.3.2 Actuator Simulation Results

A test circuit is built up to simulate the actuator separately. The signals are set as follows. The *ON* and *OFF* signals are inverted with 50% duty cycle. The duty cycle of the *IN_PWM* signal is 15%, which is the -3 dB full-scale signal. The rising edge of the *OFF* signal is aligned with the falling edge of the *IN_PWM* signal. V_C varies from $V_{TH,INV}$ to V_{DD}.

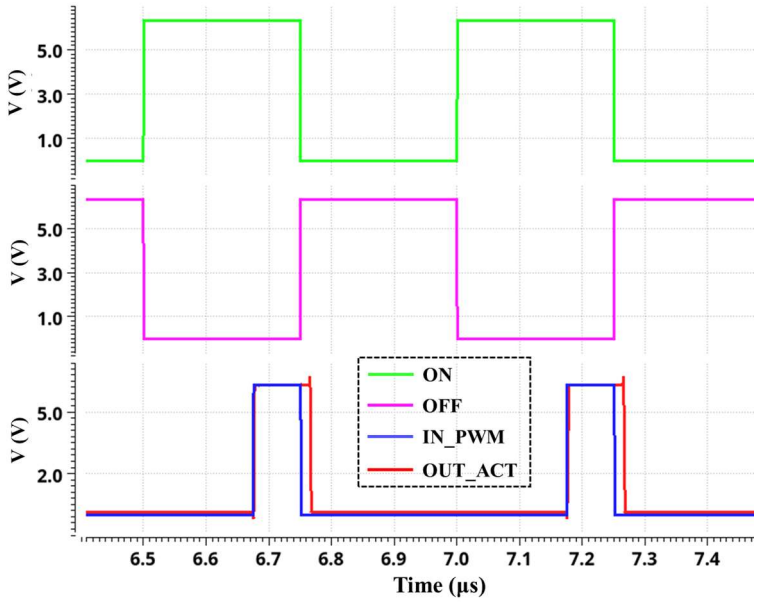


Figure 3.7 Simulation results with the actuator test circuit

Figure 3.7 shows the simulation results. The rising edge of the output signal *OUT_ACT* follows with the rising edge of the input PWM signal *IN_PWM*, and there is a delay time added to the falling edge of *OUT_ACT* compared with *IN_PWM*.

Table 3.5 lists the rising edge delay time $T_{d,rising}$ and falling edge delay time $T_{d,falling}$ between *IN_PWM* and *OUT_ACT* with different V_C values (typical corner, 25℃).

When switch S_1 is open and S_2 is closed, C_{ACT} and R_{ACT} form an RC circuit. It can be derived that the relationship between $T_{d,falling}$ and V_C is:

$$T_{d,falling} = A + B \cdot \ln V_C \qquad (3.1)$$

, where A and B are constants. From the equation, $T_{d,falling}$ is positively correlated with V_C, but not strictly linear with V_C.

Table 3.5 Delay time of rising edge and falling edge of *OUT_ACT* compared with *IN_PWM*, and relative delay time for different V_C values (typical corner, 25℃)

V_C (V)	$T_{d,rising}$ (ns)	$T_{d,falling}$ (ns)	Relative delay (ns)
2.2	0.56	6.00	5.44
3.0		16.39	15.83
3.8		24.38	23.82
4.6		31.23	30.67
5.4		37.08	36.52
6.3		42.74	42.18

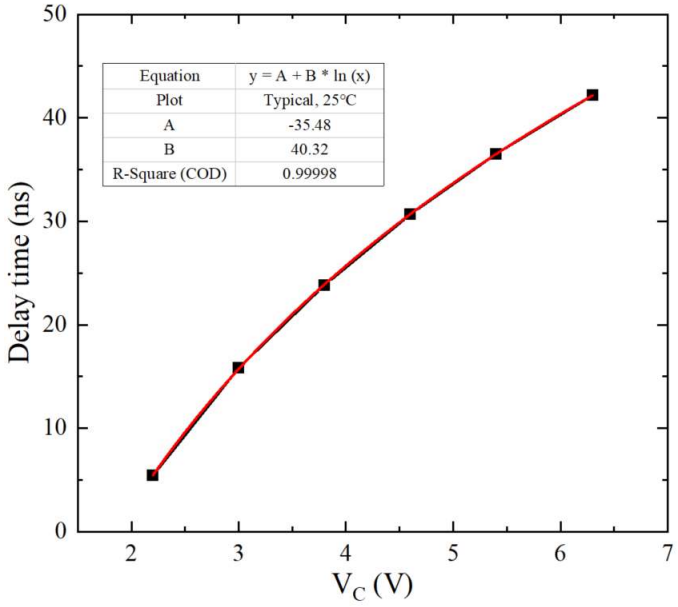


Figure 3.8 $T_{d,falling}$ vs. V_C (black) and logarithm fitting line (red)

Figure 3.8 shows the $T_{d,falling}$ vs. V_C (black line) curve and the logarithm fitting line (red line). The fitting line uses the expression of Equation 3.1. The coefficient of determination R^2 of the logarithm fitting line is around 1, which means perfect fitting.

Figure 3.9 shows the $T_{d,falling}$ vs. V_C for all process corners at 25℃ and 100℃. Table 3.6 lists the maximum delay time that the actuator can provide with different cases. In Table 3.6, the default dead time of V_{SW} is also listed, which will be further explained in Section 4.2. For all the cases, the maximum delay time that the actuator can provide is larger than the default dead time, which means the actuator satisfies the requirement.

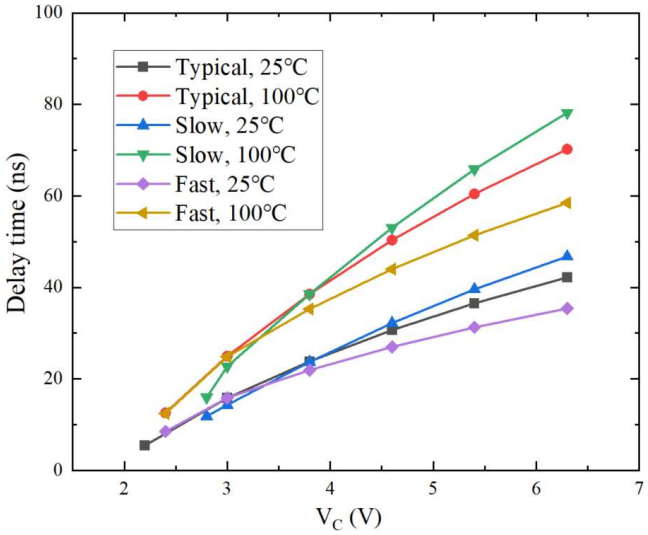


Figure 3.9 $T_{d,falling}$ vs. V_C for all process corners at 25°C and 100°C

Table 3.6 $V_{TH,INV}$, maximum relative delay time and default rising/falling edge dead time for all process corners at 25°C and 100°C

	$V_{TH,INV}$ (V)	**Max Delay Time (ns)**	**Rising/falling edge default dead time (ns)**
Typical corner, 25°C	2.16	42.2	29.9/20.2
Typical corner, 100°C	2.33	70.2	35.7/25.2
Slow corner, 25°C	2.60	46.8	34.5/24.0
Slow corner, 100°C	2.77	78.2	42.6/31.6
Fast corner, 25°C	1.75	35.4	26.5/17.3
Fast corner, 100°C	1.92	58.5	30.4/20.4

3.3.3 Actuator Clocks

When designing the *ON* and *OFF* signals of the actuator, the auto-zeroing clock in the integrator also needs to be taken into consideration. Figure 3.10 shows the integrator and the actuator circuit. Figure 3.11 shows the auto-zeroing clock and the actuator control clock, taking the rising edge as an example. The auto-zeroing signal V_{AZ_R} is explained in Section 3.2. For the rising edge, the *OFF* signal is generated by V_{MTM_F} ***AND*** V_{LS_OFF}, which is also the auto-zeroing signal for the falling edge V_{AZ_F}. The design of the actuator clock takes advantage of the following aspects.

- The rising edge of the *OFF* signal is aligned with the rising edge of V_{LS_OFF}, which is the falling edge of the low-side PWM signal. So that the actuator can add a delay time to the low-side PWM signal and reduce the dead time at the rising edge.
- The duration of the *OFF* signal is always less than half of the period, leaving more time for the *ON* signal. Since the OTA is not in the loop during the auto-zeroing phase, V_C is disturbed and needs some time to settle to the desired value after the auto-zeroing ends. Figure 3.11 shows the extreme case, the time between the turn-off of *AZ* and the turn-on of *OFF* is very short, which is denoted as T_{adj} and is only around 10 ns. Since the *ON* signal is turned on before, V_C does not need to be charged from 0. Instead, it only needs to be slightly adjusted, which can be achieved within the time T_{adj}.
- With 15% duty cycle (extreme value for -3 dB), the duration of the *OFF* signal is around 70 ns, which is still enough to discharge C_{ACT}.

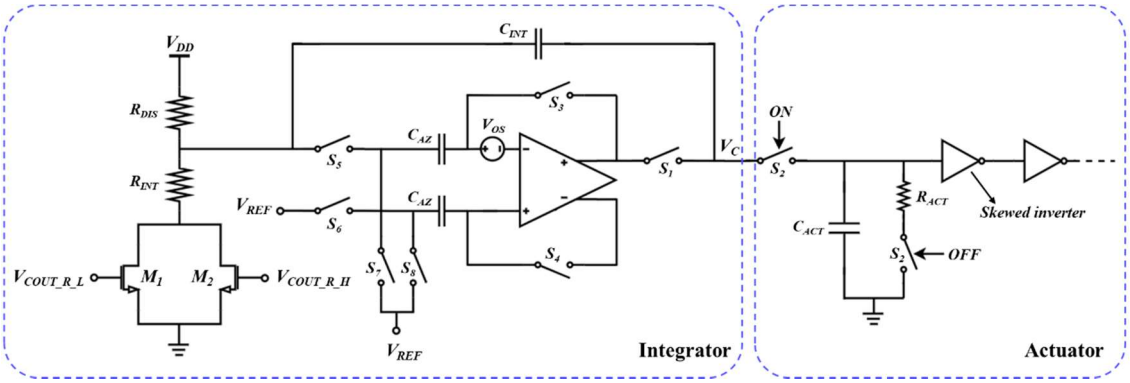


Figure 3.10 Integrator and actuator circuit

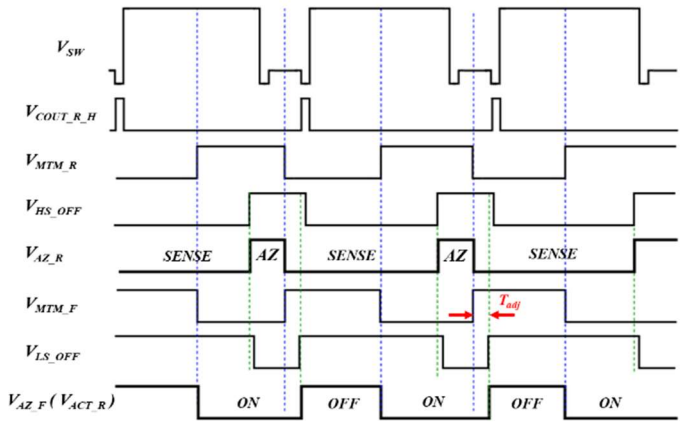


Figure 3.11 Auto-zeroing clock and actuator clock for rising edge (blue dotted line: transitions at the middle of V_{SW}; green dotted line: dead time between the high-side and low-side OFF signal)

Since during auto-zeroing, switch S_1 is open and charges will be shared between C_{INT} and C_{ACT}. V_C is disturbed. In order to make V_C adjust to the correct value in a very short time, the disturbance of V_C during auto-zeroing cannot be too large, requiring C_{ACT} much smaller than C_{INT}.

Chapter 4 Simulation Results

This chapter starts with the layout of the circuit in Section 4.1. Section 4.2 introduces the half-bridge class D amplifier test bench and the start-up of the whole circuit. Then the circuit is simulated with 15% and 85% fixed duty cycle and the results are shown in Section 4.3. In Section 4.4, the simulation results with -3 dBFS sinusoidal input are presented and discussed.

4.1 Layout

Figure 4.1 shows the layout of the proposed dead time control circuit. The size is 2.78 mm × 1.29 mm. The dead time control circuit is integrated into a half-bridge class D amplifier with an 85 V supply voltage. The chip is taped out using the 200 V GaN process.

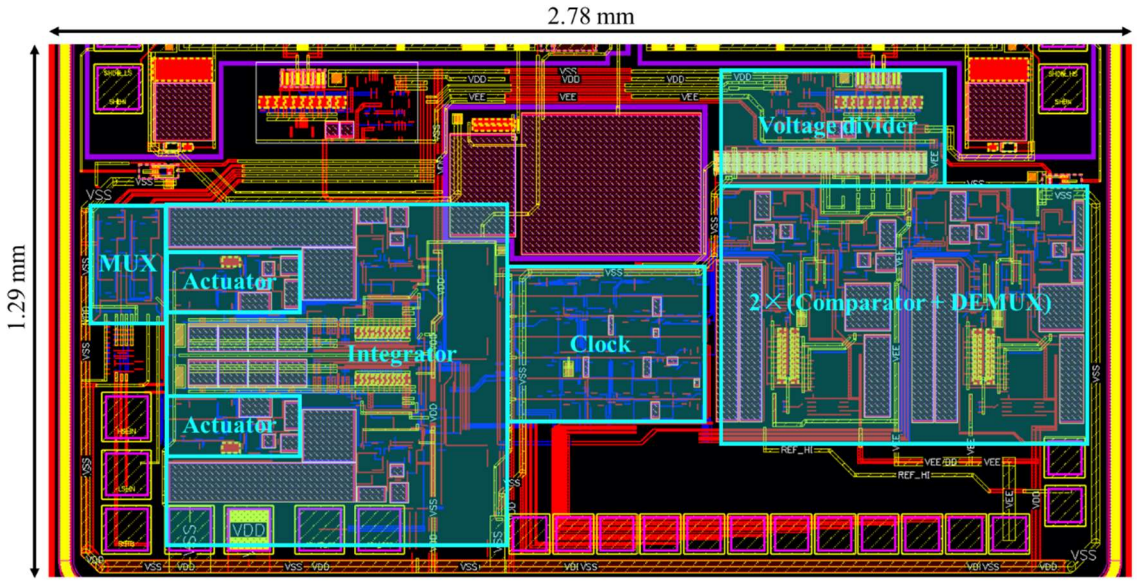


Figure 4.1 Layout of the dead time control circuit

4.2 Test Bench Introduction and Circuit Start-up

As mentioned in Chapter 2, there is a 20 ns default dead time at the input PWM signal, which is from an external setup. Due to the variation in the performance of blocks like gate drivers, the default dead time at V_{SW} varies with corners and temperature. Table 4.1

shows the simulated default dead time for different cases, using 85% fixed duty cycle as an example. As Figure 4.2 shows, the dead time is defined as the time when V_{SW} is lower than -1 V. By applying this measurement method, the real dead time is smaller than the measured value. Taking the falling edge as an example, after the dead time ends, it takes some time to pull up the V_{GS} of the low-side power transistor (from node A to B in Figure 4.2).

Table 4.1 Default dead time at V_{SW} for different corners and temperatures

Default Dead Time	Rising edge (ns)	Falling edge (ns)
Slow corner, 25℃	34.5	24.0
Slow corner, 100℃	42.6	31.6
Fast corner, 25℃	26.5	17.3
Fast corner, 100℃	30.4	20.4
Typical corner, 25℃	29.9	20.2
Typical corner, 100℃	35.7	25.2

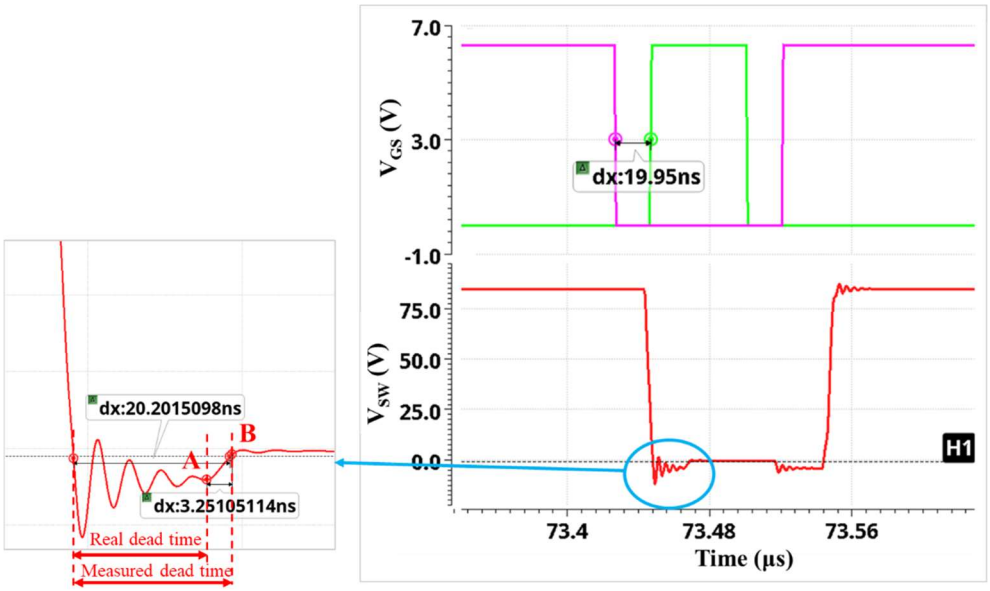


Figure 4.2 Default dead time at input and V_{SW}

The start-up of the circuit is shown in Figure 4.3. The supply voltage *PVDD* is first pulled up from 0 to 85 V. Signal *RSTB* is used to enable the output of the switching node. After *RSTB* is switched from low to high, it takes some time for V_{SW} to output stable pulses with default dead time. Then the signal *ENABLE* is switched from low to high, which enables

the dead time control circuit. After enabling the dead time control circuit, the dead time is observed to be reduced, and the control voltage V_C is increased from 0 to a stable value (for fixed duty cycle input).

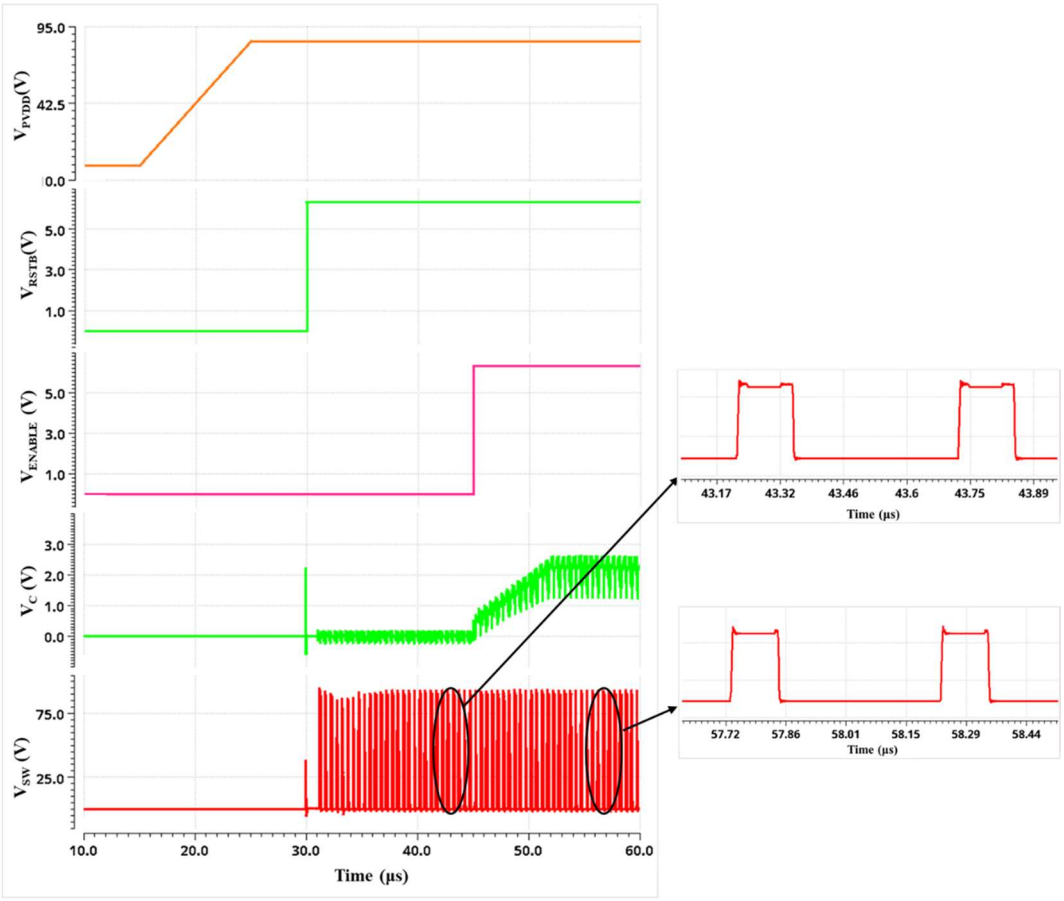


Figure 4.3 Startup of the circuit

4.3 Fixed Duty Cycle Simulation Results

The proposed dead time control circuit is simulated with the half-bridge class D amplifier test bench with 15% and 85% duty cycle, which are the extreme values of -3 dB input. The switching frequency is 2 MHz.

Table 4.2 shows the simulation results of the dead time of the rising edge and falling edge of V_{SW} before and after modulation. Figure 4.4 shows the V_{DS} curve of the low-side power transistor before and after dead time modulation for different corners and temperatures. It can be clearly observed that after modulation, dead time is reduced from a large default value to a small value of around 5 ns for all the corners and temperatures.

Table 4.2 Dead time of rising and falling edge of V_{SW} before and after modulation (85% duty cycle)

85% duty cycle	Rising edge		Falling edge	
	Before	After	Before	After
Slow corner, 25℃	34.5	6.5	24.0	7.0
Slow corner, 100℃	42.6	8.8	31.6	7.3
Fast corner, 25℃	26.5	5.8	17.3	6.6
Fast corner, 100℃	30.4	5.4	20.4	6.0
Typical corner, 25℃	29.9	5.8	20.2	6.5
Typical corner, 100℃	35.7	5.9	25.2	6.4

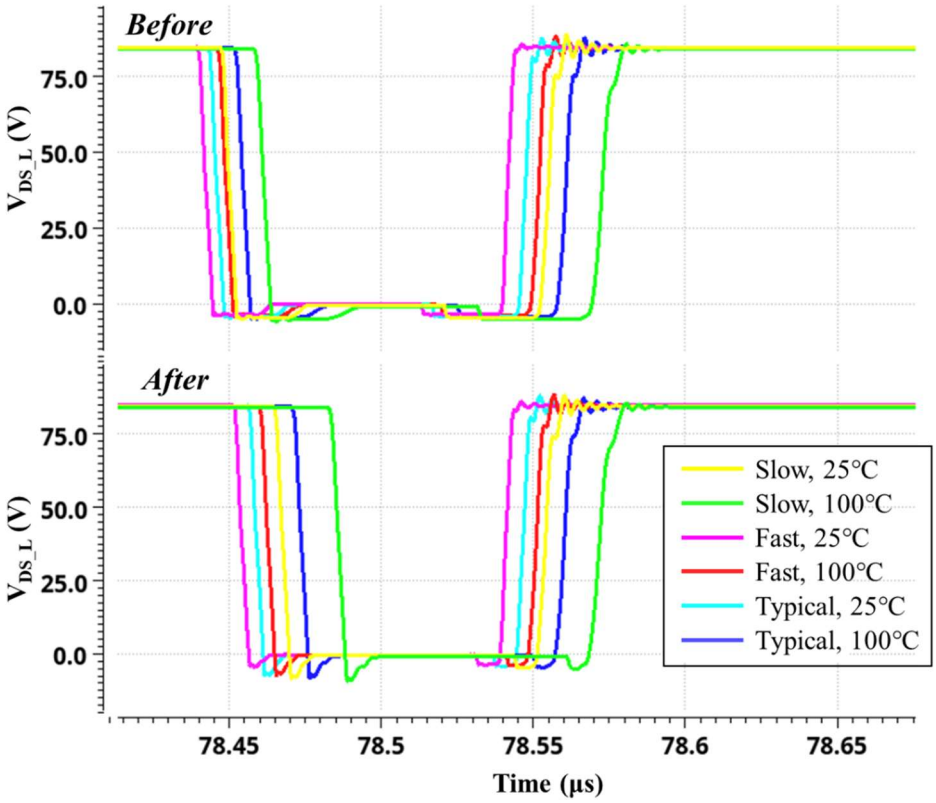


Figure 4.4 V_{DS} of low-side power transistor before and after modulation (85% duty cycle)

A similar simulation is conducted for 15% fixed duty cycle input. The dead time of V_{SW} before and after modulation is listed in Table 4.3. And V_{DS} of the high-side power transistor before and after modulation is shown in Figure 4.5.

Table 4.3 Dead time of rising and falling edge of V_{SW} before and after modulation (15% duty cycle)

15% duty cycle	Rising edge		Falling edge	
	Before	After	Before	After
Slow corner, 25℃	34.5	6.4	24.0	6.4
Slow corner, 100℃	42.6	8.2	31.6	8.2
Fast corner, 25℃	26.5	5.7	17.3	6.4
Fast corner, 100℃	30.4	5.1	20.4	5.7
Typical corner, 25℃	29.9	5.4	20.2	6.2
Typical corner, 100℃	35.7	5.8	25.2	6.1

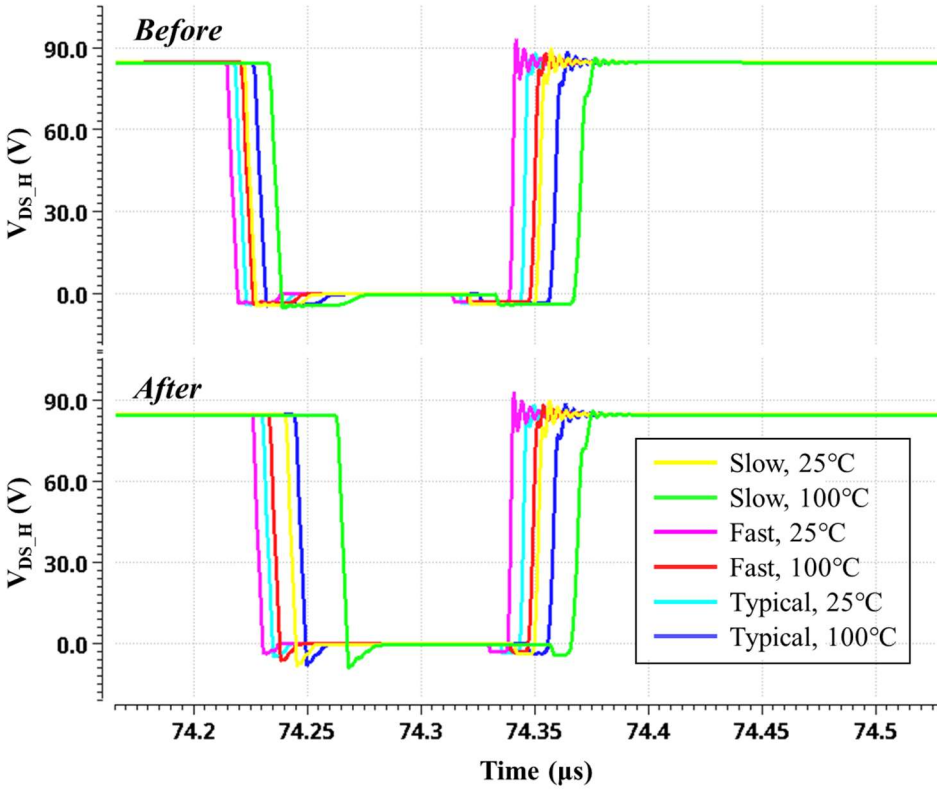


Figure 4.5 V_{DS} of high-side power transistor before and after modulation (15% duty cycle)

4.4 -3 dB Sinusoidal Input Simulation Results

The proposed dead time control circuit is simulated with -3 dB sinusoidal input at 10 kHz. The switching frequency is 2 MHz. With a 4 Ω resistive load, the output power input power and efficiency of the whole circuit (the proposed dead time control circuit with a half-bridge class D amplifier circuit) are simulated, which are listed in Table 4.4. It can be concluded that the output power is significantly increased by 1.20-1.67 times after dead time modulation. And after dead time modulation, the third-order harmonic distortion (HD3) is improved by 5-10 dB for all the corners and temperatures.

Table 4.4 Output power, input power and efficiency of the whole circuit before and after dead time modulation (-3 dB input)

-3 dB input	**Before**			**After**			$\frac{P_{out,after}}{P_{out,before}}$
	Pout	**Pin**	**Efficiency**	**Pout**	**Pin**	**Efficiency**	
Slow corner, 25℃	67.30	73.81	91.2%	93.16	101.4	91.9%	1.38
Slow corner, 100℃	58.35	66.18	88.2%	97.5	108.1	90.2%	1.67
Fast corner, 25℃	75.54	81.39	92.8%	90.46	97.49	92.8%	1.20
Fast corner, 100℃	70.49	76.86	91.7%	92.04	99.77	92.3%	1.31
Typical corner, 25℃	71.98	78.07	92.2%	91.62	98.88	92.7%	1.27
Typical corner, 100℃	65.62	72.45	90.6%	93.28	101.8	91.6%	1.42

Table 4.5 HD3 before and after dead time modulation (-3 dB input)

HD3 (dB)	**Before**	**After**
Slow corner, 25℃	-22.84	-32.21
Slow corner, 100℃	-21.01	-30.30
Fast corner, 25℃	-24.82	-29.07
Fast corner, 100℃	-23.67	-30.68
Typical corner, 25℃	-23.90	-30.33
Typical corner, 100℃	-22.49	-32.32

4.5 Simulation Results Analysis

From the fixed duty cycle simulation results, it can be discovered that for slow corner 100 ℃, the residual dead time is around 8 ns, which is ~60% larger than the desired value. The main error source is from the comparator. As Section 3.1 shows, the real bandwidth of the comparator is lower than the required value, which makes the comparator filter out useful information and induce distortion. After replacing the comparator with ideal components, the residual dead time is reduced to 6.4 ns. Other error sources include the charge sharing between C_{INT} and the auto-zeroing input capacitance C_{AZ} at the beginning of the sensing phase (when the switch S_5 in Figure 3.1 is from OFF to ON). After removing the auto-zeroing, the residual dead time is further reduced to 5.4 ns.

After dead time modulation, the output power can be increased because of the modulation in the duty cycle. Taking the typical corner (25 ℃) as an example, for a signal with 85% duty cycle, t_{before} in Figure 4.6 is 400 ns, if the average dead time at V_{SW} is estimated at 25 ns. So after the LC filter, the maximum value of V_{OUT} is $0.8V_{SUP}$. After dead time modulation, t_{after} in Figure 4.6 is 420 ns, if the residual dead time is 5 ns. So the maximum value of V_{OUT} can reach $0.84V_{SUP}$. As a result, the amplitude of V_{OUT} can be increased by 1.13 times, and the output power can be increased by 1.28 times.

From Table 4.4, the output power is increased by 91.62/71.98 = 1.27 times with simulation. The simulation result matches the calculation result well.

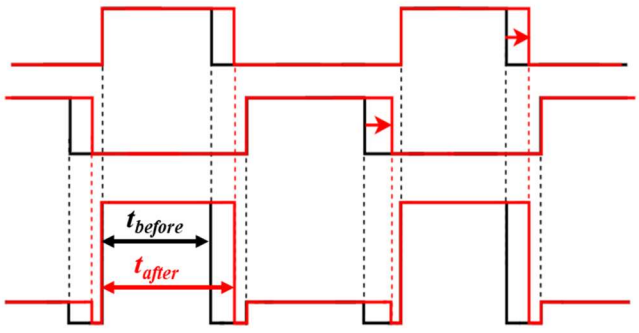


Figure 4.6 Duty cycle before and after dead time modulation

Figure 4.7 shows the output duty cycle vs. input duty cycle curve before and after dead time modulation. After dead time modulation, better linearity can be achieved, which explains better HD3.

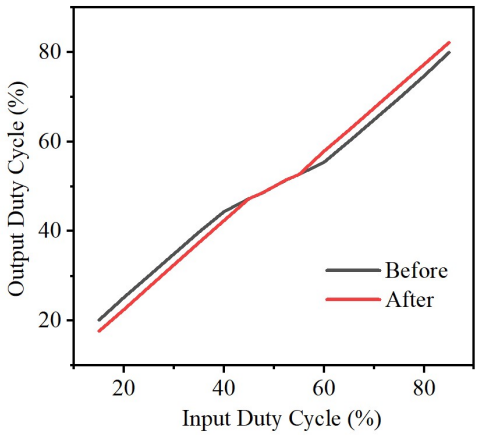


Figure 4.7 Output duty cycle vs. input duty cycle before and after dead time modulation

Chapter 5 Conclusion and Future Work

This project proposes a new kind of dead time control circuit. The dead time control circuit is integrated with a monolithic GaN class D amplifier and can work with -3 dB input signals. With the dead time control circuit, the dead time can be reduced to a small value of around 5 ns. After dead time modulation, the output power is largely increased. The third-order harmonic distortion is also improved.

There are several aspects that can be improved in the future work. Methods need to be explored to lower the errors of residual dead time for different corners, including using comparators with better performance. Besides, the stability requirements of the whole circuit needs to be explored. Furthermore, other methods of controlling dead time can be explored to make the output more linear, so that the HD3 can be further improved.

Appendix

A. Derivation of Equation 2.3

When the circuit reaches the steady state, the increase of V_C is equal to the decrease of V_C in one period.

From Equation 2.1, the decrease in V_C is:

$$\Delta V_{C1} = -\frac{V_{DD} - V_{REF}}{R_{DIS}C_{INT}}T$$

where T is the period.

From Equation 2.2, the increase of V_C is:

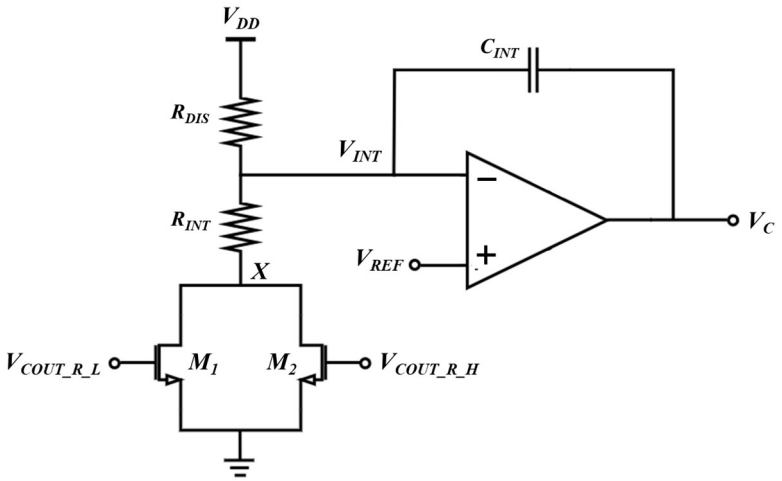
$$\Delta V_{C2} = \frac{V_{REF}}{R_{INT}C_{INT}}t_{res}$$

where t_{res} is the residual dead time.

Since $|\Delta V_{C1}| = |\Delta V_{C2}|$, the residual dead time is:

$$t_{res} = \frac{R_{INT}}{R_{DIS}}(\frac{V_{DD}}{V_{REF}} - 1)T$$

B. Derivation of the unity gain frequency of the integrator: $f_0 = \frac{1}{4\pi R_{INT}C_{INT}}$

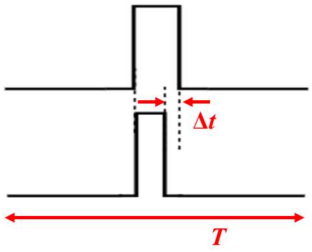


The gain of the integrator can be calculated as

$$A_V = \frac{\Delta V_{OUT}}{\Delta V_{IN}}$$

where ΔV_{OUT} is the voltage change at output V_C, and ΔV_{IN} is a small voltage change in the input.

Since the input signals are the pulses generated by comparators, ΔV_{IN} can be denoted by the average value of the pulses, which converts a change in pulse width Δt into a change in the voltage.

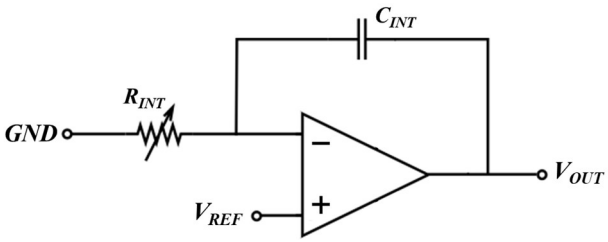


So for a small change in the pulse width Δt, ΔV_{IN} is

$$\Delta V_{IN} = \frac{\Delta t}{T} V_{DD}$$

So that

$$\Delta t = \Delta V_{IN} \cdot \frac{T}{V_{DD}}$$



The change in pulse width induces the change of equivalent resistance of R_{INT}.

$$R_{INT,eq} = \frac{R_{INT}}{t/T}$$

where R_{INT} is the real resistance, and $R_{INT,eq}$ is the equivalent resistance.

So that

$$\Delta\frac{1}{R_{INT,eq}} = \frac{\Delta t}{R_{real} \cdot T}$$

For the integrator with an ideal amplifier:

$$-\frac{V_{REF}}{R_{INT,eq}} = (V_{REF} - V_{OUT}) \cdot sC_{INT}$$

So that

$$V_{OUT} = V_{REF} \cdot (1 + \frac{1}{sC_{INT}R_{INT,eq}})$$

With a small change in the equivalent resistance,

$$\Delta V_{OUT} = \frac{V_{REF}}{sC_{INT}} \cdot \left(\Delta\frac{1}{R_{INT,eq}}\right) = \frac{V_{REF}}{sC_{INT}} \cdot \frac{\Delta t}{R_{real} \cdot T} = \frac{V_{REF}}{sC_{INT}} \cdot \frac{\Delta V_{IN}}{V_{DD} \cdot R_{real}}$$

So the gain of the integrator is

$$A_V = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{V_{REF}}{sC_{INT} \cdot V_{DD} \cdot R_{INT}} = \frac{1}{2sC_{INT}R_{INT}}$$

if V_{REF} = 1/2 V_{DD}

So the unity gain frequency of the integrator is

$$f_0 = \frac{1}{4\pi R_{INT}C_{INT}}$$