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A ±12-A High-Side Current Sensor With 25 V Input CM Range and 0.35% Gain Error From −40 °C to 85 °C

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***Abstract*—This letter presents the most accurate shunt-based high-side current sensor ever reported. It achieves a 25 V input common-mode range from a single 1.8-V supply by using a beyond-the-rails ADC. A hybrid analog/digital temperature compensation scheme is proposed to simplify the circuit implementation while maintaining the state-of-the-art accuracy. Over a ±12-A current range, the sensor exhibits 0.35% gain error from −40 °C to 85 °C with 3× better power efficiency.**

***Index Terms*—ΔΣ ADC, current sensor, high voltage (HV), high-side current sensing, shunt resistor, temperature compensation, temperature sensor.**

I. Introduction

Accurate current sensing is critical in many applications including battery management, motor control, and over-current protection. The most common and simple approach for current sensing is the use of a shunt resistor. Based on where the shunt resistor is placed, two approaches can be identified: 1) low-side current sensing and 2) high-side current sensing (Fig. 1). Compared to low-side current sensing, high-side current sensing does not increase the resistance of the ground path and enables robust short-circuit detection. However, the challenge associated with high-side current sensing is that it requires high-voltage (HV) interface circuits to accommodate large input CM voltages. Such circuits typically consist of HV instrumentation amplifiers (IAs) [1] that translate HV signals down to low voltage domain where they are digitized by a conventional ADC. In this design, a HV beyond-the-rails ADC [2] is used to directly digitize HV signals, thus obviating the need for HV IAs, and reducing both chip area and power.

To build fully integrated low-cost current sensors, shunt resistors can be realized with either metal layers of a CMOS process, or the lead-frame of a plastic package [3]. In both cases, shunt resistance will vary with temperature, thus requiring a temperature compensation scheme (TCS) for good accuracy. Unlike the digital TCS in [3] which requires a relatively accurate temperature sensor (TS), this design proposes a hybrid analog/digital TCS to greatly relax the required accuracy of the TS while maintaining the state-of-the-art accuracy. Furthermore, it also provides flexible current-sensing accuracy in different operation modes depending on different applications.

This letter is organized as follows. Section II describes the system architecture and circuit implementation of the sensor. Experimental results are presented in Section III and Section IV concludes this letter.

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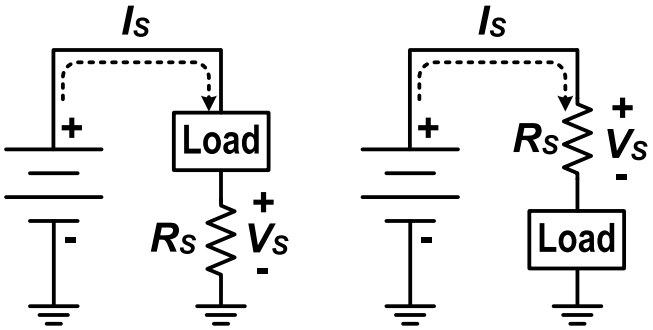

Fig. 1. Low-side current sensing (left) and high-side current sensing (right).

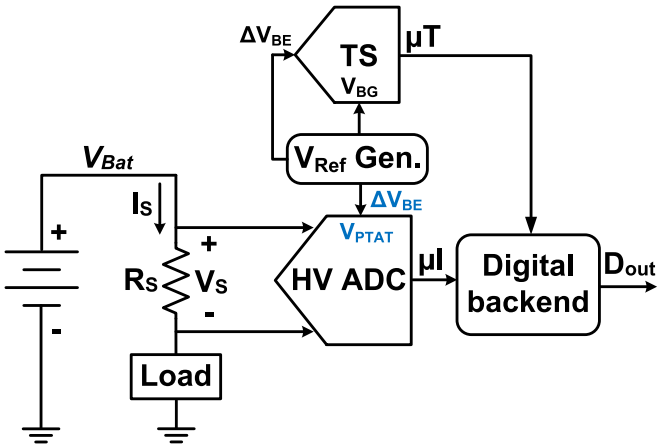

Fig. 2. System architecture of the sensor.

II. Sensor Architecture

A. System Overview

Fig. 2 shows the system architecture of the sensor. It consists of a shunt resistor R_S (∼1 mΩ) made from a copper PCB trace, a HV beyond-the-rails ADC, a TS, and a reference voltage generator (RVG).

For rapid prototyping, a PCB trace is used to emulate the lead-frame shunt used in [3]. Compared to an on-chip metal shunt [4], it enables a ±12-A current sensing range with no extra silicon area cost, which is 3× wider than [4]. Good thermal coupling and galvanic isolation are achieved by directly bonding the chip to the trace with nonconductive glue. The HV ADC digitizes the voltage drop across the shunt V_S via Kelvin contacts $S1$ & $S2$ (Fig. 3) with regard to the voltage reference V_{PTAT} generated from the RVG. Meanwhile, the TS senses the shunt's temperature, whose output μT is used to correct the digitized shunt voltage μI with the help of a single second-order polynomial.

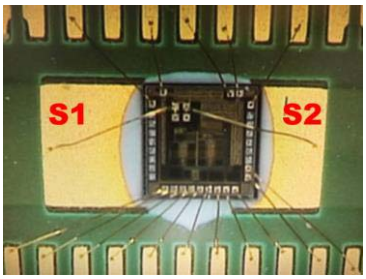

Fig. 3. Bonding diagram of the chip.

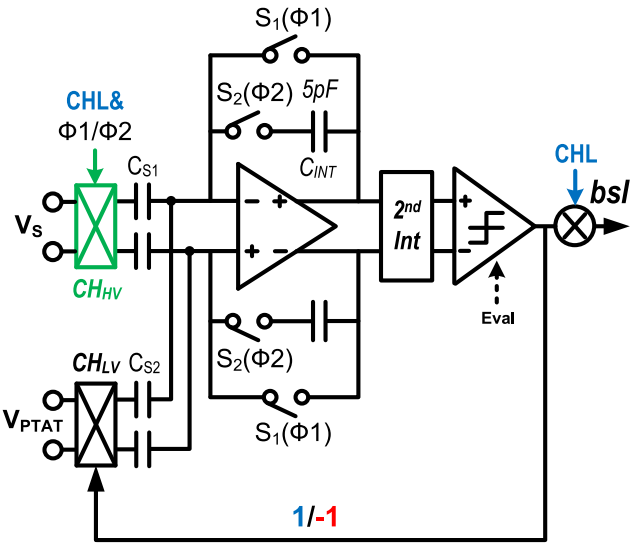

Fig. 4. Schematic of the beyond-the-rails ADC.

B. Beyond-the-Rails ADC

Fig. 4 shows the schematic of the HV beyond-the-rails ADC. It is based on a second-order switched-capacitor ΔΣ ADC. A HV chopper CH_{HV} [2] ensures that the voltage across the shunt V_S is sampled by capacitors C_{S1} (2 pF) in a cross-coupled fashion such that they block the input CM voltage. In a similar manner, the reference V_{PTAT} is sampled onto feedback capacitors C_{S2}. Both C_{S1} and C_{S2} are implemented as HV fringe capacitors with a breakdown voltage of 70 V. In this design, $C_{S2} = C_{S1}/2$, which reduces the equivalent reference voltage and ensures that the chosen ±12-A current range corresponds to ∼60% of the ADC's dynamic range (DR). This contrasts favorably with [3], in which only 10% of the ADC's DR is utilized. It improves the ADC's power efficiency by reducing the integrators' output swing, the kT/C noise contribution from its feedback branch, and the capacitive load of the first integrator. In addition, the ADC's loop filter is realized with energy-efficient current-reuse amplifiers. Correlated double sampling and low-frequency chopping (CHL) are employed in the ADC to suppress offset and 1/*f* noise. For simplicity, CHL is realized by logically controlling the states of a single HV input chopper.

The schematic of the HV chopper is shown in Fig. 5. Clock signals Φ1 and Φ2 are capacitively coupled to the gates of four switches M_{1-4} via a level shifter composed of two HV capacitors C_{1-2} and a latch M_{5-6}. A minimum selector M_{S1-2} ensures that coupled clocks are always superimposed on the $V_{\min}$ (the lower of V_{ip} and V_{in}), which minimizes the leakage current of M_{1-4} in the presence of bidirectional input voltages.

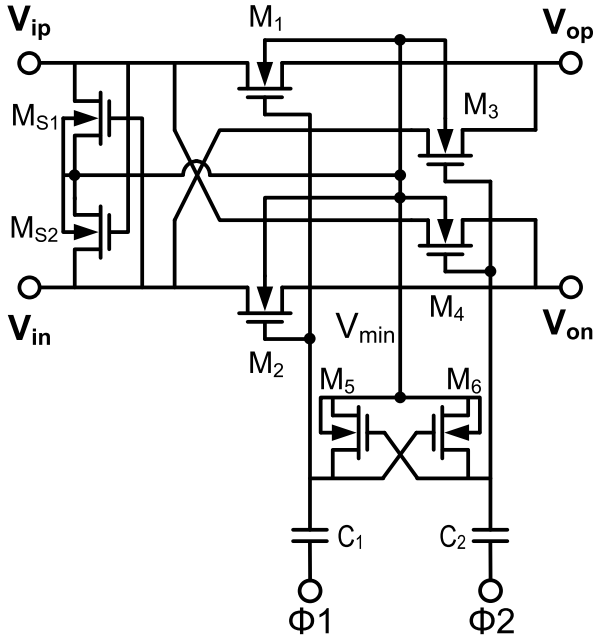

Fig. 5. Simplified schematic of the HV chopper.

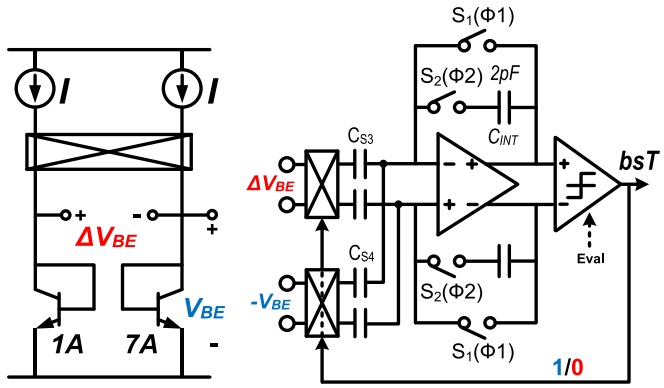

Fig. 6. Schematic of the RVG (left) and the TS (right).

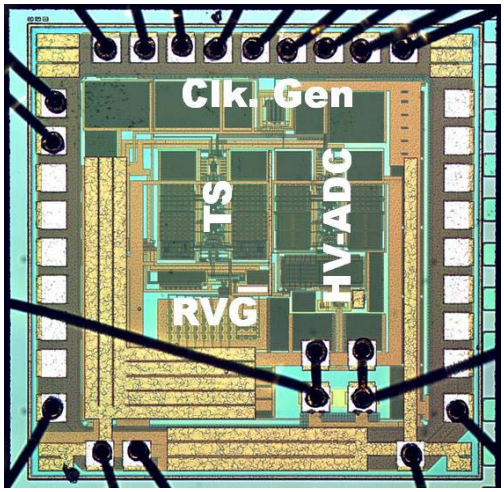

Fig. 7. Chip photograph.

C. Hybrid Analog/Digital Temperature Compensation Scheme

In [3], the shunt voltage V_S is digitized by an ADC with respect to a nearly temperature-independent bandgap reference. An on-chip

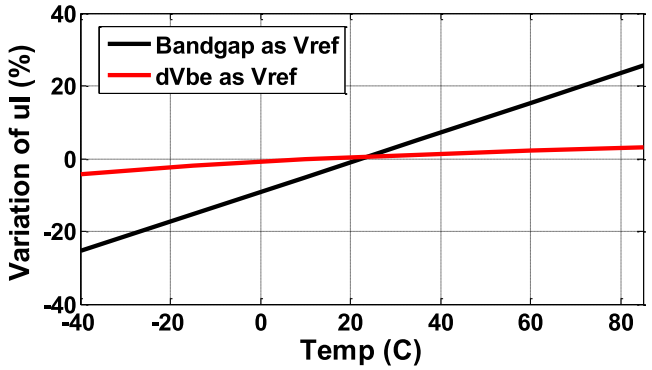

Fig. 8. Variation of μI over temperature.

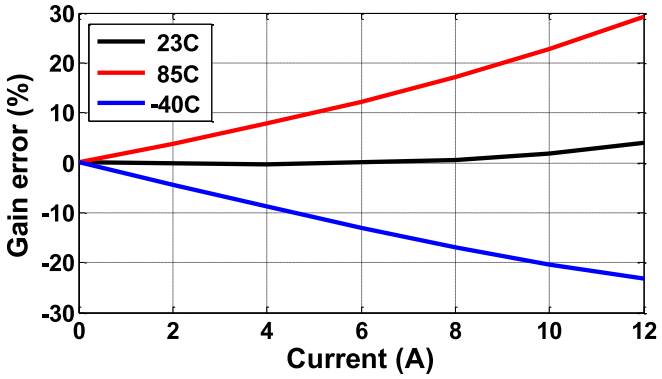

Fig. 9. Current sensing gain error without TCS.

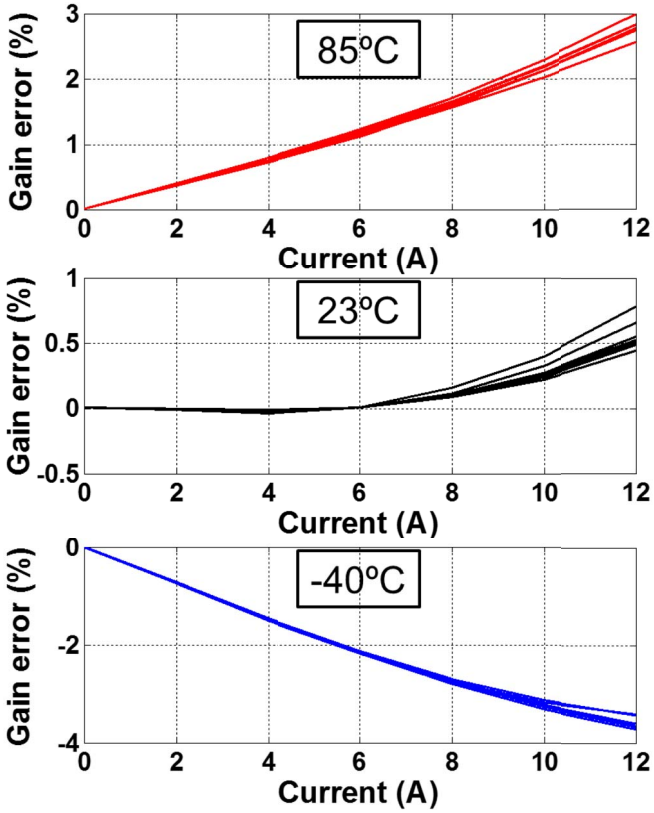

Fig. 10. Current sensing gain error with only analog TCS.

TS then senses the shunt's temperature such that its temperature dependency can be compensated in the digital domain. Since copper has a relatively large temperature coefficient of resistance (TCR $\sim$ 0.38%/°C), the TS has to achieve an inaccuracy of less than 0.5 °C in order not to become a dominant error source.

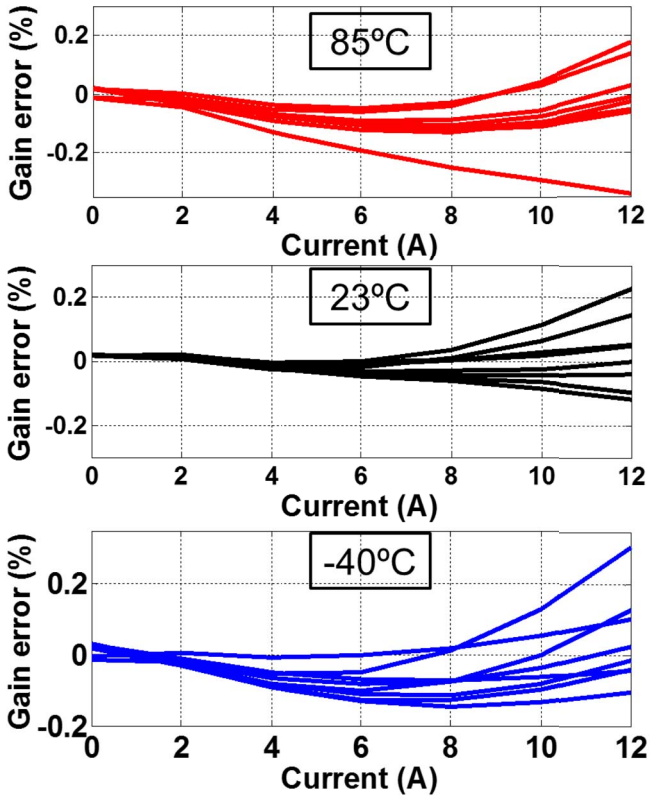

Fig. 11. Current sensing gain error with hybrid TCS.

In this design, instead of a bandgap reference, a proportional-to-absolute-temperature (PTAT) voltage V_{PTAT} is employed as the ADC's reference [4]. Since the shunt resistance's temperature dependency is also roughly PTAT, it is effectively compensated by the TC of V_{PTAT}, thus realizing an analog TCS. However, since the shunt resistance's temperature dependency is nonlinear and not perfectly PTAT, there will still be some residual error. This can be modeled by a fixed second-order polynomial and then digitally corrected with the help of the TS. Noting that the TC of this residual error is 8$\times$ less than that of copper, the TS's accuracy can be relaxed for the same current sensing accuracy.

Fig. 6 shows the schematic of the RVG and the TS. Two vertical NPN transistors are biased at a current density ratio of 7. The base-emitter voltage difference ΔV_{BE} of two NPN transistors is PTAT, and is used as the ADC's reference V_{PTAT}. Since a bandgap reference is not necessary, no V_{BE} sampling capacitors are required in the ADC (Fig. 4), unlike [3]. This avoids errors due to capacitor mismatch and V_{BE} curvature. Dynamic element matching of the NPNs and CHL for TS are eliminated in this design due to the relaxed requirement on the TS accuracy. The current sources are chopped to suppress their $1/f$ noise.

The TS digitizes the shunt's temperature by charge-balancing ΔV_{BE} against $-V_{\mathrm{BE}}/10$ [3]. When bsT is 0, C_{S3}(= 1 pF) samples $+\Delta V_{\mathrm{BE}}$ and when bsT is +1, C_{S4} (= 100 fF) samples $-V_{\mathrm{BE}}$. This results in an average value of bsT (μT) equal to $\Delta V_{\mathrm{BE}}/(\Delta V_{\mathrm{BE}}+V_{\mathrm{BE}}/10)$ [$(\Delta V_{\mathrm{BE}}+V_{\mathrm{BE}}/10)$ generates a bandgap reference], which is a linear function of temperature.

III. Experimental Results

The sensor is fabricated in a 0.18-μm HV BCD CMOS technology with a core area of 1.4 mm^2 (Fig. 7). At room temperature, it draws

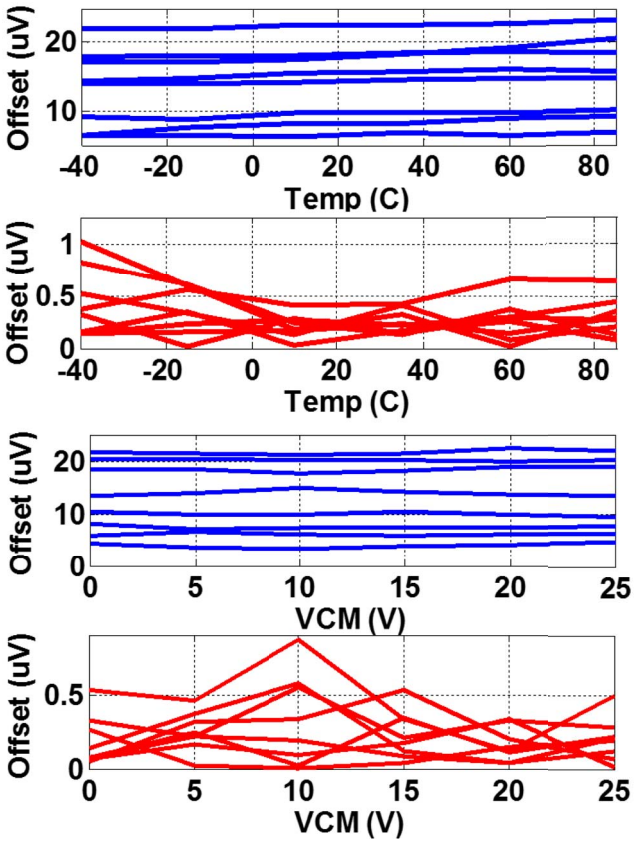

Fig. 12. Offset before CHL (blue) and after CHL (red) over temperature and input CM range.

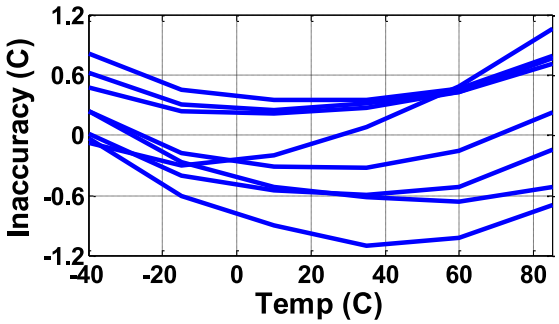

Fig. 13. Temperature sensing error.

13.8 μA from a 1.8-V supply. At a 200-kHz sampling frequency and for a conversion time of 12.5 ms, the ADC and TS achieve resolutions of 1.1 μV_{rms} and 10 mK_{rms}, respectively.

Fig. 8 shows the variation of the ADC's bit-stream average μI over temperature. For a constant input current (1 A), μI varies by ±28% from −40 °C to 85 °C due to the large TCR of the copper shunt when the bandgap reference is used. This drops to ±3.5% when the PTAT reference V_{PTAT} is used. Without the TCS, the sensor only achieves a gain error of 30% (one sample) from −40 °C to 85 °C (Fig. 9). The use of a PTAT reference (analog TCS) reduces this to 3.8% (eight samples) (Fig. 10), which is further reduced to 0.35% when the output of the ADC is digitally corrected (Fig. 11). Each sensor is individually trimmed (at ∼23 °C and 4 A) to correct the spread of the shunt's nominal resistance. From −40 °C to 85 °C and over a 25-V input CM range (ICMR), the ADC exhibits a maximum offset of 24 μV, which drops below 1 μV after applying CHL (Fig. 12). The measured inaccuracy of the TS is ±1.2 °C without trimming (Fig. 13), which is quite relaxed (2.5× worse) compared to the TS used in [3].

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	ICMR	I range	T_{Conv} (ms)	SNR (dB)	Gain error (%)	Power	FoM* (dB)
This work	**25V**	**±12A**	**12.5**	**72**	**0.35**	**25µW**	**137**
[3]	0.75V	±36A	18	67.4	0.3	19.5µW	132
[4]	25V	±4A	2.5	79	0.9	16.4µW	149
[5]	36V	±10A	8.2	69	0.5**	1.5mW	--
[6]	30V	10mA	--	--	0.1***	1mW	--

* FoM = SNR+10·log(1/(Power×2T_{Conv}))
** Uses a custom low-TC shunt
*** One sample is measured only at room temperature

The performance of the sensor is summarized in Table I. Among high-side current sensors [4], [5], this design achieves the best accuracy. Compared to [3], it achieves similar accuracy, 3× better power-efficiency and 30× wider ICMR, by using a beyond-the-rails ADC and a hybrid TCS.

IV. CONCLUSION

A shunt-based high-side current sensor has been implemented in a 0.18-μm HV BCD process. The beyond-the-rails ADC enables direct digitization of small differential signal in the presence of large CM voltage and hence reduces the power and chip area of HV interface circuits. Thanks to the hybrid TCS, the temperature sensor is greatly simplified due to the relaxed requirement on its accuracy. Based on these two techniques, the sensor achieves the state-of-the-art accuracy with 3× better power efficiency compared to previous work.

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