STELLINGEN

Behorende bij het proefschrift:

Aluminum-Mediated Selective Solid-Phase Epitaxy of High-Quality Silicon Diodes

door

Yann CIVALE

Delft, November 4, 2008

1. Mocht het mogelijk zijn een defectvrije siliciumdioxide oppervlakte te vormen, dan is het mogelijk een ideaal selectieve aluminium gemedieerde vaste-fase-epitaxie (SPE) siliciumgroei te verkrijgen (dit proefschrift, hoofdstuk 2) .

2. De steeds kleiner wordende junctiediepte in door aluminium gemedieerde vaste-fase-epitaxie silicium-diodes wordt beperkt door de minimum dikte van de "physical-vapor-deposited" aluminiumlagen die kunnen worden gefabriceerd (dit proefschrift, hoofdstuk 2).

3. Secundaire-ionen-massaspectroscopie vereist een analysegebied van enkele tientallen vierkante micrometers. Echter voor zeer goed controleerbare processen is dit eveneens toepasselijk in het submicron gebied (dit proefschrift, hoofdstuk 3).

4. Terwijl verkleining van de dimensies de kwaliteit van de door aluminium gemedieerde SPE siliciumlaag niet verslechtert, veroorzaken toepassingen voor grote-oppervlakte-elektronica een probleem (dit proefschrift, hoofdstuk 4 en 5).

5. Het groeimechanisme van de door aluminium gemedieerde vaste-fase-epitaxie silicium is langzaam. Dit maakt het mogelijk om laterale overgroei van zuiver mono-kristallijn silicium op siliciumdioxide te verkrijgen (dit proefschrift, hoofdstuk 4).

6. De ontwikkeling van moderne communicatiemiddelen maakt het mogelijk om langeafstandsrelaties te doen floreren ten koste van meer basale locale sociale interacties.

7. De mogelijkheid dat onderzoekers met de buitenwereld kunnen communiceren over de perspectieven van hun onderzoek is essentieel om toekomstige technologische progressie te verzekeren.

8. De verhouding prijs tot voedselkwantiteit, typisch voor de Franse keuken, bereikt een maximum waarde voor Franse-keuken-restaurants in het buitenland.

9. Voor mannelijke studenten geeft het schrijven van een PhD-proefschrift de gelegenheid om uit eerste hand de ongerustheid van de zwangerschap te ervaren.

10. Wonen in het buitenland ontwikkelt het gevoel deel te zijn van jouw nationale gemeenschap.

Deze stellingen worden opponeerbaar en verdedigbaar geacht en zijn als zodanig goedgekeurd door de promotor Prof. dr. L. K. Nanver.

1. If a defect-free silicon dioxide surface could be formed, it would be possible to achieve an ideally selective aluminum-mediated solid-phase epitaxial (SPE) silicon growth (this thesis, Chapter 2).

2. The downscaling of the junction depth in aluminum-mediated solid-phase epitaxy silicon diodes is limited by the minimum thickness of the physical-vapor-deposited aluminum films that can be fabricated (this thesis, Chapter 2).

3. Secondary ion-mass spectroscopy requires tens-of-μm^2-wide analysis area. However, for highly-controllable processes, it is applicable to the sub-micron range (this thesis, Chapter 3).

4. Whereas downscaling does not degrade the quality of aluminum-mediated SPE silicon, application to large-area electronics poses problem (this thesis, Chapter 4 and 5).

5. The aluminum-mediated solid-phase epitaxial growth mechanism of Si is slow. This makes possible the formation of laterally-overgrown monocrystalline silicon on silicon dioxide (this thesis, Chapter 4).

6. The development of modern communication tools has enabled long distance relationships to flourish at the expense of the more basic local social interactions.

7. The ability of researchers to communicate to the outside world about the perspectives of their research is essential for ensuring future technological progress.

8. The price to food-quantity ratio, typical of “French cuisine”, reaches a maximum value in French-style restaurants abroad.

9. Writing a PhD-thesis gives male students the opportunity to experience first hand the anxieties associated with pregnancy.

10. Living abroad develops the feeling of being part of your national community.

These propositions are considered opposable and defendable and as such have been approved by the supervisor Prof. dr. L. K. Nanver.

Aluminum-Mediated Selective Solid-Phase Epitaxy of High-Quality Silicon Diodes

Yann CIVALE

Aluminum-Mediated Selective Solid-Phase Epitaxy of High-Quality Silicon Diodes

Proefschrift

Ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof. dr. ir. J. T. Fokkema,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op dinsdag 4 november 2008 om 10:00 uur

Door

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geboren te Sète, Frankrijk

Dit proefschrift is goedgekeurd door de promotor:
Prof. dr. L. K. Nanver

Samenstelling promotiecommissie:

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Yann Civale
Aluminum-Mediated Selective Solid-Phase Epitaxy of High-Quality Silicon Diodes,
Ph.D. thesis Delft University of Technology, with summary in Dutch.

Keywords: aluminum doping, elevated contacts, low temperature crystallization, metal-induced crystallization, selective solid-phase epitaxy, silicon diodes, silicon-on-insulator, solar cells, ultra-abrupt junctions, ultrashallow junctions.

ISBN: 978-90-9023633-9

Printed by PrintPartners Ipskamp B.V., Enschede, The Netherlands.

A mes parents,
A mes grand-parents qui, d'où ils sont, veillent sur moi.

Contents

Chapter 1

Introduction

In this thesis a novel technique for forming ultrashallow abrupt silicon (Si) junctions using an aluminum-mediated solid-phase epitaxy (SPE) process is studied. This method presents several very appealing aspects: for the first, it enables to locally create mono-crystalline Si regions, doped with aluminum (Al), with a very high degree of controllability. Moreover, the Al-doping is highly uniform, which makes the as-grown p^+ Si regions directly usable for device fabrication. Several examples of electrical measurements of SPE-Si-based devices, fabricated at DIMES laboratories, are presented in this study and they show that the quality of the SPE-Si remains very good when both the vertical and lateral dimensions are scaled down to the sub-100 nm range. The thermal processing temperature of the Al-mediated SPE technique, which is kept below 500°C in this work, makes possible the incorporation of SPE grown Si modules both in front- and back-end IC processes.

This study has been performed in the general context of the very high interest in nanostructures such as nanowires (NWs) and carbon nanotubes (CNTs). Over the past decade, the techniques for forming these nanostructures have known impressive developments, driven not only by fundamental nanoscience studies but also by their claimed potential for being building blocks of future generations of transistors [1]. Among all the reported techniques, the one which has given the highest material purity and crystallinity uses a metal nanosized particle as a catalyst for semiconductor synthesis at temperature of about 500°C. However, these nanostructures are obtained by processes which are often not compatible with ex-

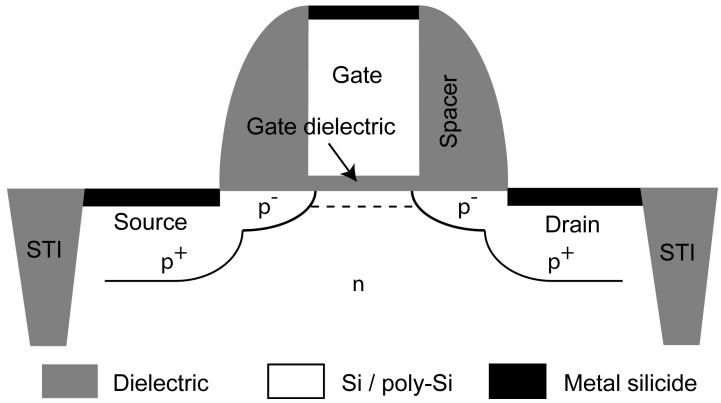


Figure 1.1: Schematic cross-section of a PMOS transistor.

isting integrated circuit (IC) processes. They commonly use materials such as gold that have high diffusivity in Si, and is known to cause midgap states that degrade junction performance. Moreover, these techniques are also characterized by a lack of controllability of the grown structure location and dimensions. Thus, future applications for nanowires are more likely in large area electronics such as lighting, solar cells, displays and sensors, where bundles of wires are used.

On the other hand, Al/Si alloys are well-known materials in microelectronics, since they were introduced in IC-processing lines in the early 1970's as a conventional metallization layer. The phenomenon of diffusion of Si through an Al thin film layer and the crystallization of Si nuclei during Al/Si alloying at low temperature (below 577°C, which is the eutectic temperature of the binary Al/Si alloy) has also been investigated for decades [3]. Thus, the ambition of this study has been to combine the recent breakthroughs on metal-catalyst growth of semiconducting nanowires with the well-established knowledge gained on the Al/Si system in order to develop a fully complementary metal-oxide-semiconductor (CMOS) compatible and scalable technique for forming Si junctions at low temperature.

This introductory chapter discusses the goals of this study by placing this work in the general perspective of low-temperature Si junction formation, for instance for applications in source and drain (S/D) regions in MOS Field Effect Transistor (FETs), large-area polycrystalline Si deposition on dielectrics and Si nanowire synthesis. The challenges, not only to form NWs but also to be able to contact

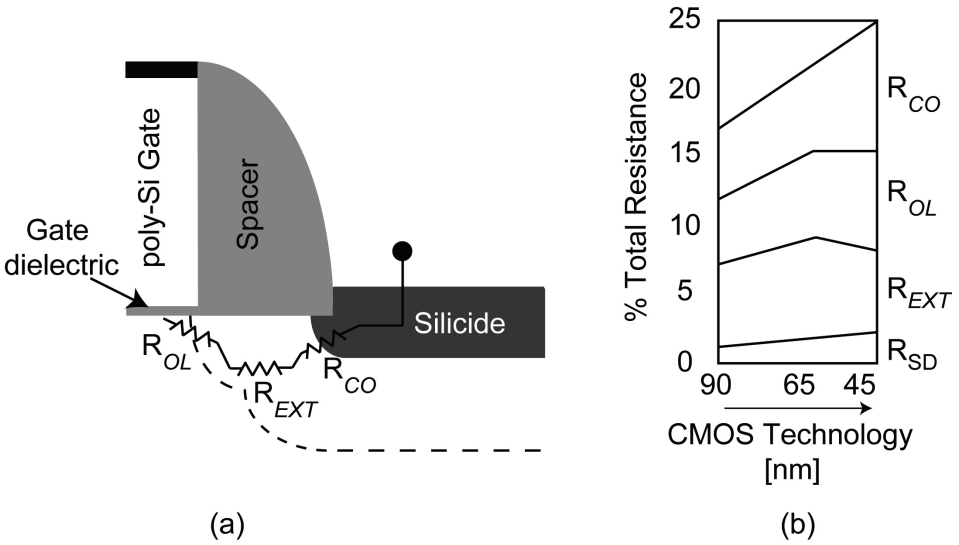


Figure 1.2: (a) Schematic illustration of the equivalent resistance in the S/D region. R_{OL}, R_{EXT}, R_{CO} and R_{SD} are the overlap resistance, the extension resistance, the contact resistance, and the S/D series resistance, respectively. (b) Evolution of the components of the total series resistance for 90 nm, 65 nm and 45 nm CMOS technology [2].

them in a consistent process according to the requirements of IC mass-production are also discussed in this introduction. Lastly, the outline of the thesis is also given.

1.1 Formation of ultrashallow silicon junctions

The downscaling of microelectronic device and circuit dimensions has been amazingly successful since the first scaling principle was introduced by Moore in the early 1970s [4]. The reduction of the cost per functionality accompanying the performance enhancement of CMOS devices (Figure 1.1) has been the general driving force for shrinking the MOSFET node [5]. From devices with channel lengths of several microns in the late 1970s to devices with channel lengths of few tens of nanometers today, the improvement has followed an exponential path and has been supported by the impressive developments of lithography equipment and

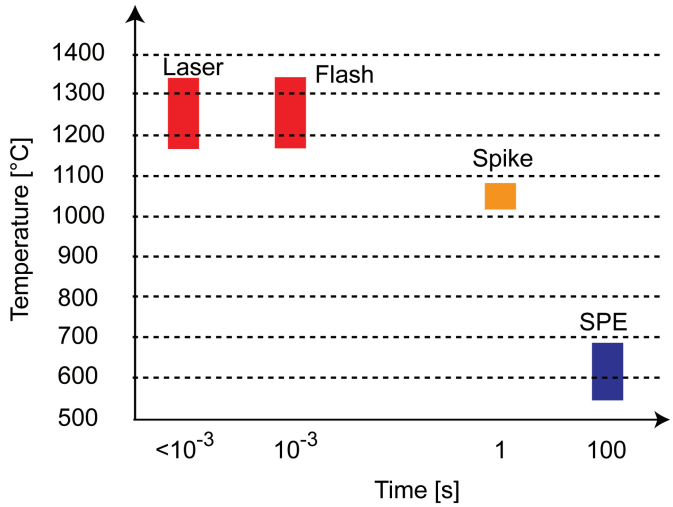


Figure 1.3: Illustration of the annealing-time and -temperature for the different ultrashallow junction formation techniques.

advances in the material science used to fabricate the devices [6].

The continuing improvements in density and speed of CMOS devices pose special challenges for the incorporation of electrically active dopants, particularly in the S/D regions. The requirements established by the International Technology Roadmap for Semiconductors (ITRS) [7] for the S/D regions can be summarized as follows: (*i*) Si junctions with depths below 10 nm are needed in order to minimize the short channel effects, (*ii*) high concentrations of electrically active dopants ($\gg 10^{20}$ cm^{-3}) are required to decrease the contact resistance and minimize the parasitic resistance of the transistor, as shown in Figure 1.2. The latter point is crucial because improvements in mobility of the channel combined with reduction of the length are making the on-state resistance increasingly limited by the parasitic resistance rather than the channel resistance [8].

Several approaches have been proposed for meeting the ITRS requirements (Figure 1.3): low-energy implants activated by flash or laser anneals, or low temperature thermal treatment to achieve solid-phase regrowth of amorphized Si regions [9, 10]. In all these techniques, high-temperature long time annealing steps have been gradually replaced by low thermal-budget processes in order to reduce the ion implantation induced transient-enhanced diffusion (TED) [11]. This phe-

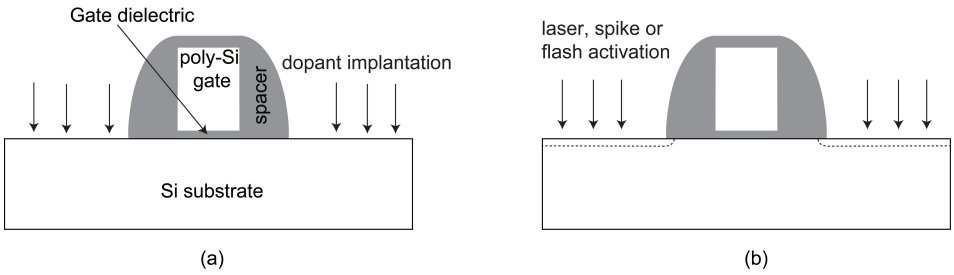


Figure 1.4: Schematic of the formation of S/D junctions by implantation and RTP-assisted activation.

nomenon, caused by defects in the silicon after implantation, results in enhanced defect-assisted ion diffusion during the very early stages of thermal activation. Diffusion coefficients a few orders of magnitude higher than the intrinsic equilibrium value have been observed for boron and have forced very strong limitations on the fabrication of ultrashallow junctions for sub-65 nm PMOS transistors, in which the boron-TED is mainly responsible for dopant motion [12]. Moreover, in BiCMOS technology, the processing of such junctions without inducing TED of the bipolar device doping profiles is crucial for attaining cut-off frequencies in the 100 to 400 GHz range [10]. The currently-used techniques to form ultrashallow junctions for S/D regions are described in more details in the following sections.

1.1.1 Dopant implantation and thermal activation

Ion-implantation can provide very high concentrations of dopants in shallow layers but it has become increasingly difficult to make the dopants electrically active while still restricting dopant diffusion during anneal. Until recently, downward scaling of junction depths could mainly be accomplished by changing the annealing temperature, the implantation dose, or the annealing technique in order to reduce the thermal budget. In more recent years, there has been a rise of interest in advanced methods for forming ultrashallow junctions, with a particularly strong focus on the challenge of boron doping, because of it fast diffusion characteristics. Relatively conventional paths include rapid-thermal processes (RTP) such as spike annealing, especially in combination with the co-implantation of electrically inert species, such as carbon (C) or fluorine (F), which reduce the dif-

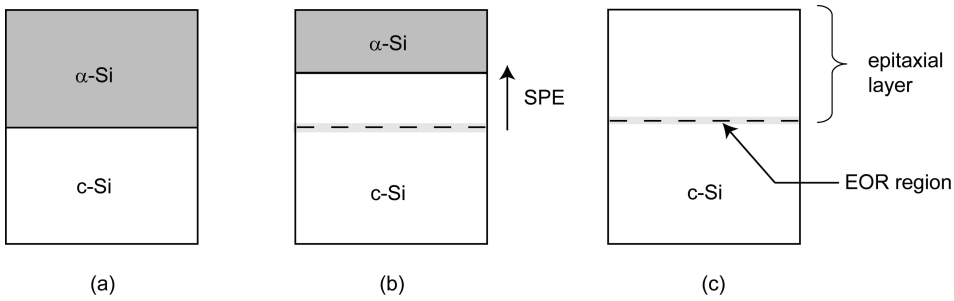


Figure 1.5: Schematic of the solid-phase epitaxy of an amorphous Si thin film on a single crystal substrate. The amorphous Si region is generally formed by Si^+ and boron-dopant implantation. It can also be formed by physical vapor deposition of an amorphous Si layer.

fusion of dopants (Figure 1.4). However, to apply the latter technique in a device technology to reach the requirements of the ITRS roadmap will always require an accurate tuning of the co-implantation to find the appropriate process window and to achieve performance improvements of the actual device [13].

The challenges of the ITRS for S/D regions have also stimulated research into much shorter anneals performed at very high temperatures. Conventional RTP systems heat the wafer isothermally and the rate of heat loss from the wafer's surfaces limits spike anneals to a > 0.5 s duration. A shorter heating cycle can be achieved by delivering a pulse of heat to the wafer's surface where the devices are formed, followed by very rapid conductive cooling to the substrate, which acts as a heat sink. This method gives heating cycles with durations from tens of milliseconds all the way down to nanoseconds. Nanosecond duration heating typically requires the use of pulsed lasers, which can deliver the extremely high power needed [14].

1.1.2 Solid-phase epitaxy

An alternative to achieve both the junction depth and high dopant activation level needed is the solid-phase epitaxy (SPE) of implanted regions during which epitaxial recrystallization of the amorphized Si regions occurs, whereby the incorporation and activation of dopants on lattice sites is achieved. The basic SPE

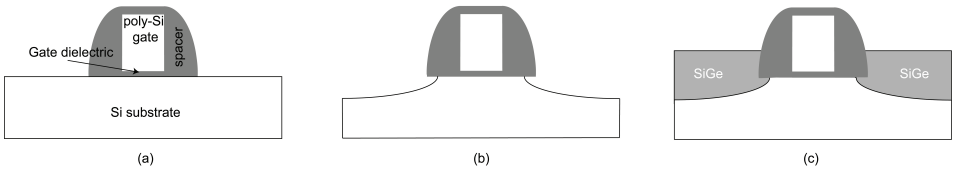


Figure 1.6: Schematic of S/D junction formation by Si or SiGe epitaxial regrowth. (a) Formation of the gate dielectric, gate contact and SiN_x spacer. (b) Definition of the elevated contact (c) Selective epitaxial Si or SiGe re-growth.

sequence is shown in Figure 1.5. The SPE growth process generally occurs when a metastable amorphous material, in contact with a single crystal template, crystallizes epitaxially in the solid state by the rearrangement of atoms at the interface between the two phases. In practice, the SPE-Si is formed by low-temperature regrowth, typically at temperatures from 550°C to 650°C. For S/D engineering, the SPE technique presents several noteworthy aspects: the main advantages of the SPE technique are the minimal dopant diffusion and consequently a good control over the junction depth, the compatibility with high-k and metal gate thermal budget requirements, and the very high degree of electrical activation, often above-equilibrium activation of substitutionally-incorporated dopants [15]. The latter is possible due to a lower activation energy and the absence of a kick-out mechanism as required for conventional thermally-induced dopant activation [16]. The drawback of this method is essentially related to the high density of residual defects in the end-of-range (EOR) region which is located just below the original position of the amorphous to crystalline interface [17]. These defects can greatly increase the junction leakage current and can also release silicon interstitials during subsequent thermal processing, causing TED of dopants and deactivation of previously active dopants. The thermal budget of post-SPE-anneal processing is then limited.

1.1.3 Chemical-vapor-deposited selective epitaxial regrowth

The recent incorporation of silicon germanium (SiGe) in the silicon-based processes for SiGe heterojunction bipolar transistors (HBTs) [18], SiGe BiCMOS [19], and strained Si/SiGe MOSFETs [20] has also motivated low thermal budget techniques for forming shallow junctions. Several studies have also demonstrated

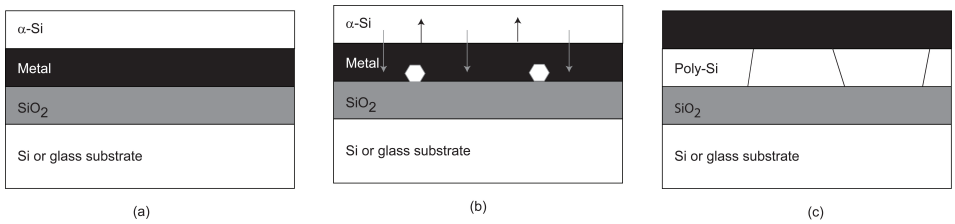


Figure 1.7: Schematic cross-section of the Si MIC process: (a) initial layer stack, (b) polycrystalline Si nucleation, (c) complete layer inversion.

that the extension implantation can be replaced by a chemical vapor deposited (CVD) selective epitaxial growth (SEG) of in situ B-doped Si or SiGe elevated S/D [20]. Indeed, Gannavaram *et al.* proposed in 2000 a new technology to address the challenges of the ITRS roadmap in the S/D regions [21]. This technique consists of isotropic Si plasma etching to define the S/D extension region to be elevated, followed by in-situ-doped selective epitaxial Si or SiGe regrowth. The replacement of Si by SiGe leads to a reduced metal–semiconductor barrier height. Furthermore, the in-situ doped SiGe growth at low temperatures enables enhancement of the active boron incorporation, compared to conventional implantation and thermal activation or Si regrowth. Indeed, the variable Ge fraction makes it possible to decrease the resistivity further, since SiGe layers can incorporate more B than pure Si [22]. Nevertheless it introduces an additional restriction on the thermal budget to keep a good crystalline quality of the strained Si and SiGe films: the first is the development of surface undulations (or roughing) from high growth temperature [23] and the second is the diffusion of the germanium [24]. Moreover, the elevated S/D gives extra-Si material for the silicidation process that is used in conventional CMOS to form the contact to the transistors regions. A possible drawback of the process is the formation of crystal defects during the first step, i.e., the plasma etching.

1.2 Metal-induced crystallization of silicon

Generally driven by the reduction in Gibbs free energy, the crystallization of amorphous silicon (α-Si) can be energetically enhanced by the presence of a metal

Table 1.1: List of metal/α-Si with their eutectic temperature (T_E) and crystallization temperature (T_C) [25].

Metal	T_E (°C)	T_C (°C)
Al	577	150
Ag	830	350
Au	360	130
Sb	630	430
Cu	802	485
Ni	964	500

layer. In this section, we describe two different techniques in which this phenomenon has been applied to form crystalline Si regions using processing temperatures below 500°C.

1.2.1 Polycrystalline silicon islands on dielectric

In the case of α-Si crystallization on dielectrics by using an intermediate metal layer, the growth mechanism has been referred in the literature as metal-induced crystallization (MIC) [27]. This technique, leading to the formation of polycrystalline Si thin films on SiO_2 or glass substrates, has been intensively investigated over the past decades for many metal/Si systems. The Table 1.1 lists the investigated Si/metal binary systems with their eutectic temperature and the corresponding MIC temperature. In particular, the cases of Ni [28] and Al [29] have attracted a lot of attention due to their overall compatibility with CMOS processes and the controllability of the as-formed Si grain orientation. The activation energy for solid-phase crystallization of α-Si of about 2.7 eV [30] is reduced to about 0.8 eV when α-Si is in contact with Al [31]. The basic mechanism of the MIC process is shown in Figure 1.7. The MIC sequence can be, in first instance, decomposed into the following consecutive steps: (*i*) the diffusion of Si through the metal-transport layer, (*ii*) the nucleation on the dielectric, (*iii*) the growth of polycrystalline Si grain and segregation of the metal layer at the surface, which eventually leads to the complete inversion of the metal and Si layer positions with respect to each other (Figure 1.8). To describe the growth of polycrystalline Si on SiO_2 or foreign

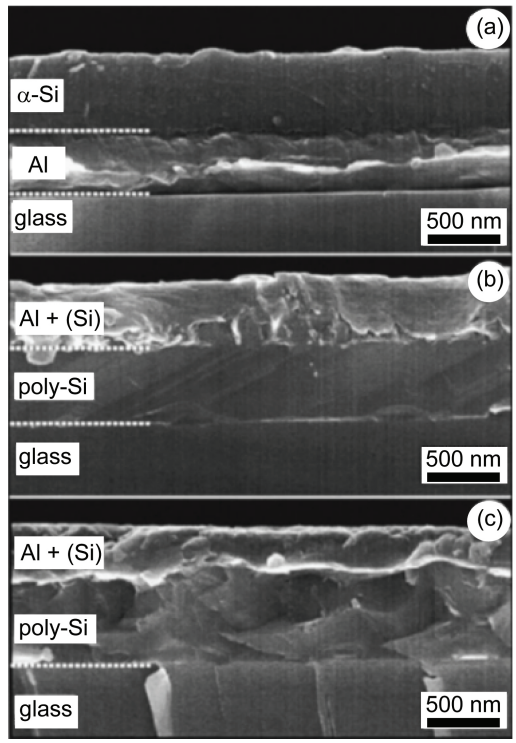


Figure 1.8: Cross-section SEM micrographs of a Si/Al/glass structure: (a) before annealing. (b) after annealing for 60 min at 500°C. (c) after annealing for 60 min at 600°C. The short white dotted lines are to guide the eye [26].

substrates such as glass, an Al/α-Si layer exchange-based mechanism of crystallization has been proposed by Nast *et al.* and generally accepted [26]. In this case, the results show it is possible to use this technique on glass or SiO_2 substrates to form a few-micron large polycrystalline Si grains. This method has been intensively used to fabricate devices such as solar cells and thin-film transistors (TFTs) on low-cost substrates. Particularly, the location-controllability of the as-grown polycrystalline Si grain boundaries has been a research focus for devices such as TFTs since the possibility to engineer the TFT source, drain and channel regions far enough from the grain boundaries can improve the device performance.

1.2.2 Metal-catalyzed silicon nanowires

For more aggressive downscaling, recent breakthroughs in nanoscale structures also offer a new approach for the formation of high-crystallinity ultra-abrupt Si regions at low temperature. Semiconducting NWs are typically 1-dimensional pillar-shaped nanostructures, of a diameter in the range of 10 nm to 100 nm and a length of several microns [32]. Semiconducting NWs can either be formed by an epitaxial growth process (the so-called "bottom-up" approach) or by the use of mask patterning and reactive ion etching (RIE) (generally referred as the "top-bottom" approach).

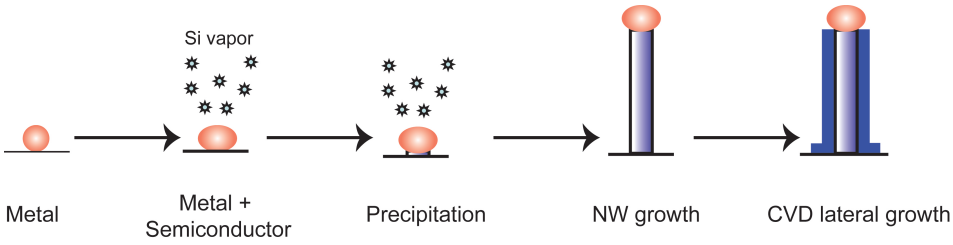


Figure 1.9: Schematic representation of VLS-assisted NW growth.

Several bottom-up approaches have been reported using chemical vapor deposition (CVD) [33], electrochemical deposition [34], or the so-called vapor-liquid-solid (VLS) techniques and a large variety of semiconducting or metallic NW, such as indium phosphate [35], gallium nitride [36], germanium [33], silicon [37], or gold [38] have been successfully formed. Among the other methods, the VLS has attracted particular attention due to the recent focus on systematic nanostructure fabrication techniques combined to the progress in the formation of nanoscale particles.

The VLS-assisted crystal synthesis was first proposed by Wagner *et al.* in 1964 for the growth of silicon whiskers with diameters from 100 nm to hundreds of microns [39], and then thermodynamically described in more detail by Givargizov in 1975 [40]. In the VLS process, a metal particle is used as a catalyst and the growth itself is induced by the incorporation of a vapor-phase Si precursor into liquid catalyst particles until supersaturation is achieved and a single crystal is grown.

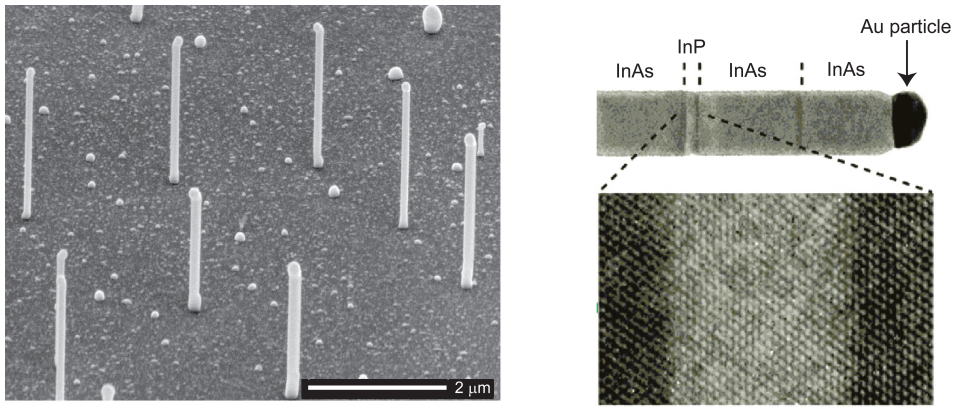


Figure 1.10: (a) SEM micrograph of semiconducting nanowires obtained by VLS [41]. (b) High resolution TEM view of InP/InAs abrupt transition [42].

The general VLS-assisted NW growth sequence, in the case of Si, is shown in Figure 1.9. First, nanosized metallic particles are formed on Si substrate. These particles are generally formed by laser ablation [43] or by the annealing of a few atom layers of metallic film above the eutectic temperature in order to break the film into discrete islands [44]. The chemical and physical properties of the metal catalyst are critical for the VLS process. The ideal candidate for the metal catalyst must be physically non active and chemically active. Because the Au/Si binary alloy does not oxidize and has a low-eutectic temperature, gold Au catalysts are frequently used. The diameter of the metal catalyst is typically in the range of 10 to 50 nm (Figure 1.10). The source material carrier gas, generally silane (SiH_4) or tetrachlorosilane ($SiCl_4$) in a mixture of nitrogen (N_2) and hydrogen (H_2) in the case of Si NW growth, is then introduced into the growth chamber. The background pressure is used to control the catalyst size, and the temperature of the tube is maintained above the binary alloy eutectic temperature. Table 1.2 shows several binary systems reported for the VLS synthesis of semiconducting NWs and their corresponding growth temperature. After Si precursor decomposition, Si atoms diffuse through the catalyst droplets. When the eutectic alloy becomes saturated, Si precipitates at the liquid-solid interface: this is the precipitation stage. The growth occurs only at the location of the liquid metallic catalyst because the stick-

ing coefficient is higher on liquid than solid surfaces. Anisotropic growth goes on while the gas flow is maintained; this step is the "elongation" or the growth itself. At the end of the process, high purity Si NWs are obtained except at one tip, which contains the solidified metallic catalyst [45]. Moreover, a thin layer of native SiO_2 often covers the whole structure. This is mainly due to air ambient native oxidation or remnants of oxygen in the tube. In spite of their remarkable properties

Table 1.2: Eutectic temperature (T_E) of commonly-used alloys.

Alloys	T_E (°C)
Au / Si	360
Au / Ge	360
Au / GaAs	630

and low processing temperatures, which make this technology very appealing for many applications, not all of the VLS-NWs can be incorporated in a straightforward way into a fully-CMOS compatible process. Indeed, materials such as Au or Fe, known to be excellent growth catalysts, are not compatible with front-end Si processing. They have high diffusivity into Si and due to mid bandgap states cause dramatic deterioration of the device performance. Recently, Wang *et al.* opened new perspectives for the incorporation of NWs into CMOS device flowchart by reporting, for the first time, the growth of Si NWs catalyzed by Al [46]. However, the ability to control the dimensions and the position of the NWs, which is an essential requirement for future IC applications, is not provided by a purely bottom-up growth mechanism. In order to grow NWs at a precise location, studies are currently proceeding to learn how to control the position of the catalyst nanoscaled droplets. Moreover, there is some controversy in the literature concerning VLS growth. Indeed, Dick *et al.* have intensively investigated the growth of III-V nanowires, obtained by metalorganic vapor-phase-epitaxy (MOVPE) at low-temperature and have demonstrated that the metal catalyst never reaches the liquid phase during the growth sequence [47]. This confirmed observations reported earlier by Sharma *et al.* who studied the synthesis of titanium-catalyzed silicon NWs at temperature of about 600°C, which is far below the eutectic tem-

perature of Ti/Si alloys, known to be above 1000°C [48]. These phenomena are not entirely explained by a standard VLS synthesis, and in parallel, a so-called "vapor-solid-solid" (VSS) mechanism is often proposed to explain these experimental observations [49].

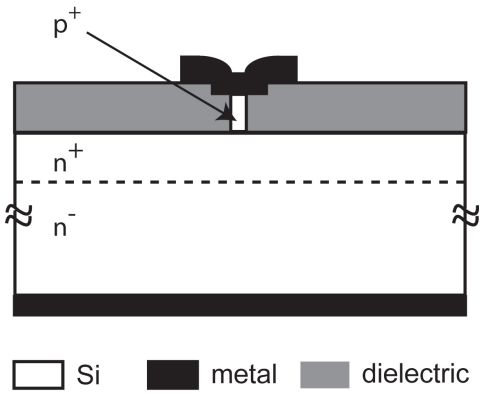


Figure 1.11: Cross section schematic of the simulated p^+-n diode. The junction between the p^+ and n^+ regions is in this case located at the substrate to pillar interface.

1.2.3 Silicon nanowire device behavior

Besides the potential for device integration, making nanowire devices is also confronted with several issues. An example of one of the problems that was examined as a part of this thesis is related to the methods used to contact them. The electrical behavior of a through-wafer contacted Si pillar-like p^+-n junction embedded in dielectric material was simulated using the MEDICI device modeling tool (Figure 1.11). In all cases, the doping of the p^+ and n^+ region is 10^{18} cm^{-3} and 10^{17} cm^{-3}, respectively. As compared to conventional micron-wide planar junctions, the depletion region in reversed bias ($V_D = -0.5V$) becomes wider at the boundary with the surrounding dielectric when the junction area A_J is reduced to the sub-100 nm range. This is explained by considering the continuity of electric displacement, which is defined as shown in the relation $\mathbf{D} \approx \varepsilon \cdot \varepsilon_0 \cdot \mathbf{E}$, in which $\mathbf{D}$, ε, ε_0, and $\mathbf{E}$ are, respectively, the electric displacement, the permittivity of the material, the permittivity of free-space and the electric field.

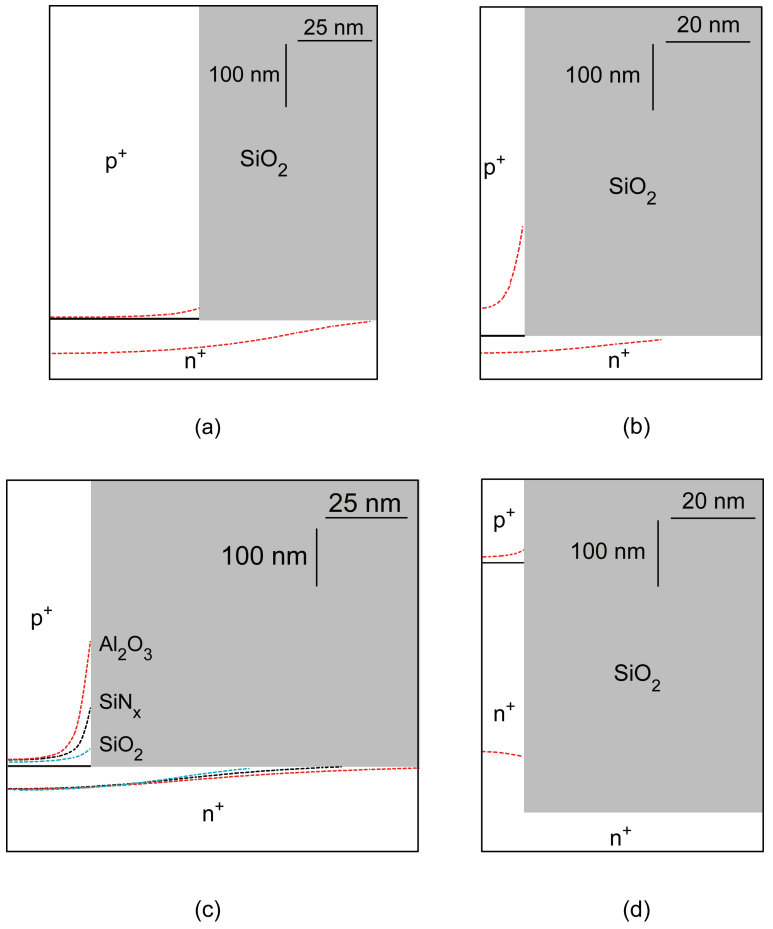


Figure 1.12: MEDICI simulation results showing the edges of the depletion region when the width of the p^+ Si pillar is: (a) 100 nm or (b) 20 nm. In both cases, the dielectric material is SiO_2. In the (c) the pillar is 50 nm wide for different dielectric materials. (d) 20 nm and the junction is located within the pillar. The solid line indicates the position of the junction.

An interesting consequence of the diameter reduction is the higher breakdown voltage compared to a bulk device with the same doping profile. This has been verified for different dielectric materials: structures using SiO_2, SiN_x, and Al_2O_3, with the corresponding permittivity ε of 3.9, 7.5 and 12 respectively, have been simulated. The results demonstrate the width of the depletion region at the edges increases as the dielectric constant of the surrounding insulator increases. This

has been experimentally verified by Agarwal *et al.* for Si nanoscale pillars formed by a state-of-the-art reactive-ion etching process [50].

When the lateral dimension of the device comes into the sub-100-nm range, the depletion region width is also determined by the position of the p^+-n junction in the pillar. The effects of the surrounding dielectric material become, in that case, predominant. Consequently, a nanoscale p^+-n junction inside the Si pillar has a much wider depletion region and consequently a higher breakdown voltage compared to a structure in which the junction is at the interface between the small structure and the Si substrate, as shown in Figure 1.12. This analysis demonstrates the current limits of Si NW-based transistor and the urgent need to develop entirely new approaches and concepts to contact them.

1.3 This thesis

In view of the general trends in the field of junction formation, the need of reliable techniques of forming ultra-abrupt ultrashallow junctions directly usable for devices remains very important. Considering the many issues to be solved for further integration, and despite a lot of promises, Si NWs do not seem to be a short-term alternative. The VLS (or VSS) technique forces also the IC technologists and designers to imagine an entirely new device architecture to be able to fully exploit the potentiality of the SiNWs. The Al-mediated SPE technique which is presented in this study presents many remarkable properties, in terms of process reliability, reproducibility, controllability, and material quality. Entirely CMOS compatible and directly usable in devices, the SPE-Si modules appear as a very promising candidate for further integration of ultrashallow abrupt junctions into both front- and back-end processings.

This thesis is organized as follows: in Chapter 2, a semi-empirical model based on phenomena observed at different growth stages and for different configurations is proposed. The understanding of the growth mechanism, leading to a better controllability of the overall process enables the fabrication of test-structures to characterize Si obtained by SPE. The results of analytical characterization to determine the material crystallinity, orientation, doping concentration and abruptness, and controllability of the overall SPE process, are addressed in more detail in Chapter 3. Chapter 4 deals with the results obtained by using SPE

in alternative configurations. Particularly, the ability to grow high-quality Si on arbitrarily-shaped contact windows, and to control the lateral overgrowth, leading to the formation of a high-crystallinity silicon on insulator region. In Chapter 5, the results of the electrical characterization of simple SPE-Si-based devices such as p^+ contacts, p^+-n diodes, and p-n-p bipolar junction transistors are presented. Chapter 6 gives the main conclusions of this work and the recommendations for future investigations.

Chapter 2

Aluminum-mediated SPE-silicon growth mechanism

2.1 Introduction

In this chapter, the mechanisms governing the SPE-Si growth are investigated. By intensively studying the growth parameters, such as temperature, growth time and layer properties, the early growth stages were successfully identified, and a better understanding of the growth phenomenon, and thus an improved controllability of the overall SPE-Si deposition was achieved. The central role of the Al transport layer in the growth sequence is addressed in this chapter and an SPE-Si growth optimization is also proposed by taking into account the influence on the epitaxial selectivity of the window-to-Si etching technique, the dielectric surface conditions and the Si substrate orientation.

2.2 Experimental procedures

In the experiments, the SPE is performed on bare Si wafers with (100), (110) or (111) orientation. However, in the bulk of the experiments, (100)-Si substrates are patterned with contact windows to the Si through a 30-nm-thermally grown silicon dioxide (SiO_2). In all cases, the preparation of the samples before the SPE growth sequence is as follows: the Si surface was first cleaned in a nitric acid solution (HNO_3) and the resulting native SiO_2 was removed by dip-etching

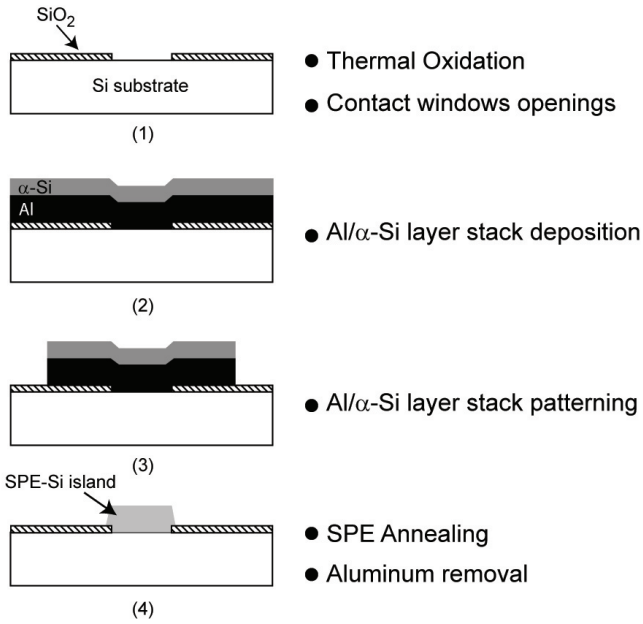


Figure 2.1: Schematic process fabrication flow of the SPE-Si growth test structures. After growth and Al removal, the SPE-Si islands are localized in contact openings etched through the SiO_2.

in diluted hydrofluoric acid (HF) 0.55% for 4 min, which provides a hydrogen-terminated surface passivation. Directly after dip-etching, wafer rinsing, and drying, a layer stack of Al (containing 1% Si) and α-Si was formed by physical vapor deposition (PVD) at 50°C. The two successive PVD depositions were performed using an argon flow of 100 sscm and without breaking the vacuum in order to prevent the formation of an insulating native aluminum oxide (Al_2O_3) layer at the α-Si to metal layer interface. The influence of an Al_2O_3 layer between the PVD thin films has already been investigated by many research groups for the case of aluminum-induced Si crystallization on SiO_2. Particularly, Schneider *et al.* showed that the presence of such an insulating interface affects the growth by introducing a diffusion barrier for the Si transport, and thus results in slower crystallization of α-Si [51] and larger polycrystalline Si islands. The influence of such Al_2O_3 layers was not investigated in this study. Unless explicitly mentioned, the results presented here correspond to thicknesses of the deposited Al and α-Si thin

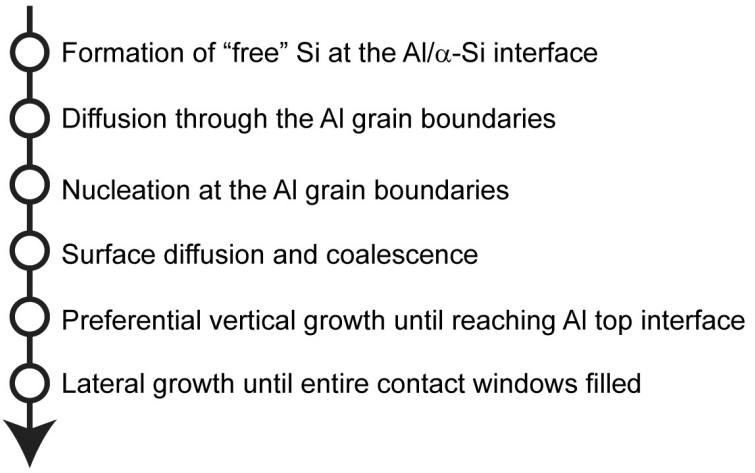


Figure 2.2: The aluminum-mediated SPE-Si growth sequence.

films of 200 nm and 20 nm, respectively. On the samples with contact windows through the SiO_2, the layer-stack was patterned in variable-width islands around the contact windows, as shown in Figure 2.1. The samples were transferred to the annealing module, in which a thermal treatment in argon was performed for 1.5 min, 2 min or 6 min at either 400°C or 500°C. After annealing, the Al layer was removed selectively to Si and SiO_2, using a conventional metal-etchant solution. The as-obtained surfaces were then analyzed by scanning electron microscope (SEM) in order to identify the successive stages of the growth sequence and to determine the dependence of the SPE-Si surface coverage on parameters such as the growth time, the Si source composition and the substrate orientation.

2.3 Basic growth mechanism

From these types of experiments, it has been possible to conclude that the growth sequence is composed of the following consecutive steps, as given in Figure 2.2: 1) formation of “free” Si at the Al/α-Si interface, 2) diffusion of Si along the Al grain boundaries, 3) nucleation at the Si substrate surface, 4) nuclei rearrangement and 5) crystal growth. A series of SEM images that illustrate the different stages of the SPE-crystal growth is compiled in Figure 2.3. Each of these stages

is addressed below in more detail.

2.3.1 Formation of "free" Si

As described by Hiraki's model, free electrons in the Al layer adjacent to the α-Si first screen the Si covalent bonding and thus weaken the Si–Si bonds [52]. The relatively weakly-bonded Si atoms are called "free" Si because of their ability to migrate through the Al layer. It is generally accepted that such a screening effect only acts over a short-range and will be restricted to the first two atomic monolayers of the α-Si layer. The formation of such "free" Si atoms is indirectly substantiated by the experimental observation that, after annealing of the Al/α-Si layer stack, only a surface coverage of Al appears on the test structures, i.e., the deposited α-Si has dissolved and diffused through the metal film.

2.3.2 Diffusion along the Al grain boundaries

The Al layer, deposited by PVD at 50°C and using an argon pressure of 4 mTorr, is microcrystalline and contains a high density of grain boundaries [53]. Thus, Si can diffuse either *(i)* through the Al grains, *(ii)* along the Al grain boundaries, *(iii)* along the Al to α-Si interface, or (*iv*) along the Al to Si substrate interface. The diffusion path along the Al grain boundaries is known to be predominant in the early stages of thermal treatment of Al/Si alloys [54]. Thermodynamically, the occurrence of Si diffusion along the Al grain boundaries is governed by the difference (2.1) between the interface energies:

$$2 \cdot \gamma_{<Al>-\{Si\}} - \gamma_{<Al>} \tag{2.1}$$

where $\gamma_{<Al>-\{Si\}}$ is the interface energy between the Al and α-Si layers, $\gamma_{<Al>}$ is the grain boundary energy of Al. Following methods previously reported by Wang *et al.*, $\gamma_{<Al>-\{Si\}}$ and $\gamma_{<Al>}$ were calculated at 500°C, and found to be 2.85×10^{-2} J·m^{-2} and 3.5×10^{-1} J·m^{-2}, respectively [55]. This establishes that there is a positive driving force for the inward diffusion of Si along the Al grain boundaries. A preference for the diffusion of the Si along the Al grain boundaries is manifested by the shape and overall pattern of the deposited Si in the coalescence stage discussed below.

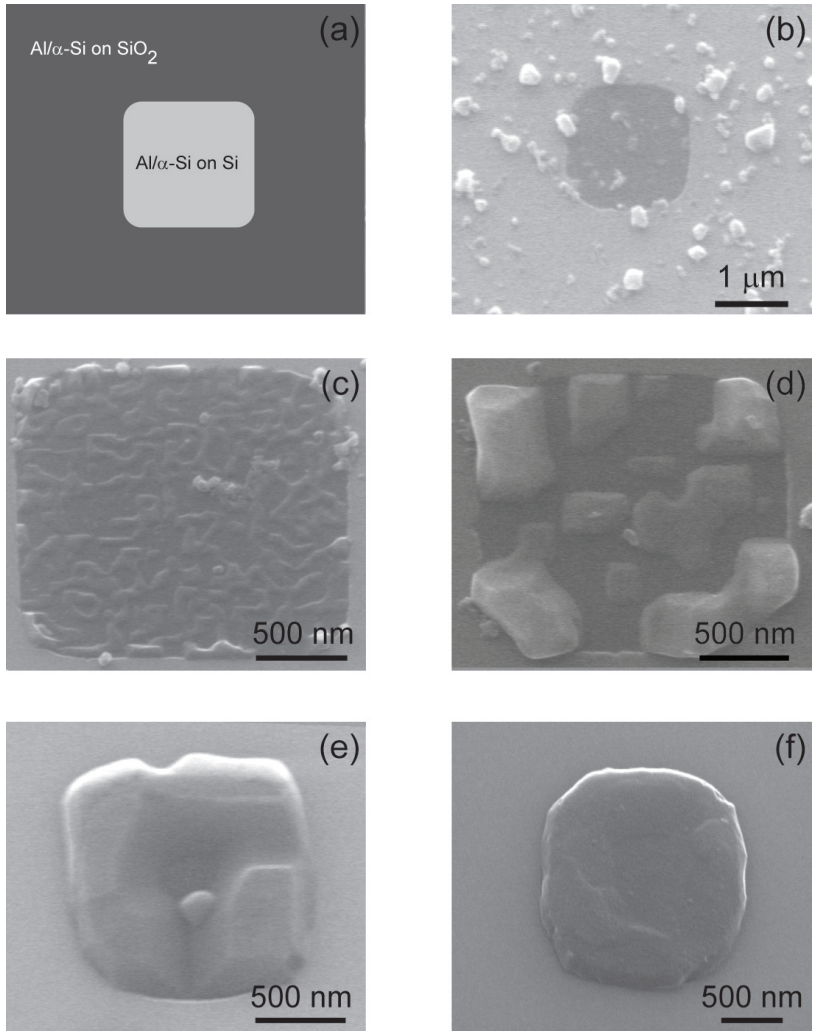


Figure 2.3: (a) Schematic top-view of the SPE-Si test structure after Al/α-Si layer stack deposition and patterning. SEM micrographs of contact windows for different growth times: (b) 1.5 min at 400°C, (c) 2 min at 400°C, (d) 6 min at 500°C, (e) 30 min at 500°C; the Si dissolved into the Al in the vicinity of the contact windows is not sufficient to entirely fill the contact windows, (f) 30 min at 500°C with optimal Al/α-Si layer stack geometry and thickness ratio.

2.3.3 Nucleation and coalescence

He *et al.* reported the existence of a critical Si thickness, h_c, above which Si crystallizes [56]. The value of h_c depends on the crystallization energy of α-Si, $\Delta G_{<Si>-\{Si\}}$, and on the interface energy of Al with respect to amorphous and crystalline Si interface, $\gamma_{<Al>-\{Si\}}$ and $\gamma_{<Al>-<Si>}$ respectively, as given by the relation (2.2)

$$h_c = \frac{2 \cdot \gamma_{<Al>-<Si>} - \gamma_{<Al>-\{Si\}}}{-\Delta G_{<Si>-\{Si\}}} \tag{2.2}$$

In our case h_c is about 0.56 nm, which corresponds to approximately 2.5 atomic monolayers, i.e., much smaller than the thickness of the deposited α-Si thin film. Accordingly, α-Si does not remain in a stable amorphous phase at the grain boundaries and will crystallize upon reaching the Si or SiO_2 surface. This nucleation stage of the growth process was observed in our experiments after an annealing time of 1.5 min at 400°C. It is characterized by a fine distribution of deposited Si nuclei, with no preferential orientation, both on the Si substrate and the SiO_2 (Figure 2.3b). As the Si diffusion along the grain boundaries progresses, both the number and the size of the Si nuclei increases until they impinge upon each other and merge. At 400°C, the diffusion process is slow enough to allow the intermediate coalescence stage to be observed. This is shown in the SEM image in Figure 2.3c, where the nucleated islands have coalesced to form a liquid-like pattern [57] that follows the Al grain boundaries. This is a strong evidence of the predominance of the diffusion along the Al grain boundaries in the early stages of the growth process, as predicted by equation (2.1).

2.3.4 Growth on non-patterned substrates

After nuclei coalescence, larger Si crystals will form because the formation of additional Si–Si bonds corresponds to a lowering in energy. Quantitatively, this energy gain corresponds to the energy necessary for a new Si facet to be attached to the already formed Si crystal. To do so, four new Si–Si bonds have to be formed per unit cell (Figure 2.4). By the use of the binding energy given by the Tersoff potential [58] for bulk Si of about $\sim$ -4.62 eV, and assuming a facet width of 0.54 nm, the energy gain corresponding to the formation of a new SPE-Si facet is

approximately $\sim$ -2.5 J·m^{-2}, which is much larger than the gain in energy from the formation of a Si to Al interface bond. This also means that there will be a tendency for the system to form large crystals since the free energy per atom (or per unit volume) decreases as the crystal volume increases.

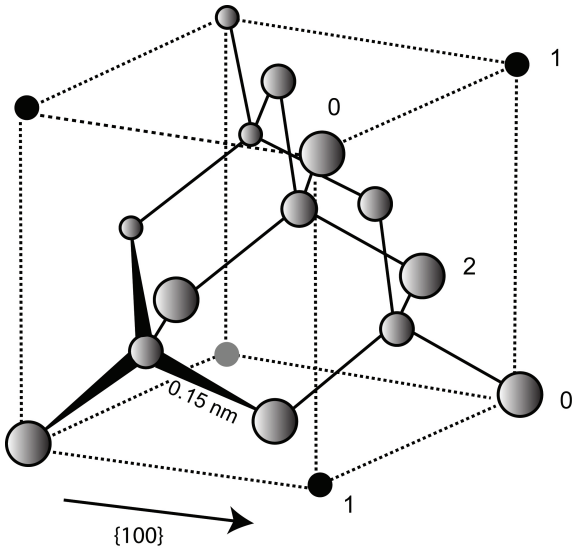


Figure 2.4: Schematic 3D-view of a diamond Si lattice. The numbers indicate the bonds necessary for a new Si facet to be attached.

An investigation of the crystal growth as a function of substrate orientation gives very clear information on the preferred growth directions and the role of the Al layer. The influence of the substrate orientation on the SPE has been investigated in the literature and few already-proposed models have demonstrated that the fastest growth rate is along the <100> directions [59]. In particular, Drosd *et al.* formulated that the main criterion for Si in the amorphous phase to crystallize is the formation of at least two undistorted bonds with the crystal [60]. On the basis of geometrical considerations, it can be concluded that this requirement is easily met in the (100) plane because one incoming Si atom can establish the necessary bonds. Along the (110) or (111) planes, however, the growth will be much slower because the bonds can only be achieved by the formation of a cluster of two or three atoms, respectively (Figure 2.5). Several of our experiments display behavior that can be well understood in the terms of this crystal growth criterion

and they are described below.

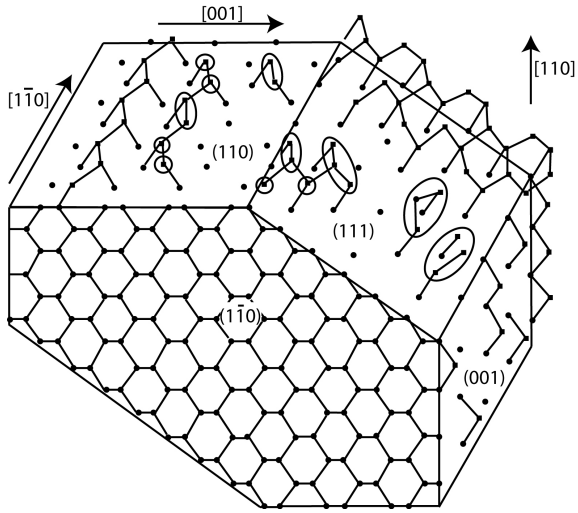


Figure 2.5: Schematic drawing of the growth process on the major surfaces of a diamond cubic crystal [60].

In Figure 2.6, SEM images are shown of the results of SPE growth on non-patterned substrates with an orientation of either (100), (110) or (111) as obtained when annealing at 400°C for 30 min.

The analysis of the (100) substrate after growth and Al removal shows that the SPE forms rectangular Si-islands with sides parallel to the $\{110\}$ directions and with a height that is equal to that of the originally deposited Al layer as shown in Figure 2.6a. This is in agreement with a fastest growth rate in the $<100>$ directions because the direction perpendicular to the Si substrate surface is a $<100>$ direction. Moreover, according to the well-established Wulff's theory, the end-shape of a growing crystal is determined by the slowest growth direction [61]. Thus, the fact that $\{110\}$ facets are exposed in the final growth stage also indicates a slower growth in the $\{110\}$ than in $\{100\}$ direction. When the total surface occupied by SPE-Si islands is integrated for the situation shown in Figure 2.6a and the island height is assumed to be within 7% of the deposited Al thickness, a total volume is found that corresponds well to the deposited volume of α-Si. This indicates that practically all the deposited α-Si is crystallized by SPE. The vertical growth apparently stops when the SPE Si height has reached the initial Al layer

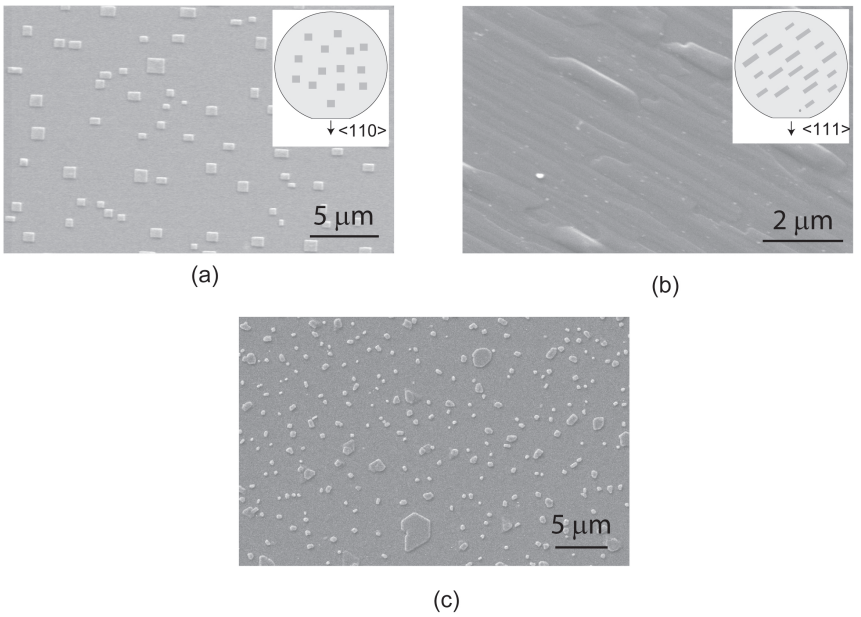


Figure 2.6: SEM micrographs showing the bare-Si substrate surface after SPE-Si growth and Al removal in the case of (a) (100)-oriented Si substrate. (b) (110)-oriented Si substrate. (c) (111)-oriented Si substrate. In all cases, the growth temperature was 400°C, the annealing time 30 min, and the Al and α-Si layer thicknesses were 200 nm and 20 nm, respectively.

thickness. This feature will be addressed in more detail in the Section 2.3.5, and in Section 2.3.6 the SPE-Si coverage as function of growth time will be analyzed.

The results obtained on (110)-oriented substrates, illustrated by Figure 2.6b, show discontinuous but micron-long stripe-like structures growing along the $<100>$ direction and essentially covering the whole of the sample surface. The height of these structures is about a few tens of nm, which is far below that of the 200 nm Al layer. Therefore, it would appear that the fast growth in the $<100>$ direction has exhausted the supply of Si at the cost of the slower vertical growth in the $<110>$ direction. An electron-back scattering diffraction analysis was performed on the (100)- and (110)-oriented Si samples and it was confirmed that the epitaxially-grown Si preserves, in both case, the orientation of the substrate.

The comparison of the shapes obtained on (100)- and (110)-oriented substrates (squares and rectangles, respectively) can be interpreted as the result of the bal-

ance between Si/Al interface energy and the Al grain boundary energy. The vertical growth of *c*-Si on (100) samples involves the formation of four new Si(110)/Al interfaces. Keeping in mind the relation 2.1, the following relation thus holds:

$$4 \cdot \gamma_{<Al>-<Si_{110}>} - \gamma_{<Al>} \leq 0 \tag{2.3}$$

On the other hand, the rectangular-shaped islands observed on Si(110) wafers tend to grow laterally rather than vertically: since this mechanism involves the creation of only two new Si to Al interfaces, it is an indication that the relation 2.1 is here restricted to

$$2 \cdot \gamma_{<Al>-<Si_{100}>} - \gamma_{<Al>} \leq 0 \tag{2.4}$$

On the (111)-oriented substrate (Figure 2.6c), only $<111>$ directions are available on the surface. Many structures, particularly the small ones, do not exhibit any clearly preferential shapes. The density of islands is much higher and the average island surface area much smaller than for the (100)-substrate situation. This inadequate ability to coalesce into larger crystals is a clear indication that growth in the $<111>$ direction is difficult to initiate. However, to a small degree, island growth similar to that observed on the (100) sample is observed and a few large micron-sized islands can be found. For these it is possible to identify a preference for forming triangular-like shapes incorporating 120° angles and a preferred growth from the corners of the crystals in the three $<111>$ directions is observed. The height of the islands is $\sim$ 180 nm which is in a good agreement with the targeted thickness of the deposited Al (1%Si) layer, i.e., 200 nm.

2.3.5 Growth on patterned (100) substrates

When SPE-Si islands are formed locally within contact windows, the mechanisms governing the SPE growth remain the same as for bare Si. However, as seen in the SEM micrograph presented in Figure 2.3d, the crystals grow predominantly at the contact window perimeter. To clarify this point, a finite element modeling (FEM) analysis was performed to evaluate the strain distribution in the as-formed SPE-Si/SiO_2/Al structure.

The results, illustrated in Figure 2.7, indicate a reduction of the Al thin-film elastic-energy-field by a partial transfer of deformation to the SiO_2 in the region

located along the edges of the contact window. If it is assumed that the incoming Si is kinetically capable of traveling across the whole Al/Si window, the SiO_2/Si interface would correspond, from a lattice deformation point of view, to a local minimum of the Si chemical potential found in the contact window [62] and this results in a preferential diffusion direction for the Si atoms.

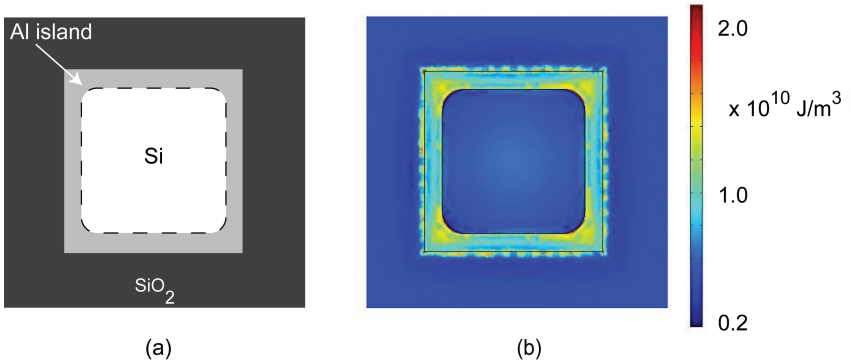


Figure 2.7: Finite-element-modeling results showing the strain distribution in Al thin film covering the contact windows opened through SiO_2, in the case of a fully-strained Al thin-film. The edges of the contact windows correspond to a reduction of Al thin-film-elastic-energy field by a partial transfer of deformation to the SiO_2 in the region located along the edges of the contact windows.

Moreover, the nucleation of *c*-Si at the window perimeter corresponds to the substitution of an SiO_2/Al interface with an SiO_2/SPE-Si plus an SPE-Si/Al interface. The corresponding surface energies are 0.15 J·m^{-2} and 0.3 J·m^{-2}, respectively [63]. Since the SiO_2/SPE-Si interface is lower in energy than the SPE-Si/Al interface, it is natural for the system to try to maximize the exposure of the SiO_2/SPE-Si interface per unit volume, as illustrated in Figure 2.8. Thus, it clearly follows from geometrical considerations that the deposition of Si at the corners of the contact windows is favorable.

As also observed on the non-patterned samples, the SPE-Si island thickness is accurately controlled by the height of the initial Al layer. If the growth of the SPE crystal was not limited in height by the Al layer, multi-faceted crystals would be expected to grow in the manner that is commonly observed for other conventional Si epitaxy techniques. This has in fact been observed in the situation where

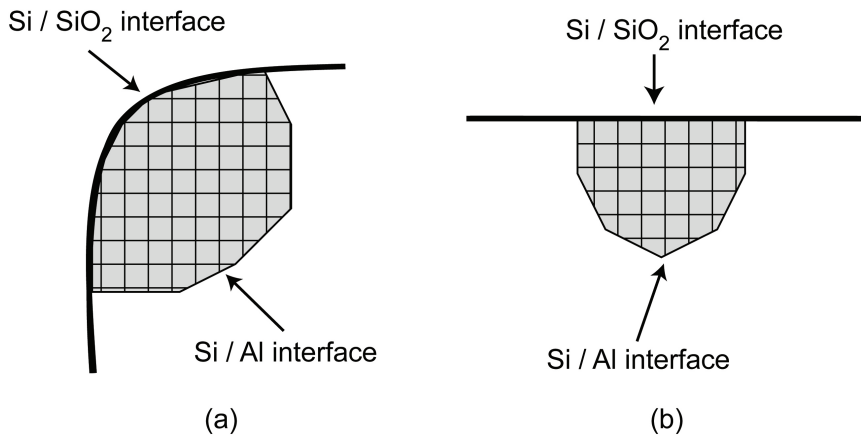


Figure 2.8: Schematic top-view of the SPE-Si deposition within the contact window opened through SiO_2.

the SPE growth is limited by the supplied Si and not the Al thickness. This has been obtained for a combination of a 200-nm-wide contact windows and only the Si supplied from a 200-nm-thick Al (containing 1% Si), without any deposition of additional Si in the form of PVD α-Si. An example of which is presented in Section2.4.4. When a sufficiently large amount of Si is supplied, the vertical growth of SPE-Si, both in the case of bare Si and samples with contact windows through SiO_2 to the Si, stops abruptly when the SPE-Si island reaches the thickness of the initial Al, the multi-faceting is inhibited and rectangular crystals form, among which the larger ones are very close to being perfect squares. This is in agreement with the results previously reported by O. Nast *et al.* for a layer-exchange aluminum-induced crystallization mechanism on glass substrates [64]. Due to the low thickness of α-Si used in our case, only 10% of the Al thickness, the SPE-Si growth is rapidly fed from the sides by diffusion of dissolved Si through the Al layer. During the Si diffusion through Al grains, the Al is segregated on top of the grown SPE-Si island, as it can be seen in Figure 2.9.

Thus, supplying thicker α-Si or wider α-Si islands does not help to form a thicker thin film, since the SPE-Si island height is truncated when it reaches the initial Al layer thickness. The growth is stopped vertically and eventually tooth-like SPE-Si islands are formed, an example of which is shown in Figure 2.3e. A

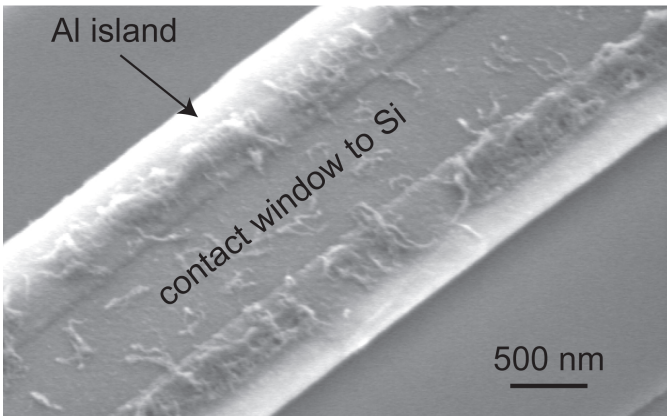


Figure 2.9: SEM micrograph of the contact window after SPE growth. The segregation of rough Al at the surface of the Al island is visible.

very slight dent is also observed in the middle of the island shown in Figure 2.3f, which shows the complete SPE window filling. Such a dent can be the result of the Al topology or due to a lack of Si reaching the center of the structure. This may occur if the supply of Si from the sides is cut off by a completed vertical growth at the window perimeter or if the Si crystallizes on the SiO_2 before reaching the contact window. The latter can be the result of nucleation on the dielectric or due to some (limited) lateral overgrowth of the SiO_2. As far as the Si nuclei on the surface are concerned, they do not play a role as long as the Si is supplied close to the contact window and it is given time enough to diffuse to the contact window.

The high diffusivity of the Si on the SiO_2 can be observed indirectly as a reduction of the Si nuclei density on the exposed SiO_2 surrounding the contact windows as the growth time increases. In Figure 2.10 the situation is shown for four neighboring contact windows covered by a non-patterned Al/α-Si layer-stack. After a 30 min anneal at 500°C a $\sim$ 7 μm-wide SiO_2 region directly around the contact windows is free of Si nuclei.

2.3.6 Surface coverage

The coverage of the contact opening with SPE-Si as a function of annealing temperature and time was extracted from SEM images, the amount of coverage is

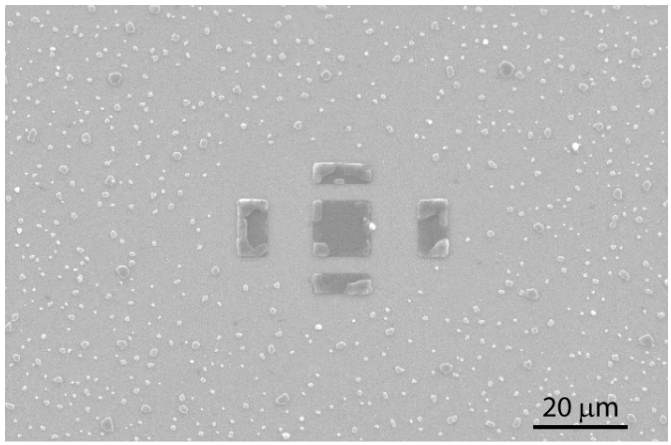


Figure 2.10: SEM micrograph of an Si/SiO_2 surface after 30 min growth at 500°C showing the preferred Si deposition inside the contact windows and the Si surface migration in the vicinity to the contact windows to Si.

plotted for different Al/α-Si layer-stack area, as shown in 2.11a.

Two distinct regions can be identified: first the SPE-Si coverage increases as the annealing time increases, which can be correlated to the growth behavior during the nucleation and the coalescence stages. Then the coverage remains constant (or slightly decreases) with further increase of the annealing time. Visual inspection of the SEM images confirms that the SPE coverage does, indeed, remains practically unchanged. However, the volume of deposited SPE-Si noticeably increases when increasing the growth time, which is substantiating evidence for the tendency to form compact structures and the fast growth in the $<100>$ vertical direction perpendicular to the Si substrate surface. A constant coverage as a function of time is observed until the vertical growth is completed, i.e., when the SPE-Si island height reaches the thickness of the initial Al transport layer. At that moment the coverage starts to increase with time because the lateral growth on the Si and possibly also overgrowth of the SiO_2 become predominant.

The SPE-Si coverage as a function of the width of the Al/α-Si layer-stack area for an annealing time of either 1.5, 2 or 6 minutes has also been plotted in Figure 2.11b. The coverage is found to be nearly constant irrespective of the Al/α-Si area. However, even though the surface coverage is nearly constant, the volume of nu-

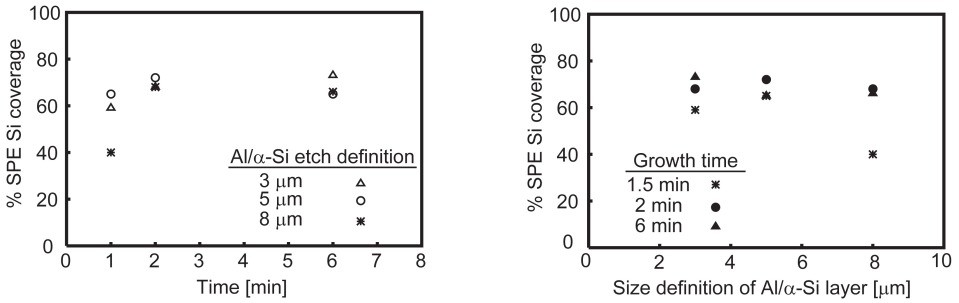
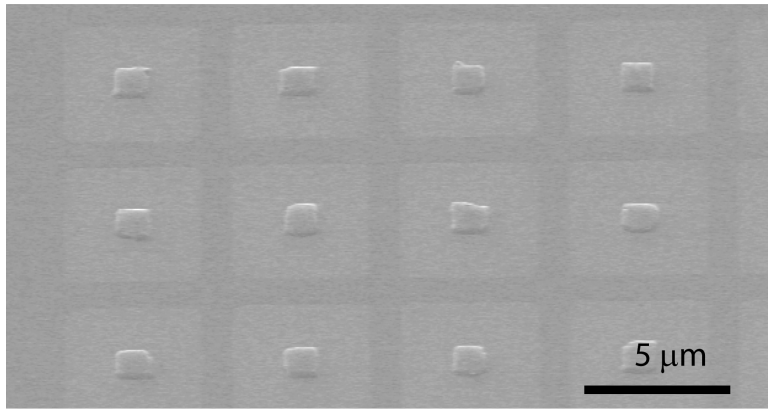


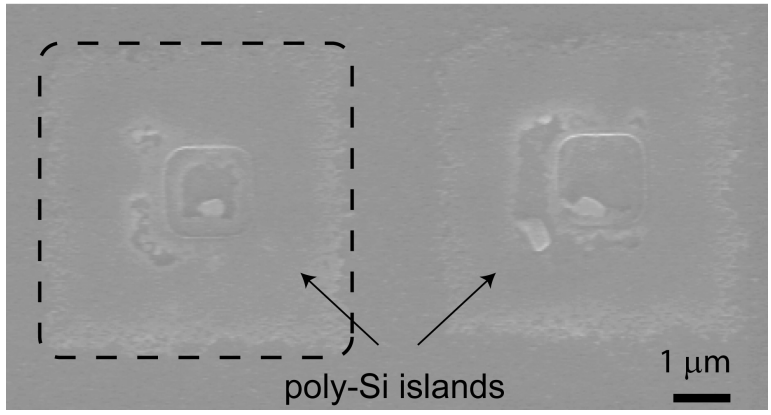
Figure 2.11: The first stages of the SPE-Si contact window coverage as a function of (a) annealing time, and (b) Al/α-Si layer stack width. In both cases, the contact window width was 1.4 μm and the growth temperature was 400°C.

cleated SPE Si increases with the Al/α-Si area. This effect is related to the ability of the Si nucleated on the SiO_2 to diffuse to the contact window. For the smallest Al/α-Si area (3×3 μm^2), the region around the contact windows is smooth and apparently Si-free, indicating that the entire α-Si layer has contributed to the vertical growth within the contact window. When the initial Al/α-Si area is much larger than the contact window, Si nucleation on SiO_2 is observed for short growth times. In this case, the Al/α-Si layer to exposed SiO_2 area ratio is apparently so large that there is a significant probability that energetically favorable defects in the thermal SiO_2 are found and given occasion to function as nucleation centers for the "free" Si atoms. Isolated polycrystalline Si islands can then grow. This will be discussed further in Section 2.4.1.

In general, it can be concluded that, if a selective filling of the contact window is desired, the amount of exposed SiO_2 surface should be as limited as possible. After a sufficiently long annealing time, typically 30 min for the 400°C anneal, the lateral growth progresses until the full window surface is covered, provided that the α-Si layer is sufficiently thick to supply the necessary Si. When more α-Si is provided so that the contact window can be more than filled, a lateral overgrowth of the SPE-Si on the surrounding dielectric is also observed. This lateral overgrowth can also be influenced in a controlled manner by designing arrays of the contact windows with specific geometry and positioning, in combination with optimized Al/α-Si layer-stack dimensions. This will be discussed in Section 4.2.



(a)



(b)

Figure 2.12: SEM micrographs of SPE growth results for two different dielectric: (a) thermally-grown SiO_2, or (b) PECVD SiO_2. The dashed line represents the Al/α-Si island to SiO_2 exposed area.

2.4 Process parameters

2.4.1 Influence of the dielectric surface properties

It has been previously shown that the Si migration at the surface of dielectric occurs during SPE and tends to increase the growth selectivity on Si. Defects in the SiO_2 film surface can function as preferred nucleation centers for the SPE-Si growth process, thus the quality of this dielectric also plays a role for controlling the growth in the contact windows. The very high selectivity achieved for the sample shown in Figure 2.12a was obtained by defining the contact windows in a low-defect density SiO_2 thermally-grown at 850°C. In this case there is a practically ideal selective deposition of SPE-Si on the *c*-Si surface with respect to the SiO_2 surface. On the other hand, for contact windows in a plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 performed at 400°C, the situation is almost completely the other way round: as shown in the example given in Figure 2.12b, very little SPE-Si is deposited in the contact windows and the available Si has been consumed by the deposition of polycrystalline Si on the SiO_2. This type of SiO_2 apparently has a surface structure that provides a dense distribution of nucleation sites for the incoming Si that is therefore largely prevented from diffusing to the contact window. Thus, for such poor quality SiO_2, selective deposition in the contact windows can only be achieved if the Al/α-Si layer-stack can be patterned with very little overlap of the contact window.

2.4.2 Influence of the contact window surface treatment

For all the above described experiments, care was taken not to damage the Si surface of the contact windows by ending the SiO_2 plasma etching with a soft landing. The significance of this procedure was experimentally investigated by also preparing and analyzing samples where a thermally-grown SiO_2 was etched by either a diluted buffered HF solution (1:7), which provides a smooth Si growth interface, or by a trifluoromethane (CHF_3) / hexafluoroethane (C_2F_6) based reactive ion etching (RIE) that is known to roughen the surface. With the latter step also a 30-nm-deep cavity was etched into the Si. In both cases, the Si surface was cleaned and the native SiO_2 was removed by a 4-min-long HF (0.55%) dip-etching. From SEM observations after growth and Al removal, examples of which

are presented in Figure 2.13, it can be concluded the damage induced by RIE at the Si growth interface influences neither the nucleation nor the growth.

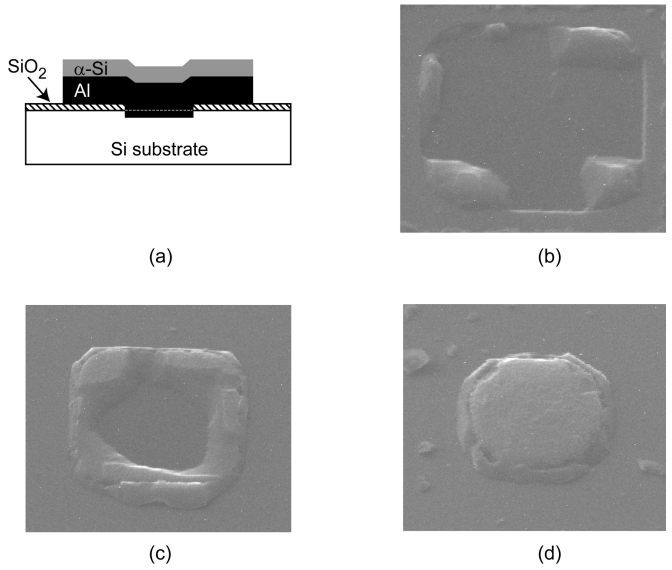


Figure 2.13: (a) Schematic of the test-structure used for investigating the influence of the soft-landing. Series of SEM micrographs obtained without soft landing on Si and illustrating the growth sequence: (b) preferential deposition at the corner of the window, (c) preferential deposition along the edges of the window, and (d) entirely-filled window.

2.4.3 Influence of the Al/α-Si etch definition

The size of the SPE islands is easily controllable since it is determined by the geometrical parameters of the contact window and the patterned Al/α-Si layer stack. The growth itself occurs for a large variety of Al thicknesses and the height of the SPE island corresponds to the thickness of the sputtered Al thin film. The control of the position and selectivity of the SPE growth is particularly enhanced by patterning of the Al/α-Si layer stack before the SPE.

Since the crystal growth, fed from the α-Si layer via a fast diffusion process in the Al layer [65], occurs selectively on the exposed Si substrate rather than on the surrounding SiO_2, the patterning of the Al/α-Si layer stack closely around

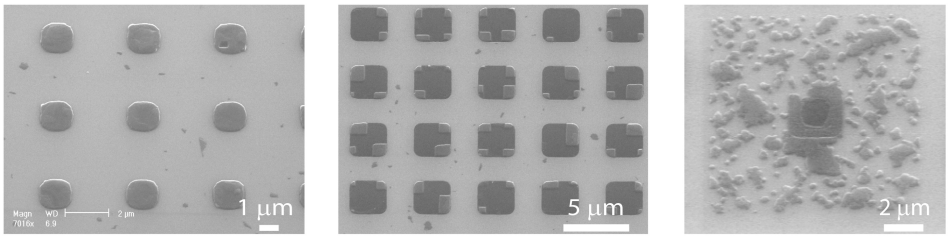


Figure 2.14: SEM micrographs showing the SPE growth results when the top Al/α-Si layer is: (a) patterned in $\sim$ 5-μm-wide island around 1.2-μm-wide window, (b) not patterned around a 3-μm-wide window, or (c) patterned in 10-μm-wide island around a 1.5-μm-wide contact window. In all cases, the thicknesses of the Al and α-Si layers were 150 nm and 10 nm, respectively.

the contact window will prevent the diffusion of the Si far away from the contact window and reduce the probability of deposition on SiO_2. The influence of the patterned Al/α-Si layer stack area is examined here more closely by SEM analysis of large arrays of contact windows with widths from 0.6 to 3 μm surrounded by Al/α-Si islands with widths from 3 to 11 μm. Initially, the size of the SPE grown crystal increases with the area of the surrounding Al/α-Si, in other words, with the amount of Si available for the growth.

On the other hand, when the layer stack of Al/α-Si is patterned in very large islands, the contact windows were found not to be entirely filled and polycrystalline Si deposition was observed on the surrounding SiO_2 (Figure 2.14). This indicates that, in this situation, a large amount of Si is consumed by the nucleation of polycrystalline Si on the SiO_2, and thus less Si material is available for SPE-Si growth in the contact window. This process may be enhanced by the exposure of the SiO_2 under the Al/α-Si to plasma and chemicals, producing faults in the SiO_2 favorable for Si nucleation. The SEM-assisted analysis provided the information necessary to determine the optimal ratio between the window size to fill in and the Al/α-Si island area to form an SPE-Si island with of a given height.

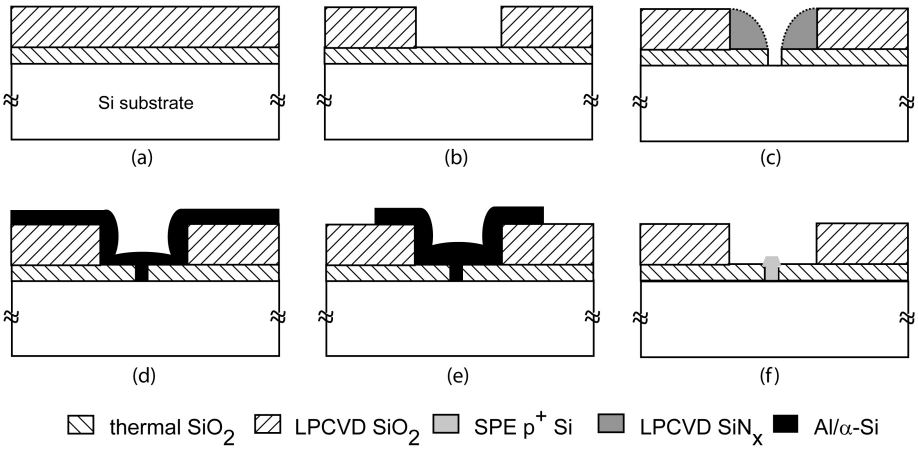


Figure 2.15: The SPE sequence for sub-micron window sizes. (a) Oxidization. (b) Contact window definition. (c) SiN_x spacer formation and SiO_2 etching. (d) Spacer removal and PVD deposition of Al/α-Si. (e) Al/α-Si etch definition. (f) Anneal with transport of α-Si through Al to the c-Si surface. The epitaxial Si is then observable in the contact windows after Al removal.

2.4.4 Influence of the downscaling of dimensions

The sequence of the SPE growth of nanoscale silicon islands in contact windows to the Si substrate is illustrated in Figure 2.15. The process fabrication sequence was modified in order to form a sub-100-nm-wide contact windows by using a silicon nitride (SiN_x) spacer technology. A 300-nm-thick low-pressure chemical-vapor-deposited silicon dioxide (LPCVD SiO_2) was deposited on top of a 30-nm-thick thermally grown SiO_2 and contact windows were patterned using conventional optical lithography. Anisotropic plasma etching through the LPCVD SiO_2 to the thermal SiO_2 was used to obtain contact windows of about 0.7 μm in width. The size of the contact windows was then reduced by using as follows: a 400-nm-thick layer of low-stress LPCVD SiN_x was deposited at 850°C and anisotropically plasma etched with C_2F_6 to leave spacers of about 350 nm wide. This reduced the width of the contact window mask to about 100 nm (Figure 2.16a).

The SiN_x spacers served as a hard mask to selectively plasma etch the remaining thermal SiO_2 with a mixture of C_2F_6/CHF_3 and applying a soft landing on the

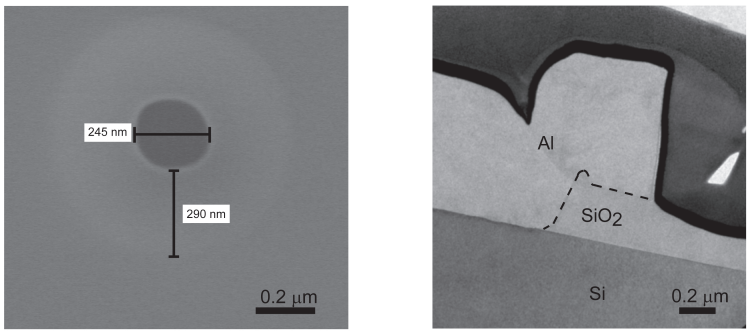


Figure 2.16: (a) SEM micrograph of contact window after SiN_x spacer formation. The initial contact window size was $\sim$ 900 nm. (b) Low-resolution cross section TEM of PVD deposited Al thin film on contact windows opened through thermally-grown SiO_2. The step height was $\sim$ 300 nm. For clarity, the edges of the SiO_2 are marked by a dashed line.

Si substrate. The native SiO_2, mainly induced by the cleaning and etching steps, was removed by dip-etching in HF 0.55% for 4 min before the transfer to the metallization module. A thin layer of aluminum was then deposited from an Al target containing 1% Si by physical vapor deposition (PVD) at room temperature.

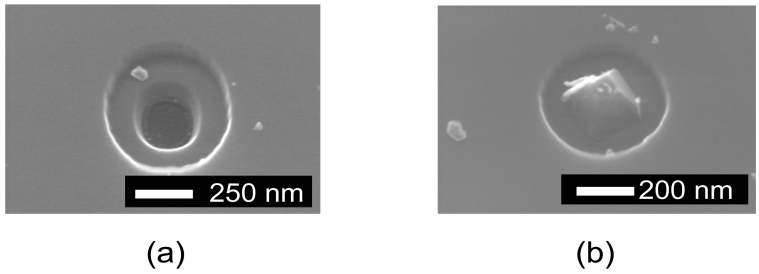


Figure 2.17: SEM micrographs of SPE growth results in the case of (a) contact windows with an aspect ratio of about 4. After Al and SiN_x spacer removal, no SPE-Si is observed on the Si surface. (b) contact windows with an aspect ratio of about 1; a Si single crystal has selectively grown in the exposed Si. Lateral overgrowth on the SiO_2 is also clearly observed.

The contact-windows step height is also an important process parameter since the PVD Al deposited at room temperature is known to have a poor conformity (Figure 2.16b). In order to reduce the aspect ratio before the metal deposition, the SiN_x spacers were selectively removed. A dilute solution of phosphoric acid (H_3PO_4) was used to etch SiN_x selectively with respect to the thermal SiO_2 and Si substrate. By heating the solution to 157°C, a selectivity of about 100 was obtained to both materials. In this manner, 90-nm-wide-contact windows were fabricated and filled with SPE-Si islands, as shown in Figure 2.17.

As a comparison, the sample in which the SiN_x spacers were not removed before the deposition of the aluminum transport layer does not exhibit any nucleation/growth in the contact windows. This is in agreement with the understanding of the growth mechanism, the poor step coverage of PVD Al thin films and the SiN_x surface morphology will inhibit the growth [66].

2.5 Conclusions

In this chapter, the growth mechanism of Si solid-phase epitaxy using Al as a transport layer was addressed. By extensively varying parameters such as the growth temperature, growth time and layer-stack properties, it was possible to distinguish specific stages in initial growth, on which basis the entire filling of contact windows to the *c*-Si with SPE-Si was semi-empirically modeled. Two important factors that are shown to be important for achieving high-quality material on (100) Si are (*i*) the strong preferential growth in the <100> directions and (*ii*) the fast diffusion of Si through Al grain boundaries and other interfaces. With the model and the much improved understanding of the deposition mechanisms, it is now possible to predict whether or not a specific window can be filled by a monocrystalline SPE-Si island.

Chapter 3

Material properties of SPE-Si

3.1 Introduction

In the previous chapter, the mechanisms governing the aluminum-mediated solid-phase epitaxy (SPE) growth were investigated. The basic process flow and the process parameters influencing the growth sequence were addressed in detail. The objective was to provide a set of parameters to optimize for the complete filling of arbitrarily-shaped contact windows with an SPE-Si island of a given height. In this chapter, the focus is placed on characterizing the quality of the Si material obtained by aluminum-mediated SPE. A good knowledge of the material properties gives a good basis for making SPE-Si devices. In the literature, Si growth techniques which involve a maximum process temperature below 500°C generally lead to the formation of a polycrystalline Si films. In this chapter, the SPE-Si crystallinity, doping concentration and profile have been investigated by using different techniques: Raman spectroscopy, high-resolution transmission electron microscopy (TEM), secondary-ion-mass spectroscopy (SIMS) and capacitance–voltage (C–V) doping profiling.

3.2 Crystallinity

3.2.1 Si precipitates from Al/Si alloy

Information on the crystallinity of Si formed by aluminum-mediated crystallization can be found in studies reported in the early 1970s, when Al/Si alloys were introduced as the standard metal in IC fabrication. At that time, the semiconductor industry was struggling with the problems caused by Si substrate migration during thermal treatment of the pure aluminum layers used for device contacting. To avoid resulting spiking phenomenon and enable further downscaling of the junction depth below the micron range, the use of an Al thin film saturated with Si (typically 2–3%) was successfully introduced as a standard metal. As seen on the phase diagram of binary Al/Si alloy, $\sim$ 0.3-0.4% of Si is dissolved in the Al at 400°C (Figure 3.1).

The excess Si was found to precipitate at the Si surface (Figure 3.2). Even though it represents a very simple way of growing Si at low-temperature, the presence of such highly aluminum p-doped Si clusters has a negative impact on the device characteristics by increasing the contact resistance to n-type Si. This has justified the introduction of Ti/TiN/Al metal stack as barrier layer [67].

However, the as-obtained Si clusters exhibit several interesting properties: first, the Si nuclei formed after thermal treatment at 400°C preferably deposit along the edges of the windows and align with the pattern of the Al grain boundaries [68]. Moreover, the clearly faceted shape suggested also a preferential growth orientation.

The SPE-Si growth technique presented in this thesis can be seen as a very controllable implementation of this well-known phenomenon, in which not only the location but the properties of the grown Si are controllable, predictable, and reproducible. The quality of the SPE-Si was verified quantitatively by local Raman spectroscopy, EBSD measurements and high-resolution TEM.

3.2.2 Raman spectroscopy

Raman spectroscopy is generally used to give a preliminary indication of the crystallographic quality of polycrystalline material at the μ-scale. In our case, the spot, of a size of about 1 μm, has been accurately positioned on 1.4 μm-wide islands

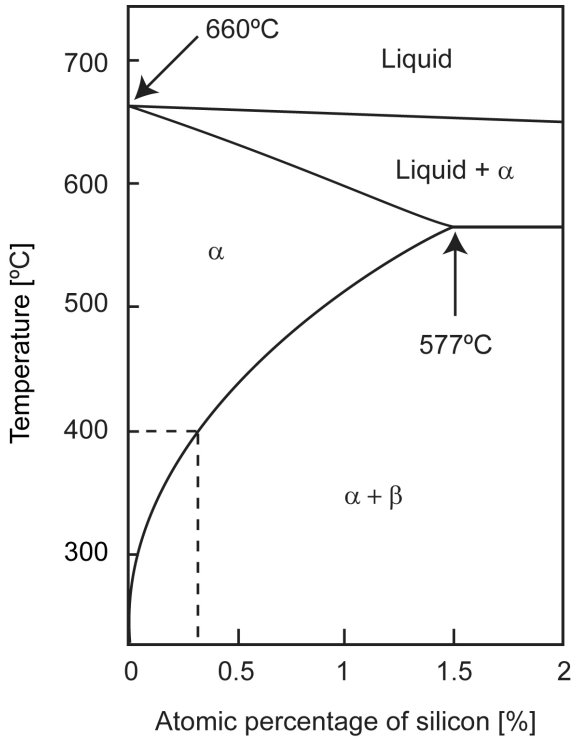


Figure 3.1: Al/Si binary phase diagram corresponding to the Al-rich region (Si concentration up to 2 %).

grown at 400°C on a (100)-Si substrate.

The results, shown in Figure 3.3, display the typical crystalline Si spectrum with the maximum peak at 517 cm^{-1}. No signature of polycrystallinity, generally detected by a deviation of the crystalline peak, is observed. This is an indication that Si grown on the Si substrate is epitaxial, even though it was not possible to extract the substrate contribution from the total signal. Therefore additional material characterization techniques have been carried out to achieve conclusive proof on the epitaxial properties of the SPE grown Si.

3.2.3 Electron back-scattering diffraction

Since the early 1990s, electron back-scattering diffraction (EBSD) has evolved to become a mature technique for microstructure analysis. During the measure-

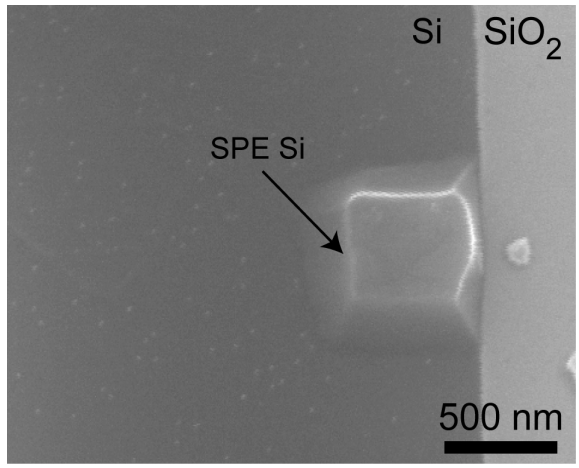


Figure 3.2: SEM micrograph of a Si island, obtained after 400°C annealing of Al layer containing 1% Si.

ment, back-scattered electrons are detected and captured with by phosphorous screen, producing an electron back-scattered pattern, which consists of Kikuchi bands from different crystal planes of the inspected spot [69]. By indexing the Kikuchi bands, the three-dimensional crystallographic orientation is readily obtained. In the DIMES laboratory, the EBSD analysis is carried out with an orientation imaging microscopy EBSD system, installed on the FEI XL50 scanning electron microscope. This system provides visual images of the microstructure of the crystalline grains. During the ESBD analysis, the sample is tilted by 70°, and the accelerating voltage is 20 kV.

The results of EBSD analysis indicate no difference between the SPE-grown Si and the Si substrate, and thus allow to conclude that the SPE-Si regions and the substrate have the same crystallographic orientation. However, electron back-scattering diffraction only provides information about the sample surface. A more detailed structural analysis is obtained by performing a local cross-section of an SPE-Si island and applying transmission electron microscopy (TEM).

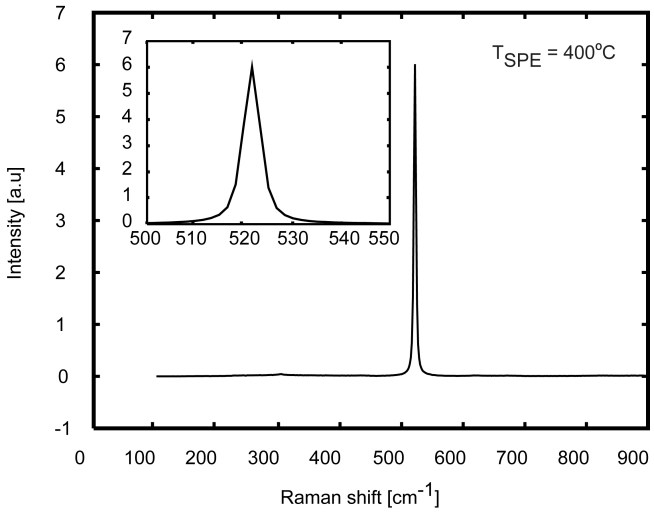


Figure 3.3: Raman scattering spectra measured on a 1.4×1.4 μm^2 SPE-Si island grown on a (100)-Si substrate. The growth temperature and duration were 400°C and 30 min, respectively.

3.2.4 Transmission electron microscopy analysis

A TEM analysis enables lattice images at an atomic-scale resolution. As electrons pass through the sample, both elastic and inelastic scattering occur. These interactions disclose diverse information about the structure of the sample. In the case of crystalline material, interactions between the electrons and the lattice atoms give rise to Bragg diffraction, on the basis of which the orientation and structure of the material can be extracted. The analysis was performed in the laboratory of the Evans Analytical Group, in the United Kingdom, using a TECNAI F20 equipment at 200 kV.

In this case, the SPE-Si to Si-substrate interface was analyzed by a high-resolution TEM cross-section of an SPE-Si island, of about $\sim$ 600 nm in width and $\sim$ 170 nm in height, grown on a (100)-Si substrate and localized in a contact window etched through SiO_2 (Figure 3.4).

The results shown in Figure 3.5 clearly substantiate that the growth is epitaxial and definitively confirm the ability to form epitaxial Si islands in a highly-controllable process, at temperatures as low as 400°C.

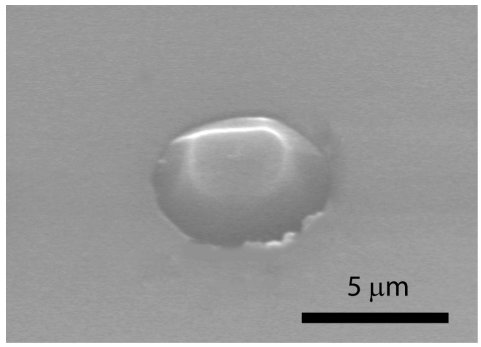


Figure 3.4: SEM micrograph of a 600-nm-wide SPE-Si island on which the TEM analysis was performed.

After aluminum-removal and unavoidable exposure to air, the surface of the island is oxidized and a 2–3-nm-thick native SiO_2 layer can be observed, as shown in Figure 3.6. An attempt to increase the size of the crystal was also performed by the use of a subsequent vapor-phase epitaxy after SPE growth: practically a silane (SiH_4) flow was introduced in the growth chamber during the thermal annealing. The as-formed epitaxial Si islands were indeed enlarged with respect to the ones obtained by SPE (without SiH_4); however, a high density of massive crystalline defects were also obtained closed to the island surface. Therefore, a process in which the α-Si is used as the unique Si source appears to be more controllable technique to obtain high-quality crystalline Si films. The presence of a thin amorphous layer (presumable SiO_2) at the growth interface has also been observed in some cases.

All these results demonstrate that Si grown on (100)-Si by aluminum-mediated SPE is monocrystalline at temperatures as low as 400°C. Aluminum is used as a transport layer to decrease the activation energy of the α-Si crystallization, as described in Section 2.3. Moreover, it is also a dopant for Si, thus the quantitative profiling of Al incorporated within the SPE-Si islands is an important aspect that must be taken into account when electrical SPE-Si based devices are to be made.

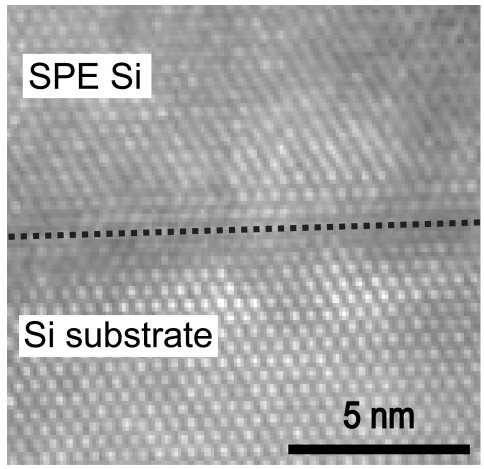


Figure 3.5: High-resolution TEM of the Si substrate to SPE-Si island interface demonstrating the epitaxial growth.

3.3 Doping concentration

The doping of the monocrystalline SPE-Si caused by the Al-metal transport layer incorporation is important for the device performance but up until now little quantitative information was available on doping incorporation for comparable processes such as metal-induced Si crystallization on SiO_2. In the case of Al, substitutionally incorporated ions will act as acceptors, i.e., the Al-mediated SPE-Si mechanism also offers a low-temperature means of creating p-doped regions. In

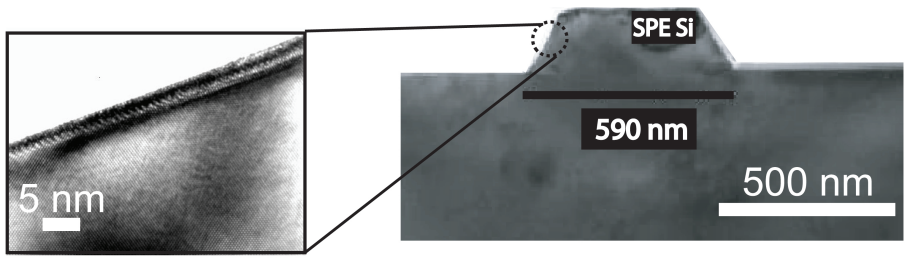


Figure 3.6: Cross-sectional TEM image of an SPE-Si island after Al transport-layer removal. The growth temperature was 500°C.

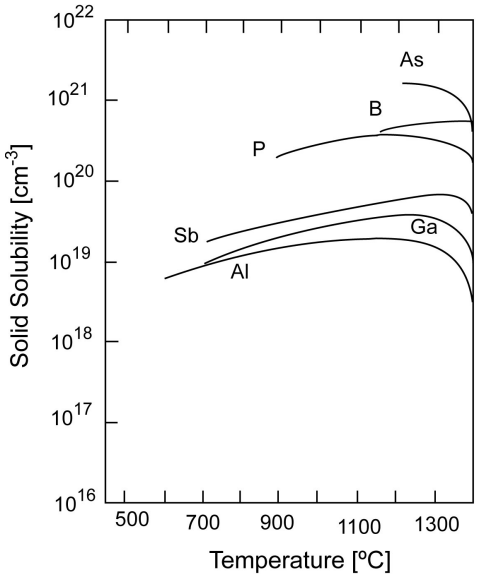


Figure 3.7: Solid solubility limits for various impurities in Si [70].

the literature, the incorporated Al-concentration is often assumed to be above the equilibrium Al solid-solubility in Si that is quite low at temperatures below 500°C, slightly above 10^{18} cm^{-3} (Figure 3.7). In principle, the concentration of Al in Si can be profiled by SIMS quantification just like the conventional dopants. However, in the Si obtained by Al-mediated SPE, the size of the crystals, typically a few μm, remains smaller than the minimum size of the SIMS analysis area ($\sim$ 60$\times$60 μm^2). Moreover, in systems where large Si areas are grown, the surface is usually not uniform enough to allow an accurate SIMS analysis.

In this section, a successful attempt to accurately profile the Al concentration within the SPE-Si island is described. The high degree of controllability of the growth mechanism has been used to create areas of SPE Si-islands that are suitable for a quantitatively correct SIMS profiling of the elemental Al concentration in the islands.

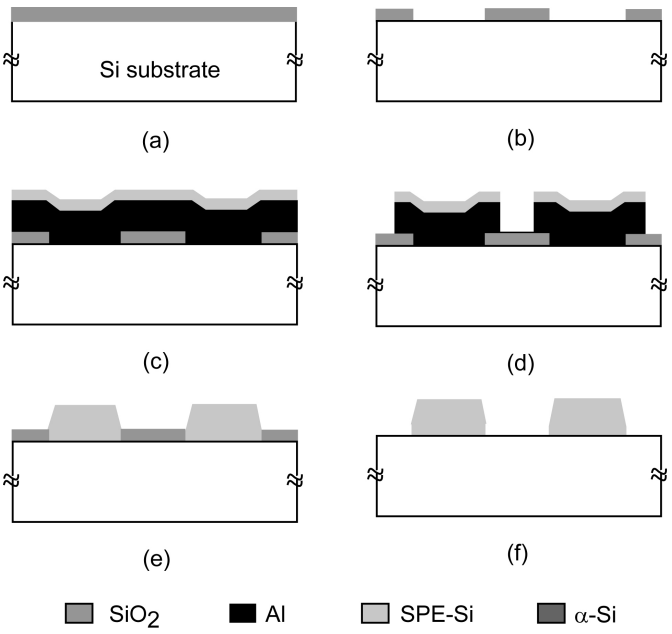


Figure 3.8: Schematic cross-section of the process done for SIMS sample preparation. (a) Thermal oxidation. (b) Contact window definition. (c) Al/α-Si PVD deposition. (d) Al/α-Si layer-stack island definition. (e) Growth and Al removal. (f) SiO_2 removal.

3.3.1 Sample preparation

SIMS analysis area fabrication

The process flow used for fabricating an SPE-Si island array with a total area of about 60×60 μm^2 and containing 90 similar islands, each approximately 1.4×1.4 μm^2 in size, is presented in Figure 3.8.

First, 1.4-μm-wide contact windows were opened by conventional lithography through a 30-nm-thick thermal SiO_2 to the (100) Si substrate by using buffered hydrofluoric acid (BHF) 1:7. The surface preparation and the experimental conditions of the PVD deposition of the Al/α-Si layer stack was described previously in Section 2.2. The thicknesses of the Al and α-Si films were, in this experiment, 200 nm and 20 nm, respectively. The Figure 3.9 shows the SPE growth result when the Al/α-Si layer stack is not patterned: even though entirely filled contact

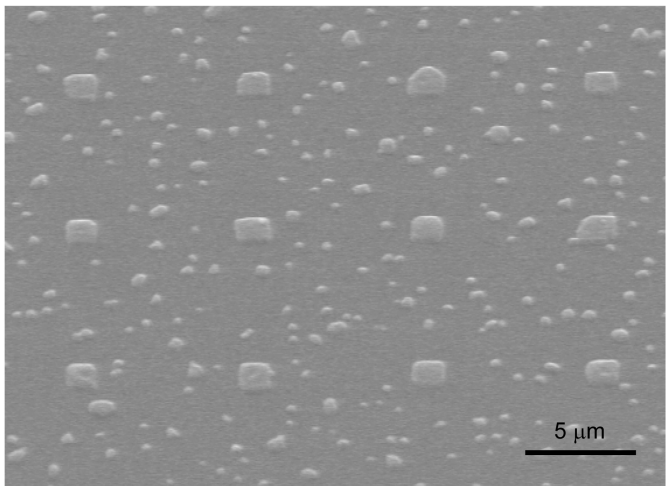


Figure 3.9: SEM micrograph of an area of Si islands grown by SPE at 400°C obtained without patterning the Al/α-Si layer-stack.

windows with SPE Si were observed, the density of the nucleation on SiO_2 is too high to perform an accurate SIMS analysis since the contribution of Si islands deposited on SiO_2, also rich in Al, cannot be subtracted from the total measured SIMS signal.

For an accurate SIMS quantification, it is essential to avoid random nucleation of Al-rich Si on SiO_2, since it is not possible to extract their signal from the total impurity signal. Optimal selective deposition was obtained for a Al/α-Si layer stack patterned in islands 5×5 μm^2 in width. With the procedure used here, a practically ideal SPE-Si growth selectivity was achieved with respect to the competing process of Si nucleation on SiO_2. On the contrary to Section 2.2, the epitaxy itself was induced, in this experiment, by a thermal anneal at 400°C for 40 min in a N_2/H_2 (10:1) mixture at atmospheric pressure. After the growth, the aluminum transport layer was removed in a solution of diluted HF 0.55%.

Moreover, the remaining SiO_2 was also removed by BHF 1:7 in order to avoid any possible SIMS artefact connected to charging effects during the SIMS sputtering: considering that the total SIMS acquisition area (60×60 μm^2) is much larger than the total area of the SPE-Si islands, $\sim$ 4.5% of the total analysis area, the risk associated with charging could not be ignored.

The SPE-Si island height, determined by the thickness of the Al transport layer [71], was about 200 nm. An SEM micrograph of the as-obtained Si surface for SIMS analysis is shown in Figure 3.10. It confirms that with this process it has been possible to choose the growth parameters (time, temperature, and Al/α-Si layer-stack patterning) in such a way that a highly selective growth in the windows is reliably achieved. Moreover, a flat surface of the islands has been obtained, which is essential for performing an accurate SIMS profiling. A SEM-assisted measurement of the island width distribution indicated an average width of 1.4 μm $\pm$ 0.056 (σ) thus substantiating the high controllability of this feature. The fact that the Si deposited by PVD is entirely consumed by the epitaxial growth in the contact windows, and no Al-rich polycrystalline Si islands are randomly deposited on the surrounding dielectric, makes it possible to give an SPE-island related-analysis of the SIMS data.

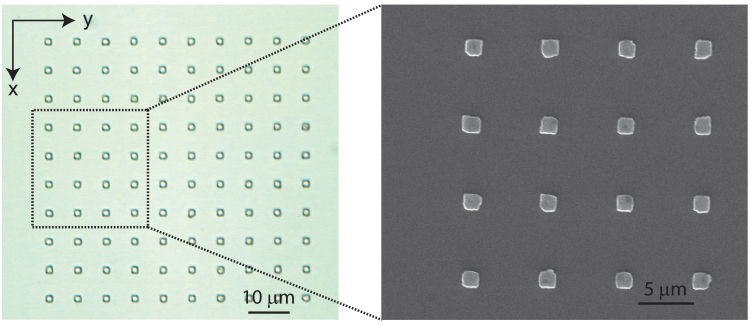


Figure 3.10: (a) Optical microscope image showing an area of $\sim 60\times60$ μm^2 Si, including 100 SPE-Si islands grown at 400°C. (b) SEM micrograph of corresponding SPE-Si islands. The location-controllability and selectivity of the SPE-Si growth is excellent so that practically no nucleation on the SiO_2 is observed.

In practice, a dynamic-SIMS (D-SIMS) analysis was performed at the laboratory of Evans Analytical Group, in the United Kingdom, using an oxygen ion O_2^+ beam, a primary ion beam of 5 keV and an angle of incidence of $\sim 45°$. The Al-concentration detection limit was 4×10^{13} cm^{-3}. The calibration was performed by measuring ion-implant standards to obtain the relative sensitivity factors (RSF), which convert the impurity secondary ion intensity into atom density [72]. With

this calibration technique, commonly used in the case of impurity concentration lower than the dilute limit, there is practically no influence on the Al to Si ratio used for the SIMS quantification as the pure Si signal, in the end, does not change when scaling down the D-SIMS raster area. This gives:

$$\int_{\frac{-L_{SIMS}}{2}}^{\frac{L_{SIMS}}{2}} \int_{\frac{-L_{SIMS}}{2}}^{\frac{L_{SIMS}}{2}} C_{meas}(x,y,z) \cdot dxdy = \int_{\frac{-L_{SIMS}}{2}}^{\frac{L_{SIMS}}{2}} \int_{\frac{-L_{SIMS}}{2}}^{\frac{L_{SIMS}}{2}} C_{meas}(z) \cdot dxdy \tag{3.1}$$

and

$$\int_{\frac{-W_{SPE}}{2}}^{\frac{W_{SPE}}{2}} \int_{\frac{-W_{SPE}}{2}}^{\frac{W_{SPE}}{2}} C_{eff}(z) \cdot dxdy = \int_{\frac{-L_{SIMS}}{2}}^{\frac{L_{SIMS}}{2}} \int_{\frac{-L_{SIMS}}{2}}^{\frac{L_{SIMS}}{2}} C_{meas}(z) \cdot dxdy \tag{3.2}$$

where L_{SIMS} is the width of the SIMS crater, C_{meas} is the measured impurities concentration, W_{SPE} is the width of the SPE-Si island, and C_{eff} is the effective impurity doping concentration in the SPE-Si island.

Therefore,

$$C_{eff}(z) = \frac{C_{meas}(z)}{\alpha} \tag{3.3}$$

where $\alpha = \frac{W_{SPE}^2}{L_{SIMS}^2}$ is the SPE-Si to SIMS analysis area ratio.

During the D-SIMS measurement, material is sputtered from both the SPE-islands and the Si of the surrounding substrate. To make sure that the quality of the 30-nm-thick thermal SiO_2 was good enough to prevent Al-dopant diffusion into the Si substrate during the epitaxy process, an area of a few hundreds of μm^2 large Si region without any contact windows was also prepared as a reference for the SIMS analysis.

3.3.2 Al-dopant profiling

The measurement of the non-patterned sample shows that the background Al-concentration doping is no more than 10^{13} cm^{-3}, i.e., there is no Al diffusion through the 30-nm-thick SiO_2 surface isolation layer into the bulk Si (Figure 3.11). A narrow Al-contamination spike is, however, visible within the top 20 nm of the surface, presumably related to Al-surface contamination prior to SIMS, for example from the aluminum layer-stack removal steps. In any case, this contami-

nation peak does not have an impact on the analysis of the Al-profile measured on the sample patterned with SPE-islands.

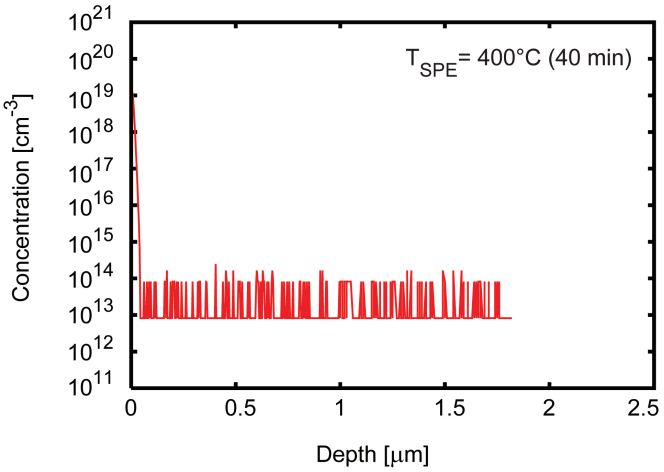


Figure 3.11: Background Al-doping profile measured by SIMS on a bare Si region exposed to diffusion of Al-dopant after 40-min growth at 400°C.

As seen in Figure 3.12, the top 20 nm of this profile can be disregarded while an uniform Al-concentration of about 4.5×10^{17} cm^{-3} is measured up to a depth of about 200 nm in region (1), which corresponds to the height of the SPE islands. As stated in Section 3.3.1, a SIMS calibration technique was chosen particularly for the measurement of low concentration levels [73]. As seen before, the quantification signal scales in proportion with the relative area of the Si islands. Consequently, as the SPE-Si islands cover only 4.5% of the total analysis area, the Al concentration in the Si obtained by SPE can be estimated 1–2×10^{19} cm^{-3}. In the following region (2), the SIMS profile displays a sudden drop in Al concentration, by more than one order of magnitude over a depth of $\sim$ 30 nm. A more gradual decrease of doping is then observed in region (3). It is safe to assume that the doping tail in regions (2) and (3) is the result of knock-on and/or differential sputtering effects.

The Al-doping in the SPE-Si islands obtained here is well above the equilibrium solid-solubility limit, which is 3×10^{18} cm^{-3} at 400°C [74]. In this connection, it is worth mentioning that SPE-Si is a non-equilibrium process, thus values

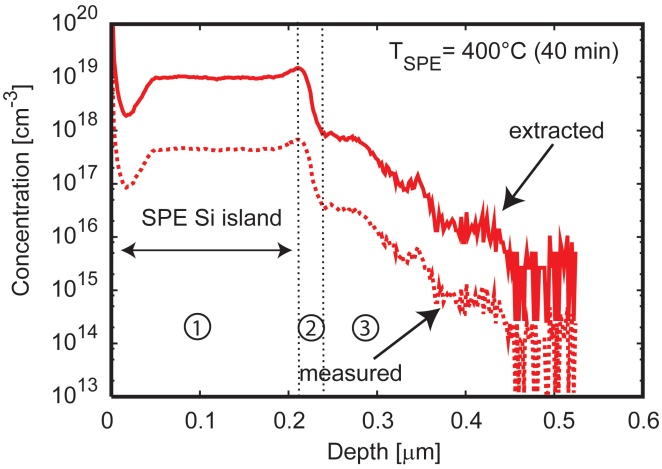


Figure 3.12: Measured (dashed-line) and extracted (solid-line) Al-doping profile determined by SIMS of a 60×60 μm^2 Si region containing an array of 90 SPE-Si islands (4.5% of the total analysis area). The extracted Al-doping in the SPE-Si islands is about 1–2×10^{19}cm^{-3}.

above the equilibrium solid-solubility are possible. Moreover, measurements of the contact resistance of Al-metallization to the SPE-islands show that the SPE-Si surface was not oxidized before the deposition of the test structure Al-interconnect layer [75]. This will be addressed in more detail in the Section 5.11. The measured contact resistivity, of about 10^{-7} Ω×cm^2, was much lower than what would be expected for an active doping around 10^{18} cm^{-3} or even 10^{19} cm^{-3}. This suggests that there may be a segregation of Al at the surface of the SPE-Si islands that gives a higher electrical activity near the contact interface. It has not been possible to include the detection of this layer in an SIMS analysis due to the necessary cleaning (10 min in a fumic nitric acid HNO_3) that leads to oxidation of the SPE-Si islands.

Table 3.1: Typical diffusivity values for a number of impurities [76].

Element	$D_0(cm^2/s)$	$E_A(eV)$
Al	8.00	3.47
Ga	3.60	3.51
B	10.5	3.69
P	10.5	3.69
In	16.5	3.90
As	0.32	3.56
Sb	5.60	3.95

3.4 Abruptness of the doping transition

3.4.1 Al-dopant diffusion

Diffusion of Al in Si is a key parameter, because it determines whether ultrashallow p^+ SPE-Si junctions can be formed. The Al diffusion in Si at a temperature T can be described by the one-dimensional Fick's equation.

$$\frac{\delta C(x,t)}{\delta t} = D \cdot \frac{\delta^2 C(x,t)}{\delta x^2} \tag{3.4}$$

where C is the impurity concentration and D the diffusion coefficient given by the Arrhenius relation (3.5)

$$D(T) = D_0 \cdot e^{\frac{-E_A}{kT}} \tag{3.5}$$

where D_0 is the diffusivity and E_A is the activation energy of diffusion.

The value of the diffusion coefficients of commonly-used dopants in Si are shown in Figure 3.13.

The diffusivity of Al dopants in Si at 500°C, D_{Al}(500°C) $\sim 2\times10^{-22}$ cm^2/s, which, assuming the typical 30-min-long anneal used for the SPE growth mechanism, corresponds to a diffusion length L of $\sim$ 0.7 nm, using the relation and values reported in 3.6 and on Table 3.1.

$$L = \sqrt{4 \cdot \ D(T) \cdot \ t} \tag{3.6}$$

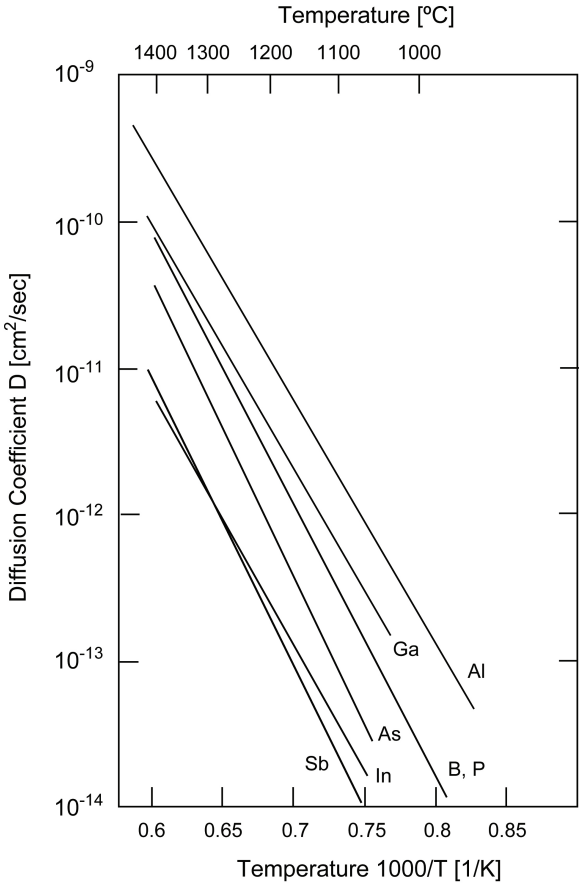


Figure 3.13: Diffusion coefficient of commonly-used dopants in Si [76].

where t is the annealing time, $D(T)$ the diffusion coefficient of Al in Si at temperature T.

Due to the low thermal budget involved in the SPE growth process, the diffusion of Al dopants in bulk Si is then negligible. Experimentally, the abruptness of the doping transition has been verified by an in-house capacitance-voltage (C–V) doping profiling technique that uses an abrupt n^+ buried layer to profile the tail of high-gradient boron-doped layers at the wafer surface [77]. A description of the test structure and obtained results are represented below.

3.4.2 Capacitance-voltage test structures

The schematic cross-section of the C–V doping profiling test structure is shown in Figure 3.14. First, the 0.1-μm-wide arsenic peak, doped to 10^{19} cm^{-3}, is grown so that the gradient of the down-going flanks is less than the SIMS resolution. In the following, the arsenic auto-doping that starts at a level of about 10^{17} cm^{-3} is reduced and compensated by growing a 0.1-μm-wide boron layer after the arsenic peak. The remaining 0.2-μm-top-layer is arsenic-doped to about 2×10^{16} cm^{-3} by the residual arsenic auto-doping. The epitaxy of these doped layers was performed at 700°C, at which temperature the dopant diffusion is negligible [77]. The C–V measurements have been performed on HP 4284A and Cascade Microtech probe station. To be sure that high series resistance was not influencing the measurement, the capacitance was checked for frequencies from 100 kHz to 1 MHz. Most of the presented results have been measured at 100 kHz with a small-signal bias amplitude of 15 mV. The DC bias voltage was varied from -0.5 V to 6 V in steps of 30 mV. The capacitance was measured on large rectangular diodes of different area and geometry so that the perimeter capacitance could be subtracted. An effective area of 500×500 μm^2 is used in the calculation of the C–V profiles.

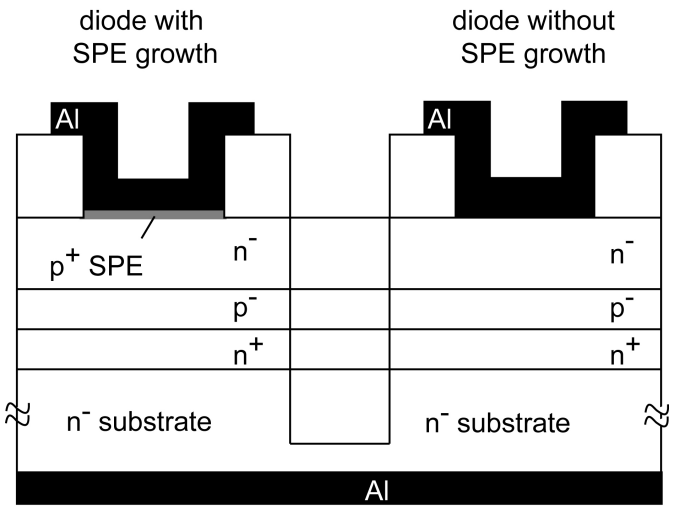


Figure 3.14: Schematic cross-section of the SPE and Schottky diode used to perform the C–V measurements. The top n^- and p^- regions are completely depleted during the measurements.

With this method, the doping can be measured up to a value of a few times 10^{18} cm^{-3}. Assuming the depletion approximation, the corresponding carrier density profiles, either n(x) or p(x) for electron and holes, respectively, have been extracted from the C–V curves by the standard equations 3.7 and 3.8:

$$W = \frac{\varepsilon_{Si} \cdot A}{C} \tag{3.7}$$

and

$$p(W) = \frac{2}{q \cdot \varepsilon_{Si} \cdot A^2 \cdot \frac{d}{dV}\left(\frac{1}{C^2}\right)} \tag{3.8}$$

where W is the width of the depletion region over which the capacitance C is measured, A is the area of the capacitor, and ε_{Si} is the permittivity of Si. The measured profile of a large contact window with random SPE-island deposition is compared to that of a neighboring contact without SPE-Si deposition (i.e., a Schottky contact).

3.4.3 Capacitance-voltage Al-doping profiling

As shown in Figure 3.15, the doping transitions are located at identical depths, which confirms that Al dopants do not diffuse in the Si substrate at the SPE growth temperature. Moreover, the doping level at the interface was found to be much higher than 10^{18} cm^{-3}, which substantiates the existence of Al-rich interface layer.

These results demonstrate the potential of Al-doped SPE-Si for shallow junction formation. Since the diffusion of Al in the substrate is negligible, the junction depth is entirely controlled by the thickness of the p-doped SPE-Si island, which is directly determined by the PVD deposited Al layer, as seen in Section 2.2. Moreover, due to the low temperature involved in the SPE process, it is not surprising that abrupt junctions can be achieved. Indeed, the technique consisting of the alloying of the Al (containing 0.7–1%Si) metallization at 400°C has been intensively used for decades in the IC industry in order to decrease the metal to Si substrate contact resistance.

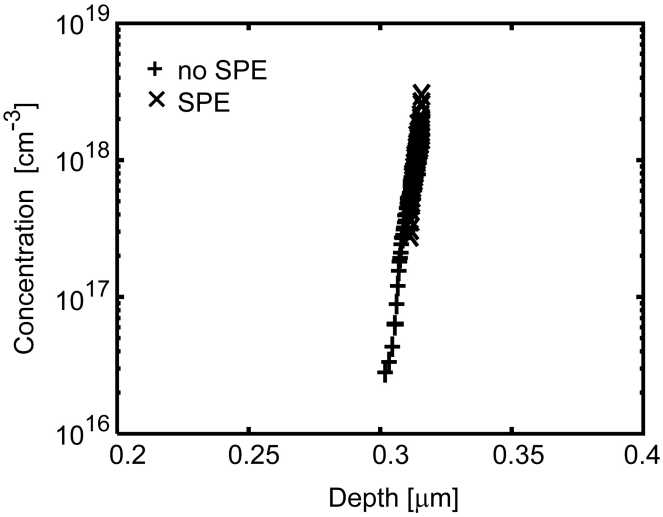


Figure 3.15: Doping profiles extracted from C–V measurements from a buried n^+ layer to the contact window surface.

3.5 Conclusions

In this section, the properties of Si material obtained by Al-mediated SPE at low temperature were evaluated. In spite of the low thermal budget, a remarkably high-quality monocrystalline Si has been confirmed by Raman spectroscopy, EBSD and local HR-TEM analysis. Moreover, an innovative sample preparation technique to measure the elemental Al doping concentration by SIMS was applied to accurately profile the Al-dopants incorporated in the SPE-Si. A uniform Al concentration of about $\sim$ 1–2$\times 10^{19}$ cm^{-3} was reliably measured. The abruptness of the Al doping transition has also been verified by doping profiles extracted from C–V measurements. The high diffusivity of Al dopants in Si was also not an issue since the temperature remains below 500°C for the whole process. All these properties make the Si obtained by SPE a very promising module for forming ultrashallow abrupt p^+-n junctions for both front- and back-end processes.

Chapter 4

Other configurations and materials

4.1 Introduction

This chapter deals with two implementations of the SPE technique that have been developed on the basis of the understanding gained from the study of the phenomena influencing the growth sequence on Si. First, the formation of Silicon-on-Insulator (SOI) by highly-controllable SPE-Si lateral overgrowth on SiO_2 is described. Then, few-micron long ring-shaped contact windows were successfully filled in with SPE-Si, which substantiates the possibility to apply the Al-mediated technique to arbitrarily-shaped geometry.

4.2 Lateral SPE silicon-on-insulator overgrowth

4.2.1 Introduction

For the case of locally-positioned SPE growth on Si, it was demonstrated in Section 2.3 that Si deposits preferably within contact windows rather than on the surrounding SiO_2. This has been generally observed when contact windows to the Si substrate are separated by more than some tens of μm, and the thickness of the α-Si layer is precisely chosen for filling a single contact opening of a given width. In this situation, SEM and TEM measurements of the island dimensions

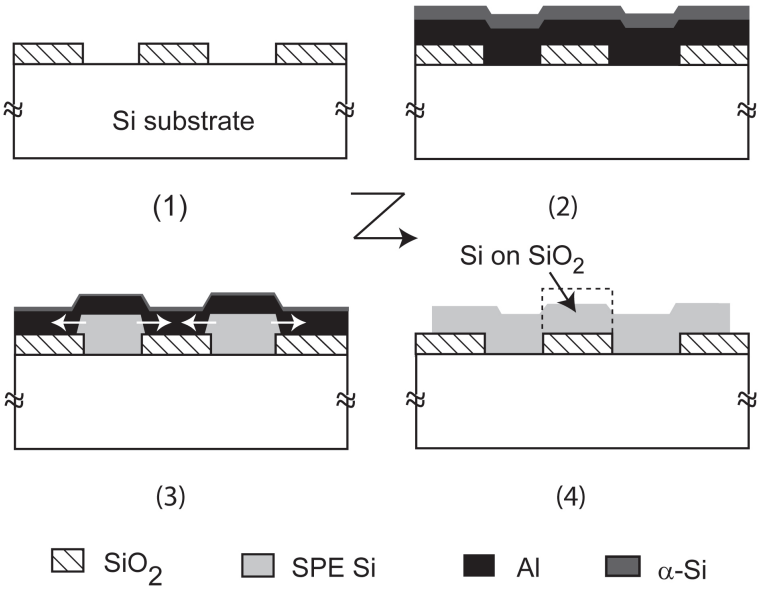


Figure 4.1: Schematic cross-section of the process formation of SPE-Si on SiO_2.

after growth have shown that a limited lateral Si overgrowth on the SiO_2 occurs, resulting in slightly wider SPE-Si island than the initial size of the contact window to be filled. This section treats the experimental conditions that can be used to enhance the lateral overgrowth of SPE-Si on SiO_2. The crystallinity of the as-formed regions and the process parameters that control the SPE growth are also addressed below.

4.2.2 Experimental preparations

To investigate the formation of SPE-Si regions on SiO_2, special test-structures were fabricated in which the lateral overgrowth is controlled by the pitch and width of the contact windows that are used to initiate the SPE growth (Figure 4.1). Thus, contact windows with a variety of widths and pitches, ranging from 0.6 μm to 1 μm and from 1 μm to 2 μm, respectively, were fabricated on thermally oxidized (100)-Si substrates. The isolation of the Si surface prior to the Al/α-Si layer-stack deposition was similar to that described earlier in Section 2.2. The Si/SiO_2 arrays were then covered with 200 nm of Al (containing 1%Si) and 100

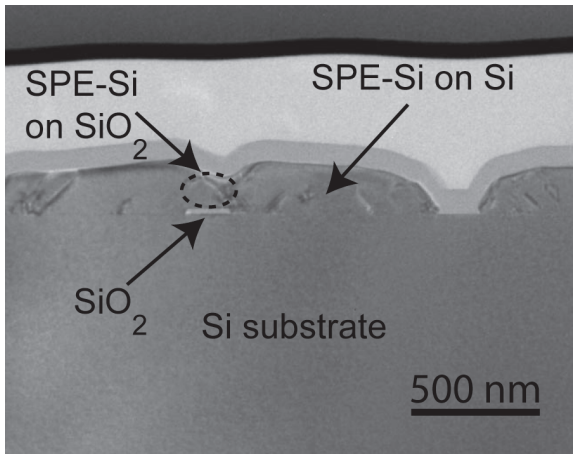


Figure 4.2: TEM cross-sectional view after SPE growth and Al removal. The magnification is 5×10^3. A 100-nm-thick layer of PECVD SiO_2 was deposited at 400°C to cover the entire sample in order to avoid possible scratches before performing the cross-section.

nm α-Si and annealed at 400°C in N_2/H_2 at atmospheric pressure for 30 min. The Al transport layer was then removed selectively to the SiO_2 and Si using conventional metal etchants.

A low-magnification TEM cross-sectional view of the as-obtained grown islands is shown in Figure 4.2. A good control of the nucleation site, enhanced by the use of low-defect density thermally-grown SiO_2, inhibits the parasitic nucleation of polycrystalline Si islands on SiO_2 that could lead to the presence of polycrystalline Si with the associated grain boundaries. Moreover, as already discussed in Section 2.3, the corners are preferred locations for the SPE initiation, so the Si surface near the contact window edges plays, in this experiment, the role of nucleating seeds for further lateral overgrowth on SiO_2.

The SPE-Si nucleated first within the contact windows, so the SiO_2 step height was found to be a limiting factor for the lateral overgrowth for a given Al/α-Si layer stack thickness. Indeed, the analysis of fabricated test structures of different SiO_2 thicknesses (30 nm, 50 nm, and 100 nm, respectively) clearly substantiates that the SPE-Si deposition on SiO_2 decreases when the SiO_2 thickness increases, for a given Al/α-Si stack thickness (Figure 4.3). Indeed, when the thickness of

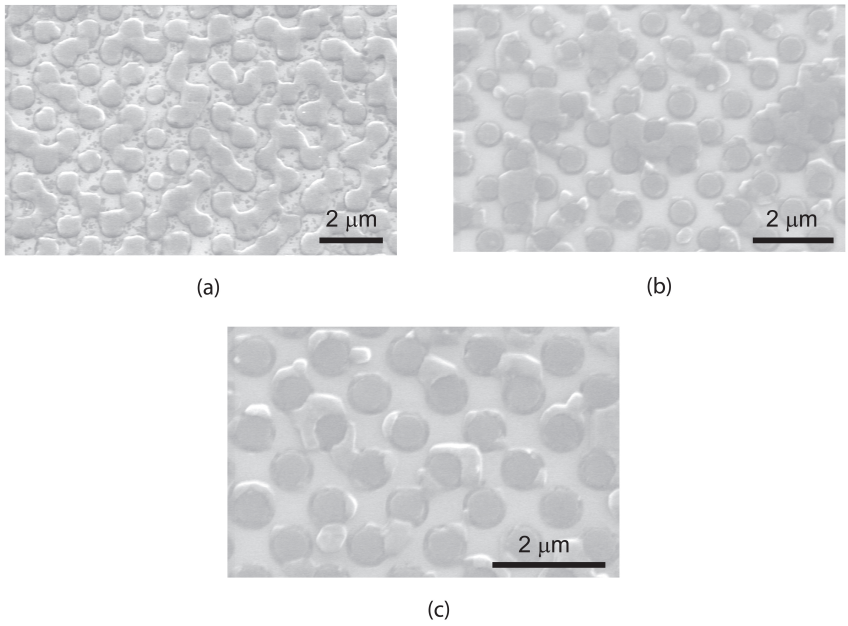


Figure 4.3: SEM micrographs of SPE growth for contact windows opened through (a) a 30-nm-thick SiO_2, (b) a 70-nm-thick SiO_2 or, (c) a 100-nm-thick SiO_2. In all cases, the α-Si and Al thicknesses were 100 nm and 200 nm, respectively, and the growth temperature was 400°C.

SiO_2 increases, the deposition of SPE-Si on SiO_2 is reduced. For thick SiO_2, the sidewalls, exposed to aggressive chemical etching, are larger and consequently the parasitic nucleation on SiO_2 can be enhanced. This leads to the formation of large polycrystalline Si island on SiO_2 initiated from the region closed to the contact windows edges (Figure 4.3c). Moreover, for much thicker dielectric layers, the issues related to the poor conformity of Al thin films deposited by PVD at the edges of the contact window, as discussed in Section 2.4.4, can also appear. The SEM analysis also confirms that the SPE-Si growth is initiated within the contact windows.

The influence of the α-Si layer thickness was also investigated. Three different thicknesses (20 nm, 50 nm, and 100 nm) have been deposited on the same test structure with a 200-nm-thick Al transport layer. A series of SEM images, representative of the three different situations after the growth sequence, are shown in

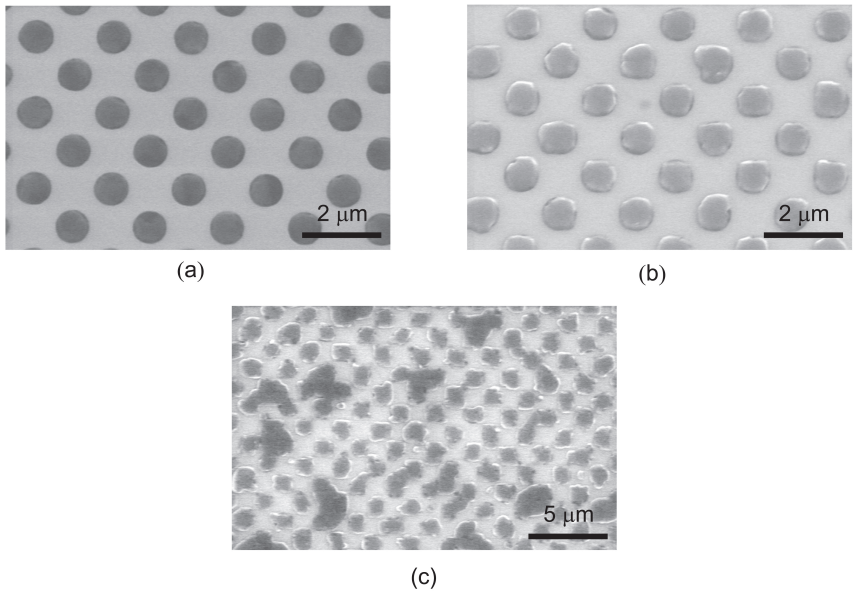


Figure 4.4: SEM micrographs of SPE-Si growth when (a) 20-nm-thick α-Si, (b) 50-nm-thick α-Si or, (c) 100-nm-thick α-Si, is deposited by PVD. In all cases, the thickness of the thermal SiO_2 was 30 nm, and the growth temperature was 400°C.

Figure 4.4. As expected, the volume of Si deposited on the Si substrate and SiO_2 scales with the α-Si layer thickness, i.e., more SPE-Si deposits on SiO_2 when the α-Si thickness increases. It is also noteworthy that, in all cases, the contact windows are entirely filled with an SPE-Si island, which substantiates the preferential deposition on the Si substrate and the key-role played by Si diffusion on the SiO_2 layer during the growth sequence.

A SEM view of the laterally overgrown SPE-Si on SiO_2, obtained in the case of an array of 770-nm-wide contact windows, a hole-pitch of 970 nm, and for an Al/α-Si layer-stack thicknesses of 200 nm and 100 nm, respectively, is shown in Figure 4.5. These overgrowth conditions were found as quasi-optimal for the corresponding Al/α-Si layer stack and SiO_2 step height which was about 27 nm. Initiated from the contact windows, SPE-Si overgrows laterally on SiO_2, and merges following a diagonal pattern corresponding to the (100) preferential orientation.

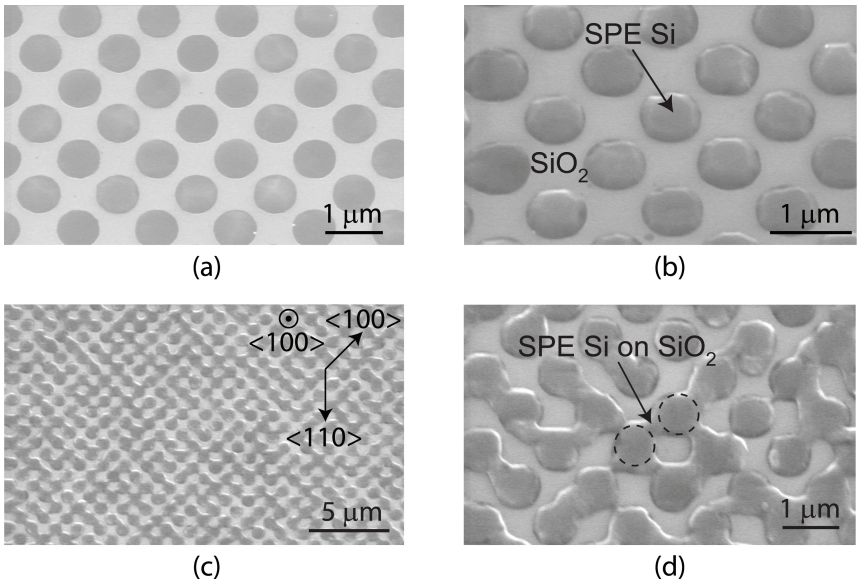


Figure 4.5: SEM micrographs showing the results of SPE growth at 400°C for 30 min when the thickness of the α-Si layer is (a) 20 nm, (b) 50 nm, (c) and (d) 100 nm. In all cases, the contact window width and pitch was 700 nm and 1.4 μm, respectively, and the thickness of the SiO_2 and Al layer was 30 nm and 200 nm, respectively.

4.2.3 Characterization of SPE-Si overgrowth on SiO_2

The crystallinity of the SPE-Si deposited on SiO_2 has been analyzed by EBSD. The results show that both the SPE-Si located within contact windows and that on SiO_2 are (100)-oriented (Figure 4.6). In particular, no grain boundaries in the SPE-Si film were found.

Additionally, the crystallinity of the SPE-Si deposited on SiO_2 was also investigated by transmission electron microscopy (TEM) analysis, including selected area diffraction (SAD) using a spot size as small as 200 nm. The SAD results, shown in Figure 4.7, confirm that the Si region deposited on SiO_2 is monocrystalline and (100)-oriented. The center spot in Figure 4.7b is much more intense due to the diffraction from the amorphous layer (PECVD) deposited above the SPE-Si as a scratch protection layer. However, micro-twin-like defects were sometimes observed on HR-TEM images at the boundaries between the SPE-

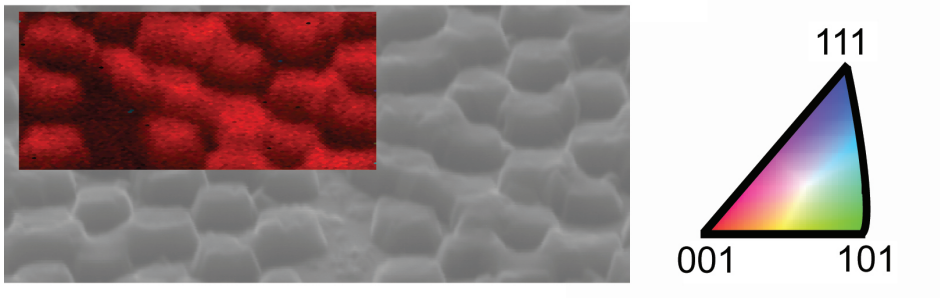


Figure 4.6: SEM micrograph of SPE-Si overgrowth on SiO_2 (with 75° tilt). Inset is the result of EBSD analysis, indicating the (100)-orientation (red) of the SPE-Si deposited both within the contact windows and on surrounding SiO_2, and the absence of grain boundaries in the overgrown region.

Si grown on Si and SiO_2, as shown in Figure 4.8. These defects do not appear sharp enough to be dislocations and they might also be induced by phenomena of stress-release during the TEM preparation. Further investigation is required to understand and control the presence of these defects.

The Al-doping of the as-grown SPE-Si regions has also to be taken into account before incorporating the SPE-Si on SiO_2 module into existing device process flows. As already discussed in Section 3.3, the elemental Al-concentration was measured to be about $1 - 2\times10^{19}$ cm^{-3} by secondary ion-mass spectroscopy (SIMS). As a front-end step, the high diffusivity of the Al in Si can be used for thermally driving the Al dopants out of the Si to obtain a very lightly doped SOI directly usable for further device fabrication. Moreover, as a back-end step, the low process temperatures involved enable the formation of high-crystallinity Si on SiO_2 regions directly usable for device fabrication.

4.3 Arbitrarily-shaped SPE-Si islands

If enough α-Si is provided, the growth model given in Section 2.3 predicts that a large variety of contact window geometries can be filled completely if (*i*) the nucleation on the surrounding SiO_2 is avoided, and (*ii*) the supply of Si to the central regions of the structure is not cut off by a too early filling of the perimeter regions. For an entirely selective deposition in the contact window, the quantity

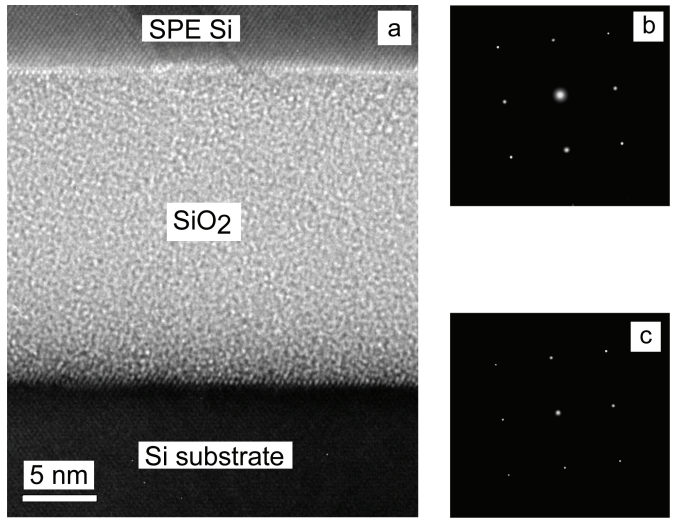


Figure 4.7: (a) High-resolution TEM image of the SPE-Si/SiO_2/Si substrate interfaces. Selective area diffraction (SAD) patterns obtained for the SPE-Si region (b) on the SiO_2, (c) on the Si substrate. The diffraction patterns are essentially identical.

of Si supplied must correspond to the volume of the contact region to be filled. In addition, the temperature-dependent deposition time must be long enough to complete the SPE-Si deposition. Using these guidelines and as shown in Figure 4.9, lines as narrow as 65 nm, which were defined by electron-beam lithography through SiO_2, were successfully filled selectively with high-quality SPE-Si. Also very large structures were filled, such as the ring-shaped contact windows. In this case, the quality of the epitaxial interface was checked by fabricating and characterizing p^+-n diodes, the I–V characteristics are shown in Section 5.2.4.

4.4 Conclusions

In this chapter, the flexibility of the aluminum-mediated SPE-Si technique was demonstrated through the implementation of different growth configurations. The lateral Si overgrowth was shown to be highly controlled by the process parameters, such as SiO_2 step height, or α-Si thickness. The crystallinity of SPE-Si deposited on SiO_2 has also been verified by EBSD and TEM: all confirm the fact that SPE-

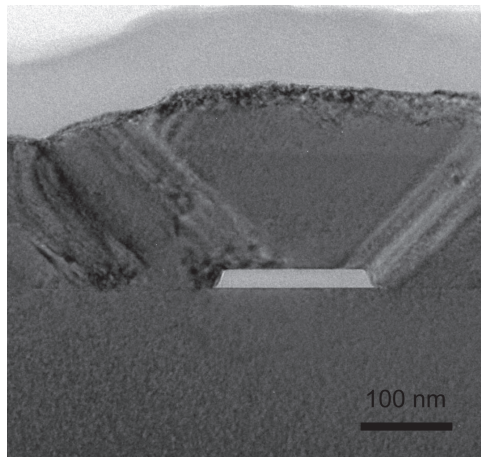


Figure 4.8: Low-resolution TEM image of SPE-Si on SiO_2.

Si keeps the same orientation of the substrate. The aluminum-mediated SPE-Si technique was also successfully extended to the filling of hundreds of μm-long ring structures and 65-nm wide contact windows. This demonstrates the potentiality of this technique for integration in many different situations.

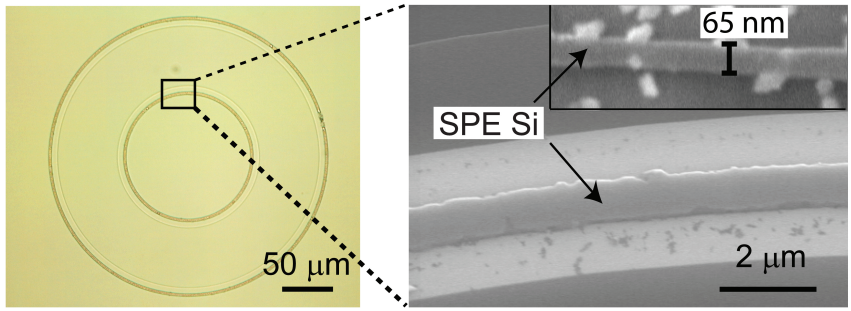


Figure 4.9: (a) Optical and (b) SEM micrograph of an SPE-Si region grown selectively within a 395-μm-long and 1-μm-wide ring-shaped window. The thicknesses of Al and α-Si were 100 nm and 75 nm, respectively. In the inset is shown an SEM micrograph of 65-nm-wide SPE-Si line, opened before growth by electron-beam lithography.

Chapter 5

Fabrication and electrical characterization of SPE-Si devices

5.1 Introduction

In this chapter, we present several examples of p^+ SPE-Si modules for integration in electrical devices: p^+-n diodes, ohmic contacts, laterally-contacted resistors and Si emitters for PNP bipolar junction transistors (BJTs). Moreover, the influence of growth temperature and dimensional shrinking on the device electrical behavior was also investigated. The knowledge gained by the characterization of these SPE-Si devices complements the analytical results presented in Chapter 3.

5.2 SPE-Si p^+-n diode

5.2.1 Diode fabrication

A schematic cross-section of SPE-Si through-wafer contacted p^+-n diodes, fabricated on a 2 – 5 Ω·cm n-type (100) Si substrate, is shown in Figure 5.1. The standard procedure to obtain SPE-Si islands locally positioned in contact windows through SiO_2 to the Si substrate has been already described in the Section 2.2. After growth and Al transport-layer removal in diluted HF 0.55%, a 375-nm-

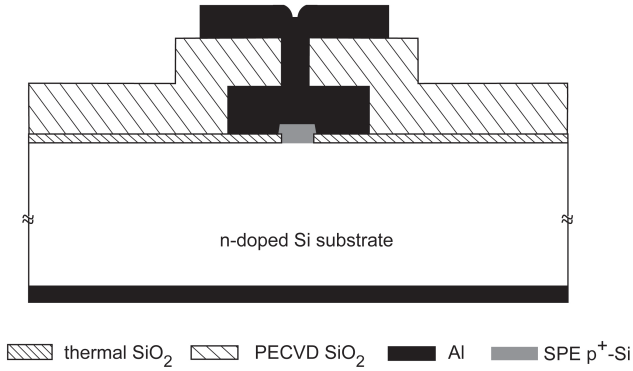


Figure 5.1: Schematic cross-section of a through-wafer contacted SPE-Si p^+-n diode.

thick Al (containing 1%Si) was deposited by PVD at 50°C, and patterned around the SPE-Si island in order to form a good electrical contact to the grown Si region. Indeed, the 30-nm-thick SiO_2 isolation layer has been exposed to plasma etching of the Al/α-Si layer stack, which may cause thinning of the SiO_2. In particular, the initial thermal SiO_2, of a thickness in the range of less than 10 nm after SPE-growth, Al transport removal and Al island patterning, was found to be leaky. To avoid any current leakage through this layer, an additional 150-nm-thick PECVD SiO_2 was then deposited at 400°C and patterned with contact windows to the already-formed Al island which covers the SPE-Si region. A second Al-layer was then deposited and patterned for forming the measurement bondpads.

5.2.2 I–V characteristics and ideality factor

In all cases, the measurements shown below have been carried out by the use of an HP4156A semiconductor parameter analyzer on a Cascade probing station equipped with a thermo-chuck. A representative example of the measured I–V characteristics of an SPE-Si p^+-n diode is shown in Figure 5.2. In this case, the p^+-region is formed by a 1×1 μm^2 SPE-Si island grown at 400°C. The ideality factor of the p^+-n diodes, measured from the slope of the I–V curve at V_D = 0.4 V, was found to be approximately 1.05, which is remarkably low for a 400°C process. The low leakage current indicates a very low density of generation/recombination

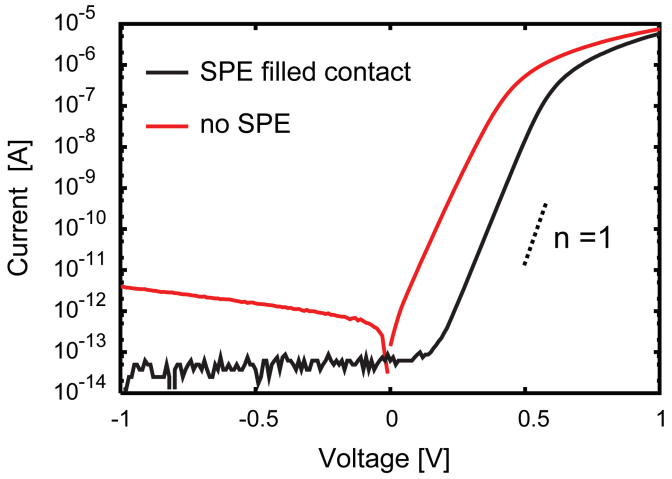


Figure 5.2: Measured I–V characteristics of a 1×1 μm^2 p$^+$-n SPE-Si diode. When no SPE growth is performed on the n-Si substrate doped to 2×10^{15} cm^{-3}, an Al/n-doped Si Schottky diode is measured.

centers in the depletion region, which only can be achieved by a low defect-density at the growth interface. This is noteworthy since the metallurgic junction is situated at the growth interface, which hence must be situated within the junction depletion region, as verified by TEM results shown in Section 3.2.4. As expected, when there is no SPE-Si island grown in the contact window, an Al to n-doped Si Schottky diode is formed that has a two-decades-higher saturation current. This is also shown in Figure 5.2.

5.2.3 Influence of the p$^+$-n junction area downscaling

The influence of the lateral junction dimensions on the measured p$^+$-n diode characteristics has been investigated by reducing the width of the contact windows down to 0.2 μm. These dimensions were not directly accessible by the use of the lithography equipment available at DIMES. Even though the on-mask width of the contact openings is varying from 0.1 to 3 μm, contact windows smaller than 0.6 μm cannot be patterned reliably in photosensitive resist with the available optical lithography tool. Instead, a mature SiN_x spacer technology already developed at DIMES was used to scale the width of the contact windows down to the 0.1 μm

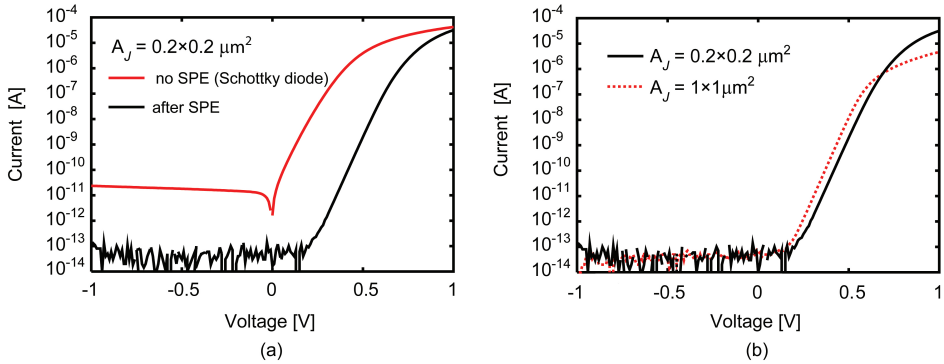


Figure 5.3: Measured I–V characteristics of through-wafer SPE-Si-based p^+-n diode (a) for a junction area (A_J) of 0.2×0.2 μm^2, and (b) for two different values of A_J. In all cases, the doping of the n-doped Si is $\sim 2\times10^{15}$ cm^{-3} and the SPE temperature was 400°C.

range [78]. The process flow including the use of SiN_x was already given in detail in Section 2.4.4.

The I–V characteristics measured on as-formed p^+-n diodes are shown in Figure 5.3. The ideality factor remains practically unchanged when the junction surface is decreased down to 0.2×0.2 μm^2, which demonstrates the high quality of the epitaxial growth at the contact window perimeter. This aspect is a very appealing property of the whole SPE-Si technology presented in this thesis. Moreover, the forward current of the 0.2×0.2 μm^2 SPE-Si diode, measured in the ideal region (V_D = 0.4 V) is approximately 5 times lower than that of the 1×1 μm^2 diode while the area is 25 times smaller. This is seen in Figure 5.4 where the measurement temperature dependence of the saturation current and ideality factor are shown. Over the whole temperature range the diode behavior is ideal. This result is in good agreement with the fact that, for such device dimensions and p^+-n doping level, the junction perimeter current will dominate over the area current and the perimeter ratio is 5.

5.2.4 Arbitrarily-shaped diodes

As seen in Section 4.3, a good understanding of the mechanisms governing the growth sequence makes it possible to apply the SPE technique to the case of an

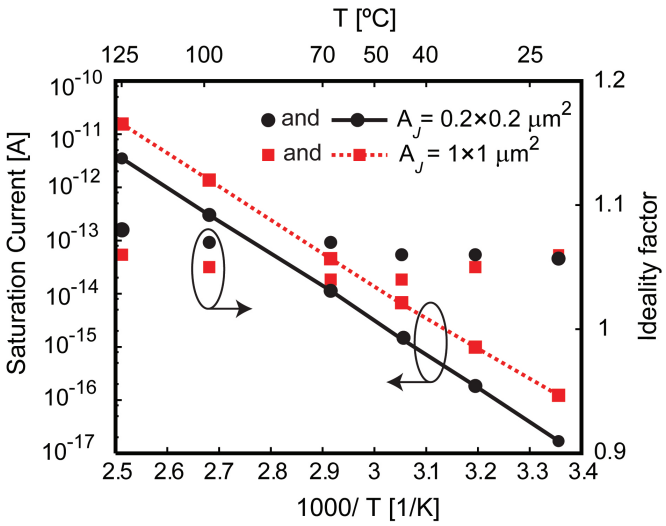


Figure 5.4: Measured saturation current for two different junction areas as function of the measurement temperature.

arbitrarily-shaped contact window. By predicting the Si amount necessary to fill contact windows of a given dimension, and adjusting the growth time and temperature, tens of μm-long ring-shaped p$^+$ SPE-Si islands were successfully formed as shown in Figure 4.9. On n-type substrates, these islands were contacted through the wafer. As seen in Figure 5.5, the ideality factor is essentially the same as for the small islands.

5.2.5 Breakdown voltage

In an asymmetric planar diode, the breakdown voltage V_{BR}, due to avalanching is, in general, given by the relation:

$$V_{BR} = \left(\frac{E_{BR}^2 \cdot \varepsilon_S \cdot \varepsilon_0}{2q} \right) \left[\frac{1}{N_A} + \frac{1}{N_D} \right] \tag{5.1}$$

where E_{BR}, ε_S, ε_0, N_A, and N_D are the electric field at breakdown, the dielectric constant of Si, the permittivity of free space, the doping in the p- and n-doped region, respectively.

When $N_A \gg N_D$, the breakdown voltage is primarily determined by the dop-

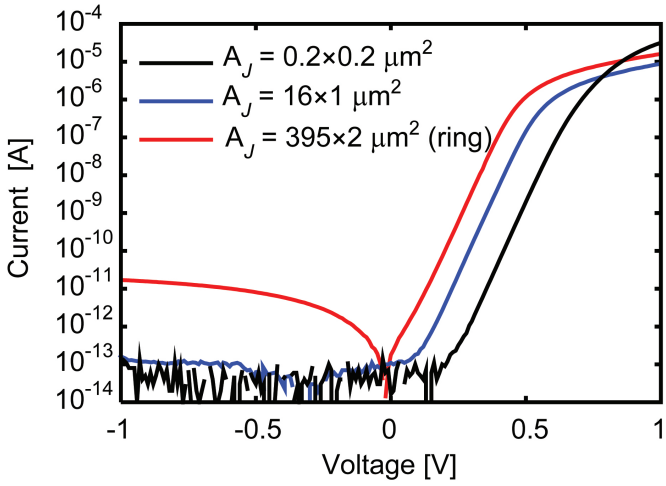


Figure 5.5: Measured SPE-Si p^+-n diodes I–V characteristics for three different geometries and junction areas A_J.

ing of the lightly doped bulk region. A representative example of the measured breakdown voltage is shown in Figure 5.6.

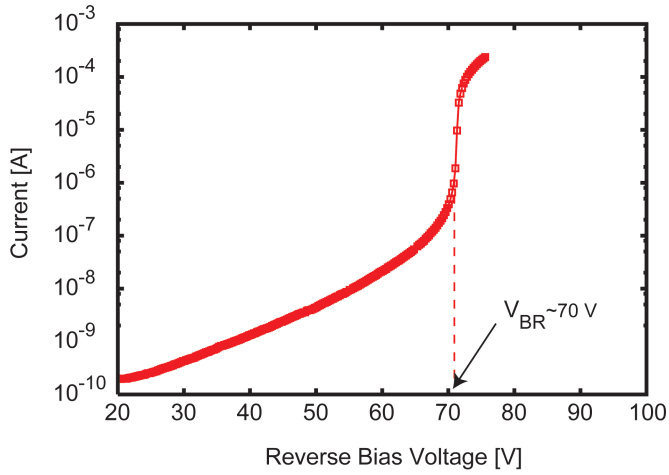


Figure 5.6: Measured reverse-bias I–V characteristic of SPE-Si p^+-n diode (A_J = 1×1 μm^2). A breakdown voltage of 71 V is measured at 25°C.

The breakdown voltage V_{BR} is about 71 V, which is in good agreement with

the theoretical value as given by the Equation 5.1, using $N_D = 2\times10^{15}$ cm^{-3}, and E_{BR} in the range of $2-3\times10^5$ V/cm. This is a further indication that there are no significant defects present to supply generation/recombination centers at the SPE-Si to substrate interface, which would lower the breakdown voltage with respect to the theoretical value.

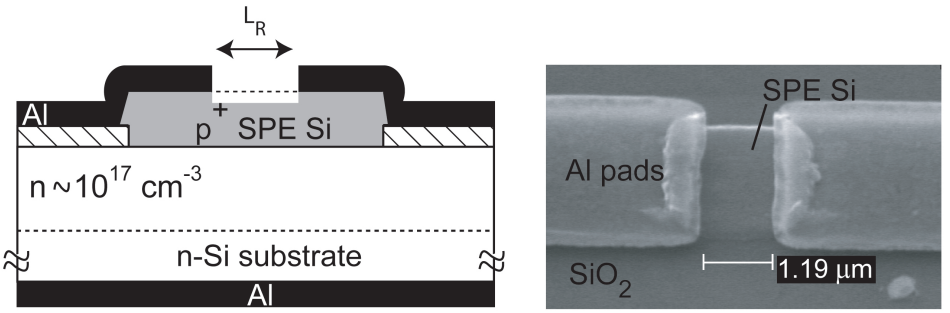


Figure 5.7: (a) Schematic cross-section of the laterally-contacted SPE-Si resistors fabricated. (b) Corresponding SEM micrograph. The height of the SPE-Si island is $\sim$ 120 nm.

5.3 Sheet resistance

In Section 3.3, it was shown by the use of SIMS that the elemental Al doping concentration in the grown-Si island is uniform with a level of a $1-2\times10^{19}$ cm^{-3}. On the other hand, the electrically-active Al-dopant concentration in the SPE-Si islands must be estimated electrically. This can be performed by measuring the resistance of laterally-contacted p$^+$ SPE-Si resistors.

5.3.1 Fabrication of laterally-contacted SPE-Si resistors

SPE-Si islands were formed at 500°C on n-type Si substrates with a doping of the top 0.3 μm of about 10^{17} cm^{-3}. This provides a good electrical isolation of the resistor to the substrate without causing excessive depletion of the p-doped region. After growth and Al transport-layer removal, the SPE-Si islands were then

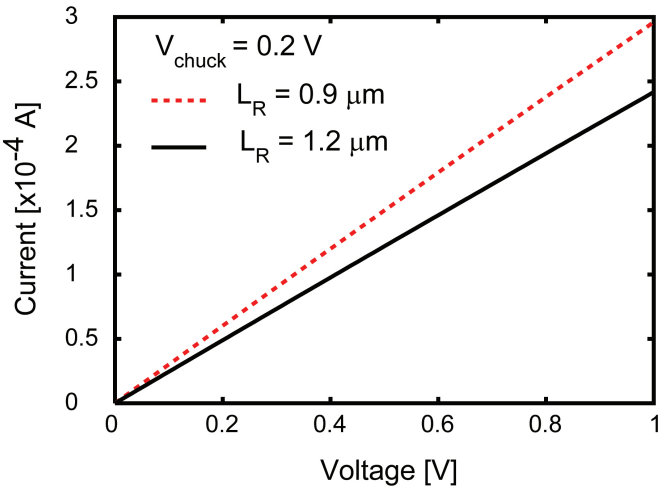


Figure 5.8: Measured I–V characteristics of laterally-contacted SPE-Si resistors for two different resistor lengths (L_R). For both devices, the height of the SPE-Si island is $\sim$ 120 nm.

covered with a 0.675-μm-thick Al layer, which was patterned by RIE selectively to the SiO_2, but non-selectively to the SPE-Si (Figure 5.7). In this manner, the resistor region and metal stack to contact the resistor are defined simultaneously. The etching into the SPE-Si island surface was measured on SEM images to be $\sim$ 20 nm deep. To directly measure the resistance of the SPE bulk-Si, arrays of laterally-contacted SPE-Si resistors with different geometries were fabricated.

5.3.2 I–V characteristics and sheet resistance measurements

The I–V characteristics were measured for resistors of different lengths L_R (Figure 5.8). From the measured resistance and knowing the corresponding window width, a sheet resistance value $R_s \sim 4\times10^3$ Ω/sq was extracted. Assuming that the SPE-Si islands are 120 nm high and using the resistivity value as a function of Al-dopant-concentration published by Galvagno *et al.* for Al-implanted Si, this corresponds to an aluminum doping of about 2×10^{18} cm^{-3} [80]. This value is in good agreement with the value reported in the literature for polycrystalline Si on SiO_2 obtained by aluminum induced crystallization [26]. This would also mean that the electrical activation level is less than 20% of incorporation level.

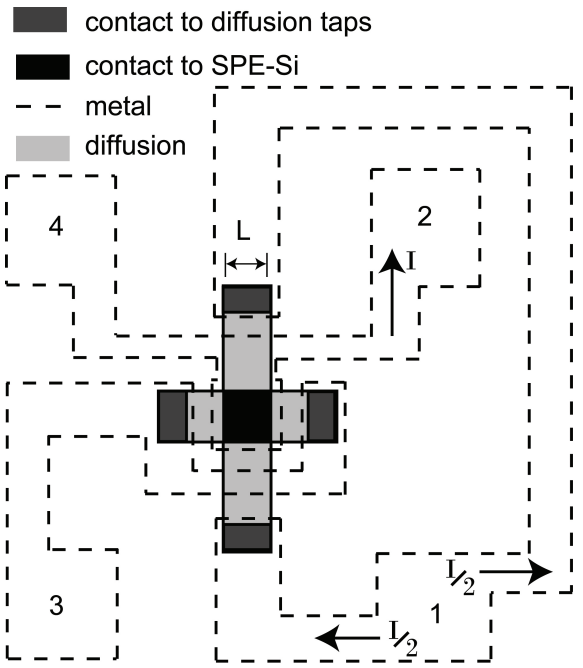


Figure 5.9: Schematic top-view of the Kelvin contact resistance test structure [79].

5.4 Aluminum to p$^+$ SPE-Si contact resistance

5.4.1 Kelvin test structures

For applications such as elevated source and drain or emitters in PNP SiGe HBTs, a doping level in the range of 10^{18} cm^{-3} is much lower than what it is usually aimed for. However, a high doping is often only necessary for decreasing the metallization to p-doped Si contact resistance R_C. Thus, an accurate measurement of the value of R_C is essential to complete the description of the electrical properties of Al-doped SPE-Si regions. Many approaches have been proposed in the literature to measure R_C. The commonly-used test structures for the extraction of R_C are the contact front-resistor, contact end-resistor, and cross-bridge Kelvin resistor [81]. The Kelvin test structure used in this thesis was developed particularly for measuring the contact resistance of regions that are self-aligned to the contact [75] and is shown in Figure 5.9. A cross section of the structure is also shown in Figure 5.10.

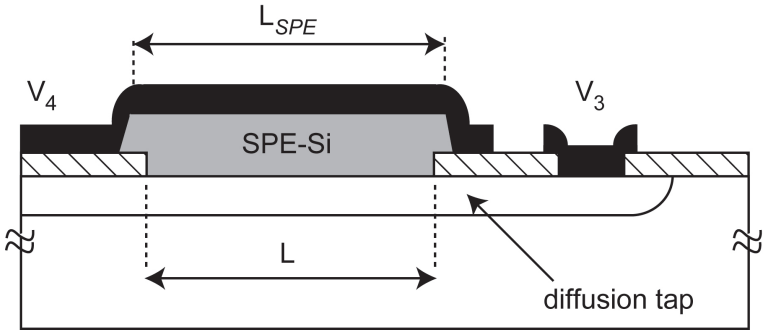


Figure 5.10: Schematic cross-section view of the Kelvin contact resistance test structure.

The measured value of R_K is determined as:

$$R_K = \frac{V_{34}}{I_{12}} \tag{5.2}$$

and consists of three components: the series resistance through the bulk SPE-Si region R_S, the actual contact resistance R_C to be estimated and a geometry-dependent parasitic resistance R_{GEOM}, as given by

$$R_K = R_S + R_C + R_{GEOM} \tag{5.3}$$

In the used Kelvin structure, the diffusion taps to the contact are low ohmic in order to decrease the parasitic currents around the contact that set the minimum for the measurable contact resistance. For this purpose, the diffusion tap cross is also designed as closely as possible around the contact under investigation. Practically, it was formed by boron-implantation dose of 3×10^{15} cm^{-2} at 15 keV, and activated by thermal annealing at 1050°C for 1 min. In this situation, it has been previously demonstrated by Nanver *et al.*, that the correction R_{GEOM} can be disregarded for ρ_C in the range of 10^{-7} Ω·cm^2 [79].

5.4.2 Contact resistance measurements

In the case of an SPE-Si island to Al layer Kelvin resistance measurement, the measured resistance R_K consists of two components, as given by the Equation

5.4:

$$R_K = R_S + R_C = R_S + \frac{\rho_C}{L^2} \tag{5.4}$$

where ρ_C is the specific contact resistivity.

The I–V characteristics of SPE contacts to p-doped bulk-Si regions show ohmic behavior. The contact resistance values determined from the Kelvin structure measurements, shown in Figure 5.11, show that the Al to SPE island contact resistivity is less than 10^{-7} Ω·cm^2 for SPE growth at 400°C and 500°C. Such a low value normally corresponds to a surface doping above 10^{20} cm^{-3}. The bulk activated doping was found to be no more than a few times 10^{18} cm^{-3}, which corresponds to an R_S of about 1.5×10^{-7} Ω for a 1×1 cm^2 contact. Therefore, the low resistivity extracted from the Kelvin resistance measurement is of the same order as the series resistivity. This suggests that the actual Al to SPE-Si contact resistivity is much lower than the measured value, which is dominated by the R_S. This could be explained by a phenomenon of segregation of Al dopant at the SPE-Si surface, inducing a much higher Al content and, thus, a higher electrical activity at the surface.

5.4.3 Influence of the annealing temperature

As can be seen in the Figure 5.11a, the measured Kelvin resistance slightly decreases when the SPE annealing temperature increases from 400°C to 500°C. This is probably due to the fact that the electrically active doping in the SPE-Si island slightly increases when the growth temperature increases, as shown by the Al solid-solubility in Si as a function of temperature (Figure 3.7). Indeed, when the growth temperature is increased from 400°C to 500°C, the resistivity of the bulk SPE-Si island decreases by $\sim$15%, which corresponds to a change of resistance of about 2 Ω for a 1×1 μm^2 contact window. This is in very good agreement with the resistance change shown in Figure 5.11a. Moreover, this also supports the assumption that the measured Kelvin resistance is essentially dominated by the series resistance of the bulk SPE-Si island, and that the contact resistance to p-doped Si formed with the Al-mediated SPE technique is extremely low.

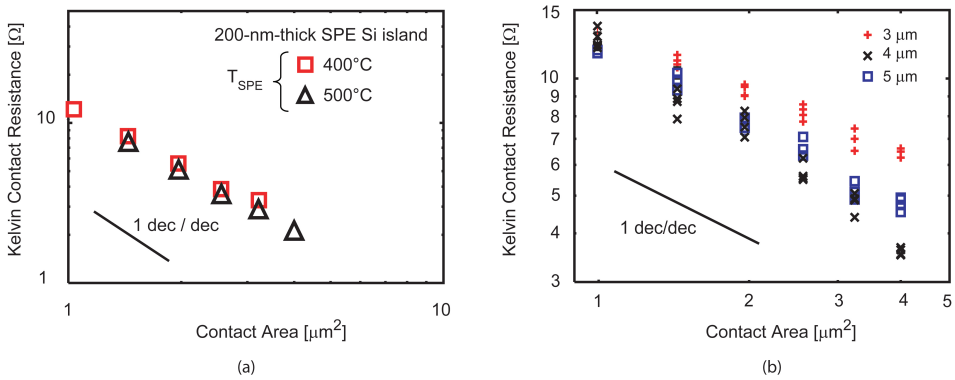


Figure 5.11: Measured Kelvin contact resistance of the Al to SPE p^+ Si islands (a) grown either at 400°C or 500°C, or (b) as a function of the Al/α-Si stack etch definition for a growth temperature of 500°C. In both cases, the growth was 20 min, the SPE island thickness was 200 nm.

5.4.4 Influence of the Al/α-Si etch-definition

The influence of the Al/α-Si layer-stack etch definition on the contact resistance measurements has also been studied. As seen in Figure 5.11b, the results show that the contact resistance of the Al to the SPE-Si decreases when the width of the Al/α-Si island increases. This can be explained by the phenomenon of lateral overgrowth, which has been described in more detail earlier in the Section 4.2. Indeed, the SPE-Si lateral overgrowth on the surrounding SiO_2, corresponding to $(L_{SPE} - L)$ in Figure 5.10, slightly increases when the Al/α-Si etch definition increases. Consequently, the SPE-Si surface to contact metallization slightly increases, and thus the resistance of the contact as a whole decreases. Assuming the resistivity of the SPE-Si region remains unchanged, which is reasonable since the growth temperature is the same, the change of the series resistance, of about 2–3 Ω, observed when the Al/α-Si is increased by a micron corresponds to a change of L_{SPE} of about 0.2 μm. This corresponds then to an overgrowth of 0.1 μm on SiO_2. This is in very good agreement with all the SEM-assisted SPE-Si width measurements.

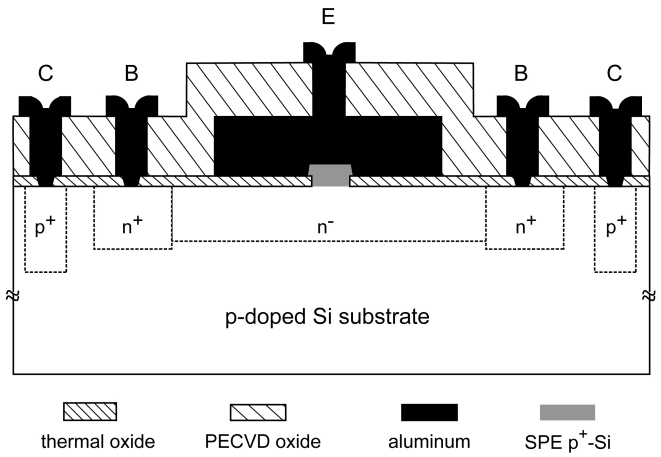


Figure 5.12: Schematic cross-section of the PNP BJT in which the emitter is formed by Al-mediated SPE. The base doping concentration is about 2×10^{17} cm^{-3}.

5.5 SPE-Si emitter bipolar junction transistor

5.5.1 BJT fabrication and characteristics

PNP BJTs with aluminum-doped SPE-Si emitters were fabricated. The intrinsic and extrinsic base, and the collector plug were first implanted and then thermally activated at 1050°C for 1 min before the SPE-emitter formation. The emitter contact was then opened through the SiO_2 to the Si substrate. After SPE-Si emitter formation, the implanted regions of the PNP were contacted, as shown on the schematic cross-section in Figure 5.12.

5.5.2 Electrical characterization

A 100-nm-thick SPE-Si island was used as emitter in a PNP BJT. An analysis of the transistor characteristics indicates near-ideal forward base and collector currents, and a current gain $h_{FE} = \frac{I_C}{I_B}$ of about 4 (Figure 5.13).

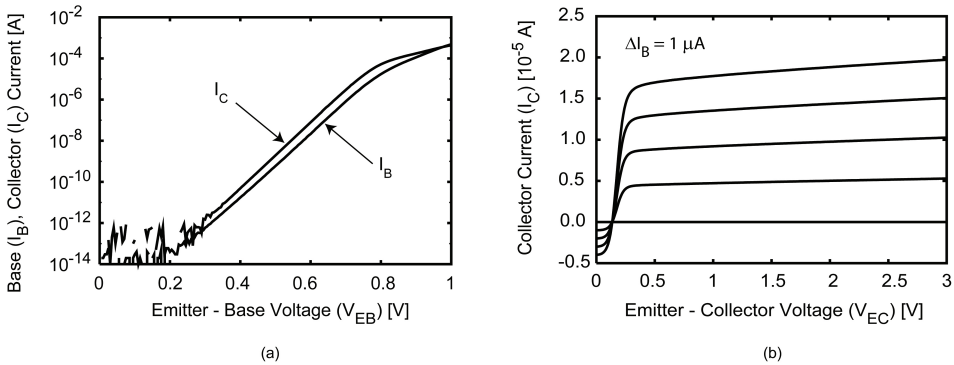


Figure 5.13: Measured (a) Gummel plot and (b) output characteristics of a representative PNP BJT with an emitter area (A_E) of 1×1 μm^2. The base doping concentration was 2×10^{17} cm^{-3}.

5.5.3 Influence of the SPE emitter thickness and growth temperature

Stable growth conditions were found that enabled control of both the height and the width of the SPE emitter. Transistors with a SPE-Si emitters of different widths have been characterized and practically ideal base current have been measured, as seen in Figure 5.14.

Moreover, SPE-Si islands as thin as 50 nm were used as a p^+ emitters. Emitter-base junctions with a 25-nm-thick p^+ regions were even successfully formed and characterized. The corresponding current gain was found to be low due to higher base current.

5.5.4 1-D device simulations

In this section, the possible use of aluminum-mediated SPE-Si islands as ultra-shallow Al-doped emitters in PNP SiGe HBTs is evaluated. For modeling of more complex devices such as SiGe HBTs, knowledge of the carrier lifetime τ and surface recombination velocity ν is essential. It has been possible to evaluate the value of these two parameters by (*i*) first extracting the laterally-uniform component of the base and collector current from measured Gummel plots of the fabricated BJTs of different emitter widths, (*ii*) then fitting the simulated I_B and I_C to the extracted values. These two successive stages are addressed in more

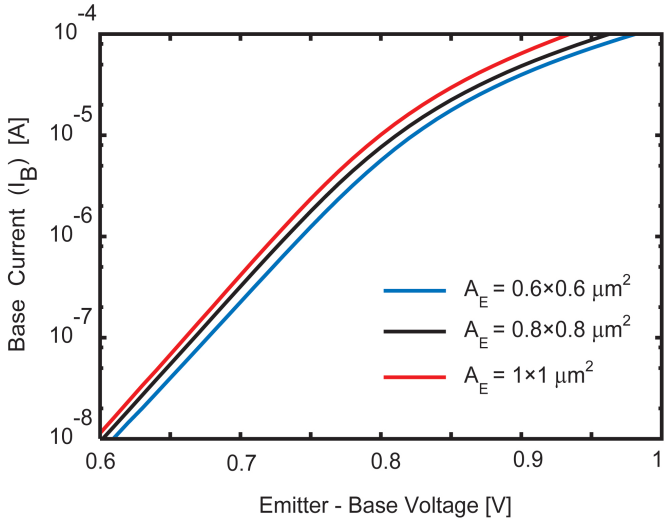


Figure 5.14: Base currents of devices with different emitter areas (A_E). The height of the emitter was 100 nm and the SPE growth temperature was 500°C.

detail below.

The measured currents can be generally modeled by the relation (5.5):

$$I = I_A \cdot A + I_P \cdot P + I_K \tag{5.5}$$

where I_A and I_P are the components that scale linearly with the area and perimeter, respectively, I_K is the current related to the corners, A and P are the area and the perimeter of the contact, respectively. A number of square-shaped emitters with on-mask length L_m from 0.6 to 1.6 μm have been fabricated and electrically characterized. The on-wafer L and on-mask L_m emitter lengths are related by

$$L = L_m + 2 \times \Delta L \tag{5.6}$$

where the length mismatch ΔL is unknown and dependent on the entire fabrication process. It is assumed that ΔL is independent of L_m, and, thus, for two devices with on-mask emitter lengths $L_{m,i}$ and $L_{m,j}$, can be derived from (5.5) that

$$\frac{I_j - I_i}{L_{m,j} - L_{m,i}} = I_A \cdot (L_{m,j} - L_{m,i}) + 4 \cdot I_A \cdot \Delta L + 4 \cdot I_P \tag{5.7}$$

Based on the equation (5.7), accurate values of the laterally-uniform component I_A of the base and collector currents have been extracted at constant V_{EB} from the slope of the curves shown in Figure 5.15 . Then, these values have been used in 1-D MEDICI simulation [82] to separately estimate the two available fitting parameters, i.e., the carrier lifetime and the surface recombination velocity. The entire fabrication process flow has been first simulated by TSUPREM4 to provide the 1-D emitter-base-collector doping profile [83]. This profile was imported in MEDICI device simulator to model the 1-D PNP device. A good fitting of the simulated and measured forward Gummel plots is achieved when the value of the surface recombination velocity ν ranges from 7×10^5 cm/s to 1.2×10^6 cm/s. For the evaluation of the minority carrier lifetime, ν was fixed to 10^6 cm/s.

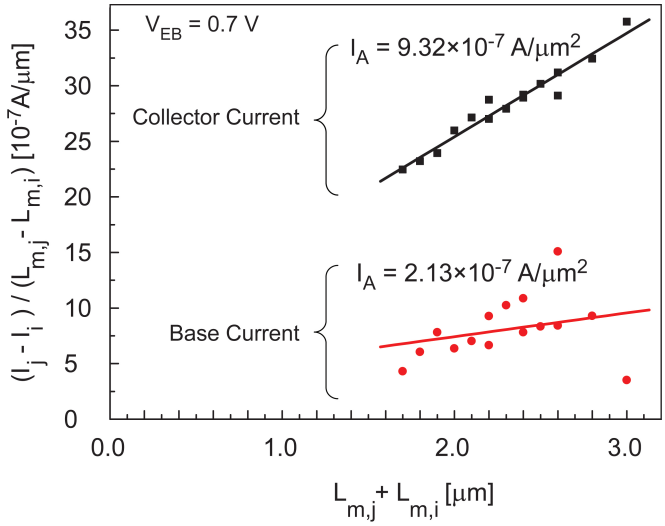


Figure 5.15: Measured base and collector currents for different emitter lengths for V_{EB} = 0.7 V and V_{CB} = 0 V, plotted to allow the determination of I_A from the slopes as given by (5.7).

The carrier lifetime τ was estimated to be around $2 - 3\times10^{-8}$ s, as seen from the results shown in Figure 5.16. This value corresponds to what would be expected for a B-doped high-quality monocrystalline Si.

The analysis of the I–V characteristics of a Si PNP with an Al-mediated SPE

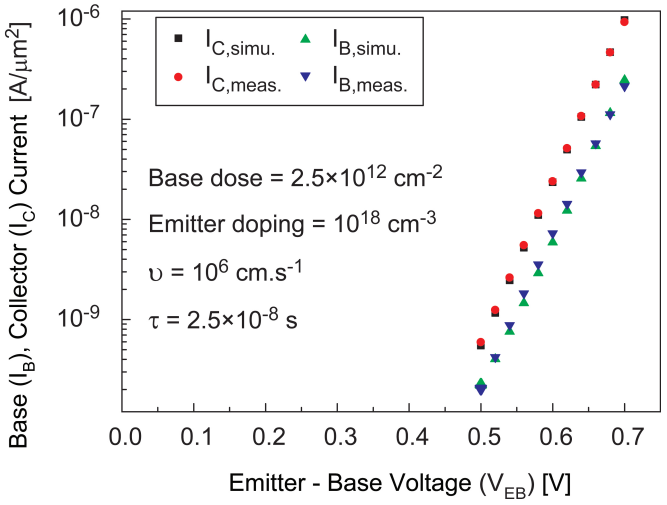


Figure 5.16: Simulated and measured Gummel plot showing a very good agreement after adjusting the two fitting parameters, i.e., the surface recombination velocity ν and the carrier lifetime τ . The emitter thickness is 100 nm and the base doping is 2×10^{17} cm^{-3}.

emitter region shows that the basic parameters of this Al-doped emitter are comparable to those of conventional B-doped emitters. The uniformity of the base current over the wafer is very good, showing that there is little variation in both these parameters and the emitter doping. From this analysis, it can be concluded that the SPE-emitters can be applied and modeled in the same manner as B-doped emitter regions. The SPE process itself is attractive because of its low processing temperature, damage-free junction, and abrupt doping profile. For the use in SiGe HBTs, it may be attractive to have a more highly-doped emitter which could be achieved, to some degree, by increasing the annealing temperature from the presently used 500°C to a value closer to the eutectic temperature of 577°C.

5.5.5 Reproducibility

The high quality of the SPE-Si has been demonstrated by local TEM analysis of the growth interface which, as discussed in Section 3.2.4, demonstrated the crystallinity of the material. The electrical device measurements give the possibility

to evaluate the material over the wafer and from wafer-to-wafer in an economic manner. The results support the idea that the epitaxial growth is well controlled and reliably of high quality.

The reproducibility of the SPE-Si properties were investigated by systematic wafer to wafer measurements of the base current I_B of the PNP BJT, which depends on the emitter properties as given by:

$$I_B = \frac{A_E\ q\ D_{nE}\ n_{iE}^2\ (e^{\frac{V_{BE}}{V_T}} - 1)}{N_E\ T_E} \tag{5.8}$$

where I_B is the base current, A_E the emitter area, D_{nE} the diffusion length of the minority carriers in the emitter, n_{iE} the intrinsic carrier density in the emitter, V_{BE} the emitter base voltage, V_T the thermal voltage, N_E the emitter doping, and T_E the emitter thickness.

The results of these measurements showed that, in the ideal region for V_{EB} = 0.6 V, the over-the-wafer-measured base current is very stable, I_B = 16 $\pm$ 2.8 nA (2σ), for a p^+ SPE-Si emitter width of 1×1 μm^2. The influence of the pre-SPE process steps (e.g., lithography, wet chemical over-etch) are also included in the given spread of I_B.

For several runs, the I_B and I_C and current gain h_{FE} were measured for different SPE-Si region with and Al/α-Si stack edge definition. Practically, the base and collector currents were normalized to the emitter area by estimating $A_B^{eff}(W_E)$ and $A_C^{eff}(W_E)$, respectively, whereby process-induced deviations from the mask sizes and the hole current spreading around the emitter are taken into account. The results of the measured current gain h_{FE}, base and collector current densities, J_B and J_C respectively are presented in the Figure 5.17.

When the amount of Si deposited is not sufficient to entirely fill the contact opening, the emitter-base junction forms a Schottky diode, which results in higher base current and, thus, in the absence of current gain. This corresponds to the region in black in Figure 5.17. Optimized growth conditions are localized in the region in white, which corresponds to entirely filled p^+ SPE-Si emitter.

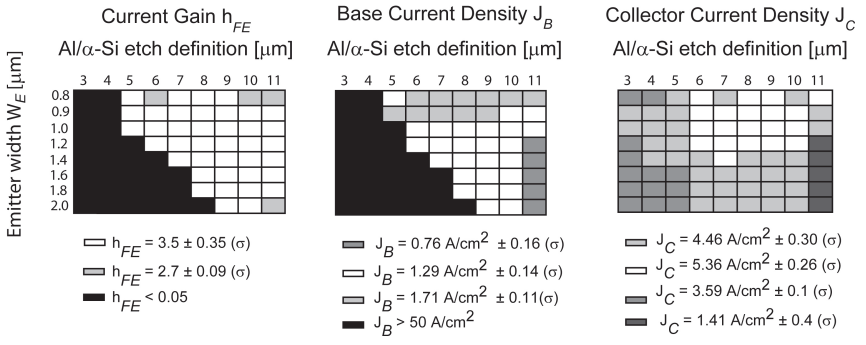


Figure 5.17: Measured base current density J_B, collector current density J_C and current gain h_{FE} of PNPs in an array with different contact window widths W_E to Al/α-Si etch definition ratios.

5.6 Conclusions

In this chapter, the fabrication and electrical characteristics of several SPE-Si based devices were presented. Near-ideal I–V characteristics and low ohmic contacts were reproducibly formed, which confirmed the Al-mediated SPE technique enables the formation of directly usable high-quality monocrystalline Si. Moreover, the SPE-Si quality was found not to be affected by the SPE-island width downscaling, which gives promises of possible integration of SPE-Si modules both in front- and back-end processes for nanoscale device fabrication.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

The main conclusions of this thesis are:

- Al-mediated solid-phase epitaxy is a very promising technique for forming monocrystalline p^+-Si junctions at temperatures below 500°C. In particular, these low processing temperatures, for which no Al diffusion into the Si substrate occurs, offer the possibility to locally form ultra-abrupt doping transitions both in front- and back-end processing. The junction depth, precisely controlled by the height of the Al transport layer thickness, can also be scaled down due to the high controllability achieved by the PVD deposition equipment.

- The SPE-Si growth mechanism is not selective to Si, i.e., the deposition is also observed on the SiO_2 surrounding the contact windows to the Si substrate. However, a very good selectivity to Si can be achieved by keeping the dielectric surface smooth and optimally structuring the Al/α-Si layer stack and the contact windows to be filled.

- The Al doping in the SPE-Si region has been quantitatively determined on the basis of a state-of-the-art SIMS analysis. The doping level in SPE-Si

was found to be very uniform and in the range of 1–2$\times 10^{19}$ cm^{-3}. However, the activated doping, extracted from the electrical characterization of laterally-contacted SPE-Si based resistors, was found to be less than 20% of the concentration measured by SIMS and in agreement with the equilibrium solid-solubility limit of Al in Si at the SPE growth temperature.

- Devices have been fabricated using the p^+ SPE-Si module and electrical characterization confirmed that a practically defect-free epitaxial growth was obtained, also at the contact-window perimeter. In particular, p^+-n diodes, with an ideality factor of 1.04, were successfully obtained using a maximum temperature of 400°C. Moreover, low-ohmic contacts were also formed and the specific contact resistivity to the SPE-Si region was found to be about 10^{-7} Ω·cm^2. This value includes also the bulk SPE-Si resistance which is of the same order as the measured contact resistance. All the results suggest the actual contact resistivity is very low, probably due to the presence of an Al-rich region at the surface of the SPE-Si island.

- The growth sequence of Al-mediated SPE-Si functions with equally good results when the contact windows in which the nucleation is initiated are downsized. Thus, this technique appears very promising for nanotechnology applications. In particular, the I–V characteristics remain practically ideal when the SPE-Si island width is reduced to the sub-200 nm range. With respect to other methods applied to form nanostructures, this technique presents also the advantage of a possible straightforward incorporation into CMOS process flows and devices.

- The SPE technique has been successfully implemented for the location-controlled formation of SPE-Si on SiO_2. This is achieved by lateral overgrowth of SPE-Si on SiO_2 using the contact window height, width and pitch, and the Al/α-Si layer stack properties as a control parameters.

6.2 Recommendations for future work

- The implementation of this module in a complementary process, which would demand a n-doped SPE-Si process, remains very challenging. Dif-

ferent solutions can be investigated, such as the use of an n-doped Si target during the PVD deposition of the α-Si layer-stack or the use of a metal layer which could act as n-dopant for Si (such as antimony). More generally, methods of changing the doping of Al-mediated c-Si layers, to drive out the Al dopants as well as to achieve more activated dopants, are still needed for giving more flexibility before further integration.

- A better understanding of the mechanisms governing the deposition of monocrystalline Si on dielectric such as SiO_2, SiN_x, and aluminum nitride (AlN) remains essential for achieving larger SPE-SOI regions.

- The qualitative analysis (doping, crystallinity, controllability), as well as the process parameters influencing the formation of SPE-Si obtained after growth at 300°C and below, would be interesting for future incorporation of SPE-Si modules into silicon-on-glass Si/SiGe HBT processes that are running in the DIMES cleanrooms.

- The implementation of the metal-mediated SPE-Si growth techniques to other systems, such as Al/Ge or Al/Si/Ge, might also be worth investigating.

- Even though it potentiality has been demonstrated for many low-thermal budget applications in which high-crystallinity material is required, the incorporation of Al-mediated SPE-Si modules into more complex devices such as Si/SiGe HBTs, n-channel JFETs or PMOS devices would be of interest for demonstrating the performance enhancement that can be achieved with such a low-temperature TED-free process.

- Further SIMS doping profiling needs to be performed to clearly identify the doping at the surface of the SPE-Si islands.

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Summary

Title: Aluminum-Mediated Selective Solid-Phase Epitaxy of High-Quality Silicon Diodes

by: Yann Civale

The downscaling of CMOS transistor dimensions makes the need of new techniques for forming ultrashallow ultra-abrupt junctions very high. Several methods are currently investigated and some of them give good promise of meeting the requirements defined by the International Technology Roadmap for Semiconductors (ITRS). In this thesis, a new technique is presented: it is a novel low-temperature method of growing Si based on the crystallization of amorphous silicon (α-Si) by solid-phase-epitaxy (SPE) using an aluminum (Al) layer as a transport medium. Chapter 1 gives the general context of this study by addressing the general trends in the field of ultrashallow junctions. Particular attention is also paid to recently-developed techniques for forming semiconducting nanowires, the synthesis mechanism of which has similarities with the Al-mediated SPE-Si growth.

In Chapter 2, a model for the Al-mediated SPE growth mechanism is proposed based on experimental and theoretical considerations. The situation where SPE of Si is induced on a monocrystalline Si surface, either on uniform wafers or in contact windows to the Si through an SiO_2 layer, is treated. The successive stages of the SPE-Si sequence are observed by scanning electron microscopy (SEM) and described thermodynamically. Moreover, basic considerations of surface energies enable a preliminary explanation of the preferential deposition along the edges of the windows etched through the silicon dioxide (SiO_2). The process parameters influencing the properties of the SPE-Si islands are also given: in particular, the dielectric surface state greatly influences the growth selectivity since any defects at the surface of the SiO_2 are favorable sites for parasitic nucleation of polycrys-

talline Si. The soft landing procedure used during plasma etching of the windows to the Si substrate, which consists in a 4-minute dip-etching in hydrofluoric acid (HF) 0.55%, is also addressed in this chapter. The results show that no significant change in the growth sequence is observed if the soft landing is not applied. The influence of other growth process parameters, such as the Al/α-Si island width, the SiO_2 step height, and the downsizing of the window, is also addressed.

In Chapter 3, the properties of the Si obtained by Al-mediated SPE-Si are described in detail. The crystallinity has been investigated locally by three different techniques: Raman spectroscopy, electron back-scattering diffraction (EBSD), and high-resolution transmission electron microscopy (TEM). All these techniques confirm that the deposition on the Si substrate is epitaxial. On the other hand, knowledge of the Al-doping concentration in the SPE-Si is also essential when implementing the SPE process module in devices. A novel dopant quantification, based on a secondary-ion mass spectroscopy (SIMS) analysis of a Si region containing 100 identical SPE-Si islands, has also been realized. The theoretical and practical issues related to this SIMS dopant profiling are explained. The results indicate a highly-uniform Al-dopant concentration in the SPE-Si region, in the range of 10^{19}cm^{-3}. The abruptness of the SPE-Si based junction is also verified using an in-house capacitance–voltage (C–V) profiling method. The results demonstrate that ultra-abrupt junctions can be reliably formed by the use of the Al-mediated SPE technique at 400°C.

In Chapter 4, two implementations of the Al-mediated SPE technique are presented. In the first, the SPE-Si lateral overgrowth is controlled for forming hundreds-of-nanometer-wide monocrystalline-Si (c-Si) regions on SiO_2. The process parameters influencing the SPE-deposition of Si-on-insulator, such as the window pitch and width, and the SiO_2 thickness, are presented and a practically-ideal set of parameters is given. The crystallinity of such SPE-Si on SiO_2 is confirmed by both EBSD and high-resolution TEM. In the second implementation, the SPE-Si technique described in Chapter 2 and 3 is applied to the case of arbitrarily-shaped contact windows. The SEM micrographs obtained when the SPE growth is performed on hundreds-of-micron long ring-shaped contact windows, as well as the ones obtained in the case of 65-nm-wide openings exposed by electron beam lithography are presented. The results substantiate that the phenomena governing the aluminum-mediated SPE-Si growth are well controlled for a large variety of configurations, and thus make the entire technique a very promising module for further integration in both front- and back-end processes.

Chapter 5 deals with the use of SPE-Si modules as building blocks for semi-

conductor devices. The fabrication process flows and the results of the electrical characterization of the fabricated SPE-Si based devices are given. The results show that near-ideal p^+-n diodes can be formed on n-doped Si at 400°C with a remarkably low ideality factor of about 1.04, and low-ohmic contacts are reliably obtained on p-doped Si with a noteworthy low contact resistivity, below 10^{-7} $\Omega{\cdot}cm^2$. The I–V characteristics of laterally-contacted SPE-Si based resistors also indicate that the electrically-active Al dopant concentration is in the range of 10^{18} cm^{-3}. At last, SPE-Si regions are used as emitters in bipolar junction transistors (BJTs). The measurement results of fabricated transistors display near-ideal Gummel plots and a high reproducibility from wafer-to-wafer and run-to-run. Further integration into more complex devices such as Si/SiGe heterojunction bipolar transistors (HBTs) is evaluated using MEDICI device simulation tools, and the results show that the Al-doped Si emitters can be treated as if they were conventional boron-doped emitters as far as HBT device modeling is concerned.

Chapter 6 presents the conclusions of this thesis and the recommendations for future work are also given.

Samenvatting

Titel: Door aluminium gemedieerde selectieve vastefase-epitaxie van hoogwaardige siliciumdiodes

Door: Yann Civale

De reductie van CMOS-transistorafmetingen noopt tot nieuwe technieken voor de vorming van ultra-ondiepe, ultra-abrupte juncties. Op dit moment worden verscheidene methodes onderzocht. Een aantal hiervan zal naar verwachting voldoen aan de eisen van de International Technology Roadmap for Semiconductors (ITRS). In dit proefschrift wordt een nieuwe techniek gepresenteerd: een nieuwe lage temperatuur methode om silicium (Si) te groeien op basis van de kristallisatie van amorf silicium (α-Si) door vaste fase-epitaxie (SPE) met gebruikmaking van een aluminium (Al) laag als transportmedium. Hoofdstuk 1 schetst de algemene context van dit onderzoek aan de hand van een bespreking van de algemene trends op het gebied van ultra-ondiepe juncties. Ook wordt speciale aandacht besteed aan recentelijk ontwikkelde technieken voor de vorming van halfgeleidende nanodraden, waarvan het groeimechanisme overeenkomsten vertoont met de door Al gemedieerde SPE-Si-groei.

In hoofdstuk 2 wordt op basis van experimentele en theoretische overwegingen een model voorgesteld voor het door Al gemedieerde SPE-groeimechanisme. De situatie wordt besproken waarin SPE van Si wordt opgewekt op een monokristallijn Si-oppervlak, hetzij op uniforme wafers, hetzij op Si in siliciumdioxide contactgaten. De opeenvolgende stadia van het SPE-Si-proces worden waargenomen met behulp van scanning electronenmicroscopie (SEM) en thermodynamisch beschreven. Voorts maken fundamentele beschouwingen over oppervlakte-energieën een inleidende verklaring mogelijk van de voorkeursdepositie langs de randen van de gaten die in het siliciumdioxide (SiO_2) zijn geëtst. Ook worden de pro-

cesparameters gegeven die de eigenschappen van de SPE-Si-eilanden beïnvloeden: in het bijzonder is de dielektrische oppervlaktetoestand sterk van invloed op de groeiselectiviteit, omdat onregelmatigheden in het oppervlak van het SiO_2 geschikte locaties zijn voor de vorming van parasitaire kernen van polykristallijn Si. Ook de "zachte-landing"-procedure wordt in dit hoofdstuk behandeld. Deze wordt toegepast tijdens het plasma-etsen van de gaten in het SiO_2 tot op het Si-substraat. Dit etsproces bestaat uit een 4 minuten durende onderdompeling in waterstoffluoride (HF) 0.55%. De resultaten laten zien dat er geen significante verandering in de groeisequentie wordt waargenomen als de 'zachte landing' niet wordt toegepast. De invloed van andere groeiprocesparameters, zoals de breedte van het Al/α-Si-eiland, de hoogte van de SiO_2-stap, en de verkleining van het gat, komt ook aan de orde.

In hoofdstuk 3 worden de eigenschappen van het door Al-gemedieerde SPE-Si verkregen Si in detail beschreven. De kristallijne toestand is lokaal onderzocht met drie verschillende technieken: Ramanspectroscopie, electron backscattering diffractie (EBSD), en hoge resolutie transmissie elektronenmicroscopie (TEM). Al deze technieken bevestigen dat de depositie op het Si-substraat epitaxiaal is. Anderzijds is ook de kennis van de Al-doopstofconcentratie in het SPE-Si essentieel wanneer de SPE-procesmodule in devices wordt toegepast. Ook is een nieuwe doopstofkwantificering gerealiseerd. Deze is gebaseerd op een analyse met secundaire-ionen-massaspectroscopie (SIMS) van een Si-gebied dat 100 identieke SPE-Si-eilanden bevat. De theoretische en praktische kwesties die samenhangen met deze SIMS-doopstofprofilering worden verklaard. De resultaten wijzen op een uiterst uniforme Al-doopstofconcentratie in het SPE-Si-gebied, in de orde van 10^{19} cm^{-3}. De abruptheid van de op SPE-Si gebaseerde junctie wordt ook geverifieerd door middel van een intern uitgevoerde capaciteits-spannings-(C-V) profileringsmethode. De resultaten laten zien dat ultra-abrupte juncties op betrouwbare wijze kunnen worden gevormd door middel van de Al-gemedieerde SPE-techniek bij 400°C.

In hoofdstuk 4 worden twee implementaties van de Al-gemedieerde SPE-techniek gepresenteerd. In de eerste wordt de laterale overgroeiing van SPE-Si gecontroleerd voor de vorming van honderden nanometers brede monokristallijne-Si (c-Si)-gebieden op SiO_2. De procesparameters die de SPE-depositie van Si-on-insulator benvloeden, zoals de onderlinge afstand en de breedte van de gaten, en de dikte van het SiO_2, worden gepresenteerd en er wordt een in praktisch opzicht ideale verzameling parameters gegeven. De kristalliniteit van dergelijk SPE-Si op SiO_2 wordt bevestigd met zowel EBSD als hogeresolutie-TEM. In de

tweede implementatie wordt de SPE-Si-techniek die in de hoofdstukken 2 en 3 is beschreven, toegepast op de case van willekeurig gevormde contactgaten. Aan de orde komen de SEM-micrografen die worden verkregen wanneer de SPE-groei wordt uitgevoerd op honderden microns lange, ringvormige contactgaten. Ook wordt ingegaan op de resulterende micrografen in het geval van 65 nm-grote, door elektronenbundellithografie getoonde openingen. De resultaten bevestigen dat de verschijnselen die de alumnium-gemedieerde SPE-Si-groei beheersen, goed zijn gecontroleerd voor een grote verscheidenheid aan configuraties. Dat maakt de gehele techniek tot een veelbelovende module voor verdere integratie in zowel front-end- als back-end-processen.

Hoofdstuk 5 behandelt het gebruik van SPE-Si-modules als bouwstenen voor halfgeleiderdevices. Aan de orde komen de processtromen voor fabricage en de resultaten van de elektrische karakterisatie van de gefabriceerde, op SPE-Si-gebaseerde devices. De resultaten laten zien dat bijna-ideale p^+-n-diodes kunnen worden gevormd op n-gedoteerde Si bij 400°C met een opvallend lage idealiteitsfactor, ongeveer 1.04. Ook blijkt dat op betrouwbare wijze laag-ohmische contacten worden verkregen op p-gedoteerde Si, met een opmerkelijke lage contactweerstand, namelijk minder dan 10^{-7} $\Omega{\cdot}\mathrm{cm}^2$. De I-V-karakteristieken van lateraal gecontacteerde, op SPE-Si gebaseerde weerstanden geven ook aan dat de elektrisch actieve Al-doopstofconcentratie in de orde van 10^{18} cm^{-3} ligt. Tenslotte worden SPE-Si-gebieden gebruikt als emitters in eenvoudige bipolaire junctietransistors (BJT's). De meetresultaten van de gefabriceerde transistors vertonen bijna-ideale Gummel-plots en een hoge wafer-to-wafer- en run-to-run-reproduceerbaarheid. Verdere integratie in complexere devices zoals Si/SiGe heterojunctie bipolaire transistors (HBT's) wordt geëvalueerd met gebruikmaking van MEDICI-device simulatiesoftware. De resultaten laten zien dat de Al-gedoteerde Si-emitters kunnen worden behandeld alsof zij conventionele boor-gedoteerde emitters zijn, voor zover het gaat om HBT-devicemodellering.

In hoofdstuk 6 worden de conclusies van dit proefschrift gepresenteerd en worden aanbevelingen gedaan voor toekomstig werk.

List of Abbreviations

Al: aluminum
Ag: silver
Au: gold
A_B: base area
A_C: collector area
A_E: emitter area
BJT: bipolar-junction transistor
B: boron
CMOS: complementary metal oxide semiconductor
CNT: carbon nanotube
CVD: chemical vapor deposition
C-V: capacitance voltage
CHF_3: trifluoromethane
Cu: copper
C_2F_6: hexafluoroethane
D: electric displacement
DIMES: Delft Institute of Microsystems and Nanoelectronics
D_{nE}: diffusion length of the minority carriers in the emitter
D_0: diffusion coefficient
D-SIMS: dynamic secondary ion mass spectroscopy
E: electric field
E_A: activation energy
E_{CR}: electric field at breakdown
EBSD: electron back scattering diffraction
Fe: iron
FEM: finite element modeling
FET: field-effect transistor
Ge: germanium
HBT: heterojunction bipolar junction transistor
HF: hydrofluoric acid

HR-TEM: high-resolution transmission electron microscopy
H_3PO_4: phosphoric acid
H_2: hydrogen
h_{FE}: current gain
ITRS: international technology roadmap for semiconductors
IC: integrated circuits
I_B: base current
I_C: collector current
I_A: component of the total current that scales linearly with the area
I_P: component of the total current that scales linearly with the perimeter
I_K: current related to the corners
I-V: current-voltage
JFET: junction field effect transistor
LPCVD: low-pressure chemical vapor deposition
MIC: metal-induced crystallization
MOSFET: metal oxide semiconductor field-effect transistor
n_{iE}: intrinsic carrier density in the emitter
N_E: emitter doping
Ni: nickel
NW: nanowire
N_2: nitrogen
PECVD: plasma-enhanced chemical vapor deposition
PVD: physical vapor deposition
RIE: reactive ion etching
RTP: rapid-thermal annealing
R_{OL}: overlap resistance
R_{CO}: contact resistance
R_{EXT}: extension resistance
SAD: selective area diffraction
Sb: antimony
SEG: selective epitaxial growth
SPE: solid phase epitaxy
SEM: scanning electron microscopy
SiGe: silicon germanium
SiO_2: silicon dioxide
Si: silicon
SIMS: secondary ion mass spectroscopy
SiN_x: silicon nitride
SiH_4: silane
S/D: source and drain

T_E: emitter thickness
TED: transient enhanced diffusion
TEM: transmission electron microscopy
TFT: thin film transistor
Ti: Titanium
TiN: Titanium nitride
T_C: crystallization temperature
VLS: vapor-liquid-solid
VSS: vapor solid-solid
V_T: thermal voltage
W_E: emitter width
V_{EB}: Emitter-Base Voltage
V_{CB}: Collector-base Voltage
α-Si: amorphous silicon
ϵ_{Si}: permittivity of Si
ϵ_0: permittivity of free-space
ν: surface recombination velocity
τ: minority carrier lifetime
ρ_C: specific contact resistivity

List of Publications

Journals

1. Y. Civale, L.K. Nanver, C. Biasotto, and V. Jovanović, "Versatile sub-500°C silicon solid-phase epitaxy lateral overgrowth for silicon-on-insulator applications," *to be submitted to Electrochemical and Solid-State Letters*, 2008.

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Acknowledgements

There are not so many places like DIMES, where Ph.D students can propose new concepts and have the possibility to be involved, from the mask designing to the electrical measurements and the final packaging, in the entire device fabrication process. I really enjoyed working at DIMES. Also because I found there a very nice research environment. The results shown in this thesis would not have been obtained without the contribution of many people. It is time to express here my gratitude to them.

I first would like to deeply thank my promotor Prof. dr. Lis Nanver for her great supervision. In this very wide project, she gave me the freedom to pursue my ideas, which has made this research very personal. Moreover, her passion for silicon device technology, her enthusiastic guidance and her daily-basis interest for my numerous experiments have been a permanent source of motivation and ambition. Moreover, I express my gratitude for her patience and her availability for reviewing and improving all my technical writings.

I would like to thank the Stichting voor Fundamenteel Onderzoek der Materie (FOM) for funding this research.

I would like to acknowledge Prof. Lina Sarro and Prof. dr. ir. Cees Beenakker for giving me the opportunity to pursue my PhD research at DIMES and for creating the inspiring atmosphere I enjoy so much for more than four years.

I would like to thank Prof. dr. ir. Jan Slotboom, Prof. dr. ir. Ronald Dekker, Prof. dr. ir. Rob Wolters, Prof. Peter Hadley, Prof. Leo Miglio and Dr. Volker Schmidt for their interest in my research and their participation in my promotion committee.

The cleanroom work has been essential for the completion of my project. Also, I would like to thank all the DIMES ICP-cleanroom staff. In particular, I would like to thank Hugo Schellevis for his advices and his interest for my work. Thanks are also due to Tom Scholtes for his guidance in the cleanroom, and his interest for what I was doing there. I would also like to thank Silvana Milosavljević for introducing me to a consistent cleanroom work and her availability for helping me with all process-related issues. Many thanks go to Bert Goudena, Alex van

den Bogaard, Dr. Henk van Zeijl, Charles de Boer, Ruud Klerks, Wim Wien, John Slabbekoorn, Jan Groeneweg, Cassan Visser, Mario Laros, Wim van der Vlist, Loek Steenweg, Jan Cornelis Wolff, Johan van der Cingel for their assistance with processing. Wim van der Vlist and Loek Steenweg are also acknowledged for their assistance with dicing and packaging my samples. Peter Swart and Sebastiaan Maas are acknowledged for their help with electrical measurements.

I would like to thank all the former and present post-doctoral researchers and PhD students I have met during my stay at DIMES: special thanks to Michael Wank and Luigi La Spina, my office-mates at DIMES. Thanks are due to Dr. Vladimir Jovanović, Viktor Gonda, Cleber Biasotto, Gianpaolo Lorito, and Miloš Popadić for their contribution to my work. Chen Tao, Dr. Nobuyuki Matsuki and Olindo Isabella are acknowledged for their assistance with EBSD and AFM analysis, respectively. Francesco Sarubbi is also acknowledged for his help with C-V measurements.

I also would like to thank Dr. Nebojša Nenadović for the consideration he had for me when I had to face the troubles caused by Mother Nature. I did not forget it.

I would like to thank Guglielmo Vastola for the very nice and fruitful collaboration on the understanding of the Al-mediated SPE-Si growth mechanism. Thanks are also due to Rani Mary-Joy who performed her MSc. thesis under my supervision.

I would like to thank Jan-Chris Staalenburg, Karl Agatz, Wim Tiwon and Rino Martillia for keeping our computer systems running. Marian Roozenburg-de Bree, Marysia Langendijk-Korzeniewski, and Tamara den Hartog are acknowledged for their help with administrative work.

Special thanks to my football team-mates, the “regulars”: Gennaro Gentile, Alessandro Baiano, Mauro Marchetti, Fabio Santagata, Sadek Guenaneche, Marcel Steenwijk and Giacomo Perfetti, as well as the many occasional players for the funny evenings and the few victories we had together. Thanks also to Yann Dufournet, and my friends from the 20th floor.

In spite of the distance, I always feel very closed to my family. Also, I would like to first thank my girlfriend Aurélie. Her constant support, her patience and her encouragements to pursue my objectives have been very important for me over the past few years.

Many thanks go to my brother Eric and my sister-in-law Virginie for their encouragements. Thanks are also due to my nephew Ugo and the newly-born niece Romane who daily enlighten our family.

At last, I would like to express my gratitude to my parents Christiane and Robert. Your discrete presence and your unconditional support have been essential for me for so many years. I always feel very lucky for having such great

people keeping an eye on me. This gives me the feeling that there is nothing I can overcome. Maman, Papa, merci aussi de m'avoir encouragé à ne pas douter de ces valeurs simples qui m'ont permis de surmonter, jusqu'ici, toutes les épreuves. Sachez que tout cela n'aurait été possible sans vous.

About the author

Yann Civale was born in Sète, France, on May 29, 1979. In December 2003, he became Ingénieur from the Ecole Centrale Marseille, in France after the completion of his thesis with Philips Research Laboratories, in Eindhoven, The Netherlands, on the development of polycrystalline-silicon and aluminum thermoelectric micro-generators for autonomous microsystems. He conducted the fabrication, the electrothermal characterization and the device optimization by the use of the substrate-transfer-technology.

In January 2004, Yann Civale joined the Faculty of Electrical Engineering, Mathematics, and Computer Science in Delft University of Technology, where he started research towards his Ph.D degree at the Delft Institute of Microsystems and Nanoelectronics (DIMES). At the Laboratory of Electronic Components, Technology and Materials (ECTM), his research focused on an innovative sub-500°C crystalline Si growth technique for forming ultrashallow abrupt junctions. He also investigated the integration of Si-nanopillar diodes using MEDICI device simulation. From 2006 to 2007, Yann Civale was also co-responsible of the DIMES IC Technology course for MSc. students.

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