Temperature Sensors and Voltage References Implemented in CMOS Technology

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***Abstract*—This paper reviews the concepts, opportunities and limitations of temperature sensors and voltage references realized in CMOS technology. It is shown that bipolar substrate transistors are very suited to be applied to generate the basic V_{BE} and PTAT voltages. Furthermore, it is shown that dynamic element matching and auto-calibration can solve the problems related to mismatching of components and $1/f$ noise. The effects of mechanical stress are a major source of inaccuracy. In CMOS technology, the mechanical-stress effects are small, as compared to those in bipolar technology. It is concluded that, with low-cost CMOS technolog, rather accurate voltage references and temperature sensors can be realized.**

***Index Terms*—Bandgap references, smart temperature sensors, temperature sensors, voltage references.**

I. Introduction

In CMOS technology, both MOS and bipolar transistors can be applied to generate the basic signals for temperature sensors and voltage references [1]–[4]. In case of MOS transistors, the basic signals are derived from the threshold voltage and the mobility. In the bipolar transistors the base-emitter voltage and the saturation current is used for the extraction of the basic signals. It appears that the base-emitter voltage and saturation current of the bipolar transistors show better temperature characteristics than the threshold voltage and mobility of the MOS transistors. Thus, most of the circuits of temperature sensors and voltage references apply bipolar transistors as the basic components. In this paper, the attention is mainly focused on the achievements in circuit design of the temperature sensors and bandgap references, applying bipolar transistors as basic components.

The designers of both integrated temperature sensors and bandgap-voltage references take advantage of a unique property of a bipolar transistor: the base-emitter voltage provides us with two intrinsic physical references, being the thermal voltage kT/q, which is proportional to the absolute temperature (PTAT), and the bandgap voltage V_{go}. In [5]–[7], the principles and typical features of these circuits have been reviewed. Many of the presented circuits offer smart solutions to eliminate the effects of specific component nonidealities or to optimize the device and circuit behavior for a specific technology. In general, it appears that the accuracy and long-term stability of conventional CMOS bandgap-voltage references are much less than that of bipolar ones. The low accuracy of the CMOS references is due to mismatching of components, drift, temperature effects, $1/f$ noise, and mechanical stress. Recently, in [4], [8]–[11], it has been shown that a major part of the CMOS problems can be solved by using auto-zeroing, auto-calibration, signal chopping, and by dynamic element matching. This paper reviews these novel dynamic signal-processing techniques. When we consider an ideal signal processing, the overall accuracy will be limited by the accuracy of the basic signals. These basic signals are the base-emitter voltage V_{BE} of a bipolar substrate transistor and the difference ΔV_{BE} of two of these base-emitter voltages. From these two voltages, the intrinsic signals, the thermal voltage kT/q, and the bandgap voltage V_{go} are extracted. This paper presents novel results of an experimental and theoretical study of the accuracy of these basic signals for CMOS technology. Furthermore, it is shown how these signals can be processed without losing accuracy. The presented signal-processing method takes advantage of the powerful features of microcontrollers for algorithmic processing.

II. Basic Principles and Device Characterization

A. Basic Principles

The principles of CMOS bandgap references are similar to those of bipolar ones. Fig. 1 shows basic schematics of some conventional bandgap reference circuits implemented in bipolar and CMOS technologies, respectively. In both circuits, a compensating voltage $V_C(T)$ is added to $V_{BE}(T)$ to compensate for at least the first-order temperature dependence of $V_{BE}(T)$. This correction voltage is obtained by amplifying the difference $\Delta V_{BE} = (kT/q)\ln p$ of these base-emitter voltages of two transistors operated at unequal collector-current densities with ratio p. In this way, an output voltage V_{ref} is obtained for which it holds that

$$V_{ref} = V_{BE}(T) + V_C(T) = V_{BE}(T) + A\,\Delta V_{BE}(T), \quad (1)$$

where A denotes an amplification factor. The analysis presented in this paper refers to NPN transistors. In case of PNP transistors, the opposite signs for the current and voltage direction holds true.

For instance, in the circuit of Fig. 1(a) the action of the current mirror (Q_3, Q_4) ensures that the ratio of the collector currents of Q_1 and Q_2 remains constant. Neglecting the influence of the

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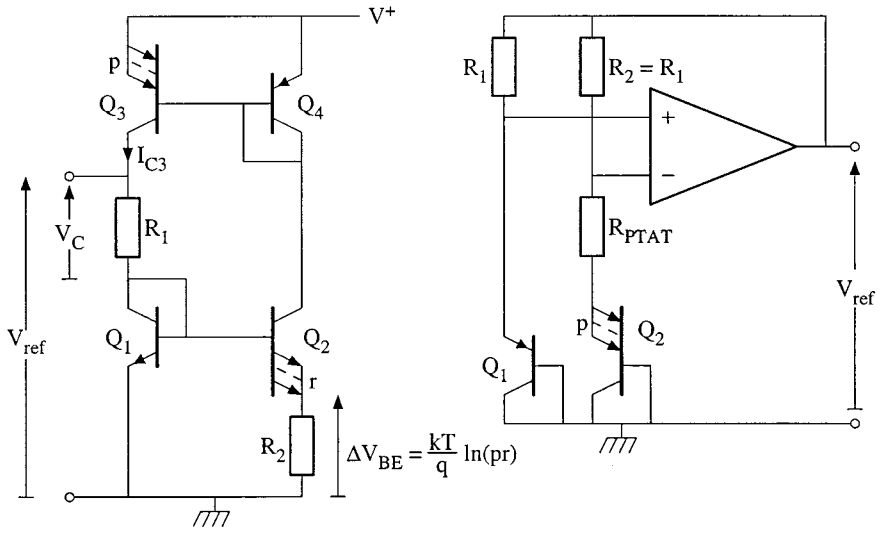


(a) (b)

Fig. 1. Simple bandgap-reference circuits, implemented in (a) bipolar technology and (b) CMOS technology.

base currents and base-width modulation for the voltage ΔV_{BE} across R_2, we find that

$$\Delta V_{BE} = \frac{kT}{q} \ln(pr), \tag{2}$$

where r and p denote the saturation-current ratios I_{S2}/I_{S1} and I_{S3}/I_{S4} of (Q_2, Q_1) and (Q_3, Q_4), respectively. For the output voltage V_{ref}, it holds that

$$V_{ref} = V_{BE1} + V_C = V_{BE1} + p\frac{R_1}{R_2}\frac{kT}{q} \ln(pr). \tag{3}$$

Considering CMOS technology, lateral as well as substrate transistors can be applied. The (vertical) substrate transistors have the better performance with respect to nonidealities of the $I_C(V_{BE}, T)$ characteristics [7]. Therefore, this type of transistor is preferred to generate the V_{BE} and $V_{\rm PTAT}$ voltages. Because all of the collectors of the substrate transistors are connected to the common substrate, special amplifier configurations are required to amplify the PTAT voltage. Fig. 1(b) shows a basic configuration for a CMOS bandgap reference. The generated output amounts to

$$V_{ref} \cong V_{EB2} + \left(1 + \frac{R_2}{R_{\rm PTAT}}\right)(V_{\rm PTAT} + V_{OS}) \tag{4}$$

where $V_{\rm PTAT} = (kT/q)\ln p = (V_{EB1} - V_{EB2})$ and V_{OS} is the offset voltage of the amplifier A.

In the configuration of Fig. 1(b), the current density ratio of Q_1 and Q_2 equals their emitter-area ratio. The main problems of the traditional CMOS bandgap references are caused by the nonidealities of the applied amplifier. Recently, Bakker *et al.* [10] showed how to reduce the offset problem, using a nested-chopper instrumentation amplifier. This solution is very suited for real-time signal processing. However, the errors introduced by gain inaccuracy are not eliminated. In Section III of this paper, it will be shown how to reduce both, gain and offset errors, using dynamic techniques. In these dynamic circuits, the accuracy is limited by that of the basic signals $V_{BE}(T)$ and $\Delta V_{BE}(T)$.

In integrated temperature sensors, the same principles and circuit are used as in bandgap references. The main difference between both types of circuits is that, in bandgap references, the PTAT voltage $A\Delta V_{BE}$ is added to the base-emitter voltage V_{BE}, in order to compensate for its temperature coefficient, while in temperature sensors, the base-emitter voltage V_{BE} is subtracted [5] from the PTAT voltage $A\Delta V_{BE}$ in order to enhance the temperature coefficient. In the next sections, it will be shown that for both circuits the aspects concerning accuracy, calibration, and long-term stability are closely related.

B. Characterization of $V_{BE}(T)$ and $\Delta V_{BE}(T)$

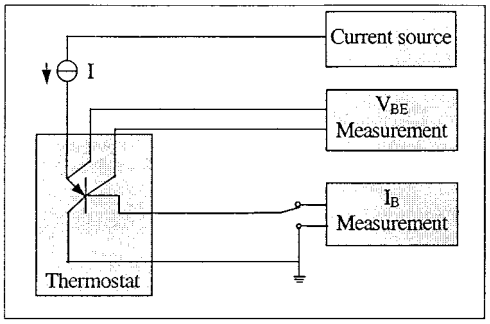
In order to characterize $V_{BE}(T)$ and $\Delta V_{BE}(T)$ for CMOS substrate transistors, we performed a number of measurements for transistors made in a 0.5 μm CMOS process of Alcatel microelectronics [12]. The test setups are shown in Fig. 2(a) and (b), respectively. In the setup of Fig. 2(b), it holds that $I_2 = 3I_1$. The switch unit is used to enable two alternating cross connections of the two current sources. After averaging the effect of a small mismatching between the transistor, Q_1 and Q_2 are eliminated.

As a result, Fig. 3 shows the measured ΔV_{BE} voltage normalized with respect to an ideal PTAT voltage $V_{\rm PTAT\_i}$ versus the current I_1, for various temperatures.

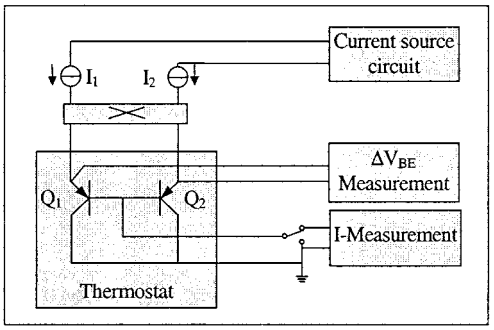
At current levels $I_C > 10\,\mu$A, a large deviation from the ideal value is found. For the main part, this is due to the effect of the base resistances, which causes an error $\Delta(I_B R_B)$ equal to

$$\Delta(I_B R_B) = I_{B2} R_{B2} - I_{B1} R_{B1}. \tag{5}$$

It can be shown that the so-called high-level injection only occurs at much higher current levels ($I_{kF} \approx 4$ mA). The value of R_B can be calculated using the data plotted in Fig. 3, together with the data of $I_B(I_E)$. Subtracting the values of $\Delta(I_B R_B)$



(a)



(b)

Fig. 2. Test setups to measure (a) $V_{BE}(T)$ and (b) $\Delta V_{BE}(T)$.

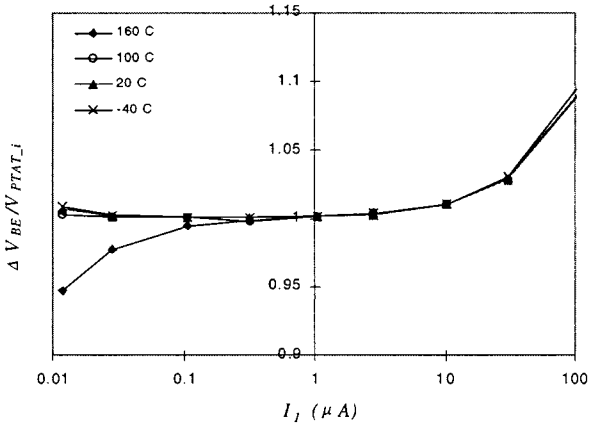


Fig. 3. Measured $\Delta V_{BE}(T)$ voltage normalized with respect to an ideal PTAT voltage versus the biasing current.

from the measured values of ΔV_{BE} results in the data plotted in Fig. 4 versus the absolute temperature T.

These results allow us to improve the model of $\Delta V_{BE}(T)$ by introducing the so-called emission coefficient n [12], according to the equation

$$\Delta V_{BE} = \frac{nkT}{q} \ln\left(\frac{J_1}{J_2}\right) \tag{6}$$

where J_1 and J_2 represent the current densities of Q_1 and Q_2, respectively.

Physically, the nonunity of n can be explained from the temperature dependency of the depletion-layer width [13]. From Fig. 4, it can be concluded that $n \approx 1.001$. Furthermore, it can be concluded that over the temperature range 250 K $< T <$ 430 K, the remaining relative errors in $\Delta V_{BE}(T)$ are less than 400×10^{-6}.

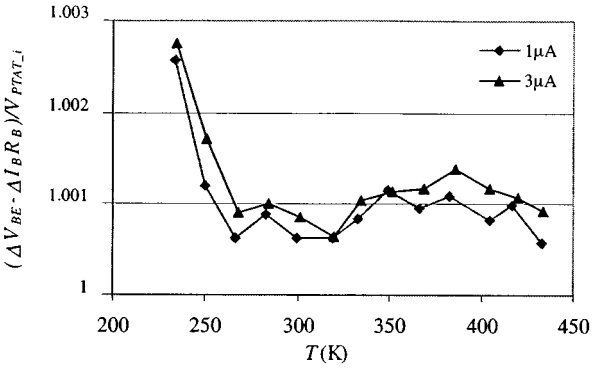


Fig. 4. Corrected $\Delta V_{BE}(T)$ value versus the temperature.

Next, the $V_{BE}(I_C, T)$ characteristics have been evaluated. The measurement results show that the temperature dependency satisfies the well-known equation [5], [12]

$$V_{BE} = V_{g0}\left(1 - \frac{T}{T_r}\right) + \frac{T}{T_r} V_{BE}(T_r) - \eta \frac{kT}{q} \ln\left(\frac{T}{T_r}\right) + \frac{kT}{q} \ln\left(\frac{I_C(T)}{I_C(T_r)}\right), \tag{7}$$

where

$V_{BE}(T_r)$ base-emitter voltage at a certain reference temperature;T_r,

V_{g0} extrapolated bandgap voltage at 0 K;

η constant representing the curvature of the $V_{BE}(T)$ characteristic.

From our measurement results, we found the experimental values: $V_{go} = 1.141$ V and $\eta = 4.3$. These values are close to those of NPN transistor fabricated in bipolar technology [5].

From the $V_{BE}(I_C)$ data, the high-level injection parameter I_{KF} and the emission coefficient n can be derived. For our devices under test, it has been found that $I_{KF} = 3.7$ mA and $n = 1.001$. The latter value is equal to that found from the ΔV_{BE} measurements.

C. Calibration and Trimming

To maximize the accuracy of a bandgap reference or integrated temperature sensor, it is necessary to calibrate the devices. Without calibration, the spread in V_{BE} and ΔV_{BE} will cause a temperature-dependent error in the output voltage. In bandgap references, with proper calibration at a certain reference temperature T_r, the linear temperature dependence of $V_{BE}(T)$ is compensated by the amplified PTAT voltage $A_1 \Delta V_{BE}(T)$. When the bipolar transistor is biased with a PTAT current, this results in an output voltage V_{ref}, which equals [6], [7]

$$V_{ref} = V_{g0} + (\eta - 1)\frac{kT_r}{q} + (\eta - 1)\frac{k}{q}\left(T - T_r - T \ln \frac{T}{T_r}\right). \tag{8}$$

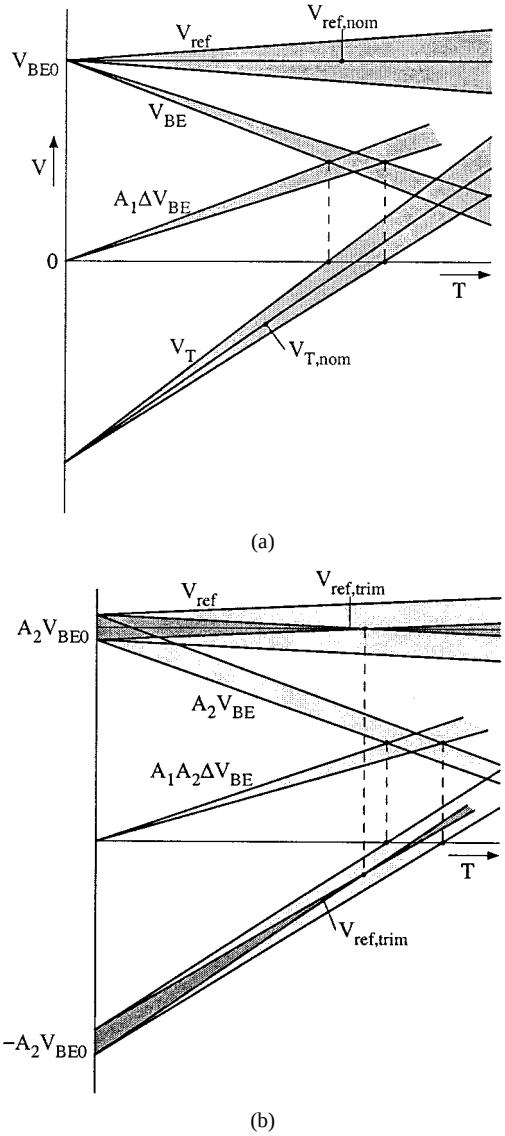


Fig. 5. Effect of spreading in V_{BE} and $A\Delta V_{BE}$ at the output voltage V_{ref} of a bandgap reference and at the output voltage V_T of a temperature sensor, before and after calibration (the curves are shown as their linear extrapolated approximations); (a) for an unscaled device ($A_2 = 1$); (b) for a scaled devices ($A_2 \neq 1$).

To increase the temperature sensitivity and to adjust the offset voltage in temperature sensors, the base-emitter voltage is subtracted from the amplified PTAT voltage (Fig. 5).

The nonlinearity in the $V_{BE}(T)$ characteristic does not affect the calibration procedure. Therefore, for simplicity, we discuss the calibration methods using linearly extrapolated approximations of the temperature characteristic. For this simplification, we approximate the nonlinear $V_{BE}(T)$ characteristic by its tangent for an arbitrary reference temperature T_r. This tangent intersects the vertical axis at the voltage V_{BE0}. From Eq. (8), it is found that

$$V_{BE0} = V_{g0} + (\eta - 1)\frac{kT_r}{q} \tag{9}$$

where it holds that $V_{BE0} \cong 1.24$ V.

To trim a linear (temperature) characteristic, two points have to be fixed. Fortunately, in the case of bandgap references and

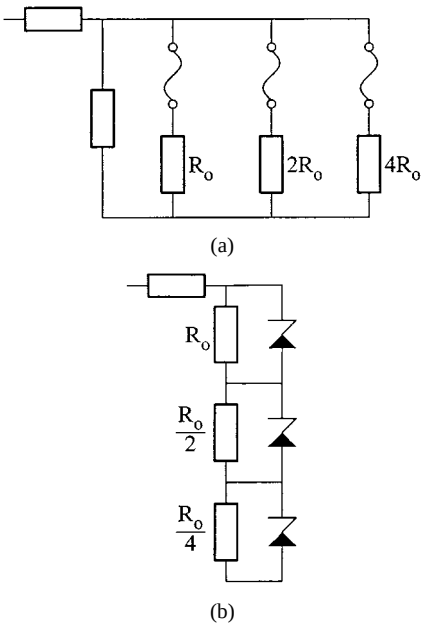


Fig. 6. Adjustment of resistors is achieved by (a) blowing-up interconnections, (b) short-circuiting zener diodes.

temperature sensors, one calibration point is already fixed by physical constants. As can be concluded from Eqs. (6) and (9), at 0-K, the extrapolated curves of $\Delta V_{BE}(T)$ and $V_{BE}(T)$ intersect the vertical axis at the values of 0 V, and V_{BE0}, respectively [Fig. 5(a)].

Adjusting the amplification factor A_1 or the bias-current density of the bipolar transistor performs trimming [5]. During this trimming, the curves for $A_1\Delta V_{BE}(T)$ and $V_{BE}(T)$ rotate around the 0 K values, being 0 V and V_{BE0}, respectively [Fig. 5(a)]. Once the trimming is performed in such a way that the output voltage has its nominal value, the output voltage automatically has its nominal value $V_{ref,\,nom}$ for the full-temperature range. This means that a single-temperature trimming is sufficient to obtain a full-temperature range calibration.

Special care has to be taken for devices with scaled output voltages. For instance, suppose that a reference voltage is realized according to the equation

$$V_{ref} = A_2(V_{BE} + A_1\Delta V_{BE}). \tag{10}$$

In this case, the spreading in the scaling factor A_2 directly effects the 0-K value of the output voltage [Fig. 5(b)]. This means that after a single-step, trimming a certain temperature-dependent deviation from the nominal characteristic will remain, as indicated by the dark-shaded area in Fig. 5(b). To avoid this, it is advised to use an amplification factor A_2 with a very high intrinsic accuracy and stability. This is possible when using dynamic-feedback amplifiers, as discussed in Section III.

For the device trimming, various techniques can be applied. In common use are

- fusible links [Fig. 6(a)], to blow-up connections;
- zener zapping [Fig. 6(b)], to short-circuit connections;
- laser-trimming, to adjust resistors.

The advantage of fusible links is that the applied voltages during trimming can be rather low (<5 V). For zener zapping, voltages up to 100 V are required. Special precautions have to be taken

to protect the circuit during trimming. On the other hand, the zener-zapped components are highly reliable and show a good long-term stability. With fusible links, special precautions have to be taken to avoid deterioration of the wafer test probes and metal regrowth due to on-chip electromigration.

D. Long-Term Stability of $V_{BE}(T)$ and ΔV_{BE}

The mismatching in the thermal coefficient of expansion (TCE) of different materials of the wafers and packages causes mechanical stress, which is temperature- and time-dependent. The stress-induced change in the $I_C(V_{BE})$ characteristic of bipolar transistors is the main cause of the long-term drift and hysteresis during thermal cycling or humidity changing of bandgap references [5], [14]. Although silicon has no mechanical hysteresis, many materials, such as epoxy or plastic, show features of viscoelasticity, which are responsible for mechanical hysteresis in the silicon die. The geometry and material properties of the molding material directly affect the stress characteristics. Normally, low-cost, plastic packages introduce high mechanical stress and hysteresis in the silicon die [15].

The stress-induced change in the $I_C(V_{BE})$ characteristic of bipolar transistors is called piezo-junction effect. The piezo-junction effect is anisotropic and its magnitude depends on: a) the amount and orientation of the stress, b) the current direction through the base, c) the minority carrier type in the base, and d) temperature. The silicon wafer axis is the reference for the stress orientation and current direction. Most of the industrial IC processes use the $\{100\}$ wafer crystal orientation as a standard. Therefore, we investigated the piezo-junction effect for transistors implemented in this wafer crystal orientation.

It has been found that the piezo-junction effect in the basic voltage $V_{BE}(T)$ causes approximately 80% of the total output error induced by stress of the commercial temperature sensor SMT160-30 [16], [17]. This temperature sensor is fabricated in a conventional BiCMOS process and the basic V_{BE} and V_{PTAT} signals are generated using NPN transistors. Another way to generate the V_{BE} and V_{PTAT} signals is to use the PNP substrate transistors, implemented in CMOS technology. The different type of minority carriers in the base causes different stress sensitivity for PNP substrate and NPN transistors.

To enable a systematic investigation, a test structure containing both types of transistors was designed and fabricated in bipolar technology, using a $\{100\}$-oriented wafer [16]. Due to the symmetrical crystal orientation of a $\{100\}$-oriented silicon wafer, the stress-induced change of the transistor characteristic is between two limits for any stress oriented in the wafer plane. The uniaxial stress orientations $\langle 100\rangle$ and $\langle 110\rangle$ determine these limits. The transistors have been tested for uniaxial stress in these orientations and the results are shown in Fig. 7.

For an arbitrary compressive (negative) or tensile (positive) stress oriented in the wafer plane, the change in V_{BE} is in the shaded areas. Based on this result, we can conclude that: a) the stress-induced change in V_{BE} of the pnp substrate transistors is smaller than that of the npn transistors, and b) both transistors have a lower stress-sensitivity for tensile stress than for compressive stress. Afterwards, the pnp test devices structures, using the substrate pnp transistors in CMOS technology, have also been fabricated and tested. It has been found that these transistors show the same stress dependency as those fabricated in bipolar technology.

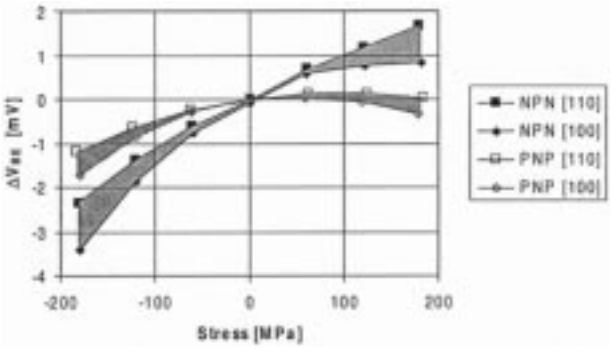


Fig. 7. Stress-induced change in V_{BE} for the npn and pnp substrate transistors for an arbitrary stress orientation.

It is concluded that the pnp substrate transistors fabricated in CMOS technology show a much better performance with respect to the mechanical stress than the npn transistors fabricated in bipolar or BiCMOS technology. As shown in Fig. 7, the amount of improvement depends on the amount of stress. Using low-cost plastic packagin, the stress will vary over the range of ± 150 MPa [14], depending on temperature and long-term variations. According to Fig. 7, the ΔV_{BE} variations over this range for pnp transistors are about a factor of two-and-a-half less than that for bipolar npn transistors. In case of a ceramic substrate, such as in a COB package, this difference is even much larger. This is due to the thermal expansion coefficient of the ceramic material, which is slightly higher than that of silicon. This causes a tensile stress on the die surface. As can be concluded from Fig. 7, the piezo-junction effect for pnp transistors for tensile stress is about a factor of seven less than that for bipolar npn transistors.

Regarding the long-term drift and instability of npn-transistor temperature sensors in [14], a value of about 0.1 K has been reported. As a result of our own experimental work, we found a similar drift for the smart temperature sensor SMT160-30 of Smartec [18]. Also, this smart temperature sensor is using bipolar npn transistors for the basic-signal generation.

Recently, Fruett and Meijer [19] found that the other basic signal in temperature sensors and bandgap references, the PTAT voltage ΔV_{BE}, is much less sensitive to stress than the base-emitter voltage V_{BE} itself. Fig. 8 shows the stress-induced error normalized in temperature scale for the V_{BE} and V_{PTAT} generated using pnp substrate transistors.

Summarizing these results, it is to be expected that the long-term drift of integrated temperature sensors and bandgap references, as due to package-induced stress, for CMOS devices using pnp substrate transistors, will be about two to seven times less than that of bipolar or BiCMOS devices using npn transistors.

III. Concepts of Dynamic Voltage References and Temperature Sensors

Once the basic signals have been generated with a high precision and stability, care has to be taken to maintain the per-

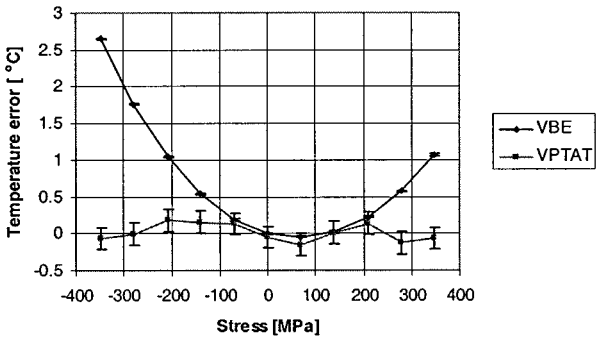


Fig. 8. Measured temperature error due to the stress-induced change in V_{BE} and $V_{\rm PTAT}$ for pnp substrate transistors.

formance during the further signal processing. In this section, we will show that the application of dynamic voltage processing, using dynamic element matching (DEM), and dynamic voltage division, will enable to get a very high performance. Using these techniques, even without trimming or adjustment, and even when using low-cost inaccurate components, a high precision of an amplifier-gain factor is obtained. Characteristic for the dynamic signal-processing techniques is that the circuit configuration is changed over various states within a measurement cycle. For each state, a sub-measurement is performed. The results of these sub-measurements are stored in a digital or analog memory. The sub-measurement results are processed in, for instance, a microcontroller, so that after a complete cycle, an averaged or another type of filtered signal is obtained. The application of these techniques will be discussed for the generation of the PTAT voltage and the amplification/division of the basic voltages.

A. A Dynamic $V_{\rm PTAT}$ Generator

In bandgap voltage references and temperature sensors, such as the SMT160-30 of Smartec [17], about half the output signal is derived from the small signal ΔV_{BE}. Because of the small value of this voltage, special care has to be taken to avoid the occurrence of errors due to mismatching, inaccuracy, and drift of the bias-current ratio. This goal can be achieved by applying a dynamic method, according to the principle shown in Fig. 9 [20]. The transistors M_1–M_4 represent four current mirrors. One of these transistors supplies current to the bipolar transistor Q_1, while the other three supply current to Q_2, so that the current (I_{c2}) passing through Q_2 is three times the current (I_{c1}) passing through Q_1. The difference between the base-emitter voltages V_{BE2} and V_{BE1} represents the PTAT voltage. This voltage is processed and converted to a digital signal, which is stored in, for instance, a microcontroller. Next, using the switches, the positions of M_1–M_4 are cyclically interchanged and the measurement procedure repeated.

After a complete cycle, the averaged measurement results represent a PTAT voltage in which the effect of any mismatch in the characteristic of the transistors M_1–M_4 is strongly reduced.

In order to eliminate the mismatch in the transistors Q_1 and Q_2, their positions are interchanged as well. So, for the configuration of Fig. 9, a complete cycle consists of eight sub-cycle states. The average value of $V_{\rm PTAT}$ over these eight switching states is almost equal to $(nkT/q)\ln 3$.

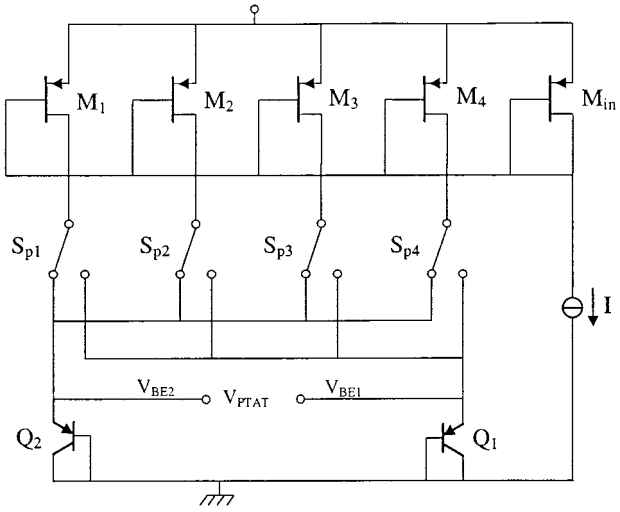


Fig. 9. Generation of $V_{\rm PTAT}$ using DEM, according to [20].

Example: Let us assume a mismatch in the current mirror so that I_{D1} of M_1 is ΔI larger than the current of the other MOS transistors i.e., $I_{D1} = I + \Delta I$. Further, we assume a mismatch ΔI_s in the saturation currents I_{s1} and I_{s2} of ΔI_s, i.e., $I_{s1} = I_{s2} + \Delta I_s$. In this case, the average value of $V_{\rm PTAT}$ over the eight measurement states is

$$V_{\rm PTAT} = \frac{n}{8}\frac{kT}{q}\left[6\ln\left(\frac{3I+\Delta I}{I}\right)+2\ln\left(\frac{3I}{I+\Delta I}\right) +4\ln\left(\frac{I_{s2}+\Delta I_s}{I_{s2}}\right)-4\ln\left(\frac{I_{s2}}{I_{s2}+\Delta I_s}\right)\right] = n\frac{kT}{q}\ln 3+\Delta V_{\rm PTAT}. \quad (11)$$

When, for instance, $\Delta I/I = \pm 0.01$ and $\Delta I_s/I_{s2} = \pm 0.01$, the relative inaccuracy $\Delta V_{\rm PTAT}/V_{\rm PTAT}$ is only $\pm 7.5 \times 10^{-6}$, whereas, without applying DEM, the maximum error can be as large as $\pm 18\,000 \times 10^{-6}$. Thus, the application of DEM reduces the worst-case error by a factor of more than 200.

An additional advantage of using the DEM technique to generate $V_{\rm PTAT}$ is that the low-frequency noise of the current mirrors can be reduced as well. This is an important contribution toward filtering out the flicker noise of the CMOS transistors. For this filtering, it is required that the corner frequency is less than the cycling frequency ($\cong$100 kHz) of the generated $V_{\rm PTAT}$ voltage. This can be achieved by choosing the appropriate dimensions for the CMOS transistors.

B. Dynamic Amplification and Division

In Section II-A, it has been shown that, in case of a scaled output voltage, it is important to have a very high accuracy of the scaling factor A_2, in order not to lose the precision of the calibration point at 0 K. Both amplification factors A_1 and A_2 should have a well-defined long-term stability in order to maintain the accuracy for a long time after calibration. Such a high accuracy and long-term stability can be realized with a dynamic-feedback (DEM) instrumentation amplifier [9], [21]. The principle of this amplifier is shown in Fig. 10. The resistive feedback circuit consists of a chain of K-matched resistors. The chain will be made

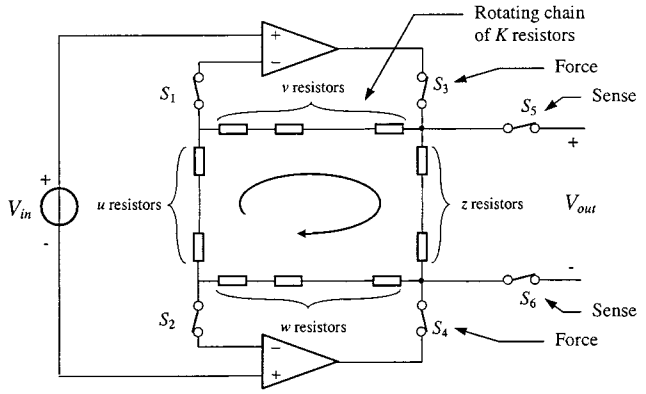


Fig. 10. Principle of a dynamic-feedback instrumentation amplifier, according to [20].

rotating by addressing of the appropriate switches. The feedback is realized by u, v, and w resistors, respectively. Since the resistors are connected as a chain, a resistive load will be present which consists of z resistors. Therefore, it holds that

$$K \equiv u + v + w + z. \tag{12}$$

By applying force and sense wires, the effect of the ON resistances of the switches S_1–S_6 is completely eliminated. The dynamic feedback is made by rotation of the resistor chain between the two op-amps. Therefore, the feedback has K states. So, a resistor that is part of the load will become part of the feedback later. For this reason, this load resistor is of vital importance for the functionality of the dynamic feedback. The average gain $\overline{G}$ of this amplifier over K successive states is equal to

$$\overline{G} = 1 + \frac{v+w}{u}. \tag{13}$$

Any mismatches between the resistors hardly affect the average gain because there is a compensating effect when the resistors move along the chain. The resistor chain is controlled by a digital-state machine, which addresses the appropriate switches. Every successive state, the chain rotates one position, with a frequency of about 50 kHz. The control of the resistor chain requires that there are 6 switches connected to a single point between every two resistors, which results in a total of $6 \times K$ switches.

The output voltages are converted into the time domain, where for instance, a microcontroller takes care for the digitization and algorithmic processing [11].

In [22] and [23], a DEM amplifier has been presented, implemented with switched-capacitors (SC) in the feedback loop. A special feature of this amplifier is that the input signals can be handled over the full rail-to-rail common-mode input voltage range.

The circuit of the DEM amplifier is shown in Fig. 11. For an amplifier with gain of G, $G+1$ identical capacitors are needed. The DEM technique is realized by rotating the positions of the capacitors sequentially in each clock cycle. In each clock cycle, one of the $G+1$ identical capacitors is in the feedback position of C_F, where all the others are in the position of C_I. The average value of the amplification factor in a complete cycle is equal to G, where the effect of capacitor mismatching is almost eliminated.

The average of the amplification factor can be expressed as

$$\overline{G} = \frac{1}{G+1} \sum_{i=1}^{G+1} \frac{\sum_{j=1}^{G+1} C_j - C_i}{C_i} = G + \Delta G \tag{14}$$

where ΔG represents the residual second order error of the mismatching. For example, $G = 7$, with 8 capacitors which show 1% mismatching, the relative error due to mismatching is only 29×10^{-6}. Without DEM, the relative error can be as large as $\pm 1\%$.

In order to apply auto-calibration, as described in Section IV, the voltage-to-time (or A/D) converter should have a very good linearity. In practical circuits, a high linearity can be realized only within a limited input-voltage range. To release the requirements, the low-level signals (ΔV_{BE} and ΔV_{os}) can be amplified and/or the high-level signal (V_{BE}) can be divided. The absolute accuracy of a passive voltage divider depends on the components matching. Therefore, aging effects will cause drift of the divider factor. To solve this problem, in [24], a dynamic voltage divider is proposed (Fig. 12). This divider has the advantage of being simple and insensitive to the ON resistance of the MOS switches. The circuit consists of a resistive voltage divider combined with a capacitive voltage divider. The divider is realized with N_R resistors and N_C capacitors, resulting in an accurate division ratio of $\alpha_d = N_C N_R$.

Implementation of the DEM techniques requires signal and data-processing circuits, such as switch controllers, memory, and calculation circuits. These features can conveniently be obtained by using a microcontroller. Once a microcontroller is used, besides switch control, it is also easy to perform data processing, in the frame of an overall system design. The data processing steps can include, for instance, averaging, nonlinearity compensation, auto-calibration, self-testing, and filtering. For a part, this is shown in the next section, which discusses a thermocouple-voltage processor. A bandgap reference is used as a voltage reference for the measurand, while an integrated temperature sensor is used to measure the reference-junction temperature. It appears that the overall system can easily be designed to include the auto-calibration technique. This technique is very powerful to solve to major problems of CMOS amplifiers: offset and $1/f$ noise.

IV. Auto-Calibration and Further Signal Processing

The accuracy of conventional CMOS temperature sensors and bandgap references has been limited by the offset voltage and $1/f$ noise of the amplifiers, needed to amplify the small PTAT voltage. Applying auto-zeroing [4], chopping technique [10], and auto-calibration [8] can solve these problems. To apply these powerful techniques, it is very suited to use a microcontroller or another type of computer. In this case, it is possible to store the information of the various signals in a memory, to perform algorithmic processing, and to control switches. Moreover, with such a computerized system, it is easy to perform nonlinearity correction. Finally, with such a system,

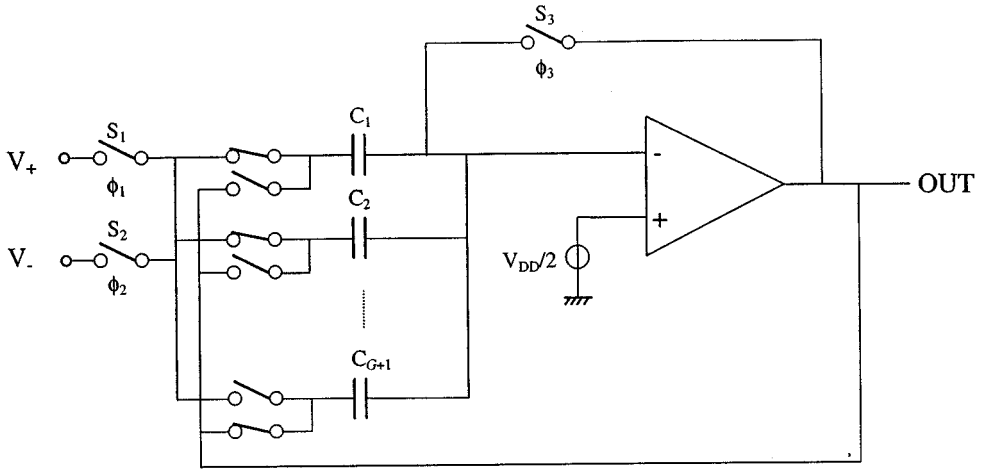


Fig. 11. DEM switched capacitor amplifier, according to [22].

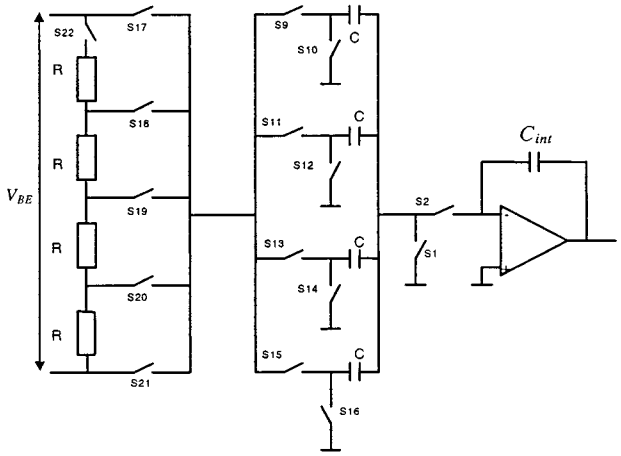


Fig. 12. Dynamic voltage divider according to [24].

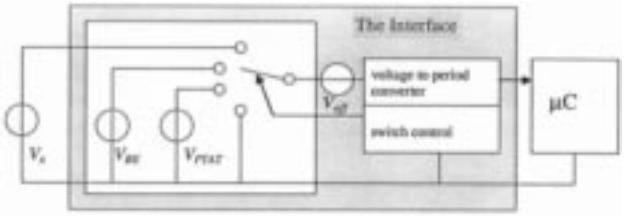


Fig. 13. Basic setup for a dynamic voltage measurement system.

it is simple to perform dynamic signal processing according to the principles described in the previous section.

As an example, Fig. 13 shows a basic setup for a thermocouple-voltage processor [11]. The two measurands are the thermocouple voltage V_X and the reference-junction temperature T_J. The required voltage reference is implemented as a dynamic bandgap reference, according to the principles discussed in this paper. The basic circuits and signals used for the bandgap reference are also applied to measure the absolute temperature of the integrated circuit. When a good thermal coupling between this integrated circuit and the thermocouple reference-junction is made, the chip temperature is equal to the reference-junction temperature T_J. All together, in this system, four basic signals, V_X, V_{BE}, ΔV_{BE}, and the offset voltage V_{OS}, are measured. The voltages V_{BE} and ΔV_{BE} are used for both the voltage reference and the integrated temperature sensor, while the offset voltage V_{OS} is measured to allow offset compensation by applying auto-calibration. All algorithmic signal processing, including adding, subtracting, division, and nonlinearity correction, is performed in the microcontroller. Also, data storage and data processing is performed in the microcontroller. To enable this, the voltages are firstly converted to the time domain by a linear voltage-to-period converter. When the output periods during the successive measurements are t_X, t_{BE}, $t_{\rm PTAT}$ and t_{OS}, respectively, then the final result F_V for the voltage measurement amounts to

$$F_V = \frac{t_x - t_{0S}}{t_{BE} + At_{\rm PTAT} - (A+1)t_{0S}} = \frac{V_x}{V_{ref}}. \qquad (15)$$

The final result F_V is independent of the multiplicative and additive errors and parameters of the converter. In a similar way, the chip temperature can be calculated from the three periods t_{BE}, $t_{\rm PTAT}$, and t_{OS}, respectively [8].

The applied technique is called auto-calibration because the system calibrates itself, with respect to the converter properties, in every measurement cycle. When the measurement is repeated with a certain frequency f_m, low-frequency noise and interference can be high-pass filtered, where f_m is the cut-off frequency. Also for this purpose, the microcontroller is used, to perform digital filtering.

The schematic diagram of the CMOS interface circuit is shown in Fig. 14. The dynamic VPTAT generator is implemented according to the principle shown in Fig. 9. For the dynamic voltage divider, a circuit similar to that shown in Fig. 12 has been used.

The first offset capacitor $C_{\rm off1}$ is used to realize an sampling time interval for the sample-and-hold function of C_4. During this sampling time, the signal voltages are converted into a charge over the capacitor C_4. In the next sub-phase of a measurement cycle, this charge is transferred to the integrator capacitor $C_{\rm int}$. Together with the comparator and controlled

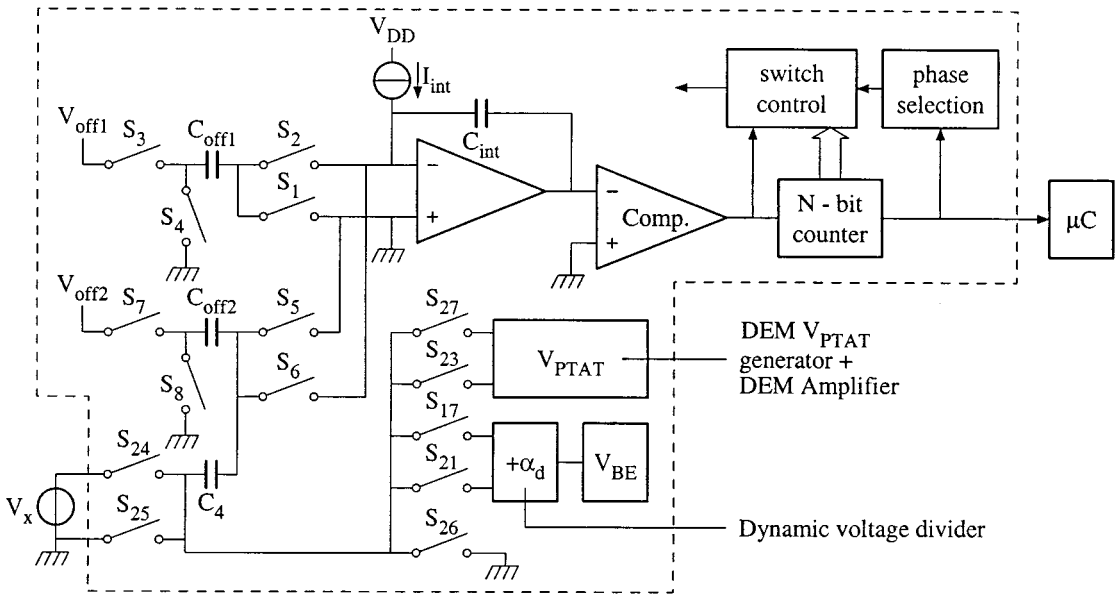


Fig. 14. Schematic diagram of an interface with a dynamic voltage-reference circuit.

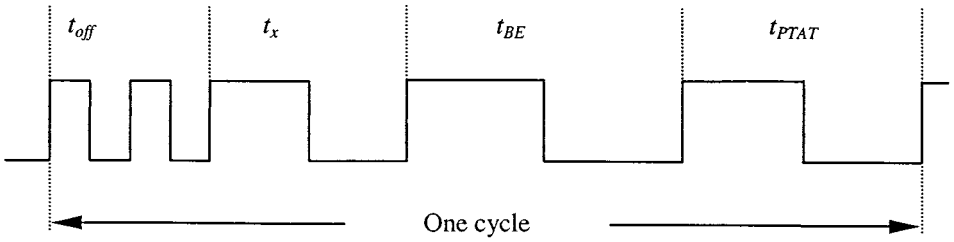


Fig. 15. Interface output signal.

switches, a charge-controlled relaxation oscillator is formed which linearly converts the voltages into periods of the oscillator output signal. The second offset capacitor C_{off2} is needed to enable negative values of the thermocouple voltages. More details concerning the applied signal processing techniques in this circuit are presented in [11] and [25], [26].

A block of M modulation periods (Mt_{mod}) corresponds to one measurement phase. One complete cycle of the output signal contains four measurement phases, as shown in Fig. 15. The four time intervals, t_{BE}, t_{PTAT}, t_{off}, and t_x, are proportional to the attenuated base-emitter voltage (V_{BE}/α_d), the PTAT voltage (ΔV_{BE}), the offset voltage (V_{off}) and the unknown voltage (V_x), respectively. The micro-controller measures the duration of each phase and calculates the ratio F using Eq. (13) and a similar equation for the calculation of the chip temperature.

The chip has been tested and shows a standard deviation of 8 μV for the voltage measurement and 50 mK for the temperature measurement, for a measurement time of 50 ms. For the voltage measurement, a relative (scale) error of -550×10^{-6} is reported. For this interface circuit, long-term stability tests have not yet been performed.

V. Discussion and Conclusion

The paper shows how accurate temperature sensors and bandgap references can be realized, using low-cost CMOS technology. It is shown that the temperature behavior of bipolar pnp substrate transistors can be well characterized with conventional models. To obtain a good accuracy of the temperature sensors and bandgap references, implemented with these transistors, a proper biasing-current level should be selected.

An accurate PTAT voltage can be generated by applying dynamic element matching of the applied transistors. The small PTAT voltage can be amplified using a CMOS operational amplifier. A very high intrinsic accuracy of the gain factor of the amplifier factor is achieved by applying dynamic element matching of the feedback components. A similar technique can be applied to realize an accurate divider, which can be used to further reduce the dynamic range of the set of basic signals (V_{BE} and V_{PTAT}) by dividing V_{BE}.

It is shown that the effect of mechanical stress in bipolar substrate transistors implemented in CMOS technology is much lower than that of the bipolar components fabricated in a bipolar process. Especially when a ceramic or an epoxy-package is used, this will result in a much better accuracy and long-term stability.

When the temperature sensors and bandgap references make part of a data-acquisition system in which a microcontroller is applied, the dynamic techniques can easily be implemented. The microcontroller can perform the control functions and the algorithmic data processing. To take full advantage of the powerful features of microcontrollers, the basic signals $V_{BE}(T)$

and $\Delta V_{BE}(T)$ are converted to time-modulated signals so that they can be read out by the microcontroller. As compared to the conventional temperature sensors and bandgap references, this will result in a novel architecture: signal-processing steps, such as adding and subtracting of the basic signals $V_{BE}(T)$ and $\Delta V_{BE}(T)$, amplification of $\Delta V_{BE}(T)$, and linearization of $V_{BE}(T)$, which were usually implemented in the device hardware, can now be replaced by more easy and more accurate data-processing steps performed in the microcontroller. However, to compensate for the spreading in the base-emitter voltage, calibration and trimming is still needed.

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