# CAPACITIVE MICROELECTRODE ARRAYS FOR IN-VITRO ANALYSIS OF NEURAL ACTIVITY

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# Capacitive Microelectrode Arrays for in-vitro Analysis of Neural Activity

THESIS FOR THE DEGREE OF MASTER OF SCIENCE

in

Electrical Engineering

Microelectronics

by

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Technische Universiteit Delft

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Submitted: 22/08/2019

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**Abstract:**

Microelectrode arrays (MEAs) are extensively used for measuring neural activity in-vitro given their ability to monitor several neurons simultaneously unlike techniques such as patch clamp. However, MEAs still have limitations in acquiring high spatial resolution data due to limited number of channels that can be parallelly scanned, the need for bulky anti-aliasing filters, and limitations in signal-to-noise ratio (SNR) arising from thermal noise. Commercially available MEAs rely on resistive or self-capacitive sensing scheme, but this research proposes a new approach to increase the number of sensing locations while reducing the channels and to increase SNR. Fundamental design aspects of a MEA such as the shape and size of electrodes are revisited and a parametric sweep of parameters relating to the capacitance and the coverage of the cell over the capacitor are performed to enhance the sensitivity. By employing traditional lithographic fabrication techniques, these arrays with various geometries were fabricated and characterized to compare their SNR. Neural cultures are seeded on these MEAs to record neural activity in the electrical domain and concurrently Calcium (Ca+2) Imaging is performed to correlate and verify the activity, giving us insights into why a capacitance change occurs on the firing of a neuron.

**Keywords:**

Microelectrode Array, Neural Interface, In-vitro analysis, Calcium (Ca+2) Imaging, Impedance Characterization

# ACKNOWLEDGMENTS

This Master thesis presents months of work on my master final project in Electrical Engineering, direction Microelectronics at Delft University of Technology. The project was carried out at laboratory of biosensors and bioelectronics (LBB) of ETH Zurich as an exchange student for master's thesis from TU Delft.

I would like to thank my advisor Prof. Janos Voros very much for creating this opportunity and welcoming me to work at your laboratory. I would also like to thank Prof. Wouter Serdijn and Dr. Virgilio Valente for encouraging me to take this project and for continuously supporting me during this period. I would specially thank Mr. Sean Weaver and Ms. Aline Renz for supervising my work on a daily basis and for providing valuable insights towards my project. I feel very lucky for being a part of this work, for not only have I learned much during this period, I have also met amazing people at both LBB, ETH Zurich, as well as at bioelectronics section of TU Delft.

Furthermore, I would like to sincerely thank various technicians and mentors Mr. Aldo-Ricardo Rossi and Mrs. Ela Burmeister for patiently helping me out with resources and processes for my work.

Yashwanth Sai Reddy Vyza
Delft, The Netherlands
August 22, 2019

# Contents

# List of Figures

# Chapter 1

# Introduction

The human brain and nervous system are one of the complex systems posing many scientific questions. Understanding how brain works, the characteristics of neurons, and their communication shall open new areas of research and medicine. Recent advances in technologies have led to the rapid development of systems to tap into these systems and answer the scientific questions. By getting answers to these scientific questions, it would be easier to tackle various neurodegenerative diseases or other neural disorders.

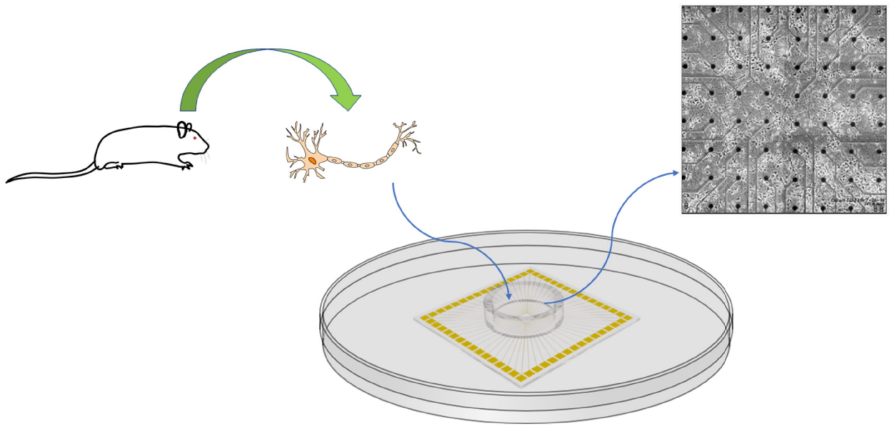


Figure 1.1: Visualization of an in-vitro experiment using MEA

As a part of these technologies, neural interfaces play a vital role to advance our understanding of the nervous system, owing to their comprehension of physiological processes at the cellular level. Being electrogenic (capable of producing electrical impulses), neurons can be accessed in the electrical domain, something that is very well understood. Limiting our view only to sensor-based neural interfaces, they can be broadly classified based on the mode of the interface in an experiment. They can be directly placed inside the brain known as the in-vivo interface. Or by taking out a few neurons or brain slices and analyzing them outside the body known as in-vitro analysis. This project emphasizes on developing these in-vitro sensors that can be associated with the electrical behavior of neurons. Microelectrode Arrays (MEAs) are the most widely used sensors for such applications. These sensors contain an array of electrodes, microns in size that are made to come in contact with neurons. This contact will directly pick up the local electrical changes generated by the electrophysiological processes of neurons. Examination of these changes helps us understand the phenomena occurring at the cellular

level. A visualization of the in-vitro experiment for this thesis can be seen in figure 1.1.

Microelectrodes have been used from over a century to understand the electrophysiological activity of the nervous system. An extracellular metal electrode was first used to record from a single neuron (Renshaw, 1946; Lorente,1928). In in-vitro studies, a platinum electrode, of diameter 175 um was used to record from rat diaphragm motor neurons using a micromanipulator (Tasaki et al., 1968). Soon after multiple electrode arrays were developed to increase the spatial distribution, the first being a simple assembly of multiple electrodes (Verzeano, 1956). Hanna and Johnson (1968) assembled an array of 20-30 electrodes on a plastic sheet, but these were not microelectrodes and had variable sizes mostly in the range of millimeters. In recent times, various aspects of MEAs such as the electrode impedance, surface properties, geometry, etc. are being explored to provide a better pathway for higher charge transfer, high-spatial resolution, and easy processing. Lots of work on such aspects is being produced every day to make these sensors more robust.

Techniques from nanotechnology are being used to produce high-quality electrodes. The sensitivity of such sensors majorly relies on the impedance of these electrodes. Thus to decrease the interface impedance alternatives are being sought after such as electroplating platinum black [2] or three-dimensional electrode structure,[3, 4] or TiN sputtering.[5] Recently even more advanced materials such as nanostructures or carbon nanotubes (CNTs) have also been used.[6] These materials provide a higher surface area to have a better signal acquisition. Gold flake nanostructures were produced to increase the effective area by Kim et al.[7] Similarly Park et al. reported using electroplated 3D nanoporous Pt-microelectrodes.[8] CNT based mesh-like electrode surfaces were fabricated by Gabay et al. [9] But not just limited to the surface and material modifications, but advances have been made on the lines of electrode geometry itself where innovative 3D structures or biomimetic MEAs that can grasp the membrane have been produced to have better cell contact.[10] A. Heirlmann et al. work on extensively high-density MEAs ($\geq$ 1000 electrodes) based on CMOS technology emphasizing to improve the spatial resolution of MEAs.[11] Numerous companies have been established to commercialize these MEAs and also contribute to the research on these sensors (Eg. Multichannel Systems, Ayanda Biosystems, etc.)

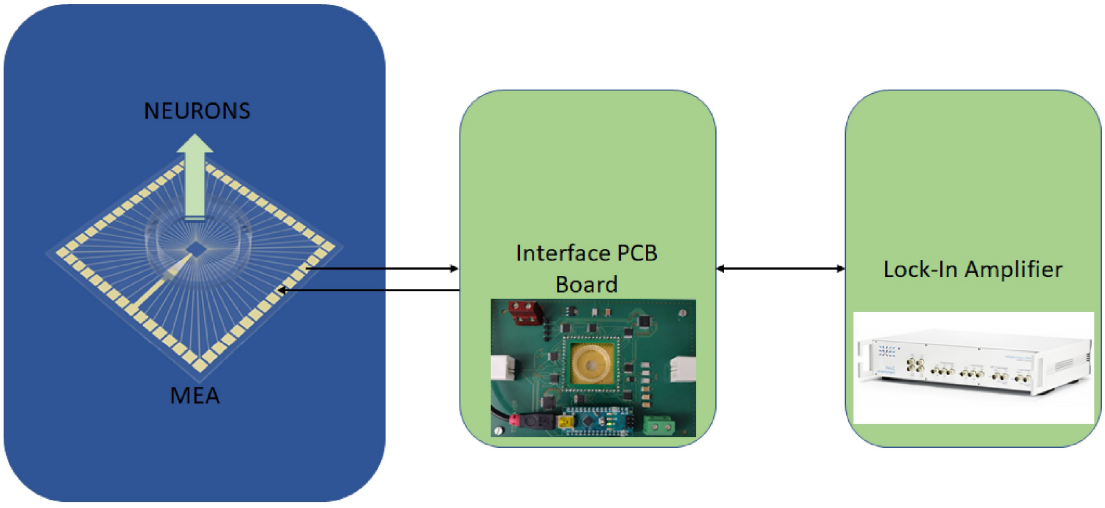



Figure 1.2: Block-diagram for capacitive sensing based MEAs

Despite many such advances, MEA based technology is still being optimized to achieve better resolution, high signal content with respect to noise, and to be compatible to process the acquired data. This thesis deals with improving the signal quality by introducing a new sensing paradigm working at higher frequency ranges. Unlike most MEAs available, which rely on resistive sensing, this sensing scheme allows the signal to be pushed into a capacitive regime. To be more specific, by stimulating through one co-planar electrode and recording from another with the cell body sitting in between the electrodes acting as dielectric. By doing this, we attempt to record action potentials in the form of capacitance changes. Working in capacitive domain helps one to notice even the smallest of the changes and also is less susceptible to thermal noise. This work shall potentially shed light on how the cell itself acts as a dielectric and how its properties change.
In this report, we first introduce the background theory to the principles of the electrode-electrolyte interface and the phenomena involved, then followed by the theory of aqueous dielectrics to understand the microscopic phenomena occurring and the principle of lock-in detection used to detect these small changes. Next, in the methods, design, fabrication of these MEAs, and the interface system has been elaborated. Finally, the results with cells and without cells have been discussed. This thesis ends with the conclusions drawn and suggestions for future work explained. The entire work can be summarized by the block diagram 1.2. All aspects of this project, from grasping the theory behind such phenomena to designing these MEAs based on theoretical calculations and then to fabricate, interface these MEAs was performed. These capacitive MEAs once fabricated were characterized and prepared neurons were seeded to see changes in neuronal activity.

# Chapter 2

# Background

Biological systems being very complex in nature with a myriad of interdependent components can be very difficult to analyze at once. In-vitro studies break down this sophisticated setting allowing one to concentrate on a few elements of interest.[12] This makes such studies popular with units such as cells, bio-molecules, and micro-organisms. For example, in this project, we aim to measure activity from neurons seeded in an in-vitro platform to understand their characteristics. These studies are convenient and more straightforward, allowing species-specific analysis than can be done with a whole biological organism. In-vitro sensors and methods can be automated, miniaturized thereby allowing screening with high-throughput.[13] A class of sensors called the microelectrode arrays are widely used for in-vitro studies.

Active cells such as neurons, cardiac and muscle cells when excited generate ionic currents through the membranes causing voltage changes in the intracellular and extracellular domain. To understand the electrophysiology of these cell types, one can use minuscule electrodes to pick up these changes. By making electrodes the size comparable to that of cells i.e., micrometer range, one can effectively transduce this change in voltage arising from ionic currents in the cellular medium into electronic current on the electrode. An aggregation of microelectrodes into an array to sense these changes from the cells is called an MEA. An MEA can be used for analyses from slices of tissue or dissociated cell cultures.[14, 15] Compared to traditional methods such as patch-clamp, MEAs have more advantages such as: allowing access to multiple electrodes at once, ability to concurrently record data from various electrodes, ability to select multiple sites within the array, being non-invasive and finally higher spatial resolution.[1] MEAs can be helpful in studying pharmacological effects on dissociated cultures. Combining this with microscopy enables understanding of network growth in neurons. [16] Electrical activity from extracellular networks of cardiac cells and neurons in organs such as the heart or brain can shed light on physiological information which in turn can be used to identify pathological degenerations like Alzheimer's or Parkinson's and many more.

However, acquiring high spatial resolution data of neural cultures from (MEAs) is challenging due to the limited number of channels which can be simultaneously scanned. The need for bulky anti-aliasing filters, and thermal noise are also serious problems MEAs face. Current MEAs typically rely on a self capacitive or resistive sensing scheme, where changes in the local ion concentration around the electrode cause a change in voltage on the electrode. This work introduces a new approach, aiming to increase the number of sensing locations while reducing the total number of channels needed. Additionally, to improve the sensitivity, which is especially crucial for single-cell sensing.

## 2.1 Electrode-Electrolyte interface

### 2.1.1 Electrical Double Layer

Immersing materials into polar solvents give rise to charges by physical adsorption of ions or dissociation of chemical groups to the surface. [17] In case of metals or semiconductors applying an electrical potential can give rise to excess charge at the surface. This developed surface charge will be subsequently balanced out by oppositely charged ions of equal magnitude. To balance out the charge, these counter ions accumulate at the surface, thereby creating a charged region in space commonly known as Electrical Double Layer (EDL). EDL created controls various processes like biological membrane phenomena [18], colloidal dispersion [19], electrokinetics [20]. This makes EDL a must understand phenomena to analyze biological systems at the cellular level and also for electrochemistry, colloids, etc.

The earliest theory on EDL and its structure were put forward in 1853 by Henry Helmholtz [21]. This theory described the interface between two dissimilar metals to be composed of charged layers. Further, in 1879, Helmholtz extended his theory to metal-solution interface assuming that the excess charge resides only on the surface and no potential is applied to the metal. [22]. The approach also stated that the counter ions are accumulated only near the surface, assuming excess charge resides over the surface. It was noted that these counterions in solution also reside directly at the surface separated only by a distance of molecular order. This EDL formed at the surface can be compared to a parallel plate capacitor, and this should have a constant capacitance value since it is dependent only on the charge separation distance and the dielectric constant. In reality, measurements show that this constant capacitance is not constant but rather changes with changes in ionic concentration and applied voltage. This deviation from what is expected in theory is a significant drawback for this model.

Counter ions in electrolytic solutions are drawn towards the excess charge on the surface, but this attraction is counteracted by Diffusion because of the concentration gradient developed, leading to a thicker double layer than Helmholtz presented. In the early 1900s, Gouy and Chapman extended the model for solution phase to account for diffusion. [23, 24] They said that given the excess charge still resides on the surface, for equilibrium, the ions diffusing due to the applied potential are distributed in accordance with the Boltzmann distribution. In the diffuse model of the double layer charge distribution of ions changes as a function of distance from the metal-based on Maxwell–Boltzmann statistics which describes a probability distribution of the ions. That is the potential decreases exponentially away from the interface. This model positively took into account the fact that the counter-ions closest to the surface will repel further counter ions moving towards the electrode, causing the exponential decrease. This was then integrated with Poisson's equation relating the charge density with the potential, thereby giving rise to the nonlinear Poisson-Boltzmann equation, as shown in equation 2.1. [17, 25, 26]

$$\nabla^2\phi = -\frac{e}{\epsilon}\sum_i c_{io} e z_i \exp(-\frac{z_i e\phi}{k_B T}) \tag{2.1}$$

Here e is the elementary charge, $\epsilon$ the dielectric constant, $C_{io}$ is the ion concentration, $\phi$ is the potential, T is the temperature and $k_B$, the Boltzmann constant. The net counter ion charge density is highest at the surface and decreases with distance away from the interface. At this distance, it can be treated as a bulk solution allowing us to assume there is an equal number of positive and negative ions. The non-linearity of Poisson-Boltzmann equation can be removed by considering for small potentials as put forward by the Debye-Hückel approximation ($\phi \leq k_B \mathrm{T/e} \approx 26mV$) giving,

$$\nabla^2\phi = \kappa^2\phi \tag{2.2}$$

where $\lambda_D = \kappa^{-1}$ is commonly known as the Debye screening length,

$$\kappa^{-1} = \lambda_D = (\frac{\epsilon k_B T}{2 c_o e^2})^{1/2} \tag{2.3}$$

Generally this Debye screening length is in the range of atomic order for very high ionic concentrations and can increase up to 1 micron for pure water ($c_o \approx 0.1$ $\mu$M) with practically no ions present. Debye screening lengths for various aqueous solutions have been summarized in Table 2.1. By this theory, the capacitance of this EDL within the diffusion layer is no longer considered to be constant.

| $c_o$ | $\lambda_D$ |
|---|---|
| 1M | 0.3 nm |
| 100 mM | 1 nm |
| 1 mM | 10 nm |
| 100 $\mu M$ | 30 nm |
| 1 $\mu M$ | 300 nm |
| 0.1 $\mu M$ | 1 $\mu m$ |

Table 2.1: Debye screening length of various aqueous electrolyte solutions of decreasing ionic concentrations

Even though the Gouy-Chapman model overcomes certain drawbacks of the Helmholtz model of EDL, it still considers the ions to be point charges and neglects the finite ion size. Due to this reason, the Gouy-Chapman model fails for high voltages ($\leq$ 80 mV) and high bulk ion concentrations ($\leq$ 10e3M).[27, 28] This is because the model converges to high electric fields and ion concentrations that are unrealistic. Amongst all this, it was Stern in 1924, who first proposed a model considering the finite sizes of ions forming into a compact layer at the EDL interface.[29] This layer is assumed to be approximately the radius of hydrated ions and is known as the Stern layer. As an extension to the Gouy-Chapman model, this model came to be known as the Gouy-Chapman-Stern model or the modified Gouy-Chapman model.

The interface was further modified and explained more clearly by Grahame, who divided the Stern layer into two subregions[28, 30]. Using the concept of ions that lose solvation shell to get in direct contact with the interface (specifically adsorbed ions), he used them as a basis to divide the Stern layer. He divided the Stern layer by considering two planes, one cutting through the center of these specifically adsorbed ions and the next through the center of solvated ions at the closest approach to EDL interface. The prior plane is known as the Inner Helmholtz Plane (IHP) and the latter Outer Helmholtz Plane (OHP). The Gouy-Chapman-Stern model with the Grahame modification was illustrated as in figure 2.1 with a positive charge over the electrode. There is a linear potential drop over the charge-free regions between the OHP and IHP and in between IHP and electrode as well, both of which can be assumed to be a series combination of two parallel plate capacitors. Starting at the OHP the potential drops across the diffuse layer until it reaches the value that of the bulk solution. Considering aqueous solutions, water molecules specifically align based on their dipoles on the surface in IHP region.[31] Thus the dielectric permittivity inside IHP and OHP differ from that of the bulk value. In IHP region it can be of the order of $\epsilon = 6$ to $\epsilon = 30$ in the OHP region.[28] Due to breaking down of Stern layer, it can be seen as a small separation between counterions and electrode double layer which can give rise to quite high capacitances values, usually around 10 to 40 $\mu$F/cm2.

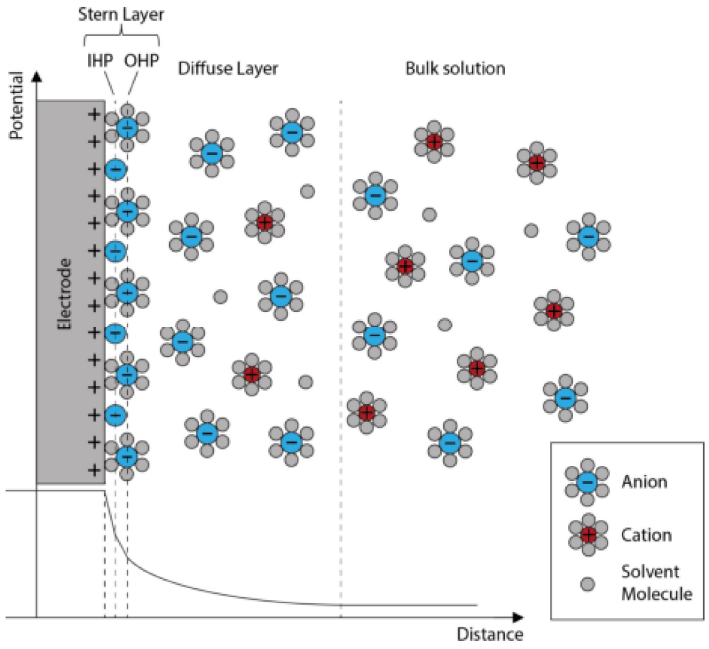



Figure 2.1: Gouy-Chapman-Stern model

The Gouy-Chapman-Stern model even though it addresses many of the drawbacks of previous models and replicates a more realistic scenario.[17, 32] There are a few more improvements that can be done to adjust any mismatch between experiments and theoretical bases such as variations of the dielectric permittivity near the EDL interface, the polarizability or ion-ion interactions at the interface.[32] The exact process occurring at EDL is still not clearly understood in-depth and poses as an essential topic of research.

### 2.1.2 The Poisson-Nernst-Planck (PNP) Model

The Poisson–Nernst–Planck (PNP) model describes the ion interactions and transport along with a continuum description of electrostatic potential and concentration based on a mean-field approximation. Not just a qualitative basis but this model is also capable of quantitative predictions for various ion transport problems in areas such as biological systems, fluidic systems, and semiconductor devices. Even though the PNP model is capable of giving a good prediction of the ionic and transport phenomena, it can be a tedious task to solve the equations. Each ion species will have one diffusion coefficient profile concerning the position and also one Nernst-Planck equation. This would then be extended to all the ion species in the system.

But the PNP system already simplifies studying these ionic interactions by neglecting interactions between ions thereby averaging them. It considers individual ions to be point charges with a certain electrical charge and mobility. The distribution of ionic densities and their transport depends on these parameters, which are explained by the Nernst-Planck (NP) equation. [17, 33] According to the equation the flux of each individual ion species $i$ will by,

$$\frac{\partial c_i}{\partial t} = \nabla.(D_i \nabla c_i + \mu_i z_i e c_i \nabla \phi) \tag{2.4}$$

$D_i = \mu_i k_B \mathrm{T}$, Einstein's relations establishes the diffusion coefficient $D_i$ expressed in terms of mobility $\mu_i$. The above equation can then be understood as a straight forward drift-diffusion equation neglecting more complex interactions such as convective transport. To describe the other parameter of ionic

charge, the charge density of this ionic species and its relation with the electrostatic potential is represented using the Poisson's equation,

$$-\nabla.(\epsilon\nabla\phi) = \sum_i z_i e c_i \tag{2.5}$$

Equations (3.1) and (3.2) put together represent the complete PNP model. Examining the equations, due to their non-linearity and coupled partial derivatives it would be a challenging task to solve them. Only knowing the primary parameters, the potential $\phi$ and ionic concentrations of each species $c_i$ would reduce the complexity. In a purely qualitative sense, this also illustrates the basic features of an electrical double layer (EDL). That is when a potential is applied at an electrode surface, ions with the same charge will be repelled, while oppositely charged ions drift towards the electrode. Following the equations of the PNP model, this ionic motion is facilitated by the local potential gradient and while in drift motion, it is hindered by diffusion. At equilibrium, this creates a space charge distribution region representing the EDL. The time needed to reach the equilibrium is related to the charging time of EDL.

Capable of quantifying the EDL, this model also satisfies the Gouy-Chapman model as discussed in the above segment and also suffers from the same drawbacks. Given the small sizes of these ions, very small potentials can also generate high electric fields at the electrodes which imply ion concentrations out of range. Not considering the finite size of an ion into the model and neglecting of ion-ion interaction effects are two major drawbacks to this model. [34] Various extensions to the PNP model like Poisson-Nernst-Boltzmann-Planck model take into consideration these interactions and finite-size, thereby giving more accurate results closer to the real scenario. [35]

## 2.2 Dielectric properties and behavior of aqueous solutions

The tendency of a charge distribution like an electron cloud of an atom or a molecule to be distorted by an external electric field is known as polarizability. In more simpler terms, it is the ability to form instantaneous dipoles. Dipoles are simply a pair of electrical charges of opposite signs and equal magnitude separated by a distance. The dipole moment is the measure of this separation of dipoles, that is, a measure of the system's overall polarity. Now, dipole moment can be of two types, either permanent or induced. The permanent dipole moment is something that generally exists in polar molecules due to their inherent structure and the charge distribution around them. On the other hand, a dipole moment that arises due to the orientation of particles or atoms by an external field is known as the induced moment. All atoms and molecules possess dipole polarizability $\alpha$, which is the dipole moment induced by a unit electric field.

Some molecules due to the asymmetric arrangement of bonds containing opposing charges give rise to a net dipole moment and such molecules are known as polar molecules. Water with a slight positive charge on one side and a small negative charge on the other is an example for a polar molecule. Molecular structure of water contains two polar O−H bonds in a bent (nonlinear) geometry. Oxygen with high electronegativity creates a dipole with the negative end, and the positive pole arises midway between both hydrogen atoms. The dipole moments here do not cancel out, resulting in a net dipole moment. This can be visualized by the depiction in figure 2.2.

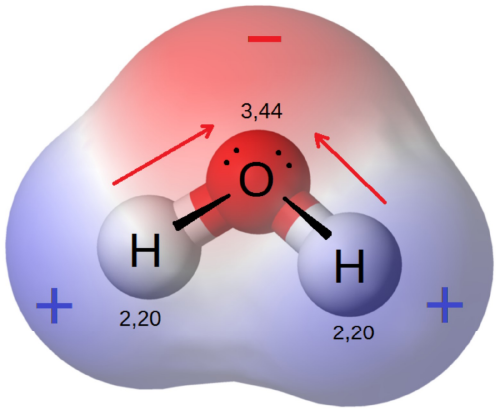



Figure 2.2: Illustration of structure of water molecule

Water being a polar molecule can easily dissolve other polar molecules. An electrolyte is a substance that breaks down into cations and anions when dissolved in a polar solvent like water. When an electrical field is applied to an electrolytic solution, the cations move towards the more negative end of the field and the anions towards the positive field. This movement of cations and anions in a solution amounts to the induced dipole moment. Thus changing the concentration of the electrolyte will change the densities of these cations and anions, which in turn changes the dipole moment induced. Neurons are cells with gated-ion channels and continuously exchange various ions like Sodium (Na+2), Potassium (K+1) or Calcium ions (Ca+2), etc.[36] These ions released when a neuron fires add to the existing cations and anions in the electrolytic solution thereby causing a change in the dipole moment which is reflected in the dielectric constant. In simpler terms, the neurons here act as the dielectric medium, and one can measure the changes in this electrically.

Dielectric constant or permittivity is the measure up to which the electric charge distribution within the material can be polarized. The polarization (P) of a substance is the density of electric dipole moments (M) for a given volume V, as shown in the equation below.

$$\mu = PAd = PV \tag{2.6}$$

The charge density of the dipoles would be the sum of the polarization and the effect of the applied field.

$$Q = P + \epsilon_0 E \tag{2.7}$$

Where P is the polarization, $\epsilon_0$ the permittivity in free space and E the electric field. But as

$$Q = \epsilon E \tag{2.8}$$

$$\epsilon = \epsilon_r \epsilon_0$$

$$P = (\epsilon_r - 1)\epsilon_0 E$$

Where $\epsilon_r$ is the dielectric constant of the material. It is necessary to understand that macroscopic and microscopic polarization effects are entirely different. The calculation of microscopic polarization or the molecular dipole moment is not just dividing the macroscopic polarization by molecular volume. This is because the actual field felt by the molecule is not the same as the macroscopic field applied externally.

It was Debye who first calculated the polarization of a system of rigid polar molecules randomly oriented in the absence of electric field.[37] Debye proposed that the moments are distributed about an applied field in accordance with Boltzmann's law. This relation would be

$$(\epsilon_r - 1)/(\epsilon_r + 2) = \frac{P_m}{V} \tag{2.9}$$

$P_m$ is the polarization molar polarization and can be defined as

$$P_m = \frac{N_A}{3\epsilon_0}(\alpha + \frac{\mu^2}{3K_BT}) \tag{2.10}$$

Where $\alpha$ is the polarizability of the molecules induced by the external field, $N_A$ is the Avogadro number, $K_B$ is the Boltzmann constant, T is the absolute temperature and $\mu$ the permanent dipole moment. However, Debye's equation had certain limitations as it did not take into account the Lorentz inner field. This was improved by considering all detailed forces by Kirkwood yielding the Kirkwood-Frohlich equation as follows:

$$\frac{(\epsilon - n^2)(2\epsilon + n^2)}{\epsilon(n^2 + 2)^2} = \frac{4\pi N_0 g \mu_g^2}{9KTV} \tag{2.11}$$

These equations work for all cases but fail when an alternating field is applied as new effects arise. An alternating electric field applied over a dielectric of certain frequency gives rise to dielectric dispersion. That is the motion of orientation of dipoles results in frequency variation of the dielectric constant, and subsequently a dielectric loss over a broader range of frequencies. The phenomena here are that when the direction of the field is changing considerably fast, at one point, the dipoles are unable to follow the changes. Therefore at these frequencies, the orientation of the permanent dipole no longer contributes to the dielectric constant. Utilizing this aspect that there will be no induced dipole due to the rapidly changing field direction, the capacitive MEAs at higher frequencies will only be sensitive to the local ionic concentration changes and not anything due to the external field. The complex notation of dielectric can describe this phenomenon:

$$\epsilon^\star = \epsilon' - j\epsilon'' \tag{2.12}$$

Where the real part $\epsilon'$ represents the dielectric constant discussed in the prior equations and $\epsilon''$ is the imaginary part known as the dielectric loss. Mutual transformation relations as a function of frequency were developed by Kramers-Kronig, and the absolute values of these constants can be estimated by the Deby-Drude equations that reveal the dependence of $\epsilon$ with frequency.

$$\epsilon^\star = n^2 + \frac{(\epsilon_s - n^2)}{1 + j\omega\tau} \tag{2.13}$$

$$\epsilon' = n^2 + \frac{(\epsilon_s - n^2)}{1 + \omega^2\tau^2} \tag{2.14}$$

$$\epsilon'' = \frac{(\epsilon_s - n^2)\omega\tau}{1 + \omega^2\tau^2} \tag{2.15}$$

Where n is the refractive index, $\epsilon_s$ is the static dielectric constant, $\omega$ is the frequency, and $\tau$ is the mean collision rate - momentum scattering time.

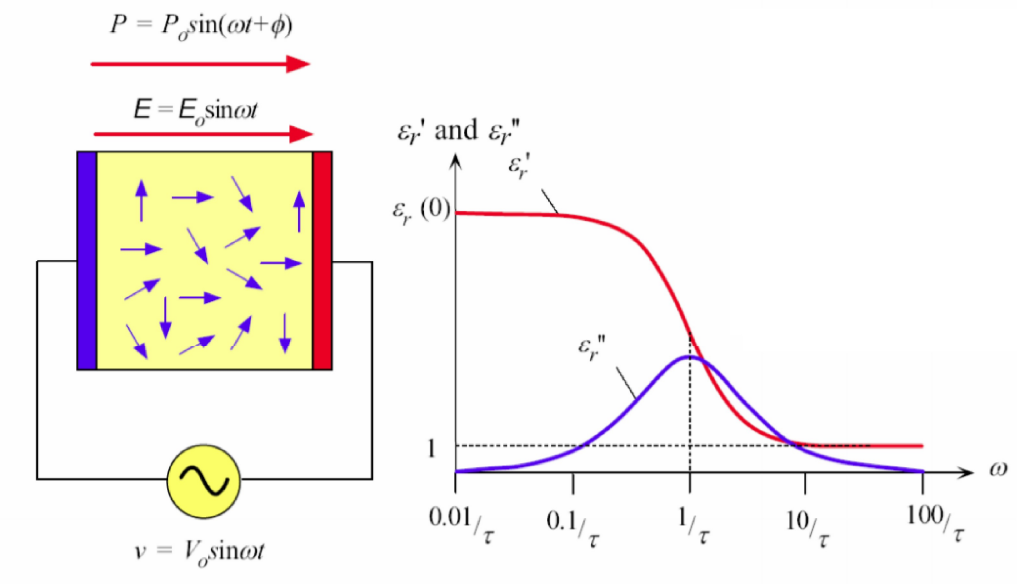



Figure 2.3: For an AC field, components of complex dielectric constant with respect to frequency

As discussed earlier, variation in the concentration of electrolytes varies the number of ionic species, thereby influencing the polarizability of water reflected in the change in dielectric constant. For measurements using electrodes, there could potentially be other effects of ionic concentrations that are causing a change in dielectric constant. Through Debye-Huckel theory,[38] it was proposed that the static dielectric constant varies by a linear relationship as

$$\epsilon_{ss} = \epsilon_{sw} + \delta C \tag{2.16}$$

Here the $\epsilon_{ss}$ is the static dielectric constant of solution or electrolyte, C the concentration and $\epsilon_{sw}$ is the static dielectric constant of water. This change of dielectric concerning concentration can be seen in figure 2.4. The parameter $\delta$ is known as the dielectric decrement and is variable for different ion species. This difference is based on the sizes and number of different ions. Thus, changes on $\epsilon_{ss}$ would make the complex dielectric to change as well. Therefore by a transitive relation, a change in the concentration would yield a change in not just the static dielectric but also in a complex dielectric for alternating fields.

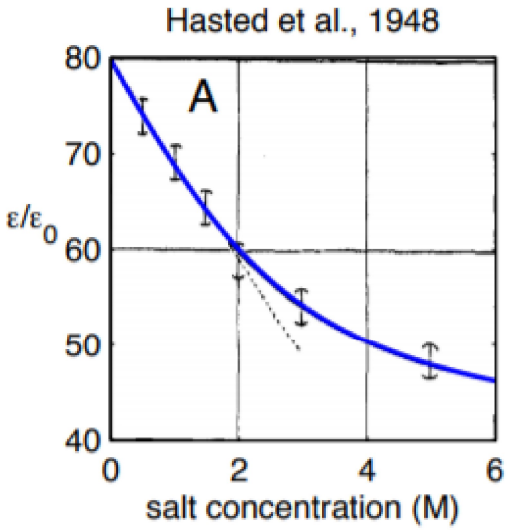



Figure 2.4: Static dielectric versus concentration

### 2.2.1 Cell - Electrode Interface

The interface between the electrode and electrogenic neural cells can be represented by an equivalent circuit as shown in figure 2.5.[1] Action potentials propagating through the ion channels in the neuronal membrane (illustrated by purple lines in the figure 2.5) an imbalance of charge arises. The neural electrical interface then transduces Time-varying imbalance from multiple neurons. This interface can then be put into an equivalent electrical circuit with passive components Constituents such as buffer resistance ($R_s$), trace resistance ($R_m$), shunt capacitance ($C_s$) and amplifier impedance can typically be ignored for a well-developed system. Electrode material resistance ($R_e$) and electrode double-layer capacitance ($C_e$) together known as electrode impedance ($Z_e$) along with seal resistance ($R_{seal}$) are the most important parameters to understand the interface. Therefore for this project, the main emphasis is on understanding the electrode impedance ($Z_e$) for various frequencies and to see how it fairs in higher frequency range.

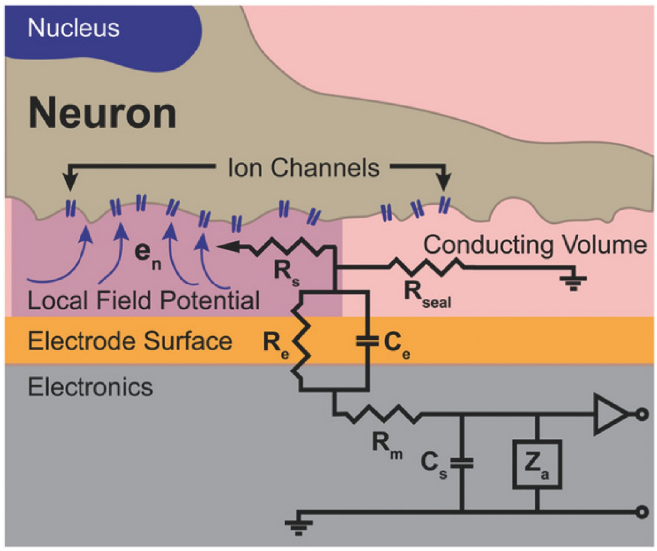



Figure 2.5: Equivalent circuit at the electrical measurement interface (Borrowed from [1])

## 2.3 Capacitance of co-planar electrodes

To understand the capacitance between two electrodes on the same plane and the mathematical basis behind it, one can study it by an analogy to symmetrical-strip lines as shown in figure 2.6.[39] This attempt to solve for the capacitance per unit length for strip lines would require the use of the Schwarz-Christoffel transformation by which the estimation can be made much more straightforward. Schwarz–Christoffel transformation is a conformal mapping of the upper half-plane to the interior of a simple polygon such as a rectangle.

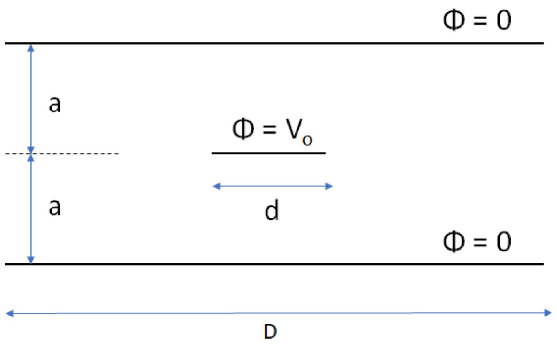



Figure 2.6: Symmetrical strip transmission lines

If the spacing $a$ is much much smaller than the width $D$ of outer strips, the field at the edges would necessarily be zero. This allows us to assume that the outer strips are infinitely wide. The thickness of the center strip is negligible and environment for this problem sake would be free space with electrical parameters $\epsilon$, $\mu$. By the principle of symmetry, the electrostatic boundary-value problem is reduced to that illustrated in figure 2.7.

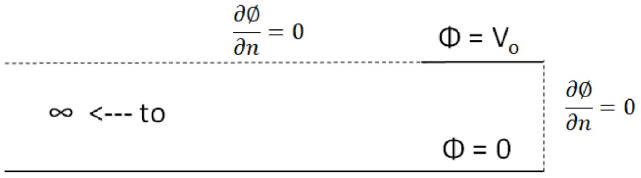



Figure 2.7: Simplification of strip lines using symmetry

By the application of Schwarz-Christoffel transformation, the strip lines are mapped onto a rectangle for easier analysis. This mapping is in the W plane, which is the standard complex plane with curvilinear coordinates. The gradient of the potential $\Phi$ is zero as we traverse through portions of the boundary. With reference to the next figure 2.8, as the points $W_1$ and $W_4$ tend to $-\infty$, a capacitor configuration can be obtained.

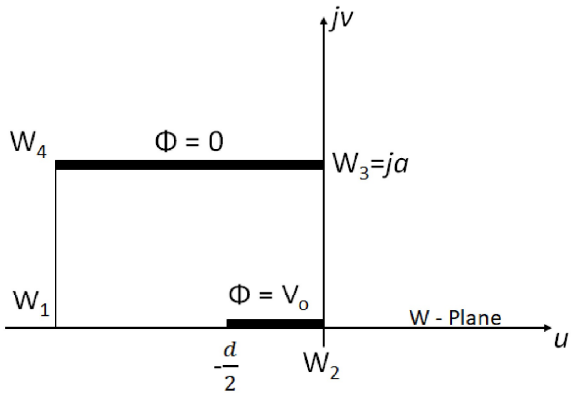



Figure 2.8: Conformal mapping into rectangle in W complex plane

To solve this boundary-value problem more efficiently, we make a transformation to project the polygon from W plane into the real axis of the Z (complex) plane.

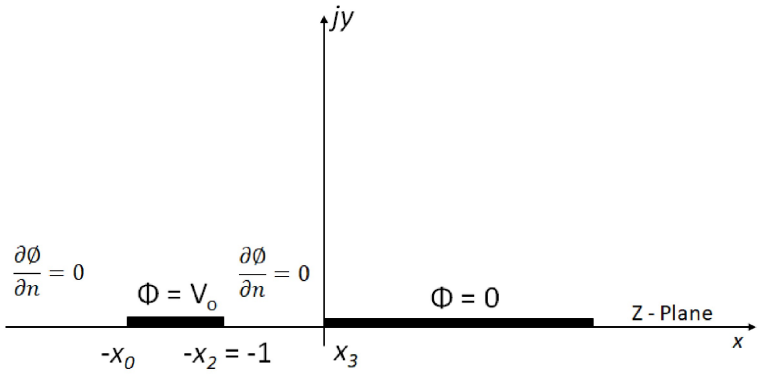



Figure 2.9: Conformal mapping in Z complex plane

By which the mapping function takes the form,

$$W = A' \int^{Z} (Z - x_1)^{-1/2}(Z - x_2)^{-1/2}(Z - x_3)^{-1/2}(Z - x_4)^{-1/2} dZ + B$$
$$= A \int^{Z} [(1 - \frac{Z}{x_1})(1 - \frac{Z}{x_4})(Z - x_3)(Z - x_2)]^{-1/2} dZ + B \tag{2.17}$$

Where A = A'$(x_1 x_4)^{-1/2}$ and A' is an arbitrary constant. Further simplified to final transformation

$$W = -\frac{2a}{\pi} \ln[Z^{1/2} + (Z + 1)^{1/2}] + ja \tag{2.18}$$

For W = -$d/2$, Z would correspond to be -$x_0$. From equation 2.18 we then get,

$$x_0^{1/2} + (x_0 - 1)^{1/2} = e^{d\pi/4a}$$
$$x_0 = \cosh^2(\pi d/4a) \tag{2.19}$$

Since the boundary-value problem in the Z plane is still as difficult to solve as the first case, and it puts us in the same position as the beginning. Therefore a different mapping function is used to map the above The x-axis in Z plane to form a rectangle in another W' complex plane as shown in figure 2.10.

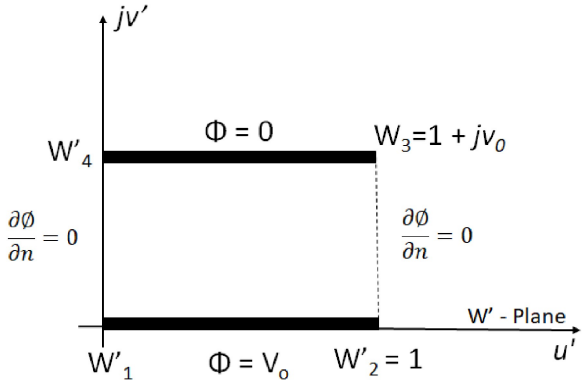



Figure 2.10: Final mapping for a strip-line cross section in W' complex plane

If it is possible to perform this mapping and transform it into W' plane, the capacitance can be determined easily, since the boundary-value is more easy to solve. It is obvious that capacitance is C $= \epsilon/\upsilon$, where $\upsilon$ represents plate spacing in W' plane. In the W' plane, the boundary conditions can be brought up to be $W_1' = 0$ for Z = -$x_0$, $W_2' = 1$ corresponding to Z = -1, and finally $W_3' = 1 + j\upsilon$ with Z = 0. Therefore the required mapping takes the form,

$$W' = A_1 \int^Z \frac{\mathrm{d}Z}{[Z(Z + x_0)(Z + 1)]^{1/2}} + B_0 \tag{2.20}$$

This integral cannot be evaluated directly and thus cannot be minimized into basic functions. However, it represents an inverse elliptic function, for which there are evaluation tables readily available. To evaluate the constants, we apply the boundary conditions by substituting the values Z = -$x_0$, -1, 0 and corresponding values of W'. The $sn^{-1}(x, k)$ function is elliptical and can be defined by an integral as below

$$sn^{-1}(x, k) = \int_0^x \frac{\mathrm{d}\lambda}{[(1 - \lambda^2)(1 - k^2\lambda^2)]^{1/2}} \tag{2.21}$$

where x may be a complex variable, and k is called the modulus of the elliptic function. Since $B_0$ is as yet arbitrary in equation 2.21, we may put in a lower limit of integration and, by introducing a new constant,

$$A_0 = 2jA_1/x_0^{-1/2}$$

Finally solving for the required mapping in equation 2.20 we obtain $\upsilon_0$ by which the capacitance can be calculated as C = $\epsilon_0/\upsilon_0$

$$\upsilon_0 = \frac{-jsn^{-1}(1, x_0^{-1/2})}{sn^{-1}(x_0^{1/2}, x_0^{-1/2}) - sn^{-1}(1, x_0^{-1/2})} \tag{2.22}$$

The function sn(x +$jy$) is periodic in nature both in x and y. For x with a period of 4K, thus

$$K = \int_0^1 \frac{\mathrm{d}\lambda}{[(1-\lambda^2)(1-k^2\lambda^2)]^{1/2}} \tag{2.23}$$

and period of 2K' in y, where

$$\begin{aligned} K' &= \int_0^1 \frac{\mathrm{d}\lambda}{[(1-\lambda^2)(1-\lambda^2+k^2\lambda^2)]^{1/2}} \\ &= \int_1^{1/k} \frac{\mathrm{d}\lambda}{[(\lambda^2-1)(1-k^2\lambda^2)]^{1/2}} \end{aligned} \tag{2.24}$$

Also sn(K - jK') = 1/k, and sn K = 1; so $sn^{-1}$(1,k) = K, and $sn^{-1}$(1/k,k) = K - jK'. Therefore, equation 3.15 gives

$$\upsilon_0 = \frac{K}{K'} = \frac{K(k)}{K(k')} \tag{2.25}$$

where k' = $(1-K^2)^{1/2}$ and K as given by equation 3.16 represents a complete elliptic integral of the first kind. The table below depicts how $x_0$, K, K', and $upsilon_0$ vary for typical variations in the parameter d/a. This table is compiled by estimating $x_0$ for a given value of d/a by utilizing equation 2.22. Since our analysis was limited to the mapping of a one-quarter section in the W' plane, the capacitance per unit length of the stripline would be four times the calculated value. hence C = $4\epsilon_0/\upsilon_0$. Assuming an air-filled line, $Z_c = 30\pi\upsilon_0$ would be the characteristic impedance. The key to analyzing such co-planar problems is to utilize conformal transformations from which characteristic impedance and capacitance per unit length are easy to explain from the above equations. Thus an inference can be made that increasing the (d/a) characteristic value, the $\upsilon_0$ value decreases. Since this term $\upsilon_0$ is inversely proportional to the capacitance, design of these co-planar electrodes can be tuned to have maximum capacitance.

| ***d/a*** | $x_0$ | ***K*** | ***K'*** | $\upsilon_0$ |
|---|---|---|---|---|
| 2 | 6.3 | 1.64 | 2.26 | 0.695 |
| 4 | 134 | 1.57 | 3.84 | 0.41 |
| 6 | $0.25e^{4\pi}$ | 1.57 | 6.98 | 0.225 |
| 8 | $0.25e^{5\pi}$ | 1.57 | 8.55 | 0.184 |
| 10 | $0.25e^{10\pi}$ | 1.57 | 16.4 | 0.0958 |

Table 2.2: Parameters to estimate capacitance of coplanar strips

## 2.4 Principles of Lock-in detection

Lock-in detection is a technique used to extract a signal from a noisy background in time domain.[40] In order to pick up the very small changes from the cells using MEAs, we employ this technique. A lock-in amplifier uses the concept of lock-in detection where it multiplies the input signal with a reference signal after which a low-pass filter is applied to the result, as shown in figure 2.11. This multiplication isolates the signal at the interested frequency from rest all frequency components. This is known as Phase-Sensitive Detection. Averaging over time the signal-to-noise ratio (SNR) of the signal can be increased, allowing detection of very small signals with high accuracy and making lock-in amplifiers suitable for such applications. The reference signal is either generated in the amplifier itself or supplied externally. A sine wave is commonly used as a reference and upon demodulation allows selective measurement at the frequency of interest or any of its harmonics.

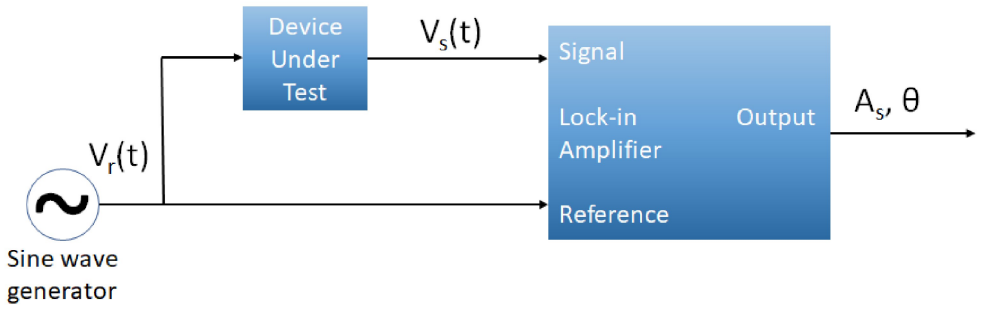



Figure 2.11: Basic measurement setup of a lock-in amplifier [Source: Zurich Instruments]

Most amplifiers multiply the signals using a mixer along with a band-pass filter and the resulting signal is low-pass filtered. The mixer shifts the input signal to baseband (ideally DC), and the low-pass filter removes all the higher frequency components. This is shown in schematic 2.12 where the reference and a 90-degree phase-shifted reference is multiplied with the input signal using mixers. This constitutes the quadrature components, capable of measuring both amplitude and phase.[41] The outputs are low-pass filtered to remove the higher harmonics and noise. The output is the demodulated signal (X +iY), where X is the real and Y the imaginary part which is then converted into polar coordinates. This can be done with the help of the equations 2.26 and 2.27.

$$R = \sqrt{X^2 + Y^2} \tag{2.26}$$

$$\theta = \arctan(Y, X) \tag{2.27}$$

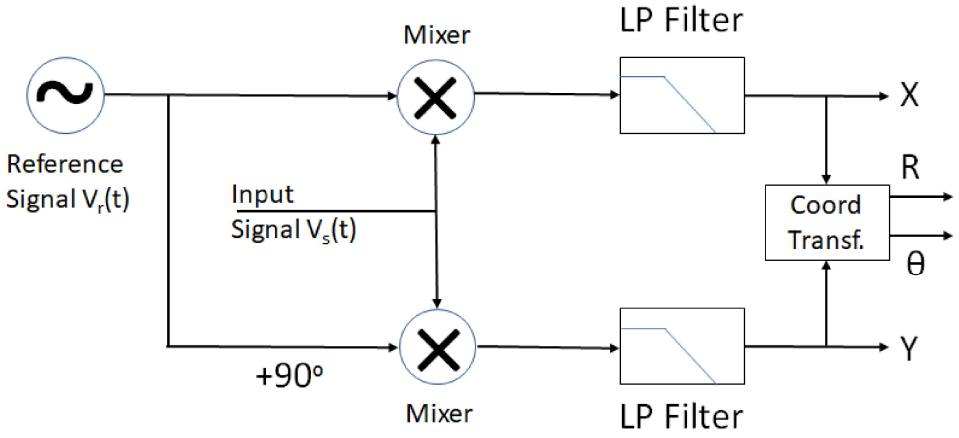



Figure 2.12: Mixing and low-pass filtering in a lock-in amplifier [Source: Zurich Instruments]

Lock-in detection is important for work like this to measure small, stationary or slowly varying signals which are completely buried in noise like thermal noise or the 1/f noise and slow drifts. This technique allows the weak signal to be shifted to a higher frequency away from the noise as depicted in figure 2.13. This modulated signal can be shifted back efficiently after filtering the noise, which can further be measured using a lock-in amplifier.

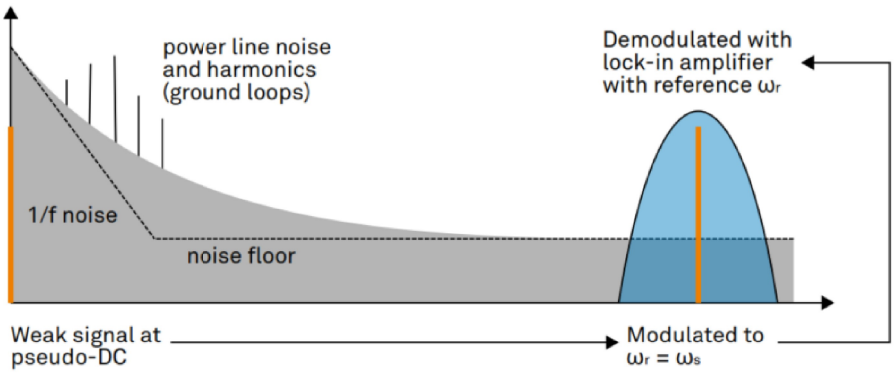



Figure 2.13: Lock-in detection of a noisy signal [Source - Zurich Instruments]

## 2.5 Conclusions

In this chapter, the background theory behind the ionic interactions and phenomena occurring at the electrode-electrolyte interface have been explained. Next the important aspects of the behavior of aqueous dielectrics was explained. From which it can be concluded changes in concentration and frequency change the dielectric constant. This project represents MEAs that exactly exploit this point of theory. Based on the equivalent circuit the cell-electrode interface is visualized and we learn that impedance is a direct indication of sensitivity of detection. Finally, capacitance calculations were worked out for the coplanar electrodes to understand how various dimensional parameters affect the capacitance value. Basing on this, the MEA design choices were made.

# Chapter 3

# Methods

This Section summarizes the methodologies used to build these MEAs for recording the extracellular signals from neurons. The methods section can be broadly classified into three segments: firstly the aspects and design of the MEA sensor, then the methodology for the fabrication of these MEAs and finally the experimental setup with the recording electronics, cell culturing, imaging and data analysis.

## 3.1 MEA system for cell culturing

MEAs as sensors allow both recording and stimulation, making them one of the most widely used means for electrical measurements on in-vitro experiments. They are economical to manufacture and reusable upon proper cleaning. Electrodes allow the exchange of ionic and electrical currents and detection of changes in electrical parameters. Therefore it is crucial to make careful design considerations for these electrodes. MEAs have two main advantages: first, the electrodes are made in the micrometer scale comparable to that of the cellular sizes for better cellular-electrode contact. Second, it is an array of multiple electrodes which allows simultaneous access to various cells. Simple MEA design would look like that in figure 3.1.

(a) (b)

Figure 3.1: Commercial MEA from Multi-channel systems (3.1a). Outlook, (3.1b). Zoomed in version of the microelectrodes

The characteristics of the recorded signal depend on contact between the electrode and cells (area, etc.), electrode characteristics (geometry, material, noise), signal processing (bandwidth, gain, etc.). Out of these tunable parameters, the electrode characteristics such as the shape, size, material, etc. are the most critical design considerations atleast to fabricate MEAs.

## 3.2 Design of MEAs

Microelectrode arrays designed in this work are comprised of Gold electrodes patterned over a glass substrate. MEAs were created in a standard fashion with that of the Multi-Channel systems with the micro-electrodes fanning out to much larger contact pads as seen in 3.3. It is these contact pads that can be integrated with the external electronics. As explained earlier, neurons due to the incoming and outgoing of ions change the concentration of ions in the electrolyte, which in turn changes the polarizability of water, giving rise to changes in dielectric constant. This implies, in a way, the cell body acts as the dielectric. This change is seen in the changing dielectric constant that can be picked up electrically, and the geometry of the electrode plays a crucial role to detect these. Therefore the MEAs designed were of different sizes and varying inter-electrode distance all arranged as capacitors (or symmetrical strip lines). The motivation was to see how the size or the inter-electrode distance affects the sensitivity. A trend of increasing sizes and parameters like inter-electrode distance was maintained to provide a control and allow one to draw conclusions with ease.

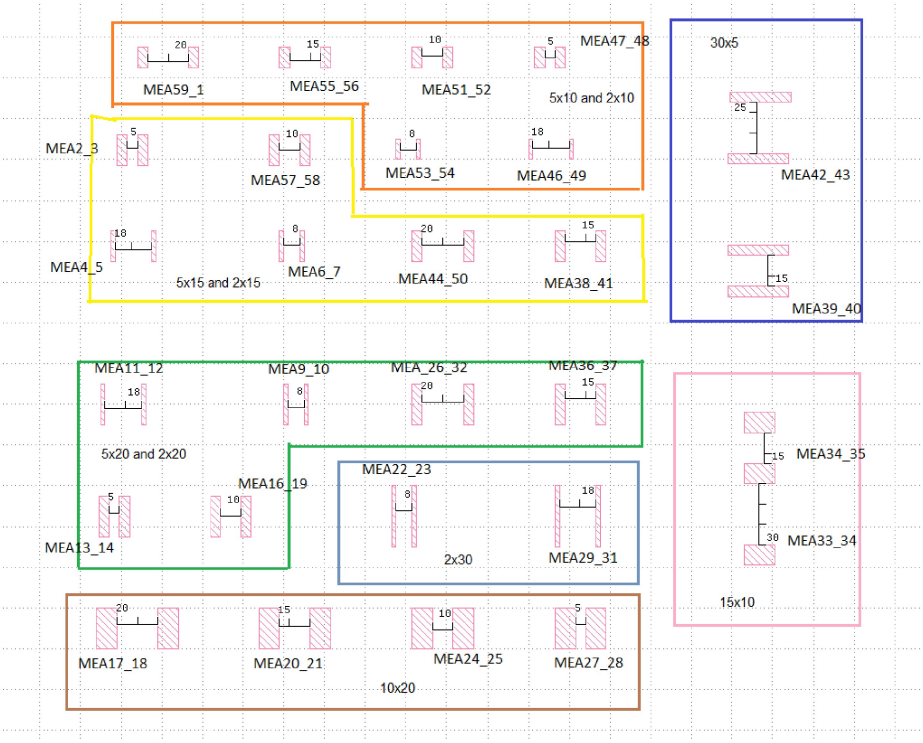



Figure 3.2: Various trends in electrode distance and size

Since these MEAs were produced by lithographic patterning techniques; the microelectrode arrays would have to be patterned with the help of a mask. K-Layout, an open-access CAD software, was used to design the mask for the MEAs and to generate the GDS II file that was further transferred onto a mask. The design was carefully inspected for uniformity and to make compatible with a commercially available MEA (Here Multi-channel systems standard 60-electrode MEA) enabling one to compare the performance between both as shown in figure 3.3. The MEA created has 55 working electrodes to record or stimulate and one relatively larger reference electrode. To obtain better yield, the design was set to make three MEAs (two identical MEAs with rectangle shape and varying sizes and one with diverse shapes as shown in figure 3.4) on a single 4-inch glass wafer. The smallest feature size was designed to be 2 microns making it comparable to the size of subcellular features of a single neuron. No features were opted below this value as it then becomes difficult to print a mask with finer details and also the reliability to pattern such small features is low. For patterning the Gold

electrodes, the bottom layer mask was designed and then to pattern an insulation layer over the whole MEA except the electrodes and contact pads, an upper layer mask was designed. The bottom layer and upper layer masks were printed such that the layer on the CAD is not transparent, and the rest are. Alignment markers were added to enable alignment of the top mask with the pattern transferred from the bottom mask on the wafer.

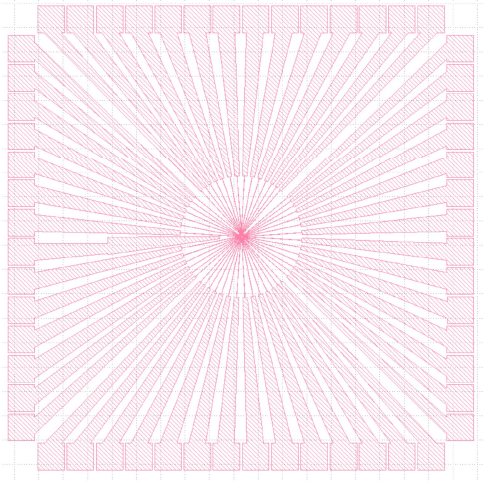
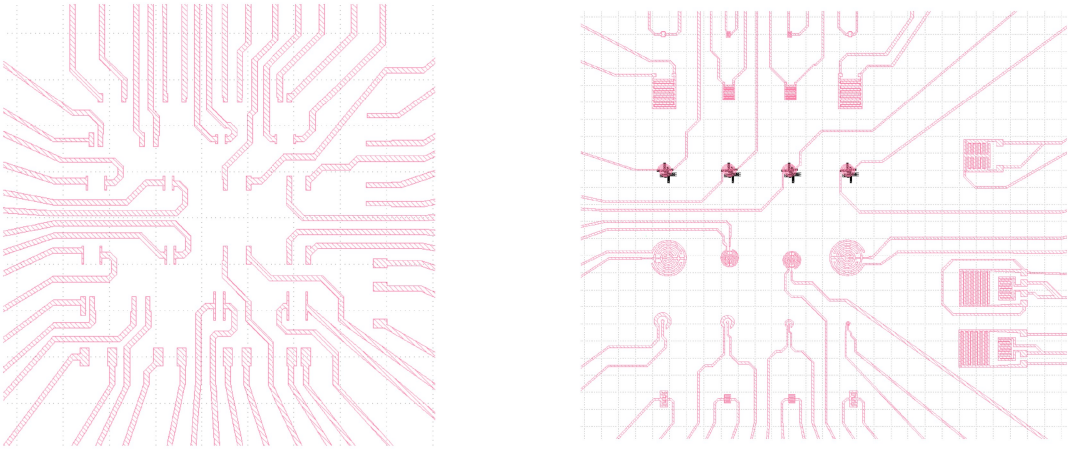


Figure 3.3: K-Layout mask CAD design of a complete MEA with contact pads



(a) (b)

Figure 3.4: (K-Layout mask CAD design of a MEA 3.4a). with rectangle shape and varying sizes, (3.4b). with diverse shapes

## 3.3 Fabrication of MEAs

Cleaned glass wafers of 500-micron thickness were spin-coated with a photoresist which was then baked and exposed to UV light through the mask. The spinning RPM was adjusted to obtain a desired thickness of resist coating. Since the feature polarity is negative to assist lift-off with a darkfield mask, a negative photoresist was used. Meaning the region which is not exposed to the light will be removed by the developer. A negative photoresist was chosen because it is possible to obtain an undercut profile, which is not the case with positive photoresist. After exposure, the wafer was developed in an etching developer and rinsed thoroughly leaving the pattern on the photoresist.

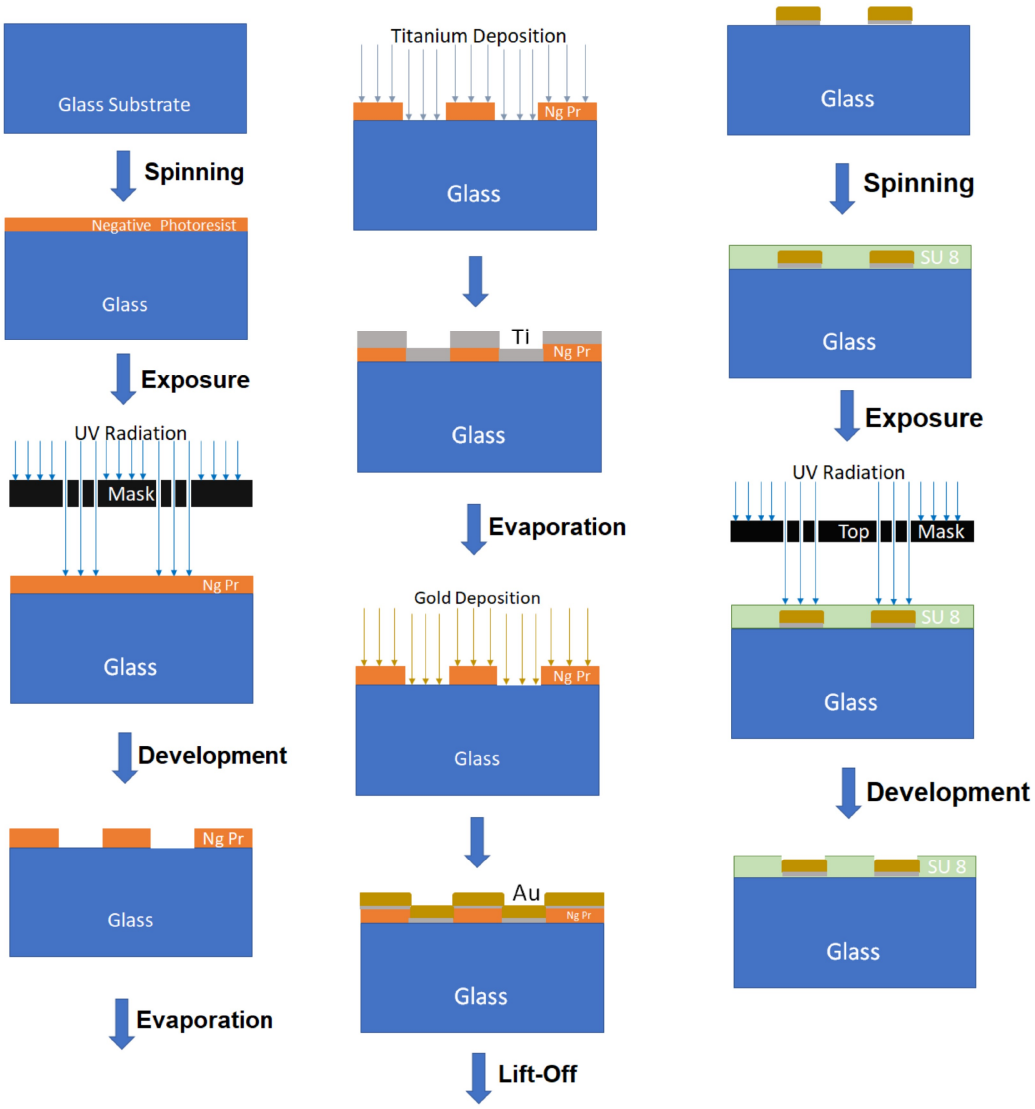
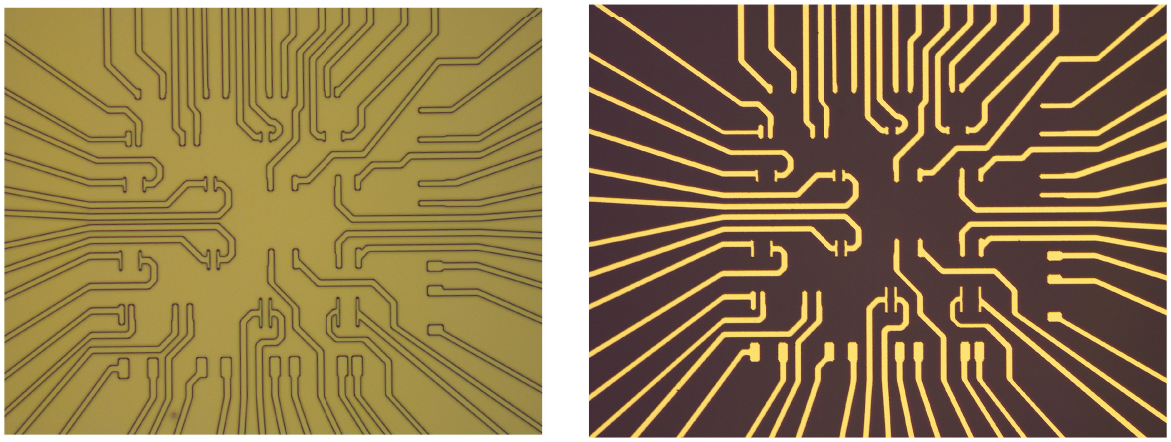



Figure 3.5: Flow chart for MEA fabrication process

Gold (Au) of roughly 150 nm thickness with a ≈ 5 nm Titanium (Ti) adhesion layer was evaporated on this wafer containing patterned resist. A thin layer of Ti is used to increase the adhesion between Au and glass. Au was chosen because of its high conductivity and less degradation from environmental factors. Wafer with an evaporated layer of Au-Ti was then immersed in a solvent for the lift-off of tracks. Warm Di-Methyl Sulfoxide (DMSO) was used as the solvent in an ultrasonic bath for lift-off. The wafer was placed upside down during this process such that the dislodged Au does not re stick to the wafer side with features. Since the adhesion between Ti and glass is very high, during lift-off, the solvent attacks the photoresist. Photoresists are usually soluble in solvents, thereby allowing the lift off. The ultrasonic bath assists in faster lift-off process due to agitation, this way the Au-Ti in contact with the glass is retained and the rest of it is released. Once the electrodes, with the tracks and contact pads, are neatly visible, the wafer is rinsed and prepared for adding an insulation layer.

A polymer SU-8 was spun to insulate the whole wafer. SU-8 was chosen because of its high transparency in thin layers and good stability. This transparency would help us during imaging of the MEA with cells. As the Au electrodes have to make contact with the cell body, the SU-8 layer was

patterned using the top layer mask, exposing just the electrodes whilst the rest is insulated. With the aid of alignment markers already patterned using the bottom mask, the top mask was aligned with accuracy for exposure. Patterning of SU-8 involves additional steps such as pre-baking, post-baking, and developing to get accurate patterns. The pre-baking step is done to evaporate the solvent to make the SU-8 photoresist more solid. The post-bake step is to provide energy for the reaction to proceed after exposure. Finally, a hard bake step was done to evaporate all the solvent and harden the SU-8 polymer, this makes it chemically and thermally inert thereby acting as a protection and electrically insulating layer. This entire process can be explained as in flowchart **??** to yield results of neatly patterned MEAs.



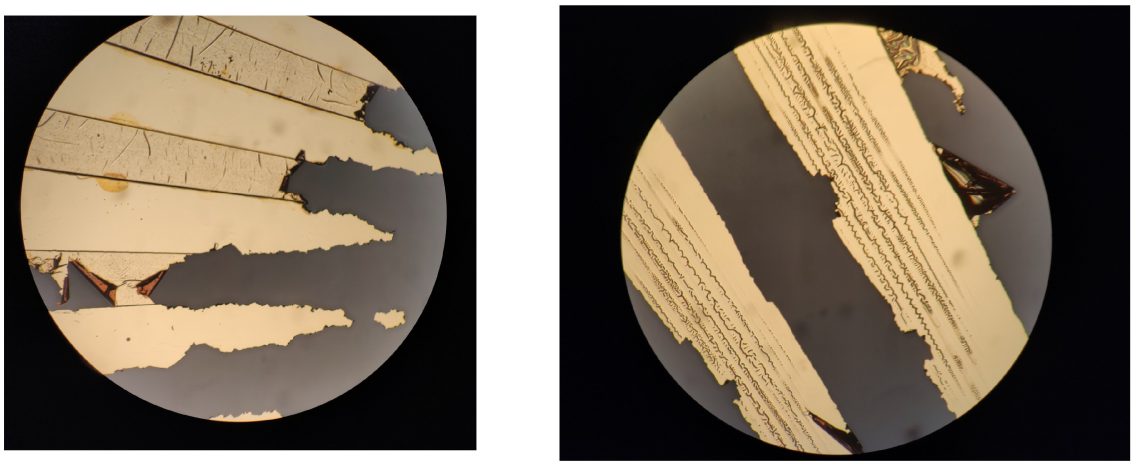
(a) (b)

Figure 3.6: Fabricated MEAs (3.7a). Gold deposited on patterned Photoresist, (3.6b). Patterned microelectrodes after lift-off process

### 3.3.1 MEA fabrication issues

Fabrication of these MEAs involved a lot of fine-tuning to obtain perfect patterns. Considering the major challenges encountered, they have been explained in detail, and the solution thought of has also been put forward.

#### Broken tracks during lift-off



(a) (b)

Figure 3.7: MEAs with broken tracks wile lift-off

One of the critical problem faced was the breakage and damage of tracks and at times even breakage of electrodes during the lift-off process. Ultrasonication was used to aid the lift-off process as agitation assists in allowing the solvent to penetrate the photoresist quickly, thereby releasing the unwanted gold. But several trials during fabrication resulted in the tracks being broken or complete dislodgement of gold film or layer from the wafer soaking in DMSO solvent. This problem was identified as residual under-developed photoresist still present on the glass wafer. Due to these remnants, when titanium and gold are evaporated, there was still some resist left underneath, which reacted with the solvent causing the removal of gold. This was rectified by carefully regulating the ultrasonic power. Next by making sure that the development process is complete. A series of quality control steps, i.e. to visually inspect if there are any remnants of resist and by thorough cleaning of the wafer with DI water after the development process. Employing these precautions made sure that perfect tracks and electrodes were fabricated.

**Fringes after exposure**

Another complication during the fabrication was with the exposure. After spinning the photoresist and baking, the wafer was exposed to UV radiation through the mask. But this resulted in fringe-like patterns (as shown in figure **??** and figure **??**) being developed on the resist rather than that the mask pattern exactly being transferred.

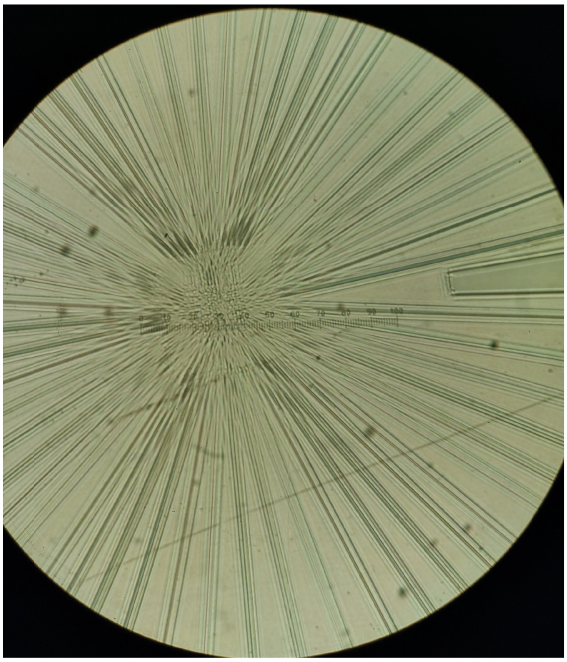


Figure 3.8: Fringe like patterns seen on photoresist after exposure

It was identified that this was a result of the soft-contact setting in the exposure program. The soft-contact program places the mask above the wafer with a gap of 100 microns. Given that the minimum feature size was 2 microns, placing the mask this far apart created diffraction at the mask causing some amount of light to be scattered around the actual pattern. This scattered light not being strong enough caused only partial reaction with the resist. On development, this partial resist, along with the exposed resist, created these fringes. These structures were similar to how stairs look like, but with a gradient. Due to this, it was difficult to focus on the edges using a microscope.
This was corrected by setting the program to hard-contact in which the gap between the mask and the wafer is only 20 microns. Additionally, a black non-reflecting sheet was placed beneath the glass wafer to prevent any backscattering. After changing the program and using the black sheet has provided

clear mask patterns being imprinted on the resist.

**Exposure and development times**
Another major issue from the beginning was the adjustment of exposure and development times. The MEA design in this project has sizes going from 2 millimeter down to 2 micrometer. Thus it was necessary that not just the larger feature sizes were transferred but also the finer ailments were inspected for proper features. Going down to such small feature sizes like 2 microns, the exposure dose listed in the datasheet of the resist had to be adjusted. On performing exposure with the listed dosage resulted in overexposure again causing fringe like patterns. This was corrected by performing a study by varying the dosage and gauging the resultant patterns. The same was performed on development times, optimizing them to get properly patterned structures. A table describing one of such study has been listed in Appendix 1.

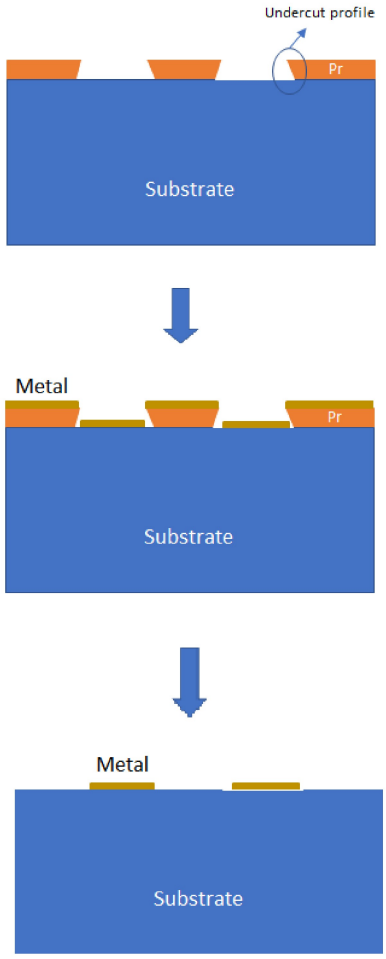



Figure 3.9: Description of undercut profile

This study was repeated over different development times as well. Being an intensive optimization,

such studies do demand lot of preparation and time. Moreover, the development times were set to slightly higher values than the one required to obtain perfect features. This was done on purpose to enable slight over-etch, which resulted in an undercut profile. Undercut profile is advantageous for the fact that when Au-Ti is evaporated, it allows the gold deposited on the glass to be discrete and not connected to the gold on the resist. Thereby allowing more cleaner lift-off process. It can be illustrated, as shown in figure 3.9.

## 3.4 Electronic interface board for readout

An electronic readout interface board was designed to tap into the contact pads, thereby enabling one to either record or stimulate into an electrode. The task of stimulating is the equivalent of writing operation from the interface board, and the task of recording from an electrode would be reading operation. The circuit implemented has 64 pins connected to switching multiplexers out of which 60 were connected via pogo pins to all contact pads of an MEA. By using this board, one can tap into all the electrodes at once and perform simultaneous read/write operation of their choice at any two electrodes. Connected only through two BNC connectors that fan-out and fan-in into the electrode pins can be directly connected to a bench-top measuring instrument via BNC cables. This can be visualized with the block diagram 3.10

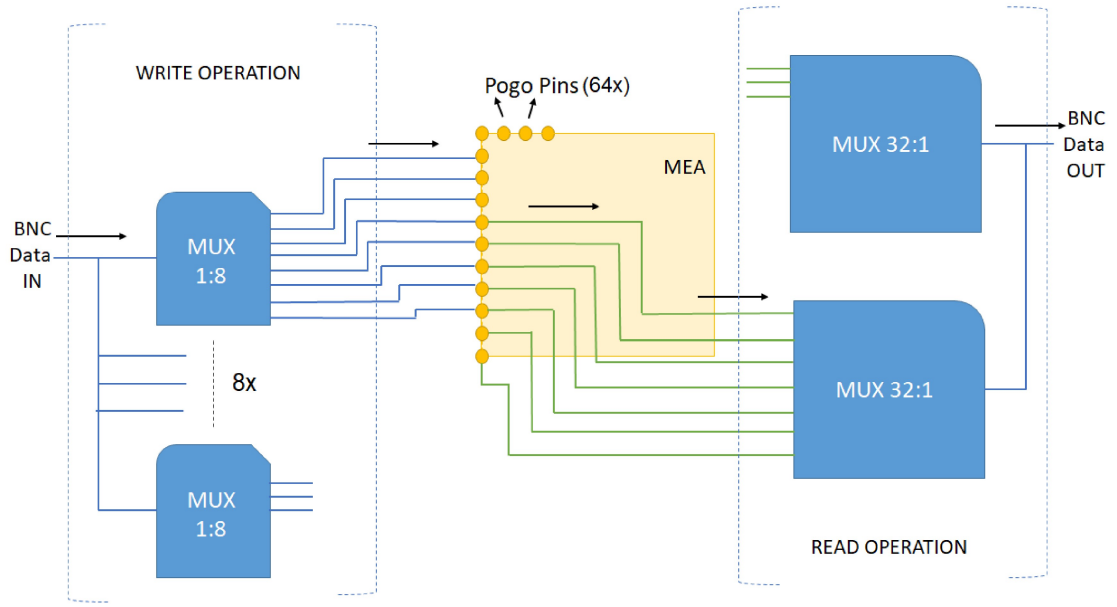



Figure 3.10: Block diagram of the PCB interface board

Separate top the shelf multiplexer integrated circuits (ICs) were used to design this switching circuit. Specifically ADG731 and ADG738 were preferred due to their low noise levels and faster switching (more details have been listed in Appendix 4 with datasheets of these ICs). Therefore each of the pins connects to one of the read switches and one of the write switches. The multiplexers were controlled using SPI interface. All of these switching ICs were laid out on a Printed circuit board (PCB) along with the powering electronics and a microcontroller to control them. The PCB designed was a four-layer PCB with the second layer being the power plane and the third layer the ground plane. Write switching multiplexer based traces were laid out on the top side of the PCB and the read traces on the bottom side for isolation. Careful precautions were taken to match the grounds and implement a

noise/interference reduction design. The design was optimized to match the trace lengths as much as possible to avoid any impedance mismatch. For the read operation, all the 64 pins were connected to two 32:1 multiplexer (switches) and the outputs of these two ICs were combined to fan-out into the read BNC connector. Similarly, for the write operation, the BNC connector getting the input signal fans-in to eight 1:8 multiplexers (switches) thereby giving 64 lines, which are further connected to the MEA.

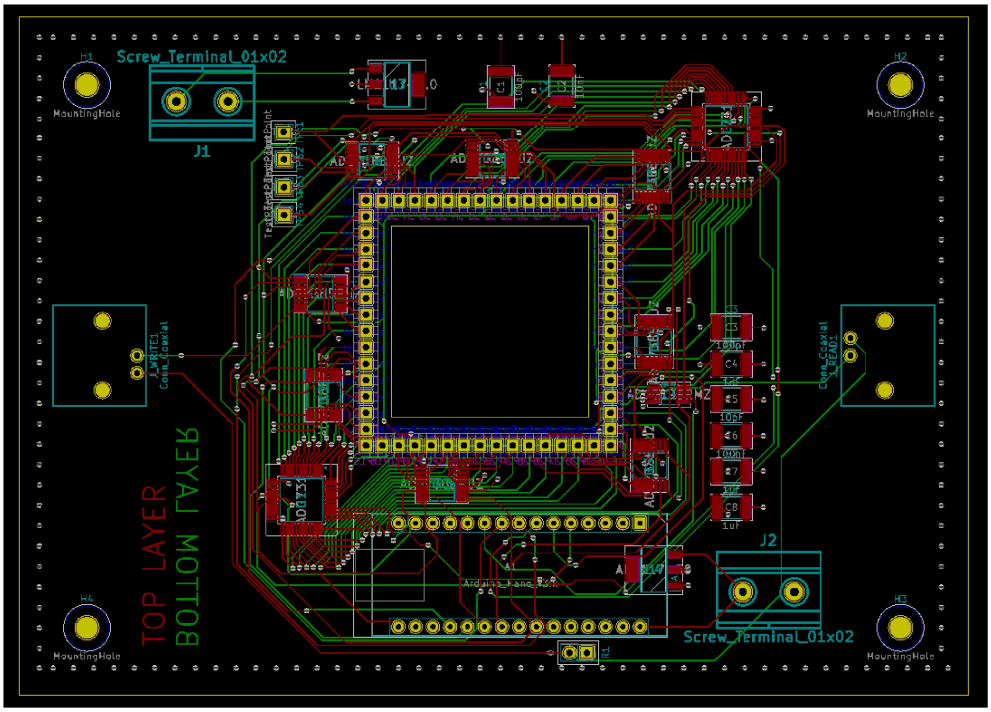



Figure 3.11: PCB layout for interface board

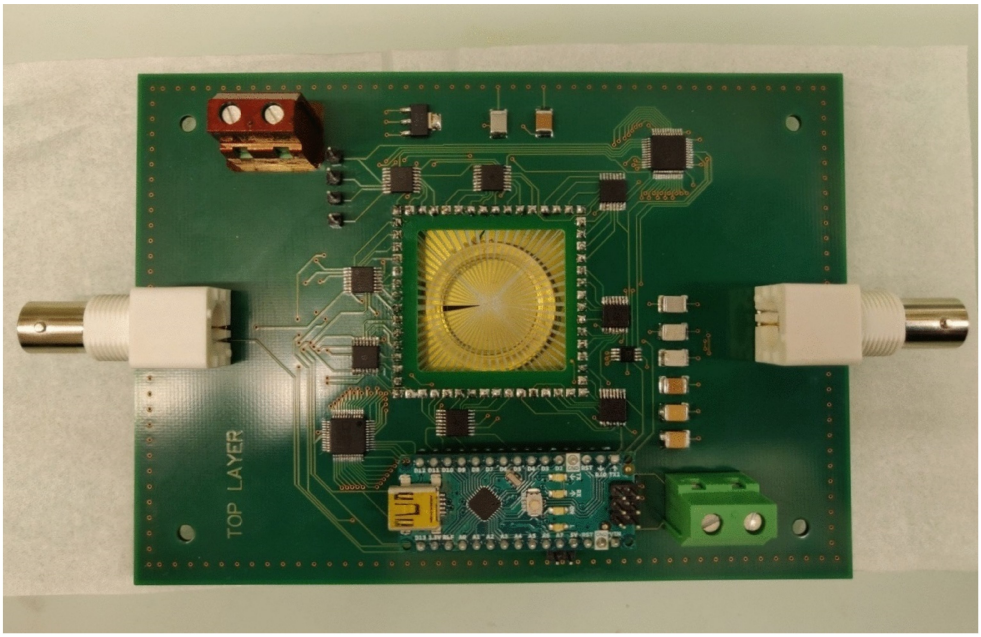



Figure 3.12: PCB interface board with MEA placed inside

## 3.5 Bench-top setup for electrical measurements

The electrical signals from the cells being small in amplitude are integrated with noise. It is for this purpose that electronic processing techniques in the form of measuring instruments are needed to enhance the signal. One of the most common techniques for detecting signals which are comparable and integrated with noise is the coherent detection or more commonly known as lock-in principle. Thus all real-time electrical measurements from the neurons, impedance measurements, and noise measurements of MEAs were realized with a lock-in amplifier HF2LI (Zurich Instruments, Switzerland).
Lock-in amplifiers work on the principle of phase-sensitive detection. A known periodic reference signal is modulated with the signal coming from the device under test (here from neurons) which alters the phase and amplitude. On comparing these changes by synchronizing with the reference signal, lock-in amplifiers can measure even very minute signal changes that are overwhelmed by noise. This lock-in amplifier was combined with preamplifiers namely trans-impedance amplifier and current amplifier (HF2TA and HF2CA, Zurich Instruments, Switzerland) to pre-amplify the signal coming from the electrodes by setting the gain and coupling.

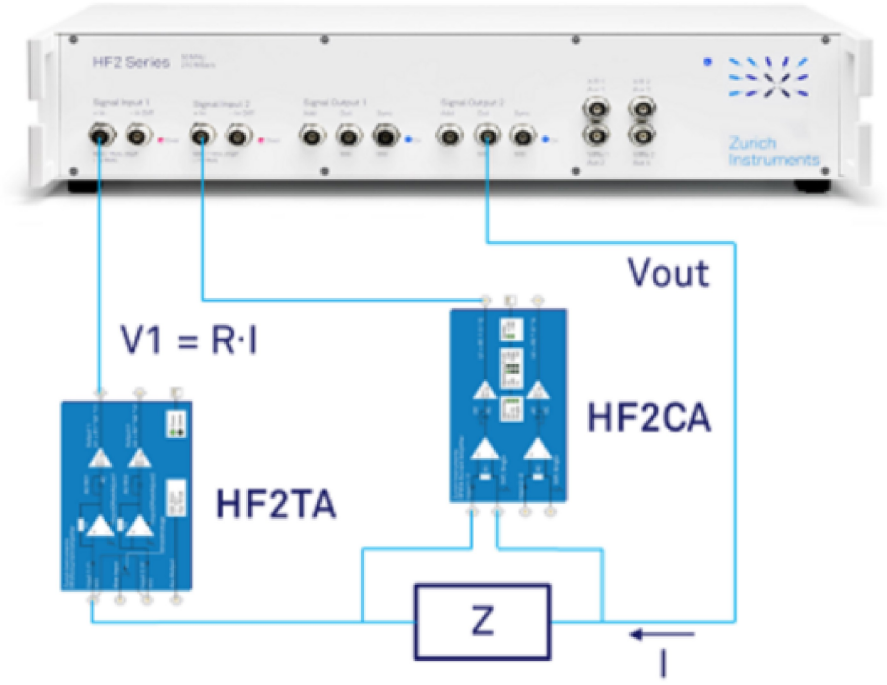



Figure 3.13: HF2LI four-point measurement setup

To measure impedance with high accuracy with taking into account all characteristics of Z, four-point setup is chosen. The four-point method is an accurate simultaneous measurement of current flowing through the measured impedance and voltage drop across the device via two separate paths. This is implemented by injecting voltage through one of the electrodes and measuring current from the neighboring electrode. Being a different sensing paradigm, the voltage injected, and the frequency of this signal are relatively high. For much higher accuracy, the voltage preamplifier with high-input impedance causes a voltage drop across the impedance $V_Z = VIn2$. This drop is measured differentially through the HF2CA and then converted to single-ended input to the lock-in amplifier. The current through the impedance is directly connected in a single-ended fashion to the lock-in amplifier. Both

the amplifiers are connected via ethernet cables to the lock-in instrument and can be set and used through the user interface of Zurich Instruments - Lab One. Assuming that the $V_{In2}$ is the voltage drop across Z, R and G are the resistor setting and the gain of the trans-impedance amplifier; then the impedance can be estimated using the following equation:

$$Z = R * G * V_z/V_{In1} = R * G * V_{In2}/V_{In1} \quad \text{(assuming voltage pre-amp gain = 1)} \tag{3.1}$$

The Lab One graphic user interface provides a wide range of options to tune the lock-in amplifier. This software enables one to optimize parameters such as the lock-in frequency or the reference frequency, sampling rate, filter characteristics to omit higher harmonics, etc. HF2LI lock-in amplifier has a signal generator that can be combined to output the reference signal as well. Therefore as per the four-point setup, the output of the signal generator was used as the reference signal over the MEA setup (into the write BNC of PCB running into one electrode), i.e., the stimulating signal. The read signal from the MEA setup (from the read BNC of the PCB coming from the neighboring electrode) was connected to the transimpedance amplifier as this carried the electrical current from the electrode. This transimpedance amplifier converts this current into a voltage, making it easy for the lock-in amplifier to measure it.

## 3.6 Cell culturing

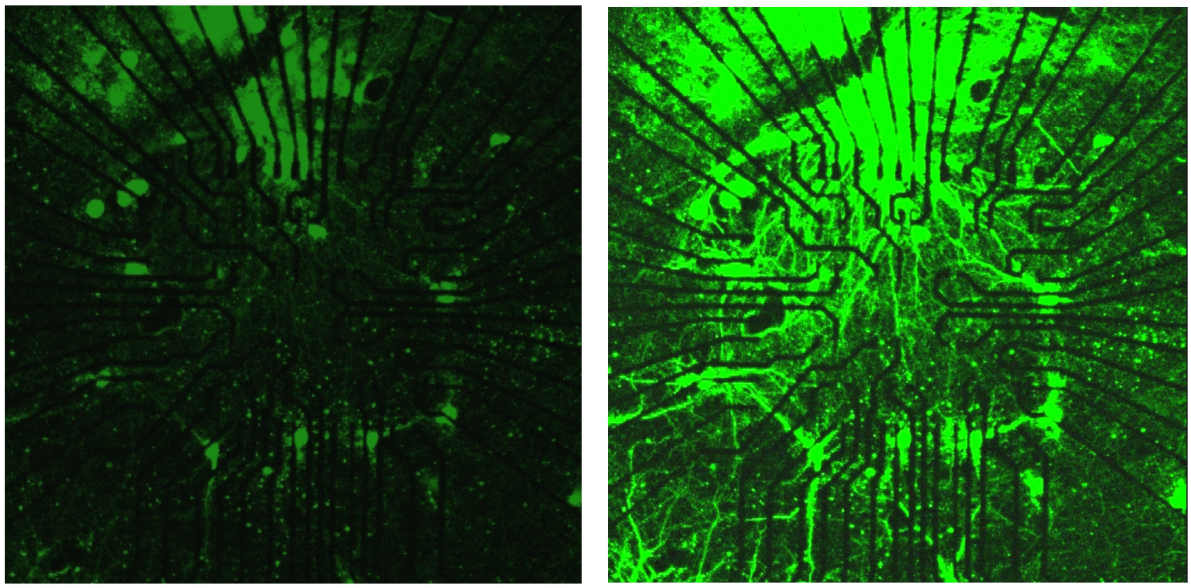
To this point, the MEA was designed, fabricated, integrated with a readout board, and measuring instruments. This section now describes the process of cell culturing and the protocols used. Using a plastic ring over the MEA, a well was created to seed the neuronal cultures. This plastic ring was attached to the MEA by the help of the polymer Polydimethylsiloxane (PDMS) and baking it at 100-120 degrees for 10-15 minutes to fixate it. This is followed by thorough rinsing and cleaning of the MEA with ethanol, 2% SDS in millipore (soap), and milli-Q water (ultrapure water). To remove any remaining organic compounds and to majorly active the surface to be hydrophilic, the MEAs were plasma cleaned using O2 plasma. Making the surface hydrophilic allows more adhesion of poly ( D- Lysine) (PDL). Coating the MEA with PDL acts as an attachment factor, thereby enhancing cell adherence. After $\geq$ 40 min, PDL was washed out with pure buffer solution more than three times from the MEA ready for seeding of neurons.

All neuronal cultures were primarily hippocampal cells from E18 embryos of time-mated pregnant Wistar rats (Harlan Laboratories, Netherlands). The Cantonal Veterinary Office approved all animal experiments of Zurich. The cortices were dissociated in a 37 ° C / 5% CO 2 incubator for 15 min in 5 mL of a filter-sterilized solution of 0.5mg / mL papain and 0.01mg / mL deoxyribonuclease in PBS supplemented with 0.5 mg / mL bovine serum albumin and 10 mM D - (+) - glucose. The supernatant was then removed and resuspended three times with 5mL of Neurobasal medium supplemented with 2% GlutaMAX and 1% penicillin-streptomycin, thereby leaving the cells dissociated and suspended in the medium. The remaining solution was gently clipped. Then, the cell solution was spun down and re-suspended into new media reading for seeding. This protocol has been explained in detail in Appendix 2. Approximately 1 ml of solution with roughly 200,000 neurons were seeded per well. For functional imaging experiments, un-tagged cells were transfected at DIV5 with a calcium indicator - GCaMP (AAVDJ.hSyn1.GCaMP.WPRE.SV40, University of Zurich Viral Vector Facility, Switzerland) for convenient visualization during activity measurements. Across all trials, cells were seeded onto new MEAs. Each MEA was one of the best ways to ensure all MEAs were of optimal quality. In all experiments, media was changed every three DIVs and needed constant supervision. These MEAs were stored in an 37 ° C / 5% CO 2 incubator.
The cell cultures seeded were many a times not useful for making measurements. This was sometimes due to the cells dying due to lower viability or the neurons not present over the desired electrode regions or even that the neurons are present and alive but not connected/firing. Due to this multiple cell cultures were seeded but only little amount of data could be recorded.

## 3.7 Calcium (Ca+2) Imaging and Confocal Laser Scanning Microscopy (CLSM)

One of the key goals of the project is to detect neural activity of in-vitro cultures which is indicated by recording the action potentials from the culture. These action potentials are spikes in the electrical domain arising from the synchronous firing of the neuronal network. Therefore it is a necessity to verify that these spikes are actually originating from the activity of neurons and are not from external factors such as noise. For this verification process, Ca+2 imaging was performed on the cellular cultures being electrical recorded from.

Ca+2 imaging is the technique that uses so-called calcium indicators, fluorescent molecules that respond to the binding of Ca2+ ions by changing their fluorescence properties. By this technique, one can monitor the out/in- flux of Ca+2 ions traversing through the membrane. This correlates to the firing of neurons since various ions like potassium, sodium, or calcium are exchanged across the membrane of a neuron during an action potential. Genetically encoded calcium indicators (GECI) derived from green fluorescent protein (GFP) are used to indicate the Ca+2 ions. These need not be loaded onto cells; rather, these can be efficiently transfected to cell lines through proteins. As mentioned in the previous section, GCaMP is the calcium indicator used for these experiments, and GCaMP is a GECI. This Ca+2 indicator can now be easily imaged through fluorescence microscopy with a laser running at a responsive wavelength (here 482 nm for GCaMP) as that of the indicator.



(a) (b)

Figure 3.14: Calcium Imaging of neuronal culture on a MEA. (3.14a). Same culture when not firing, (3.14b). Same culture when firing

Confocal laser scanning microscopy (CLSM) is an imaging technique that utilizes a spatial pinhole for blocking out-of-focus light while image formation to increase the optical resolution and contrast. The very same CLSM can be used as a fluorescence microscope to perform Ca+2 imaging. Where the sample (here neural culture) is radiated with the light of a specific wavelength (lasers in general - here 482 nm was used) which causes fluorophores to get excited. Upon de-excitation, they emit light of longer wavelengths. This emitted light is separated using a spectral emission filter and other optical components. Using this emitted light, the image is reconstructed. The working principle of the CLSM can be visualized as below in figure 3.15.

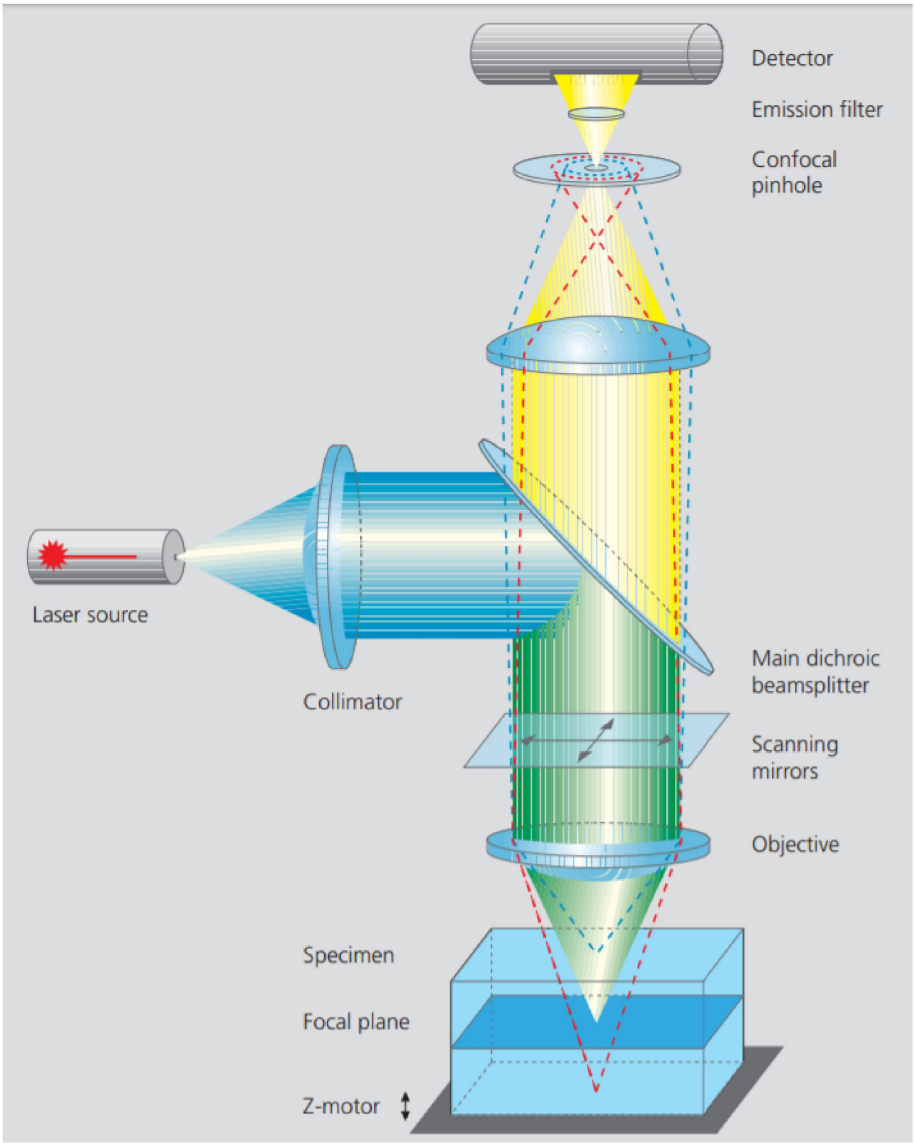
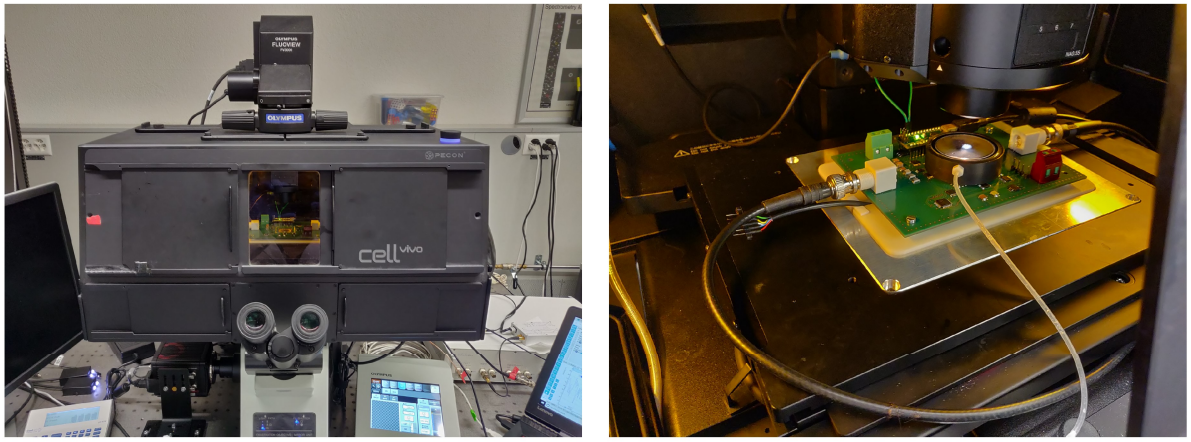



Figure 3.15: Working principle of a confocal laser scanning microscope [Source: Carl Zeiss]

## 3.8 Data acquisition and analysis

So far different methodologies to design, make, and integrate these MEAs have been discussed. But what is important that how all of these components come together as a system or as an experiment to provide data that will allow us to make conclusions. On this line, data acquisition for this work can be broadly classified into two categories: one with cells and the other without cells. Addressing data with cells, the most important experiment is to collect electrical signals using the lock-in amplifier i.e. to observe action potentials during the firing of neurons and concurrently perform imaging to verify these APs. For this, the MEA with neuronal culture was placed along with the PCB interface board in a controlled environment of temperature and $CO_2$ level. This compartment for controlling the environment for the cells (incubator) is also a part of the CLSM microscope, thereby allowing us to electrically measure and image at the same time. Thus a lock-in amplifier placed outside is connected via BNC cables to the PCB board mounted on the MEA with neurons inside the imaging compartment. This setup looks as shown in figure 3.16a and figure 3.16b.




(a) (b)

Figure 3.16: Experimental setup for MEA electrical measurements along with imaging setup. (3.16a). Microscope with an incubator and bench-top lock-in amplifier. (3.16b). Zoomed in version of interface board with MEA inside the incubator

The other category of measurements involve MEA without cells. These experiments are focused on the characterization of the electrodes, their impedance profiles. For this characterization, electrical impedance measurements were made for MEAs with Milli-Q water to get the variation between different sizes of electrodes. Next, impedance measurements with buffer solution (PBS) of various concentration were carried out to understand the dependence of impedance concerning the concentration of the solution in the MEA. For each of these gathered measurements multiple parameters like the frequency, amplitude, impedance, phase were varied and recorded into .csv or .txt file formats as seen in Appendix 3.

To be more specific, the quadrature components (real and imaginary parts) of the voltage $(X_2 + iY_2)$ and current $(X_1 + iY_1)$ signals were acquired by varying the frequency. Using equations 2.26, the respective R values were estimated for both voltage and current independently. Equation 3.1 was then used to calculate the amplitude of impedance based on the four-point setup with the resistance of the transimpedance amplifier to be $R_amp$ (= 1000 ohms here). Similarly, equation 2.27 was used to estimate the phase component — the imaginary part of the impedance obtained in the form of (X+iY) [Eq. 3.6] using both voltage and the current was equation to the $(1/j\omega C)$ to obtain the capacitance. Therefore all the equations used for calculations can be summarized as below:

$$\mid R_{voltage} \mid = \sqrt{X_2^2 + Y_2^2} \tag{3.2}$$

$$\mid R_{current} \mid = \sqrt{X_1^2 + Y_1^2} \tag{3.3}$$

$$\mid R_{total} \mid = \mid Z \mid = \mid R_{amp} * \frac{R_{voltage}}{R_{current}} \mid = R_{amp} * \frac{\sqrt{X_2^2 + Y_2^2}}{\sqrt{X_1^2 + Y_1^2}} \tag{3.4}$$

$$Phase(\theta) = \frac{\arctan 2(Y2, X2)}{\arctan 2(Y1, X1)} \tag{3.5}$$

$$Z = 1000 * \frac{(X_1X_2 + Y_1Y_2) + i(X_1Y_2 - X_2Y_1)}{X_1^2 + Y_1^2} \tag{3.6}$$

$$C = \frac{X_1^2 + Y_1^2}{1000 * 2\pi f(X_2Y_1 - X_1Y_2)} \tag{3.7}$$

Since the gathered data is quite huge, nearly 400 GB data for all the electrical measurements carried out, dictionaries were created in Python to access these files saved in various folders directly. Once the data was read, different parameters were computed and plotted to make conclusions out of.

## 3.9 Conclusions

From this chapter it can be concluded that the MEAs were designed with various sizes and electrode distances. This designed transferred to a mask was used in the fabrication. Extensive training was obtained to effectively master this fabrication process. Alongside various studies were performed in time to optimize the process and to perfect them. More than 75 MEAs were fabricated using the whole process. Lots of major and minor problems were encountered during the whole fabrication process, but were effectively identified and solved to obtain MEAs with good reliability. The interface electronics was designed to make choice of electrodes much simpler to couple with the external measuring instruments. Cell culturing, another time intensive was performed over more than 30 MEAs to obtain reliable data with repeatability. Finally the data acquisition was made by combining both the electrical measurements and imaging.

# Chapter 4

# Results and Discussion

## 4.1 Impedance characterization of MEAs

Characterization is the description of the properties or features of a material or device. It is a necessity to characterize the MEAs fabricated as this allows one to get a proper understanding of the array's itself. Properties such as impedance, capacitance, etc. can be used as the features to describe these capacitive MEAs. Based on the differences between these features such as impedance for electrodes with the varying sizes and inter-electrode distance, it is possible to distinguish and highlight which one's fare better. As described earlier, four-point setup with the lock-in amplifier was used to measure the impedance. First an empty MEA without any solution and then with ultrapure water (milliQ water) was analyzed using the measurement setup. Next PBS in step-wise dilution was put in the MEA and the corresponding impedance was calculated. Graphs were plotted by calculating the real and imaginary part of impedance with respect to frequency for both MEA with milliQ water and PBS filled MEA data. This was performed multiple times (6 measurements) on all electrode pairs of the MEA as shown in figure 3.2 and averaged.

### 4.1.1 Impedance vs Frequency

As explained in the dielectrics for aqueous solutions section, supplying an alternating field changes the dielectric constant. Here this change in dielectric constant is estimated in terms of changes in impedance with respect to frequency.The impedance is calculated by 3.6 looks as in the graph **??** for most of the electrode pairs with slight deviations. It is observed that the impedance is in the order of $10^7$ ohms and drops with the increase in frequency as it should be ideally. This drop is due to the increasing capacitive component. At lower frequencies, spiking behavior was noticed. This is due to the transient behavior of the electrochemical process at the electrode as soon stimulation is started concurrently with a frequency sweep. Due to this reason, only at the lower frequencies, transient fluctuations were seen. Another reason for more unstable behavior at lower frequencies is due to the limitation of the instrument itself. Being close to the low-pass filter cut-off range, the signal being acquired still picks up more amount of noise than at higher frequencies.

For the same impedance characteristic, a sudden spike in the impedance was noticed around frequency of $10^6$, this could be attributed to an inductive influence arising from the PCB interface board. But it can still be seen that the impedance further decreases after this spike therefore allowing one to safely assume that the spike is an artifact. This was verified by measuring the impedance directly from the MEA to the lock-in amplifier without the switching PCB board and the resulting impedance looks like 4.2. For this figure it can be clearly seen that the spike in impedance is less evident implying that this was introduced was PCB and was confirmed with other electrode pairs as well. Thus to make it easier, all the graphs plotted further are limited to the range of 1 MHz. This range is still sufficient to analyse the capacitive sensing scheme.

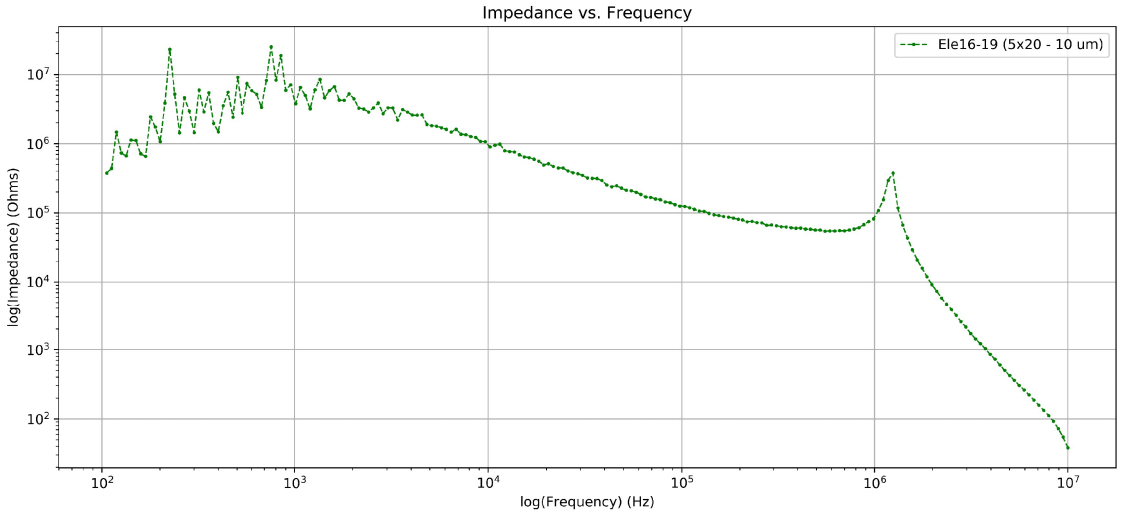



Figure 4.1: Impedance vs frequency characteristic

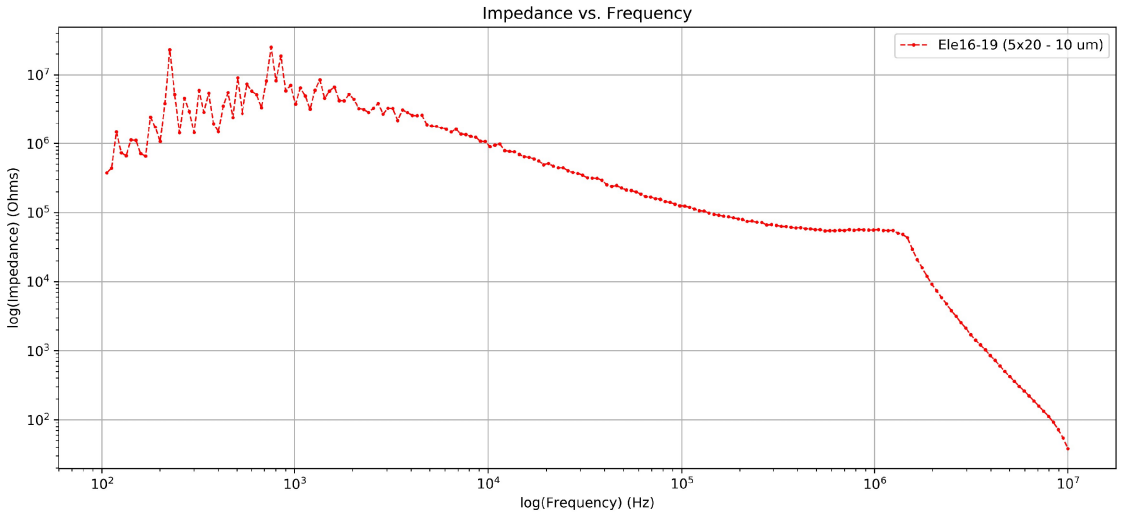



Figure 4.2: Impedance vs frequency without switching PCB board

Sweeping frequency to higher values, the phase was calculated as in 4.3 by using the real and imaginary parts to see if the impedance seen at higher frequencies is capacitive in nature. Due to the noise seen at lower frequencies, it can be observed that the phase also seems to vary abruptly below $10^3$ Hz. But at higher frequencies above this 1 KHz mark, it settles down close to -90 degrees phase, which corresponds to the lag of the capacitive component. Therefore given the fact that we are interested to notice changes at higher frequencies, the fluctuations at lower values can be ignored and capacitive measurements can be done in confidence. Since dielectric constant is related to capacitance, the change in capacitance with frequency have also been plotted. Capacitance is seen to be in the range of $10^{-11}$ (10s of Picofarad) for higher frequency range as shown in figure 4.4. Capacitance also decreases with increase in frequency as expected ideally. This is because of at higher frequencies, the induced dipole moment tends to zero. Since impedance drops with increasing frequency, and impedance being

highly capacitive in nature at higher frequencies also drops. Again due to huge number of electrodes, characteristics for only certain electrodes are shown here but similar behavior was noticed for all pairs.

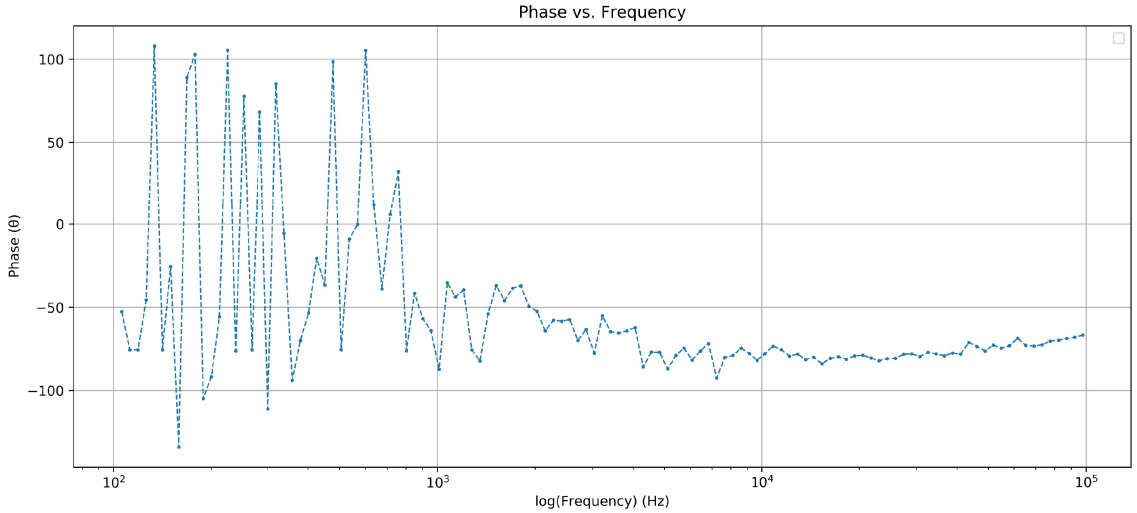



Figure 4.3: Phase vs frequency

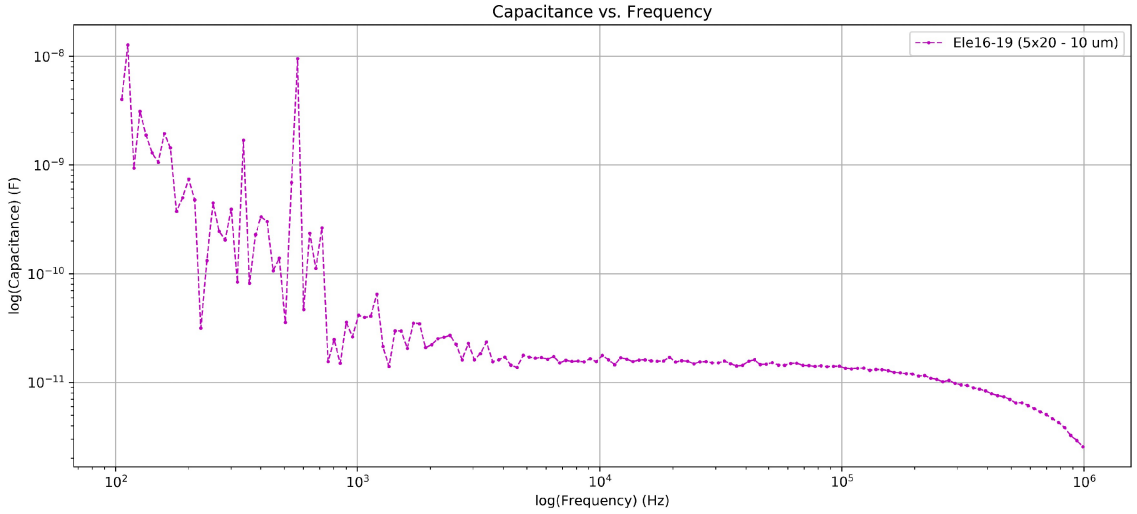



Figure 4.4: Capacitance vs frequency

### 4.1.2 Impedance for varying Electric field

Electric field strength represented by the amplitude of the stimulating voltage was varied and the corresponding impedance versus frequency plot was obtained in graph 4.5. It was noted that increasing the amplitude causes a drop in the impedance and this can be justified as increasing amplitude will cause much stronger field thereby improving the coupling between the electrodes and dropping the impedance. But for very high field ranges ($\geq$ 300 mV), opposite behavior in impedance for varying frequency was observed. The impedance increased with increasing frequency and this can be attributed

to the ionic current tending to zero much faster due to the very strong field. Once the ionic current is no longer the contributing factor, it is only the orientation of the water molecules that induces change in impedance. But at this point, also a strong EDL is formed which further prevents the easy flow of ions towards the electrode thereby increasing the impedance. Another interesting observation made was how the amplitude along with the geometry of electrodes affect the impedance sensitivity. It can be seen between figure 4.5 (5x15 $\mu m^2$/5 $\mu$m) and figure 4.7 (5x15 $\mu m^2$/5 $\mu$m) that the later electrode has lower change in impedance for various amplitudes than the prior case. This can be understood by the optimization of size and inter-electrode distance, in further results it has been shown that increasing the size and decreasing the distance gives much lower impedance and thereby higher sensitivity. This was verified for both the mentioned electrode cases while changing the amplitude as well.

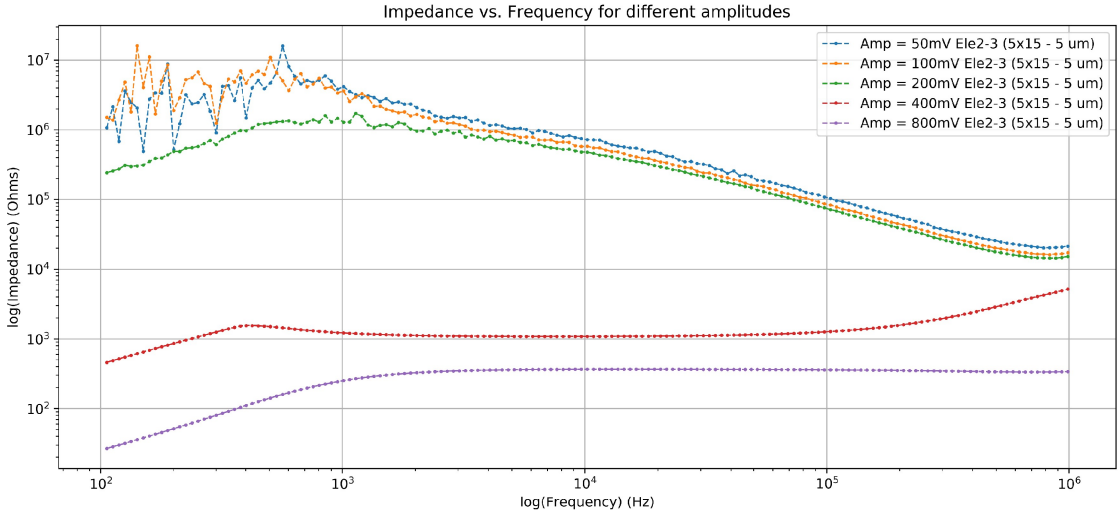



Figure 4.5: Impedance vs frequency for varying amplitude for 5x15 $\mu m^2$/5 $\mu$m

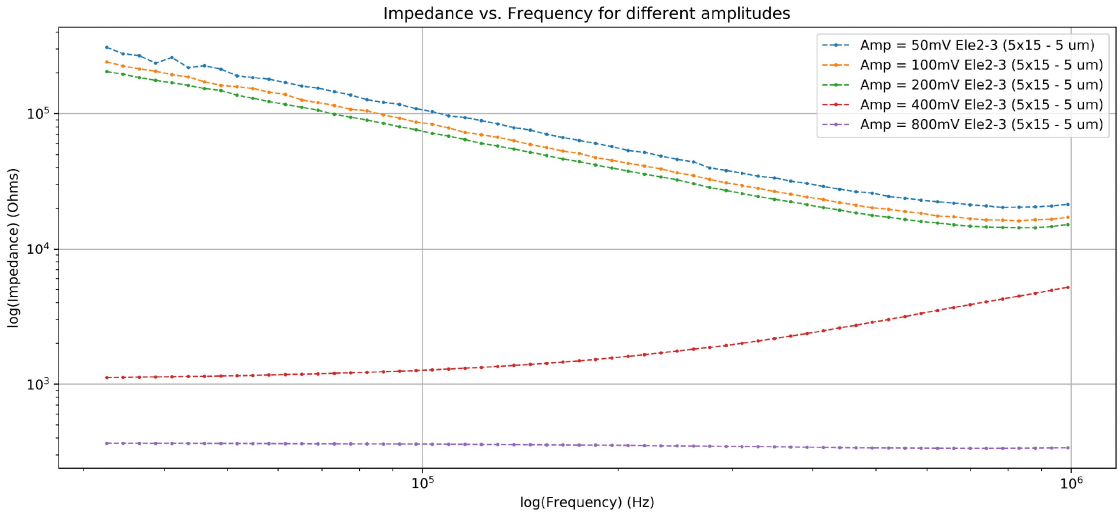



Figure 4.6: Zoomed-in Impedance vs frequency for varying amplitude for 5x15 $\mu m^2$/5 $\mu$m

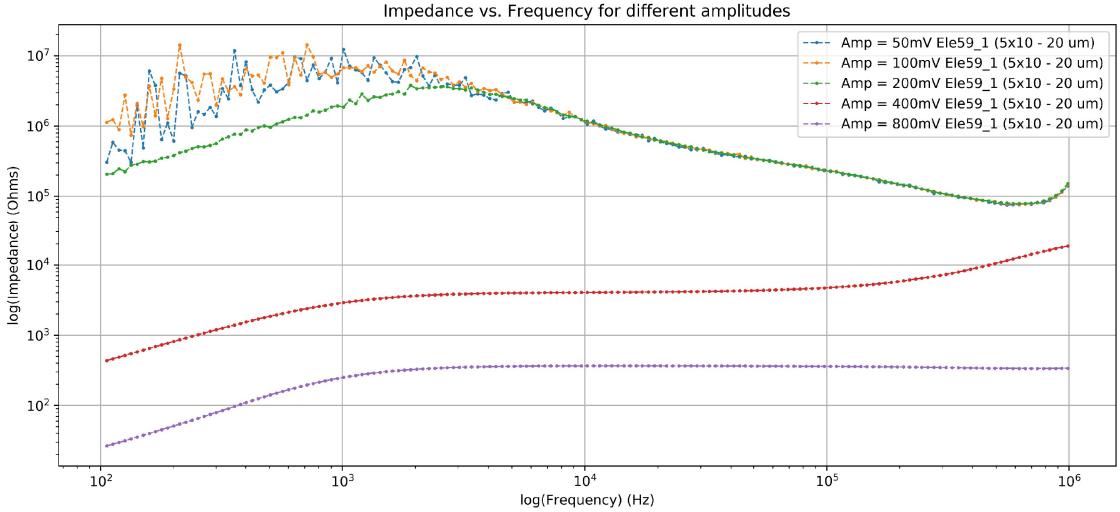



Figure 4.7: Impedance vs frequency for varying amplitude for 5x10 $\mu m^2$/20 $\mu$m

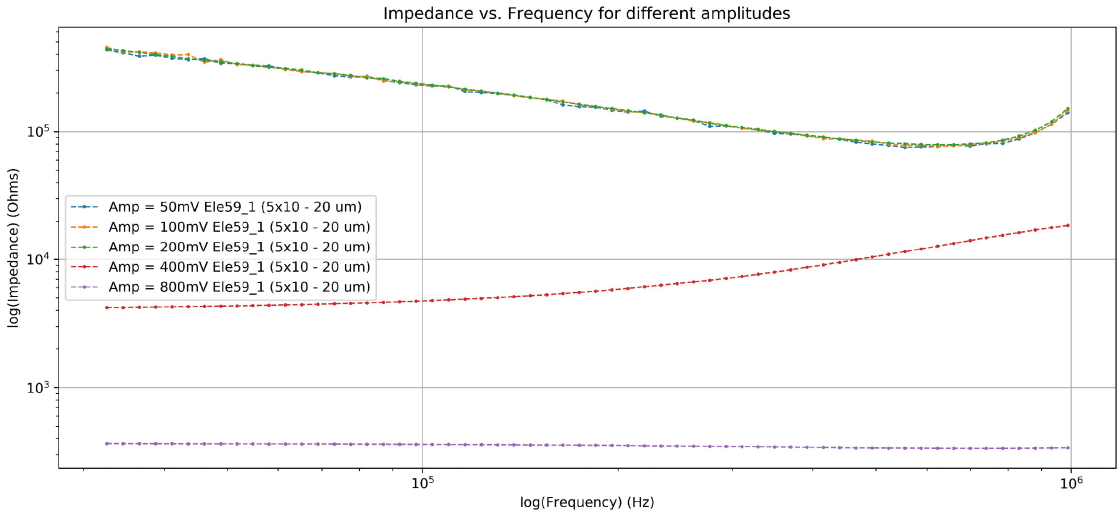



Figure 4.8: Zoomed-in Impedance vs frequency for varying amplitude for 5x10 $\mu m^2$/20 $\mu$m

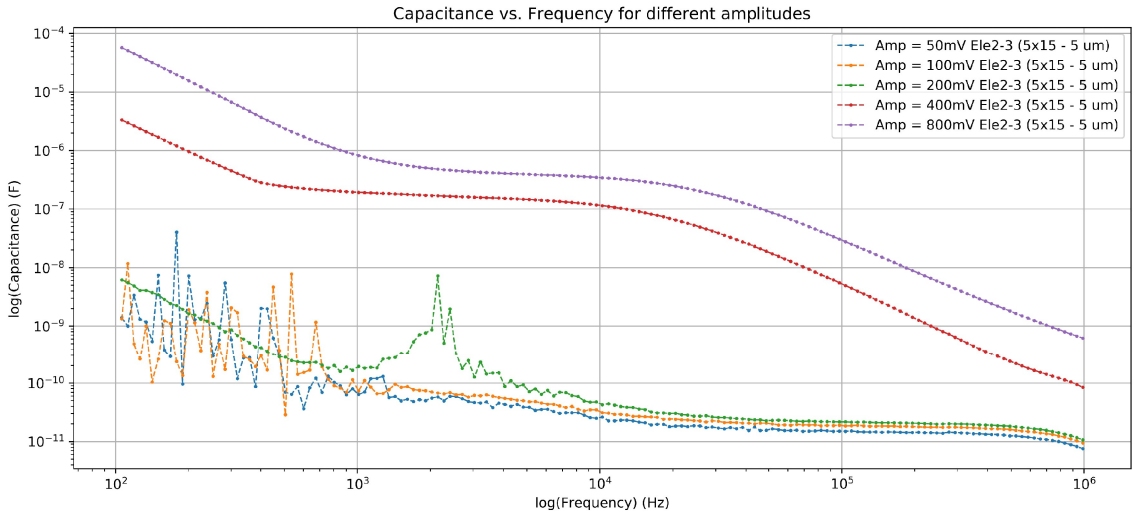



Figure 4.9: Capacitance vs frequency for varying amplitude for 5x15 $\mu m^2$/5 $\mu$m

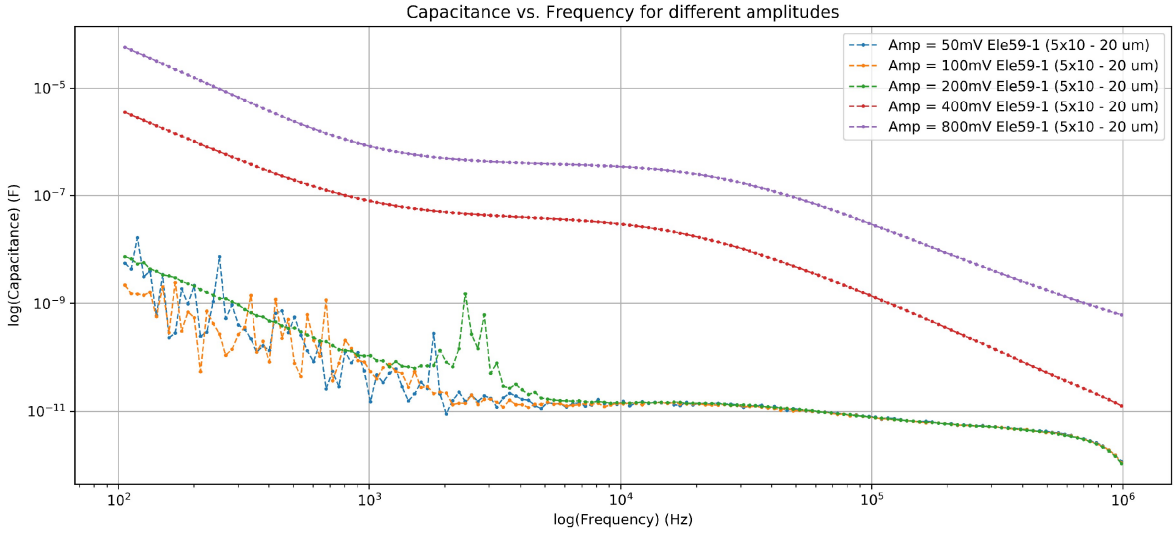



Figure 4.10: Capacitance vs frequency for varying amplitude for 5x10 $\mu m^2$/20 $\mu$m

### 4.1.3 Variability across various MEAs

All the measurements were obtained over three MEAs and have been averaged over all of them to obtain all the results listed in this report. The variability between MEAs has been shown in figure **??**. The graph shown represents the variability for one set of electrodes, but this is consistent with all other electrodes across the three MEAs.

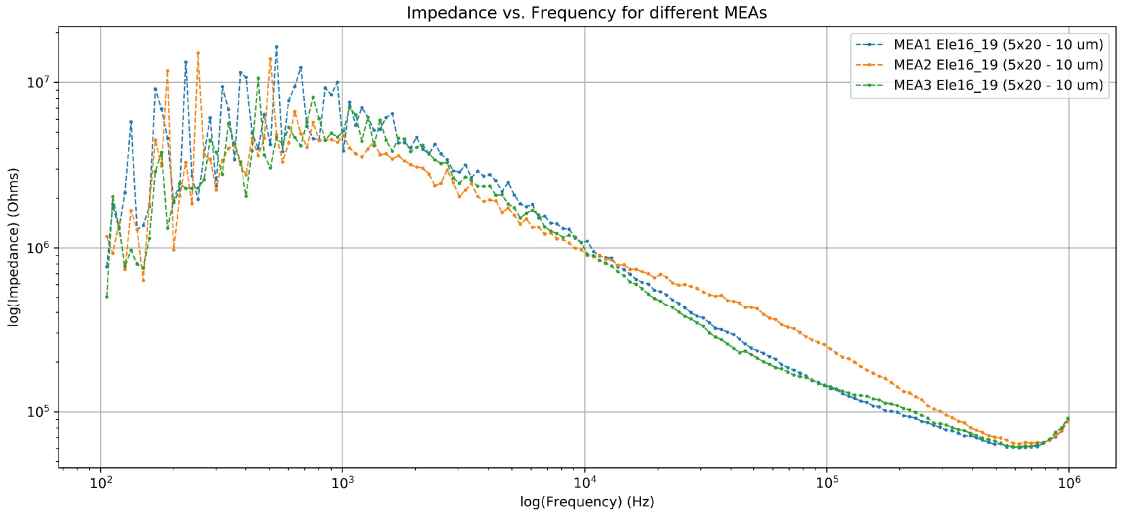



Figure 4.11: Impedance vs frequency variability over multiple MEAs

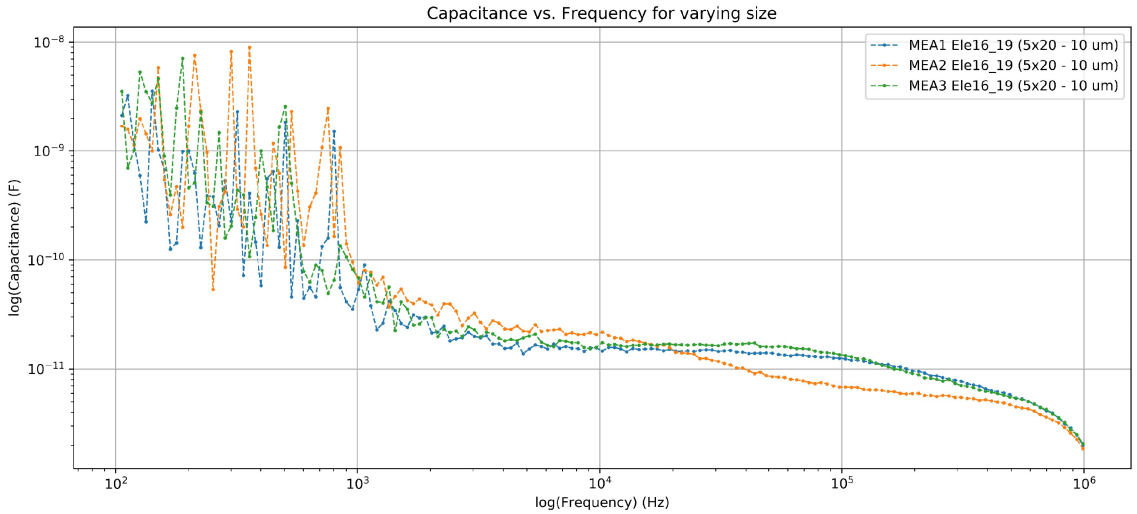



Figure 4.12: Capacitance vs frequency variability over multiple MEAs

### Varying electrode size

One of the aim of this work was to see how different sizes of electrodes perform and impedance of these electrodes was compared to draw conclusions. On observation over various trends of increasing sizes, it has been observed that an increase in the size of electrode leads to a decrease in the impedance value as evident from graphs below. In figure 4.13 the size of electrodes increases as 2x10 $\mu m^2$ , 2x15 $\mu m^2$ and 2x20 $\mu m^2$ for a fixed inter-electrode distance of 18 $\mu$m, and it can be seen at the 1Hz frequency, the electrodes with larger are have less impedance. The capacitance increases on making the electrodes larger in size and certainly more sensitive to capacitive changes. But it is a trade-off to reach the optimal size such that the capacitance is large enough at the same time the electrodes are small enough to capture changes at single cell spatial range.

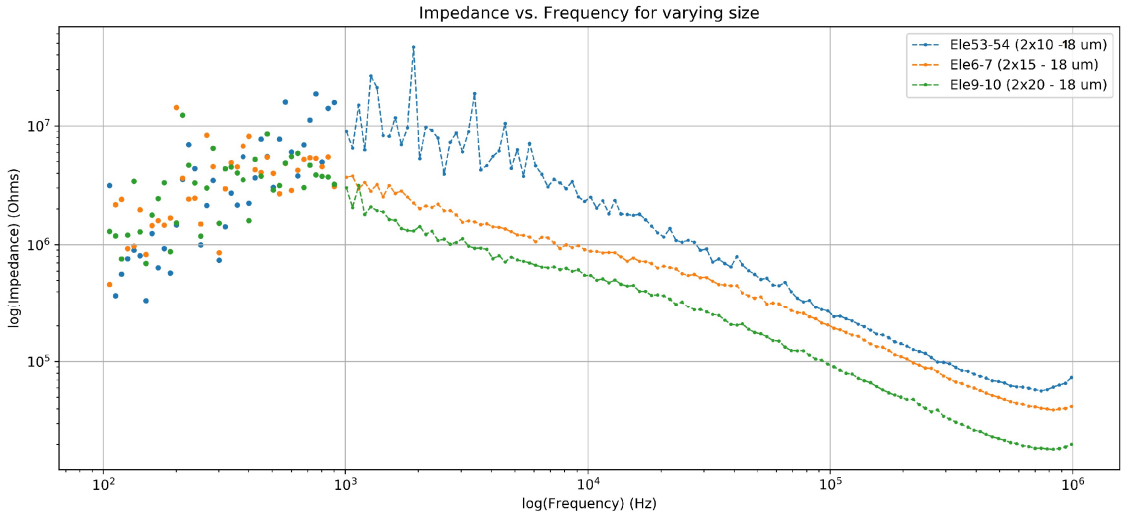



Figure 4.13: Impedance vs frequency for electrodes with increasing size

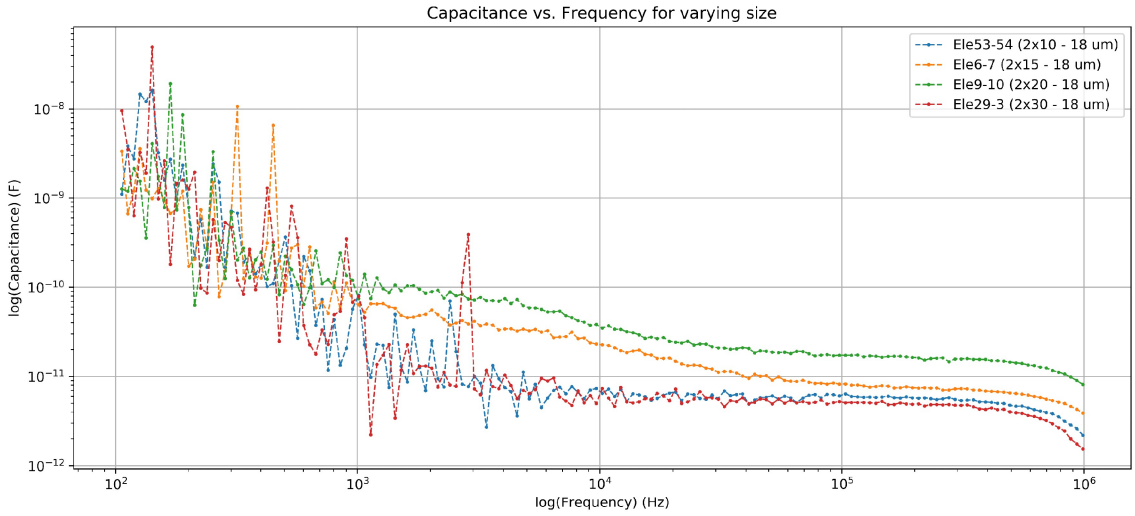



Figure 4.14: Capacitance vs frequency for electrodes with increasing size

A similar trend of increasing sizes but with 5x10 $\mu m^2$ and 10x20 $\mu m^2$ for the fixed distances of 5 and 10 $\mu$m between the electrodes were analyzed. The graphs 4.15 and 4.16 shows that the increasing electrode size decreases impedance.

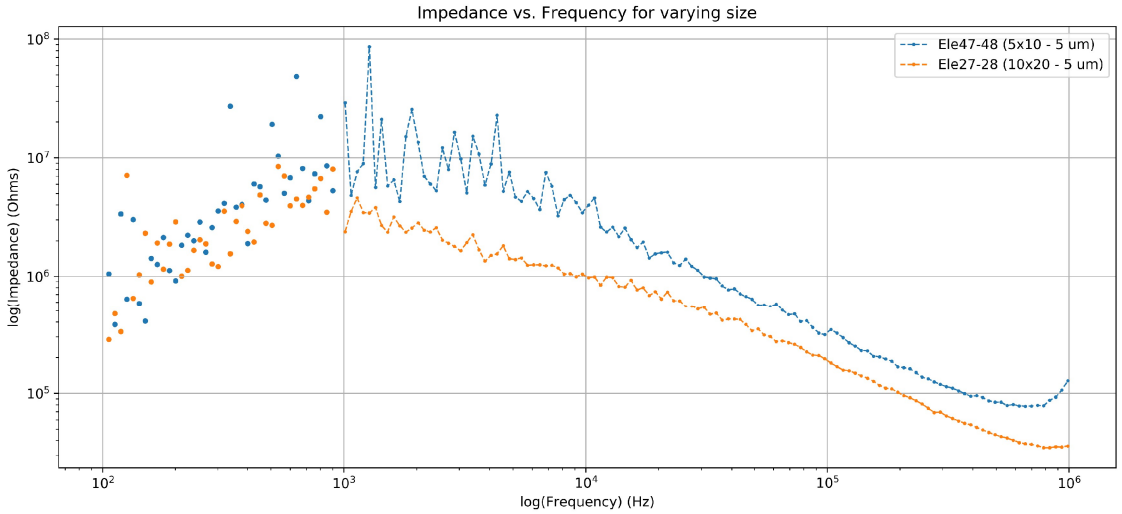



Figure 4.15: Impedance vs frequency for increasing size of electrodes 5x10 $\mu m^2$ and 10x20 $\mu m^2$ at 5 $\mu$m distance

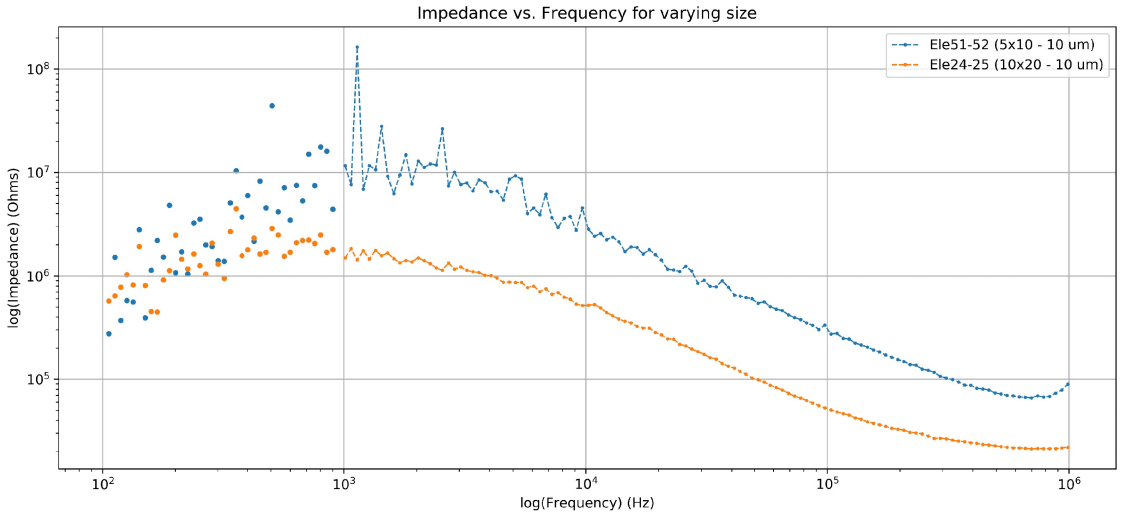



Figure 4.16: Impedance vs frequency for increasing size of electrodes 5x10 $\mu m^2$ and 10x20 $\mu m^2$ at 10 $\mu$m distance

Similarly it has been noticed that capacitance increases with frequency on increasing the size of the electrodes as shown in **??** for electrodes 5x10 $\mu m^2$ and 10x20 $\mu m^2$ which are 5 $\mu$m apart. This holds true because the impedance drops on growing size and given impedance is inversely proportional to capacitance, it increases.

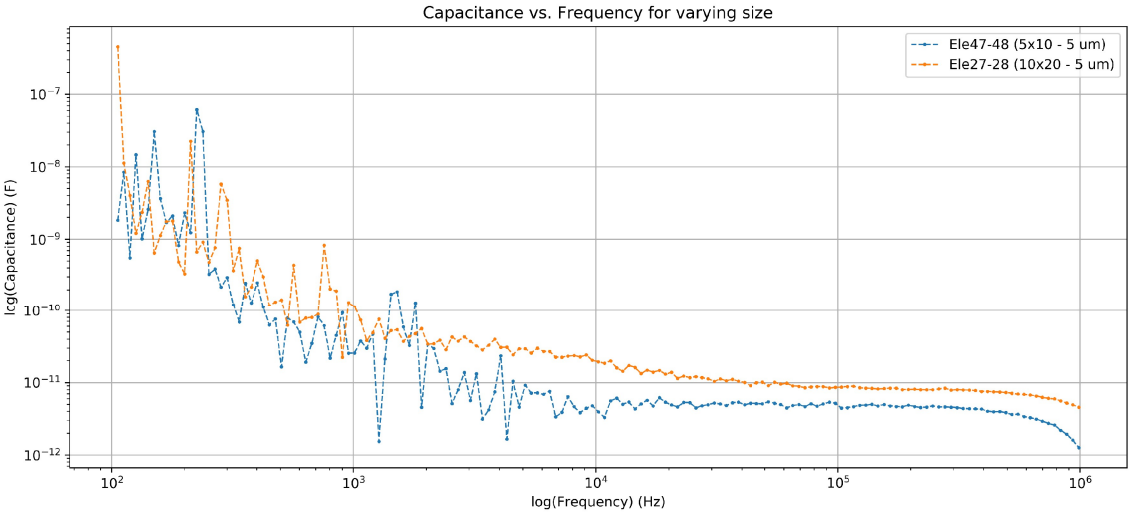



Figure 4.17: Capacitance vs frequency for increasing size of electrodes 5x10 $\mu m^2$ and 10x20 $\mu m^2$ at 5 $\mu$m distance

Certain comparisons of increasing the size of the electrodes seemed to deviate at certain ranges such as in 4.18. Here the increase is 5x10 $\mu m^2$ , 5x15 $\mu m^2$ and 5x20 $\mu m^2$ for a fixed inter-electrode distance of 10 $\mu$m. Again the same inference can be drawn that increasing the size from 5x10 $\mu m^2$ lowers the impedance, but 5x15 $\mu m^2$ or 5x20 $\mu m^2$ are seen to be very close and show opposite behavior for few frequencies. This could be due to any slight changes during the experimentation or other anomalies such as improper coverage of SU-8, etc. It is also interesting to notice that the deviation from 5x10 to 5x15 $\mu m^2$ is much higher than 5x15 to 5x20 $\mu m^2$. This is due to the limiting nature of the electrode size, and for larger electrode sizes the sensitivity in impedance change is reduced.

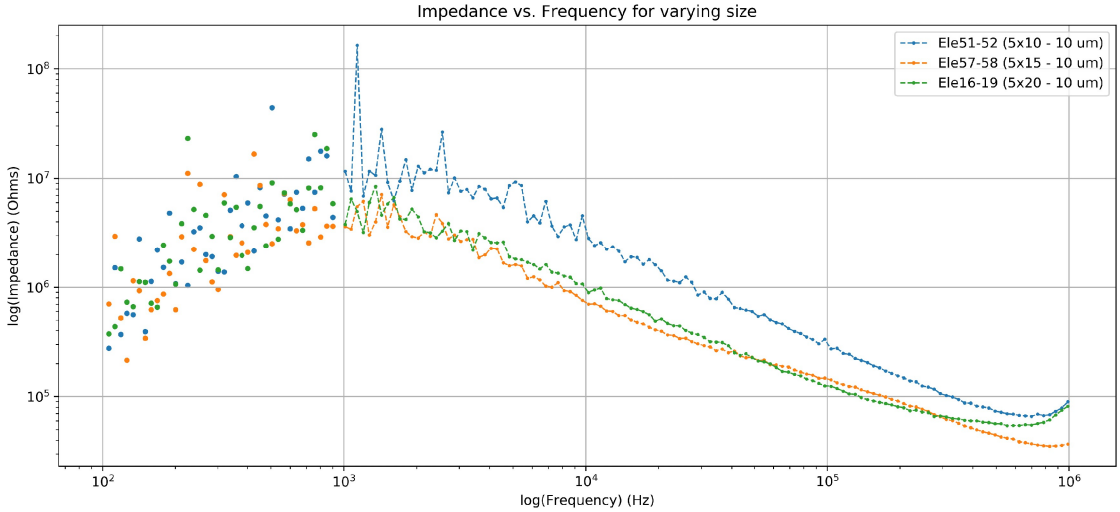



Figure 4.18: Impedance vs frequency for electrodes - 5x10 $\mu m^2$ , 5x15 $\mu m^2$ and 5x20 $\mu m^2$

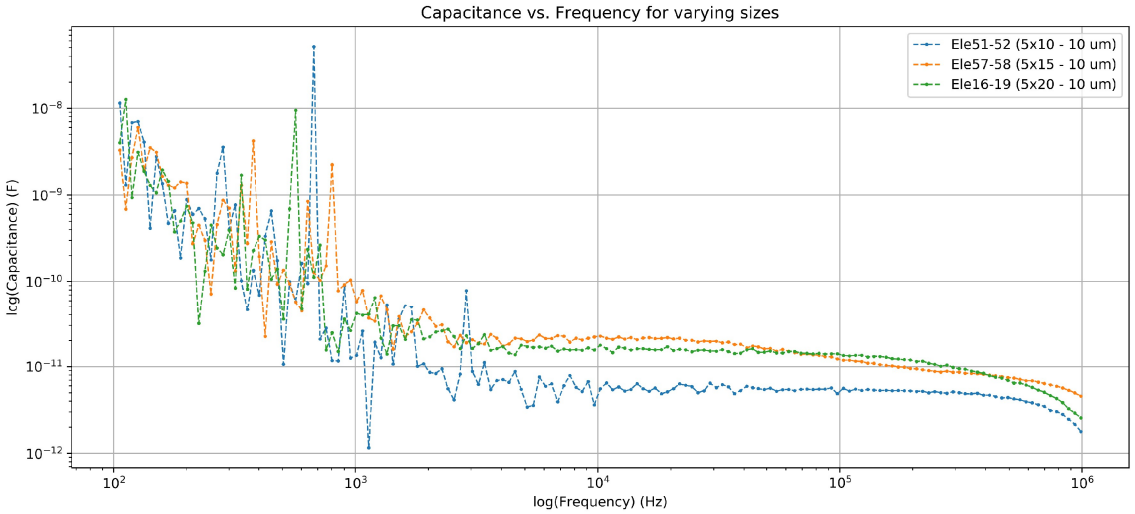



Figure 4.19: Capacitance vs frequency for increasing electrode size

### Varying inter-electrode distance

Next the inter-electrode distance was varied for the same size of electrodes. Again impedance versus frequency plots were obtained to draw conclusions. First the electrodes of size 10x20 $\mu m^2$ with varying distances 10 $\mu$m, 15 $\mu$m and 20 $\mu$m were analyzed. On observation it can be inferred that decreasing the inter-electrode distance causes an drop in the impedance for figure 4.21. This can be justified by the fact that, bringing the electrodes closer has a higher electric field coupling thereby reducing the impedance.

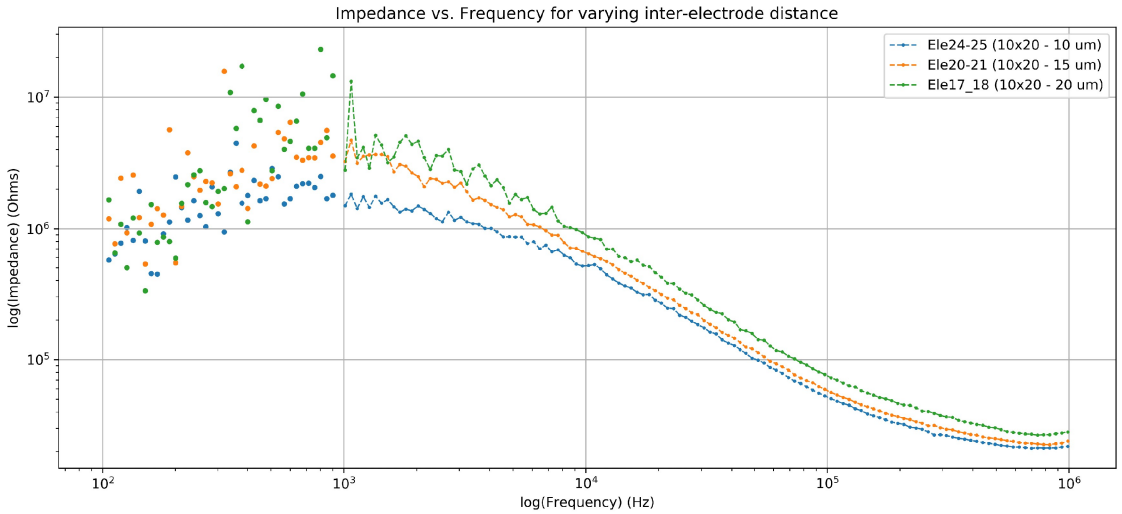



Figure 4.20: Impedance vs frequency for electrodes with 10 $\mu$m, 15 $\mu$m and 20 $\mu$m spacing

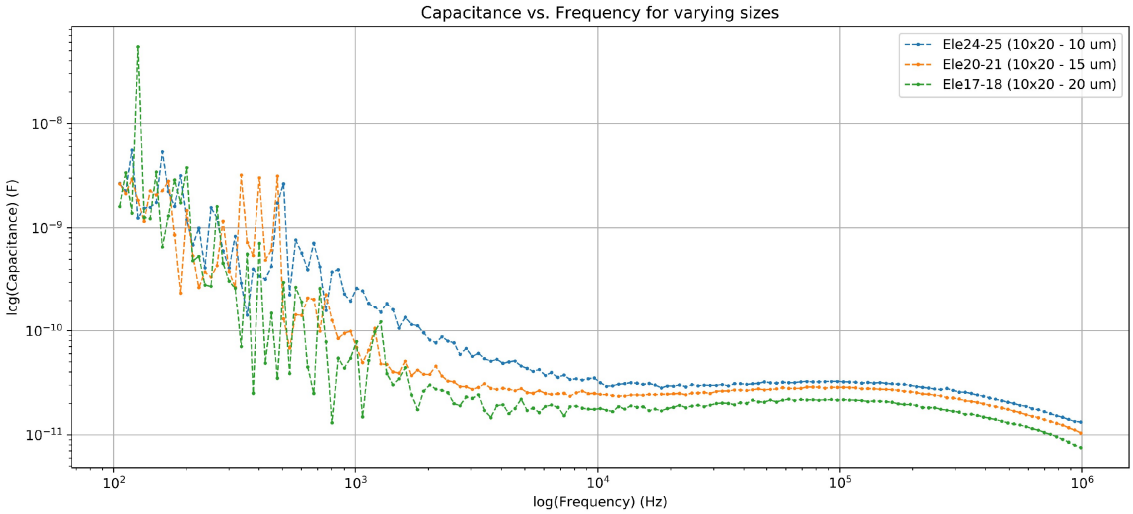



Figure 4.21: Capacitance vs frequency for electrodes with 10 $\mu$m, 15 $\mu$m and 20 $\mu$m spacing

Similar trends were seen on comparing the other electrode sizes with varying sizes - 5x30 $\mu m^2$ and 2x30 $\mu m^2$ with distances varying as 15 $\mu$m/25 $\mu$m and 8 $\mu$m/18 $\mu$m respectively in 4.22 and 4.23. Again just like the variation in size, the inter-electrode distance varied for larger size electrodes causes much lesser variation in the impedance.

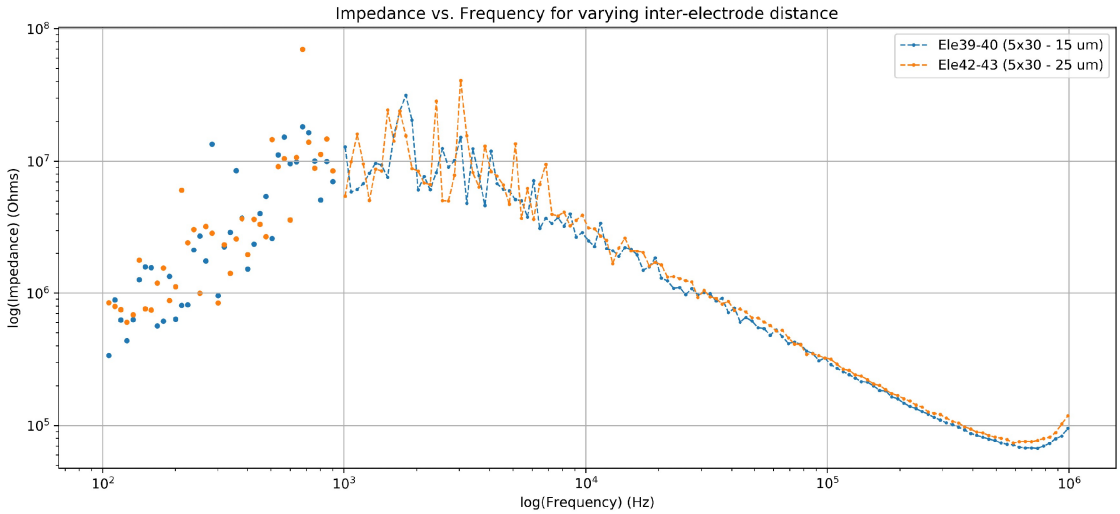



Figure 4.22: Impedance vs frequency for 5x30 $\mu m^2$ electrodes

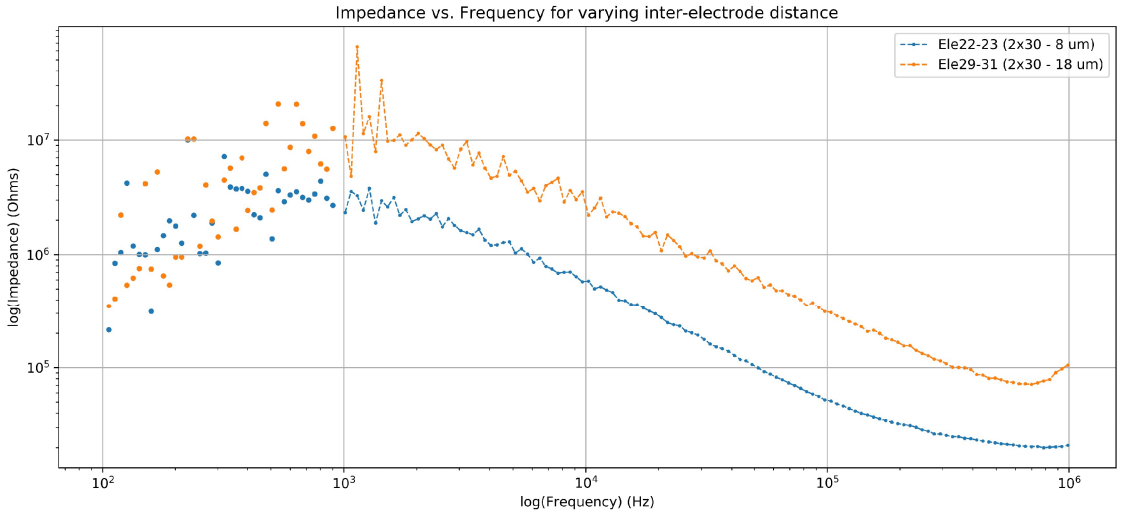



Figure 4.23: Impedance vs frequency for 2x30 $\mu m^2$ electrodes

Certain dissimilarities were observed such as in 5x15 $\mu m^2$ with varying distances 4.24, but the general trend that decreasing distance also drops the impedance was still verified. Again, these disparities can be attributed to inaccuracies in experimentation or the MEA itself. The capacitance plotted in 4.25 also checks out with the fact that bringing the electrodes closer will have a better electrical field coupling thereby giving higher capacitive sensitivity.

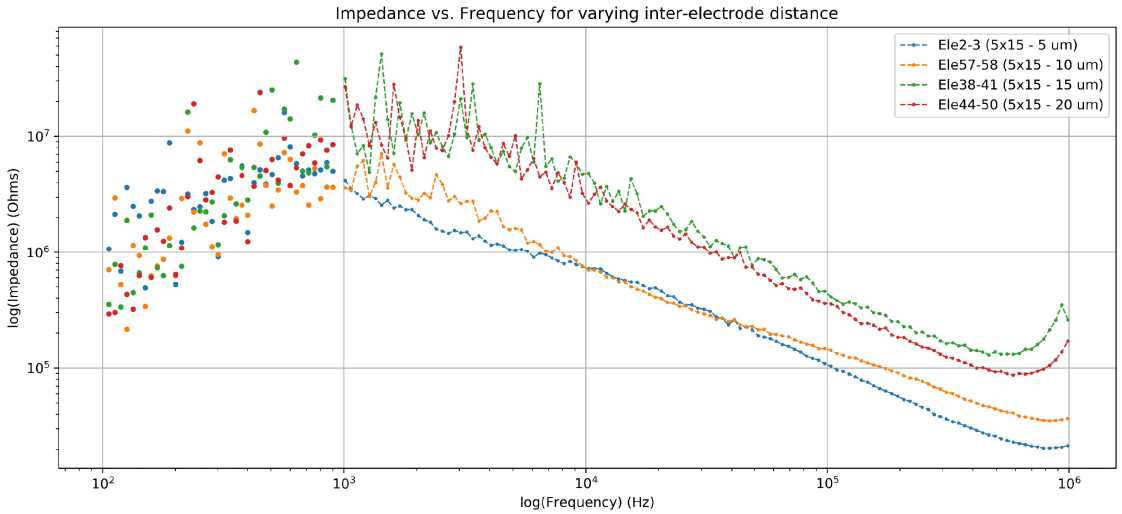



Figure 4.24: Impedance vs frequency for 5x15 $\mu m^2$ electrodes

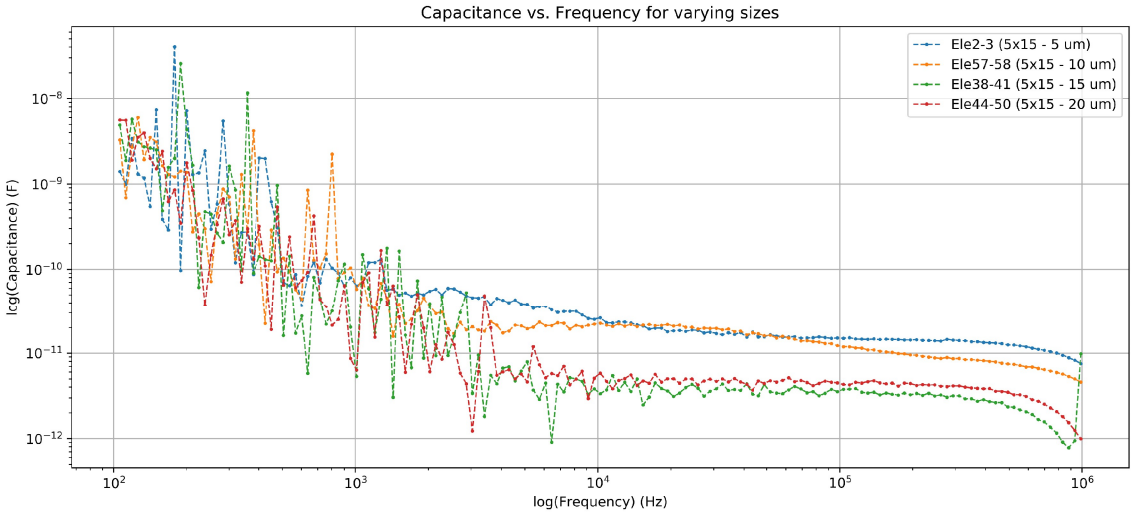



Figure 4.25: Capacitance vs frequency for 2x30 $\mu m^2$ electrodes

Therefore based on both the observations of varying size and varying electrode distance, it can be inferred that having bigger electrodes with less distance between them causes to impedance drop, thereby increasing the capacitance. This is important to get better sensitivity for electrodes which enabling them to pick up even the smallest of the dielectric changes when a cell is placed. One can choose a suitable point between the trade-off of having high capacitance to that of making a large electrode that wouldn't be very useful for more of single cell analysis.

### 4.1.4 Impedance for varying Concentration

Impedance measurements were made with MEA containing varying concentrations of Buffer solution PBS with respect to the frequency. Here 1 $\mu l$ - PBS in the graphs implies 1 $\mu l$ with the rest 999 $\mu l$ milliQ water in MEA. Similarly for the other concentrations, PBS was diluted with milliQ water always totaling to 1 ml of solution to maintain control in the experiment. Impedance versus frequency for varying concentration has been plotted for few electrode pairs as below.

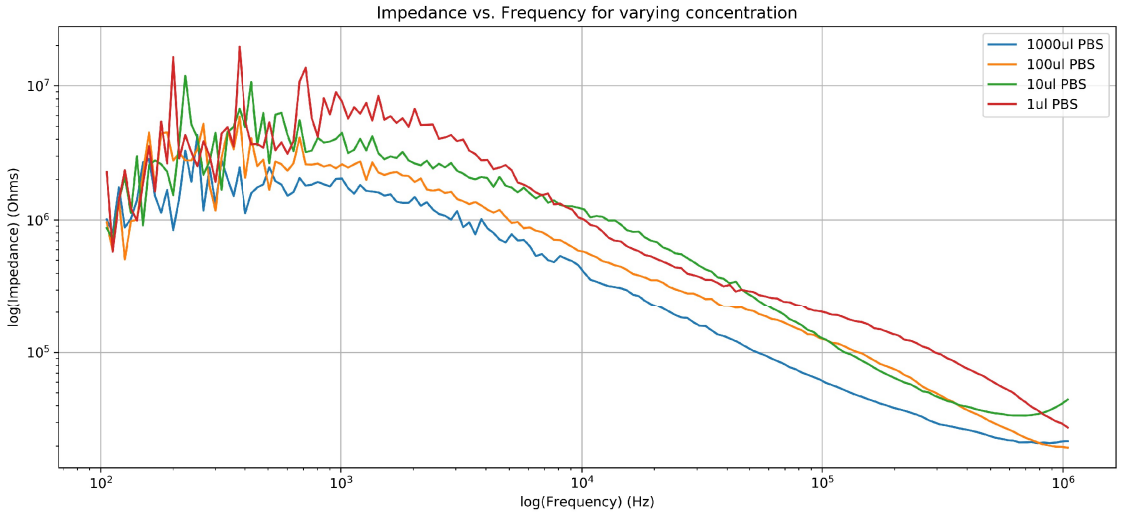



Figure 4.26: Impedance vs frequency for varying concentration of PBS

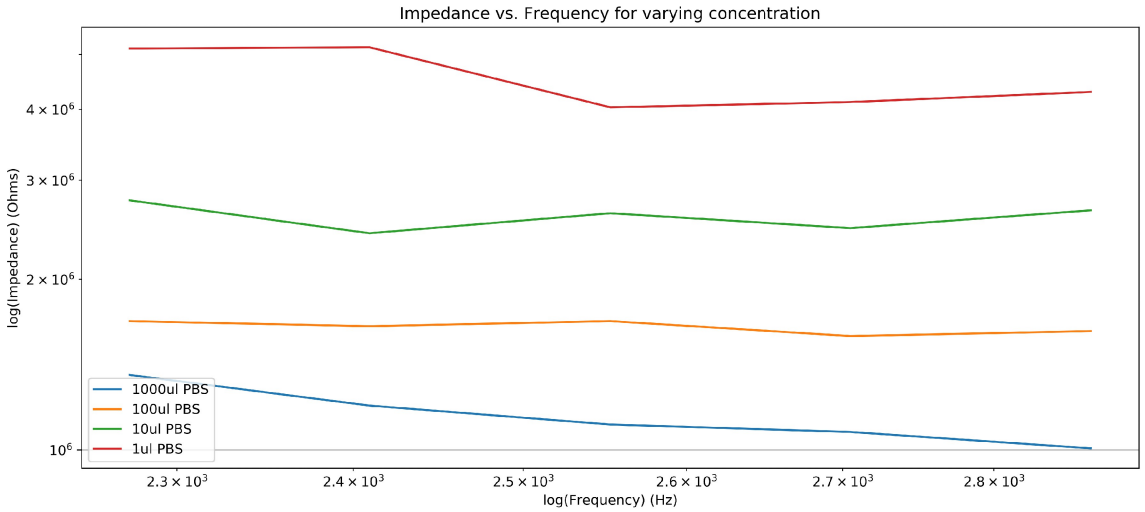



Figure 4.27: Impedance vs frequency for varying concentration of PBS

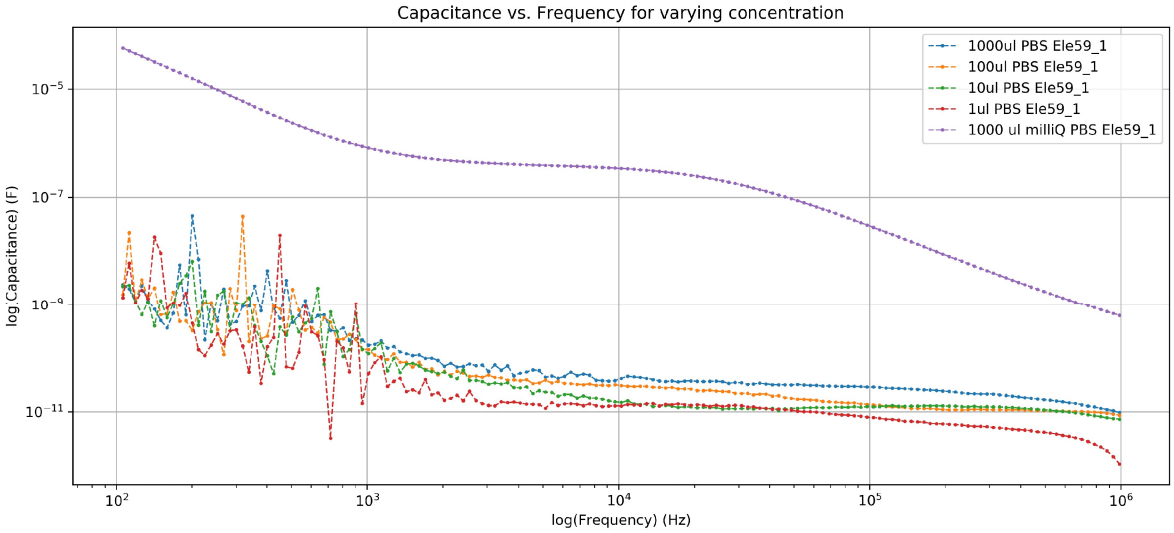



Figure 4.28: Capacitance vs frequency for varying concentration of PBS

From the above graphs it can be understood that increasing the concentration, lowers the impedance value. This is crucial because when neurons fire, the increase in concentration will lower the impedance or increase the capacitance that we intend to measure. Through this it has been demonstrated that concentration changes as small as 1 $\mu l$ can be detected sensitively.

## 4.2 Electrical measurements with cells

This section describes the electrical measurements performed using MEAs with neurons seeded on them. The goal of these experiments was to detect action potentials. That is to observe a change in the impedance when an action potential is fired. To verify that these changes were a result of an action potential, Ca+2 imaging data was used. Keeping in mind the optimal settings as inferred from the results in the above section, slightly higher amplitude and higher frequency ranges close to 100KHz were used to record these action potentials. Time windows of electrical impedance and their corresponding Ca+2 image has been shown for two instances when the neurons are firing and vice-versa. It was seen that the action potentials could be detected as spikes on the impedance data and when no neurons are firing, there are no spikes except for the baseline and noise.

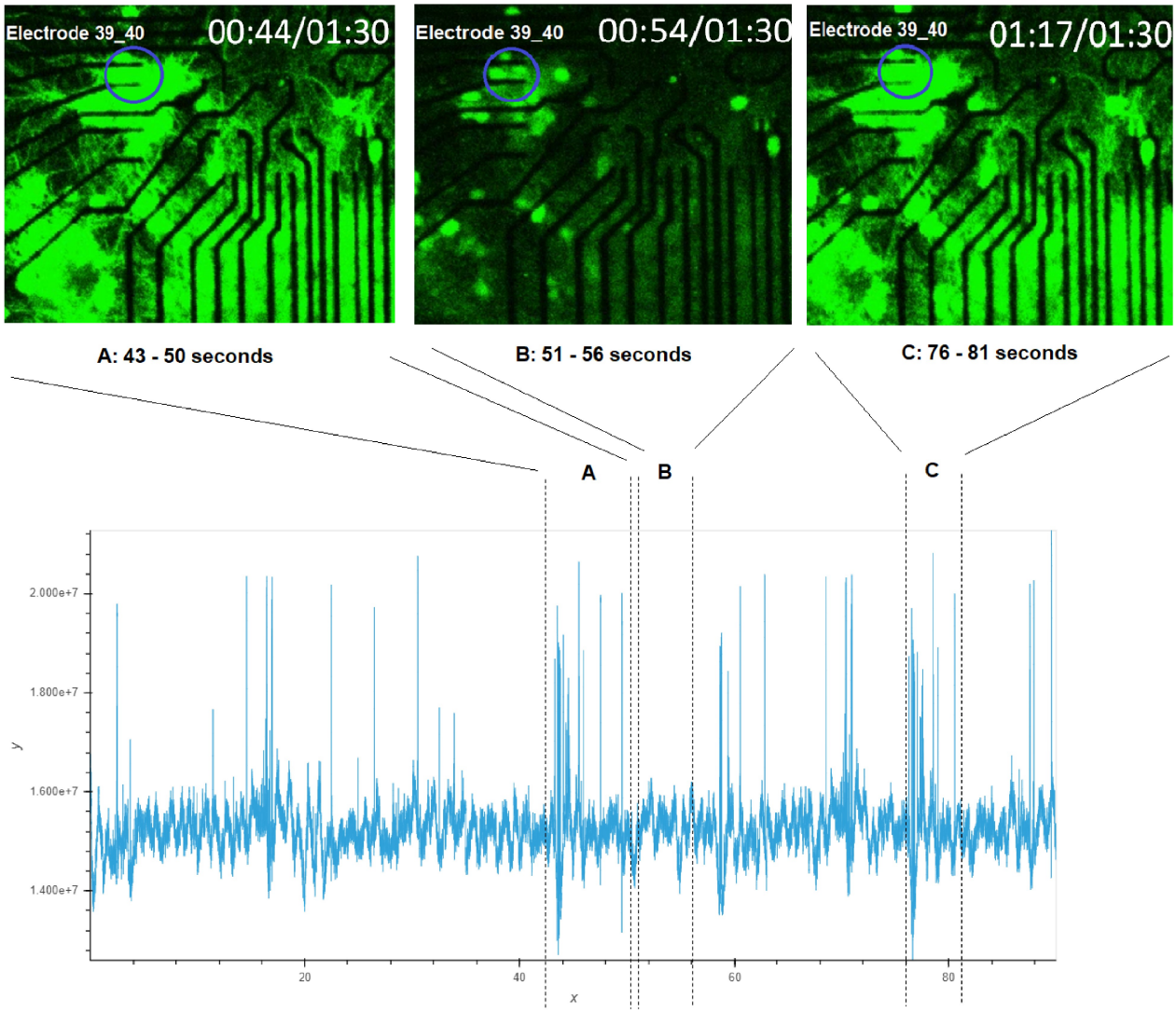



Figure 4.29: Electrical impedance with spikes when firing and no spikes when not firing

Many of these action potentials were zoomed into and analyzed to obtain the shape of the action potential spike and validate the resemblance with a true action potential. Another example of the recorded action potentials was listed in appendix 4.

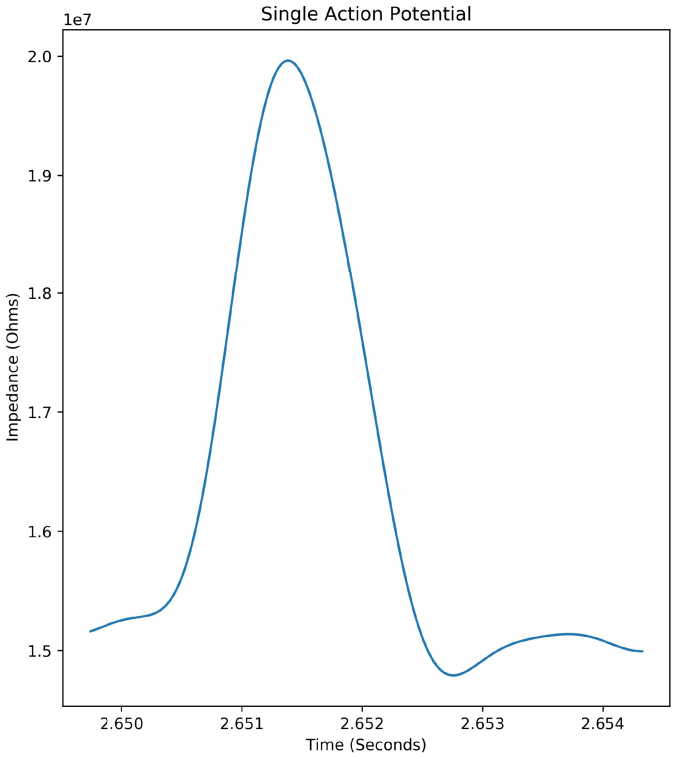



Figure 4.30: Zoomed in single action potential

## 4.3 Conclusions

From this chapter it can be concluded all electrical measurements pertaining to all electrodes were obtained and analyzed. Repeatability and variability has also been accounted in these measurements. As for the inferences from the results, it can be observed that having bigger electrodes with less distance between them causes to impedance drop, thereby increasing the capacitance. This is important to get better sensitivity for electrodes which enabling them to pick up even the smallest of the dielectric changes when a cell is placed. One can choose a suitable point between the trade-off of having high capacitance to that of making a large electrode that wouldn't be very useful for more of single cell analysis. Additionally, very small concentration changes were detected successfully which can help pick up the minutest of the changes from the cell. Finally action potentials from the cells were measured and noted thereby proving that the capacitive MEAs are an effective way to acquire neuronal activity.

# Chapter 5

# Conclusions and Outlook

The main aim of this thesis was to design, fabricate and interface MEAs, to seed neurons and record action potentials from them using the new sensing technique. This goal was successfully accomplished and a complete modular setup has been established that can simultaneous perform recording and stimulation from neurons.

**Contributions:**

Several modalities such as the electrode planar geometry were explored in detail to enhance the signal quality. Impedance characterization of all the electrodes both empty and along with an electrolytic solution has been successfully performed.

An overview of the sub-tasks solved in order to achieve the main goal are given in the following list:

1. **Design and fabrication of MEAs:**
   To understand how the electrode size or the inter-electrode distance will have an effect on the signal quality. Trends of these parameters were varied and the design choices were made based on the sizes comparable to that of a neuron. This was backed up the background theory and working pricinples. Once designed, these MEAs were fabricated and improved to achieve MEAs of good quality for experimentation.

2. **Electronic interface and measurement setup:**
   To interface this MEA to the measurement setup, a customized PCB was designed and fabricated to allow flexible recording/stimulation scenarios. Further, the bench-top setup such as the lock-in amplifier and its working was understood to integrate it with the MEA and the PCB. Using this setup successful characterization of MEAs was performed by measuring the impedance of all the electrodes.

3. **Neuronal cell cultures and imaging:**
   Cell culturing was carried out to seed neurons on the MEAs. Protocols to do perform the seeding of neurons and to work with them were learnt. Principles of operation of a CLSM was understood and Ca+2 imaging was performed in conjunction with electrical measurements.

4. **Data processing:**
   Finally the acquired electrical measurements were processed and the resulting graphs were plotted. Based on the data, interpretations were made to answer the questions posed in this thesis.

Finally it can be concluded that new capacitve sensing paradigm works. With the help of impedance characterization data, the optimal way to proceed is to increase the size of electrodes for lower impedance but still keep them small enough to access single neurons or just a few of them. Furthermore based on the concentration experiments, we conclude that capacitance changes were observed for very small concentration changes. Both of these goals were achieved and are in accordance with the ideal scenario. Action potentials were detected using this sensing scheme and have resulted to be

correct based on the verification from the imaging data. Therefore to conclude, the proof of concept of capacitive MEAs has been implemented and is shown to be quite effective.

**Recommendations:**

1. As an outlook, it would be very interesting to see the in-detailed characteristics of these action potentials.
2. To do a comparative study between the spikes detected by this method to that of the traditional sensing method.
3. It would also be interesting to further explore many more shapes of these microelectrodes to further enhance the signal quality.
4. Even a comparitive study between commercial and capacitive MEAs from this work would be interesting to observe.

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# Appendix

## Appendix: 1

Optimization of dosage for proper pattern transfer for the smaller feature sizes such as electrodes. The power of the UV lamp was fixed at 7.46 mW/$cm^2$, based on which the exposure time was calculated and used. Exposure time = (exposure dosage/power of the UV lamp):

| **Dosage (mJ/cm2** | **Observation** |
|---|---|
| 550 (listed in datasheet) | No patterns were transferred (due to overexposure) |
| 400 | No visible patterns due to overexposure |
| 250 | Faint patterns observed but without resolution |
| 100 | Patterns clearly visible but not with resolution |
| 55 | Clean transfer of patterns noticed |
| 20 | Patterns transferred but exposure not sufficient |

Based on the study, it was understood that the 55mJ was the perfect dosage to obtain good feature clarity. Some of the images taken during the study can be seen as below.

Figure 5.1: No patterns visible for 550 mJ dose

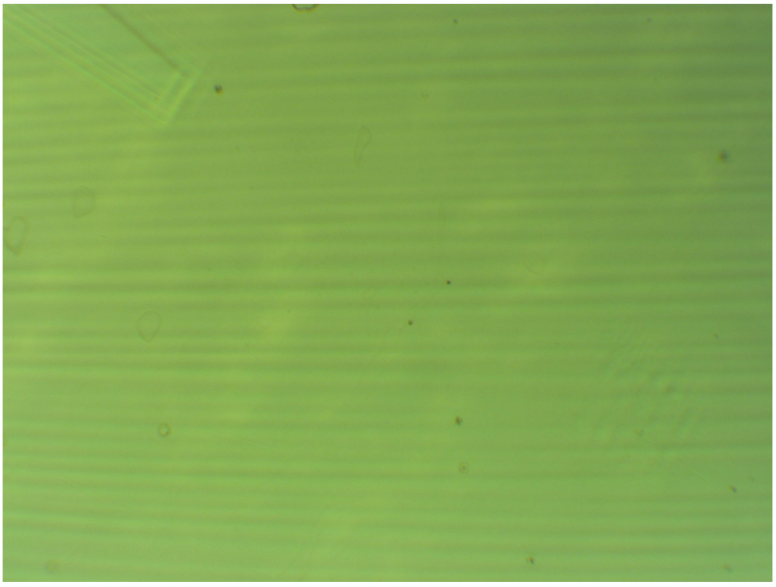


Figure 5.2: Very faint patterns for a dosage of 250 mJ

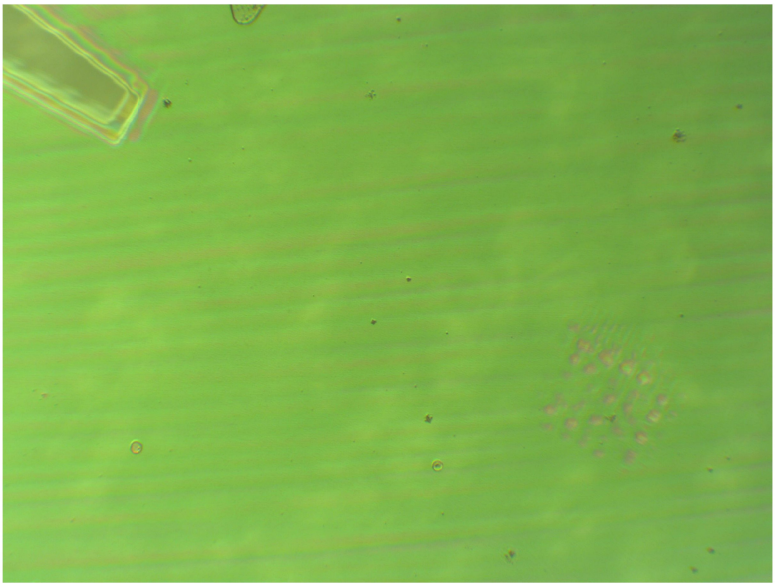


Figure 5.3: Patterns for 100 mJ dose - have very poor resolution

# Appendix: 2

**Protocol for Neuron Dissociation**
**To make PBG:**
Total = 50 mL

1. Dissolve 50 mg of BSA in 50 mL sterile PBS.
2. Add 90.08 mg (per 50 mL) of glucose.
3. Store in cell culture room 4 degree celsius fridge.

**To make PBG-papain-DNase solution:**
Total = 5 mL

1. Take 5 mL of PBG from the stock.

2. Add 2.5 mg of papain (stored in -20 C freezer). Make sure to wash the spatula at microbalance before and after use with ethanol-water-MilliQ water.

3. Vortex briefly then put in 37 C bath until papain is full dissolved (est time 30 mins).

4. Filter with 0.2 um sterile filters into a new tube.

5. Add DNase only after filtering. Add 5 uL of Dnase. Pipet up and down to mix.

**To dissociate hippocampul/cortical neurons:**

1. Remove PBG already in tube (usually 10 mL) carefully without disturbing the brain tissue at the bottom.

2. Add 5mL of PBG-papain-DNase solution prepared.

3. Shake gently and out in the 37 C incubator for 15 minutes.

4. Remove PBG solution without disturbing the pellet.

5. Gently add 5 mL of Neurobasal media (NB and let it sit for atleast 3 minutes.

6. Remove the media without disturbing pellet and perform the above step thrice.

7. Add 2 mL of Neurobasal media and pipette up and down for a minute with a 1000 uL pipette to break the cell clump.

8. Prepare eppendorf container with 90 uL of media. After mixing the cells, add 10 uL of the cell solution into the 90 uL of media.

9. Pipetter to mix. Remove 10 uL from this and put it into a second eppendorf container (to dilute the cells for counting 1:10). If there are not many cells, do not dilute.

10. Take this 10 uL to the cell counter and add 10 uL of Trypan Blue. Add 10 uL of this solution to each side of the cell counter slide and count cells. Make sure to factor the dilution back into it.

# Appendix: 3

Data containing the current, voltage components and frequencies are saved as .txt files as shown below.

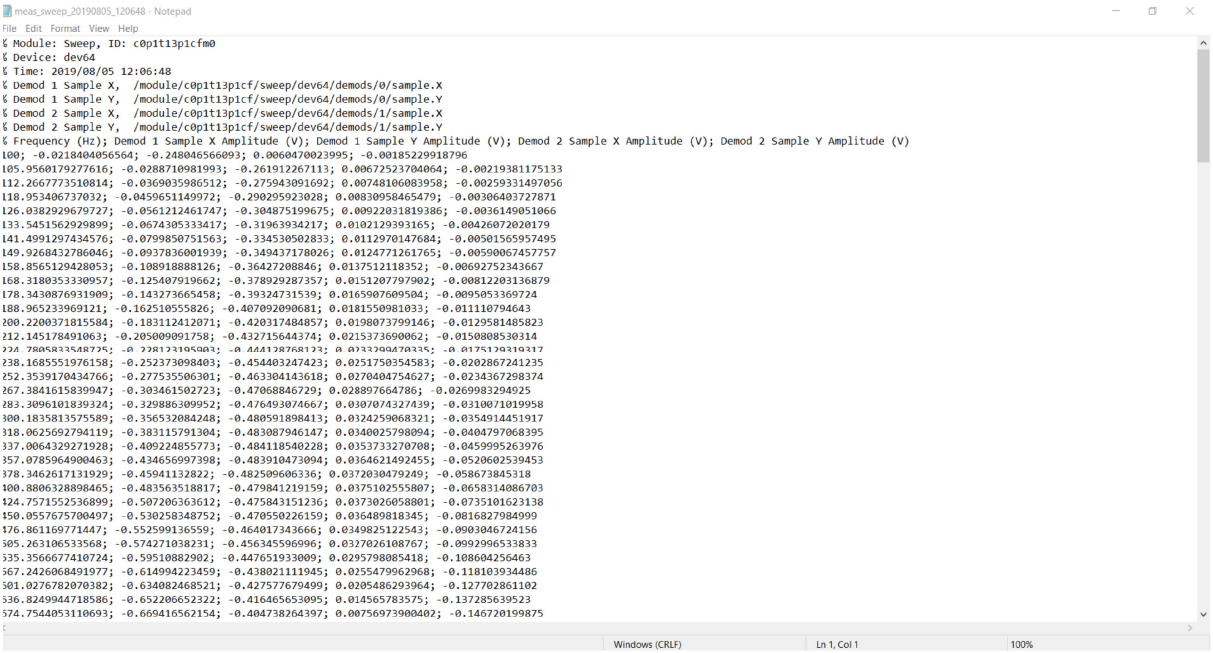



Figure 5.4: Saved text file with current and voltage information

# Appendix: 4

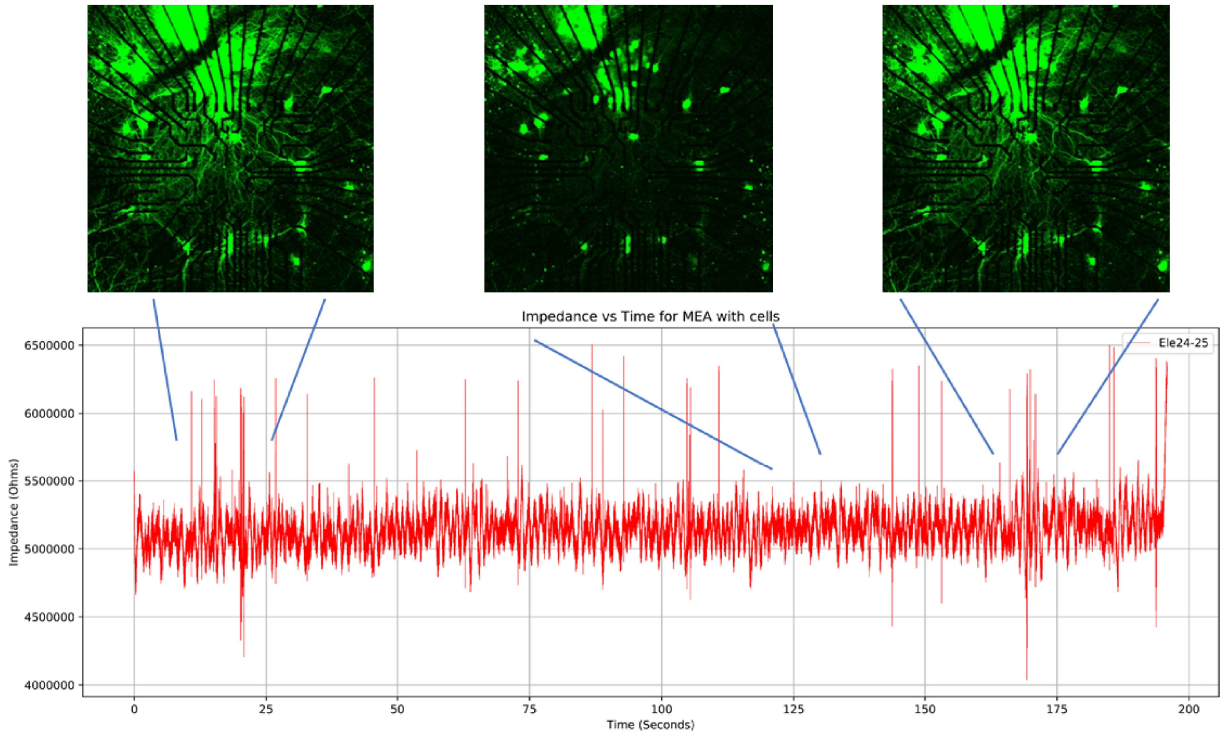



Figure 5.5: Action potential from a different MEA culture

# Appendix: 5

# 16-/32-Channel, Serially Controlled 4 Ω 1.8 V to 5.5 V, ±2.5 V, Analog Multiplexers

## ADG725/ADG731

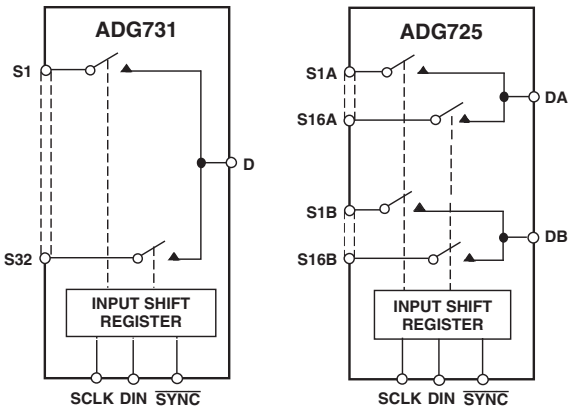
### FEATURES

- 3-Wire SPI Compatible Serial Interface
- 1.8 V to 5.5 V Single Supply
- ±2.5 V Dual-Supply Operation
- 4 Ω On Resistance
- 0.5 Ω On Resistance Flatness
- 7 mm x 7 mm 48-Lead Chip Scale Package (LFCSP) or 48-Lead TQFP Package
- Rail-to-Rail Operation
- Power-On Reset
- 42 ns Switching Times
- Single 32-to-1 Channel Multiplexer
- Dual/Differential 16-to-1 Channel Multiplexer
- TTL/CMOS Compatible Inputs
- For Functionally Equivalent Devices with Parallel Interface, See ADG726/ADG732

### APPLICATIONS

- Optical Applications
- Data Acquisition Systems
- Communication Systems
- Relay Replacement
- Audio and Video Switching
- Battery-Powered Systems
- Medical Instrumentation
- Automatic Test Equipment

### FUNCTIONAL BLOCK DIAGRAM




### GENERAL DESCRIPTION

The ADG731/ADG725 are monolithic, CMOS, 32-channel/dual 16-channel analog multiplexers with a serially controlled 3-wire interface. The ADG731 switches one of 32 inputs (S1–S32) to a common output, D. The ADG725 can be configured as a dual mux switching one of 16 inputs to one output, or a differential mux switching one of 16 inputs to a differential output.

These mulitplexers utilize a 3-wire serial interface that is compatible with SPI®, QSPI™, MICROWIRE™, and some DSP interface standards. On power-up, the Internal Shift Register contains all zeros and all switches are in the OFF state.

These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed with very low on resistance and leakage currents. They operate from a single supply of 1.8 V to 5.5 V or a ±2.5 V dual supply, making them ideally suited to a variety of applications. On resistance is in the region of a few ohms, is closely matched between switches, and is very flat over the full signal range.

These parts can operate equally well as either multiplexers or demultiplexers and have an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

The ADG731 and ADG725 are serially controlled 32-channel, and dual/differential 16-channel multiplexers, respectively. They are available in either a 48-lead LFCSP or TQFP package.

### PRODUCT HIGHLIGHTS

1. 3-Wire Serial Interface.
2. 1.8 V to 5.5 V Single-Supply or ±2.5 V Dual-Supply Operation. These parts are specified and guaranteed with 5 V ±10%, 3 V ±10% single-supply, and ±2.5 V ±10% dual-supply rails.
3. On Resistance of 4 Ω.
4. Guaranteed Break-Before-Make Switching Action.
5. 7 mm × 7 mm 48-Lead Chip Scale Package (LFCSP) or 48-Lead TQFP Package.

Rev. B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Technical Support www.analog.com

# ADG725/ADG731–SPECIFICATIONS[1] ($V_{DD}$ = 5 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V, unless otherwise noted.)

| Parameter | B Version +25°C | B Version –40°C to +85°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 4 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_{DS}$ = 10 mA; |
| | 5.5 | 6 | Ω max | Test Circuit 1 |
| On Resistance Match between | | 0.3 | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_{DS}$ = 10 mA |
| Channels ($\Delta R_{ON}$) | | 0.8 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.5 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_{DS}$ = 10 mA |
| | | 1 | Ω max | |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = 5.5 V |
| Source OFF Leakage $I_S$ (OFF) | ±0.01 | | nA typ | $V_D$ = 4.5 V/1 V, $V_S$ = 1 V/4.5 V; |
| | ±0.25 | ±1 | nA max | Test Circuit 2 |
| Drain OFF Leakage $I_D$ (OFF) | ±0.05 | | nA typ | $V_D$ = 4.5 V/1 V, $V_S$ = 1 V/4.5 V; |
| ADG725 | ±0.5 | ±2.5 | nA max | Test Circuit 3 |
| ADG731 | ±1 | ±5 | nA max | |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.05 | | nA typ | $V_D$ = $V_S$ = 1 V or 4.5 V; |
| ADG725 | ±0.5 | ±2.5 | nA max | Test Circuit 4 |
| ADG731 | ±1 | ±5 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.8 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | ±0.5 | μA max | |
| $C_{IN}$, Digital Input Capacitance | 5 | | pF typ | |
| DYNAMIC CHARACTERISTICS[2] | | | | |
| $t_{TRANSITION}$ | 42 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; Test Circuit 5 |
| | 53 | 62 | ns max | $V_{S1}$ = 3 V/0 V, $V_{S32}$ = 0 V/3 V |
| Break-Before-Make Time Delay, $t_D$ | 30 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | | 1 | ns min | $V_S$ = 3 V; Test Circuit 6 |
| Charge Injection | 5 | | pC typ | $V_S$ = 2.5 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; Test Circuit 7 |
| Off Isolation | –72 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Test Circuit 8 |
| Channel-to-Channel Crosstalk | –72 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Test Circuit 9 |
| –3 dB Bandwidth | | | | |
| ADG725 | 34 | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Test Circuit 10 |
| ADG731 | 18 | | MHz typ | |
| $C_S$ (OFF) | 15 | | pF typ | f = 1 MHz |
| $C_D$ (OFF) | | | | |
| ADG725 | 170 | | pF typ | f = 1 MHz |
| ADG731 | 340 | | pF typ | f = 1 MHz |
| $C_D$, $C_S$ (ON) | | | | |
| ADG725 | 175 | | pF typ | f = 1 MHz |
| ADG731 | 350 | | pF typ | f = 1 MHz |
| POWER REQUIREMENTS | | | | $V_{DD}$ = 5.5 V |
| $I_{DD}$ | 10 | | μA typ | Digital Inputs = 0 V or 5.5 V |
| | | 20 | μA max | |

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# SPECIFICATIONS[1] ($V_{DD}$ = 3 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V, unless otherwise noted.)

| Parameter | B Version +25°C | B Version –40°C to +85°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 7 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_{DS}$ = 10 mA; |
| | 11 | 12 | Ω max | Test Circuit 1 |
| On Resistance Match between | | 0.35 | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_{DS}$ = 10 mA |
| Channels ($\Delta R_{ON}$) | | 1 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | | 3 | Ω max | $V_S$ = 0 V to $V_{DD}$, $I_{DS}$ = 10 mA |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = 3.3 V |
| Source OFF Leakage $I_S$ (OFF) | ±0.01 | | nA typ | $V_S$ = 3 V/1 V, $V_D$ = 1 V/3 V; |
| | ±0.25 | ±1 | nA max | Test Circuit 2 |
| Drain OFF Leakage $I_D$ (OFF) | ±0.05 | | nA typ | $V_S$ = 1 V/3 V, $V_D$ = 3 V/1 V; |
| ADG725 | ±0.5 | ±2.5 | nA max | Test Circuit 3 |
| ADG731 | ±1 | ±5 | nA max | |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.05 | | nA typ | $V_S$ = $V_D$ = 1 V or 3 V; |
| ADG725 | ±0.5 | ±2.5 | nA max | Test Circuit 4 |
| ADG731 | ±1 | ±5 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | | 2.0 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.7 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | ±0.5 | μA max | |
| $C_{IN}$, Digital Input Capacitance | 5 | | pF typ | |
| DYNAMIC CHARACTERISTICS[2] | | | | |
| $t_{TRANSITION}$ | 60 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; Test Circuit 5 |
| | 80 | 90 | ns max | $V_{S1}$ = 2 V/0 V, $V_{S32}$ = 0 V/2 V |
| Break-Before-Make Time Delay, $t_D$ | 30 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | | 1 | ns min | $V_S$ = 2 V; Test Circuit 6 |
| Charge Injection | 1 | | pC typ | $V_S$ = 0 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; Test Circuit 7 |
| Off Isolation | –72 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Test Circuit 8 |
| Channel-to-Channel Crosstalk | –72 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Test Circuit 9 |
| –3 dB Bandwidth | | | | |
| ADG725 | 34 | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Test Circuit 10 |
| ADG731 | 18 | | MHz typ | |
| $C_S$ (OFF) | 15 | | pF typ | f = 1 MHz |
| $C_D$ (OFF) | | | | |
| ADG725 | 170 | | pF typ | f = 1 MHz |
| ADG731 | 340 | | pF typ | f = 1 MHz |
| $C_D$, $C_S$ (ON) | | | | |
| ADG725 | 175 | | pF typ | f = 1 MHz |
| ADG731 | 350 | | pF typ | f = 1 MHz |
| POWER REQUIREMENTS | | | | $V_{DD}$ = 3.3 V |
| $I_{DD}$ | 5 | | μA typ | Digital Inputs = 0 V or 3.3 V |
| | | 10 | μA max | |

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

# DUAL-SUPPLY SPECIFICATIONS[1] ($V_{DD}$ = +2.5 V ± 10%, $V_{SS}$ = –2.5 V ± 10%, GND = 0 V, unless otherwise noted.)

| Parameter | B Version +25°C | B Version –40°C to +85°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | $V_{SS}$ to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 4 | | Ω typ | $V_S$ = $V_{SS}$ to $V_{DD}$, $I_{DS}$ = 10 mA; |
| | 5.5 | 6 | Ω max | Test Circuit 1 |
| On Resistance Match Between | | 0.3 | Ω typ | $V_S$ = $V_{SS}$ to $V_{DD}$, $I_{DS}$ = 10 mA |
| Channels ($\Delta R_{ON}$) | | 0.8 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.5 | | Ω typ | $V_S$ = $V_{SS}$ to $V_{DD}$, $I_{DS}$ = 10 mA |
| | | 1 | Ω max | |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = +2.75 V, $V_{SS}$ = –2.75 V |
| Source OFF Leakage $I_S$ (OFF) | ±0.01 | | nA typ | $V_S$ = +2.25 V/–1.25 V, $V_D$ = –1.25 V/+2.25 V; |
| | ±0.25 | ±0.5 | nA max | Test Circuit 2 |
| Drain OFF Leakage $I_D$ (OFF) | ±0.05 | | nA typ | $V_S$ = +2.25 V/–1.25 V, $V_D$ = –1.25 V/+2.25 V; |
| ADG725 | ±0.5 | ±2.5 | nA max | Test Circuit 3 |
| ADG731 | ±1 | ±5 | nA max | |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.01 | | nA typ | $V_S$ = $V_D$ = +2.25 V/–1.25 V; Test Circuit 4 |
| ADG725 | ±0.5 | ±2.5 | nA max | |
| ADG731 | ±1 | ±5 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | | 1.7 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.7 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | ±0.5 | μA max | |
| $C_{IN}$, Digital Input Capacitance | 5 | | pF typ | |
| DYNAMIC CHARACTERISTICS[2] | | | | |
| $t_{TRANSITION}$ | 55 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; Test Circuit 5 |
| | 75 | 84 | ns max | $V_{S1}$ = 1.5 V/0 V, $V_{S32}$ = 0 V/1.5 V |
| Break-Before-Make Time Delay, $t_D$ | 15 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | | 1 | ns min | $V_S$ = 1.5 V; Test Circuit 6 |
| Charge Injection | 1 | | pC typ | $V_S$ = 0 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; Test Circuit 7 |
| Off Isolation | –72 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Test Circuit 8 |
| Channel-to-Channel Crosstalk | –72 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Test Circuit 9 |
| –3 dB Bandwidth | | | | |
| ADG725 | 34 | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Test Circuit 10 |
| ADG731 | 18 | | MHz typ | |
| $C_S$ (OFF) | 13 | | pF typ | |
| $C_D$ (OFF) | | | | |
| ADG725 | 130 | | pF typ | f = 1 MHz |
| ADG731 | 260 | | pF typ | f = 1 MHz |
| $C_D$, $C_S$ (ON) | | | | |
| ADG725 | 150 | | pF typ | f = 1 MHz |
| ADG731 | 300 | | pF typ | f = 1 MHz |
| POWER REQUIREMENTS | | | | $V_{DD}$ = +2.75 V |
| $I_{DD}$ | 10 | | μA typ | Digital Inputs = 0 V or 2.75 V |
| | | 20 | μA max | |
| $I_{SS}$ | 10 | | μA typ | $V_{SS}$ = –2.75 V |
| | | 20 | μA max | Digital Inputs = 0 V or 2.75 V |

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

# TIMING CHARACTERISTICS[1, 2]

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Conditions/Comments |
|---|---|---|---|
| $f_{SCLK}$ | 30 | MHz max | SCLK Cycle Frequency |
| $t_1$ | 33 | ns min | SCLK Cycle Time |
| $t_2$ | 13 | ns min | SCLK High Time |
| $t_3$ | 13 | ns min | SCLK Low Time |
| $t_4$ | 13 | ns min | $\overline{SYNC}$ to SCLK Falling Edge Setup Time |
| $t_5$ | 40 | ns min | Minimum $\overline{SYNC}$ Low Time |
| $t_6$ | 5 | ns min | Data Setup Time |
| $t_7$ | 4.5 | ns min | Data Hold Time |
| $t_8$ | 33 | ns min | Minimum $\overline{SYNC}$ High Time |

NOTES
[1]See Figure 1.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of $V_{DD}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
Specifications subject to change without notice.

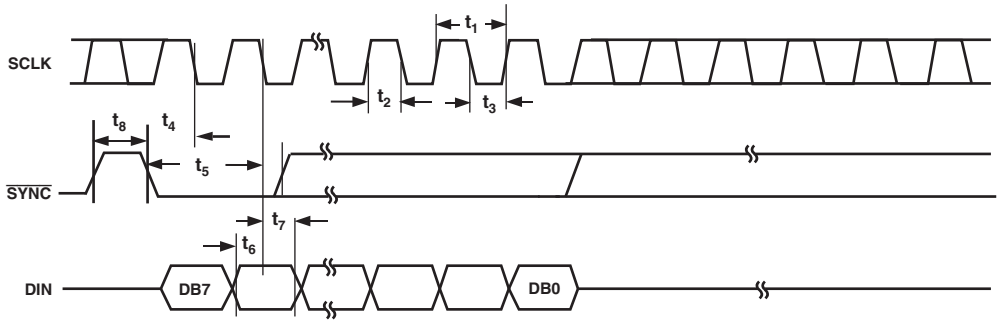



*Figure 1. 3-Wire Serial Interface Timing Diagram*

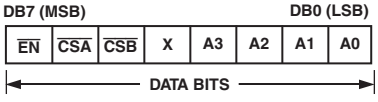



*Figure 2. ADG725 Input Shift Register Contents*

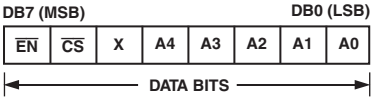



*Figure 3. ADG731 Input Shift Register Contents*

**ABSOLUTE MAXIMUM RATINGS**[1]

($T_A$ = 25°C, unless otherwise noted.)

$V_{DD}$ to $V_{SS}$ . . . . . 7 V
$V_{DD}$ to GND . . . . . –0.3 V to +7 V
$V_{SS}$ to GND . . . . . +0.3 V to –7 V
Analog Inputs[2] . . . . . $V_{SS}$ – 0.3 V to $V_{DD}$ + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs[2] . . . . . –0.3 V to $V_{DD}$ + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D . . . . . 60 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D . . . . . 30 mA
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
Thermal Impedance (4-Layer Board)
48-lead LFCSP . . . . . 25°C/W
48-lead TQFP . . . . . 54.6°C/W
Lead Temperature, Soldering (10 seconds) . . . . . 300°C
IR Reflow, Peak Temperature (<20 seconds) . . . . . 235°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

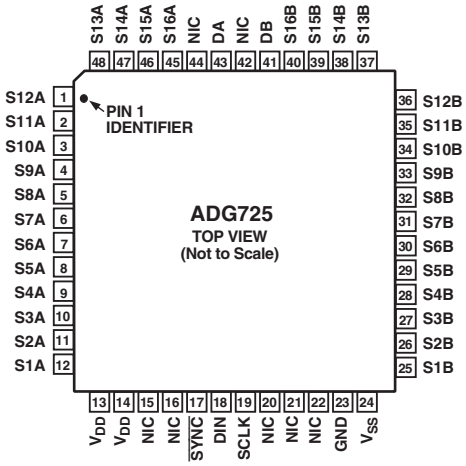
[2] Overvoltages at SCLK, $\overline{\text{SYNC}}$, DIN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG725/ADG731 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

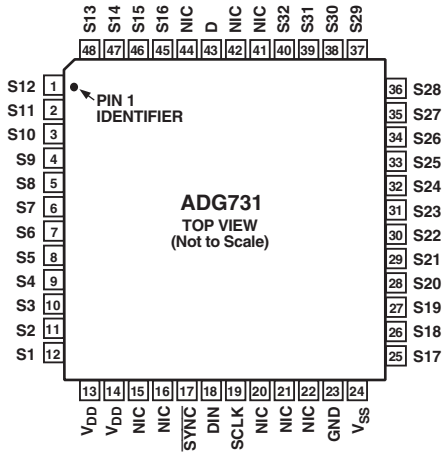
## PIN CONFIGURATIONS

### 48-Lead LFCSP and TQFP




NIC = NOT INTERNALLY CONNECTED.

THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, $V_{SS}$.




NIC = NOT INTERNALLY CONNECT

## PIN FUNCTION DESCRIPTIONS

| ADG725 | ADG731 | Mnemonic | Function |
|---|---|---|---|
| 1–12, 25–40, 45–48 | 1–12, 25–40, 45–48 | Sxx | Source. May be an input or output. |
| 13, 14 | 13, 14 | $V_{DD}$ | Power Supply Input. These parts can be operated from a single supply of 1.8 V to 5.5 V and a dual supply of ±2.5 V. |
| 17 | 17 | $\overline{SYNC}$ | Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers and the input Shift Register is enabled. An 8-bit counter is also enabled. Data is transferred on the falling edges of the following clocks. After eight falling clock edges, switch conditions are automatically updated. $\overline{SYNC}$ may be used to frame the signal or just pulled low for a short period of time to enable the counter and input buffers. |
| 18 | 18 | DIN | Serial Data Input. Data is clocked into the 8-bit Input Register MSB first on the falling edge of the serial clock input. |
| 19 | 19 | SCLK | Serial Clock Input. Data is clocked into the Input Shift Register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz. |
| 23 | 23 | GND | Ground Reference |
| 24 | 24 | $V_{SS}$ | Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect to GND. |
| 41, 43 | N/A | DA, DB | Drain. May be an input or output. |
| N/A | 43 | D | Drain. May be an input or output. |
| | | EPAD | Exposed Pad for LFCSP. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, $V_{SS}$. |

**Table I. ADG725 Truth Table**

| A3 | A2 | A1 | A0 | $\overline{EN}$ | $\overline{CSA}$ | $\overline{CSB}$ | Switch Condition |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | 1 | 1 | Retains Previous Switch Condition |
| X | X | X | X | 1 | X | X | All Switches OFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | S1A – DA, S1B – DB |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | S2A – DA, S2B – DB |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | S3A – DA, S3B – DB |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | S4A – DA, S4B – DB |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | S5A – DA, S5B – DB |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | S6A – DA, S6B – DB |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | S7A – DA, S7B – DB |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | S8A – DA, S8B – DB |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | S9A – DA, S9B – DB |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | S10A – DA, S10B – DB |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | S11A – DA, S11B – DB |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | S12A – DA, S12B – DB |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | S13A – DA, S13B – DB |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | S14A – DA, S14B – DB |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | S15A – DA, S15B – DB |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | S16A – DA, S16B – DB |

X = Don't Care

**Table II. ADG731 Truth Table**

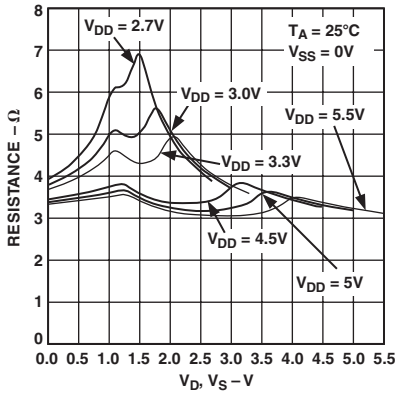
| A4 | A3 | A2 | A1 | A0 | $\overline{EN}$ | $\overline{CSA}$ | Switch Condition |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | 1 | Retains Previous Switch Condition |
| X | X | X | X | X | 1 | X | All Switches OFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 2 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 3 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 4 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 5 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 6 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 7 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 8 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 9 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 10 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 11 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 12 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 13 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 14 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 15 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 16 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 17 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 18 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 19 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 20 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 21 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 22 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 23 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 24 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 25 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 26 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 27 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 28 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 29 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 30 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 31 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 32 |

X = Don't Care

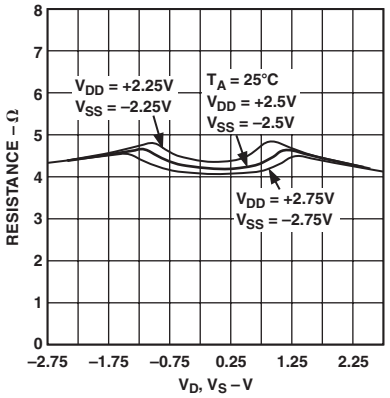
## TERMINOLOGY

| | |
|---|---|
| $V_{DD}$ | Most Positive Power Supply Potential. |
| $V_{SS}$ | Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect to GND. |
| $I_{DD}$ | Positive Supply Current. |
| $I_{SS}$ | Negative Supply Current. |
| GND | Ground (0 V) Reference. |
| S | Source Terminal. May be an input or output. |
| D | Drain Terminal. May be an input or output. |
| $V_D$ ($V_S$) | Analog Voltage on Terminals D, S. |
| $R_{ON}$ | Ohmic Resistance between D and S. |
| $\Delta R_{ON}$ | On Resistance Match between any Two Channels. |
| $R_{FLAT(ON)}$ | Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range. |
| $I_S$ (OFF) | Source Leakage Current with the Switch OFF. |
| $I_D$ (OFF) | Drain Leakage Current with the Switch OFF. |
| $I_D$, $I_S$ (ON) | Channel Leakage Current with the Switch ON. |
| $V_{INL}$ | Maximum Input Voltage for Logic 0. |
| $V_{INH}$ | Minimum Input Voltage for Logic 1. |
| $I_{INL}$ ($I_{INH}$) | Input Current of the Digital Input. |
| $C_S$ (OFF) | OFF Switch Source Capacitance. Measured with reference to ground. |
| $C_D$ (OFF) | OFF Switch Drain Capacitance. Measured with reference to ground. |
| $C_D$, $C_S$ (ON) | ON Switch Capacitance. Measured with reference to ground. |
| $C_{IN}$ | Digital Input Capacitance. |
| $t_{TRANSITION}$ | Delay time measured between the 50% points of the eighth clock falling edge and 90% points of the output when switching from one address state to another. |
| $t_D$ | OFF time measured between the 80% points of both switches when switching from one address state to another. |
| Charge Injection | A measure of the glitch impulse transferred from the digital input to the analog output during switching. |
| OFF Isolation | A measure of unwanted signal coupling through an OFF switch. |
| Crosstalk | A measure of unwanted signal is coupled through from one channel to another as a result of parasitic capacitance. |
| On Response | The Frequency Response of the ON Switch. |
| Insertion Loss | The Loss Due to the On Resistance of the Switch. |

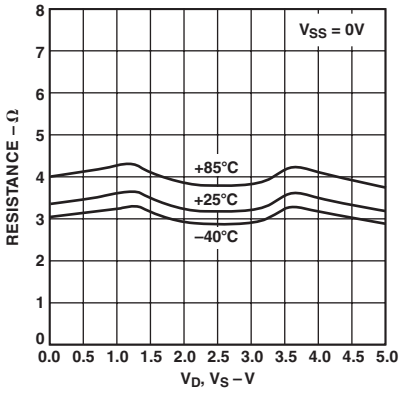
# ADG725/ADG731–Typical Performance Characteristics



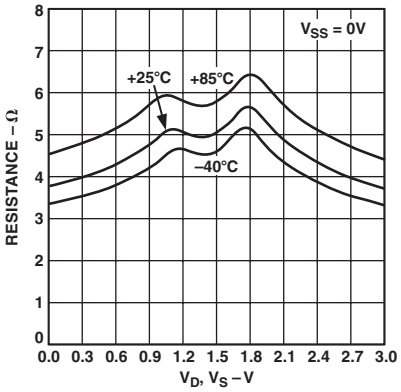

*TPC 1. On Resistance vs. $V_D$ ($V_S$), Single Supply*



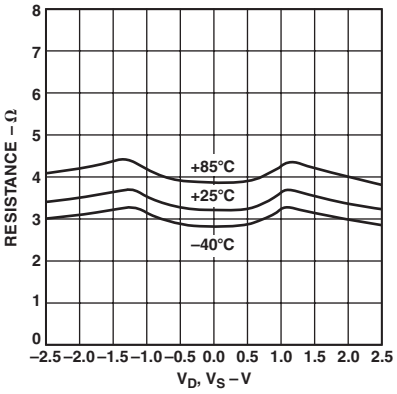

*TPC 2. On Resistance vs. $V_D$ ($V_S$), Dual Supply*



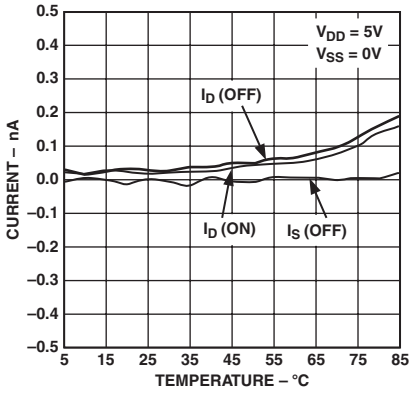

*TPC 3. On Resistance vs. $V_D$ ($V_S$) for Different Temperatures, Single Supply*



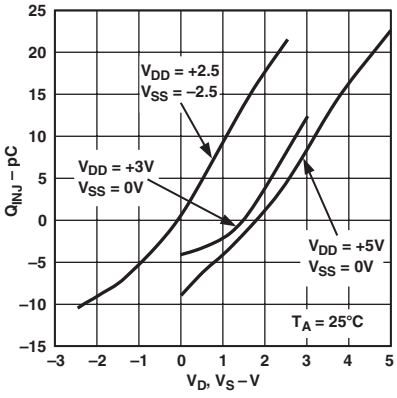

*TPC 4. On Resistance vs. $V_D$ ($V_S$), Single Supply*



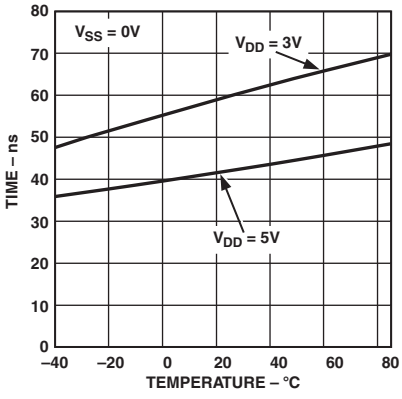

*TPC 5. On Resistance vs. $V_D$ ($V_S$), Dual Supply*



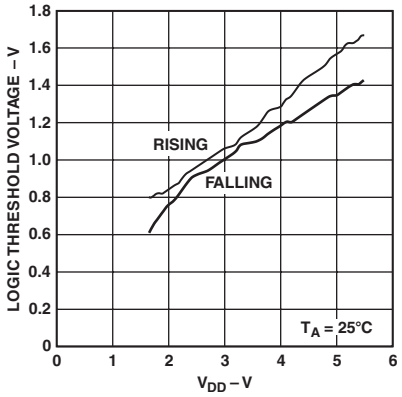

*TPC 6. Leakage Currents vs. Temperature*



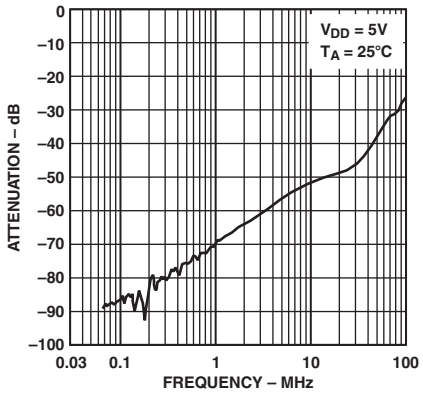

*TPC 7. ADG731 Charge Injection vs. Source Voltage*



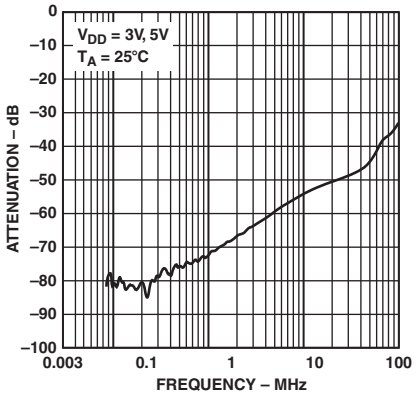

*TPC 8. Switching Times vs. Temperature*



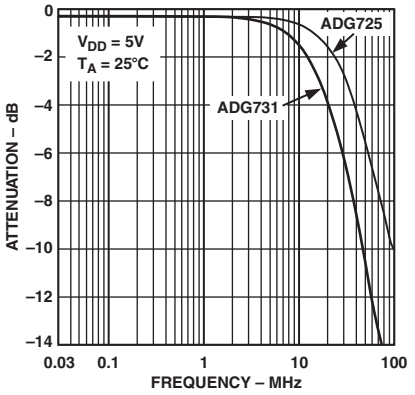

*TPC 9. Logic Threshold Voltage vs. Supply Voltage*




*TPC 10. OFF Isolation vs. Frequency*

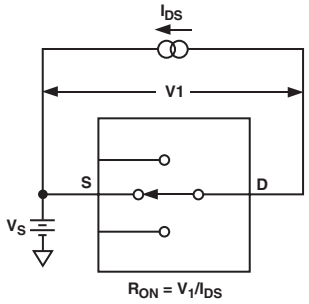



*TPC 11. Crosstalk vs. Frequency*

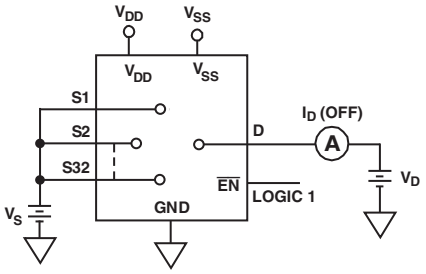



*TPC 12. ON Response vs. Frequency*

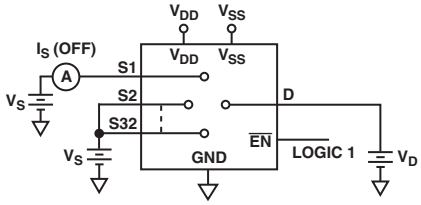
## Test Circuits



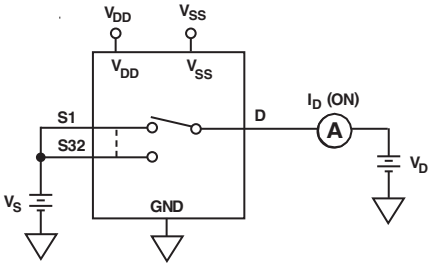

*Test Circuit 1. On Resistance*




*Test Circuit 3. $I_D$ (OFF)*

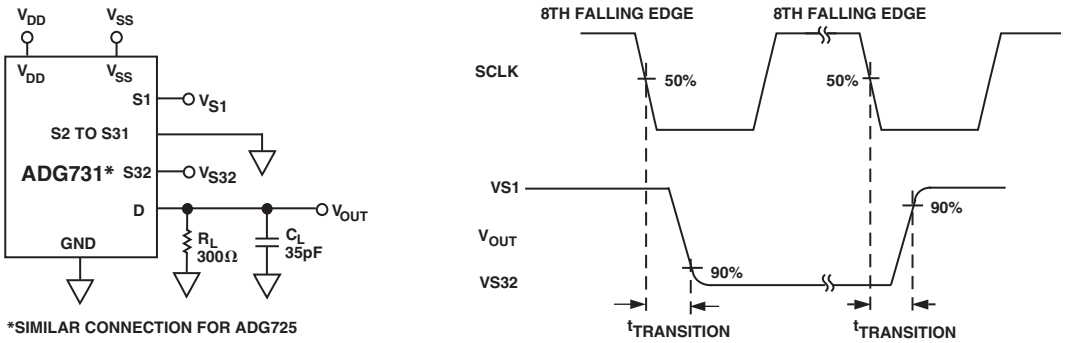



*Test Circuit 2. $I_S$ (OFF)*

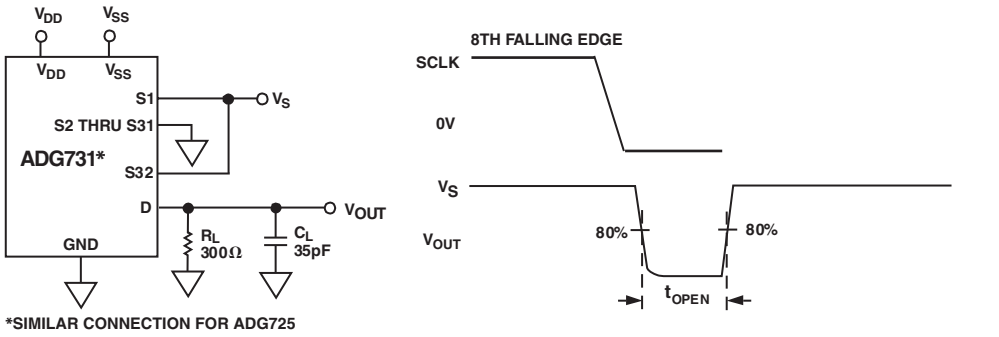



*Test Circuit 4. $I_D$ (ON)*

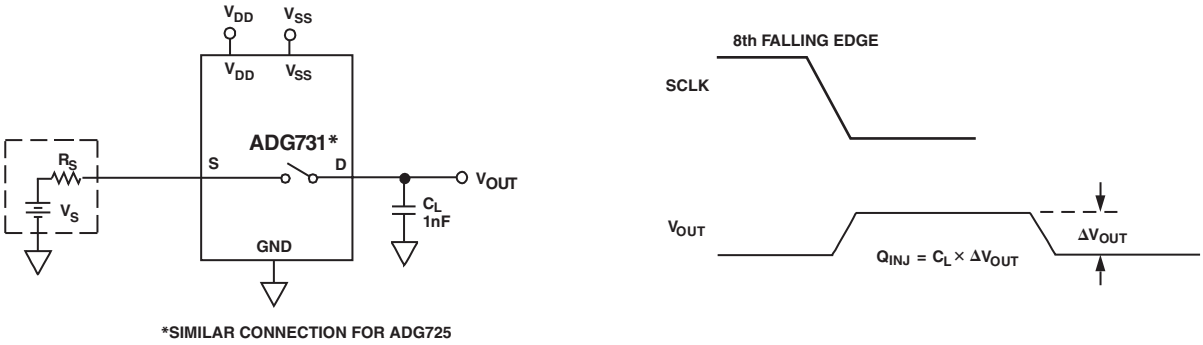
**TEST CIRCUITS (continued)**



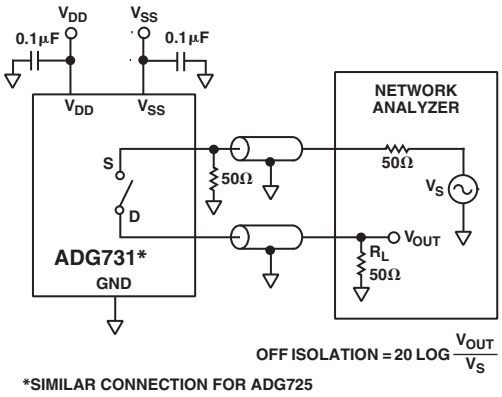

*Test Circuit 5. Switching Time of Multiplexer, $t_{TRANSITION}$*



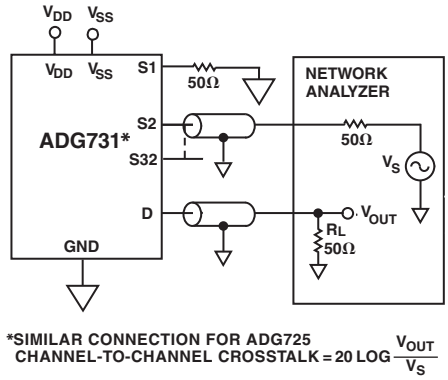

*Test Circuit 6. Break-Before-Make Delay, $t_{OPEN}$*



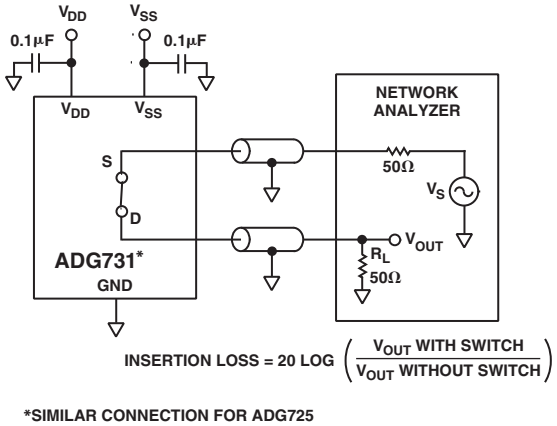

*Test Circuit 7. Charge Injection*




*Test Circuit 8. OFF Isolation*




*Test Circuit 9. Channel-to-Channel Crosstalk*




*Test Circuit 10. Bandwidth*

**POWER-ON RESET**

On power-up of the device, all switches will be in the OFF condition. The Internal Shift Register is filled with zeros and will remain so until a valid write takes place.

**SERIAL INTERFACE**

The ADG725 and ADG731 have a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards and most DSPs. Figure 1 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit Shift Register via DIN under the control of the $\overline{SYNC}$ and SCLK signals.

When $\overline{SYNC}$ goes low, the Input Shift Register is enabled. An 8-bit counter is also enabled. Data from DIN is clocked into the Shift Register on the falling edge of SCLK. Figures 2 and 3 show the contents of the Input Shift Registers for these devices. When the part has received eight clock cycles after $\overline{SYNC}$ has been pulled low, the switches are automatically updated with the new configuration and the Input Shift Register is disabled.

The ADG725 $\overline{CSA}$ and $\overline{CSB}$ data bits allow the user the flexibility to change the configuration of either or both banks of the multiplexer.

**MICROPROCESSOR INTERFACING**

Microprocessor interfacing to the ADG725/ADG731 is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The ADG725/ADG731 requires an 8-bit data-word with data valid on the falling edge of SCLK.

Figures 4–7 illustrate simple 3-wire interfaces with popular microcontrollers and DSPs.

**ADSP-21xx to ADG725/ADG731 Interface**

The ADSP-21xx family of DSPs are easily interfaced to the ADG725/ADG731 without the need for extra logic. Figure 4 shows an example of an SPI interface between the ADG725/ADG731 and the ADSP-2191M. SCK of the ADSP-2191M drives the SCLK of the mux, while the MOSI output drives the serial data line, DIN. $\overline{SYNC}$ is driven from one of the port lines, in this case $\overline{SPIxSEL}$.

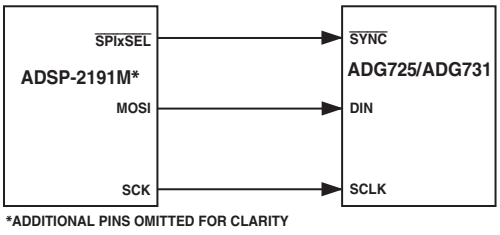



*Figure 4. ADSP-2191M to ADG725/ADG731 Interface*

A serial interface between the ADG725/ADG731 and the ADSP-2191M SPORT is shown in Figure 5. In this interface example, SPORT0 is used to transfer data to the switch. Transmission is initiated by writing a word to the Tx Register after the SPORT has been enabled. In a write sequence, data is clocked out on each rising edge of the DSP's serial clock and clocked into the ADG725/ADG731 on the falling edge of its SCLK. The update of each switch condition takes place automatically after the eighth SCLK falling edge, regardless of the frame sync condition.

Communication between two devices at a given clock speed is possible when the following specs are compatible: frame sync delay and frame sync setup and hold, data delay and data setup and hold, and SCLK width. The ADG725/ADG31 expects a $t_4$ ($\overline{SYNC}$ falling edge to SCLK falling edge set-up time) of 13 ns minimum. Consult the ADSP-21xx User Manual for information on clock and frame sync frequencies for the SPORT Register.

The SPORT Control Register should be set up as follows:

TFSW = 1, Alternate Framing

INVTFS = 1, Active Low Frame Signal

DTYPE = 00, Right Justify Data

ISCLK = 1, Internal Serial Clock

TFSR = 1, Frame Every Word

ITFS = 1, Internal Framing Signal

SLEN = 0111, 8-Bit Data-Word

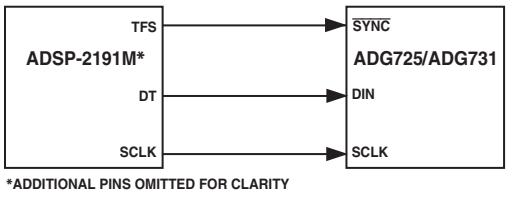



*Figure 5. ADSP-2191M to ADG725/ADG731 Interface*

**8051 to ADG725/ADG731 Interface**

A serial interface between the ADG725/ADG731 and the 8051 is shown in Figure 6. TXD of the 8051 drives SCLK of the ADG725/ADG731, while RXD drives the serial data line, DIN. P3.3 is a bit-programmable pin on the serial port and is used to drive $\overline{SYNC}$.

The 8051 provides the LSB of its SBUF Register as the first bit in the data stream. The user will have to ensure that the data in the SBUF Register is arranged correctly as the switch expects MSB first.

When data is to be transmitted to the switch, P3.3 is taken low. Data on RXD is clocked out of the microcontroller on the rising edge of TXD and is valid on the falling edge. As a result, no glue logic is required between the ADG725/ADG731 and microcontroller interface.

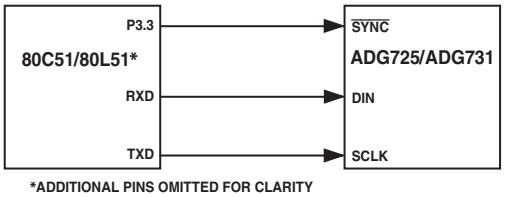



*Figure 6. 8051 to ADG725/ADG731 Interface*

**MC68HC11 Interface to ADG725/ADG731**

Figure 7 shows an example of a serial interface between the ADG725/ADG731 and the MC68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the mux, while the MOSI output drives the serial data line, DIN. $\overline{SYNC}$ is driven from one of the port lines, in this case PC7. The 68HC11 is configured for Master Mode: MSTR = 1, CPOL = 0, and CPHA = 1. When data is transferred to the part, PC7 is taken low, and data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK.

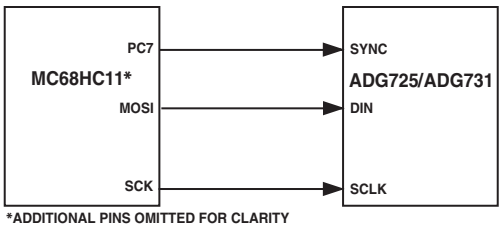



*Figure 7. MC68HC11 Interface to ADG725/ADG731*

## APPLICATION CIRCUITS

**ADG725/ADG731 in an Optical Network Control Loop**

The ADG725/ADG731 can be used in optical network applications that have higher port counts and greater multiplexing requirements. The ADG725/ADG731 are well suited to these applications because they allow a single control circuit to connect a higher number of channels without increasing board size and design complexity.

In the circuit shown in Figure 8, the 0 V to 5 V outputs of the AD5532HS are amplified to a range of 0 V to 180 V and then used to control actuators that determine the position of MEMS mirrors in an optical switch. The exact position of each mirror is measured using sensors. The sensor readings are muxed using the ADG731, a 32-channel switch, and fed back to a single-channel 14-bit ADC (AD7894).

The control loop is driven by an ADSP-2191L, a 32-bit DSP with an SPI compatible SPORT interface. It writes data to the DAC, controls the multiplexer, and reads data from the ADC via a 3-wire serial interface.

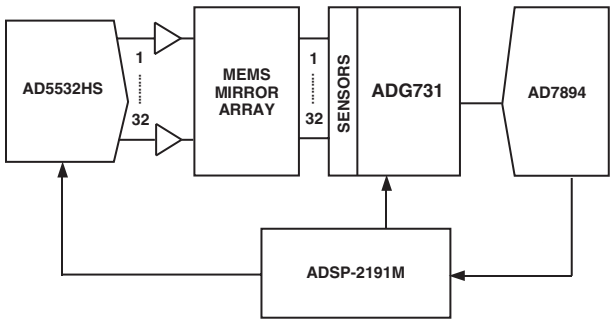



*Figure 8. Optical Network Control Loop*

**Expand the Number of Selectable Serial Devices Using the ADG725/ADG731**

The $\overline{SYNC}$ pin of the ADG725/ADG731 can be used to select one of a number of multiplexers. All devices receive the same serial clock and serial data, but only one device will receive the

SYNC signal at any one time. The mux addressed will be determined by the decoder. There will be some digital feedthrough from the digital input lines. Using a burst clock will minimize the effects of digital feedthrough on the analog signal channels. Figure 9 shows a typical circuit.

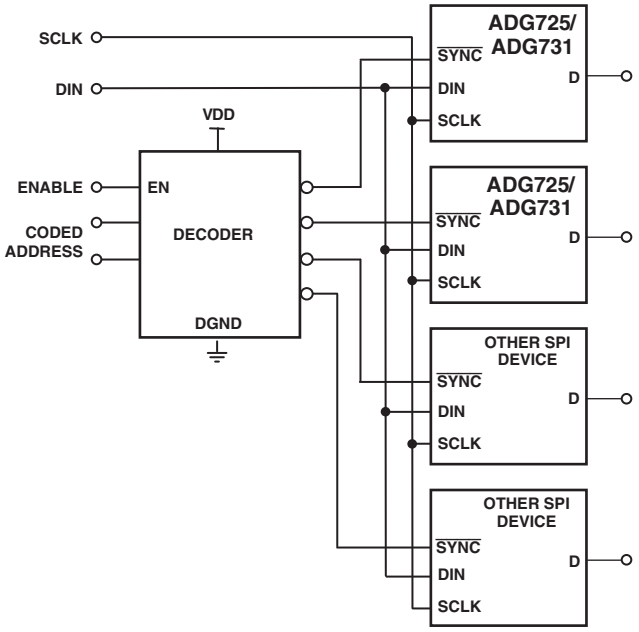



*Figure 9. Addressing Multiple ADG725/ADG731s Using a Decoder*

# OUTLINE DIMENSIONS

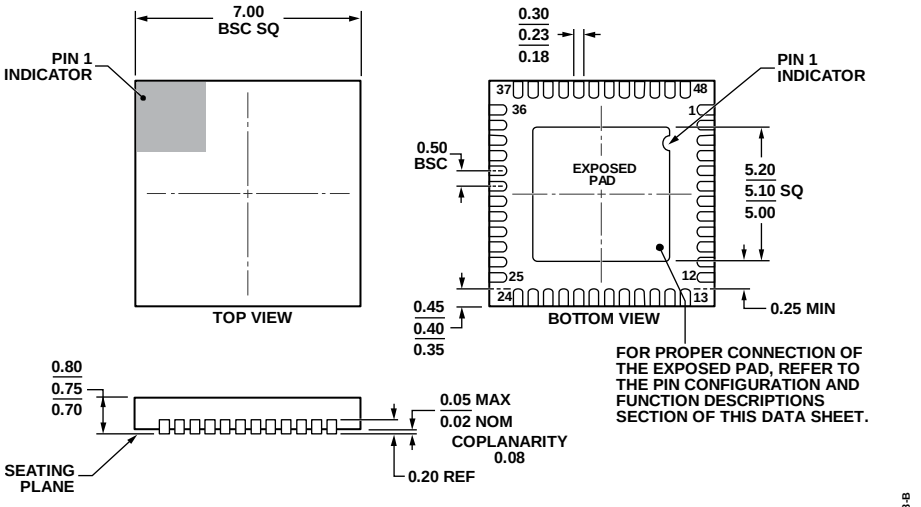



*Figure 10. 48-Lead Lead Frame Chip Scale Package [LFCSP]*
*7 mm × 7 mm Body and 0.75 mm Package Height*
*(CP-48-4)*
*Dimensions shown in millimeters*

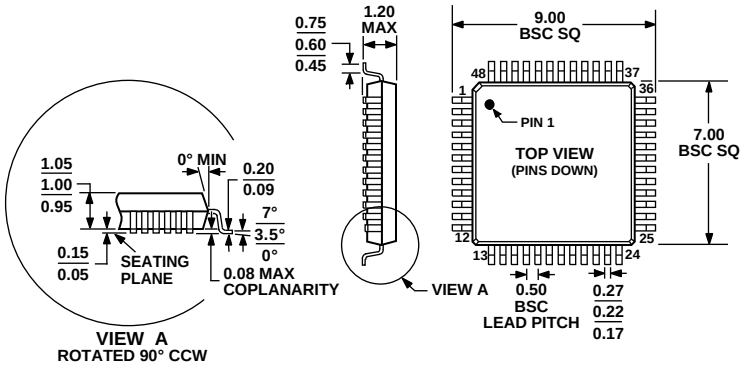



*Figure 11. 48-Lead Thin Plastic Quad Flat Package [TQFP]*
*(SU-48)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADG725BCPZ | –40°C to +85°C | 48-Lead Frame Chip Scale Package [LFCSP] | CP-48-4 |
| ADG725BSUZ | –40°C to +85°C | 48-Lead Thin Plastic Quad Flat Package [TQFP] | SU-48 |
| ADG731BCPZ | –40°C to +85°C | 48-Lead Frame Chip Scale Package [LFCSP] | CP-48-4 |
| ADG731BCPZ-REEL | –40°C to +85°C | 48-Lead Frame Chip Scale Package [LFCSP] | CP-48-4 |
| ADG731BCPZ-REEL7 | –40°C to +85°C | 48-Lead Frame Chip Scale Package [LFCSP] | CP-48-4 |
| ADG731BSUZ | –40°C to +85°C | 48-Lead Thin Plastic Quad Flat Package [TQFP] | SU-48 |

[1] Z = RoHS Compliant Part.

## REVISION HISTORY

**9/15—Rev. A to Rev. B**

Changed NC Pin to NIC Pin ..... Throughout
Added Exposed Pad Notation, ADG725 Pin Configuration ..... 7
Updated Outline Dimensions ..... 16
Changes to Ordering Guide ..... 16

**6/03—Rev. 0 to Rev. A**

Edits to Ordering Guide ..... 6
Edits to Pin Configurations ..... 7
Edits to Pin Function Descriptions ..... 7
Changes to Test Circuit 3 ..... 11
Updated Outline Dimensions ..... 16


D02766-0-9/15(B)

# CMOS, Low Voltage, 3-Wire Serially-Controlled, Matrix Switches

Data Sheet **ADG738/ADG739**

## FEATURES

- 3-wire serial interface
- 2.7 V to 5.5 V single supply
- 2.5 Ω on resistance
- 0.75 Ω on-resistance flatness
- 100 pA leakage currents
- Single 8-to-1 multiplexer ADG738
- Dual 4-to-1 multiplexer ADG739
- Power-on reset
- TTL/CMOS-compatible
- Qualified for automotive applications

## APPLICATIONS

- Data acquisition systems
- Communication systems
- Relay replacement
- Audio and video switching

## FUNCTIONAL BLOCK DIAGRAMS

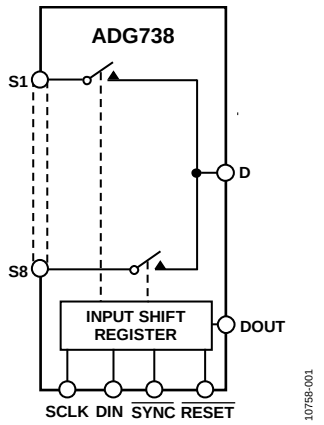



*Figure 1.*

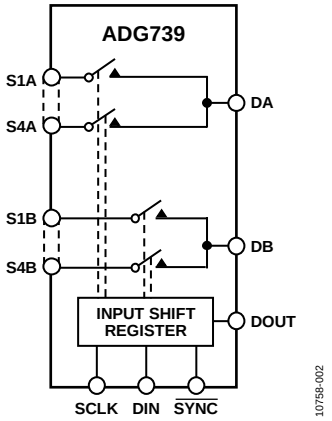



*Figure 2.*

## GENERAL DESCRIPTION

The ADG738 and ADG739 are CMOS analog matrix switches with a serially-controlled 3-wire interface. The ADG738 is an 8-channel matrix switch, while the ADG739 is a dual 4-channel matrix switch. On resistance is closely matched between switches and very flat over the full signal range.

The ADG738 and ADG739 utilize a 3-wire serial interface that is compatible with SPI™, QSPI™, MICROWIRE®, and some DSP interface standards. The output of the input shift register, DOUT, enables a number of these parts to be daisy-chained. On power-up, the internal input shift register contains all zeros and all switches are in the off state.

Each switch conducts equally well in both directions when on, making these parts suitable for both multiplexing and demultiplexing applications. As each switch is turned on or off by a separate bit, these parts can also be configured as a type of switch array, where any, all, or none of the eight switches may be closed at any time. The input signal range extends to the supply rails.

All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

The ADG738 and ADG739 are available in 16-lead TSSOP packages.

## PRODUCT HIGHLIGHTS

1. 3-Wire Serial Interface.
2. Single Supply Operation. The ADG738/ADG739 are fully specified and guaranteed with 3 V and 5 V supply rails.
3. Low On Resistance, 2.5 Ω typical.
4. Any configuration of switches may be on or off at any one time.
5. Guaranteed Break-Before-Make Switching Action.
6. Small 16-lead TSSOP Package.

Rev. A Document Feedback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Tel: 781.329.4700 
Technical Support www.analog.com

# TABLE OF CONTENTS



## REVISION HISTORY

**11/12—Rev. 0 to Rev. A**

Updated Format ... Universal
Changes to Features Section ... 1
Added W Version Specifications to Table 1 ... 3
Added W Version Specifications to Table 2 ... 4
Changes to Table 4 ... 6
Changes to Figure 7, Figure 8, and Figure 11 ... 9
Changes to Figure 12 ... 10
Deleted Figure 22 ... 12
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

**4/00—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD}$ = 5 V ± 10%, GND = 0 V, unless otherwise noted.

**Table 1.**

| Parameter | 25°C | B Version −40°C to +85°C | W Version −40°C to +105°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 2.5 | | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA; see Figure 19 |
| | 4.5 | 5 | 6 | Ω max | |
| On-Resistance Match Between Channels ($\Delta R_{ON}$) | | 0.4 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA |
| | | 0.8 | 1 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 0.75 | | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA |
| | | 1.2 | 1.5 | Ω max | |
| LEAKAGE CURRENTS | | | | | $V_{DD}$ = 5.5 V |
| Source Off Leakage $I_S$ (Off) | ±0.01 | | | nA typ | $V_D$ = 4.5 V/1 V, $V_S$ = 1 V/4.5 V; see Figure 20 |
| | ±0.1 | ±0.3 | ±0.6 | nA max | |
| Drain Off Leakage $I_D$ (Off) | ±0.01 | | | nA typ | $V_D$ = 4.5 V/1 V, $V_S$ = 1 V/4.5 V |
| | ±0.1 | ±1 | ±1.3 | nA max | |
| Channel On Leakage $I_D$, $I_S$ (On) | ±0.01 | | | nA typ | $V_D$ = $V_S$ = 1 V/4.5 V, see Figure 21 |
| | ±0.1 | ±1 | ±1.3 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | | | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | | | 0.8 | V max | |
| Input Current, $I_{INL}$ or $I_{INH}$ | 0.005 | | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | ±0.1 | ±0.1 | μA max | |
| $C_{IN}$, Digital Input Capacitance | 3 | | | pF typ | |
| DIGITAL OUTPUT | | | | | |
| Output Low Voltage | | 0.4 | | max | $I_{SINK}$ = 6 mA |
| $C_{OUT}$, Digital Output Capacitance | 4 | | | pF typ | |
| DYNAMIC CHARACTERISTICS[1] | | | | | |
| $t_{ON}$ | 20 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, see Figure 22; $V_{S1}$ = 3 V |
| | | 32 | 35 | ns max | |
| $t_{OFF}$ | 10 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, see Figure 22; $V_{S1}$ = 3 V |
| | | 17 | 20 | ns max | |
| Break-Before-Make Time Delay, $t_D$ | 9 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 1 | 1 | ns min | $V_{S1}$ = $V_{S8}$ = 3 V, see Figure 22 |
| Charge Injection | ±3 | | | pC typ | $V_S$ = 2.5 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; see Figure 23 |
| Off Isolation | −55 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz |
| | −75 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; see Figure 25 |
| Channel-to-Channel Crosstalk | −55 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz |
| | −75 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; see Figure 24 |
| −3 dB Bandwidth | | | | | |
| ADG738 | 65 | | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, see Figure 25 |
| ADG739 | 100 | | | MHz typ | |
| $C_S$ (Off) | 13 | | | pF typ | |
| $C_D$ (Off) | | | | | |
| ADG738 | 85 | | | pF typ | |
| ADG739 | 42 | | | pF typ | |
| $C_D$, $C_S$ (On) | | | | | |
| ADG738 | 96 | | | pF typ | |
| ADG739 | 48 | | | pF typ | |
| POWER REQUIREMENTS | | | | | $V_{DD}$ = 5.5 V |
| $I_{DD}$ | 10 | | | μA typ | Digital Inputs = 0 V or 5.5 V |
| | | 20 | 20 | μA max | |

[1] Guaranteed by design, not subject to production test.

$V_{DD}$ = 3 V ± 10%, GND = 0 V, unless otherwise noted.

**Table 2.**

| Parameter | 25°C | B Version −40°C to +85°C | W Version −40°C to +105°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 6 | | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA; see Figure 19 |
| | 11 | 12 | 16 | Ω max | |
| On-Resistance Match Between Channels ($\Delta R_{ON}$) | | 0.4 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA |
| | | 1.2 | 1.4 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 3.5 | | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA |
| LEAKAGE CURRENTS | | | | | $V_{DD}$ = 3.3 V |
| Source Off Leakage $I_S$ (Off) | ±0.01 | | | nA typ | $V_S$ = 3 V/1 V, $V_D$ = 1 V/3 V; see Figure 20 |
| | ±0.1 | ±0.3 | ±0.6 | nA max | |
| Drain Off Leakage $I_D$ (Off) | ±0.01 | | | nA typ | $V_D$ = 3 V/1 V, $V_D$ = 1 V/3 V |
| | ±0.1 | ±1 | ±1.3 | nA max | |
| Channel On Leakage $I_D$, $I_S$ (On) | ±0.01 | | | nA typ | $V_D$ = $V_S$ = 3 V/1 V, see Figure 21 |
| | ±0.1 | ±1 | ±1.3 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | | | 2.0 | V min | |
| Input Low Voltage, $V_{INL}$ | | | 0.4 | V max | |
| Input Current, $I_{INL}$ or $I_{INH}$ | 0.005 | | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | ±0.1 | ±0.1 | μA max | |
| $C_{IN}$, Digital Input Capacitance | 3 | | | pF typ | |
| DIGITAL OUTPUT | | | | | |
| Output Low Voltage | | 0.4 | | max | $I_{SINK}$ = 6 mA |
| $C_{OUT}$, Digital Output Capacitance | 4 | | | pF typ | |
| DYNAMIC CHARACTERISTICS[1] | | | | | |
| $t_{ON}$ | 40 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, see Figure 22; $V_{S1}$ = 2 V |
| | | 70 | 75 | ns max | |
| $t_{OFF}$ | 14 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, see Figure 22; $V_{S1}$ = 2 V |
| | | 25 | 40 | ns max | |
| Break-Before-Make Time Delay, $t_D$ | 12 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 1 | 1 | ns min | $V_S$ = 2 V, see Figure 22 |
| Charge Injection | ±3 | | | pC typ | $V_S$ = 1.5 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; see Figure 23 |
| Off Isolation | −55 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz |
| | −75 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; see Figure 25 |
| Channel-to-Channel Crosstalk | −55 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz |
| | −75 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; see Figure 24 |
| −3 dB Bandwidth | | | | | |
| ADG738 | 65 | | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, see Figure 25 |
| ADG739 | 100 | | | MHz typ | |
| $C_S$ (Off) | 13 | | | pF typ | |
| $C_D$ (Off) | | | | | |
| ADG738 | 85 | | | pF typ | |
| ADG739 | 42 | | | pF typ | |
| $C_D$, $C_S$ (On) | | | | | |
| ADG738 | 96 | | | pF typ | |
| ADG739 | 48 | | | pF typ | |
| POWER REQUIREMENTS | | | | | $V_{DD}$ = 3.3 V |
| $I_{DD}$ | 10 | | | μA typ | Digital Inputs = 0 V or 3.3 V |
| | | 20 | 20 | μA max | |

[1] Guaranteed by design, not subject to production test.

## TIMING CHARACTERISTICS

$V_{DD}$ = 2.7 V to 5.5 V. All specifications −40°C to +105°C, unless otherwise noted.

**Table 3.**

| Parameter[1, 2] | Limit at $T_{MIN}$, $T_{MAX}$ | | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| | Min | Max | | |
| $f_{SCLK}$ | | 30 | MHz | SCLK cycle frequency |
| $t_1$ | 33 | | ns | SCLK cycle time |
| $t_2$ | 13 | | ns | SCLK high time |
| $t_3$ | 13 | | ns | SCLK low time |
| $t_4$ | 0 | | ns | $\overline{SYNC}$ to SCLK active edge setup time |
| $t_5$ | 5 | | ns | Data setup time |
| $t_6$ | 4.5 | | ns | Data hold time |
| $t_7$ | 0 | | ns | SCLK falling edge to $\overline{SYNC}$ rising edge |
| $t_8$ | 33 | | ns | Minimum $\overline{SYNC}$ high time |
| $t_9$[3] | 20 | | ns min | SCLK rising edge to DOUT valid |

[1] See Figure 3.
[2] All input signals are specified with tr = tf = 5 ns (10% to 90% of $V_{DD}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3] $C_L$ = 20 pF, $R_L$ = 1 kΩ.

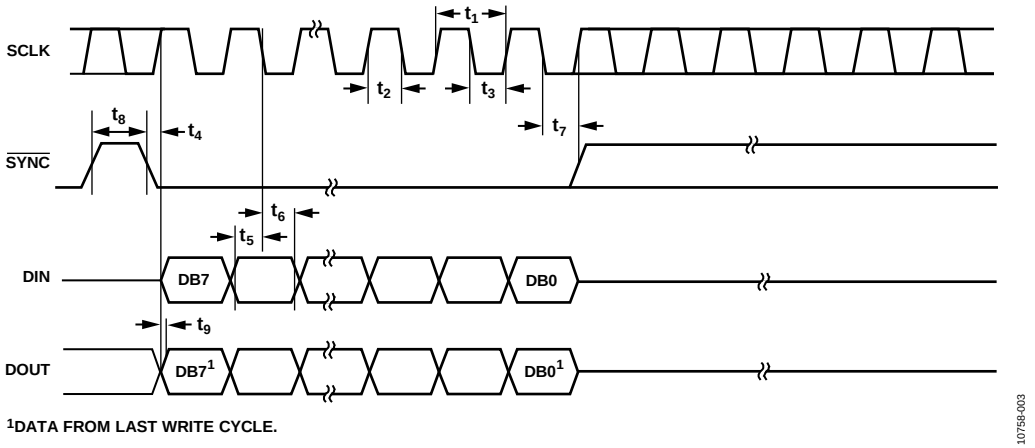



*Figure 3. 3-Wire Serial Interface Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C unless otherwise noted.

**Table 4.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| Analog, Digital Inputs[1] | −0.3 V to $V_{DD}$ + 0.3 V or 30 mA, Whichever Occurs First |
| Peak Current, S or D | 100 mA (Pulsed at 1 ms, 10% Duty Cycle Max) |
| Continuous Current, Each S | 30 mA |
| Continuous Current D | |
| ADG739 | 80 mA |
| ADG738 | 120 mA |
| Operating Temperature Range | |
| Industrial (B Version) | −40°C to +85°C |
| Industrial (W Version) | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| TSSOP Package | |
| $\theta_{JA}$ Thermal Impedance | 150.4°C/W |
| $\theta_{JC}$ Thermal Impedance | 27.6°C/W |
| Lead Temperature, Soldering | As per JEDEC J-STD-020 |

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Limit current to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

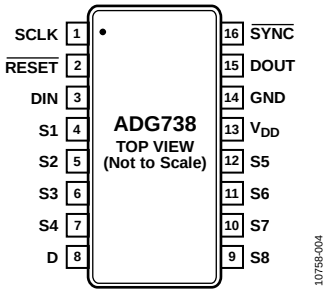



*Figure 4. ADG738 Pin Configuration*

**Table 5. ADG738 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | SCLK | Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz. |
| 2 | $\overline{\text{RESET}}$ | Active Low Control Input. This pin clears the input register and turns all switches to the off condition. |
| 3 | DIN | Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input. |
| 4, 5, 6, 7 | S1, S2, S3, S4 | Source. May be an input or output. |
| 8 | D | Drain. May be an input or output. |
| 9, 10, 11, 12 | S8, S7, S6, S5 | Source. May be an input or output. |
| 13 | $V_{DD}$ | Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V. |
| 14 | GND | Ground Reference. |
| 15 | DOUT | Data Output. This allows a number a parts to be daisy-chained. Data is clocked out of the input shift register on the rising edge of SCLK. This is an open drain output, which should be pulled to the supply with an external resistor. |
| 16 | $\overline{\text{SYNC}}$ | Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following clocks. Taking $\overline{\text{SYNC}}$ high updates the switch conditions. |

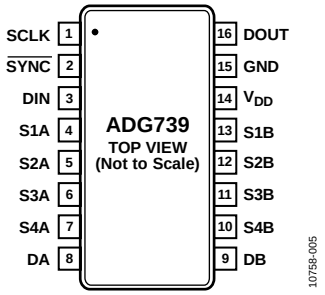



*Figure 5. ADG739 Pin Configuration*

**Table 6. ADG739 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | SCLK | Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz. |
| 2 | $\overline{\text{SYNC}}$ | Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following clocks. Taking $\overline{\text{SYNC}}$ high updates the switch conditions. |
| 3 | DIN | Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input. |
| 4, 5, 6, 7 | S1A, S2A, S3A, S4A | Source. May be an input or output. |
| 8, 9 | DA, DB | Drain. May be an input or output. |
| 10, 11, 12, 13 | S4B, S3B, S2B, S1B | Source. May be an input or output. |
| 14 | $V_{DD}$ | Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V. |
| 15 | GND | Ground Reference. |
| 16 | DOUT | Data Output. This allows a number a parts to be daisy-chained. Data is clocked out of the input shift register on the rising edge of SCLK. This is an open drain output, which should be pulled to the supply with an external resistor. |

# TYPICAL PERFORMANCE CHARACTERISTICS

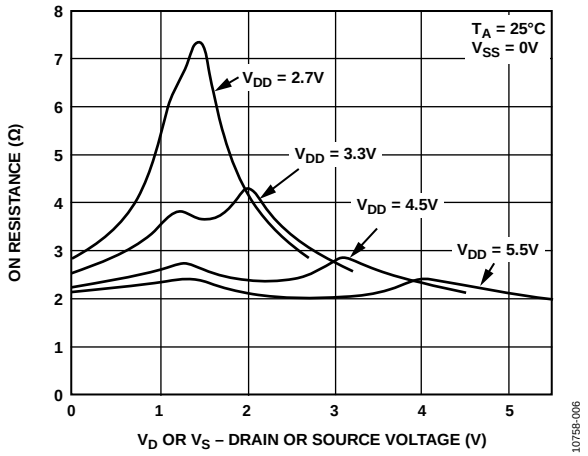



Figure 6. On Resistance as a Function of $V_D$ ($V_S$)

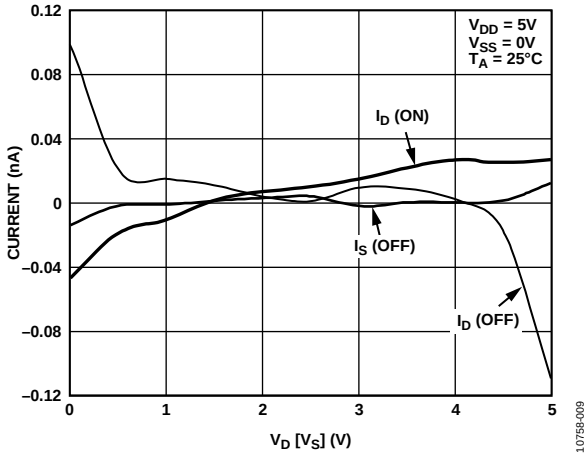



Figure 9. Leakage Currents as a Function of $V_D$ ($V_S$), $V_{DD}$ = 5 V

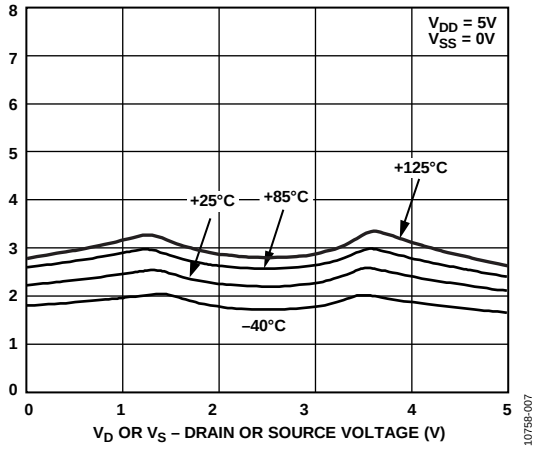



Figure 7. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures, $V_{DD}$ = 5 V

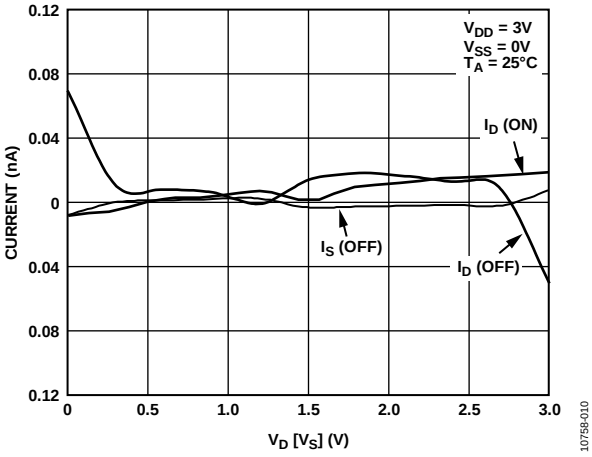



Figure 10. Leakage Currents as a Function of $V_D$ ($V_S$), $V_{DD}$ = 3 V

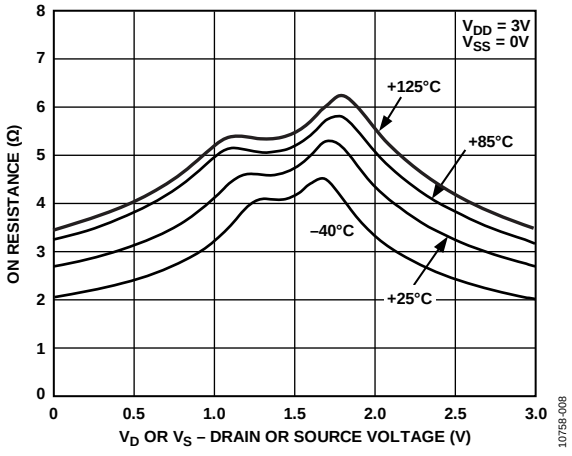



Figure 8. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures, $V_{DD}$ = 3 V

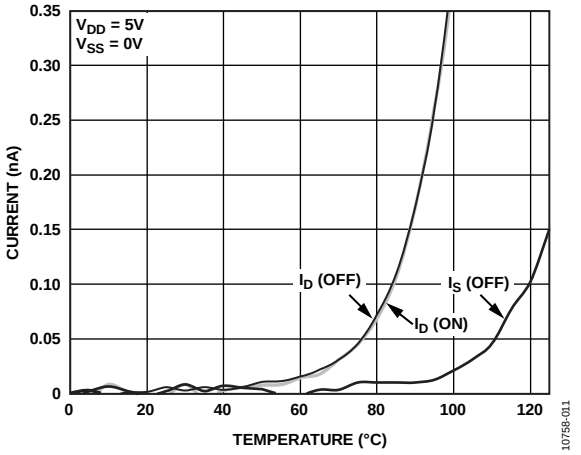



Figure 11. Leakage Currents as a Function of Temperature, $V_{DD}$ = 5 V

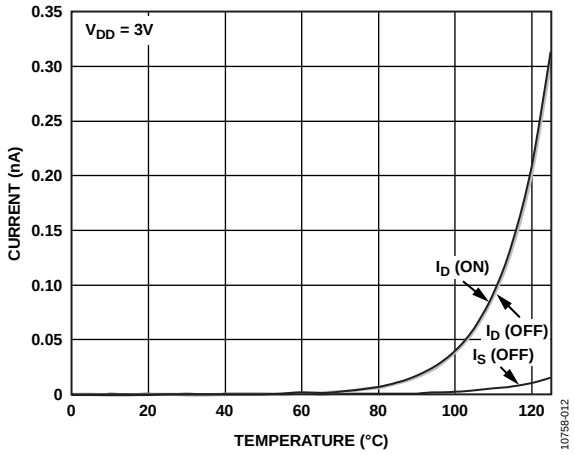



*Figure 12. Leakage Currents as a Function of Temperature, $V_{DD}$ = 3 V*

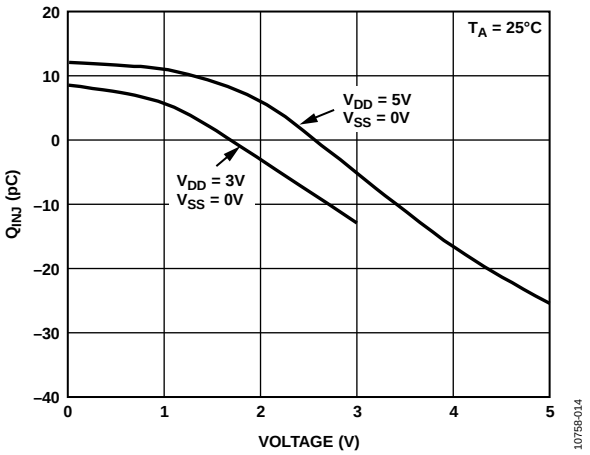



*Figure 14. Charge Injection vs. Source Voltage*

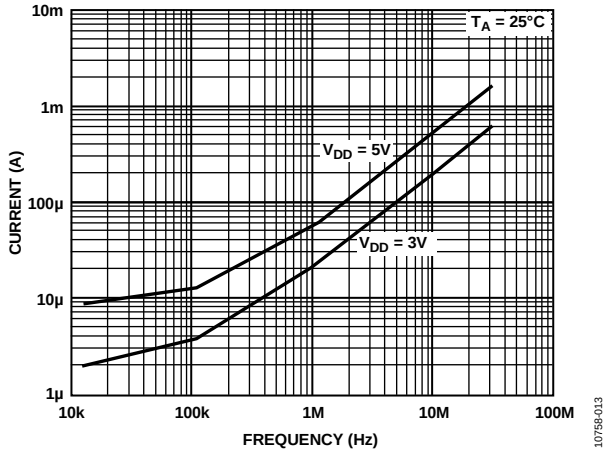



*Figure 13. Input Currents vs. Switching Frequency*

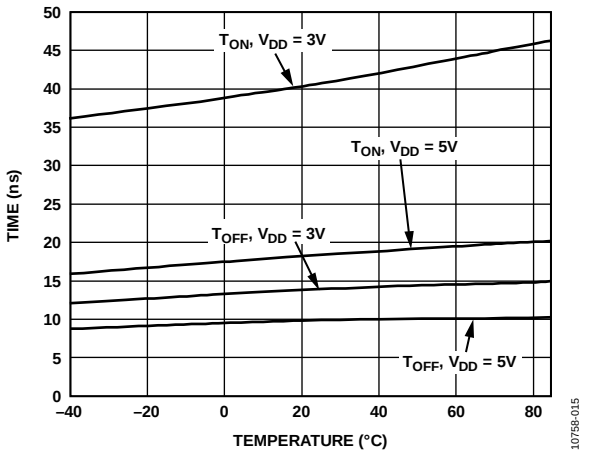



*Figure 15. $T_{ON}$/$T_{OFF}$ Times vs. Temperature*

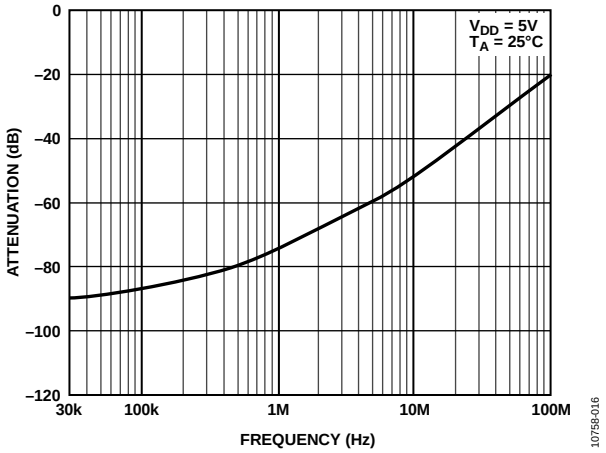



Figure 16. Off Isolation vs. Frequency

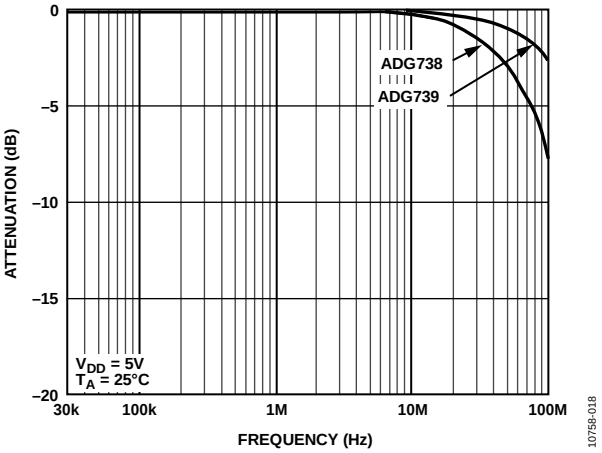



Figure 18. On Response vs. Frequency

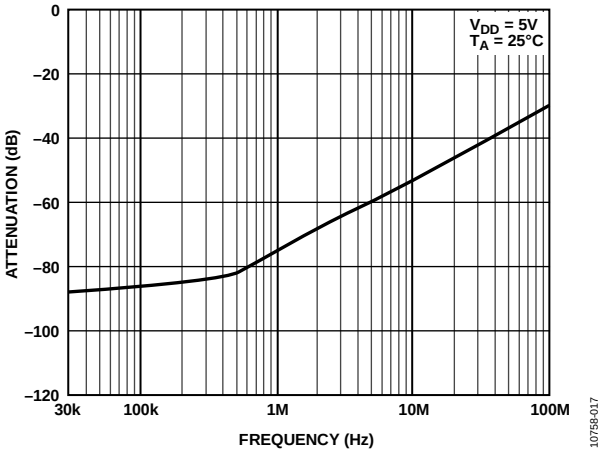



Figure 17. Crosstalk vs. Frequency

# TEST CIRCUITS

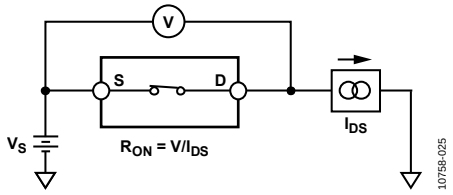



Figure 19. On Resistance

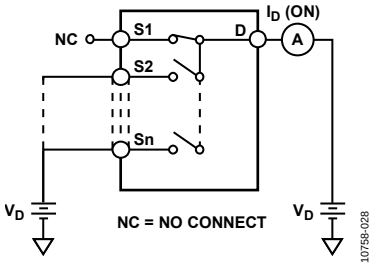



Figure 21. $I_S$, $I_D$ (On)

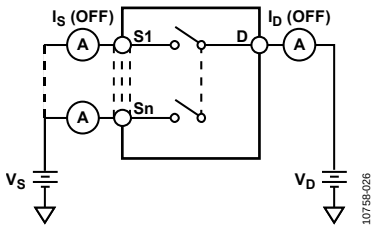



Figure 20. $I_D$ (Off), $I_S$ (Off)

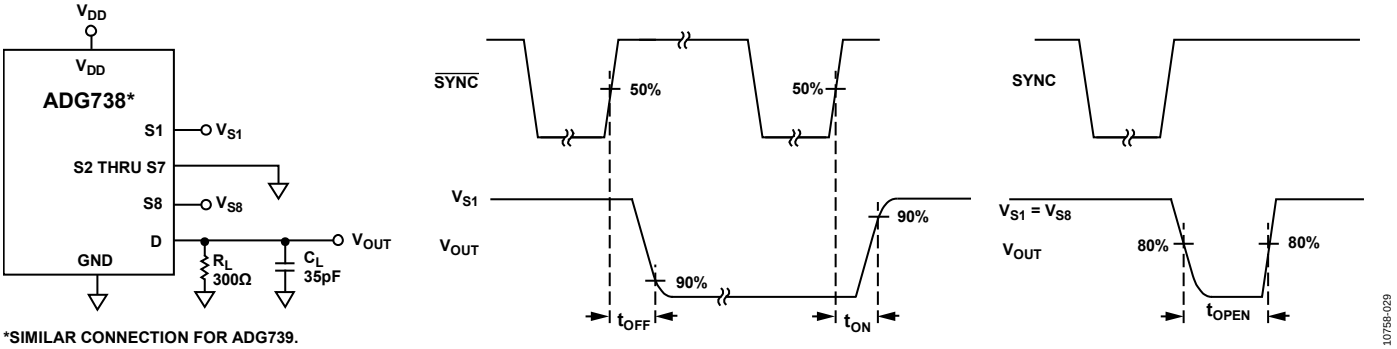



Figure 22. Switching Times and Break-Before-Make Times

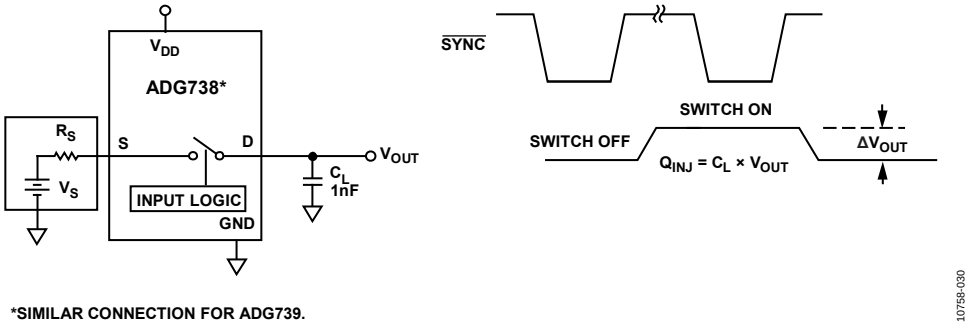
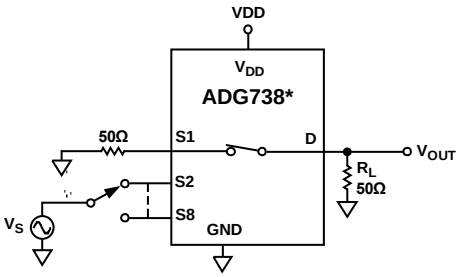



Figure 23. Charge Injection

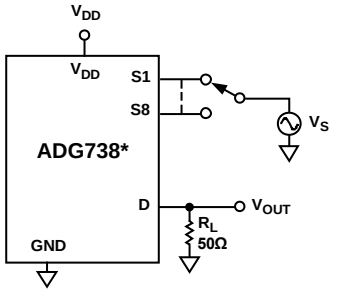



*SIMILAR CONNECTION FOR ADG739.

CHANNEL-TO-CHANNEL CROSSTALK = $20\text{LOG}_{10}$ ($V_{OUT}/V_S$)

10758-031

*Figure 24. Channel-to-Channel Crosstalk*




*SIMILAR CONNECTION FOR ADG739.

S1 IS SWITCHED OFF FOR OFF ISOLATION MEASUREMENTS AND ON FOR BANDWIDTH MEASUREMENTS

OFF ISOLATION = $20\text{LOG}_{10}$ ($V_{OUT}/V_S$)

INSERTION LOSS = $20\text{LOG}_{10}\left(\frac{V_{OUT}\text{ WITH SWITCH}}{V_{OUT}\text{ WITHOUT SWITCH}}\right)$

10758-032

*Figure 25. Off Isolation and Bandwidth*

# TERMINOLOGY

**$V_{DD}$**
Most positive power supply potential.

**$I_{DD}$**
Positive supply current.

**GND**
Ground (0 V) reference.

**S**
Source terminal. May be an input or output.

**D**
Drain terminal. May be an input or output.

**$V_D$ ($V_S$)**
Analog voltage on Terminal D, Terminal S.

**$R_{ON}$**
Ohmic resistance between D and S.

**$\Delta R_{ON}$**
On resistance match between any two channels, that is, $R_{ON}$max – $R_{ON}$min.

**$R_{FLAT(ON)}$**
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

**$I_S$ (Off)**
Source leakage current with the switch off.

**$I_D$ (Off)**
Drain leakage current with the switch off.

**$I_D$, $I_S$ (On)**
Channel leakage current with the switch on.

**$V_{INL}$**
Maximum input voltage for Logic 0.

**$V_{INH}$**
Minimum input voltage for Logic 1.

**$I_{INL}$ ($I_{INH}$)**
Input current of the digital input.

**$C_S$ (Off)**
Off switch source capacitance. Measured with reference to ground.

**$C_D$ (Off)**
Off switch drain capacitance. Measured with reference to ground.

**$C_D$, $C_S$ (On)**
On switch capacitance. Measured with reference to ground.

**$C_{IN}$**
Digital input capacitance.

**$t_{ON}$**
Delay time between the 50% and 90% points of the $\overline{\text{SYNC}}$ rising edge and the switch on condition.

**$t_{OFF}$**
Delay time between the 50% and 90% points of the $\overline{\text{SYNC}}$ rising edge and the switch off condition.

**$t_D$**
Off time measured between the 80% points of both switches when switching from one switch to another.

**Charge Injection**
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

**Off Isolation**
A measure of unwanted signal coupling through an off switch.

**Crosstalk**
A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.

**Bandwidth**
The frequency at which the output is attenuated by 3 dB.

**On Response**
The frequency response of the on switch.

**Insertion Loss**
The loss due to the on resistance of the switch.

# THEORY OF OPERATION

The ADG738 and ADG739 are serially controlled, 8-channel and dual 4-channel matrix switches, respectively. While providing the normal multiplexing and demultiplexing functions, these parts also provide the user with more flexibility as to where their signal may be routed. Each bit of the 8-bit serial word corresponds to one switch of the part. A Logic 1 in the particular bit position turns on the switch, while a Logic 0 turns the switch off. Because each switch is independently controlled by an individual bit, this provides the option of having any, all, or none of the switches on. This feature may be particularly useful in the demultiplexing application where the user may wish to direct one signal from the drain to a number of outputs (sources). Take care, however, in the multiplexing situation where a number of inputs may be shorted together (separated only by the small on resistance of the switch).

When changing the switch conditions, a new 8-bit word is written to the input shift register. Some of the bits may be the same as the previous write cycle, as the user may not wish to change the state of some switches. To minimize glitches on the output of these switches, the part cleverly compares the state of switches from the previous write cycle. If the switch is already in the on condition, and is required to stay on, there will be minimal glitches on the output of the switch.

## POWER-ON RESET

During device power-up, all switches will be in the off condition and the internal input shift register is filled with zeros and remains so until a valid write takes place.

## SERIAL INTERFACE

The ADG738 and ADG739 have a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN), which is compatible with SPI, QSPI, MICROWIRE interface standards and most DSPs. Figure 3 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit input shift register via DIN under the control of the $\overline{\text{SYNC}}$ and SCLK signals. Data may be written to the input shift register in more or less than eight bits. In each case, the input shift register retains the last eight bits that were written.

When $\overline{\text{SYNC}}$ goes low, the input shift register is enabled. Data from DIN is clocked into the input shift register on each falling edge of SCLK. Each bit of the 8-bit word corresponds to one of the eight switches. Figure 26 shows the contents of the input shift register. Data appears on the DOUT pin on the rising edge of SCLK suitable for daisy-chaining, delayed, of course, by eight bits. When all eight bits have been written into the shift register, the $\overline{\text{SYNC}}$ line is brought high again. The switches are updated with the new configuration and the input shift register is disabled. With $\overline{\text{SYNC}}$ held high, any further data or noise on the DIN line has no effect on the shift register.

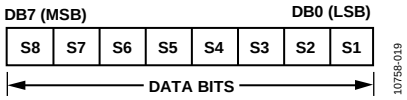



*Figure 26. Input Shift Register Contents*

## MICROPROCESSOR INTERFACING

Microprocessor interfacing to the ADG738/ADG739 is via a serial bus that uses a standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a synchronization signal. The ADG738/ADG739 requires an 8-bit data word with data valid on the falling edge of SCLK.

Data from the previous write cycle is available on the DOUT pin. The following sections illustrate simple 3-wire interfaces with popular microcontrollers and DSPs.

## ADSP-21xx TO ADG738/ADG739

An interface between the ADG738/ADG739 and the ADSP-21xx is shown in Figure 27. In the interface example shown, SPORT0 is used to transfer data to the matrix switch. The SPORT control register should be configured as follows: internal clock operation, alternate framing mode; active low framing signal.

Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. As the data is clocked out of the DSP on the rising edge of SCLK, no glue logic is required to interface the DSP to the matrix switch. The update of each switch condition takes place automatically when TFS is taken high.

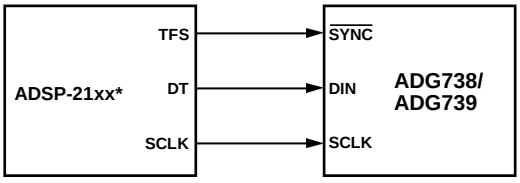



*Figure 27. ADSP-21xx to ADG738/ADG739 Interface*

## 8051 INTERFACE TO ADG738/ADG739

A serial interface between the ADG738/ADG739 and the 8051 is shown in Figure 28. TXD of the 8051 drives SCLK of the ADG738/ADG739, while RXD drives the serial data line, DIN. P3.3 is a bit-programmable pin on the serial port and is used to drive $\overline{\text{SYNC}}$.

The 8051 provides the LSB of its SBUF register as the first bit in the data stream. The user has to ensure that the data in the SBUF register is arranged correctly as the switch expects MSB first.

When data is to be transmitted to the matrix switch, P3.3 is taken low. Data on RXD is clocked out of the microcontroller on the rising edge of TXD and is valid on the falling edge. As a result no glue logic is required between the ADG738/ADG739 and microcontroller interface.

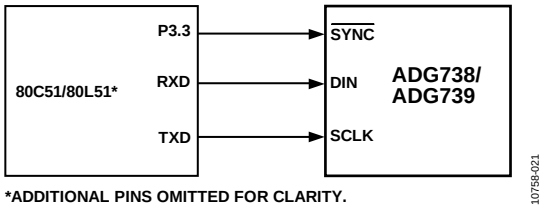



*Figure 28. 8051 Interface to ADG738/ADG739*

## MC68HC11 INTERFACE TO ADG738/ADG739

Figure 29 shows an example of a serial interface between the ADG738/ADG739 and the MC68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the matrix switch, while the MOSI output drives the serial data line, DIN. $\overline{\text{SYNC}}$ is driven from one of the port lines, in this case PC7.

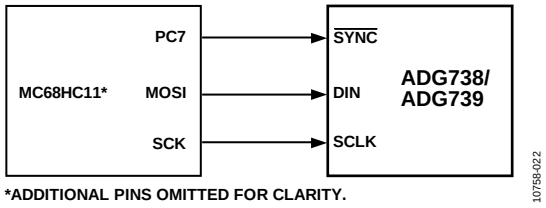



*Figure 29. MC68HC11 Interface to ADG738/ADG739*

The 68HC11 is configured for master mode; MSTR = 1, CPOL = 0, and CPHA = 1. When data is transferred to the part, PC7 is taken low, data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK.

If the user wishes to verify the data previously written to the input shift register, the DOUT line could be connected to MISO of the MC68HC11, and with $\overline{\text{SYNC}}$ low, the input shift register would clock data out on the rising edges of SCLK.

# APPLICATIONS INFORMATION

## EXPAND THE NUMBER OF SELECTABLE SERIAL DEVICES USING AN ADG739

The dual 4-channel ADG739 multiplexer can be used to multiplex a single chip select line to provide chip selects for up to four devices on the SPI bus. Figure 30 illustrates the ADG739 in such a typical configuration. All devices receive the same serial clock and serial data, but only one device receives the $\overline{\text{SYNC}}$ signal at any one time. The ADG739 is a serially controlled device also. One bit programmable pin of the microcontroller is used to enable the ADG739 via $\overline{\text{SYNC2}}$, while another bit programmable pin is used as the chip select for the other serial devices, $\overline{\text{SYNC1}}$. Driving $\overline{\text{SYNC2}}$ low enables changes to be made to the addressed serial devices. By bringing $\overline{\text{SYNC1}}$ low, the selected serial device hanging from the SPI bus is enabled and data will be clocked into its input shift register on the falling edges of SCLK. The convenient design of the matrix switch allows for different combinations of the four serial devices to be addressed at any one time. If more devices need to be addressed via one chip select line, the ADG738 is an 8-channel device and would allow further expansion of the chip select scheme. There may be some digital feedthrough from the digital input lines because SCLK and DIN are permanently connected to each device. Using a burst clock minimizes the effects of digital feedthrough on the analog channels.

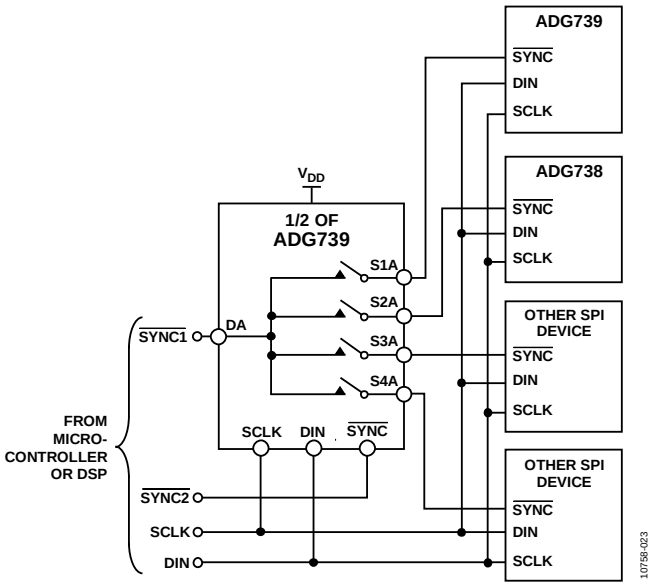



*Figure 30. Addressing Multiple Serial Devices Using an ADG739*

## DAISY-CHAINING MULTIPLE ADG738S

A number of ADG738 matrix switches may be daisy-chained simply by using the DOUT pin. DOUT is an open-drain output that should be pulled to the supply with an external resistor. Figure 31 shows a typical implementation. The $\overline{\text{SYNC}}$ pin of all three parts in the example are tied together. When $\overline{\text{SYNC}}$ is brought low, the input shift registers of all parts are enabled, data is written to the parts via DIN, and clocked through the shift registers. When the transfer is complete, $\overline{\text{SYNC}}$ is brought high and all switches are updated simultaneously. Further shift registers may be added in series.

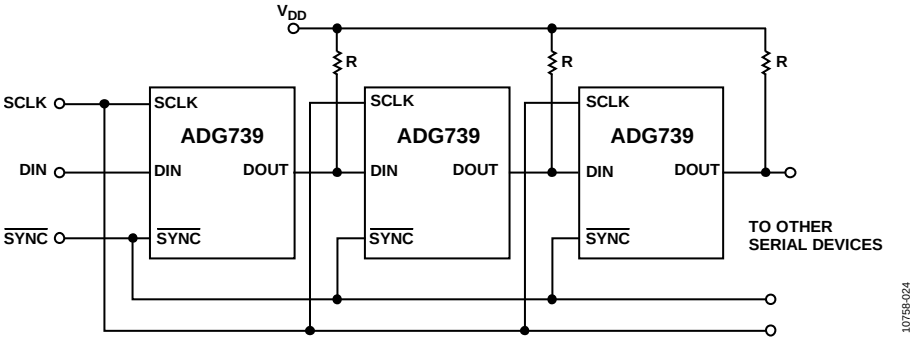



*Figure 31. Multiple ADG739 Devices in a Daisy-Chained Configuration*

# OUTLINE DIMENSIONS

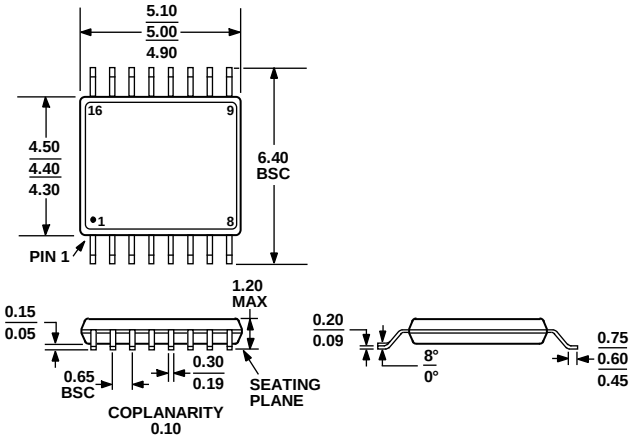



*Figure 32. 16-Lead Thin Shrink Small Outline Package [TSSOP]*
*(RU-16)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1, 2] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADG738BRU | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG738BRUZ | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG738BRUZ-REEL | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG738BRUZ-REEL7 | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG738WBRUZ-REEL | −40°C to +105°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG739BRU | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG739BRU-REEL7 | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG739BRUZ | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG739BRUZ-REEL | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG739BRUZ-REEL7 | −40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

## AUTOMOTIVE PRODUCTS

The ADG738W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

## NOTES

## NOTES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