Design and Fabrication of FS-IGBTs With Enhanced Ruggedness and the Influence of Circuit Parameters on Short-Circuit

Jingping Zhang, Houcai Luo, Huan Wu, Bofeng Zheng, Guoqi Zhang, *Fellow, IEEE*, and Xianping Chen, *Senior Member, IEEE*

***Abstract*—Field-Stop Insulated Gate Bipolar Transistors (FS-IGBTs) are widely used in various power applications due to their low conduction and switching losses. However, further reductions in cell pitch lead to increased cell density, resulting in higher saturation current that adversely impacts the short-circuit ruggedness essential for applications such as welding machines and motor drives. This paper details the design and fabrication of a 650V, 75A FS-IGBT. By incorporating dummy gate and emitter trench structures within the active gate and optimizing the layout of the three cell structures, the short-circuit characteristics of the device are markedly improved. Experimental tests confirm that the device exhibits both low saturation on-state voltage and short-circuit ruggedness. This study further investigates the circuit parameters related to short-circuit conditions and comprehensively analyzes the impact of each parameter on the short-circuit characteristics of the FS-IGBT. The experimental results indicate that the bus voltage V_{DC}, gate voltage V_G, and temperature T_C significantly influence the short-circuit performance of the FS-IGBT. Therefore, a moderate decrease in V_{DC}, V_G, and T_C can effectively enhance the short-circuit ruggedness and the short-circuit withstand time t_{SC} of the device.**

***Index Terms*—FS-IGBT, dummy gate, short-circuit, ruggedness, t_{SC}.**

I. Introduction

DURING short-circuit conduction, the IGBT must simultaneously withstand high voltage and high current. Consequently, the temperature inside the chip rises sharply within a brief interval, risking thermal failure or even device explosion [1], [2], [3], [4]. To prevent destruction of the IGBT under short-circuit conditions, the device must turn off safely after a certain conduction period, referred to as the short-circuit withstand time t_{SC} [5], [6], [7]. A longer t_{SC} indicates greater short-circuit ruggedness but comes at the cost of increased saturation on-state voltage V_{CEsat} [8], [9], [10]. The trade-off between these two parameters is a critical consideration in IGBT design and application. The industry typically uses t_{SC}= 10μs as a standard to evaluate the short-circuit withstand capability of IGBTs [11], [12]. The latest generation of FS-IGBTs features a reduced cell pitch to achieve higher current densities, posing a greater challenge to short-circuit ruggedness [13]. The reduced cell pitch can exacerbate the temperature rise during short-circuit conditions, demanding more sophisticated thermal management strategies and design optimizations to maintain device performance and ruggedness. Although numerous studies have investigated the short-circuit characteristics of IGBTs [14], [15], [16], comprehensive analyses regarding the impact of circuit parameters on short-circuit ruggedness remain insufficient.

To balance conduction losses with short-circuit ruggedness, grounded emitter trenches have been incorporated into the IGBT cell structure. Konishi et al. demonstrated the ability to reduce C_{GE} without increasing C_{GC} by optimizing the ratio and arrangement of the gate and emitter trenches, thereby achieving a low dv/dt and reduced turn-on loss [17]. Further studies have corroborated these findings and revealed that the introduction of emitter trenches also reduces EMI noise [18], [19], [20], [21]. Zhu et al. replaced the grounded emitter trench with a floating dummy gate, which reduces switching losses and mitigates surge current during short-circuit turn-on, thereby enhancing short-circuit ruggedness [22]. Building on the aforementioned studies, we incorporated both dummy gate and emitter trenches within the cell gate trench, and optimally balance conduction loss, switching loss, and short-circuit capability of the FS-IGBT through the strategic arrangement and combination of these three trench configurations.

In this paper, we successfully designed and manufactured a 650V 75A FS-IGBT. The integration of three distinct cell structures enables the FS-IGBT to exhibit a low saturation on-state voltage and enhanced short-circuit ruggedness. The device attains a saturation on-state voltage of 1.65V and a short-circuit withstand time of 13μs, thereby meeting industry-leading standards [23], [24]. Utilizing TCAD simulation design analysis and experimental verification, we propose a methodology for designing and fabricating FS-IGBTs with

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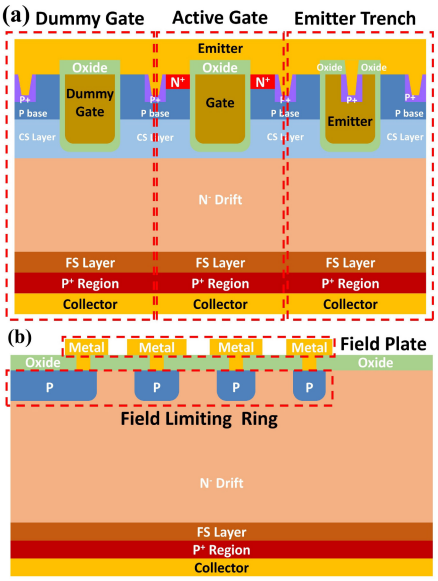

Fig. 1. Cross-sectional (a) cell and (b) terminal structure view of the FS-IGBT.

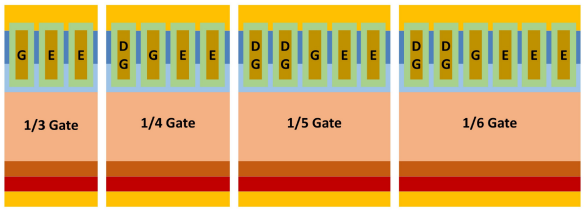

Fig. 2. Cross-sectional cell structure view of the four topologies of the FS-IGBT.

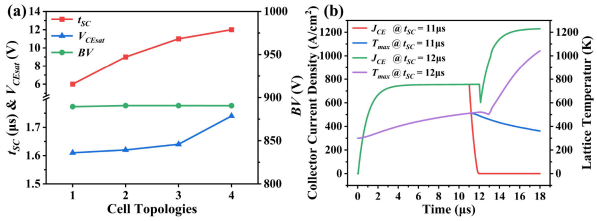

Fig. 3. (a) t_{SC} and V_{CEsat} and BV as a function of cell topologies. (b) Short-circuit characteristics of the 1/5 Gate cell structure.

TABLE I
SIMULATION PARAMETERS OF THE FS-IGBT STRUCTURE

Symbol	Symbol	Value	Unit
T_{CP+}	Collector P+ region depth	1.0	μm
$_{CP+}$	Collector P+ doping concentration	3.0×10^{17}	cm^{-3}
T_{FS}	FS layer depth	2.0	μm
N_{FS}	FS layer doping concentration	3.0×10^{16}	cm^{-3}
T_d	Drift thickness	57.0	μm
N_d	Drift doping concentration	1.0×10^{14}	cm^{-3}
T_t	Trench depth	5.0	μm
W_t	Trench width	1.0	μm
T_{ox}	Gate oxide thickness	0.12	μm
T_{CS}	Carrier storage (CS) layer depth	2.5	μm
N_{CS}	CS layer doping concentration	3.0×10^{15}	cm^{-3}
T_{Pbase}	P base depth	3.0	μm
N_{Pbase}	P base doping concentration	1.0×10^{17}	cm^{-3}
T_{N+}	N+ depth	0.3	μm
L_{N+}	N+ length	0.2	μm
N_{N+}	N+ doping concentration	1.0×10^{20}	cm^{-3}
T_{P+}	P+ depth	0.6	μm
L_{P+}	P+ length	0.4	μm
N_{P+}	P+ doping concentration	1.0×10^{20}	cm^{-3}
T_{CT}	Contact (CT) depth	0.4	μm
L_{CT}	CT length	0.3	μm

enhanced short-circuit ruggedness [25], [26]. A series of experiments was conducted to evaluate the effects of various circuit parameters, including bus voltage V_{DC}, gate voltage V_G, gate resistance R_G, and temperature T_C, on the short-circuit characteristics.

II. DEVICE DESIGN AND FABRICATION

To balance the saturation on-state voltage and short-circuit capability of the FS-IGBT, introducing dummy gate and emitter trenches in the device cell design can simultaneously reduce current density and Miller capacitance, thereby enhancing short-circuit and switching capabilities. The cross-sectional cell view of the FS-IGBT is illustrated in Fig. 1(a). The N-drift region, with a doping concentration of $1\times10^{14}cm^{-3}$ and a thickness of 62μm, is designed to withstand a forward blocking voltage exceeding 650V. Additionally, the gate oxide has a thickness of 0.12μm, while the gate trench measures 5μm in depth and 1μm in width. The mesa width is 0.8um, so the total cell pitch is 1.8μm. The other parameters are listed in Table I. To withstand a breakdown voltage of 650V, the terminal structure of the FS-IGBT employs a field plate combined with a field limiting ring, as shown in Fig. 1(b). In this paper, Sentaurus TCAD tools are used to perform the device simulations and the compact model simulations. Standard Si physical models are used in the simulation, including Fermi statistics, Shockley-Read-Hall, Auger recombination, and GradQuasiFermi avalanche. The bandgap models are OldSlotboom and NoFermi. Mobility models with PhuMob, high field saturation, and Enormal are also taken into consideration, etc.

To address the trade-off between the saturation on-state voltage and short-circuit ruggedness of the FS-IGBT, we designed the cell structure differently. Fig. 2 displays the four cell topologies. And these four cell topologies are named according to the proportion of active gate in a cell cycle: 1/3 Gate, 1/4 Gate, 1/5 Gate, and 1/6 Gate, respectively. This innovative approach aims to optimize the performance characteristics of the FS-IGBT by varying the active gate ratio, thereby enhancing the short-circuit ruggedness.

The saturation on-state voltage and short-circuit capability of the four FS-IGBT topologies were compared, with simulation results presented in Fig. 3(a). The figure shows that as the gate ratio decreases, the short-circuit withstand time and saturation on-state voltage of the FS-IGBT increase, though at a slowing rate. As the gate ratio decreases, the number of active channels inside the device also decreases, leading to lower current density. This enhances the device's short-circuit ruggedness but reduces its conduction capability. In addition, it is evident from the figure that the cell topologies exert minimal influence the device's breakdown voltage, as the FS-IGBT consistently maintains a high withstand voltage level.

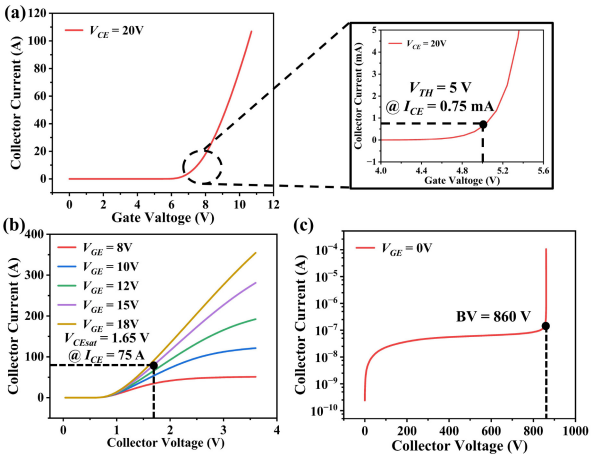

Fig. 4. Simulated (a) Transfer characteristics, (b) forward conduction and (c) forward blocking of the FS-IGBT.

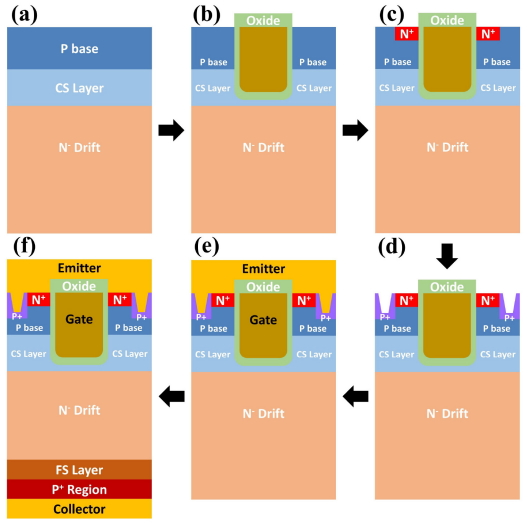

Fig. 5. The manufacturing process of the FS-IGBT.

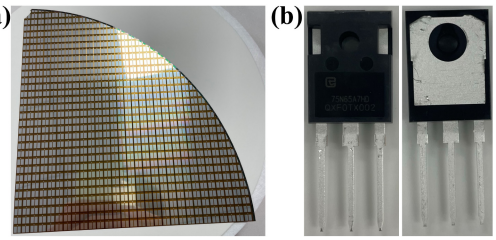

Fig. 6. (a) A quarter of 12-inch wafer and (b) TO-247 packaged device of the 650V 75A FS-IGBT.

To achieve strong short-circuit ruggedness, a 1/5 Gate cell structure was chosen as a trade-off in the final design. Fig. 3(b) illustrates the short-circuit characteristics of the 1/5 Gate cell structure. When a short-circuit occurs as soon as the device is turned on, the collector current rises instantaneously to its peak, and the max lattice temperature gradually increases over time. When the short-circuit ends at 11μs, the collector current J_{CE} drops precipitously and the max lattice temperature T_{max} slowly decreases from its peak. When the short-circuit duration extends to 12μs, the FS-IGBT fails to turn-off safely, resulting in a dramatic increase in both the J_{CE} and T_{max}, ultimately leading to device failure due to thermal runaway. Therefore, the short-circuit withstand time t_{SC} of the FS-IGBT featuring a 1/5 Gate cell structure, as determined through simulation, is 11μs.

The static characteristics of the FS-IGBT were simulated and are presented in Fig. 4. The threshold voltage of the device is approximately 5V, as illustrated in Fig. 4(a). This study designs a 650V FS-IGBT with a current conduction capacity of 75A. The saturation on-state voltage of the device at 75A is 1.65V when the gate drive voltage is 15V, as shown in Fig. 4(b). Through the strategic enhancement of the field plate and the field limiting ring within the terminal structure, the breakdown voltage of the FS-IGBT reaches approximately 860V, exceeding the design margin by 30%.

The FS-IGBTs were fabricated in a 12-inch FAB, using a total of 9 masks in the entire process flow, including a zero-layer alignment. The simplified process flow is displayed in Fig. 5. Ion implantation and annealing of the terminal field limiting ring are first performed on Si substrate wafers, followed by field oxide deposition to protect the terminals. Phosphorus and Boron are then successively implanted and annealed to form the CS Layer and P base [see Fig. 5(a)]. Subsequently, trench etching, gate oxide growth, and polysilicon deposition are carried out [see Fig. 5(b)]. Next, ion implantation of Arsenic is performed to form the N+ emitter region [see Fig. 5(c)]. This is followed by CT opening for P+ implantation and annealing [see Fig. 5(d)]. Frontside metallization forms the gate and emitter, along with passivation layer and polyimide deposition to protect the chip [see Fig. 5(e)]. The wafer is then flipped for backside thinning to 60μm, followed by ion implantation and annealing of the FS layer and P+ region, and finally, metallization is performed to form the collector [see Fig. 5(f)]. The finished wafer is shown in Fig. 6(a), and TO-247 packaging is completed in a standard Si device packaging factory, as shown in Fig. 6(b).

We used a Keysight B1506A Power Device Analyzer for Circuit Design to test the packaged 650V 75A FS-IGBT, as shown in Fig. 7. Experimental testing shows that the threshold voltage of the FS-IGBT is 5V, the saturation voltage is 1.65V, and the forward blocking voltage is 800V. The detailed experimental data are shown in Fig. 8. Comparing the results from the simulation, there are some differences in the breakdown voltage of the device, possibly caused by the chip layout or deviations in the fabrication process. Ignoring this minor difference, the accuracy of our simulation model is demonstrated.

III. Results and Discussion

The short-circuit characteristics of the 650V 75A FS-IGBT were assessed using an Edison DPTM2K04B Power Semiconductor Device Dynamic Characteristics Testing System, as illustrated in Fig. 9(a). Fig. 9(b) presents the equivalent circuit for the short-circuit test. The gate pulse waveforms for the upper and lower FS-IGBTs are shown in Fig. 9(c). Observation of Fig. 9(c) reveals that the companion device is activated first, remaining on for a duration of T_1

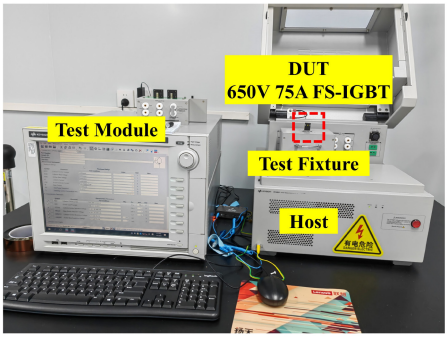

Fig. 7. Keysight B1506A Power Device Analyzer for Circuit Design.

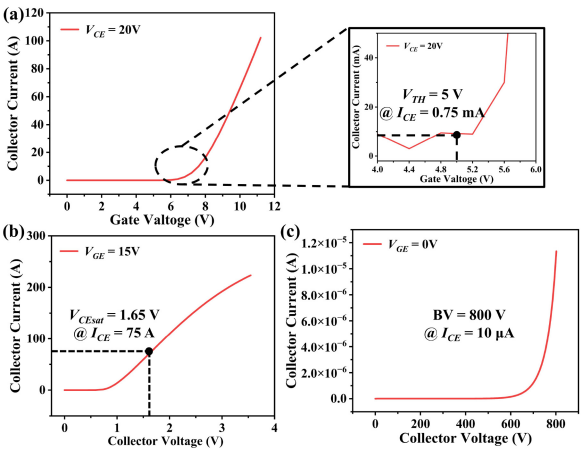

Fig. 8. Measured (a) Transfer characteristics, (b) forward conduction and (c) forward blocking of the FS-IGBT.

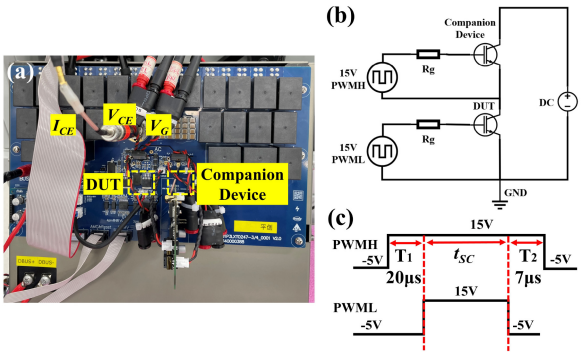

Fig. 9. (a) Edison DPTM2K04B Power Semiconductor Device Dynamic Characteristics Testing System, (b) equivalent circuit and (c) gate pulse waveforms of the upper and lower FS-IGBTs.

before the device under test is activated. Prior to the activation of the DUT, the collector voltage V_{CE} equals the bus voltage V_{DC}, while the collector current I_{CE} initially measures zero due to the load being short-circuited. Upon the application of the gate pulse to the FS-IGBT, the device immediately transitions into a short-circuit condition, resulting in the device simultaneously experiencing high voltage and high current, with power levels significantly exceeding the normal operating conditions. Upon completion of the DUT short-circuit, and after an additional duration of T_2, the companion device is deactivated to conclude the short-circuit test. In the

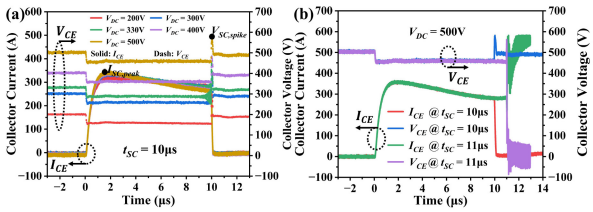

Fig. 10. (a) Short-circuit curves of FS-IGBT at t_{SC} = 10μs and different V_{DC} = 200V, 300V, 330V, 400V, and 500V. (b) Short-circuit curves of FS-IGBT at V_{DC} = 500V and different t_{SC} = 10μs, 11μs.

experiments, T_1 and T_2 were set to durations of 20μs and 7μs, respectively, to ensure that the short-circuit process of the DUT remained unaffected by the companion device. The initial conditions for the short-circuit test parameters are as follows: bus voltage V_{DC}= 400V, gate voltage V_G= 15V, gate resistance R_g= 10Ω, temperature T_C= 25°C, and short-circuit withstand time t_{SC}= 10μs. Furthermore, the companion device utilized is a 1200V 140A FS-IGBT, which exceeds the specifications of the DUT to ensure that it does not interfere with the DUT's short-circuit testing. Additionally, the parasitic inductance of the entire short-circuit test system is maintained at a low level, approximately 30nH, which exerts a negligible effect on the short-circuit test.

A. Bus Voltage V_{DC}

The short-circuit characteristics of the FS-IGBT were measured with the bus voltage set at 200V, 300V, 330V, 400V, and 500V. Fig. 10(a) indicates that as the bus voltage V_{DC} increases, both the collector voltage V_{CE} and the current rise rate of the device increase. Additionally, we investigated the extreme short-circuit withstand time t_{SC} at varying V_{DC} levels. As shown in Fig. 10(b), the FS-IGBT can safely turn-off within 10μs at V_{DC}= 500V, but when the short-circuit lasts up to 11μs, the device continues to increase the current after the turn-off until it burns out due to thermal runaway. Therefore, we obtained the short-circuit withstand time of the self-developed FS-IGBT at 500V bus voltage is 10μs.

The short-circuit withstand time t_{SC} and short-circuit energy E_{SC} of the FS-IGBT at different V_{DC} are summarized in Fig. 11(a), from which it can be found that the t_{SC} decreases with the increase of V_{DC}. This phenomenon occurs because, as V_{DC} increases, the energy loss in the device during the short-circuit process also increases, resulting in a more rapid increase in the junction temperature T_j of the device, which is confirmed in Fig. 11(b). The TCAD short-circuit simulation indicates that at V_{DC} = 500V, the internal temperature of the device at 4μs reaches the same level as that at 10μs under V_{DC} = 300V. Furthermore, when the short-circuit lasts for up to 10μs, the internal temperature of the FS-IGBT is significantly higher than that at a 300V bus voltage, which is more clearly illustrated in the longitudinal lattice temperature profile of the device shown in Fig. 11(c). The failure of FS-IGBTs results from the self-heating effect, which leads to thermal accumulation within the device, ultimately resulting in thermal runaway failure when the T_j exceeds the maximum junction temperature T_{jmax} of the intrinsic thermal breakdown limit [14].

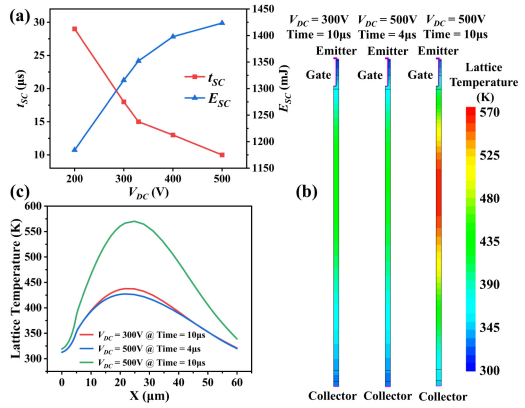

Fig. 11. (a) Curves of t_{SC} and E_{SC} as a function of V_{DC}. (b) Internal lattice temperature of FS-IGBTs for TCAD short-circuit simulation and (c) lattice temperature curves in the longitudinal direction of the device.

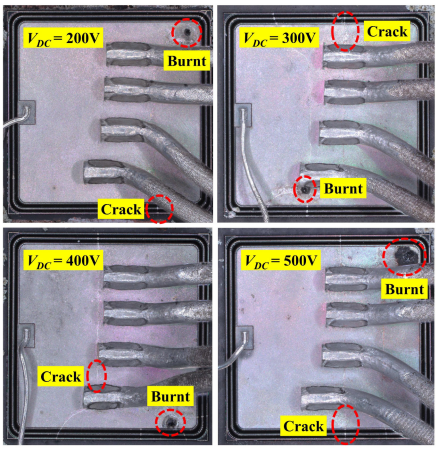

Fig. 12. Top view of decapsulated FS-IGBTs after short-circuit failure at different V_{DC}.

Fig. 12 illustrates device failure at various V_{DC} levels. Observations revealed that short-circuit failures were accompanied by distinct burn points and multiple cracks. Cracks in the device are attributed to burn points on one hand and thermal stresses at the bonding points on the other. This is because thermal stresses at the bonding points increase with temperature, potentially leading to cracking. Besides, we also found that as V_{DC} increases, the size of the burn point enlarges due to the increased E_{SC} of the device. Consequently, higher bus voltages result in shorter short-circuit withstand times for the FS-IGBT and reduced short-circuit ruggedness.

B. Gate Voltage V_G

To investigate the effect of gate voltage V_G on short-circuit capability, we tested the short-circuit curves of the devices at V_G= 12V, 14V, 15V, 16V, 18V, and 20V. Fig. 13(a) illustrates the short-circuit characteristics of the FS-IGBT at gate voltages of 14V, 15V, and 16V. The figure indicates that the collector current I_{CE} increases more rapidly with increasing V_G, with the peak value $I_{SC,peak}$ rising from 160A to 291A and then to 358 A. When the gate voltage exceeds 15V, significant voltage and current oscillations are observed in the short-circuit curve, as shown in Fig. 13(b). The oscillations of the gate voltage that occur during IGBT short-circuit are attributed to the rotation of the electric field within the device caused by the Kirk effect, which leads to continuous changes in the Miller capacitance. Dr. P. D. Reigosa conducted a detailed study on gate voltage oscillations during short-circuit conditions in the literature [27], [28].

As illustrated in Fig. 14, the internal electric field distribution of the FS-IGBT during short-circuit is compared at gate voltages of 15V and 20 V. It is observed that the electric field of the gate oxide at V_G = 20V is significantly greater than at 15V, indicating that a higher gate voltage increases the susceptibility of the gate oxide to breakdown under high collector voltage during short-circuit. Furthermore, in the device failure picture shown in Fig. 15(a), the failure at V_G = 20V is essentially identical to that in Fig. 12. From this, it can be inferred that oscillations at high gate voltages can exacerbate thermal runaway failures in the FS-IGBT.

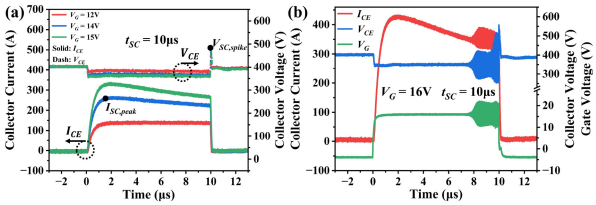

Fig. 13. (a) Short-circuit curves of FS-IGBT at t_{SC}=10μs and different V_G=12V, 14V, and 15V. (b) Short-circuit curves of FS-IGBT at t_{SC}=10μs and V_G=16V.

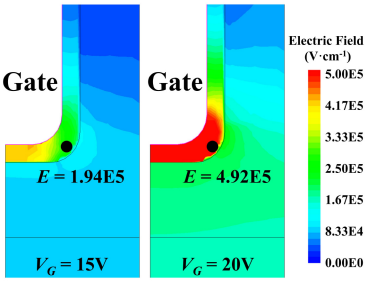

Fig. 14. Internal electric field distribution at different gate voltage V_G during the FS-IGBT short-circuit process.

Fig. 15(a) summarizes the variation of $I_{SC,peak}$, collector voltage spike $V_{SC,spike}$, and short-circuit withstand time t_{SC} with respect to V_G, where both $I_{SC,peak}$ and $V_{SC,spike}$ increase with rising V_G, while t_{SC} gradually decreases due to thermal runaway exacerbated by gate oscillations. Consequently, an increase in gate voltage can directly elevate both the short-circuit current and the short-circuit voltage spike, resulting in increased power consumption during the short-circuit process and subsequently reducing the short-circuit withstand time. Therefore, appropriately lowering the gate voltage can enhance the short-circuit ruggedness of the FS-IGBT.

C. Gate Resistance R_g

Fig. 16 illustrates the short-circuit test curves of the FS-IGBT with varying gate resistance R_g values ranging from 2Ω to 30Ω. As shown in Fig. 16(a), a smaller R_g corresponds

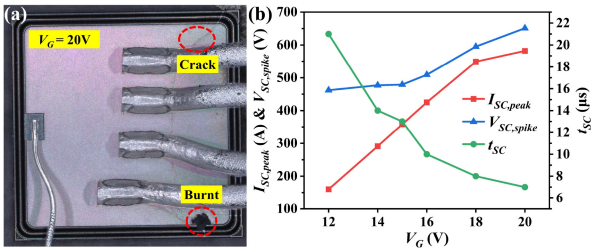

Fig. 15. (a) Top view of decapsulated FS-IGBTs after short-circuit failure at V_G = 20V. (b) Curves of $I_{SC,peak}$, $V_{SC,spike}$, and t_{SC} as a function of V_G.

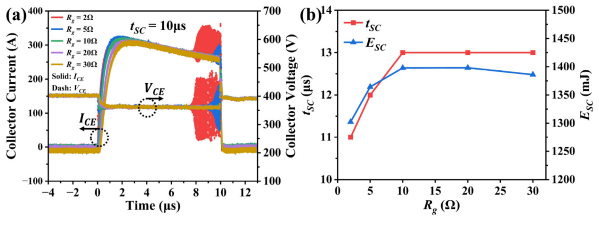

Fig. 16. (a) Short-circuit curves of FS-IGBT at t_{SC}=10μs and different R_G=2Ω, 5Ω, 10Ω, 20Ω, and 30Ω. (b) Curves of t_{SC} and E_{SC} as a function of R_G.

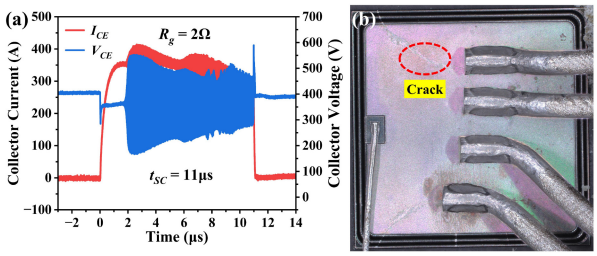

Fig. 17. FS-IGBT at R_g = 2Ω and t_{SC} = 11μs with (a) short-circuit failure curves and (b) top view of decapsulated after short-circuit failure.

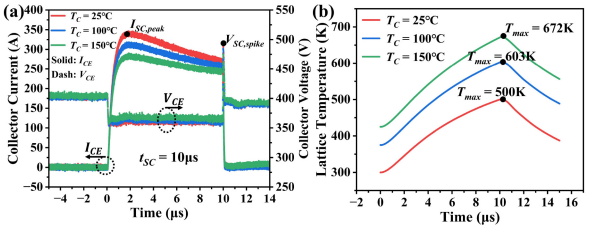

Fig. 18. (a) Short-circuit curves and (b) simulate internal lattice temperature of FS-IGBT at t_{SC} =10μs and different temperature T_C = 25°C, 100°C, and 150°C.

to a higher current rise rate. When R_g decreases to 5Ω or lower, gate oscillation re-emerges, indicating that appropriately increasing gate resistance can effectively mitigate gate oscillation in the FS-IGBT during short-circuit conditions. This finding is also corroborated by literature [27]. Further testing of the device's extreme short-circuit capability reveals its corresponding short-circuit withstand time t_{SC} and short-circuit energy E_{SC} at various gate resistances, as illustrated in Fig. 16(b). From this figure, it is observed that the t_{SC} and E_{SC} of the FS-IGBT are nearly independent of R_g. The reason for the device's t_{SC} being less than 13μs at R_g= 2Ω and R_g = 5Ω is that current and voltage oscillations caused by strong gate oscillation lead to premature device failure.

As illustrated in Fig. 17, the significant oscillations at R_g= 2Ω result in an early thermal runaway of the FS-IGBT, and the observed cracking phenomenon on the chip surface aligns with the varying V_{DC} and V_G failures discussed in the previous section. Consequently, gate resistance has minimal impact on the short-circuit withstand time and ruggedness of the FS-IGBT.

D. Temperature T_C

Temperature has a significant impact on power semiconductor devices, particularly on the short-circuit capability of FS-IGBTs. As shown in Fig. 18(a), the short-circuit current I_{SC} of the device decreases continuously as the temperature T_C rises from 25°C to 150°C. This phenomenon occurs because high temperatures increase the internal junction temperature, resulting in decreased carrier mobility and increased internal resistance, ultimately reducing the I_{SC}. Simulations of the FS-IGBT's internal lattice temperature confirm that as the T_C increases, the lattice temperature of the device also rises during the short-circuit process. By the 10th μs of short-circuit turn-off, the maximum lattice temperature rises from 500K at 25°C to 672K at 150°C, as illustrated in Fig. 18(b).

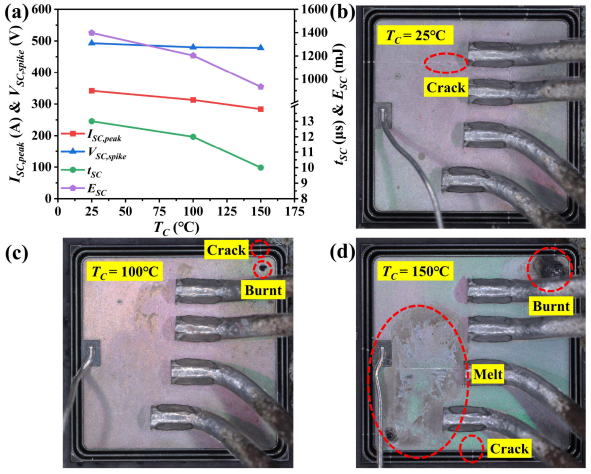

Fig. 19. (a) Curves of $I_{SC,peak}$, $V_{SC,spike}$, t_{SC} and E_{SC} as a function of T_C. (b)(c)(d) top view of decapsulated FS-IGBTs after short-circuit failure at different T_C = 25°C, <FC>100°C, and 150°C.

Not only do the short-circuit peak current $I_{SC,peak}$ and short-circuit spike voltage $V_{SC,spike}$ decrease as the T_C increases, but testing the extreme short-circuit capability also reveals that the short-circuit withstand time t_{SC} and short-circuit energy E_{SC} of the FS-IGBT both decrease as the T_C increases, as shown in Fig. 19(a). Additionally, as shown in Fig. 19(b), (c), and (d), as the temperature continues to rise, device failure progresses from a single crack to small burn points, then to large burn points and the melting of the metallic aluminum layer. The ultimate failure of the device is attributed to thermal runaway, resulting from

TABLE II
EFFECT OF CIRCUIT PARAMETERS ON SHORT-CIRCUIT OF THE FS-IGBT

Circuit Parameters	$I_{SC,peak}$	$V_{SC,spike}$	E_{SC}	t_{SC}	*Ruggedness*
Bus Voltage $V_{DC}\uparrow$	—	↑	↑	↓	↓
Gate Voltage $V_G\uparrow$	↑	↑	↑	↓	↓
Gate Resistance $R_g\uparrow$	↓	—	—	—	—
Temperature $T_C\uparrow$	↓	—	↓	↓	↓

internal heat accumulation. Consequently, elevated temperatures reduce the short-circuit ruggedness and the short-circuit withstand time t_{SC} of the FS-IGBT. Enhancing the device's heat dissipation capabilities in applications can effectively improve short-circuit ruggedness and enhance the device's reliability.

IV. CONCLUSION

This paper begins with the design of a 650V, 75A FS-IGBT using TCAD simulation. By introducing three cell structures and designing various layouts, we selected the optimal cell topology based on short-circuit withstand time and saturation on-state voltage. The FS-IGBT was successfully fabricated and packaged in a TO-247 type through a carefully designed manufacturing process. Experimental testing of the device's static characteristics revealed a saturation on-state voltage of 1.65V and a forward blocking voltage of 800V, meeting the design requirements. Subsequently, we evaluated the short-circuit characteristics of the FS-IGBT and conducted a comprehensive analysis of how circuit parameters influence its short-circuit capability. The experimental results indicate that the bus voltage V_{DC}, gate voltage V_G, and temperature T_C significantly affect the short-circuit capability of the FS-IGBT. Therefore, the short-circuit ruggedness and withstand time can be improved by appropriately decreasing V_{DC}, V_G, and T_C. Although gate resistance R_g affects the peak current during short-circuit conditions, it has a negligible impact on the short-circuit ruggedness and withstand time of the FS-IGBT. Further detailed information regarding the impact of circuit parameters on short-circuit capability is provided in Table II.

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