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A Fully Integrated Adaptive-MPP-Shifting Rectifier for Piezoelectric Energy Harvesting Outputting 580μW at 10V-V_{OC}

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Piezoelectric energy harvesting (PEH) has become a promising alternative to conventional batteries for powering wireless sensors and edge computing devices. Among various rectifier topologies for PEH, synchronized bias-flip rectifiers, such as parallel synchronized switch harvesting on inductor (SSHI) [1] and capacitors (SSHC) rectifiers [2], have garnered significant attention in recent years due to their higher output power if the optimal output voltage is reached. A typical structure of a bias-flip rectifier and its output power related to the rectifier's output voltage (V_{REC}) are shown in Fig. 1 (left). As the V_{REC} changes, a distinctive peak power exists, signifying the maximum power point (MPP) [3-5]. At this point, V_{REC} is at its optimal value, expressed by $V_{MPP}=V_{OC}/(1-\eta_F).V_{OC}$ is the open circuit voltage amplitude of a piezoelectric transducer (PT), typically between 1V and 10V under most real-world excitation levels, and η_F is the flipping efficiency of a bias-flip rectifier. To track and maintain the rectifier's output power at the MPP, an MPPT (Maximum Power Point Tracking) block is needed after the rectifier to regulate V_{REC}. While most prior designs have been mainly focused on increasing η_F, usually over 60%, for greater output power [6-16], the theoretical V_{MPP} can easily go higher than the breakdown voltage (5V) of standard CMOS devices if V_{OC} is higher than 2V. As a result, the reachable MPP still stays at 5V to protect the chip, with a much lower output power than the theoretical MPP. Though LDMOS devices allow V_{REC} to track higher V_{MPP}, the resulting high V_{REC} introduces high-voltage pressures and large voltage step-down ratios for the following power-conditioning stages. This has been an unsolved challenge limiting the output power of all CMOS bias-flip rectifiers since it was first introduced at ISSCC'2009 [1].

To address the abovementioned challenge, this paper proposes a fully integrated bias-flip rectifier with an adaptive MPP shifting scheme. It shifts the V_{MPP} to under 5V with an adaptive shifting ratio without sacrificing the peak power. By doing so, the rectifier can reliably reach the MPP in a wide range of V_{OC}. As shown in Fig. 1 (top right), the PT is modeled as an AC current source (I_P) in parallel with the intrinsic capacitor (C_P). The proposed rectifier comprises 4 on-chip flying capacitors (C_{F1}-C_{F4}) of 250pF each, with four operation modes (Φ_1-Φ_4) depending on the theoretical MPP, as shown in Fig. 1 (bottom-right). In Φ_1, when theoretical MPP is below 5V under lower V_{OC}, the V_{MPP} remains unshifted. During this mode, C_{F1}-C_{F4} are connected in parallel to transfer energy from C_P to the storage capacitor (C_S) while regulating V_{PT} (voltage across C_P) at the V_{MPP}. When vibration excitation becomes stronger, V_{OC} increases, and the theoretical V_{MPP} may go higher than 5V and no longer be tracked. To track the MPP, the modes Φ_2, Φ_3, or Φ_4 are engaged to lower the effective V_{OC} connected to the rectifier by 2X, 3X, and 4X, respectively. As a result, the V_{MPP} is left-shifted by 2X, 3X, and 4X, respectively, so it goes lower than 5V and is tracked again by the on-chip MPPT circuit within the breakdown voltage range. This design only employs up to 4X MPP shifting for verifications; hence, it can only work for theoretical V_{MPP} under 20V, which fits most applications. High MPP shifting ratios can be achieved if more modes are employed.

Fig. 2 (top left) compares the output power of the proposed MPP-shifting rectifier with that of a conventional bias-flip rectifier and a full-bridge rectifier (FBR). While the power from a conventional bias-flip rectifier and an FBR increase linearly to V_{OC} after V_{MPP} is limited to 5V, the power from the proposed rectifier keeps increasing quadratically to V_{OC} due to the always-tracked MPP. Fig. 2 (top right) shows the system's operational flowchart. When the system starts, the rectifier enters a startup phase to sample the vibration period (T) to find the first bias-flip moment. Then, a fully digital duty-cycle-based (DCB) MPPT block regulates V_{PT} at V_{MPP} by letting V_{PT} build up for T/4, corresponding to 50% rectifier conduction duty. To regulate V_{PT}, a DC-DC conversion is activated to transfer energy from C_P to C_S, and it starts from mode Φ_4 with a 4X MPP shifting ratio to protect the system. During the DC-DC conversion, the optimal mode is adaptively chosen. If the voltage across the capacitor C_{F4} (V_{F4}) is much lower than 5V, it means a smaller MPP shifting ratio can be chosen, and it is decreased by 1 (from Φ_i to Φ_{i-1}) until V_{F4} is close to 5V or it is already in Φ_1. If V_{OC} increases such that V_{F4} exceeds 5V, the mode is reset to Φ_4 to protect the circuit and restart the mode determination process.

The PT voltage is bias-flipped at the zero-crossing moment of I_P. The number of flipping phases, 2(i-1)+1, depends on the current mode (Φ_i). For example, in Φ_4, there are 7 flipping phases (P_1-P_7), as shown in Fig. 2 (bottom). From P_1 to P_3, C_{F1}-C_{F4} are connected in different configurations to transfer as much energy as possible from C_P to C_S. In each phase, two non-overlapping sub-phases are driven by an on-chip generated 14MHz clock. During P_4, the remaining charge across C_P is cleared. In the last 3 phases ($P_{5\text{-}7}$), the charge is transferred from C_S back to C_P in a sequence reverse to $P_{1\text{-}3}$. The durations of the phases are adaptively adjusted according to V_{OC}. When the V_{OC} increases, the phases $P_{1\text{-}2}$ and $P_{6\text{-}7}$ need more clock periods for complete energy transfer due to the higher energy stored in C_P. As a result, $P_{1\text{-}2}$ and $P_{6\text{-}7}$ have longer durations compared to the intermediate phases in the waveform.

Fig. 3 top shows the system architecture. The key blocks include a mode (Φ_i) configuration block, a bias-flip rectification block, a power switch logic block with switch drivers, and a power stage. The Φ_i configuration block sets Φ_i based on the position of the theoretical MPP. The mode is decided by the results of comparing the breakdown voltage (V_{Break}), usually 5V, and V_S with the voltage across C_{F4} (V_{F4}). After determining the mode Φ_i, the C_P-to-C_S DC-DC conversion operates in a constant on-time mode, driven by an on-chip oscillator (OSC_2) of 2MHz. The bias-flip rectification block is designed to flip the PT voltage. It sets a threshold voltage (V_{SH}) slightly lower than a divided value of V_{PT} for flipping. If a divided V_{PT} is lower than V_{SH}, a synchronized signal (*Syn*) generates a rising edge, and a counter-composed pulse generation (CNT PG) block generates P_1-P_7 phases and all sub-phases to flip V_{PT} driven by an on-chip 14MHz clock (OSC_1), only activated during the flipping time. The hysteresis comparator (Hys) sets a window for regulating V_{PT} at V_{MPP}. All the resulting signals are fed to the power switch logic block to generate switching signals to drive the power stage to perform C_P-to-C_S energy transfer and V_{PT} voltage flipping. The power stage consists of four on-chip MIM capacitors of 250pF each, four 20-V LDMOS switches (S_1-S_4), and ten 5-V standard CMOS switches (S_5-S_{14}). Fig. 3 bottom shows the fully digital DCB MPPT block. It is driven by the *Syn* signal and samples the vibration period by a 16-bit counter. Then, the half period is stored in two registers at each rising edge of the *Syn* signal. The stored numbers are averaged to give an accurate MPP moment. The driver for the back-to-back switches is shown in Fig. 3 (bottom-right).

The proposed chip was fabricated in a 180nm BCD process. A commercial PT (S129-H5FR-1803YB) with C_P=23nF is excited at its measured resonant frequency f_P=100Hz. Fig. 4 top-left shows measured startup, and V_{PT} is flipped after sampling a few vibration periods. The zoomed-in waveforms in one vibration period are given in Fig. 4 top middle, showing energy extraction (DC-DC) and V_{PT} bias-flipping phases. During the bias-flip process, the energy in C_P is transferred to C_S with the on-chip flying capacitors, causing V_S to rise. Then it transfers from C_S back to C_P in a reversed polarity, resulting in a partially flipped V_{PT} and a decrease in V_S. Though the flip efficiency is only around 60%, the energy extraction performance is not much affected due to some energy stays in C_S, causing slightly increased V_S after the bias-flip process. The zoomed-in bias-flip period, flipping phases, and sub-phases are shown at the bottom. Fig. 4 (top right) shows that V_{PT} is regulated at the V_{MPP} by transferring harvested energy to C_S.

Fig. 5 top shows the output power versus V_S with V_{OC} at 7V and 10V. The peak output power of the proposed rectifier is 307.8μW and 580.4μW, which are 1.28× and 1.6× enhancements, respectively, compared to a conventional bias-flip rectifier when V_S=5V, thanks to the left-shifted MPP. In contrast, conventional designs cannot reach the MPP due to the high V_{OC}. When Vs is lower, the power enhancement compared with a conventional bias-flip rectifier is higher, for instance, increasing to 2.15× and 2.7× respectively when V_S=2V. The output power versus V_{OC} is shown in the bottom left. As V_{OC} increases, the proposed rectifier exhibits a quadratic power output, whereas the output power of the traditional bias-flip rectifier stays linear. The bottom right figure presents the figure of merit (FOM), defined as $P_{IC\text{-}MAX}/(C_P f_P)$, where $P_{IC\text{-}MAX}$ is the maximum output power, and C_P and f_P linearly affect the $P_{IC\text{-}MAX}$. The x-axis represents the flying capacitors required in previous capacitor-based rectifiers. The figure illustrates that prior designs either exhibit a low FOM or necessitate the use of bulky off-chip capacitors, while the proposed design achieves an outstanding FOM using in-total 1nF on-chip capacitors. The table in Fig. 6 compares the proposed work with prior works. With the proposed MPP-shifting technique, high excitation (high V_{OC}) energy can be efficiently extracted with small on-chip capacitors. The chip micrograph is shown in Fig. 7.

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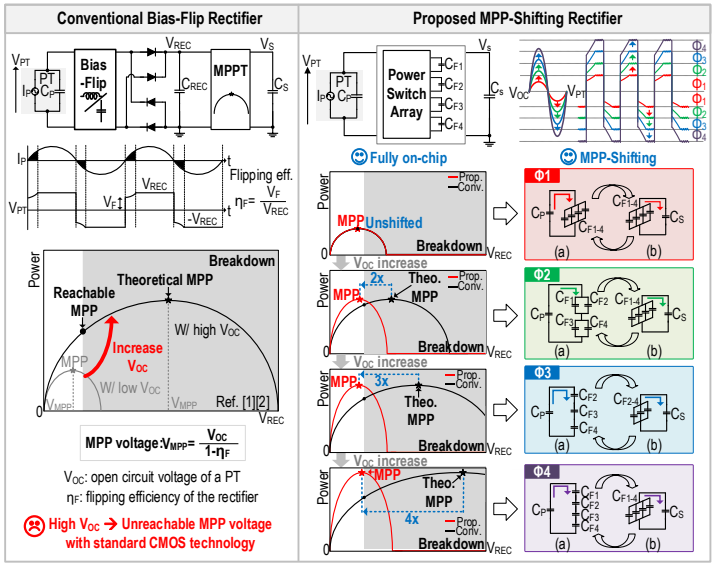


Fig. 1. Output power comparison of a conventional bias-flip rectifier (left) and proposed rectifier (right) when the open circuit voltage (V_{OC}) is increased.

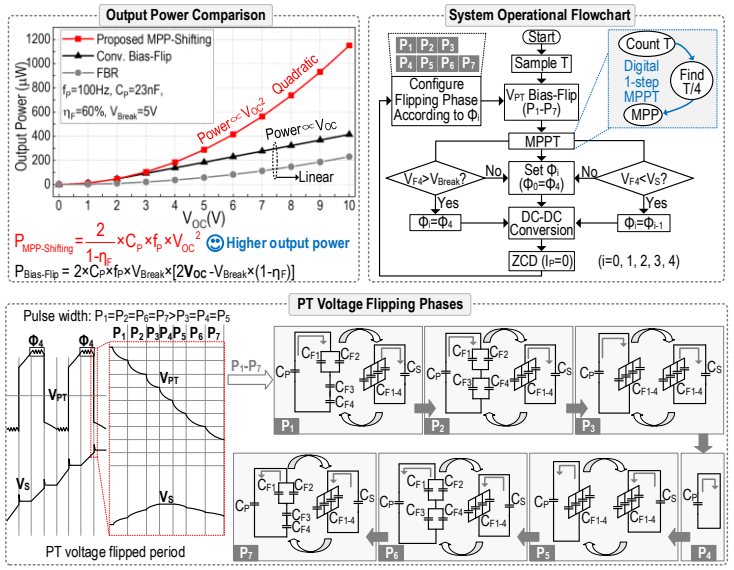


Fig. 2. Power comparison of the proposed rectifier and a bias-flip rectifier (top left), system operational flowchart (top right), and V_{PT} flipping phases (bottom).

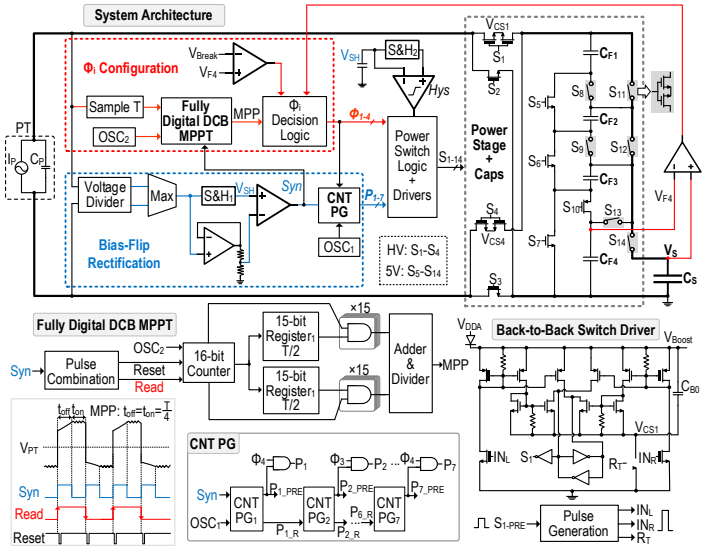


Fig. 3. System architecture of the proposed MPP-shifting rectifier (top), MPPT block, and digital PG block, and details of back-to-back switch driver (bottom).

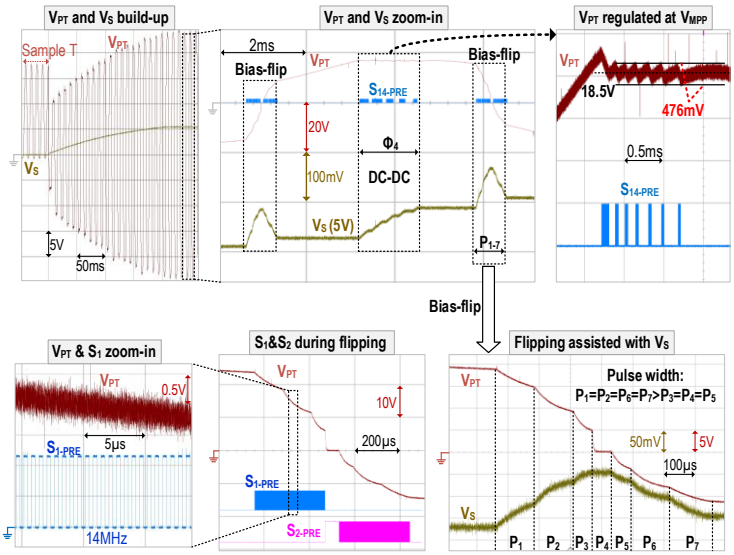


Fig. 4. PT voltage and storage voltage build-up process (top left) and related zoom-in waveforms (top middle, right); PT voltage flipping zoomed-in figures (bottom).

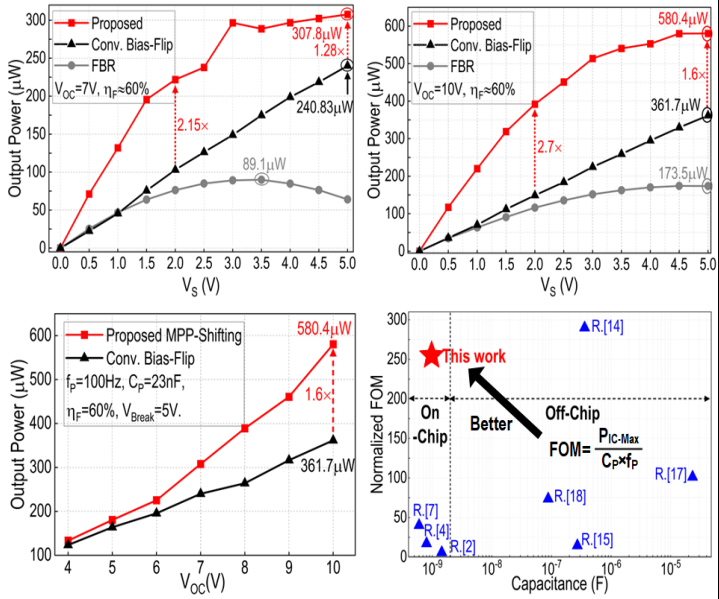


Fig. 5. Output power of the proposed rectifier and conv. bias-flip rectifier with 7V-V_{OC} and 10V-V_{OC} (top); different output power levels by changing V_{OC} and FOM comparison (bottom).

	ISSCC'09 [1]	ISSCC'17 [2]	JSSC'20 [7]	JSSC'23 [4]	ISSCC'23 [5]	ISSCC'23 [6]	This Work
Technology (μm)	0.35	0.18	0.18	0.18	0.18	0.18	0.18
Harvester Type	Mide V22b	PSI-5A4E	Customized	PZT5A	S128-1107YB	PPA 1011	S129-H5FR-1803YB
Harvesting Strategy	SSHI	FCR	SSHC	SECE	SSHI	SSHI	Switched-Cap +SSHC
C_P (nF)	12	0.0784	6	28.8	42	100	23
f_P (Hz)	225	110k	22	57	230	130	100
MPPT Tech.	No	No	No	P&O	DCB	No	DCB
1-Step MPPT	No	No	No	No	No	No	**Yes**
Key Component (Features)	Off-chip 820μH inductor (Flipping)	On-chip 1.44nF cap (Flipping)	On-chip 600pF cap (Flipping)	On-chip 800pF cap (Charge extraction)	Off-chip 120μH inductor (Flipping &MPPT)	Off-chip 10μH inductor (Flipping &MPPT)	**On-chip 1nF cap (Flipping &MPPT)**
Achievable MPP (V_{MPP})	No	Yes (2.2V)	No	Yes (2V)	No	No	**Yes (24V)**
Max V_{OC} (V)	2.4	1.2	2.34	1.8	2.0	2.0	**10**
Max Output Power (μW)	68	50.2	5.3	28	272.5	441	**580.4**
P_{IC}/P_{FBR}@V_{OC}	1 @2.4V	4.78 @2.2V	6.71 @2.34V	5.75 @2V	7.38 @2V	11.7 @1V	**3.34 @10V**
$P_{IC}/P_{Bias-Flip}$	-[1]	-[1]	-[1]	-[1]	-[1]	-[1]	**1.6×(V_S=5V) 2.7×(V_S=2V)**
FOM[2]	25.18	5.82	2.16	17.06	28.2	33.92	**252.35**

1: Not applicable. 2: Normalized FOM = $P_{IC-Max}/(C_P \times f_P)$.

Fig. 6. Comparison table between the proposed work and prior arts.

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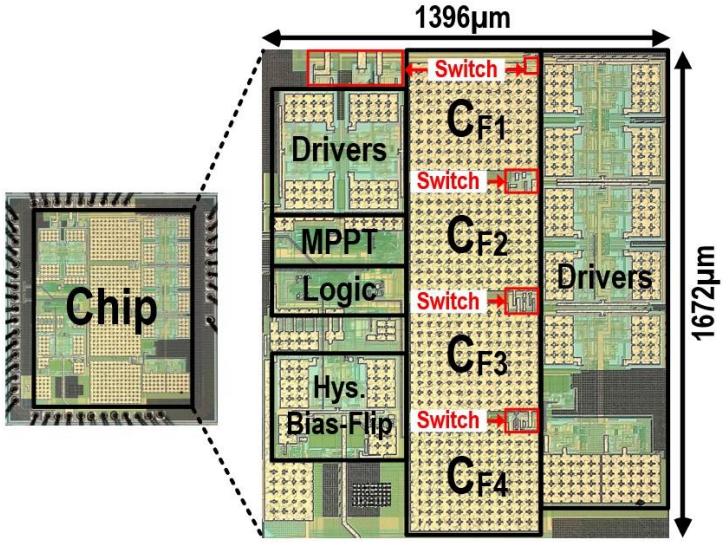


Fig. 7 Diephoto

References

[1] Y. K. Ramadass, et al., "An efficient piezoelectric energy-harvesting interface circuit using a bias-flip rectifier and shared inductor," *ISSCC*, 2009, doi: 10.1109/JSSC.2009.2034442.

[2] Z. Chen, et al, "Fully Integrated Inductor-Less Flipping-Capacitor Rectifier for Piezoelectric Energy Harvesting," *JSSC*, 2017, doi: 10.1109/JSSC.2017.2750329.

[3] S. Bandyopadhyay et al., "Platform architecture for solar, thermal and vibration energy combining with MPPT and single inductor," *VLSI*, 2011, https://ieeexplore.ieee.org/document/5986054.

[4] C. Xie, et al, "Fully Integrated Frequency-Tuning Switched-Capacitor Rectifier for Piezoelectric Energy Harvesting," *JSSC*, 2023, doi:10.1109/JSSC.2023.3261301.

[5] X. Yue, et al, "An MPPT-Integrated Bias-Flip Rectifier for Piezoelectric Energy Harvesting,"*ESSERC*, 2024, doi: 10.1109/ESSERC62670.2024.10719584.

[6] Y. -W. Jeong, et al, "30.1 A Scalable N-Step Equal Split SSHI Piezoelectric Energy Harvesting Circuit Achieving 1170% Power Extraction Improvement and 22nA Quiescent Current with a 1µH−to−10µH Low Q Inductor," *ISSCC*, 2023, doi: 10.1109/ISSCC42615.2023.10067389.

[7] P. Angelov, et al., "A Fully Integrated Multilevel Synchronized-Switch-Harvesting-on-Capacitors Interface for Generic PEHs," *JSSC*, 2020, doi: 10.1109/JSSC.2020.2979178.

[8] J. Sankman, et al., "A 12-µW to 1.1-mW AIM Piezoelectric Energy Harvester for Time-Varying Vibrations With 450-nA I_Q," *TPEL*, 2015, doi: 10.1109/TPEL.2014.2313738.

[9] A. Quelen, et al, "A 30nA quiescent 80nW-to-14mW power-range shock-optimized SECE-based piezoelectric harvesting interface with 420% harvested-energy improvement," *ISSCC*, 2018, doi: 10.1109/ISSCC.2018.8310228.

[10] C. Wang, et al., "A 0.24mm2 Bridge-less Hybrid SSHI Interface Circuit for Piezoelectric Energy Harvesting with a Wide Load Range and Up to 1620% Power-Extraction Improvement," *CICC*, 2023, doi: 10.1109/CICC57935.2023.10121268.

[11] A. Morel *et al.*, "A Shock-Optimized SECE Integrated Circuit," *JSSC*, 2018, doi: 10.1109/JSSC.2018.2868299.

[12] M. Shim, et al., "Self-Powered 30 µW to 10 mW Piezoelectric Energy Harvesting System With 9.09 ms/V Maximum Power Point Tracking Time," *JSSC*, 2015, doi: 10.1109/JSSC.2015.2456880.

[13] A. Morel *et al.*, "Fast-Convergence Self-Adjusting SECE Circuit With Tunable Short-Circuit Duration Exhibiting 368% Bandwidth Improvement," *SSCL*, 2020, doi: 10.1109/LSSC.2020.3012340.

[14] S. Du et al., "An Inductorless Bias-Flip Rectifier for Piezoelectric Energy Harvesting," *JSSC*, 2017, doi: 10.1109/JSSC.2017.2725959.

[15] Z. Chen, et al, "Piezoelectric Energy-Harvesting Interface Using Split-Phase Flipping-Capacitor Rectifier With Capacitor Reuse for Input Power Adaptation," *JSSC*, 2020, doi: 10.1109/JSSC.2020.2989873.

[16] S. Javvaji, et al., "Analysis and Design of a Multi-Step Bias-Flip Rectifier for Piezoelectric Energy Harvesting," *JSSC*, 2019, doi: 10.1109/JSSC.2019.2917158.

[17] X. Yue et al., "A Synchronized Switch Harvesting Rectifier With Reusable Storage Capacitors for Piezoelectric Energy Harvesting," *JSSC*, 2023, doi: 10.1109/JSSC.2023.3260145.

[18] Z. Li *et al.*, "Piezoelectric Energy Harvesting Interface Using Self-Bias-Flip Rectifier and Switched-PEH DC–DC for MPPT," *JSSC*, 2024, doi: 10.1109/JSSC.2023.3341865.

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