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Development of silt measuring methods

Electronic Signal Processing :

A second generation acoustic measuring system

Research report

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delft hydraulics

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A second generation acoustic measuring system

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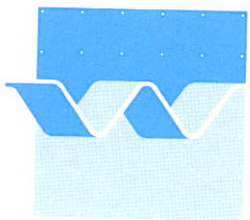

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SUMMARY

This report gives a description of the redesign of the acoustic attenuation and scattering measuring system for silt and sand particles in suspension.

The redesign was necessary because many ad hoc solutions had been accepted in the development of the first generation measuring system.
This limited its accuracy and possibilities, especially in the light of new techniques that became available later.

The new design follows a modular design, which means that each function has been realized on a separate board. This offers several advantages. For example, similar acoustic instrumentation can be realized, using the modules of the present system. Also it will be relatively easy to extend the system to meet future requirements.

The various chapters describe different system boards.
Chapters 2 and 5 have mainly been written by G.J. Dorenbos, who also designed these boards.
The majority of the hard and software bas been realized by N. Berkhoudt.

CONTENTS

1. System for acoustic attenuation and scattering particle suspensions measurements

1.1 Introduction.

A redesign of the first generation measurement system for attenuation and scattering measurements on particle suspensions, described in [1], has become necessary because the electronics includes a large number of ad hoc solutions.
Although the present system has functioned reasonably well, and it still does, new components have become available, which enable a new approach to the design.
Also, the experience and knowledge gained during the development of the first generation system, was of great value to the realization of a redesign.
The new system has a significantly better performance and is better serviceable.
The newly developed software for the system is menu driven. Also, a testprogram has been developed to supply selftesting facilities.
The new system is more accurate, for example due to the incorporation of lookup tables with measured values instead of using nominal values. It also has a larger dynamic range.
The approach chosen is flexible, in the sense that it will be possible to implement a number of future requirements, that can be anticipated now.

Some of the main improvements are the following.

- The introduction of a Software Programmable Gain Amplifier (SPGA).
  This amplifier is controlled by a DAC, so there is no need for mechanical switches (relays) to set the signal level.
- In combination with a programmable attenuator the dynamic range of the system has been increased significantly.
- A new timing board has been developed. It has 8 fully independent programmable outputs. The resolution is 100 ns and has a programming range up to several milliseconds.

- A synchronization board makes it possible to switch the burst on and off at the zero crossings. The burstlength is programmable over a wide range (from a 0.1 µs to 4 ms).
- A different transducer selection configuration has been chosen. The number of relays in the signalpath has been reduced to 2. (in the old situation it was from 2 to 7).
- A new kind of connectors has been used, the so called SMB (sub click). These connectors were chosen because of there small size, so the system becomes more compact, and because of good specifications in the required frequency range.

A block diagram of the system is shown in Figure 1.1.

Further we can think of other applications of the new system like burst backscatter measurements or broadband pulses transceivers. Some minor changes will enable the system to measure these modes.

1.2 Block diagram

A global discussion of the block diagram Figure 1.1 is given here. A detailed description of each block is postponed to the later chapters.

First, a single frequency is obtained from a synthesizer, Philips PM5390. This RF signal is fed to a synchronization board which produces a burst with a specified burstlength. The amplitude of the burst is controlled by a programmable attenuator.
In case of a 'REAL' measurement a Power Amplifier (PA), with a maximum output of 10 Watts, supplies a burst to the transducer which is selected by the relay selector. The relay selector also selects the receiving transducer, scattering or transmission.
The receiving transducers are provided with a SMD pre-amplifier.
The amplifier power supply is obtained over the coax, so a bias network is necessary to couple the DC and RF voltages.
When a 'REFERENCE' measurement is selected the PA and transducers are bypassed.
Next a Software Programmable Gain Amplifier SPGA (Gain programmable from 0 dB to 30 dB), amplifies the received burst to a level which can be processed by the detection electronics.
Then, in case of low frequency detection, a second bypass connects the output of the amplifier directly to the input of the detection board. In the other case, high frequency detection, the received burst will be mixed to an Intermediate Frequency (IF) of
10.7 MHz. A synthesized local oscillator assures a correct IF.
The detector is necessary to allow very short bursts (2 µS) be detected by the ADC (DT2801).
The timing of the whole system is controlled by a timing board. The timing is independent of the computer, so it is not influenced by the computer.
For independent triggering a DMA-trigger board is added, to enable that the computer can work under DMA.

2 MBus - MetraByte Bus.

2.1 Introduction.

In the first generation measuring system for particle suspensions, different types of digital I/O were used:

1- IEEE/GPIB for instrument setting and control.
2- MetraByte (MB) 3 x 8 bits parallel,
   one MB-board for output, one for input.
3- a logic interface to multiplex the MetraByte output-signals and address the output-devices. (relays, send/receive selector, timing-circuit).
4- DT2801A 16 bits parallel I/O.

In the new design all digital I/O is reduced to one bus, called MetraByte bus.
The aim of the MetraByte bus (MBus) is to do all digital I/O for the devices with one MetraByte board. All devices will have an addressable interface. Although it would be possible to use the GPIB-interface for all the digital I/O, the MBus is preferred because of the low costs and ease of use (programming).
The DT2801A digital I/O is not used for the same reason.

The MBus-system consists of three parts:
- the Metrabyte board,
- the MBus-driver,
- the device-interface.

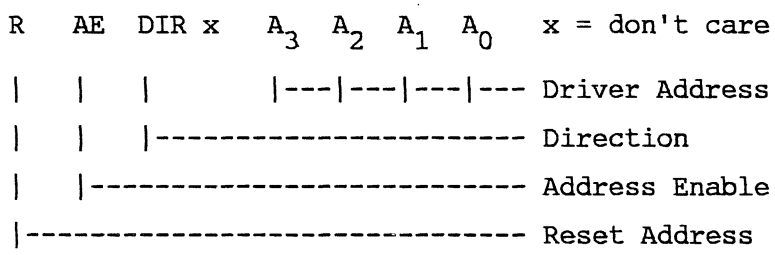
Each part will be described in the next chapters.

2.2 Metrabyte board.

The MetraByte board is an interface board (for PC) based upon the 8255 PPI (Programmable Peripheral Interface). The 8255 has four ports, port A, B, C and a internal control port which can be accessed by reading/writing to the four corresponding I/O-address locations.
Port A, B and C can be configured as input or output. The configuration of port A, B and C is set with the control-port. In this application port C will always be output, port A and B input or output.
A description of the MetraByte board is included in
Figure 2.1.1.

2.3 MBus Driver.

The MBus driver is designed to increase the output capability of the MetraByte board. The driver is configured as a device-interface with address 0, so no DIP switches are added.
The 74HCT245 is a bidirectional bus driver. This IC can programmed for output or input. The control signal is provided via the C port.

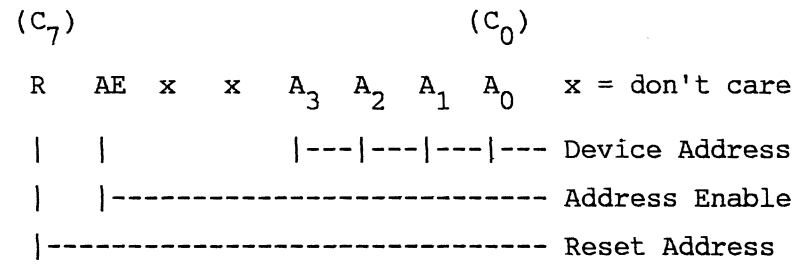


If DIR (Direction) is low the driver is in output-mode, if DIR is high the driver is in input-mode (input A,B, output C). Note that the MetraByte board must be configured for input or outputmode by writing to the controlport.
Figure 2.3.1 shows the circuitdiagram of the MBus driver.

The MBus driver is build with SMD (Surface Mounted Devices) techniques to provide a small outlined interface, which can be plugged directly on to the connector of the computer.
The layouts of the PCB are given in Figures 2.3.2 and 2.3.3.

2.4 Device Interface.

Port A and B can be used for both output to and input from devices, while port C contains control signals (or output). The contents of port C :



To address the device AE (Address Enable) must be set high. If the address $A_0..A_3$ equals the address set by a DIP-switch the device is addressed until the device is unaddressed.
The AE and the address can be set at the same time. A hardware delay ensures a correct timing of the selected device. Unaddressing is possible either by addressing another device or by pulsing R (Reset address). Once addressed, $C_0..C_5$ can be used as device-specific output. Figure 2.4.1 shows an example of a basic interface.

3 Backplane for device interconnections

In Figure 3.1 the layout of the backplane is shown. This backplane is used to connect the MBus,the powersupply and some other internal control signals to the devices.
A 64 pole connector is used to connect the devices to the backplane.

Digital ground and Analog ground should not be connected to each other on any device (only on the termination board see next chapter).
The analog ground is a 4 wire parallel structure to obtain a low impedance ground.

All MBus lines are available on the backplane. Also all eight outputs from the timing board.
The power supply is coupled on the backplane with the termination board.

4 The MBus Termination board

To ensure proper working of the MBus when more then one device is connected, it is not only necessary to use the previously described interface, but also the bus has to be terminated to prevent reflections. These reflections could cause unwanted triggers or mutilate the data.
In this case the power saving HCT termination is used instead of the TTL termination, see Figure 4.1 and 4.2.
The termination board monitors also the presence of the power supplies, the ± 5 V, ± 15 V and the 30 V.
Also the board has a connector for the MBus Interface, and the board couples the MBus with the backplane.
In most of the devices the analog and digital ground are separated. This is to avoid that spikes, caused by the digital circuits, affect the analog circuits. For proper working the digital and analog ground must be connected to each other in a starpoint configuration. This is done on the termination board.
On the front is a pushbutton. This button enables a lamptest. All LED's of the devices connected on the MBus should light up when this button is pressed, although there are few who will not.
In Figure 4.3 the schematics of the termination board is given.

5 Programmable timer

5.1 Introduction.

The programmable timer generates timing and control signals for each transducer pair. For each transducer pair two separate timing configurations are available; one for a real measurement and one for a reference measurement. Once programmed only pair-number and measurement type are needed to get the correct timing. The timer starts a timing cycle on a hardware or software trigger.

The main components of the timer are:
- static RAM memory to store the timing data.
- an 11 bits binary counter.
- an interface to control and program the timer.

The main principle of the programmable counter is that 8 output signals are created by creating a series of output bytes. The time an output-byte appears depends on the corresponding counter-value.
A blockdiagram in Figure 5.1.1 shows the main components of the timer.
A detailed description of the timer will be given in the next chapters.

5.2 RAM.

Static RAM (2k x 8 - 35 nS) is used in the timing-circuit. A data sheet of this RAM is shown in Figure 5.2.1. Three RAM's are used parallel, so 2k of 24 bits is available with an access-time of 35 nS. Nine address-lines (from the 11 available ones) are used:

$A_{0..3}$ = Space for timing-data for a single transducer-pair.

$A_{4..7}$ = Transducer number.

A_8 = real/reference measurement.

So timing values for 16 transducerpairs can be stored in the RAM.
The 24 bits stored on a single address contain:

8 bits output;
11 bits counter value;
1 bit COT (Count On Trigger) to enable triggering.
4 bits indicating 4 lowest bits of next address.

The address can be configured in two ways:

- full address from interface to program a memory location or to preset the timer to any address.
- partial address from interface ($A_{4..8}$) and partial address from NextAddress-bits in RAM ($A_{0..3}$).

The latter is the normal way of addressing. Each time the counter reaches zero, the next address will be latched in the address-latch. This is an easy and flexible way to allow all kinds of output patterns. At the end of an pattern the NextAddress will be set to zero and the COT-bit will be set high so the output-pattern will start again after a trigger..
Because of the 10 MHz clock, fast RAM has to be used; in one clockperiod (100 nS) the contents of the memory location on the NextAddress must be available. The RAM in this circuit (CY 7C128) has an access time of 35 nS.

5.3 Counter.

The counter-circuit consist of three 74F169 binary counters. The circuit diagram of this board is shown in Figure 5.3.1. They are configured as a 12 bit down-counter. Eleven bits are used so the maximum count-value is 2^{11}- 1 = 2047 (i.e. 204.8 uS). The 12-th bit is used as the COT-bit.
Counter loading is synchrone and occurs when /LP (Latch Puls) is low and the clock goes high. /LP goes low when the counter reaches zero (/TC goes low), and the clock is low. Although /TC (Terminal Count) is synchronous, the clock is added to prevent that spikes on TC generate a wrong /LP.
/LP not only loads a new count value, but also the output-latch, the NextAddress and the COT-bit. When the latched COT-bit is high the counter is disabled. The counter can be enabled by resetting the COT-latch by giving a hard- or software trigger.
The hard- or software trigger is synchronized with the clock by creating a one clock-period internal triggerpuls.
The delay between the external trigger and the internal trigger is max. one clock period (100 nS).
The three binary counters form a cascade with a ripple carry. Although a carry-look-ahead is faster, the circuit from the Philips databook (FAST TTL - 1986) did not work correctly for count values with the 4 upper bits low. The ripple carry circuit works well with a 10 MHz clock.

5.4 Interface.

The programmable timer is programmed and controlled by the PC. The PC uses a MetraByte 24 bits parallel I/O board for digital I/O.
The MetraByte (MB) is based upon the 8255 PIA, and has three 8 bits ports, port A,B and C which can be programmed for input and/or output. For use with the programmable timer the MB is configured with A,B and C as output (no input). Port A and B are used for data, port C for control signals.[1]

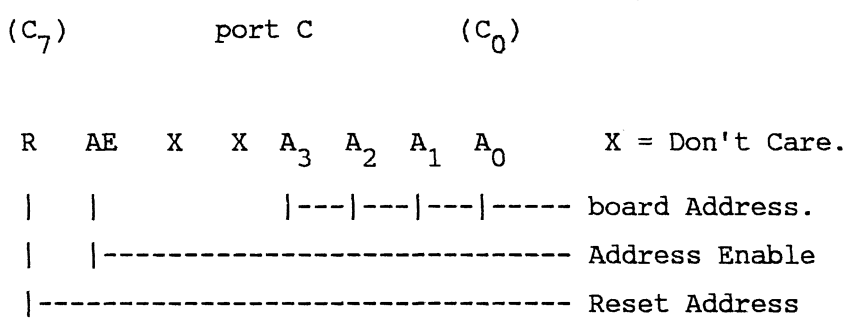


Figure 5.4.1 Port C normal mode

If AE (Address Enable) is high the address on $A_{0..3}$ is compared with the address set on the board with dip-switches. If they are equal the board is addressed, and input from port A and B is possible. The programmable timer remains addressed until the board is un-addressed by setting R (Reset Address) high, or by addressing another address.

Once the timer is addressed, the C-port contains signals for programming and control:

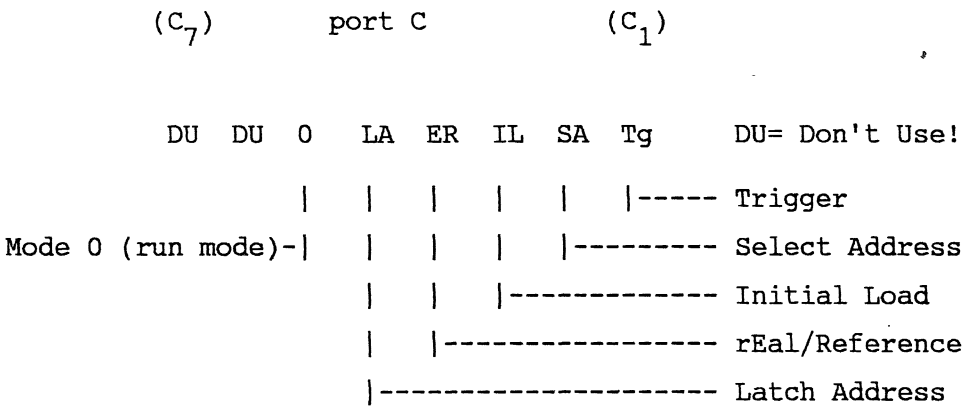


Figure 5.4.2 Port C run mode

Trigger :Software trigger to start counter (pulse).
Select Address :Select full address from port A if high.
Initial Load :Load current RAM-contents in counter, output and address-latch (pulse).
rEal/Reference :Real measurement if low, reference if high.
Latch Address :Latch address-byte (pulse).

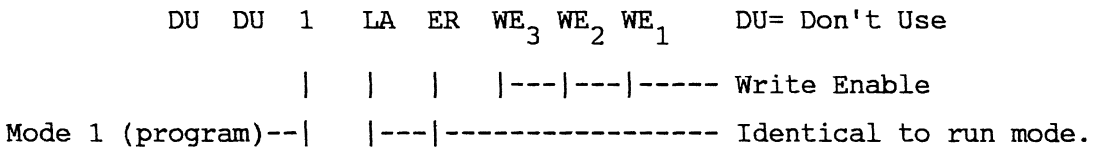


Figure 5.4.3 Port C program mode

Write Enable i :Load value on port B in RAM i (pulse).

5.5 Software.

The timing hardware has to be programmed with time differences between output states i.e. the time a particular outputbyte will occur on the outputlatch is programmed. However this representation is not easy to use because it is difficult to determine the timing of a single output. So the program consist of a 'transducer record editor' to create or alter a transducer-timing configuration, displayed in pulse-delay representation: an output is always a pulse of a certain length occurring after a certain delay.
This transducer-record will be converted in a State-Event record in which timing is stored as a series of output-bytes and the time they appear (the events). All transducer-records are stored in a file with extension TRC. This file will be converted in a file with extension TPG in which the State-Event records are used to make a file with programmable data.
The program is written in Turbo Pascal 4.0 and uses the Turbo Professional toolbox. To gain a more detailed knowledge of the program, read the programlisting and comments.

5.6 Characteristics

Supply voltage	:5V typ. (± 0.5 V)
Supply current	:... mA
Number of output-channels	:8
Output-level	:TTL
Trigger input-level	:TTL
Trigger delay	:max. 0.1 µS
Counter resolution	:0.1 µS
Max. counter value	:2047 (H7FF)
Max. number of timing configurations	:2 x 16
Max. number of outputs/configuration	:16
Interface	:MBus, 3 x 8 bits parallel.

6 Programmable Attenuator

6.1 Introduction

A programmable attenuator has been placed between the synchronization board and the power amplifier (PA) for the following reason (see also Figure 1.1).
If the programmable attenuator is set to 0, maximum output is provided. But not in all cases this maximum is necessary.
In fact the receiverside is so sensitive that in most cases this maximum level is too high. In this case the attenuator serves to reduce the burst amplitude.

6.2 Circuit

The circuit is shown in Figure 6.2.1. In this Figure the address selector of the MBus can be recognized . When the device is selected, a latch (Q4) can be programmed.
The attenuator is driven by Q6 (ULN2003) a darlington driver. Parallel a second driver, drives LED's which give a readout on the front panel, of the settings of the attenuator.
The attenuator is programmable from 0 to 31 dB in a frequency range from DC to 1 GHz. The specifications are shown in Figure 6.2.2.

6.3 Accuracy

According to the specifications of the manufacturer the attenuation is nearly linear. Actually, there is a step in the characteristics.
The measurement of the attenuation is fully automated by the program Diana. This program measures the attenuation for several frequency and attenuation settings. The measurements are done with the HP network analyzer. A result is shown in Figure 6.3.1.

A deviation of only 0.1 dB can cause a inaccuracy of 3 dB in the final result of an acoustic attenuation measurement on a suspension. Therefore it is important to use the real values of the attenuator in the final result calculations. The computer selects the correct attenuation value from a look up table.

7 Receiver Section.

7.1 Overview.

Figure 7.1.1 gives an overview of the receiver section. There is the possibility to select 1 out of 12 configurations.
This has been realized by using a bus structure. The layout reduces the number of relays in the signalpath to two. In the previous design there could be up to seven relays in the signalpath. The relay selector is designed in such a way that only one relay can be selected at a time.
Some receiving transducers have a SMD (surface mounted device) preamplifier (all high frequency transducers).

7.2 SMD preamplifiers

For the preamplifiers, the SMD technique has been chosen in order to be able to mount these amplifiers as close as possible to the transducers. In fact the amplifiers are mounted in the tube of the transducers. This has some advantages. Firstly the distance between the transducer and the amplifier is very short, improving the Signal to Noise Ratio (SNR). Secondly the output is now 50Ω, therefore reflections of the signals over the long cables are prevented.
A principal diagram of the amplifiers is shown in Figure 7.2.1.

The SMD amplifiers need a power supply of + 15 V which is supplied over the coax. To compensate for the voltage losses over the rf decoupling, a power supply with a senseline is used. For a description of this supply see the chapter power supplies.

There are two kinds of amplifiers, typenumber 2005-1 and 4005-1.
The specifications of the type 2005-1 are :

- Frequency range 1 to 20 MHz
  Gain 20 dB
  input- output impedance 50 Ω

For typenumber 4005-1 :

- Frequency range 20 to 100 MHz
  Gain 40 dB
  input- output impedance 50 Ω

The outer sizes of the amplifiers are:

- Width 15 mm
  maximum length 52 mm
  maximum height 10 mm

All amplifiers have been checked for the correct specifications and some of the results are shown in Figure 7.2.2.

The amplifiers are custom designed devices.
They are made by : IMWAVE
RF & MicroWave electronics
Postbus 331
2100 AH Heemstede

7.3 Relays

The receiver relay has 12 inputs and 1 output.
The transmitter relay has 8 inputs and 1 output.
Both relays are from RF components , Coaxial relays 50 Ω series 'C'(Mk6), delivered by Radikor.
The specifications of these relays are given in
Figure 7.3.1.
When a relay is not selected, it is terminated with 50 Ω to ground, to prevent noise and RFI disturbing the signal.

7.4 Bias network

The bias network is used to couple the DC and RF. The SMD amplifiers need their power supply over the coax. The bias network must couple the DC to the coax without interfering with the RF signal.
The bias network also has a sense output. The senseline is needed for compensation of the voltage losses over the rf decoupling.
A circuit diagram and some specifications of the bias network are given in Figure 7.4.1.

7.5 Relay selector

The relay selector simultaneously selects the transmitter and receiver. On the transmitter side the relay can select eight transmitters.
The receiverside can select twelve receivers.
Four of these receivers are used for scattering measurements and therefore use the same transmitter as the transmission receivers for a specific frequency range.
The relay selector is designed to select only one transducer pair at a time. This avoids that several transducers would become connected.
The transmitter transducer is selected by 3 bits. These 3 bits are multiplexed so only 1 transducer is selected.

For the receivertransducers 1 bit more is needed. This bit indicates if transmission or scattering is selected.
Further the selected transducerpair is displayed on the frontpanel by a group of LED's.
In Figure 7.5.1 the circuit diagram, the pcb layout and the component mounting is shown.

8 Software Programmable Gain Amplifier.

8.1 Introduction

This device has been developed to reduce the number of mechanical parts which have to be set when tuning the system.
It is used between the receiver selector and the detection electronics.
The gain of the device is fully programmable in the range from 0 to 30 dB by the MBus.

The circuit can be divided in two parts. An analog part and a digital part.
The circuit is shown in Figure 8.2.1.
First the analog part will be discussed.

8.2. Analog electronics.

The incoming signal is mixed with a time window. The mixer (SRA-3MH) filters the signal in time, to separate the desired burst and the delayed reflections (of the burst). The timing signal for the mixer is obtained from the timing board.

The following stage consists of two a MWA 110 amplifiers. These amplifiers have limited input level. When the input level is too high the signal will be distorted.
For the analog part of this device the allowed input level is -7 dBm.
Normally this input level is acceptable with the low output levels from the transducers.
If the input level is too high the attenuator on the transmitter side could select a higher attenuation.

Then follows a PIN diode attenuator, which can be programmed by regulating the bias current. Two diodes are used to get a better performance.

The principle of this method is called reflective attenuation (see[2],[3],[4]).
The basic principle is that the HF-resistance of a PIN-diode depends on the bias current. The resistance is lineair with the current. So a programmable resistance is obtained by regulating the bias-current.
The bias current is in the range of 0-150 uA.
The bias current regulation is described in the next chapter.

A disadvantage of the reflective attenuation is that for high attenuations most of the power is reflected. The amplifiers used are no longer properly set in this case. To avoid such circumstances, the attenuator could be used to select a higher attenuation, so the SPGA can be set to a better level.

The output stage is again an amplifier (MWA 130) which ensures a proper output impedance and an acceptable output level.

8.3 Digital electronics

The main part of the interface is formed by the DAC (AD577) which is programmed over the MBus. The output of the DAC is programmable from 0 to 2.56 V. The DAC has no current output, which however is necessary for driving the PIN diodes, therefore a voltage-current interface is used.
This is done with an operational amplifier (opamp) and a current mirror.
The opamp is a so called bilateral current source. The output is a current which is independent of the load.
The output current of the source depends on the ratio of the resistors. The output current varies between 0 and 200 uA when the input voltage varies between 0 and 2.56 V.

The load of the current source in this case is a transistor connected as a diode which forms a current mirror. The current is copied into the next transistor. To ensure a correct copy of the current, the two transistor must be matched. In the present case this is done with a transistor array (CA3086), both transistors are on the same substrate.
The current must be RF decoupled. This is done by resistors and capacitors. No coils are used because of their limited frequency response. The network must function in the entire frequency range from 1 to 100 MHz.

8.4 Software

The SPGA has frequency dependent characteristics and it also has nonlineair tuning characteristics. Figures 8.4.1 and 8.4.2 show these characteristics. To compensate for this dependence a lookup table is used. To get an accuracy of better then 0.1 dB it was necessary to measure 7 different frequencies in steps of approximately 1 dB. So there are 7*30= 210 values in the lookup table.
A procedure has been written which automatically gets the right gain corrected for the frequency and the nonlineair tuning characteristics.

9 Synchronization circuit.

9.1 Introduction.

The aim of the synchronization circuit is to make a burst from a RF signal. The number of periods of the burst or burstlength is programmable from 1 to 4096 periods.
The burst is switched on and off at zero-crossings.

9.2 The Circuit.

The circuit diagram of the synchronization electronics is shown in Figure 9.2.1.
The RF-signal is divided by a splitter PSC2.
One signal is translated to a clocksignal for the digital electronics.
First the signal is fed to a comparator AD9685.
For high frequencies the signal is first divided by ten using a SP8660.
High or low frequency range is selectable over the MBus.

The AD9685 is an ultra fast comparator which makes it possible to switch at zero-crossings.
Then a level translator is necessary because the comparator has an ECL output. The other electronics is Fast TTL.
The correct clocklevel is obtained from a 10125 a ECL-TTL translator.

The triggering must be synchronized with the clock to make sure the output flip-flop switches on the zerocrossings of the signal.
First a JK flip-flop is set on the rising edge of an external trigger pulse. A second JK flip-flop is set after the first flip-flop only it is synchronized with the clock signal. The second flip-flop generates a reset pulse for the first flip-flop. Also a Parallel Enable (PE) is generated to latch the burstlength value in the counters.
At the same time a monostable multivibrator is set on the rising edge of the Q output of the second flip-flop.

The output sets the J input of the third (output) JK flip-flop.
One clock cycle after the second flip-flop the output flip-flop is set.
The same time the second flip-flop is reset, because it is in the toggle mode.
The moment the output of the third flip-flop goes high the counter starts counting.
The counter counts down. When zero is reached the counter generates a reset signal for the output flip-flop.
The output flip-flop controls the burstoutput via a mixer (SRA-3MH). The mixer is switched on and off by the flip-flop. So at the output of the mixer a burst is obtained.

The counter is a twelve bit counter. So values between 1 and 4096 are programmable. The burst length is also given in a number of periods. The burstlength depends on the frequency and the programmed number of cycles. The software calculates the number of cycles needed for the specified burstlength.
However, when detecting the burst the burstlength must be taken into account to obtain the best possible accuracy, because in the worst case, the burstlength deviation can be up to several percents.

10 Detection electronics.

10.1 Introduction.

The principle of the new detection electronics has been chosen the same as that of the existing circuit.
Some other possibilities have been analyzed. However, it turned out that the already existing detector is the most flexible and the easiest solution.
Coherent detectors will cause problems when detecting the scattered signals (these signals are uncorrelated).
Some changes were made to obtain a better performance. New components were used for greater accuracy and an input amplifier provided a higher sensitivity.

10.2 The Circuit.

The input is formed by an amplifierstage MWA130 to increase the sensitivity level. The AM detector (SL623) gives the burst envelope, which is proportional to the burst amplitude.
The signal is split into two channels. In one channel the signal will be squared. The circuit diagram is shown in Figure 10.2.1.
The signal is amplified and filtered by an active second order low pas filter formed around the OP37. The filter is a so called multiple feedback infinite gain type [5].
First the channel without multiplier will be discussed. The gain of the active filter is 10 and the cutoff frequency is 1 MHz.
The next stage is a programmable amplifier which makes it possible to correct for the different burstlengths, for shorter burstlengths a higher gain. Typically, a burst of 15 µs needs a gain of 1 and a burst of 2 µs needs a gain of 8. Then an adjustable amplifier makes it possible to scale the signal for a correct output range of the integrator. Typically a gain of about 2 is used.

The integrator is formed by a OP37. The integrator is reset with a signal that forces the capacitor to discharge. The reset is caused by closing a switch, the ADG202A, a SPST CMOS switch.
The output stage is formed by a sample and hold SMP11. To avoid inaccuracy caused by the drooprate of the integrator, the sample and hold holds the output after integration.

In the other channel a multiplier AD534 is used to get the square of the signal. This signal is proportional to the intensity of the scattered sound. Because the squared signal has a greater dynamic range the gain of the amplifiers in this channel is adjusted to a lower value in order to get a correct scaling of the output of the integrator.
Also the polarity of the signal has to be changed one more time because the input signal of the multiplier is negative and the output positive, which means an extra polarity change in comparison to the other channel.

The capacitors used by the integrator and the sample&hold must be high quality capacitors. Polystyreen capacitors were used.

10.3 Control Signals.

The integrator and the sample and hold need control signals for correct timing.
All the IC's can be controlled, via the MBus or via an external control input. Another possibility is to control them separately. This avoids that spikes, occurring on the edges of the control signals, interfere with the signal.
The control signals can be obtained from the timingboard.

11 Local Oscillator.

11.1 Introduction.

The detection circuit is not able to cover the whole frequency band from 1 to 100 MHz. For frequencies above the 20 MHz a local oscillator mixes the received signal down to a IF of 10.7 MHZ.
For frequencies up to 20 MHZ the detection circuit is able to detect these signals directly.
The local oscillator is a synthesizer originally designed by G.J. Dorenbos [6].

11.2 Relay selector.

In order to select the high or low frequency detection a relay is used to switch the signal. The relay used is of the same type as used in the transmitter-receiver selector.
Integrated is also the real-reference selection.
The circuit is given in Figure 11.2.1. The first four bits of the A port A0..A3 are used to select the High-Low relay. A4..A7 are used to select the real-reference relay. Further there is a read out on the front panel of the status of the relays. Always one LED should be on otherwise an error has occurred.

11.3 Synthesizer.

In this version the synthesizer is controlled over the MBus in stead of the GPIB-bus. Therefore some changes were made.
The synthesizer itself is the same described in [6]. The GPIB-interface has been replaced by a MBus-interface. A circuit diagram of the synthesizer is shown in Figure 11.3.1.
The GPIB-interface IC has been replaced by four latches and a MBus-address decoder.
Also the output filter is integrated on the layout. This filter is a IF filter of 10.7 MHz (KACS 4520).

12 Power Supply.

The power supply exists of 4 boards.
First the + 5 V. This is a switched power supply, 3 A.
Then $\pm$ 15 V .
The - 5 V is retrieved from the -15 V.
At last + 30 V necessary for the synthesizer.

Two fans are added for cooling the electronics.
The supply of these fans is retrieved from the 30 V transformer. The voltage is rectified and directly connected to the fans.
Figure 12.1 shows the diagram of the power supply.

13 DMA trigger control

13.1 Introduction

The intention of the DMA trigger control is to make the whole system operate independently of the computer. The computer only generates one trigger pulse and then all data-aquisition is completed under DMA, so the computer is free to do calculations on previously gathered data.

13.2 The circuit

There are two devices to be programmed. First the programmable crystal oscillator PXO1000, which controls the repetition frequency of the bursts. Second a 16 bit binary counter which controls the number of bursts (up to 64536 bursts).
The PXO is programmable from 10 Hz up to 1 MHz. The aquisition time of the DT-board under DMA is about 0.1 ms (for two channels).
So a typical repetition time could be 1kHz.
The number of bursts is typically 1000 for transmission and 5000 for scattering measurements. The 16 bit binary counter is programmable from 1 to 64535 bursts.
The word for the 16 bit counter is programmed over the A and B ports of the MBus. A PE (Parallel Enable) pulse is needed to load the word into the counter. The PE pulse also sets the output of a flip-flop which controls the output port of the trigger pulses.
When the counter reaches zero the flip-flop is reset.
Two extra trigger pulses should be added for correct triggering of the DT2801 board.
To program the PXO1000 the A port of the MBus is also used. To select whether the A port should program the counter or the oscillator, two control bits are needed. Bit C0 and C1 control this option. In Figure 13.2.1 the layout of the circuit is shown.

14 References.

1 Schaafsma A.S., 1988, Development of silt measuring methods,
Study of the feasibility of concentration measuring with
ultrasound : results,
Research Report, F37/M2032, Part II, November 1988,
DELFT HYDRAULICS

2 Application Note 922
Applications of PIN Diodes
Hewlett Packard

3 Application Note 957-1
Broadbanding the shunt PIN Diode SPDT Switch
Hewlett Packard

4 Application Note 929
Fast Switching PIN Diodes
Hewlett Packard

5 Handboek aktieve filters
D.E. Johnson J.R. Johnson H.P. Moore
Maarten Kluwer's
Internationale uitgeversonderneming
Antwerpen-Amsterdam
1982

6 Dorenbos G.J. , 1987, Development of silt measuring methods,
Electronic signal processing : A detection method for
HF-bursts,
Research Report, F37-04, part I, December 1987,
DELFT HYDRAULICS

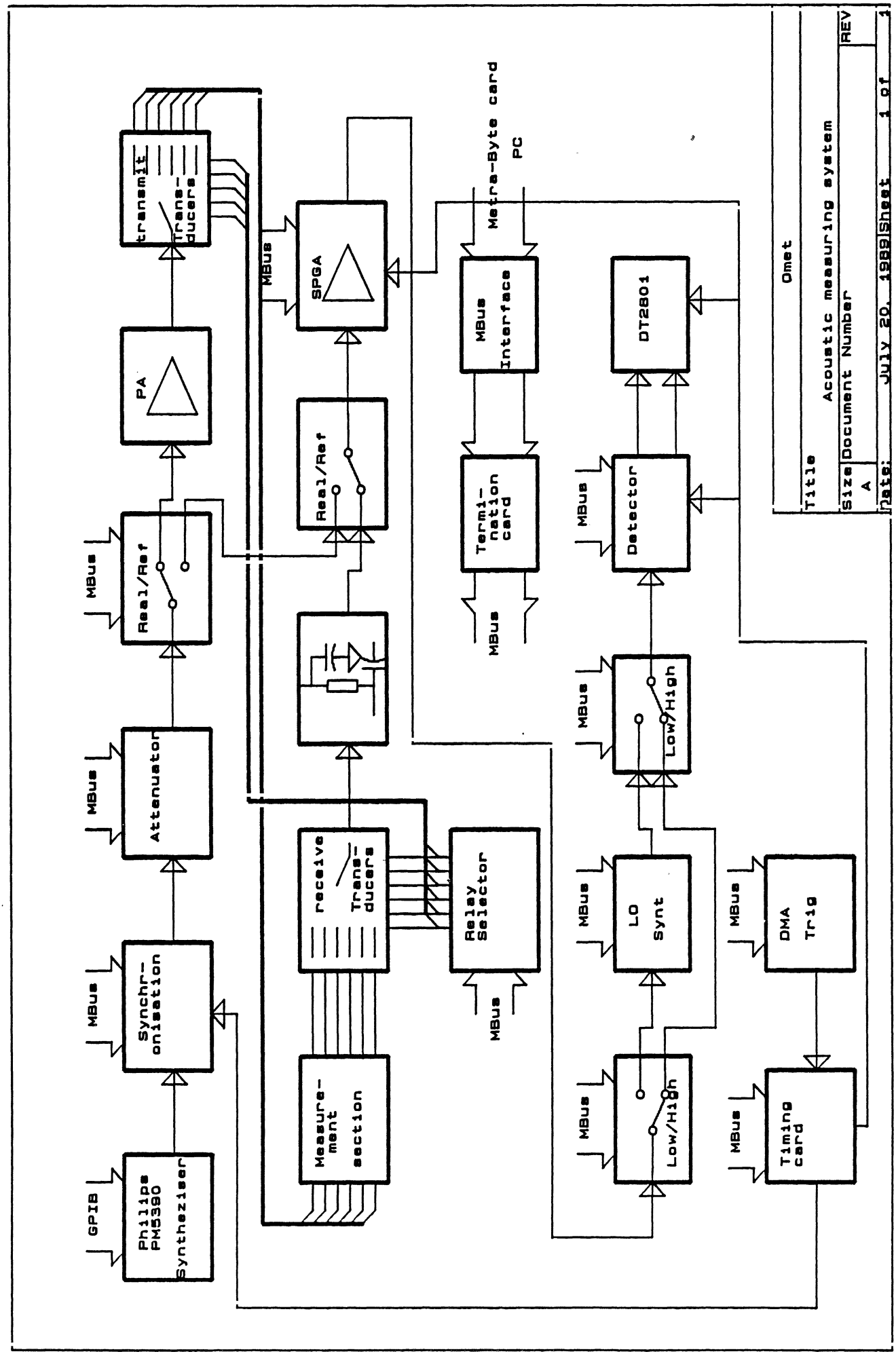
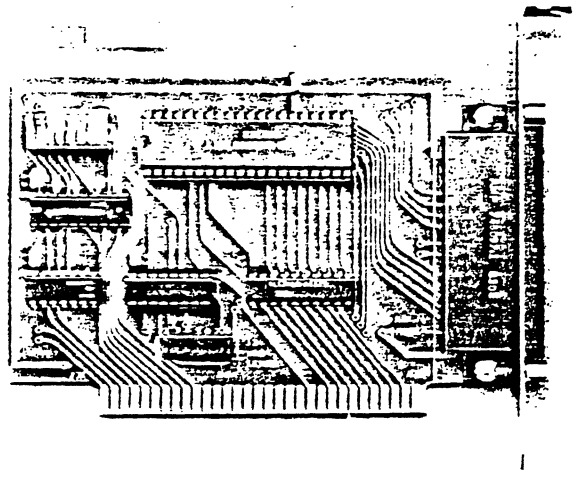


Figure 1.1 Block diagram of the system

24 BIT PARALLEL DIGITAL I/O INTERFACE MODEL PI012

DATA ACQUISITION AND CONTROL FOR IBM PC/XT/AT AND COMPATIBLE COMPUTERS



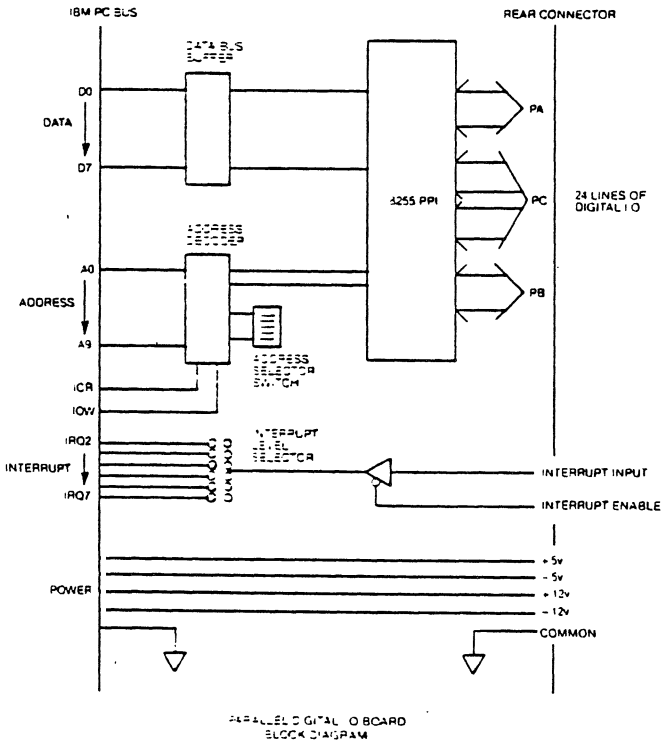
FEATURES

- 24 TTL/DTL Digital I/O Lines
- ±12V, ±5V Power from IBM PC/XT
- Unidirectional, Bidirectional strobed I/O
- Interrupt Handling
- Direct Interface to wide range of peripherals
- Plugs into IBM PC/XT Bus
- Handshaking

APPLICATIONS

- Contact Closure Monitoring
- Plotter Interface
- Printer Interface
- Digital I/O Control
- Magnetic Tape Units
- Useful with A/D's and D/A's
- Card Reader Interface

BLOCK DIAGRAM



PARALLEL DIGITAL I/O BOARD BLOCK DIAGRAM

IBM IS A REGISTERED TRADEMARK OF INTERNATIONAL BUSINESS MACHINES INC.

FUNCTIONAL DESCRIPTION

MetraByte's parallel digital I/O card provides 24 TTL/DTL compatible digital I/O lines, interrupt input and enable lines and external connections to the IBM P.C.'s bus power supplies (+5v, +12v, −12 & −5v). It is a flexible interface for parallel input/output devices such as instruments and displays and user constructed systems and equipment.

24 digital I/O lines are provided through an 8255-5 programmable peripheral interface (P.P.I.) I.C. and consist of three ports, an 8 bit PA port, an 8 bit PB port, and an 8 bit PC port. The PC port may also be used as two half ports of 4 bits, PC upper (PC4-7) and PC lower (PC0-3). Each of the ports and half ports may be configured as an input or an output by software control according to the contents of a write only control register in the P.P.I. The PA, PB & PC ports may be read as well as written to. In addition, certain other configurations are possible for unidirectional and bidirectional strobed I/O where the PC ports are used for control of data transfer and interrupt generation etc. Users are referred to the Intel 8255-5 data sheet for a complete technical description and summary of the various operating modes of the P.P.I.

Interrupt handling is via a tristate driver with separate enable (interrupt enable — active low). This may be connected to any of the interrupt levels 2-7 available on the IBM P.C. bus by means of a plug type jumper on the board. Handling of an interrupt is controlled by the 8259 interrupt controller in the IBM P.C. and this is set by BIOS on system initialization to respond to positive (low-high) edge triggered inputs. Users must program the 8259 to respond to their requirements and set up corresponding interrupt handlers.

Power from the IBM P.C. is available on the connector from the computer bus. Users should observe the current capacity limits detailed on page 2-37 of the IBM P.C. "Technical Reference Manual" and make allowance for the power consumption of any other expansion boards that may be in use.

Figure 2.1.1 Description of the MetraByte board

BASE ADDRESS SWITCH

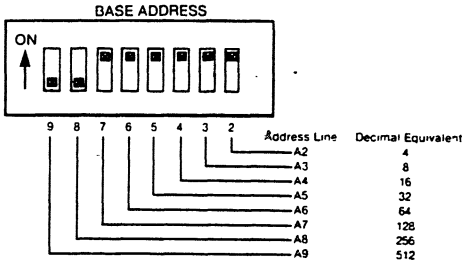
The 8255-5 P.P.I. uses 4 I/O address locations which are fully decoded within the I/O address space of the IBM P.C. . The base address is set by an 8 position DIP switch (see Fig. 1) and can in theory be placed anywhere in I/O address space, but base addresses below FF hex (255 decimal) should be avoided as this address range is used by the internal I/O of the computer. The 200-3FF hex (512-1023) address range provides extensive unused areas of I/O space, though you should check with page 2-23 of the "Technical Reference Manual" for possible conflicts with commonly installed peripherals. The address map for the P.P.I. registers is:—

Base Address	**+0**	**PA port**	**read/write**
	+1	**PB Port**	**read/write**
	+2	**PC port**	**read/write**
	+3	**Control**	**write only**

The 8255-5 P.P.I. and 74LS367N used for the interrupt interface are located in sockets. In the event of externally applied overvoltages, shorts or overloads, users may possibly damage these devices. They are readily replaced by removing them from their sockets and substituting new parts. All other I.C.'s are soldered into the board and are immune from user abuse.

BASE ADDRESS SWITCH SETTING

FIG. 1 Base Address switch setting for &H300 (300 Hex) (768 Decimal)

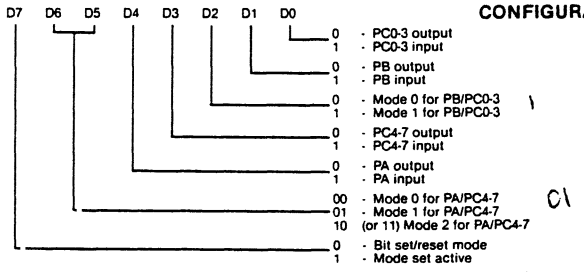


Switches have decimal values as above in the "off" position. In the "on" position decimal value is zero.

PROGRAMMING

Programming is simple whether from assembly language or BASIC. The P.P.I. should first be configured in the initialization section of your program by writing to the control register. On power up or reset, all ports are configured as inputs. A wide variety of configurations are possible by writing the appropriate control code. Some examples are detailed:—

CONTROL WORD — **CONTROL WORD CONFIGURATION**



Note that D7 must be high (=1) to set the configuration of the ports. There are three possible operating modes, and the PA/PC4-7 and PB/PC0-3 groups may be in different modes at the same time:—

Mode 0 - Basic I/O, all ports are I/O ports
Mode 1 - Strobed I/O, part of the PC port controls data transfer
Mode 2 - Bidirectional I/O on PA only, part of PC controls data transfer

Some examples:—

PA input, PB output, PC0-3 input, PC4-7 output
Control word = 1001 0001 binary or 91 hex

Strobed output on PB, PA output, PC0-3 control, PC4-7 input
Control word = 1000 1100 binary or 8C hex

To program:

1) First write to the control register to set configuration e.g. in BASIC:—
   xxxx OUT (Base address +3), &H91
2) Then you can access the ports as required. For example to read PA:—
   xxxx X% = INP (Base address + 0)
   To write to PB:—
   yyyy OUT (Base address + 1), DATA
   To read PC:—
   zzzz Z% = INP (Base address + 2)
3) Once the configuration has been set in the initialization, the P.P.I. will remain in that configuration until a further write to the control register. Users should be warned that it is a property of the 8255 P.P.I. that all port registers are cleared by a write to the control register. If you intend to make repeated changes of configuration in your program, you may also need to make provision for restoring data to cleared ports.

The following programming example demonstrates how input bits of the PC Port can be used to monitor the status of two points and when their condition is met, will output a binary value to the PB Port.

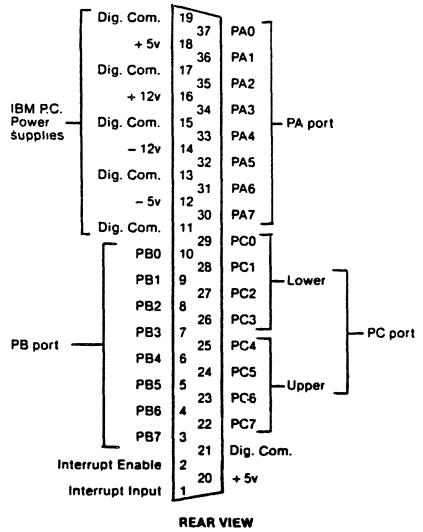
```
xxxx    OUT &H313, &H89
 20     K% = INP (&H312)
xxxx    If (K% and 5) = 5 then OUT &H311, 9
xxxx    If (K% and 5) = 0 then OUT &H311, 0
xxxx    Go to 20
```

If Input Port PC Bits 0 and 2 are true then Output A Binary 9 (Bits 0 and 3) from the PB Port, otherwise Output A zero.

CONNECTOR PIN ASSIGNMENTS

All digital I/O is through a standard 37 pin D type male connector that projects through the rear panel of the computer. For soldered connections a standard 37 pin D female (ITT/Cannon DC-37S or equivalent) is the correct mating part, and can be ordered from MetraByte as part #SFC37. Insulation displacement (flat cable) connectors are available from Amp (#745242-1), 3M, Winchester, Robinson-Nugent etc.

The connector pin assignments are as follows:



SPECIFICATIONS

LOGIC INPUTS AND OUTPUTS	Min.	Max.
Input logic low voltage:	−0.5	0.8 volts
Input logic high voltage:	2.0	5.0 volts
Input load current PA, PB, PC port (0<Vin<5v):	-10	+10 uA
Input low current, interrupt inputs:	—	−0.4 mA
Input high current, interrupt inputs:	—	20 uA
Output low voltage PA, PB, PC ports (Isink=1.7 mA):	—	0.45 volts
Output high voltage PA, PB, PC ports (Isource=200 uA):	2.4	— volts

All outputs and inputs are TTL/DTL compatible and outputs will drive 1 standard TTL load (74 series) or 4 LSTTL (74LS) loads. CMOS compatibility can be obtained by connecting a 10Kohm pullup resistor from the input or output to +5v.

BUS LOADING

Input loading on IBM P.C. expansion bus:	1 LSTTL load for all inputs
Power consumption:	170 mA typ. @ +5v

ENVIRONMENTAL

Operating temperature range:	0 to 50 deg. C.
Storage temperature range:	−40 to +100 deg. C.
Humidity:	0 to 90% Non-Condensing
Size:	Half slot
Weight:	3.5 oz.

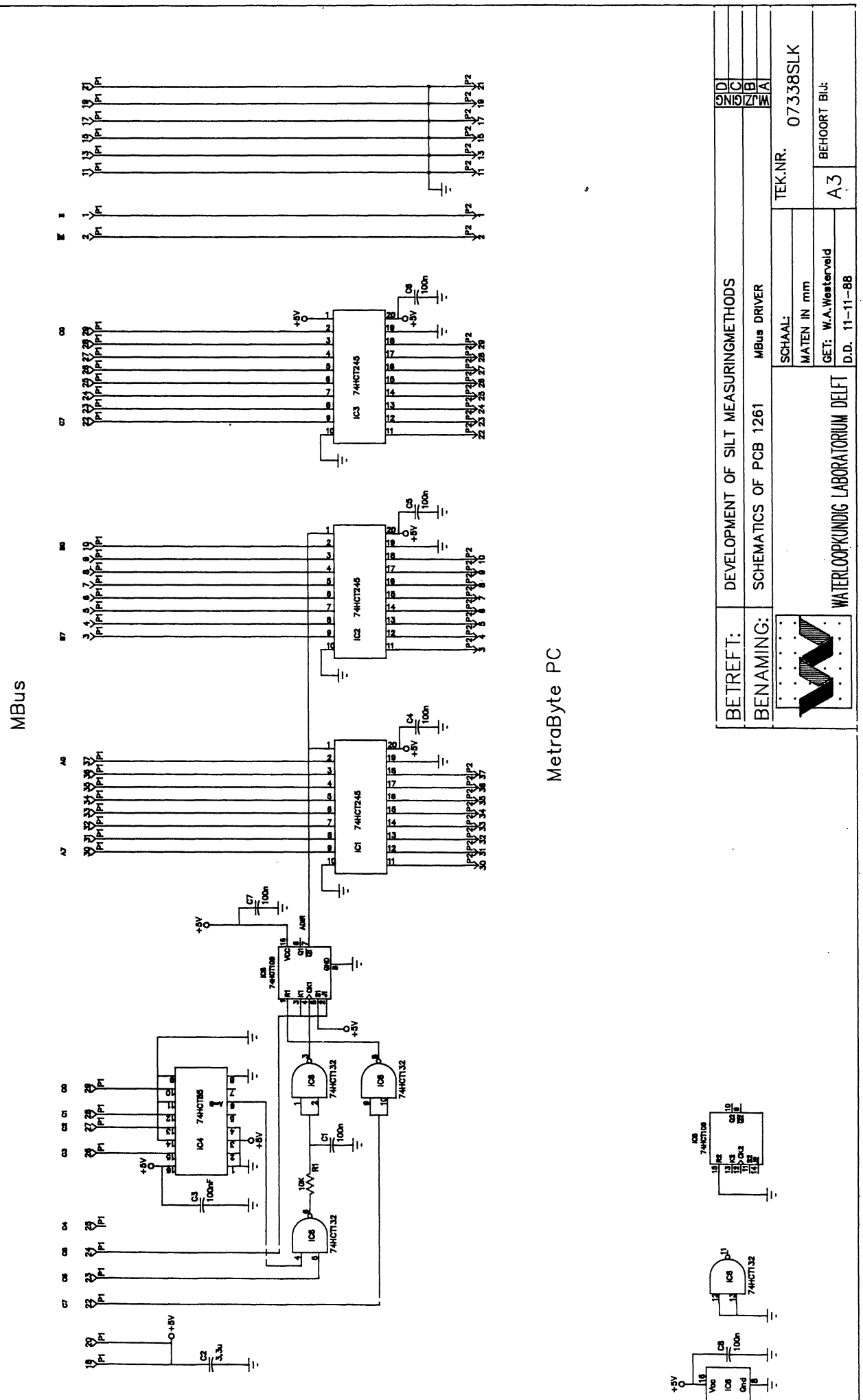


Figure 2.3.1.a Circuit diagram MBus Interface

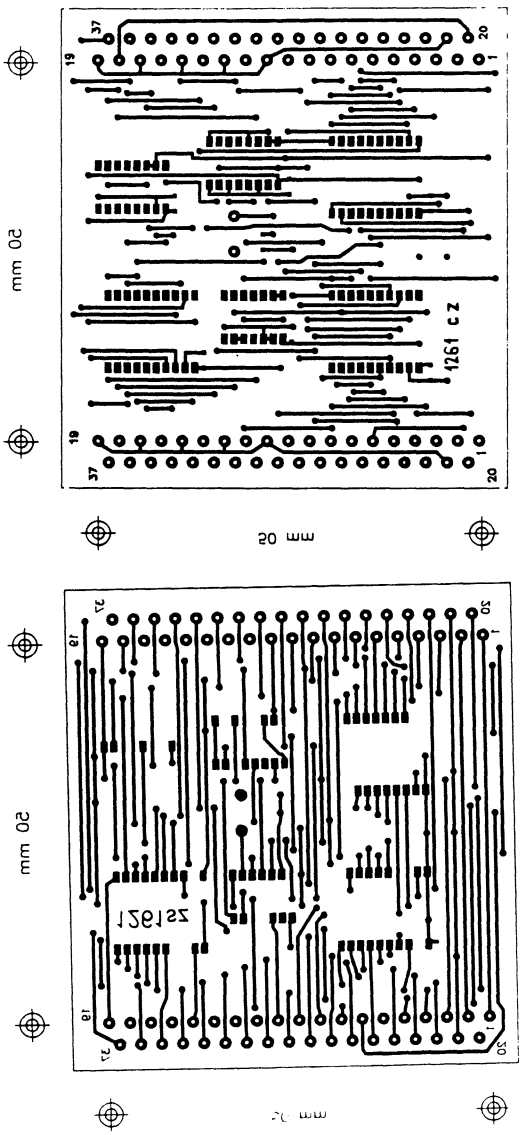
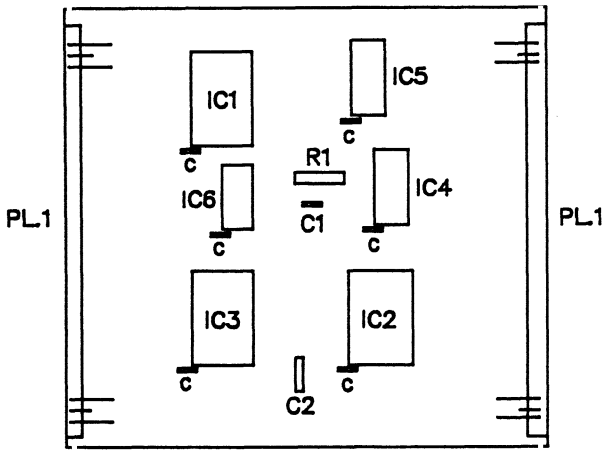


Figure 2.3.1.b PCB Layout MBus Interface



PRINT 1261

Figure 2.3.1.c Component Mounting MBus Interface

BETREFT:	DEVELOPMENT OF SILT MEASURING METHODS	WIJZIGING	D
			C
BENAMING:	COMPONENT MOUNTING OF PCB 1261		B
			A
WATERLOOPKUNDIG LABORATORIUM DELFT	SCHAAL:	TEK.NR.	07431SLK
	MATEN IN mm		
	GET: W.A.Westerveld	A4	BEHOORT BIJ:
	D.D. 11-11-88		

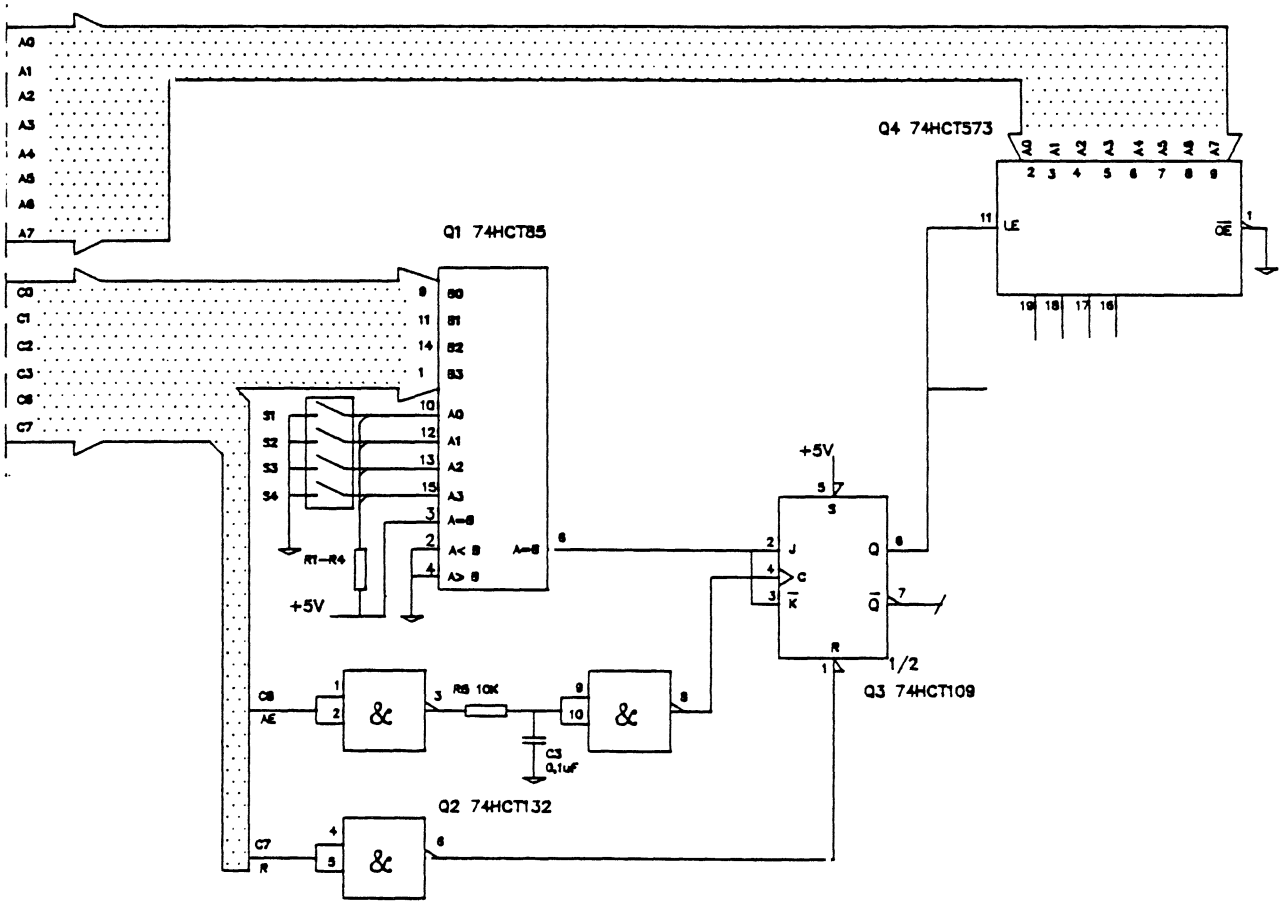


Figure 2.4.1 Basic MBus to Device Interface

```
  A                    Pin Number                    C

MB-A0-------------------1---------------------MB-A1
MB-A2-------------------2---------------------MB-A3
MB-A4-------------------3---------------------MB-A5
MB-A6-------------------4---------------------MB-A7
MB-B0-------------------5---------------------MB-B1
MB-B2-------------------6---------------------MB-B3
MB-B4-------------------7---------------------MB-B5
MB-B6-------------------8---------------------MB-B7
MB-C0-------------------9---------------------MB-C1
MB-C2------------------10---------------------MB-C3
MB-C4------------------11---------------------MB-C5
MB-C6------------------12---------------------MB-C7
Interupt Enable--------13-------------------Interupt Input
Lamp Test--------------14---------------------NC
+15 V  PS--------------15---------------------+15 V  PS
Com Analog GND---------16-------------------Com Analog GND
-15 V  PS--------------17--------------------- -15 V  PS
          -------------18-------------------
          -------------19-------------------
Digital GND------------20-------------------Digital GND
TO-0-------------------21---------------------TO-1
TO-2-------------------22---------------------TO-3
TO-4-------------------23---------------------TO-5
TO-6-------------------24---------------------TO-7
          -------------25-------------------
          -------------26-------------------
Analog GND-------------27-------------------Analog GND
Analog GND-------------28-------------------Analog GND
-5 V  PS---------------29--------------------- -5 V  PS
+5 V  PS---------------30--------------------- +5 V  PS
Com Dig GND------------31-------------------Com Dig GND
+30 V  PS--------------32--------------------- +30 V PS

MB = MetraByte-Bus
TO = Timingboard Output
PS = Power Supply
```

Figure 3.1 : Backplane Layout

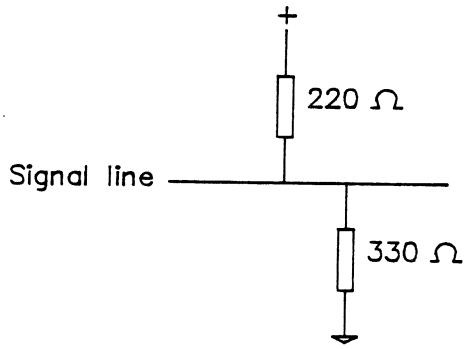


Figure 4.1 TTL Termination

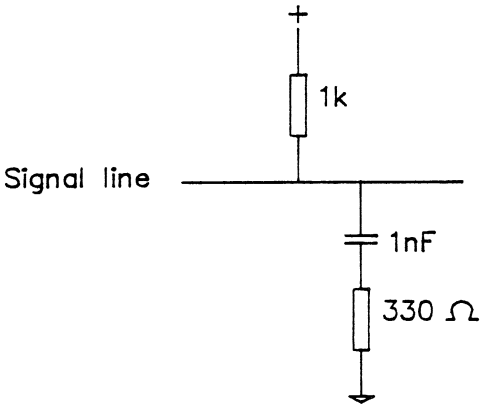


Figure 4.2 HCT Termination

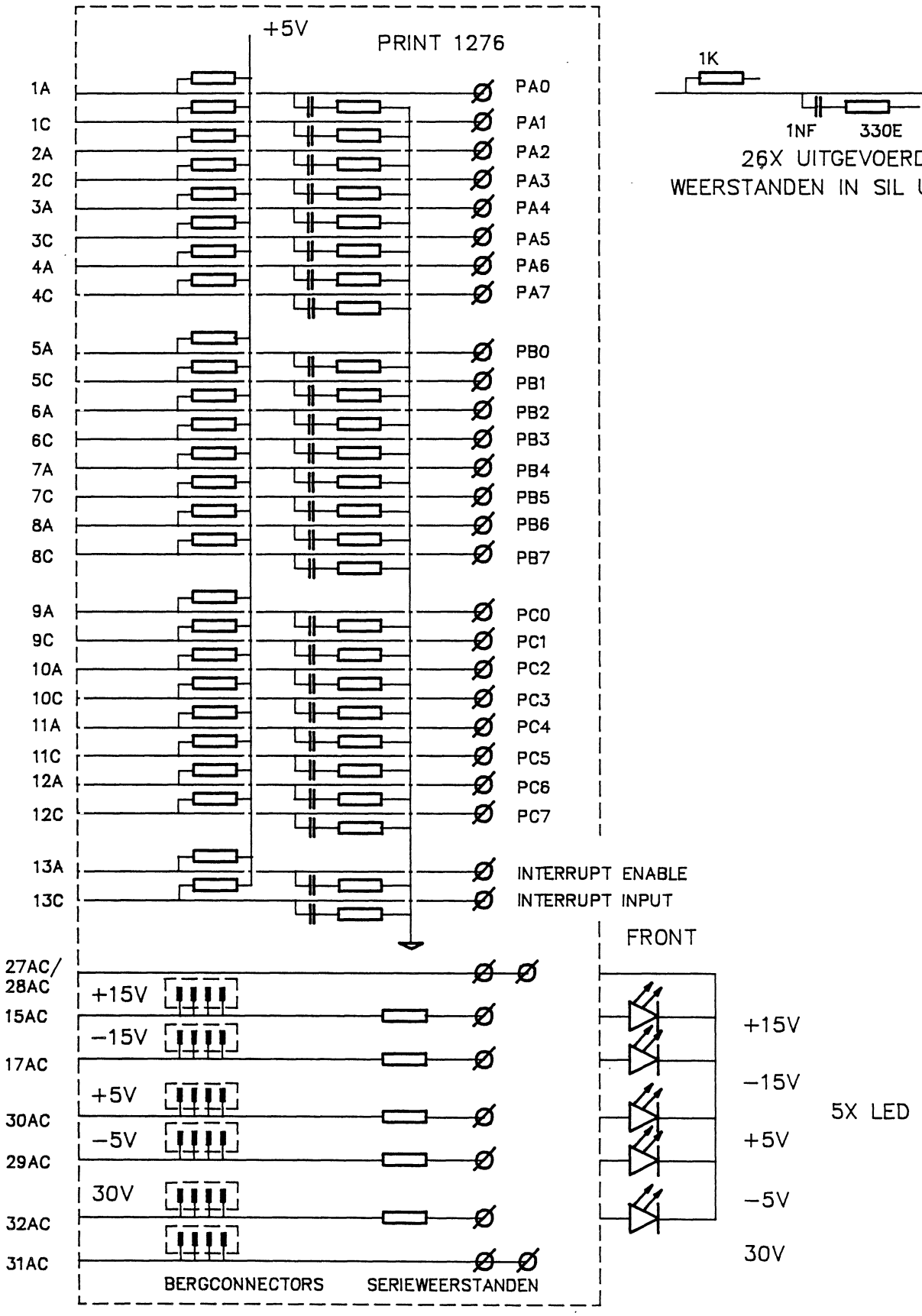


Figure 4.3.a Circuit diagram Termination board

BETREFT:	SLIBKOLOM	WIJZIGING D C B A
BENAMING:	TERMINATORPRINT	

WATERLOOPKUNDIG LABORATORIUM DELFT

SCHAAL:	TEK.NR.	07413
MATEN IN mm		
GET: H.STEENMAN	A4	BEHOORT BIJ:
D.D. 12/11/'88		

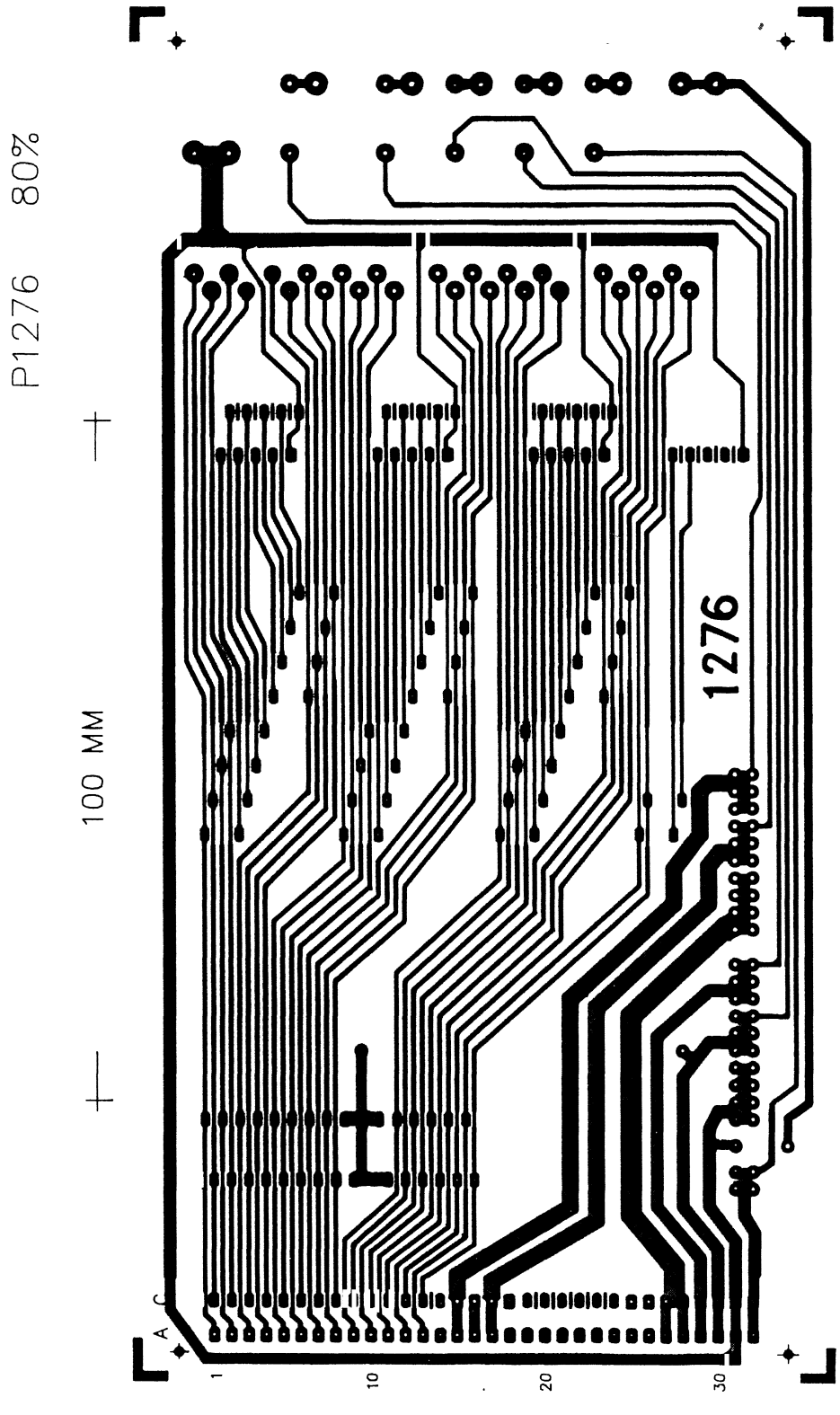


Figure 4.3.b PCB Layout Termination board

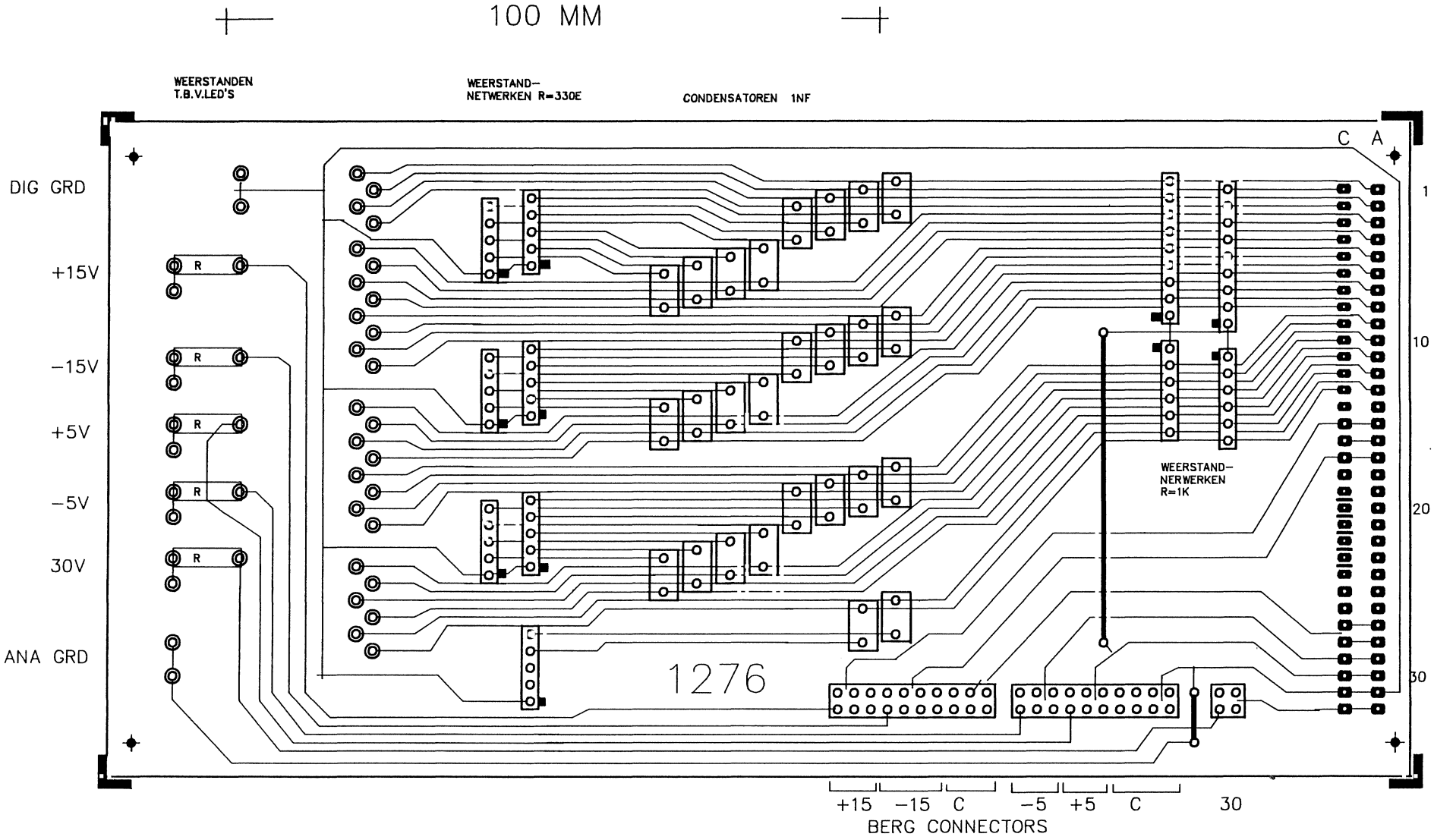
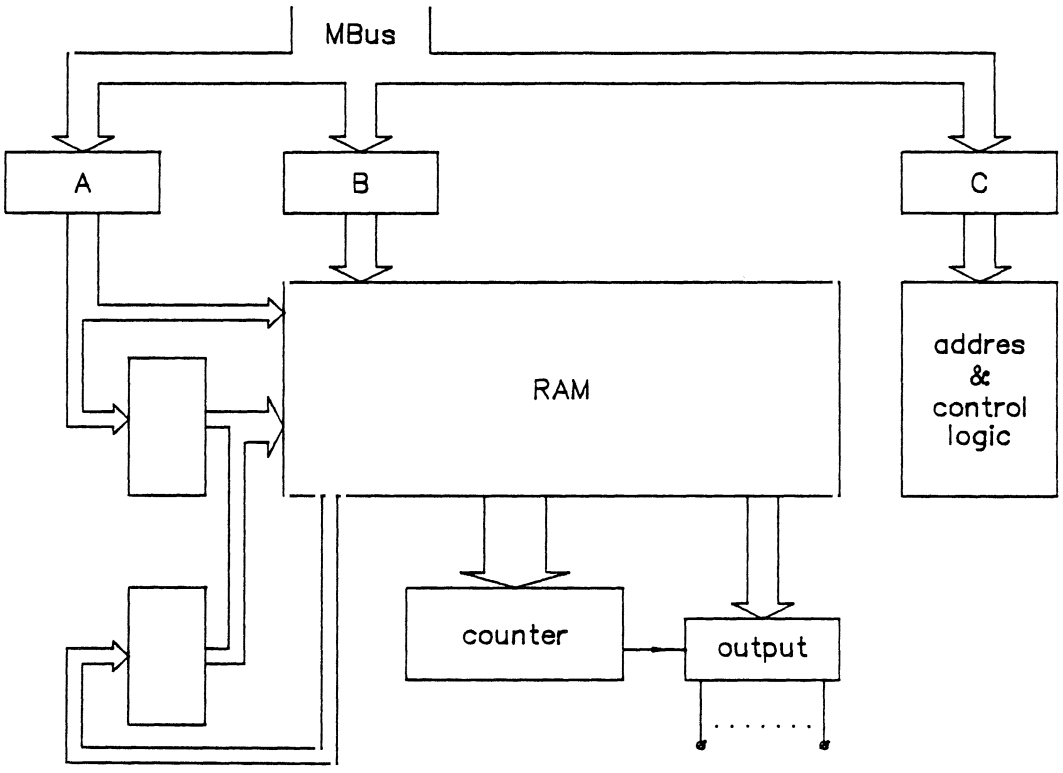


Figure 4.3.c Component Mounting Termination board

BETREFT:	TERMINATOR PRINT	WIJZIGING D C B A
BENAMING:	COMPONENTOPSTELLING	
WATERLOOPKUNDIG LABORATORIUM DELFT	SCHAAL: 1,6=1	PRINT NR: 07407
	MATEN IN mm	
	GET: H.STEENMAN	A3 SCHEMA NR:
	D.D. 17/10/'88	



Block–diagram programmable timing–circuit

Figure 5.1.1 Block diagram Timing board

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
7	CY7C123-7PC	P13	Commercial
	CY7C123-7DC	D14	
	CY7C123-7LC	L53	
12	CY7C123-12PC	P13	
	CY7C123-12DC	D14	
	CY7C123-12LC	L53	
15	CY7C123-15DMB	D14	Military
	CY7C123-15LMB	L53	

Figure 5.2.1.a DataSheet CY7C128 RAM

CYPRESS SEMICONDUCTOR

CY7C128

2048 x 8 Static R/W RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—25 ns
- Low active power
  — 660 mW (commercial)
  — 825 mW (military)
- Low standby power
  — 110 mW
- SOIC package
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2000V electrostatic discharge

Functional Description

The CY7C128 is a high performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state drivers. The CY7C128 has an automatic power-down feature, reducing the power consumption by 83% when deselected.

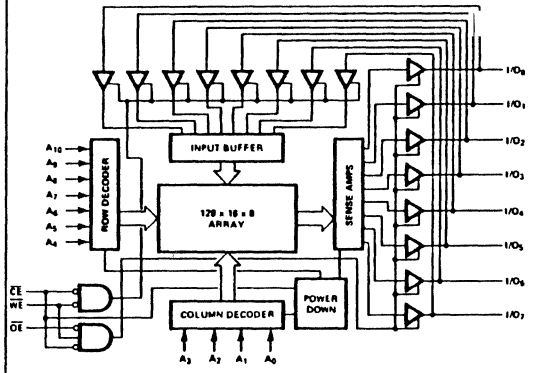
An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{10}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

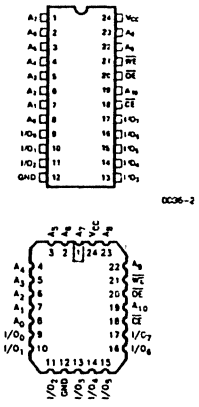
The 7C128 utilizes a die coat to ensure alpha immunity.

2

Logic Block Diagram



Pin Configurations



Selection Guide

		7C128-25	7C128-35	7C128-45	7C128-55
Maximum Access Time (ns)		25	35	45	55
Maximum Operating Current (mA)	Commercial	120	120	120	90
	Military		150	130	100
Maximum Standby Current (mA)	Commercial	20	20	20	20
	Military		20	20	20

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to + 150°C

Ambient Temperature with Power Applied ..... −55°C to + 125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to + 7.0V

DC Input Voltage ..... −3.0V to + 7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V (Per MIL-STD-883 Method 3015.2)

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		7C128 Min.	7C128 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage	Commercial -25, Military -35		2.0	V_{CC}	V
		All Others		2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC} Output Disabled		−40	40	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial -25, -35, -45		120	mA
			Commercial -55		90	mA
			Military -35		150	mA
			Military -45		130	mA
			Military -55		100	mA
I_{SB}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Commercial		20	mA
			Military*		20	

*35 ns and 55 ns only

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms

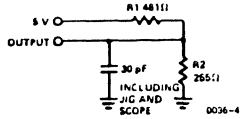


Figure 1a

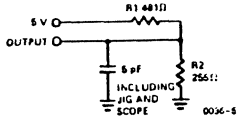


Figure 1b

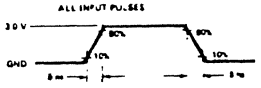
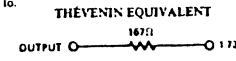


Figure 2

Equivalent to:



Switching Characteristics Over Operating Range[4]

Parameters	Description	7C128-25 Min.	7C128-25 Max.	7C128-35 Min.	7C128-35 Max.	7C128-45 Min.	7C128-45 Max.	7C128-55 Min.	7C128-55 Max.	Units
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5]		12		15		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		12		15		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		20		20		25		25	ns
WRITE CYCLE[7]										
t_{WC}	Write Cycle Time	25		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		40		50		ns
t_{AW}	Address Set-up to Write End	20		30		40		50		ns
t_{HA}	Address Hold from Write End	2		[11]		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		20		20		25		ns
t_{SD}	Data Set-up to Write End	10		15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z		10		15		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		ns

Notes:

3. Data I/O Pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. t_{HZOE}, t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in *Figure 1b*. Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are specified and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected $\overline{OE}$, $\overline{CE}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
11. 0 ns for commercial, 2 ns for military.

Switching Waveforms

Read Cycle No. 1 (Notes 8, 9)

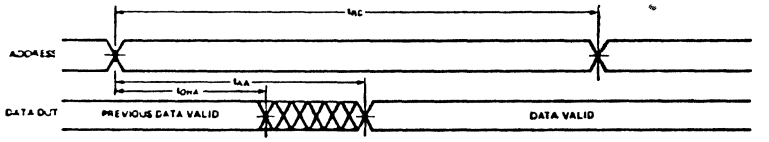
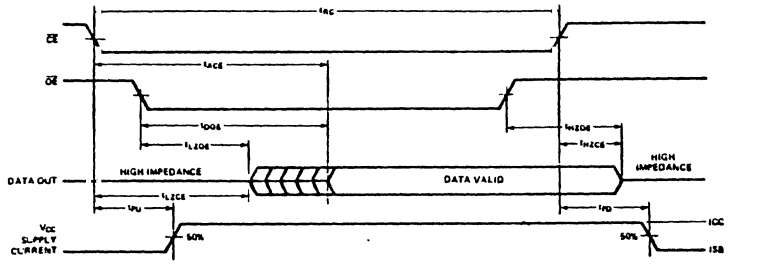


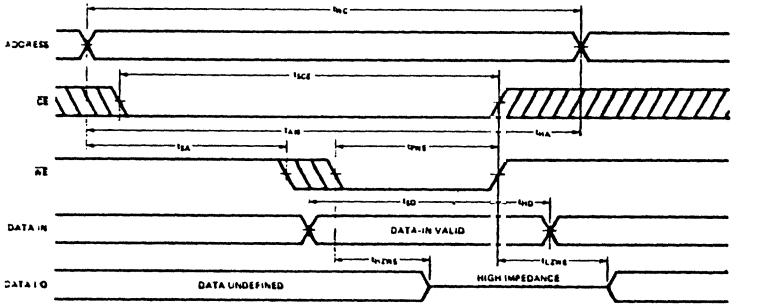
Figure 5.2.1.b DataSheet CY7C128 RAM

Switching Waveforms (Continued)

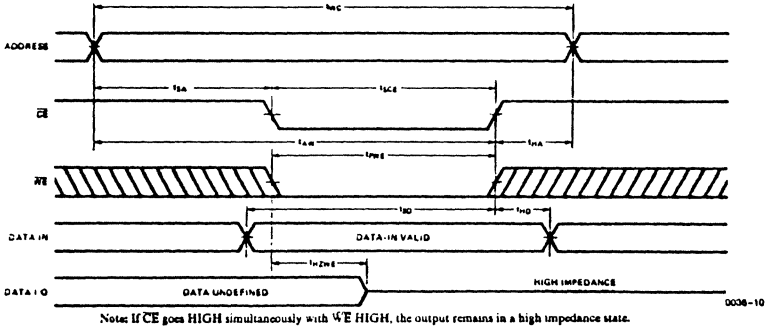
Read Cycle No. 2 (Notes 8, 10)



Write Cycle No. 1 (WE Controlled) (Notes 3, 7)



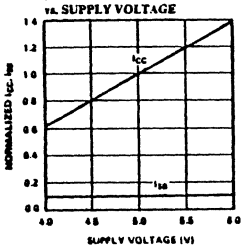
Write Cycle No. 2 (CE Controlled) (Notes 3, 7)



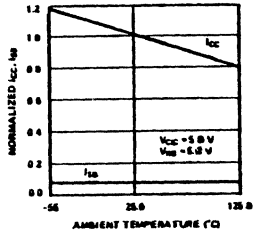
Note: If CE goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state.

Typical DC and AC Characteristics

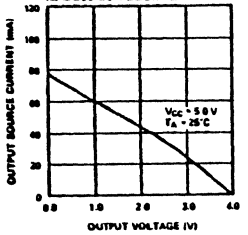
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



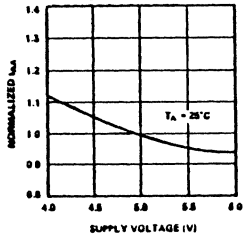
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



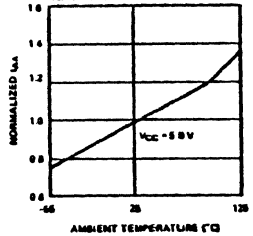
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



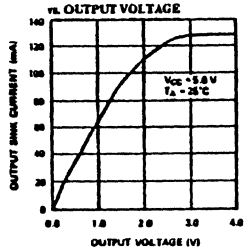
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



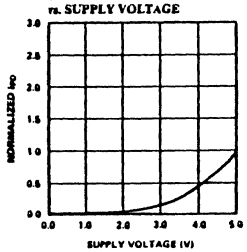
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



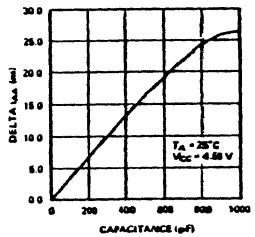
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME

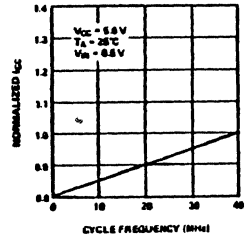


Figure 5.2.1.c DataSheet CY7C128 RAM

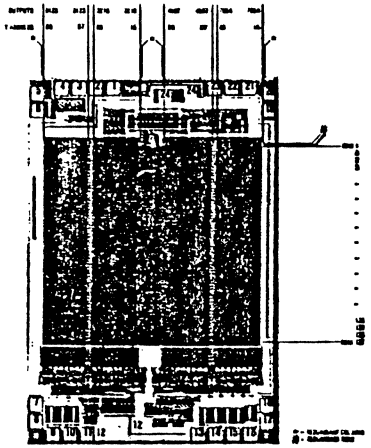
Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C128-25PC	P13	Commercial
	CY7C128-25SC	S13	
	CY7C128-25DC	D14	
	CY7C128-25LC	L53	
35	CY7C128-35PC	P13	Commercial
	CY7C128-35SC	S13	
	CY7C128-35DC	D14	
	CY7C128-35LC	L53	
	CY7C128-35DMB	D14	Military
	CY7C128-35LMB	L53	
45	CY7C128-45PC	P13	Commercial
	CY7C128-45SC	S13	
	CY7C128-45DC	D14	
	CY7C128-45LC	L53	
	CY7C128-45DMB	D14	Military
	CY7C128-45LMB	L53	
55	CY7C128-55PC	P13	Commercial
	CY7C128-55SC	S13	
	CY7C128-55DC	D14	
	CY7C128-55LC	L53	
	CY7C128-55DMB	D14	Military
	CY7C128-55LMB	L53	

Address Designators

Address Name	Address Function	Pin Number
A_0	Y_3	8
A_1	Y_2	7
A_2	Y_1	6
A_3	Y_0	5
A_4	X_2	4
A_5	X_4	3
A_6	X_3	2
A_7	X_0	1
A_8	X_1	23
A_9	X_4	22
A_{10}	X_1	19

Bit Map



0036-12

1024 x 8 Dual Port Static RAM

Features

- 0.8 micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- Master CY7C130 easily expands data bus width to 16 or more bits using SLAVE CY7C140
- BUSY output flag on CY7C130; BUSY input on CY7C140
- INT flag for port to port communication

Functional Description

The CY7C130/CY7C140 are high speed CMOS 1K x 8 Dual Port Static RAMS. Two ports are provided permitting independent access to any location in memory. The CY7C130 can be utilized as either a stand-alone 8-bit Dual Port Static RAM or as a MASTER Dual Port RAM in conjunction with the CY7C140 SLAVE Dual Port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, Bit-Slice, or multiprocessor designs.

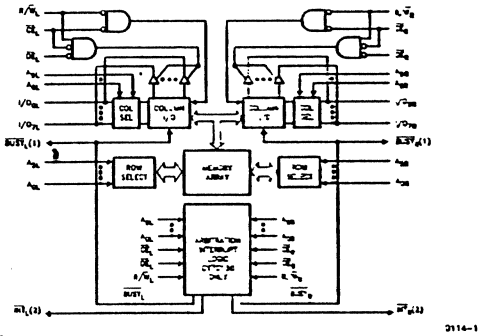
Each port has independent control pins; Chip Enable (CE), Write Enable (WE), and Output Enable (OE). Two flags are provided on each port, BUSY and INT. BUSY signals that the port is trying to access the same location currently being accessed by the other port. INT is an interrupt flag indicating that data has been placed in a unique location by the other port. An automatic power down feature is controlled independently on each port by the Chip Enable (CE) pin.

The CY7C130/CY7C140 are available in both 48-pin DIP and 52-pin LCC.

A die coat is used to insure alpha immunity.

2

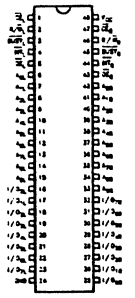
Logic Block Diagram



0114-1

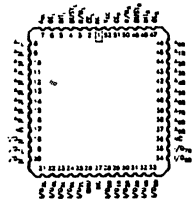
Notes:
1. CY7C130 (Master): BUSY is open drain output and requires pullup resistor.
   CY7C140 (Slave): BUSY is input.
2. Open drain outputs: pullup resistor required.

Pin Configurations



DIP
Top View

0114-2



LCC
Top View

0114-3

Selection Guide

		7C130-35 7C140-35	7C130-45 7C140-45	7C130-55 7C140-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	120	120	120
	Military		150	150
Maximum Standby Current (mA)	Commercial	30	30	30
	Military		40	40

Figure 5.2.1.d DataSheet CY7C128 RAM

Figure 5.3.1.a Circuit diagram Timing board

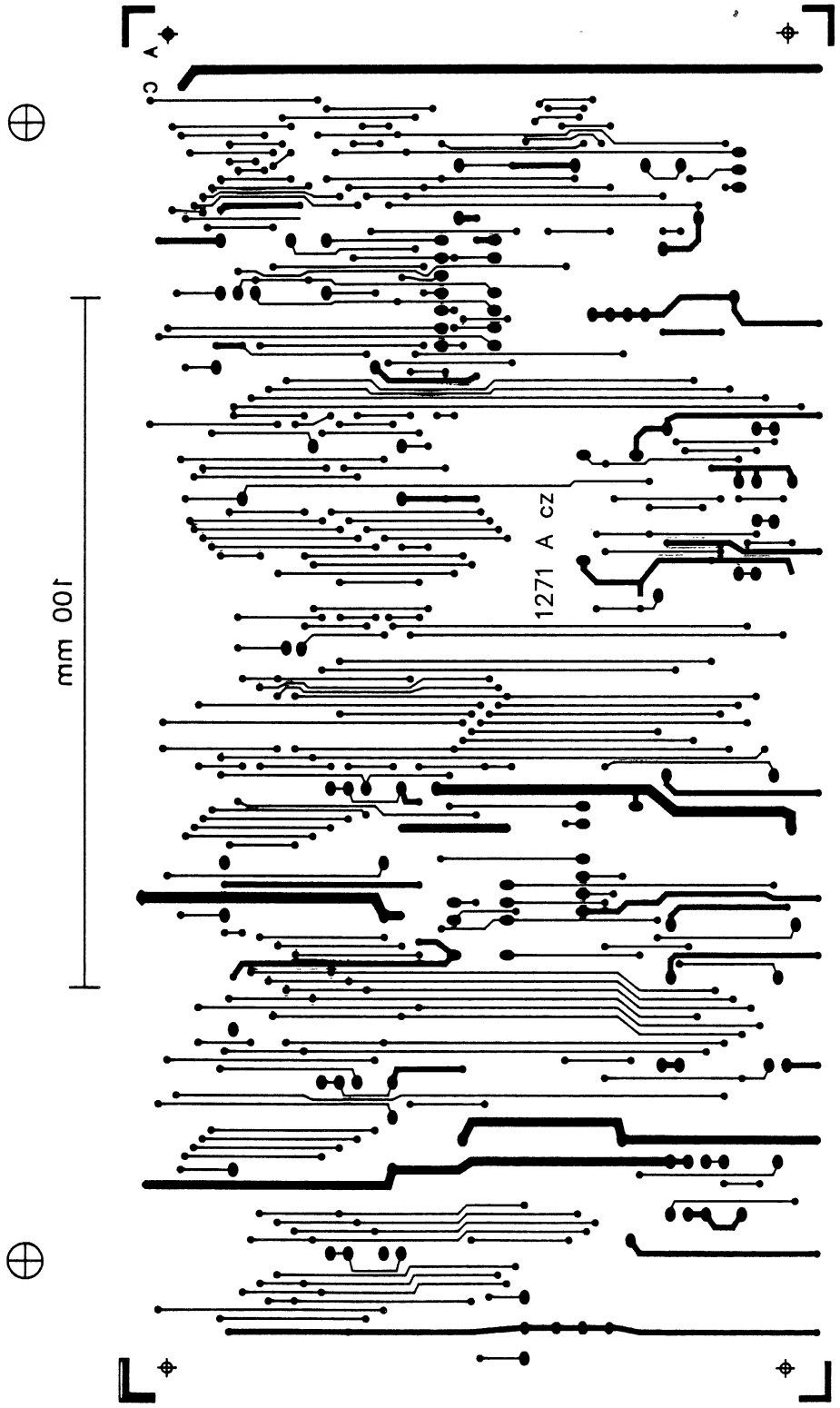


Figure 5.3.1.b PCB Layout Timing board

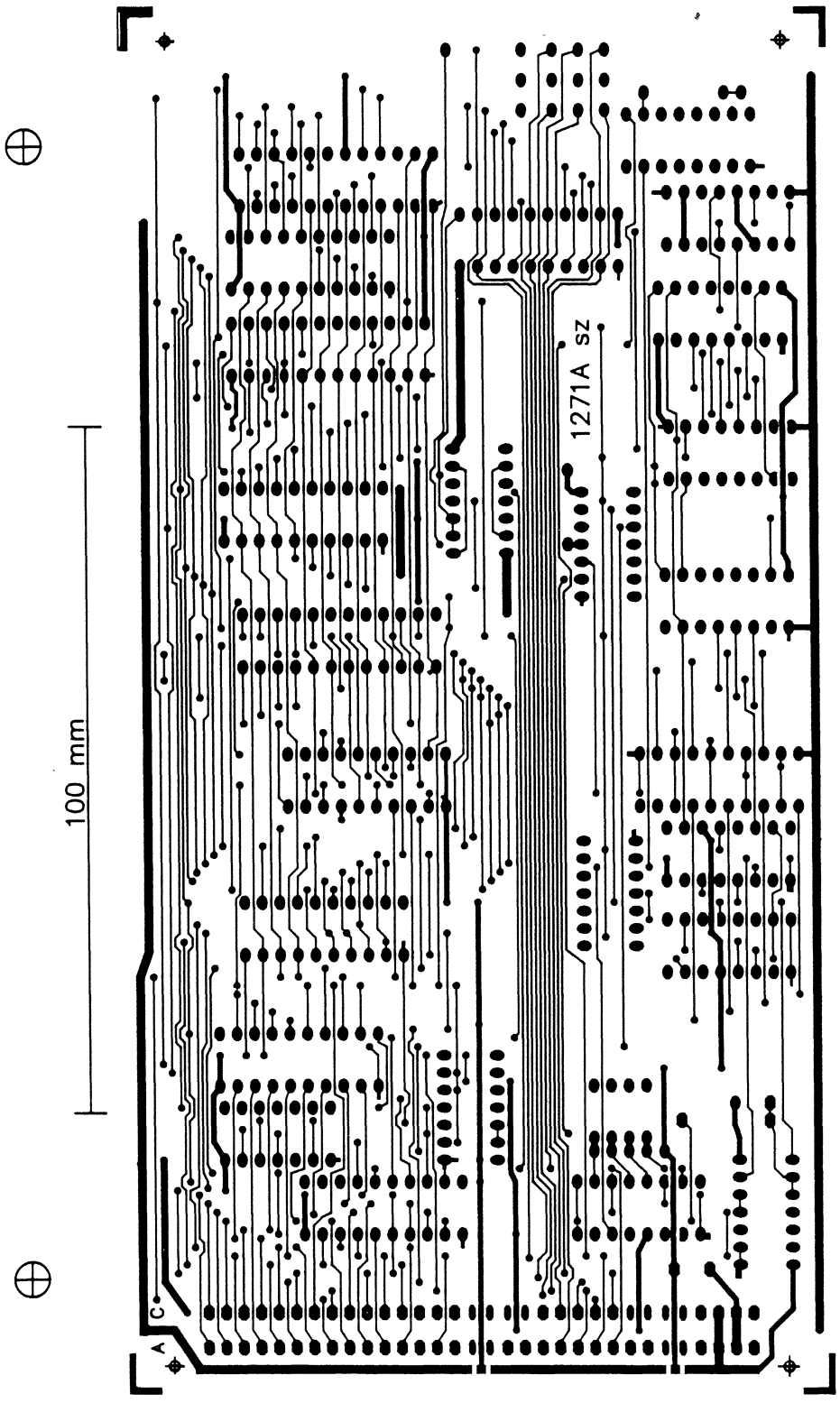


Figure 5.3.1.b PCB Layout Timing board

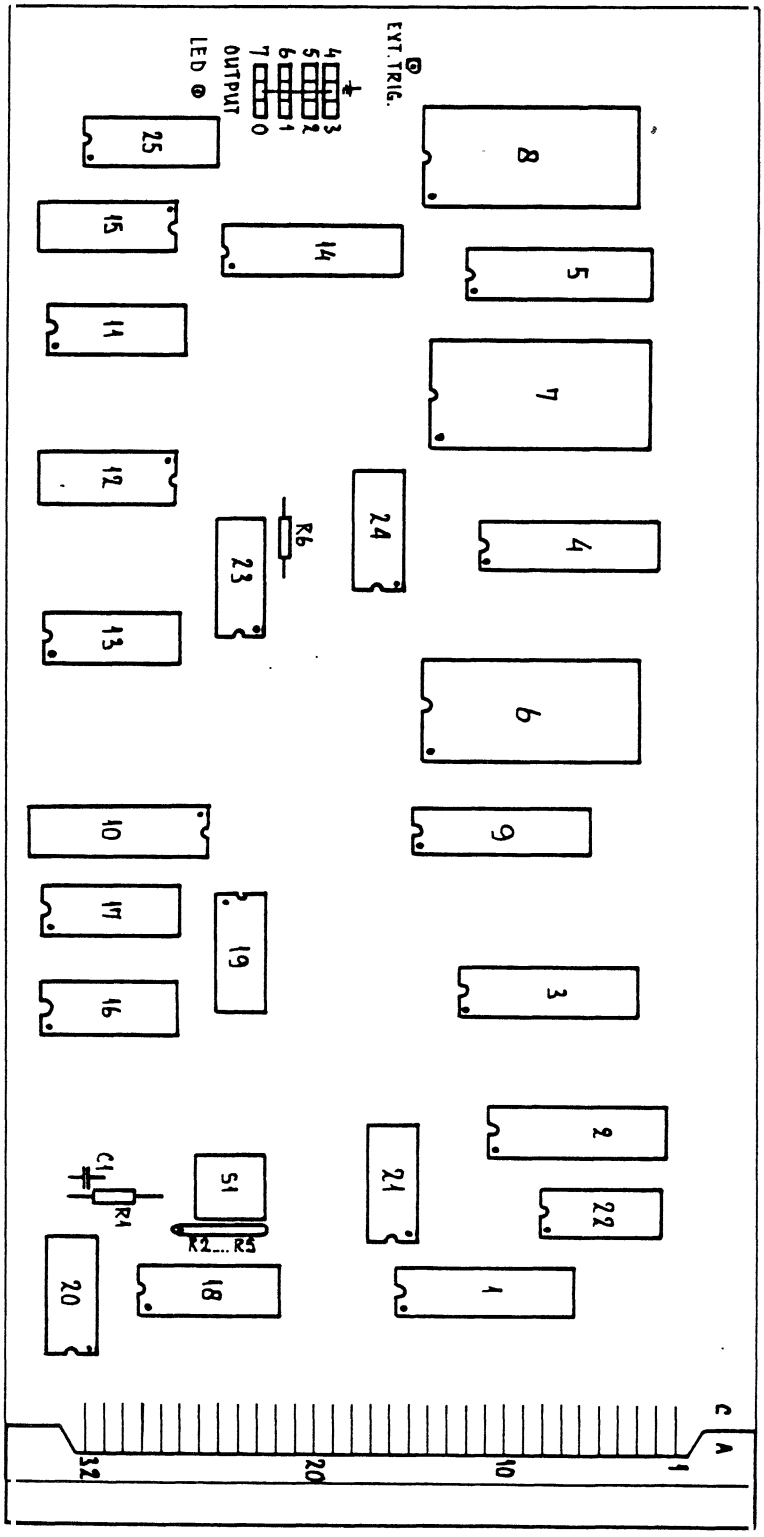


Figure 5.3.1.c Component Mounting Timing board

D	C	B	A	BETREFT: DEVELOPMENT OF SILT MEASURING METHODS	
WIJZIGINGEN				BENAMING: COMPONENT MOUNTING OF PCB 1271 A	
WATERLOOPKUNDIG LABORATORIUM DELFT				SCHAAL:	TEK.NR. 07403
				MATEN IN mm	
				x UITVOEREN	BEHOORT BIJ:
				GET.	A4
				D.D. 19-09-88	

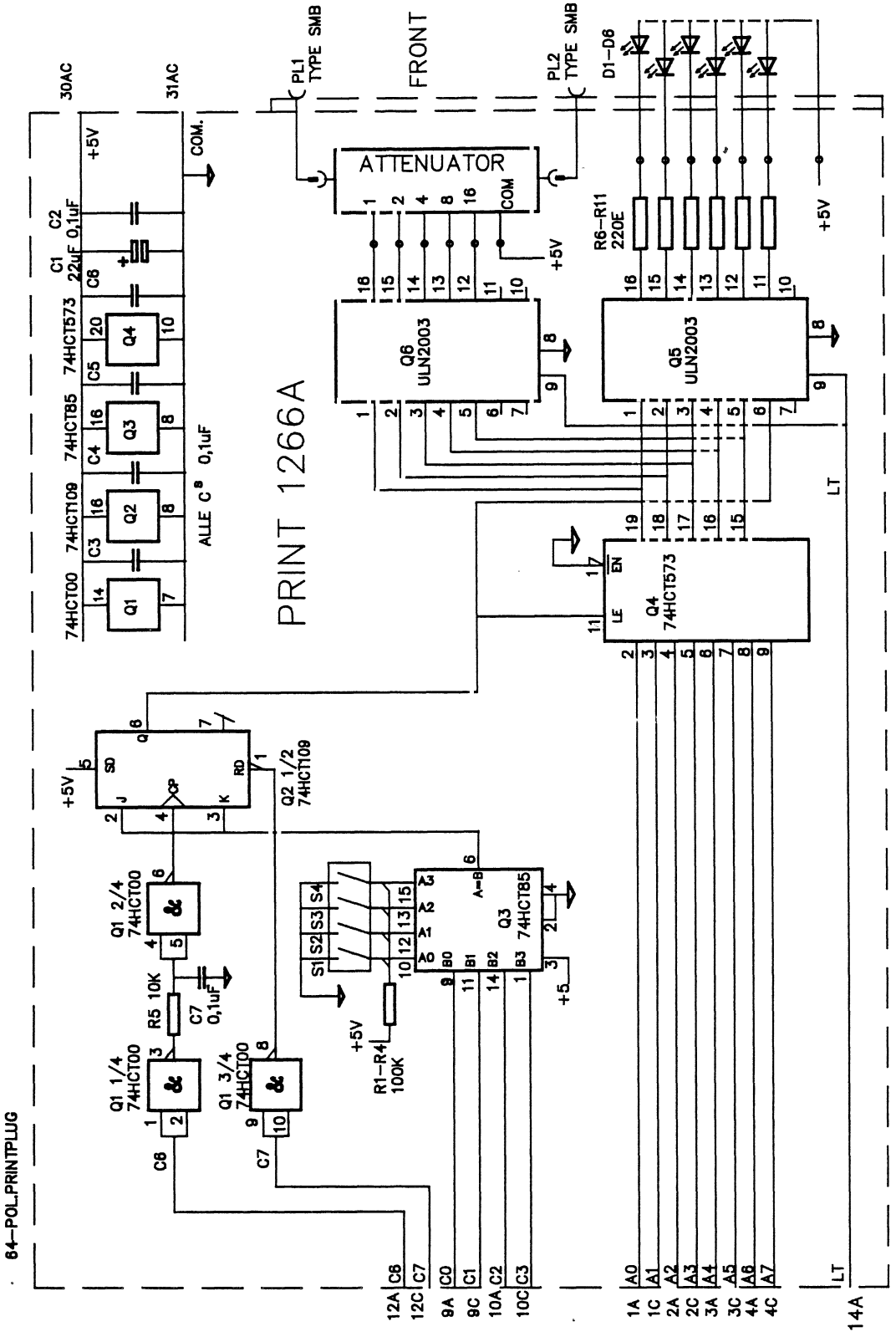


Figure 6.2.1.a Circuit diagram Attenuator board

BETREFT:	DEVELOPMENT OF SILT MEASURING METHODS	WIJZIGING	D
			C
BENAMING:	ATTENUATOR PROGRAMMER PRINT 1266 A		B 25/5/89 WAW
			A 03/08/'88 HS

WATERLOOPKUNDIG LABORATORIUM DELFT	SCHAAL:	TEK.NR.	07352SLK
	MATEN IN mm		
	GET: H.STEENMAN	A4	BEHOORT BIJ:
	D.D. 22/07/'88		

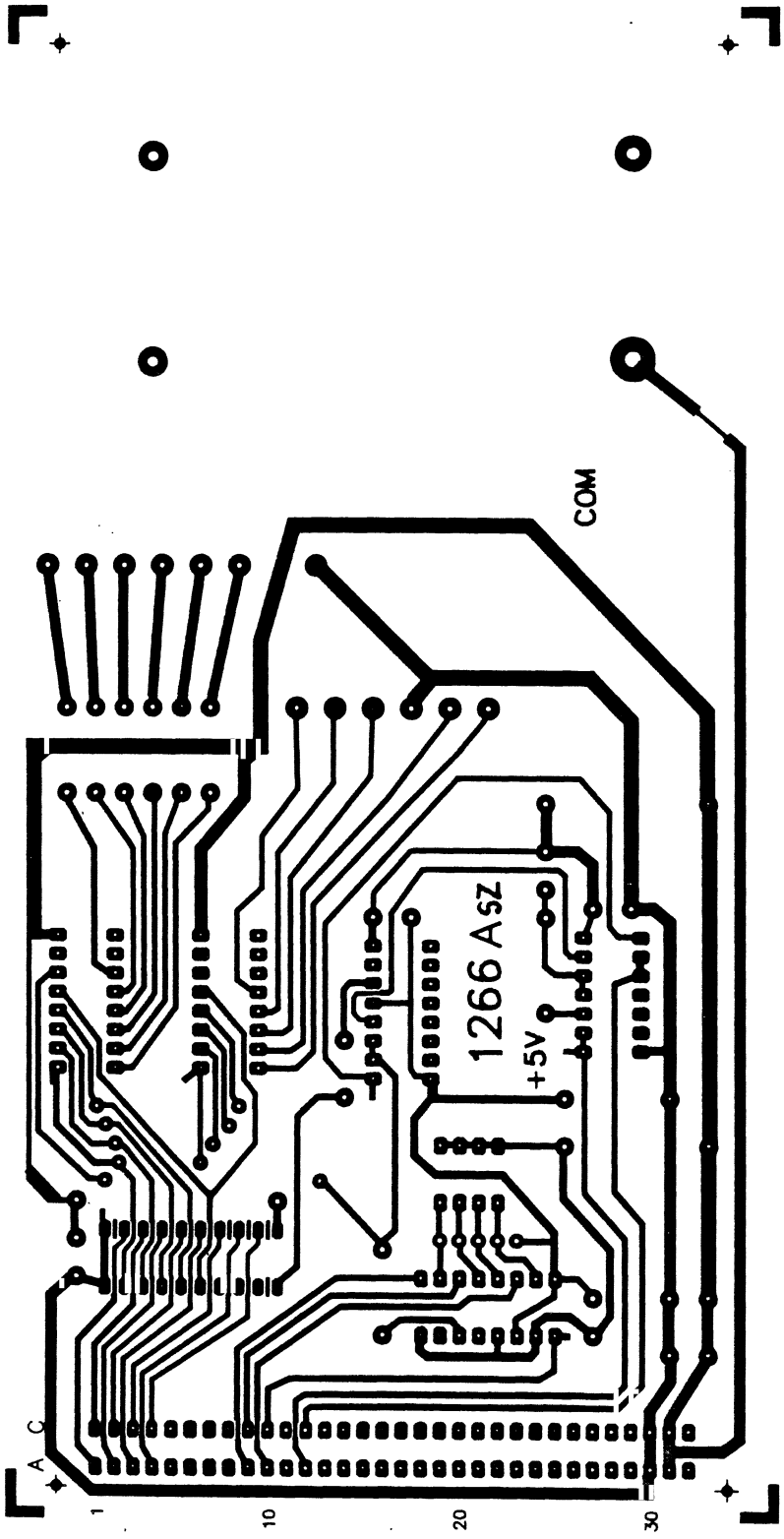


Figure 6.2.1.b PCB Layout Attenuator board

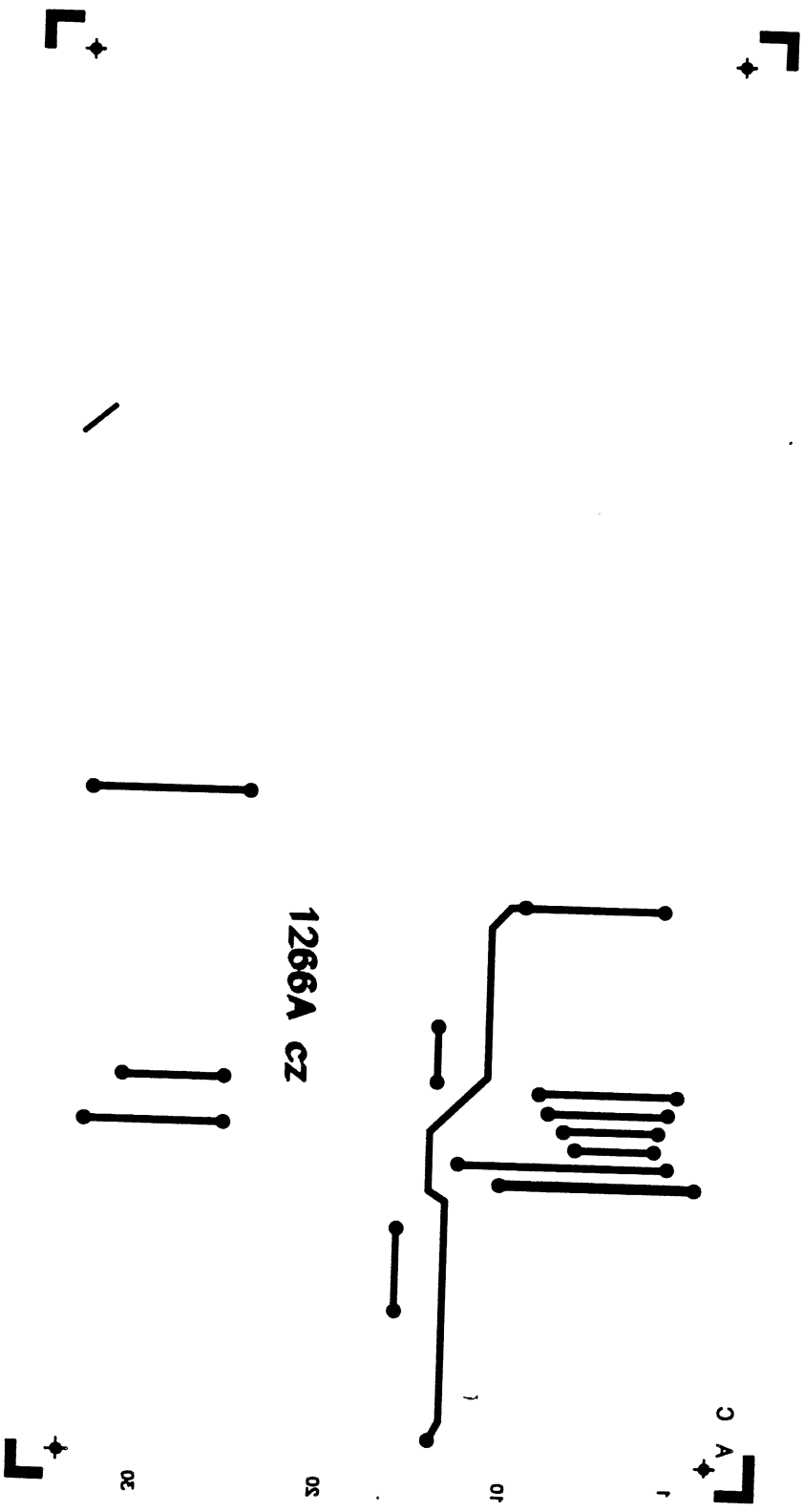


Figure 6.2.1.b PCB Layout Attenuator board

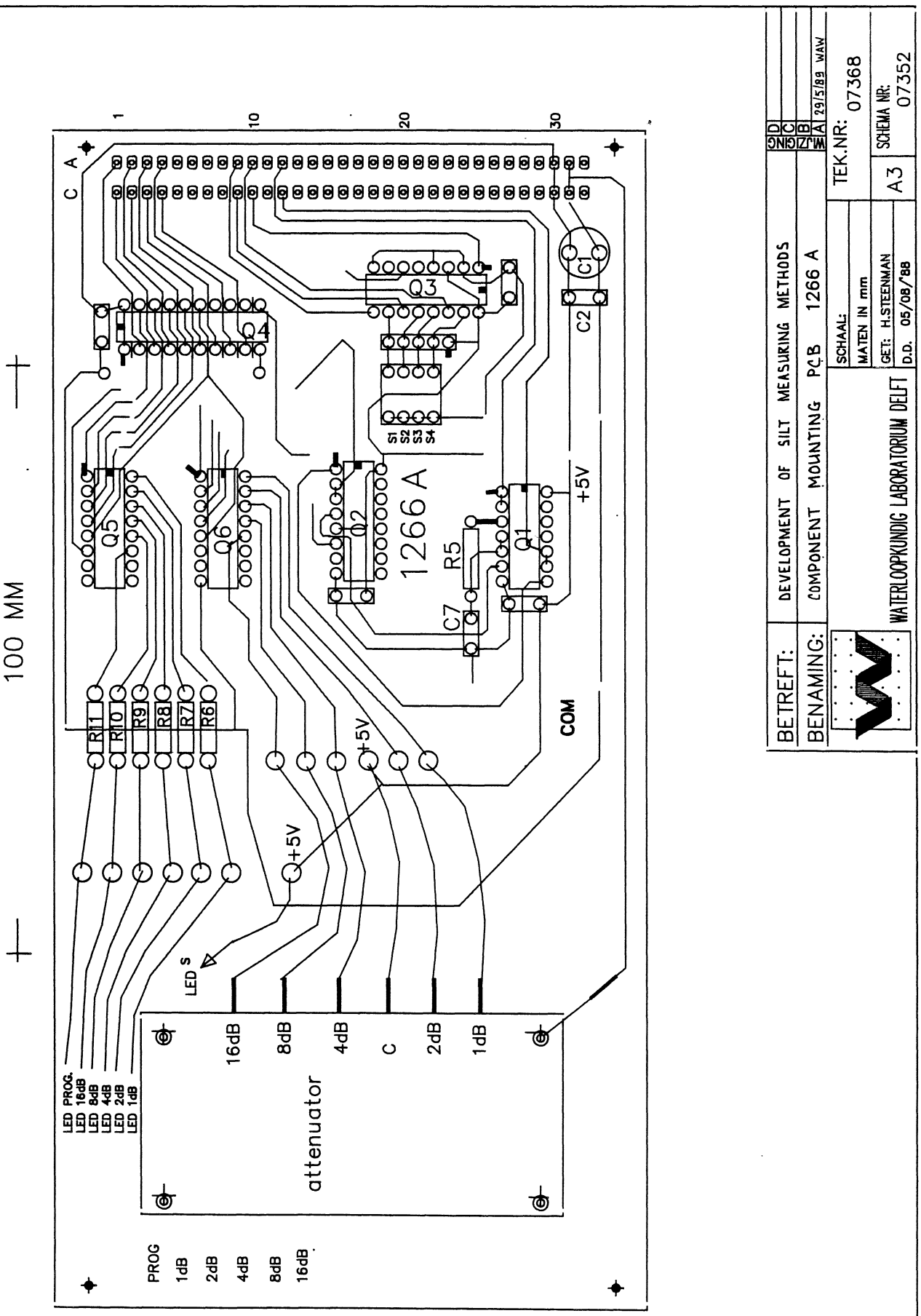
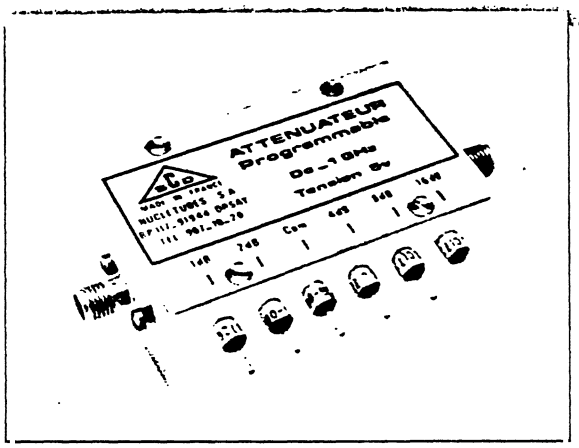


Figure 6.2.1.c Component Mounting Attenuator board

SCD atténuateur programmable

programmable attenuator



DC - 1000 MHz - 50 Ω

MODELE		AP 10 31
Bande de fréquence	Frequency range	DC – 1000 MHz
Attenuation dB		0 - 31 dB par pas de 1 dB* - 1 dB step
Pas	Step	1 - 2 - 4 - 8 - 16 dB
Pertes d'insertion	Insertion losses	2 dB - 1 GHz)
R.O.S.	V.S.W.R	1,4 : 1 max
Ondulation	Deviation	± 0,3 dB
Précision	Accuracy	± 0,3 dB
Temps de commutation	Switching time	400 μs
Alimentation	Power supply	+ 5 V (50 mA/pas) - (50 mA/step)
Puissance admissible	Input power	1 W

Figure 6.2.2 a Attenuator Specifications

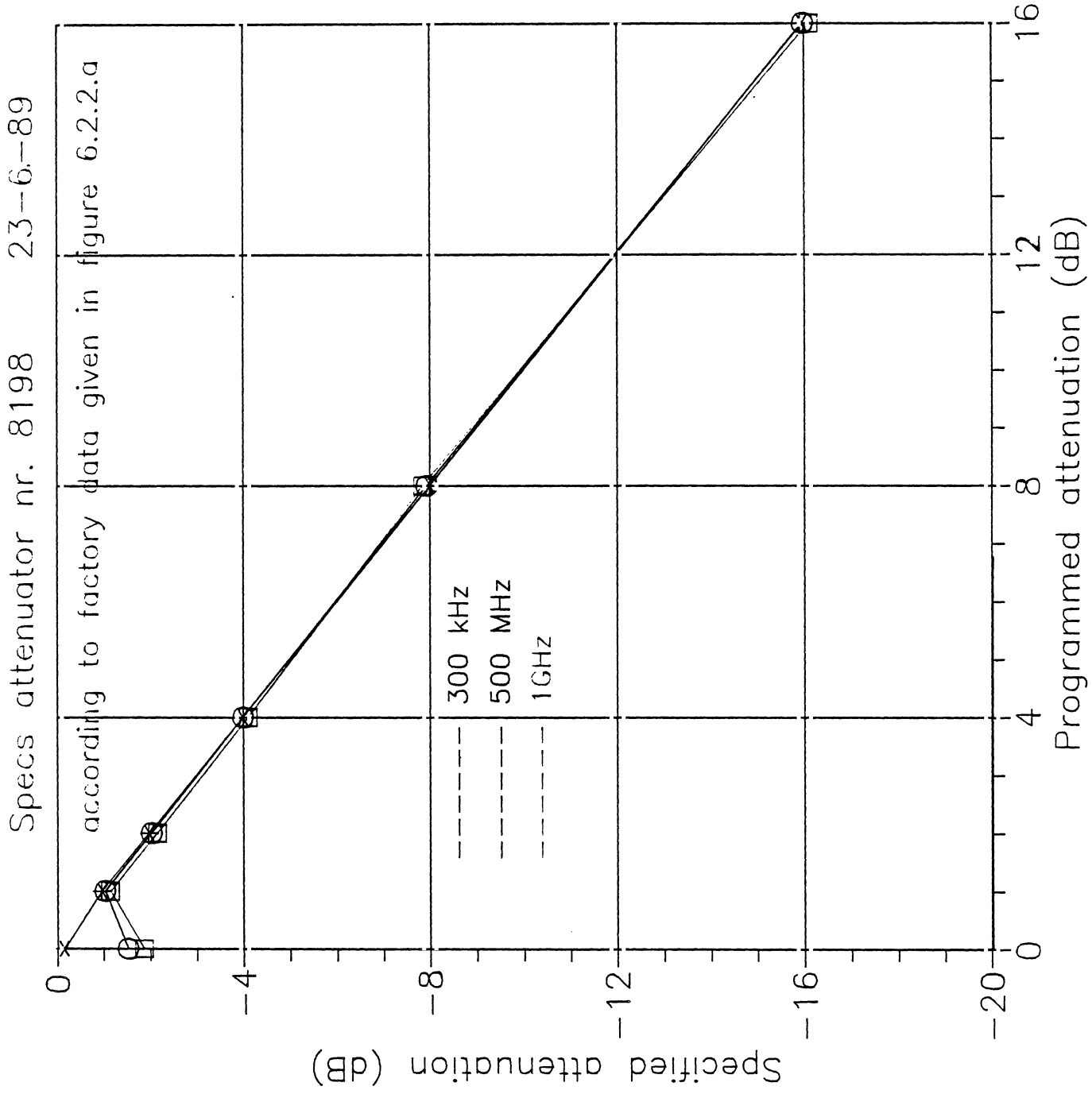


Figure 6.2.2.b Attenuator Specifications

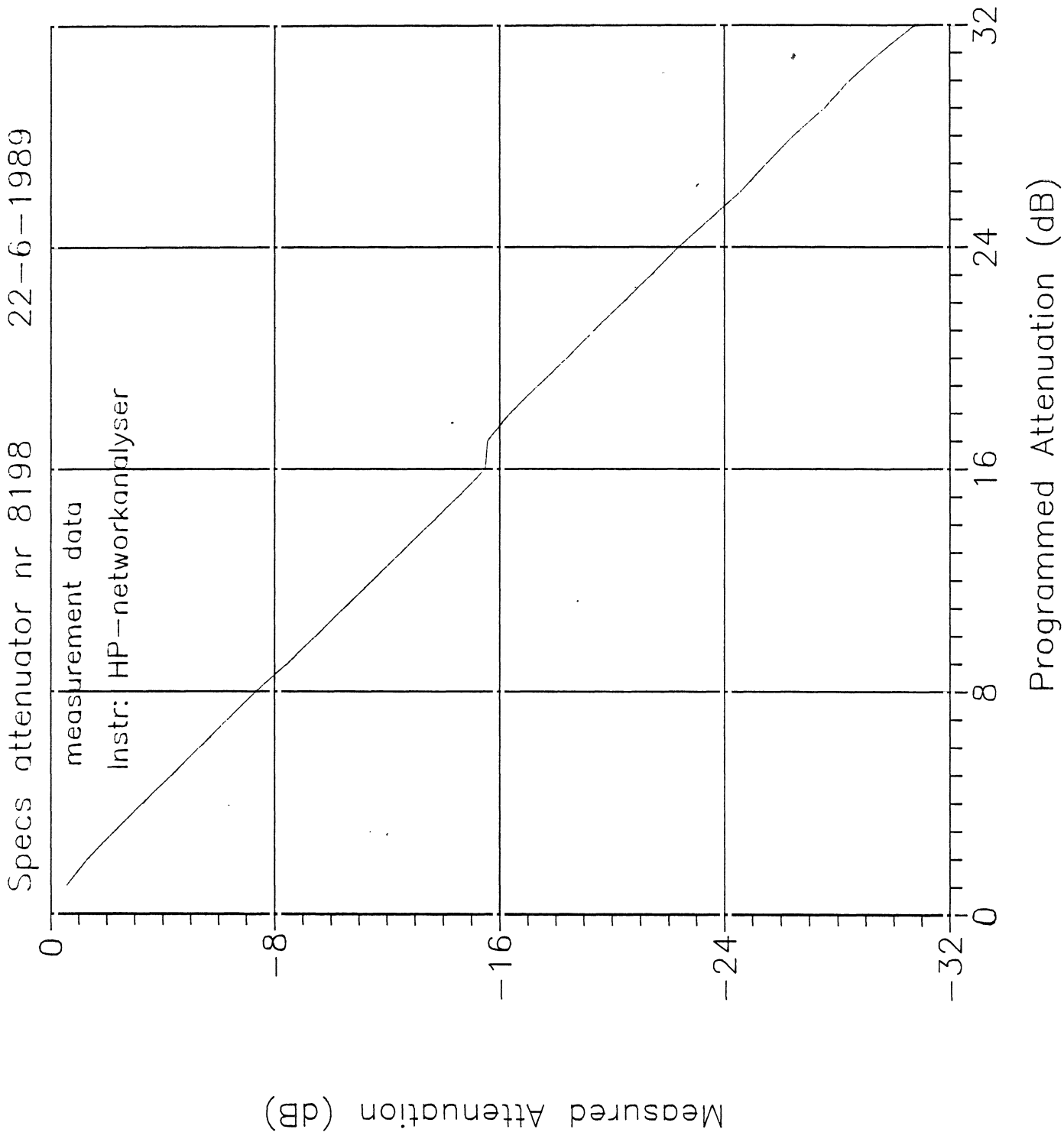


Figure 6.3.1 Measured Attenuator Specifications

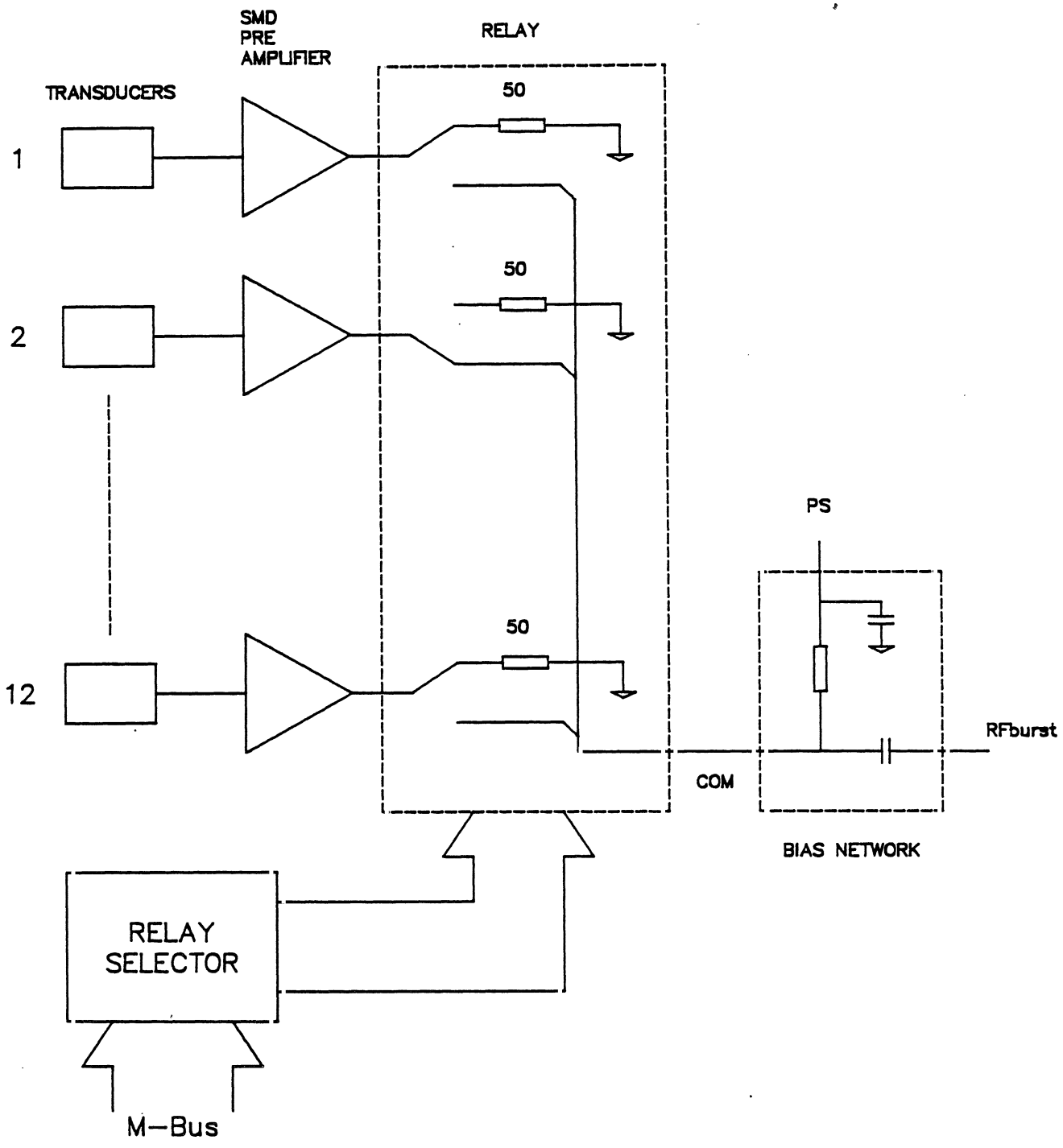
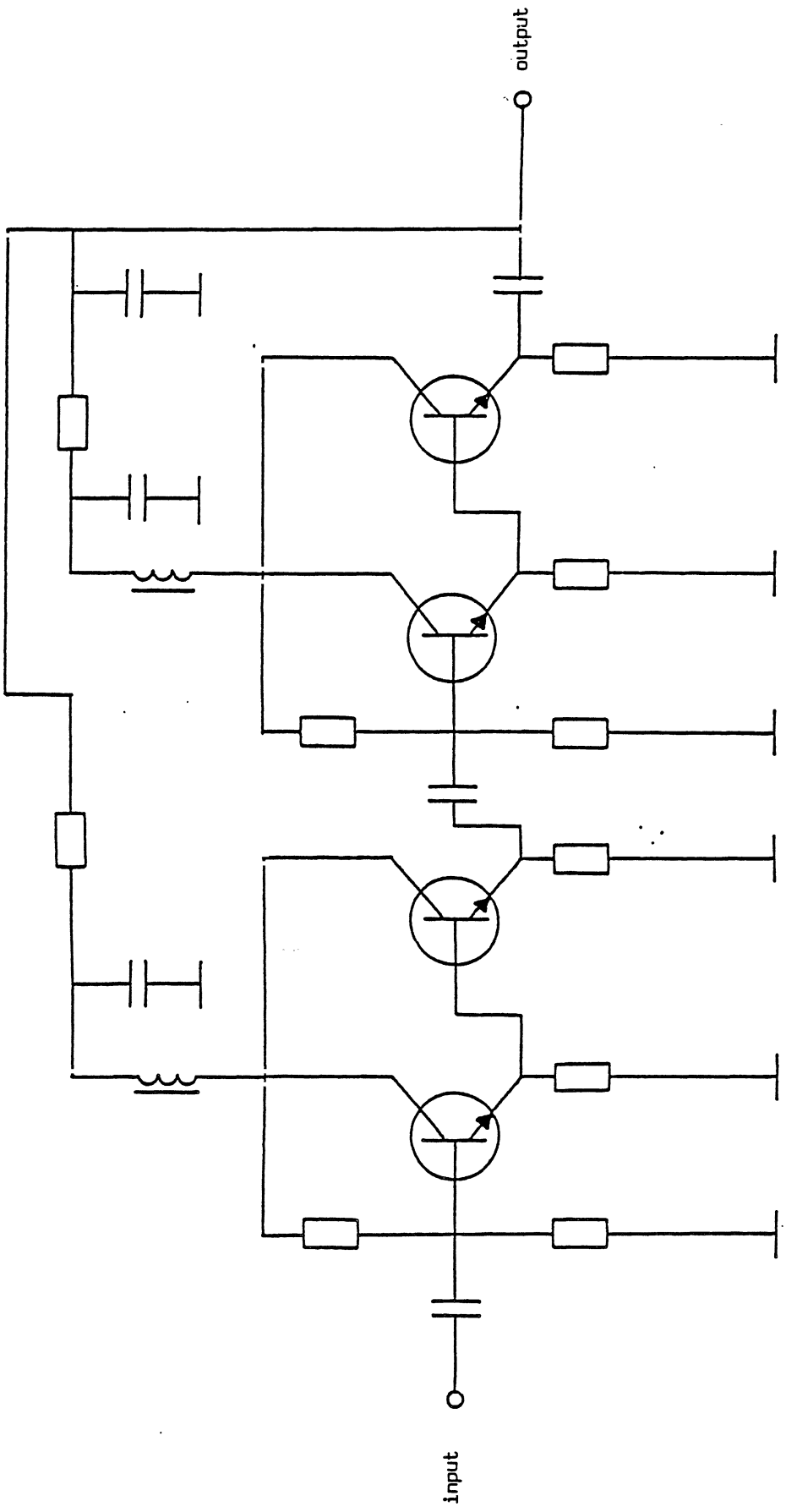


Figure 7.1 Configuration of the receiverside

BETREFT:	DEVELOPMENT OF SILT MEASURING METHODS	WIJZIGING D C B A
BENAMING:	CONFIGURATION OF RECEIVER SIDE	

WATERLOOPKUNDIG LABORATORIUM DELFT	SCHAAL: MATEN IN mm	TEK.NR. 07433SLK	
	GET: W.A.Westerveld D.D. 14–11–88	A4	BEHOORT BIJ:



AMPLIFIER CIRCUIT, 2005- en 4005 serie.

IMWAVE

RF & MICROWAVE ELECTRONICS

Figure 7.2.1 Principal circuit diagram SMD amplifiers

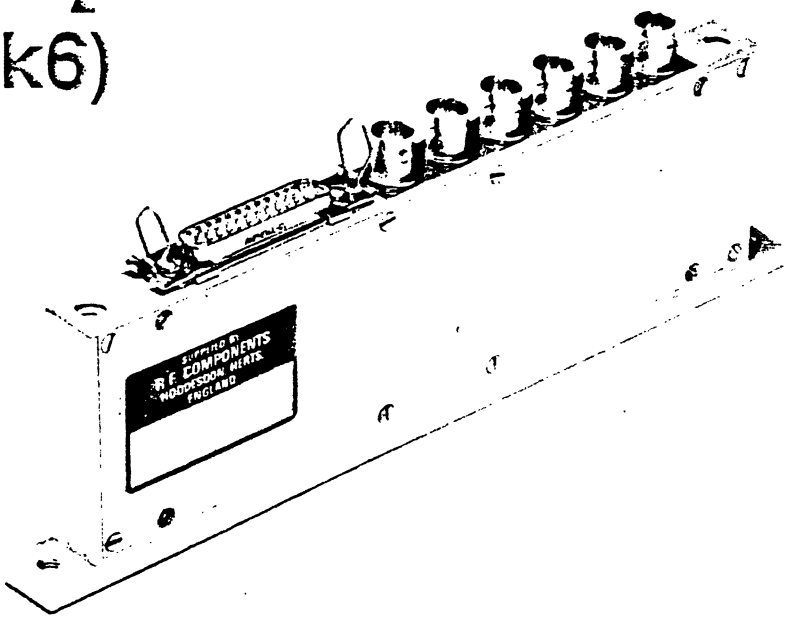
Coaxial Relays

50Ω SERIES 'C' (Mk6)

The series 'C' coaxial relay is a multiway unit designed for use from DC to UHF frequencies.

High reliability Reed switches are used in customer selectable configurations achieving excellent isolation, together with accurate resistive termination of unselected channels.

The standard range from 1 to 15 inputs catering for both 50Ω and 75Ω applications offers a selection of control circuitry and coaxial connectors. including the popular BNC and SMA.



Features

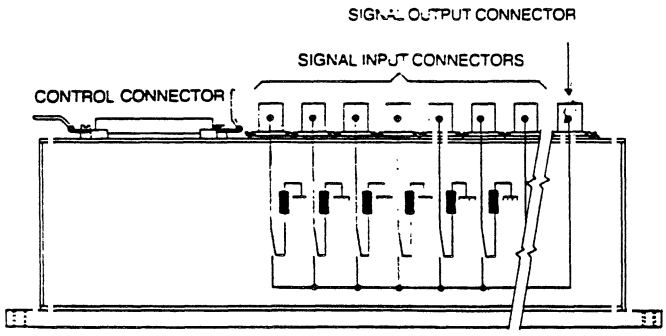
- Up to 15 Inputs Standard.
- Field Replaceable Parts.
- High Isolation.
- Bi-Directional Signal Switching.
- Useful from DC to UHF Frequencies.
- Over 10 million Permutations.
- High Reliability Reed Switches.
- Choice of Signal Input Loading.
- Hermetically Sealed Switch Contacts.
- High Insulation up to 5 x 10 - OHMS.

A VERSATILE SWITCH

Applications

- PTT.
- CCTV.
- Automation.
- Video Switching.
- Security/Surveillance.
- Aerial/Antenna Switching.
- Computer Selection.
- Transducer Switching.
- Low Current Source Switching

SIGNAL CIRCUIT



CONTROL CIRCUIT

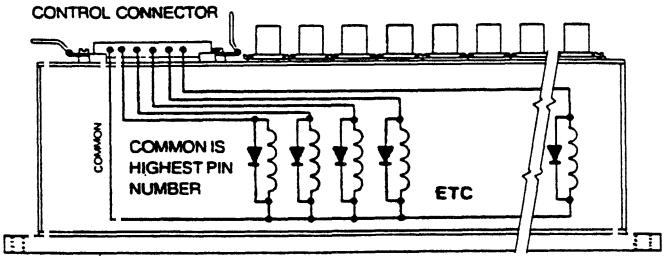


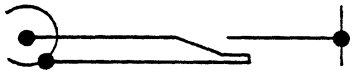
Figure 7.3.1.a Relays Specifications

SEE INTERFACE OPTIONS ON BACK PAGE

COAXIAL RELAYS 5011 SERIES 'C' (MK5)

RF COMPONENTS
RF COMPONENTS (COAXIAL SYSTEMS) LTD.
Plumpton House, Plumpton Road, Rye Park, Hoddesdon,
Hertfordshire, England EN11 0LB.
Telephone: Hoddesdon (0992) 463603 Telex: 265849

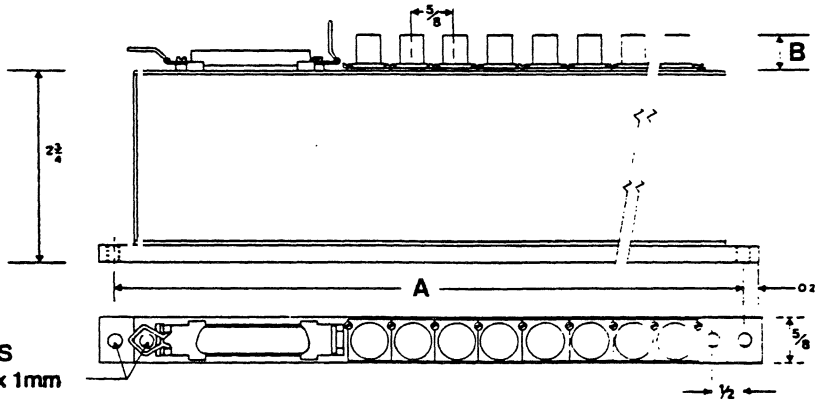
REED ASSEMBLY INFORMATION

Termination	SWITCH FUNCTION Switches Drawn in De-energised state	Code	MAXIMUM INITIAL Contact Resistance mΩ	Maximum Contact Rating VA	VRMS	mA	TYPICAL Isolation (– dB) ✱ 10 MHZ	40 MHZ	100 MHZ	400 MHZ
Non-shorting		31	100	10	100	250	60	54	42	28
		30	200	10	100	250	80	72	60	45
		✱40	200	3	28	250	>110	>110	110	70
		38	200	3	28	250	>110	>110	>110	84
Resistance	 50Ω 1/8 watt Resistor	11	100	3	28	250	50	41	30	16
		✱41	200	3	28	250	98	83	68	42
		46	200	3	28	250	>110	>110	>105	65
Short circuit		48	200	3	28	250	>110	>110	>110	80

HIGH INSULATION SWITCH

Termination	SWITCH FUNCTION Switches Drawn in De-energised state	Code	Contact Resistance mΩ	Contact Rating VA	VRMS	mA	Insulation Resistance Ω
Non-shorting		34	150	15	125	500	up to 5×10^{14}

DIMENSIONS



All dimensions in inches

PORTS OUT	IN	LENGTH A	PORTS OUT	IN	LENGTH A	PORTS OUT	IN	LENGTH A
1	1	5.750	✱1	6	8.875	1	11	12.000
✱1	2	6.375	1	7	9.500	1	12	12.625
1	3	7.000	✱1	8	10.125	1	13	13.250
✱1	4	7.625	1	9	10.750	✱1	14	13.875
1	5	8.250	✱1	10	11.375	1	15	14.500

✱Preferred Feature. For 75Ω and 93Ω systems an

Figure 7.3.1.b Relays Specifications

All dimensions in inches

SIGNAL CONNECTORS

Code	Style	B Max	Coupling	Centre Contact
*01	BNC (50Ω)	0.6	Bayonet	Socket
03	SMC (50Ω)	0.4	Screw	Pin
05	SMB (50Ω)	0.4	Snap-on	Pin
07	Solder Pot (50Ω)	0.5	Solder	Pin
11	Microdot (50Ω)	0.3	Screw	Socket
15	SMA (50Ω)	0.4	Screw	Socket
17	Radiall mQ (50Ω)	0.7	Snap-on	Socket
19	1.8/5.6 (50Ω)	0.5		Socket

For 75Ω and 93Ω systems please consult the office.

COILS (at 20°C)

Code	Resistance Ω±10%	Voltage (VDC) Typical pull-in	Voltage (VDC) Recommended Range
*04	125	2.7	3.8 – 10.5
05	250	4.4	6.2 – 15.0
*12	500	5.7	8.0 – 21.2
13	750	7.1	10.0 – 25.9
*28	1000	12.6	17.7 – 30.0
50	4000	17.5	24.5 – 60.0

CONTROL CONNECTOR

Code	Style	Manufacturer
80	25 Pin D connector with Mating (Solder Bucket connector and backshell)	Amphenol, Cannon, Cinch, Souriau

HOW TO CONSTRUCT A PART NUMBER

C — 46 — 15 — 01 — 04 — E — 80 — 06 — (AAA)

- C — Series C
- 46 — REED ASSEMBLY STYLE
- 15 — Number of input ports
- 01 — Signal Connector Style
- 04 — Coil Code
- E — INTERFACE OPTION (see back page)
- 80 — Control Connector Style 80
- 06 — Design Status (Mk5)
- (AAA) — Variant Code (see below)

* **Where insertion loss, VSWR, return loss and operation above 400 MHz are important to your application, please contact the Sales Engineering Department for assistance.**

The above example shows a 15 input 'c' series relay having high isolation 'Reed Assemblies' fitted, which terminates all unselected inputs into individual 50Ω resistors.

The signal connectors are 50Ω BNC, and the 4V coils are interfaced with and driven by a Binary Decoder.

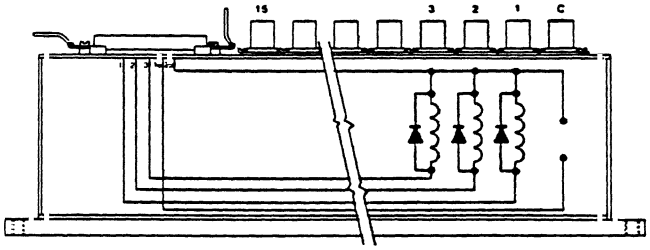
The Variant (AAA) is for a standard item and may be omitted from the part number.

Figure 7.3.1.c Relays Specifications

ARREF COMPONENTS (COAXIAL SYSTEMS) LTD.
Plumpton House, Plumpton Road, Rye Park, Hoddesdon,
Hertfordshire, England EN11 0LB.
Telephone: Hoddesdon (0992) 463603 Telex 265849

INTERFACE OPTION D

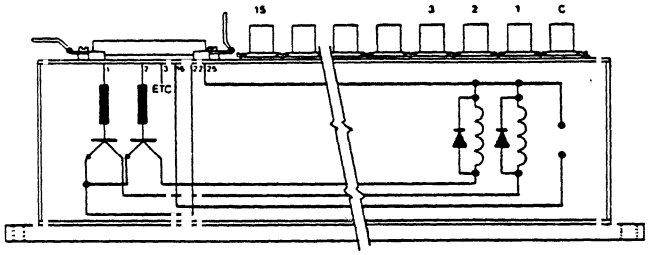
Coil & Transient Protection Diode Only



PIN DESIGNATION
1 Select O/P1
2 Select O/P2
3 Select O/P3
▼
15 Select O/P15
16 Select common O/P (only available with certain variants)
22 OV D.C supply
23 Chassis Earth
25 +ve D.C. supply

INTERFACE OPTION C

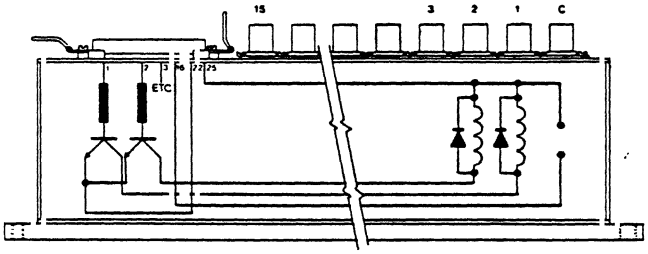
CMOS Compatible (6-15 VDC LOGIC)



PIN DESIGNATION
1 Select O/P1
2 Select O/P2
3 Select O/P3
▼
15 Select O/P15
16 Select common O/P (only available with certain variants.)
23 Chassis Earth
25 +ve D.C. supply (to be ≥ logic supply)

INTERFACE OPTION T

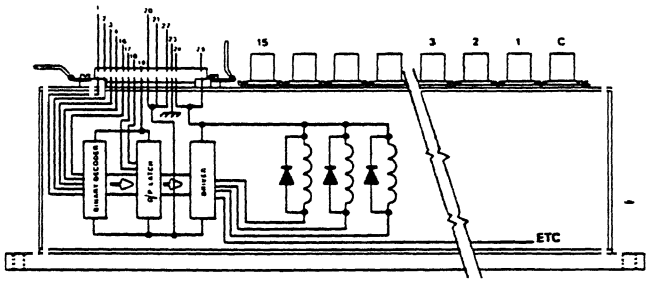
TTL Compatible (5 VDC LOGIC)



PIN DESIGNATION
1 Select O/P1
2 Select O/P2
3 Select O/P3
▼
15 Select O/P15
16 Select common O/P (only available with certain variants.)
23 Chassis Earth
25 +ve D.C. supply (to be ≥ logic supply)

INTERFACE OPTION E

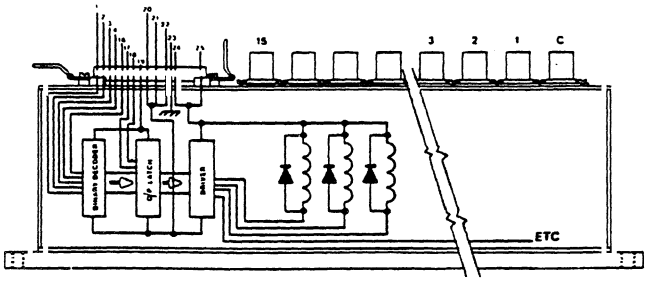
Binary Decoder with Latches (5 VDC LOGIC)



PIN DESIGNATION
1
2 } Binary Coded
3 } Address
4
16 Enable
17 Set/Reset
18 Clear
19 Logic Supply (5V DC)
20 Logical OVDC
21
22 } OVDC Supply
23 Chassis Earth
24 } +VE DC Coil Supply
25 } (to be ≥ logic supply)

INTERFACE OPTION K

Binary Decoder with Latches (6-15 VDC LOGIC)



PIN DESIGNATION
1
2 } Binary Coded
3 } Address
4
16 Enable
17 Set/Reset
18 Clear
19 Logic Supply (+6 to +15 VDC)
20 Logical OVDC
21
22 } OVDC Supply
23 Chassis Earth
24 } +VE DC Coil Supply
25 } (to be ≥ logic supply)

LOCAL AGENT

Figure 7.3.1.d Relays Specifications

RE COMPONENTS
ARREE COMPONENTS (COAXIAL SYSTEMS) LTD.
Plumpton House, Plumpton Road, Rye Park, Hoddesdon
Hertfordshire, England EN11 0LB
Telephone: Hoddesdon (0992) 463603 Telex: 265849

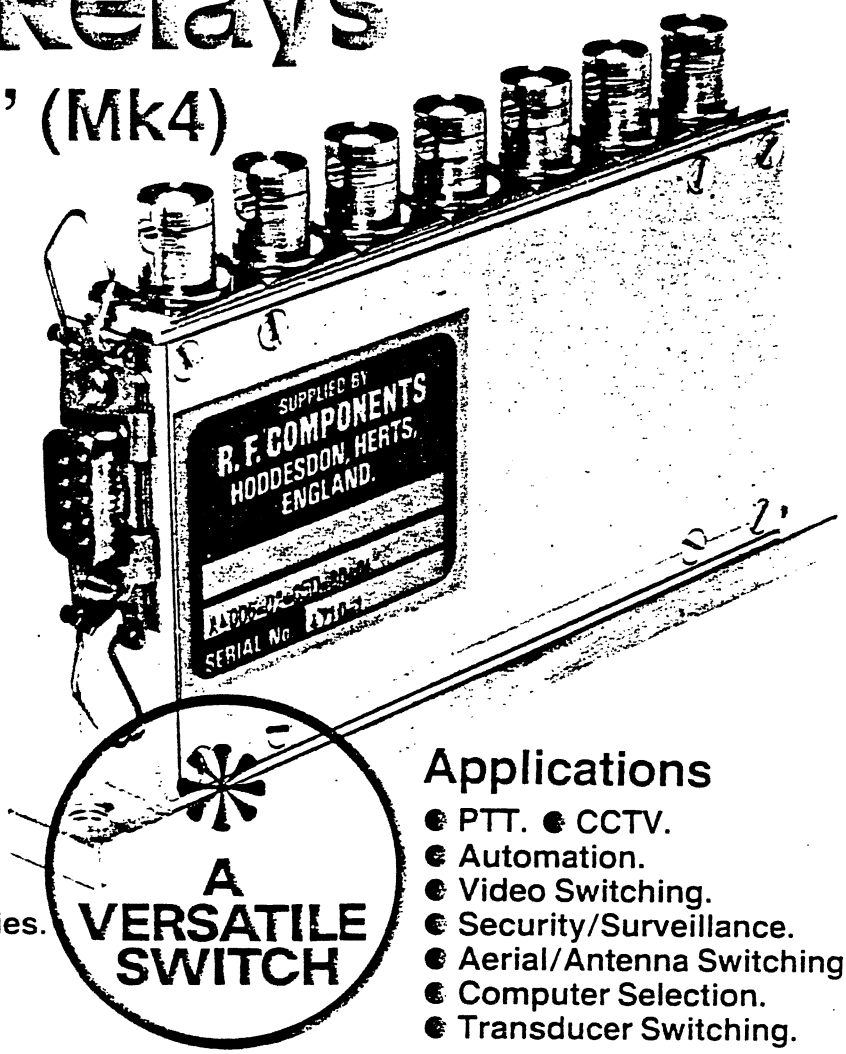
Coaxial Relays

50Ω SERIES 'A' (Mk4)

The series 'A' coaxial relay is a multiway unit designed for use from DC to UHF frequencies.

High reliability Reed switches are used in customer selectable configurations achieving excellent isolation, together with accurate resistive termination of unselected channels.

The standard range from 1 to 32 inputs catering for both 50Ω and 75Ω applications offers a selection of control voltages and coaxial connectors, including the popular BNC and SMA.



A VERSATILE SWITCH

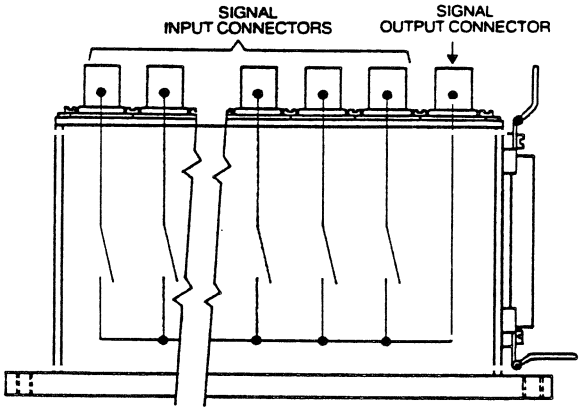
Features

- Up to 32 Ways.
- Field Replaceable Parts.
- High Isolation.
- Bi-Directional Signal Switching.
- Useful from DC to UHF Frequencies.
- Over 10 million Permutations.
- High Reliability Reed Switches.
- Choice of Signal Input Loading.

Applications

- PTT. • CCTV.
- Automation.
- Video Switching.
- Security/Surveillance.
- Aerial/Antenna Switching.
- Computer Selection.
- Transducer Switching.

SIGNAL CIRCUIT



CONTROL CIRCUIT

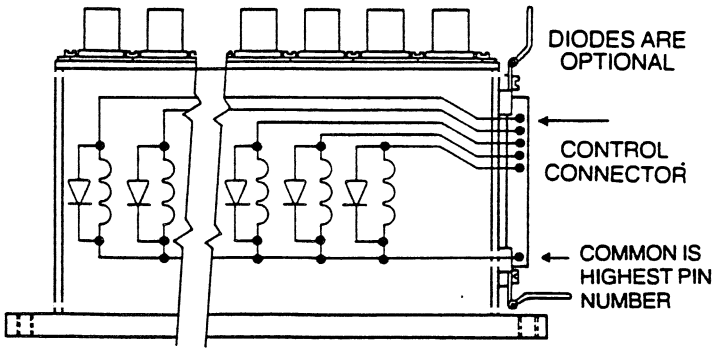
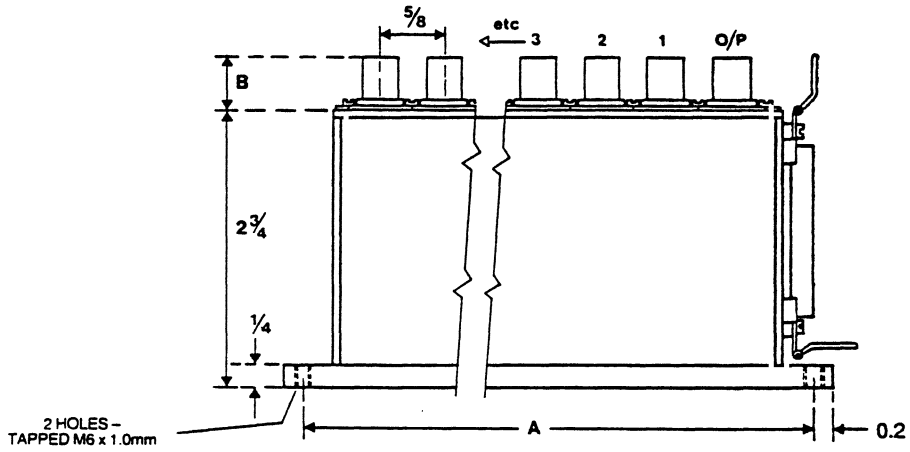


Figure 7.3.1.e Relays Specifications

RF COMPONENTS
ARREF COMPONENTS (COAXIAL SYSTEMS) LTD.
Plumpton House, Plumpton Road, Rye Park, Hoddesdon,
Hertfordshire, England EN11 0LB.
Telephone: Hoddesdon (0992) 463603 Telex: 265849

DIMENSIONS



All dimensions in inches

	Ports Out	Ports In	Length A	Control Conn. Size (Pins) 80	81	82	84	85
	1	1	2.000	9	17	9	2	16
*	1	2	2.625	9	17	9	3	16
*	1	3	3.250	9	17	9	4	16
*	1	4	3.875	9	17	9	5	16
*	1	5	4.500	9	17	9	—	16
	1	6	5.125	9	17	9	—	16
	1	7	5.750	9	17	9	—	16
*	1	8	6.375	9	17	9	—	16
	1	9	7.000	15	17	15	—	16
*	1	10	7.625	15	17	15	—	16
	1	11	8.250	15	17	15	—	16
*	1	12	8.875	15	17	15	—	16
	1	13	9.500	15	17	15	—	34
*	1	14	10.125	15	17	15	—	34
	1	15	10.750	25	17	25	—	34
*	1	16	11.375	25	17	25	—	34
	1	17	12.000	25	25	25	—	34
	1	18	12.625	25	25	25	—	34
	1	19	13.250	25	25	25	—	34
*	1	20	13.875	25	25	25	—	34
	1	21	14.500	25	25	25	—	34
	1	22	15.125	25	25	25	—	34
	1	23	15.750	25	25	25	—	34
*	1	24	16.375	25	25	25	—	34
	1	25	17.000	—	33	—	—	34
	1	26	17.625	—	33	—	—	34
	1	27	18.250	—	33	—	—	34
	1	28	18.875	—	33	—	—	34
	1	29	19.500	—	33	—	—	34
	1	30	20.125	—	33	—	—	34
	1	31	20.750	—	33	—	—	—
	1	32	21.375	—	33	—	—	—

* *Preferred Feature*

All dimensions in inches

REED ASSEMBLY INFORMATION

Termination	SWITCH FUNCTION Switches Drawn in De-energised state	Code	MAXIMUM INITIAL Contact Resistance mΩ	Maximum Contact Rating VA	VRMS	mA	TYPICAL Isolation (– dB) * 10 MHZ	40 MHZ	100 MHZ	400 MHZ
		31	100	10	100	250	60	54	42	28
Non-shorting		30	200	10	100	250	80	72	60	45
		*40	200	3	28	250	>110	>110	110	70
		38	200	3	28	250	>110	>110	>110	84
Resistance	50Ω 1/8 watt Resistor	11	100	3	28	250	50	41	30	16
		*41	200	3	28	250	98	83	68	42
		46	200	3	28	250	>110	>110	>105	65
Short circuit		48	200	3	28	250	>110	>110	>110	80
Non-shorting	Magnetic latch	33	100	5	150	500	55	43	34	22

Figure 7.3.1.f Relays Specifications

* *Preferred Feature* *For 75Ω and 93Ω and High Insulation Systems and any technical problems please consult the office.*

CONTROL CONNECTOR

	Code	Style	Manufacturer
*	80	D connector with Mating (Solder Bucket) Connector & Backshell	Amphenol, Cannon, Cinch, Souriau.
	81	Amphenol 223 with Mating Connector	Amphenol 223
	82	D Connector	Cannon
	84	Solder Post	——
	85	Ribbon Wire Header with Latches plus Mating Socket & strain relief.	Amphenol FRC2, 3M Scotchflex Varelco 8289, T&B/ANSLEY

SIGNAL CONNECTORS

	Code	Style	B Max	Coupling	Centre Contact
*	01	BNC (50Ω)	0.6	Bayonet	Socket
	03	SMC (50Ω)	0.4	Screw	Pin
	05	SMB(50Ω)	0.4	Snap-on	Pin
	07	Solder Pot (50Ω)	0.5	Solder	Pin
	11	Microdot (50Ω)	0.3	Screw	Socket
	15	SMA (50Ω)	0.4	Screw	Socket
	19	1.8/5.6 (50Ω)	0.5		Socket

COILS (at 20°C)

	Code	Resistance Ω± 10%	Voltage (VDC) Typical pull in	Voltage (VDC) Recommended Range
*	04	125	2.7	3.8–10.5
	05	250	4.4	6.2–15.0
*	12	500	5.7	8.0–21.2
	13	750	7.1	10.0–25.9
*	28	1000	12.6	17.7–30.0
	50	4000	17.5	24.5–60.0

For 75Ω Systems please consult office
For 93Ω Systems please consult office
For Reed Assembly Style 33, please consult office for coil voltage
For High Insulation Systems please consult office.

* **Where insertion loss, VSWR, return loss and operation above 400 MHz are important to your application, please contact the Sales Engineering Department for assistance.**

HOW TO CONSTRUCT A PART NUMBER

A4603–01–28D–80–04–(AAA)

- Series A
- REED ASSEMBLY STYLE
- Number of input ports
- Signal Connector Style
- Coil Code
- Variant Code (see below)
- Design Status (mk4)
- Control Connector Style
- D = TRANSIENT PROTECTION DIODE FITTED
  N = COIL ONLY

Figure 7.3.1.g Relays Specifications

The above example shows a 3 input 'A' series relay having high isolation 'Reed Assemblies' fitted, which terminates all unselected inputs into individual 50Ω resistors.

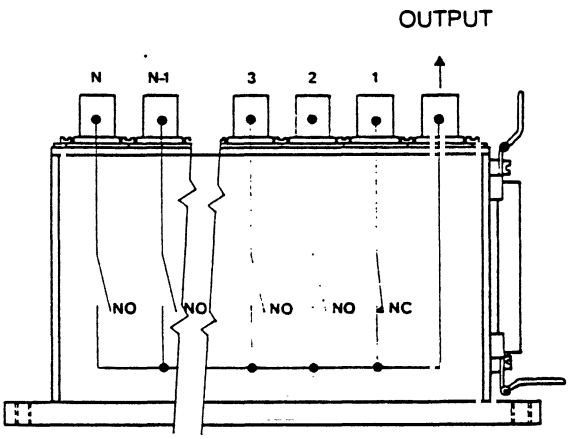
The signal connectors are 50Ω BNC, and the 28V coils have transient Protection Diodes fitted and are energised via a D type control connector.

The Variant (AAA) is for a standard item & may be omitted from the part number. For examples of other Variants please see the back page.

* Preferred feature.

ARREF COMPONENTS (COAXIAL SYSTEMS) LTD.
Plumpton House, Plumpton Road, Rye Park, Hoddesdon, Hertfordshire, England EN11 0LB.
Telephone: Hoddesdon (0992) 463603 Telex: 265849

FAIL-SAFE — VARIANT (AAD)

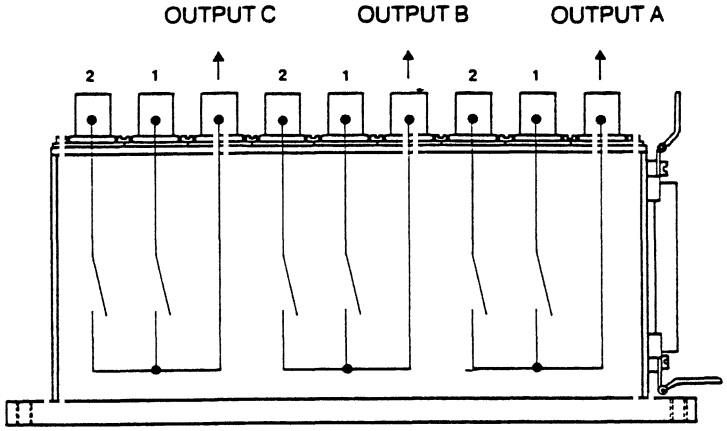


This variant has a normally closed Reed Assembly fitted in Port 1.

The normally closed Reed Assembly performance is as follows:–

Contact Resistance :– 200mΩ Max (initially).
Contact Rating:– 3VA 28VRMS 250mA Max.

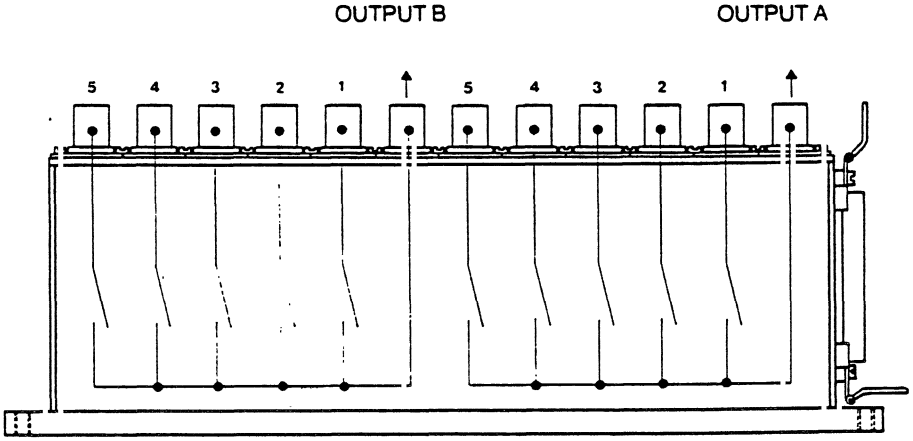
TRIPLE UNIT — VARIANT (ABB)



This variant has three relays of the specified part number in the same body.

In this example Three, 2 input relays are shown.

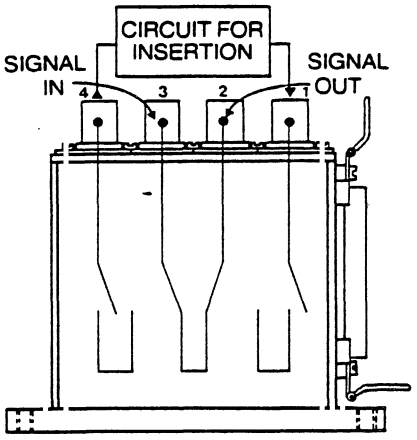
TWIN UNIT — VARIANT (ABA)



This variant has two relays of the specified part number in the same body.

In this example Two, 5 input relays are shown.

CIRCUIT INSERTION — VARIANT (ACJ)



This circuit is specifically designed to allow the insertion (or bypassing) of a circuit into a coaxial line.

The schematic diagram shows the principle of operation.

LOCAL AGENT

Figure 7.3.1.h Relays Specifications

RF COMPONENTS
ARREE COMPONENTS (COAXIAL SYSTEMS) LTD
Plumpton House, Plumpton Road, Rye Park, Hoddesdon
Hertfordshire, England EN11 0LB
Telephone: Hoddesdon (0992) 463603 Telex: 265849

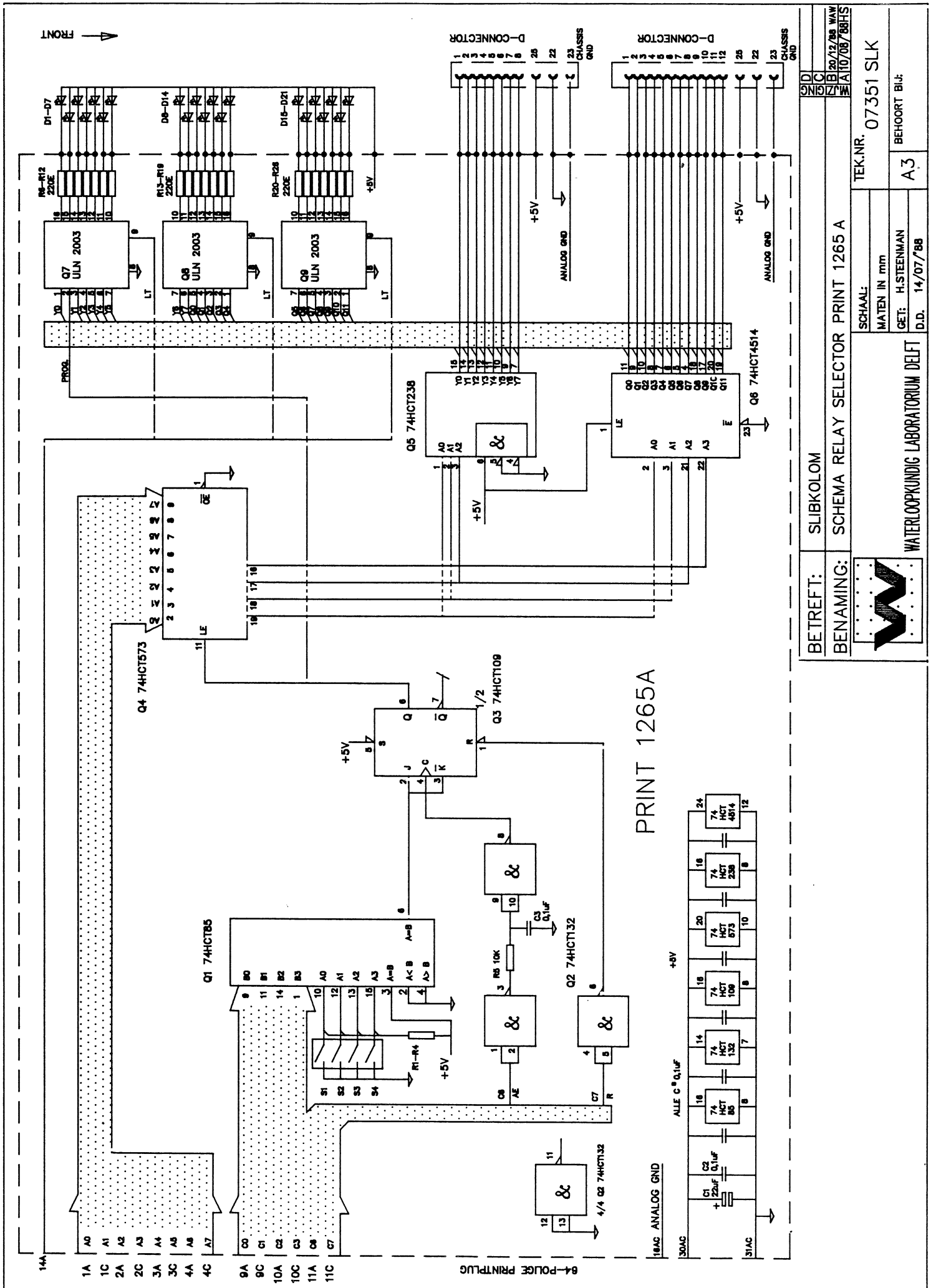


Figure 7.5.1.a Circuit diagram Relay Selector board

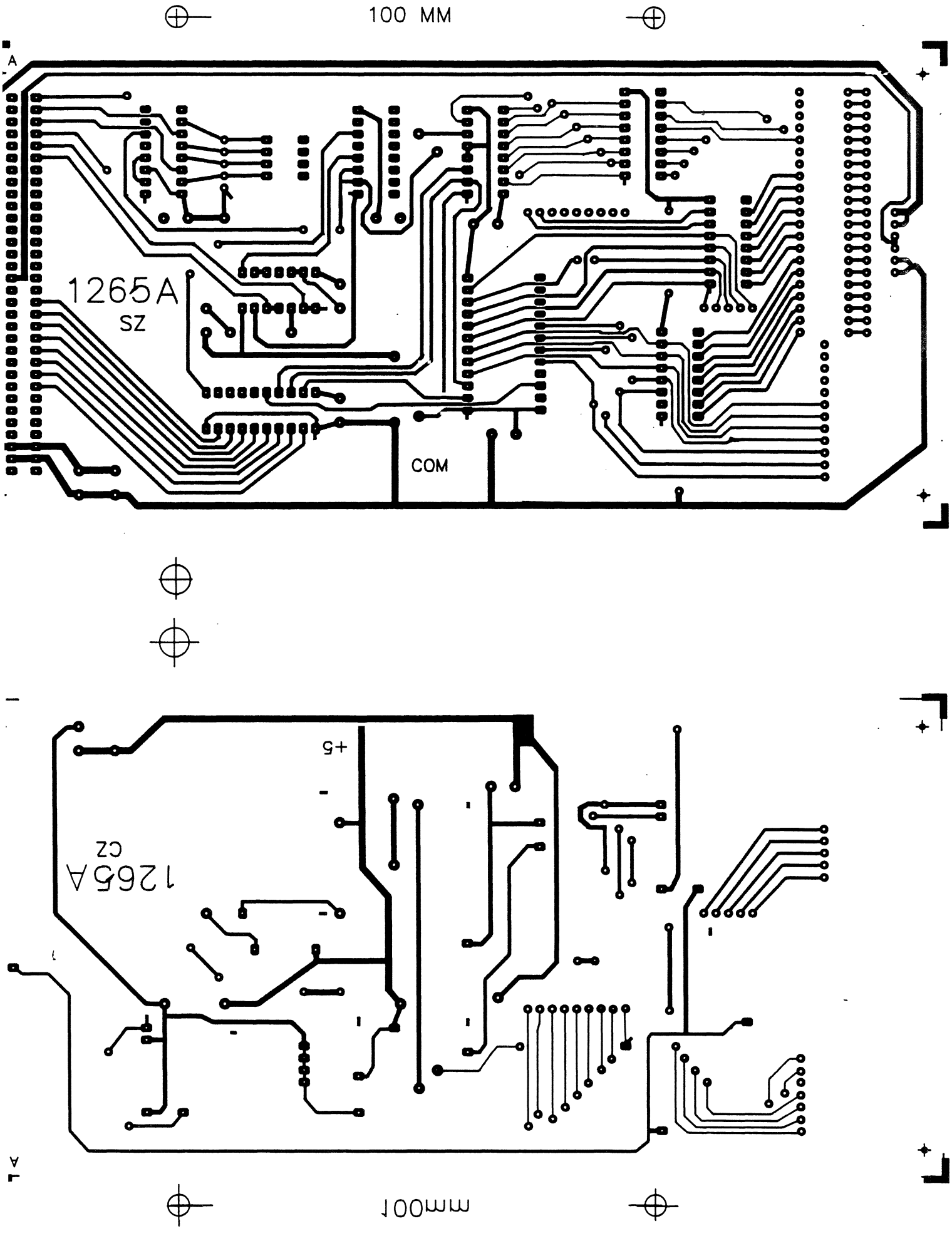


Figure 7.5.1.b PCB Layout Relay Selector board

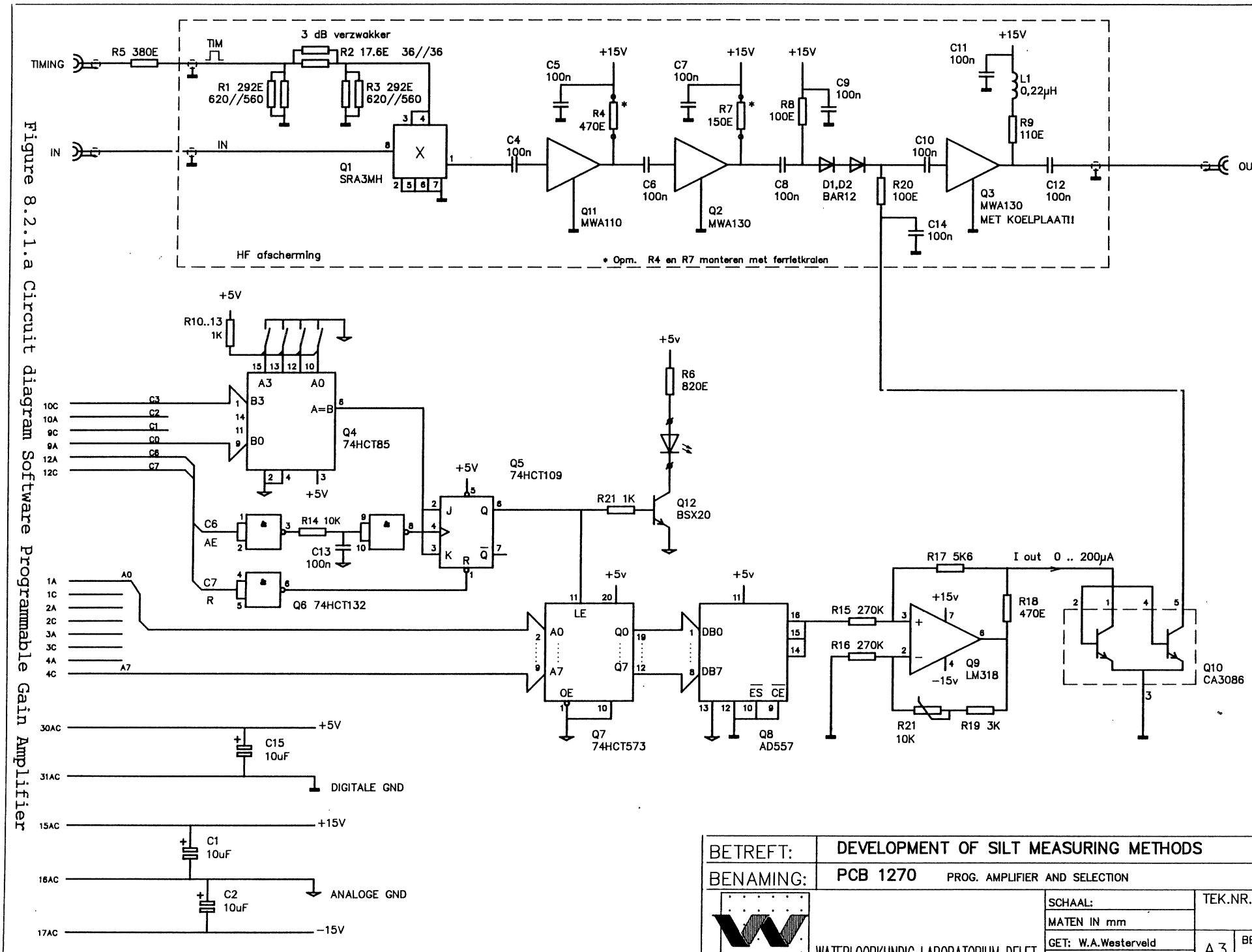


Figure 8.2.1.a Circuit diagram Software Programmable Gain Amplifier

BETREFT:	DEVELOPMENT OF SILT MEASURING METHODS	WIJZIGING	D
BENAMING:	PCB 1270 PROG. AMPLIFIER AND SELECTION		C
			B
			A
WATERLOOPKUNDIG LABORATORIUM DELFT	SCHAAL:	TEK.NR.	07357SLK
	MATEN IN mm		
	GET: W.A.Westerveld	A3	BEHOORT BIJ:
	D.D. 03-02-89		

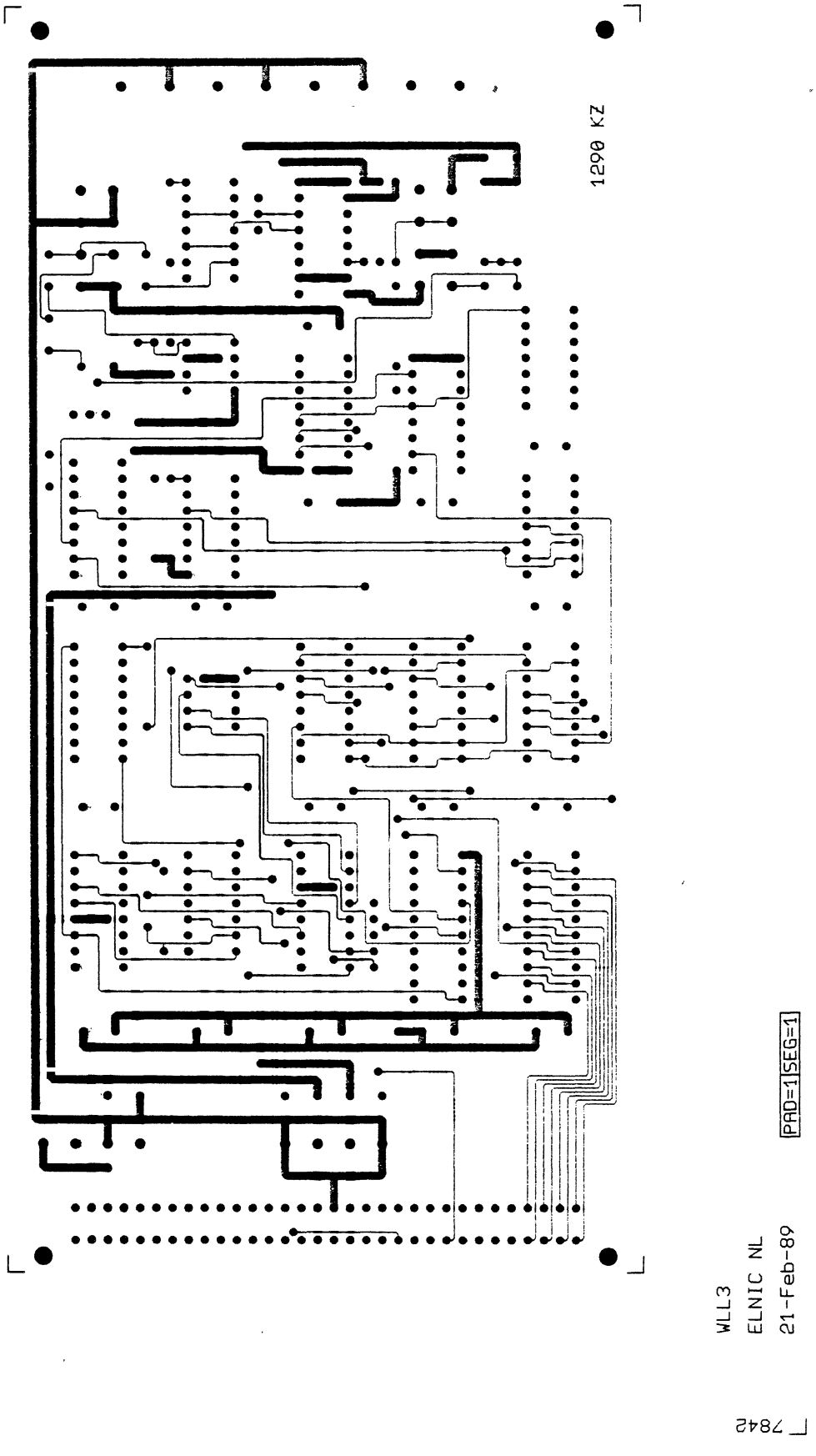


Figure 8.2.1.b PCB Layout Software Programmable Gain Amplifier

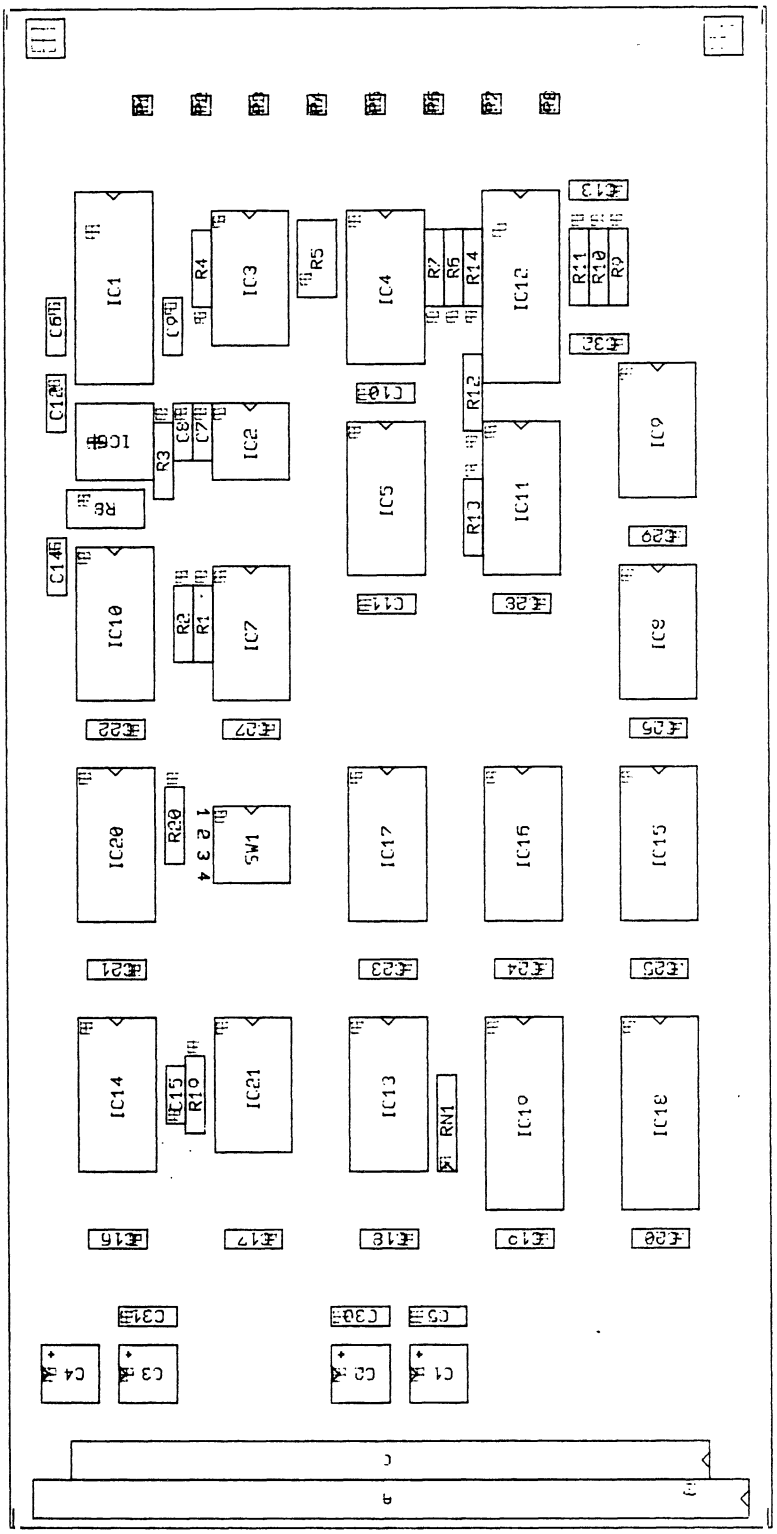


Figure 8.2.1.c Component Mounting Software Programmable Gain Amplifier

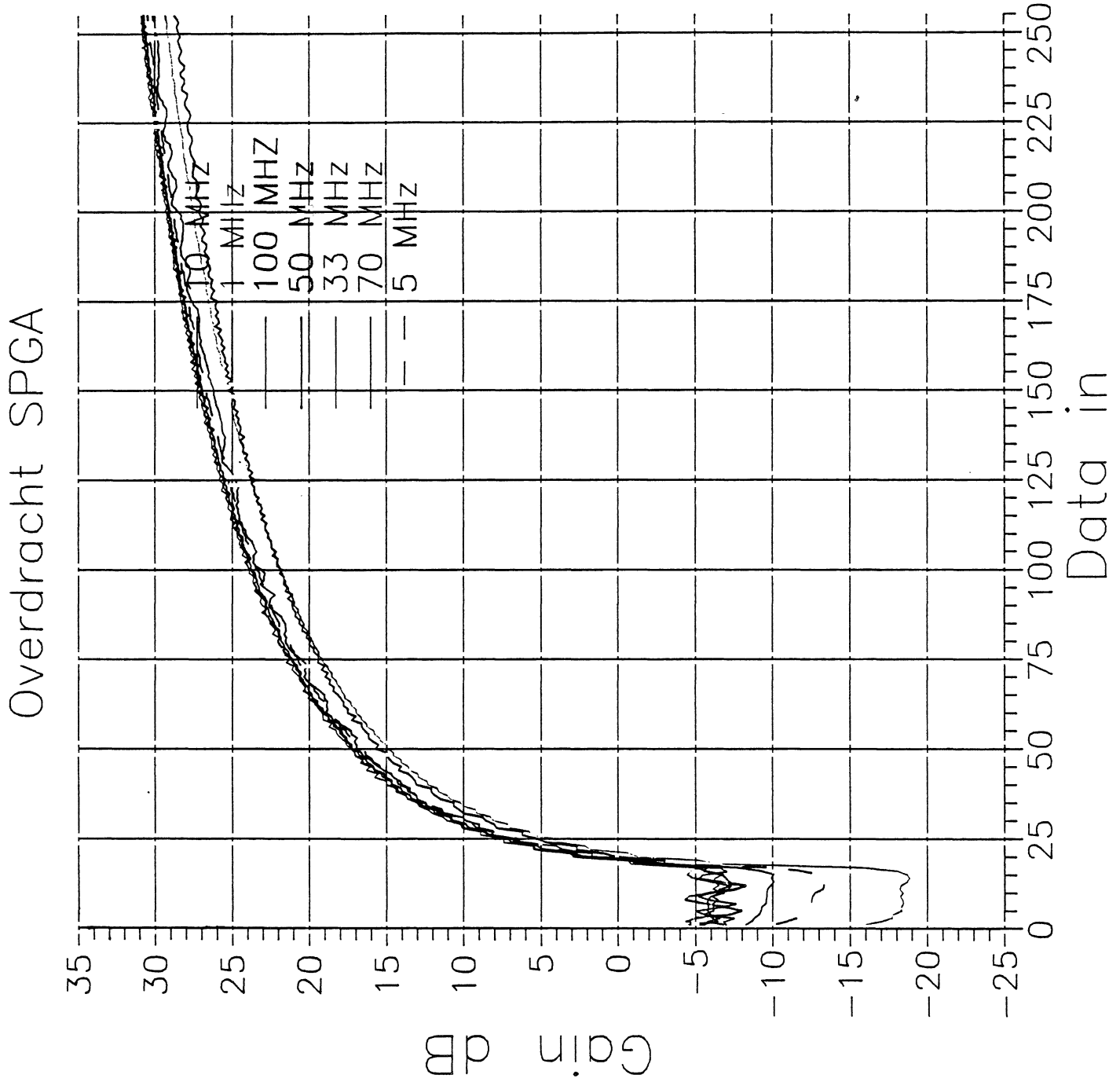


Figure 8.4.2 Nonlineair tuning characteristics SPGA

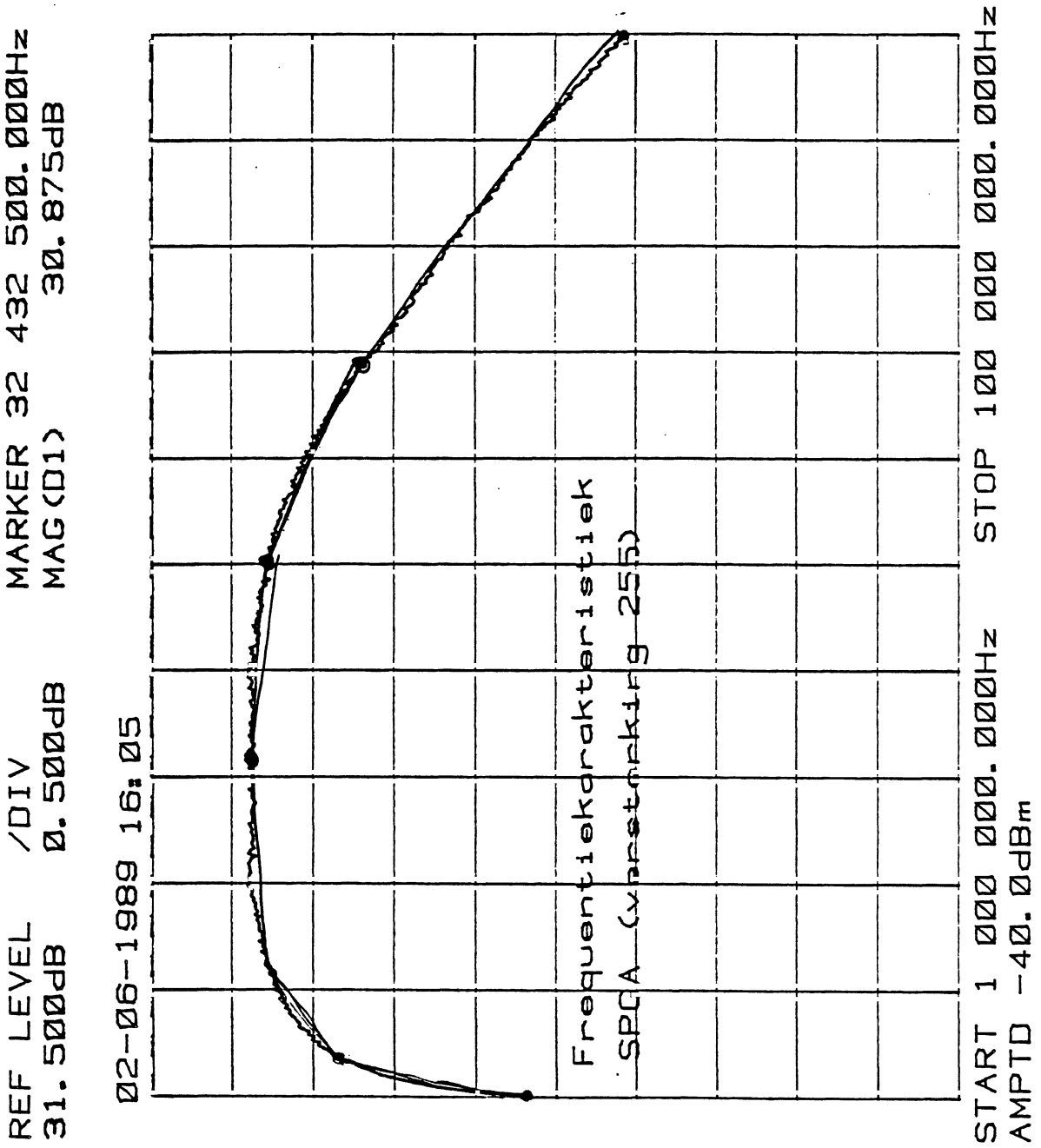


Figure 8.4.1 Frequency dependency Software Programmable Gain Amplifier

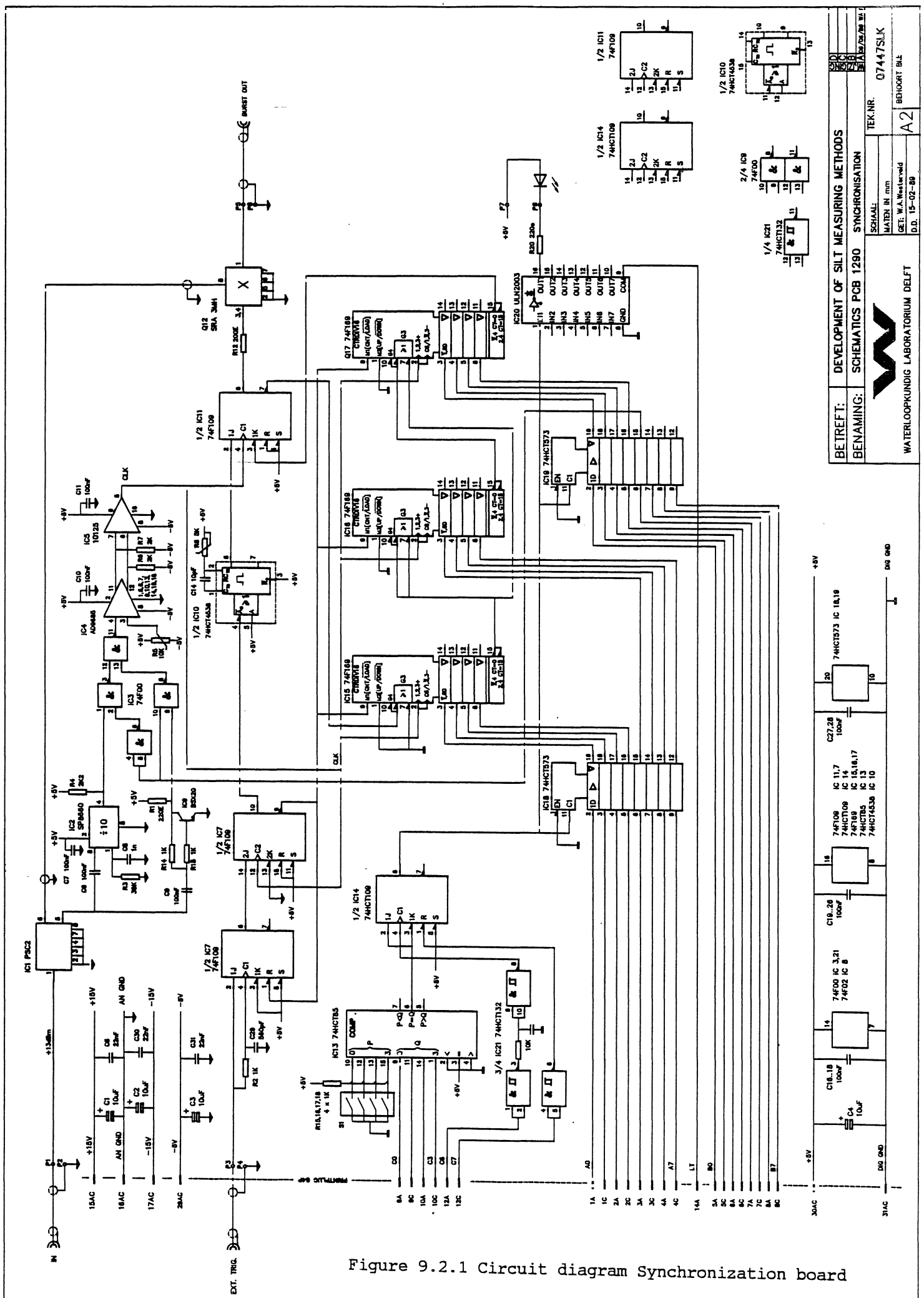


Figure 9.2.1 Circuit diagram Synchronization board

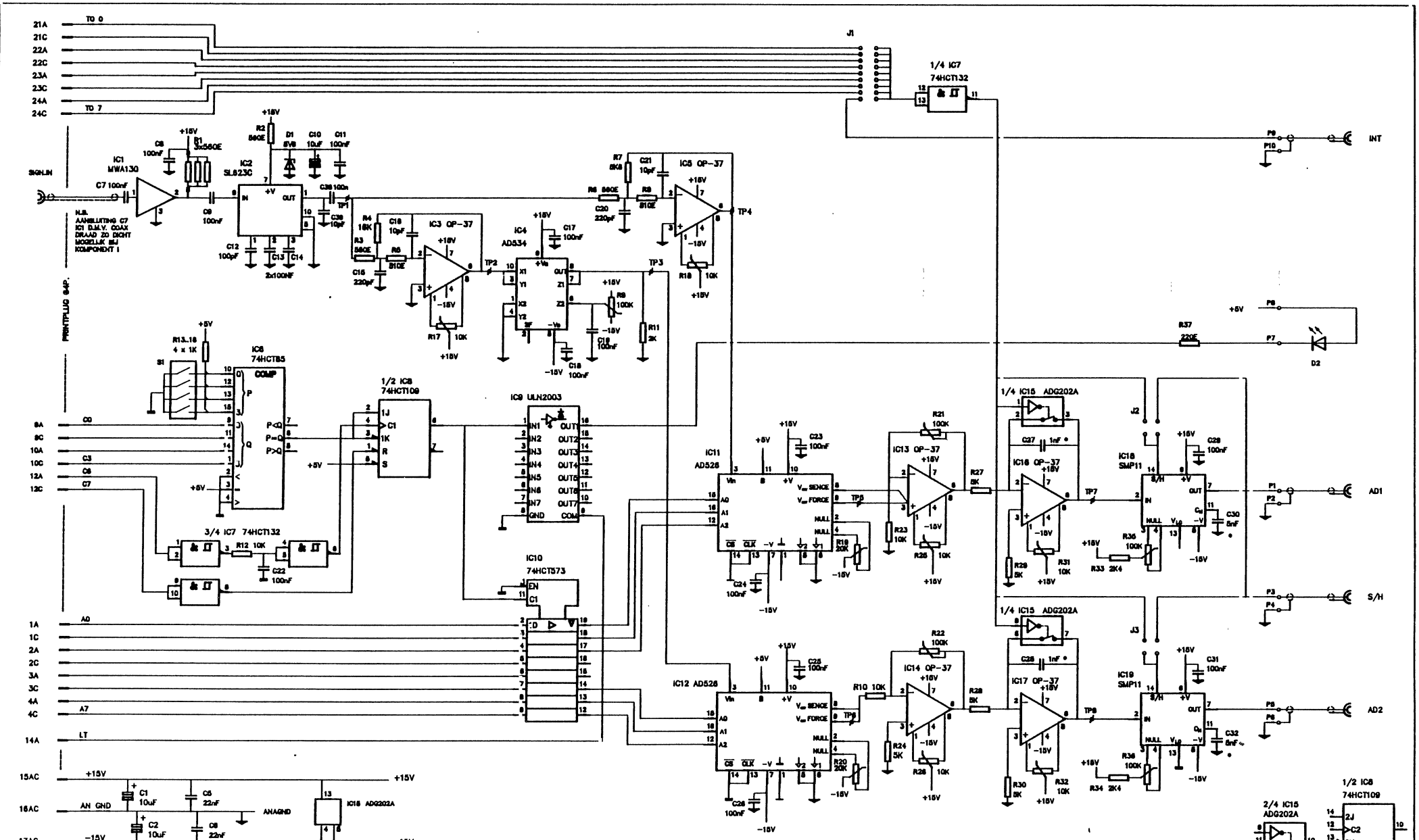


Figure 10.2.1.a Circuit diagram Detection board

• = POLYSTYREEN CAPACITOR

BETREFT:	DEVELOPMENT OF SILT MEASURING METHODS		
BENAMING:	SCHEMATICS PCB 1291 DETECTION CIRCUIT		
WATERLOOPKUNDIG LABORATORIUM DELFT	SCHAAL:	TEK.NR.	07448SLK
	MATEN IN mm		
	GET: W.A.Westerveld	A2	BEHOORT BIJ:
	D.D. 20-04-89		

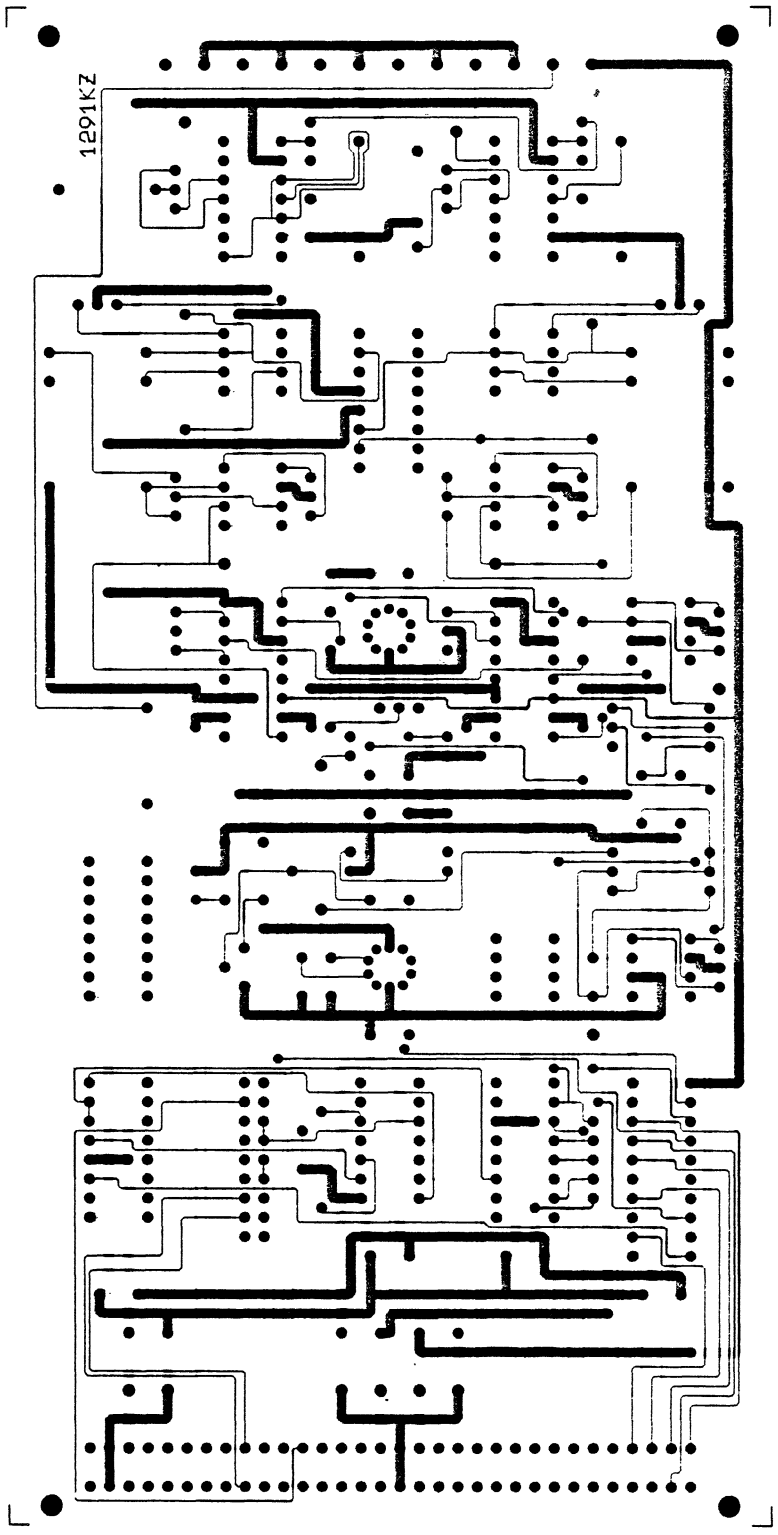


Figure 10.2.1.b PCB Layout Detection board

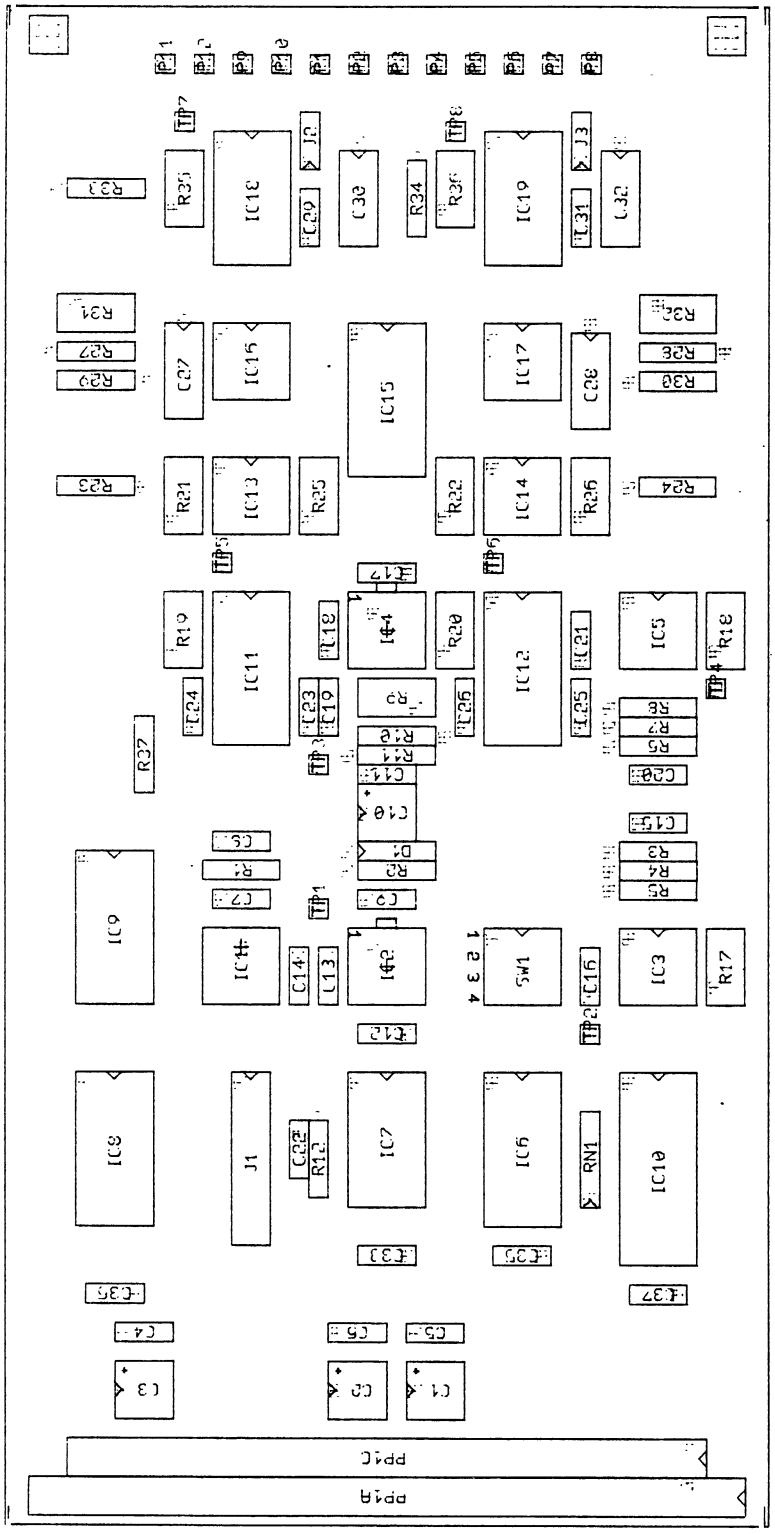


Figure 10.2.1.c Component Mounting Detection board

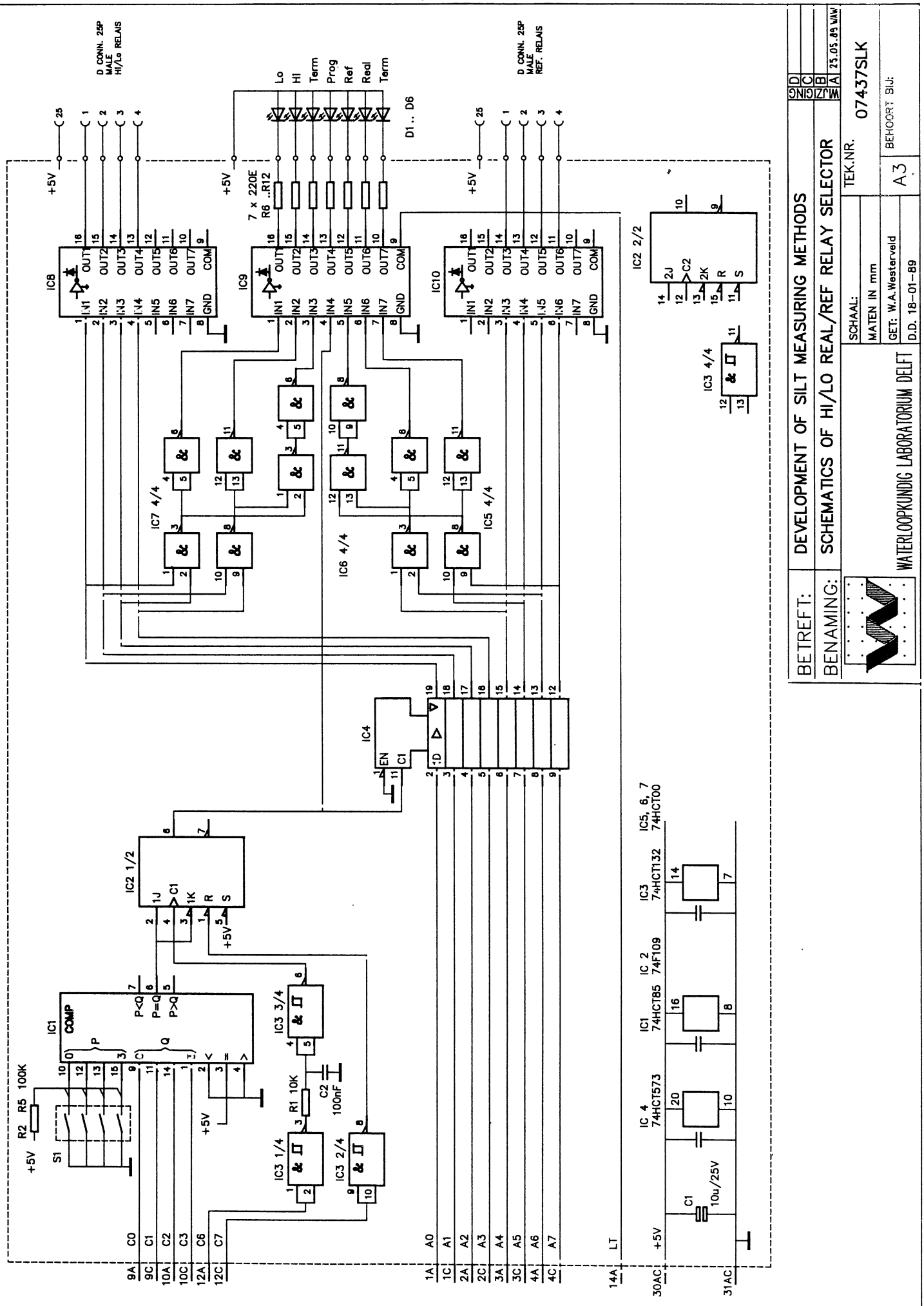


Figure 11.2.1.a Circuit diagram Relay Selector

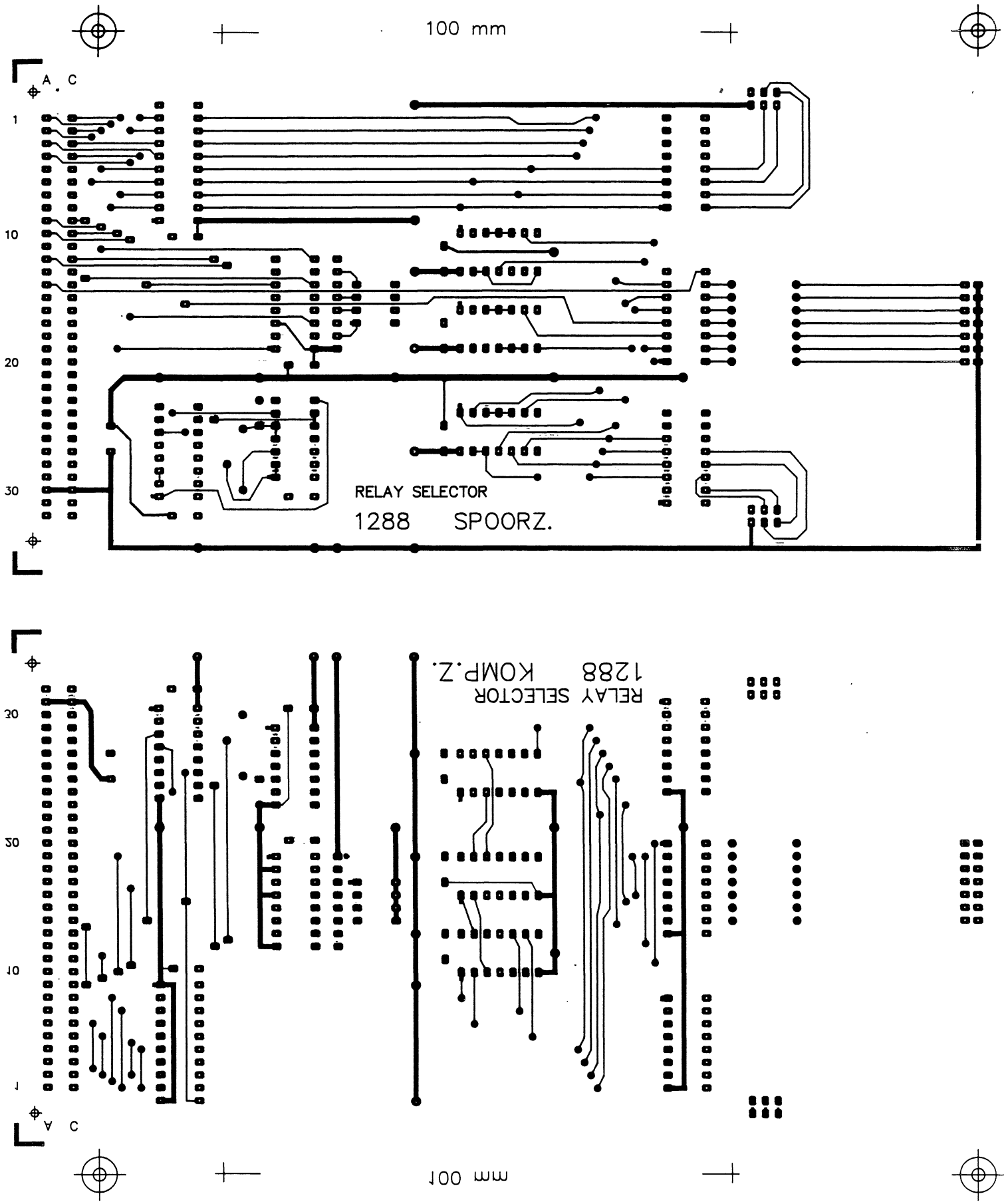


Figure 11.2.1.b PCB Layout Relay Selector

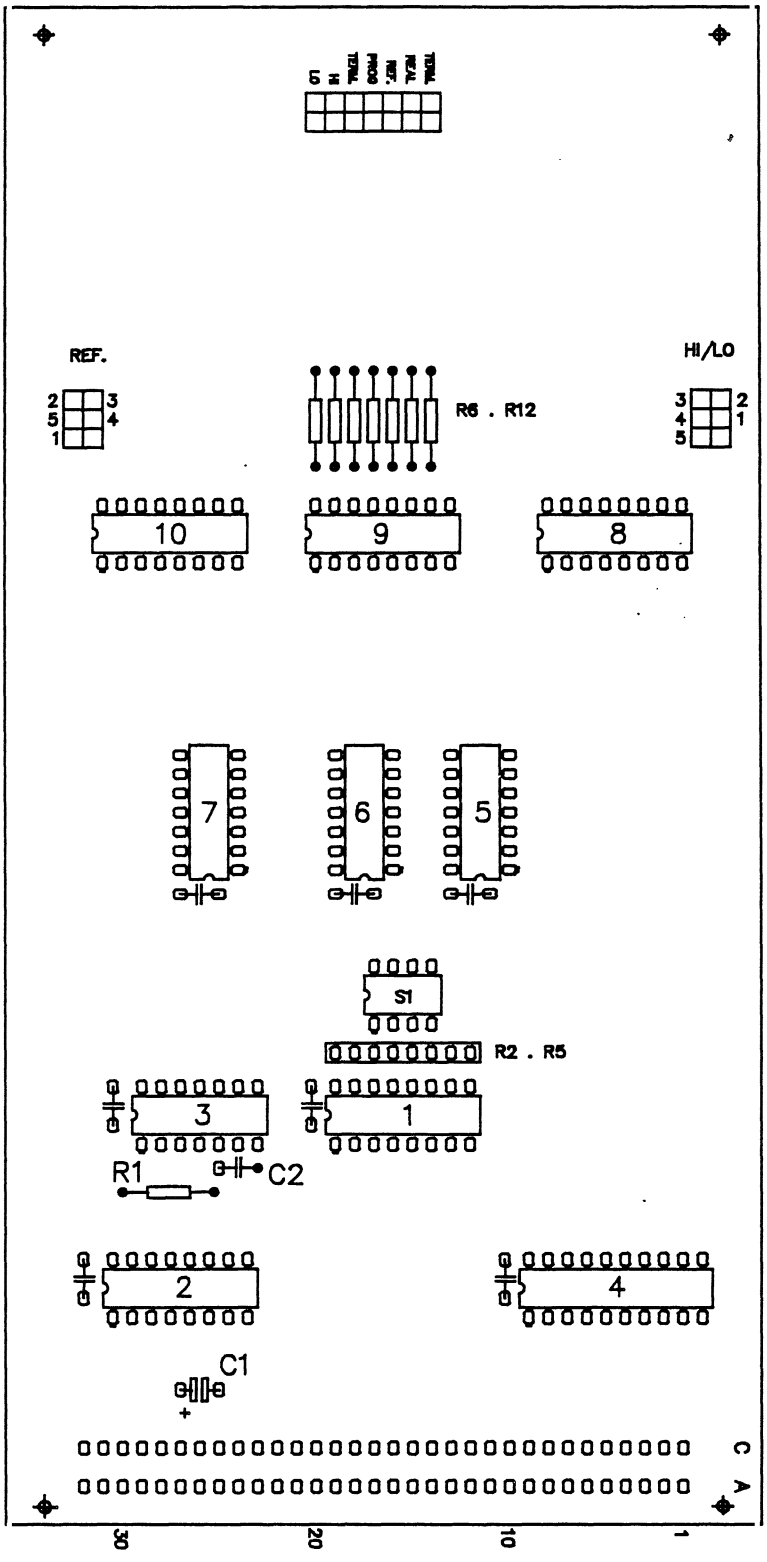


Figure 11.2.1.c Component Mounting Relay Selector

BETREFT:	DEVELOPMENT OF SILT MEASURING METHODS	WIJZIGING	D
			C
BENAMING:	COMPONENT MOUNTING OF PCB 1288		B
			A

WATERLOOPKUNDIG LABORATORIUM DELFT	SCHAAL:	TEK.NR.	07438SLK
	MATEN IN mm		
	GET: W.A.Westerveld	A4	BEHOORT BIJ:
	D.D. 18-01-89		

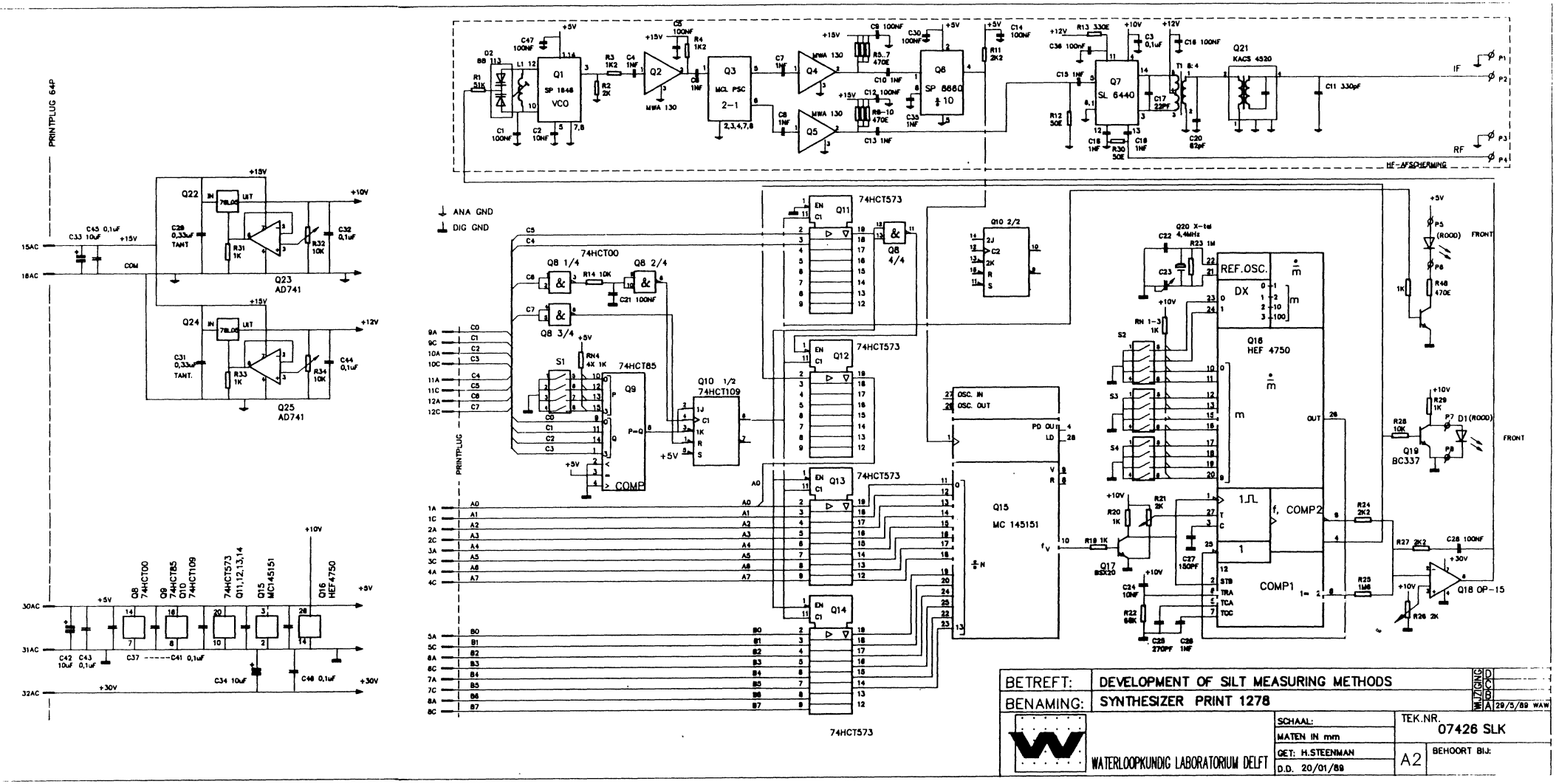


Figure 11.3.1.a Circuit diagram Synthesizer board

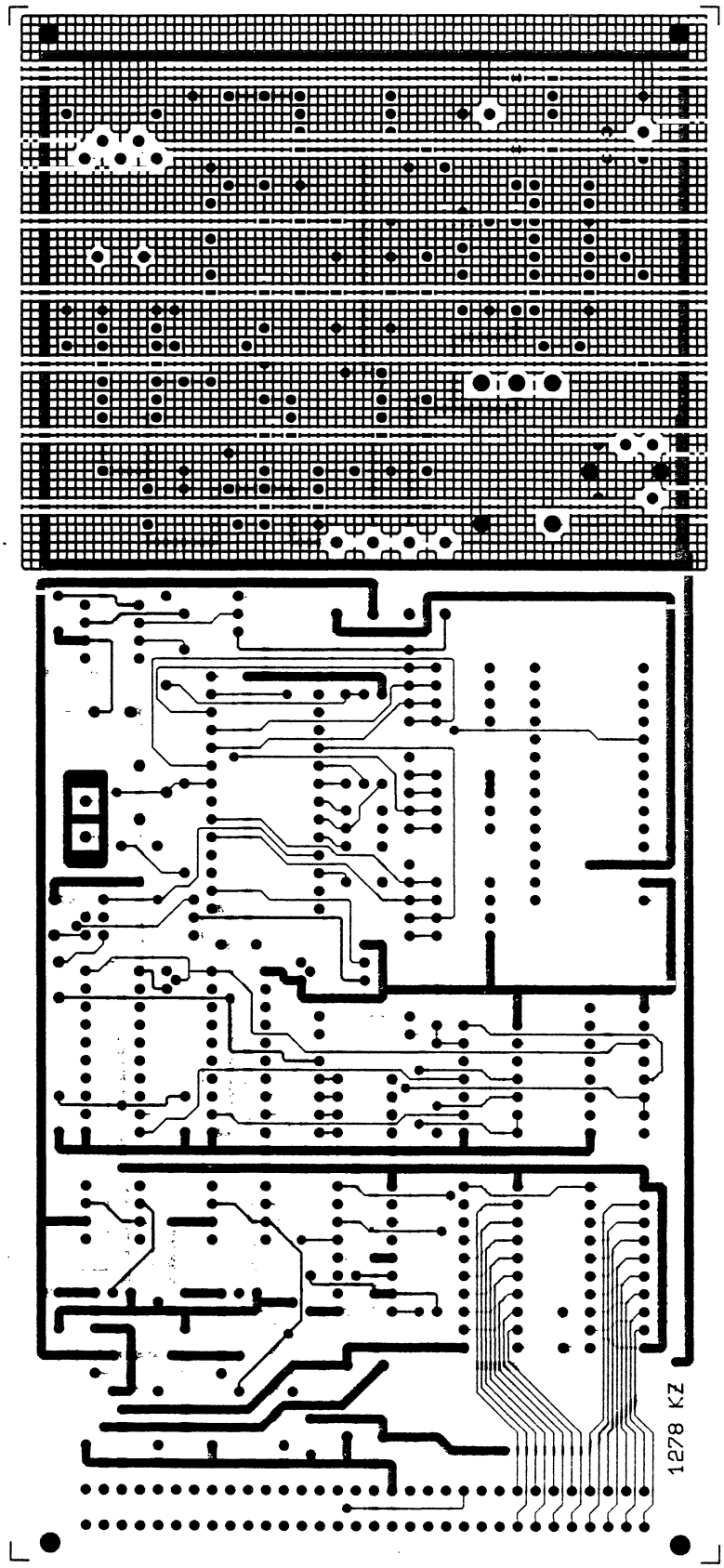
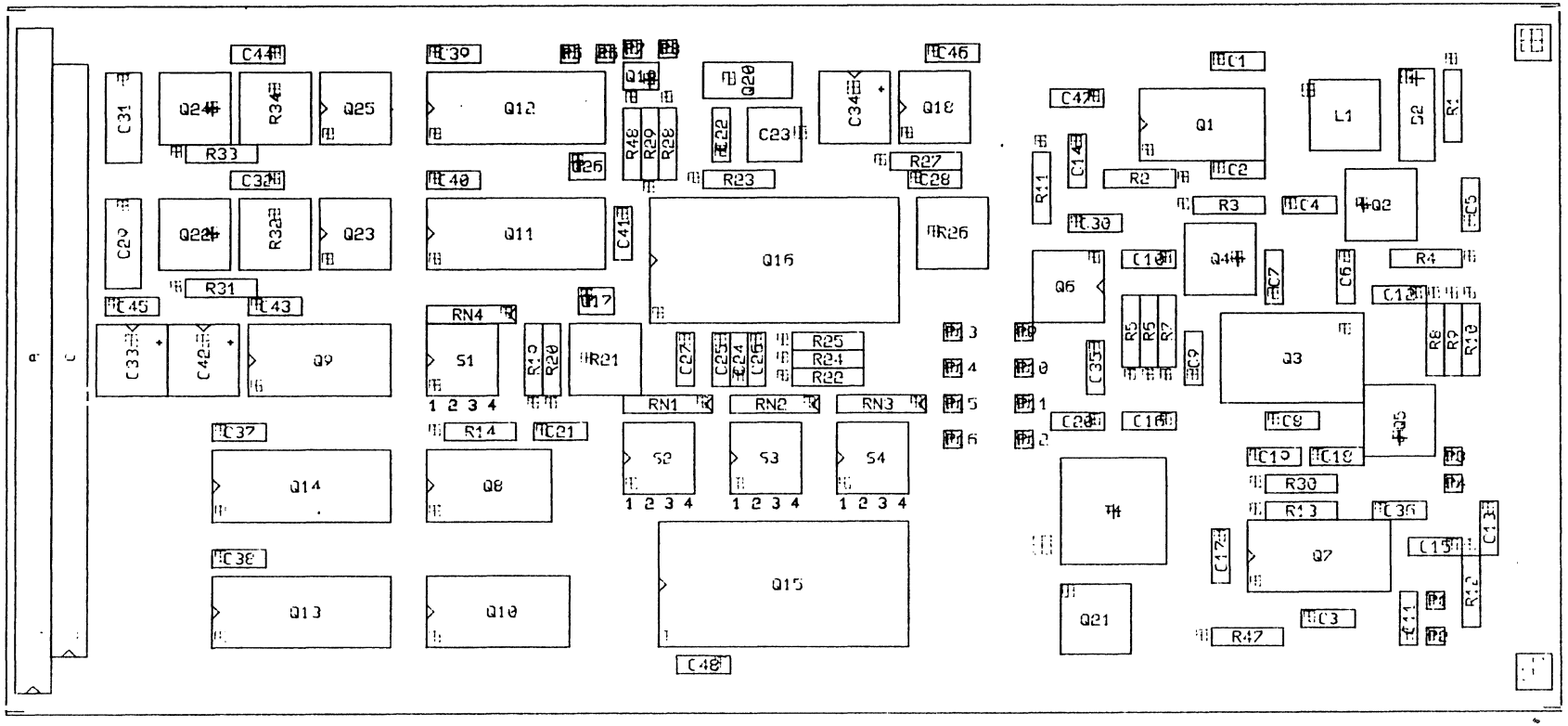


Figure 11.3.1.b PCB Layout Synthesizer board



WLL1

ELNIC NL

25-Jan-89 BPL=1 SEG=E

Figure 11.3.1.c Component Mounting Synthesizer board

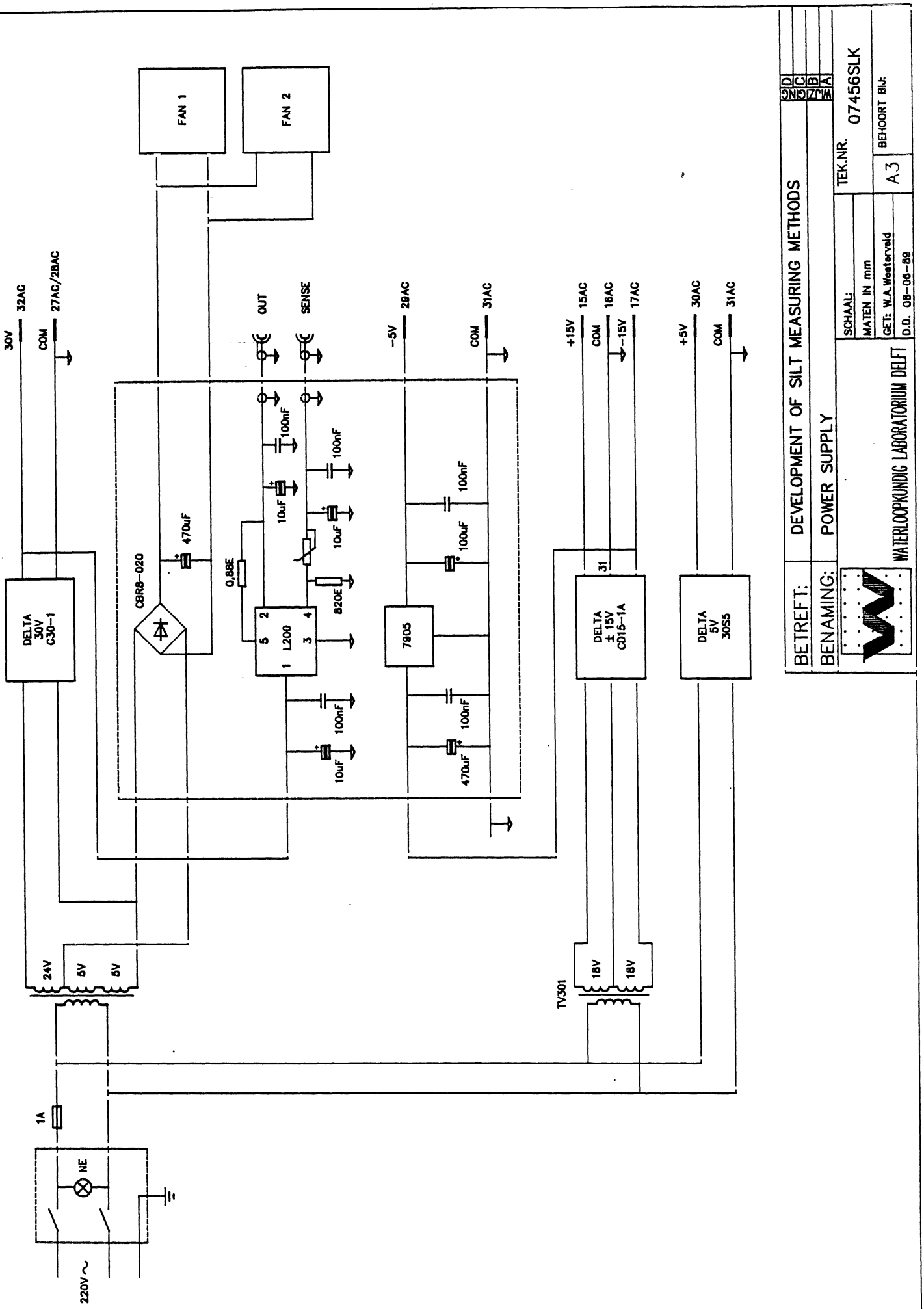


Figure 12.1 Circuit diagram Power Supply

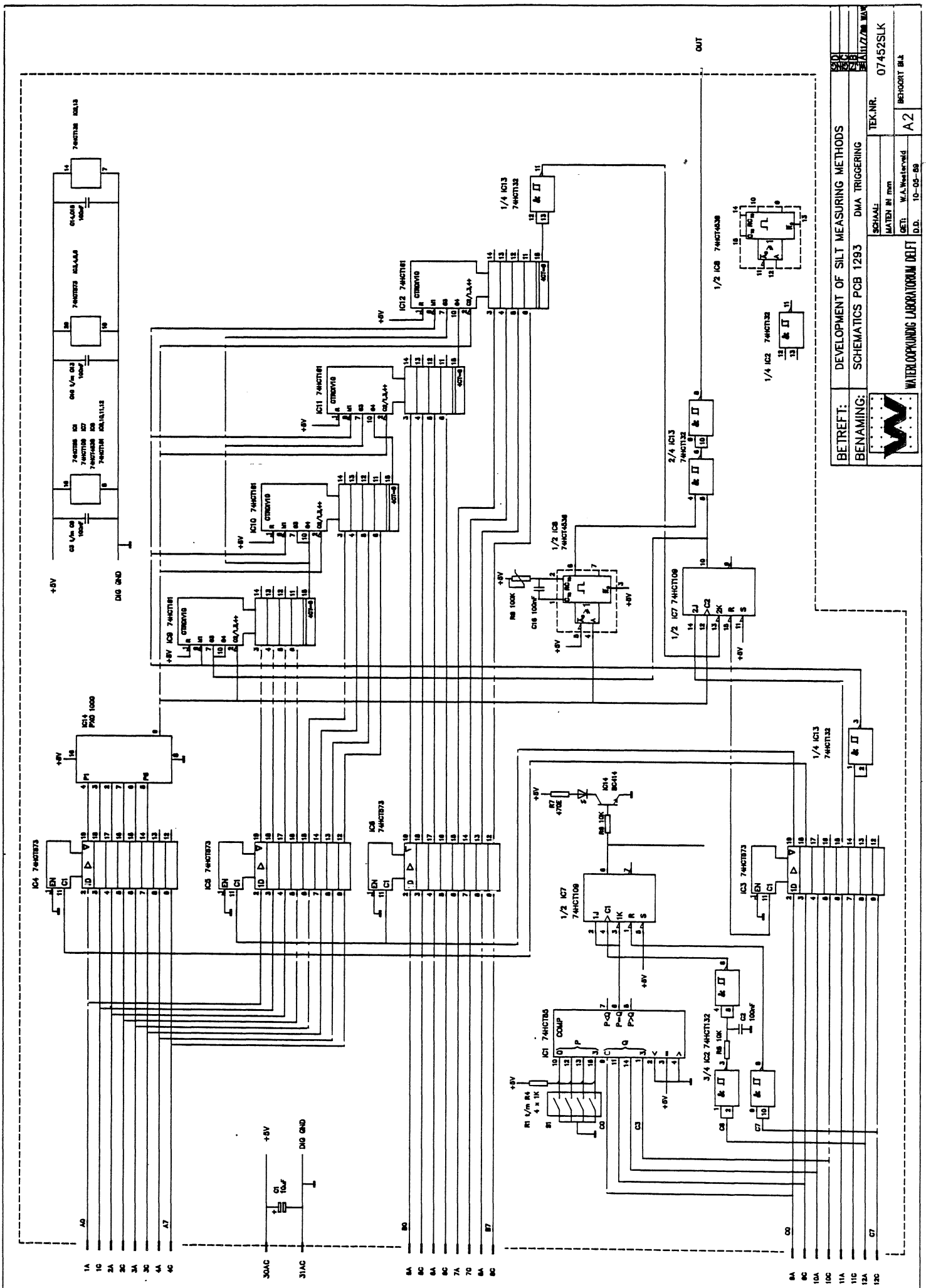


Figure 13.2.1.a Circuit diagram DMA trigger board

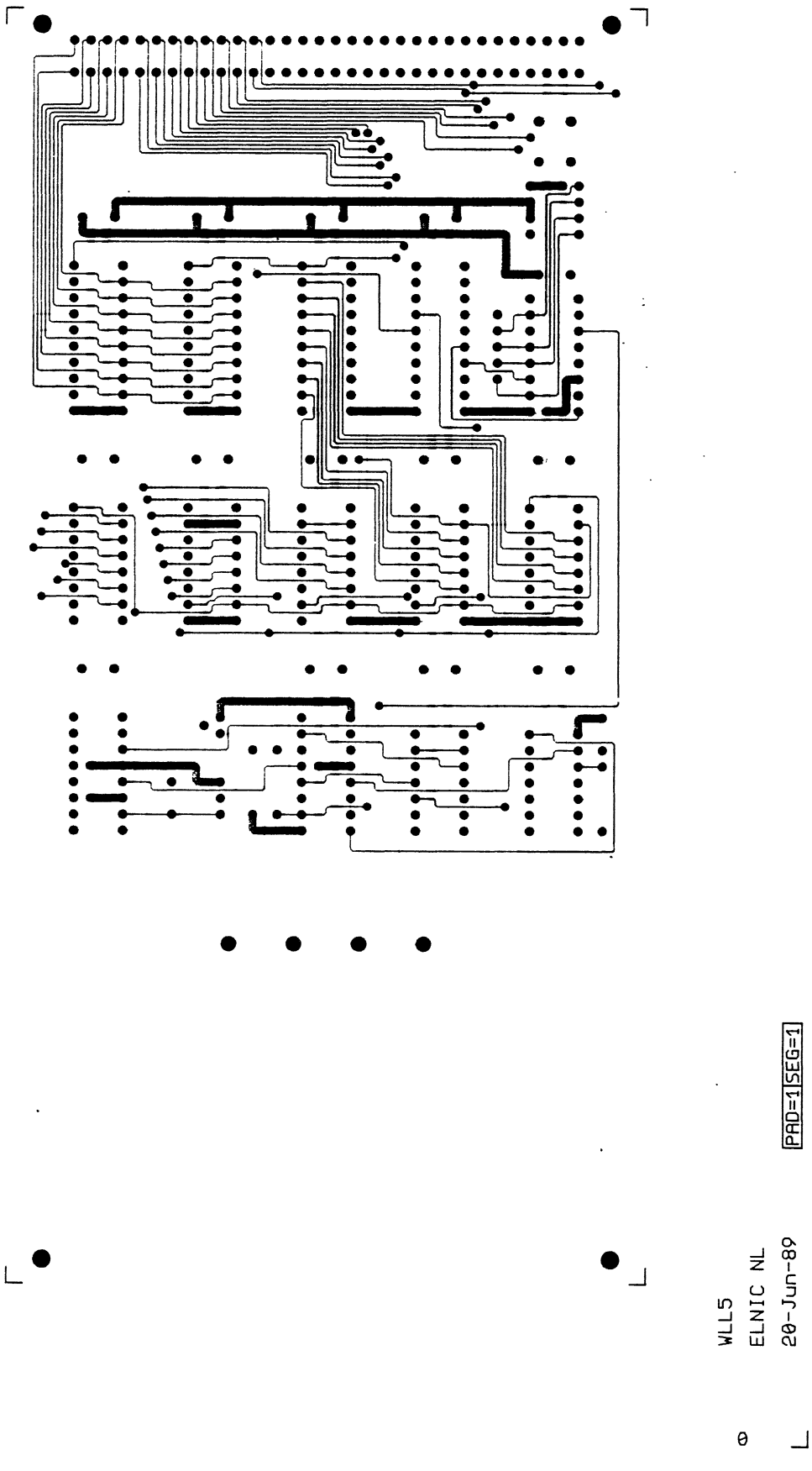


Figure 13.2.1.b PCB Layout DMA trigger board

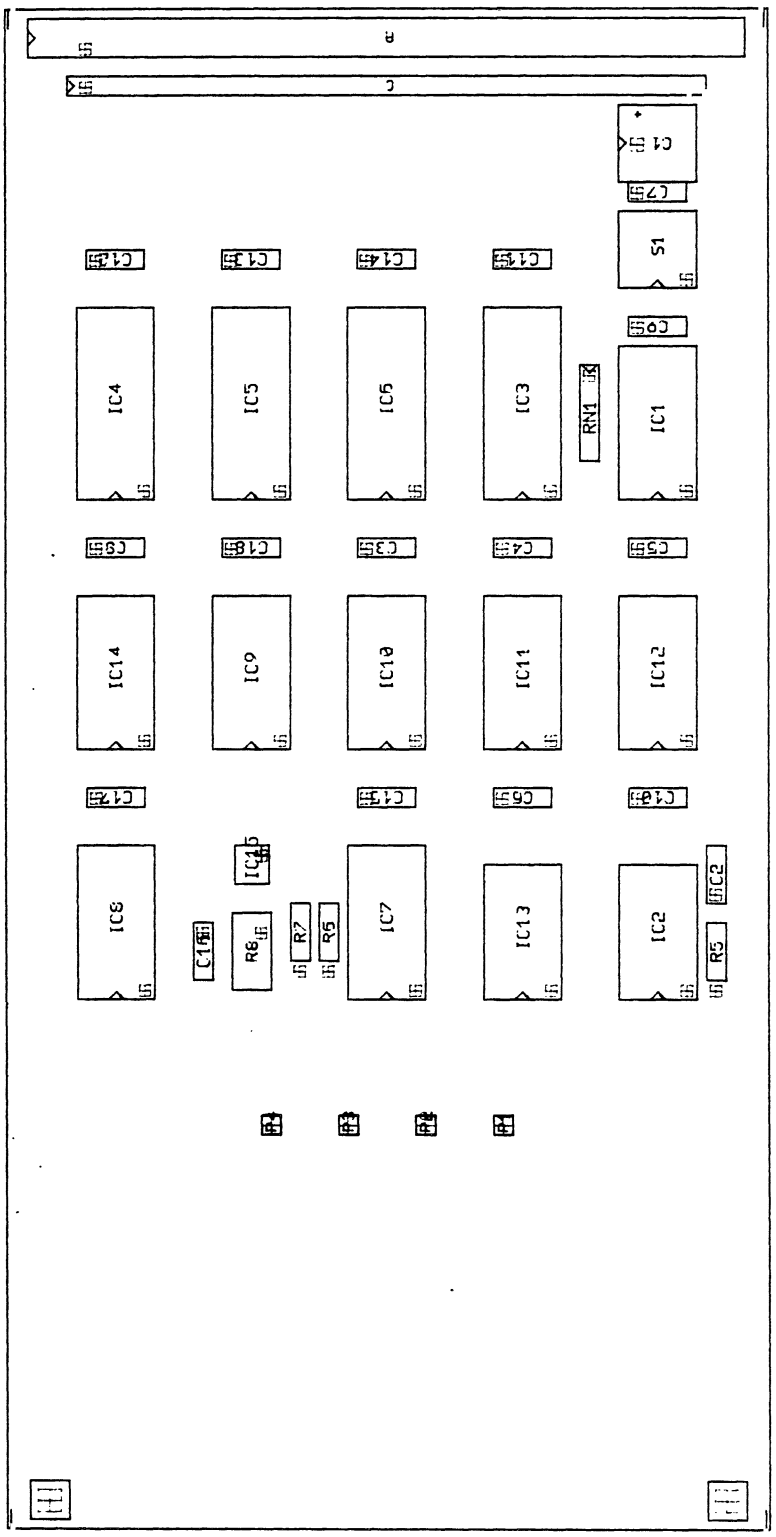


Figure 13.2.1.c Component Mounting DMA trigger board

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