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Distributed Maximum Power Point Tracking Architecture for Photovoltaic Systems

Photovoltaic to Virtual Bus Differential Power Processing

by Afshin Nazer

Distributed Maximum Power Point Tracking Architecture for Photovoltaic Systems

Photovoltaic to Virtual Bus Differential Power Processing

Dissertation

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The only way to solve the problem of nature is to solve it. Otherwise, nature will solve it.

Shahrokh Farhangi

CONTENTS

SUMMARY

This thesis introduces and develops advanced Differential Power Processing (DPP) architectures to enhance the performance and efficiency of photovoltaic (PV) systems by addressing mismatches among PV modules and strings. The work focuses on mitigating power losses due to voltage and current mismatches due to factors such as partial shading, panel misalignment, dust, and degradation. The research proposes novel architectures designed to reduce component voltage and power ratings, potentially lowering costs while maintaining high efficiency.

PV to Virtual Bus Parallel Differential Power Processing (PV2VB PDPP) Architecture: A new PV2VB PDPP architecture is introduced, leveraging a virtual bus as the input for string-level converters (SLCs). This design allows for reduced components' voltage ratings by operating the virtual bus at a lower voltage than the main bus or PV strings. The architecture employs Dual Active Bridge converters connected to Bridgeless converters as SLCs to provide isolation and handle both positive and negative outputs. Experimental results demonstrate system efficiency ranging from 96.4% to 99%.

Dynamic Analysis and Stability: The thesis includes a comprehensive dynamic analysis of the PV2VB PDPP architecture, deriving small-signal models, transfer functions, and frequency responses. These analyses aid in understanding the system's dynamic behavior, enabling effective controller design and stability studies. Experimental validation confirms fast stabilization of the virtual bus voltage (0.6 seconds) and intermediate bus voltages (15 milliseconds), ensuring efficient Maximum Power Point Tracking (MPPT) for each PV string.

Battery Integration in PV2VB PDPP Architecture: The work extends the PDPP architecture to include battery integration at the virtual bus, facilitating energy storage and management while performing MPPT. The battery integration reduces component voltage ratings and allows for efficient charging and discharging control by the central converter. Experimental evaluations show system efficiencies between 95.5% and 99%.

PV to Virtual Bus Series-Parallel Differential Power Process-

ing (PV2VB SPDPP) Architecture: To address mismatches in both series-connected modules and parallel-connected strings, a PV2VB SPDPP architecture is proposed. This architecture uses a combination of SLCs and module-integrated converters (MICs), processing only a fraction of the total power. By leveraging virtual buses for both SLCs and MICs, the architecture reduces voltage and power stress on components, improving cost-effectiveness and reliability. Real-time simulations validate the system's ability to balance power flow, ensure stable operation, and optimize PV module performance under mismatch conditions.

SAMENVATTING

Dit proefschrift introduceert en ontwikkelt geavanceerde Differentiële Stroom Verwerking (DPP)-architecturen om de prestaties en efficiëntie van fotovoltaïsche (PV) systemen te verbeteren door verschillen tussen PV-modules en strings aan te pakken. Het werk richt zich op het verminderen van vermogensverliezen door spannings- en stroomverschillen veroorzaakt door gedeeltelijke schaduw, paneelafwijkingen, stof en degradatie. Er worden nieuwe architecturen voorgesteld die de spannings- en vermogensvereisten van componenten verlagen, waardoor potentieel de kosten verlaagd kunnen worden, terwijl hoge efficiënties behouden kunnen blijven.

PV naar Virtuele Bus PDPP-architectuur: Een nieuwe Parallel Differentiële Stroom Verwerking (PDPP)-architectuur wordt geïntroduceerd, waarbij een virtuele bus wordt gebruikt als invoer voor string-niveau omvormers (SLC's). Dit ontwerp maakt lagere spanningsvereisten voor componenten mogelijk door de virtuele bus op een lagere spanning te laten werken dan de hoofd-bus of PV-strings. De architectuur maakt gebruik van dubbele actieve brug-omvormers die zijn verbonden met brugloze omvormer als SLC's om isolatie te bieden en zowel positieve als negatieve uitgangen te verwerken. Experimentele resultaten tonen een systeem efficiëntie van 96,4% tot 99%.

Dynamische Analyse en Stabiliteit: Het proefschrift omvat een uitgebreide dynamische analyse van de PV2VB PDPP-architectuur, waarbij kleine-signaalmodellen, overdrachtsfuncties en frequentieresponsen worden afgeleid. Deze analyses bieden inzicht in het dynamische gedrag van het systeem, waardoor effectieve controllerontwerpen en stabiliteitsstudies mogelijk worden. Experimentele validatie bevestigt een snelle stabilisatie van de virtuele bus-spanning (0,6 seconden) en tussen-bus-spanningen (15 milliseconden), wat zorgt voor een efficiënte Maximaal Vermogenspunt Volger (MPPT) van elke PV-string.

Batterijintegratie in de PV2VB PDPP-architectuur: Het werk breidt de PDPP-architectuur uit met batterij-integratie op de virtuele bus, wat energieopslag en -beheer mogelijk maakt tijdens het uitvoeren van MPPT. De batterij-integratie verlaagt de spanningsvereisten van componenten en stelt de centrale converter in staat om efficiënt te laden en ontladen. Experimentele evaluaties tonen systeem-efficiënties van 95,5% tot 99%.

PV naar Virtuele Bus SPDPP-architectuur: Om verschillen in zowel serie geschakelde modules als parallel geschakelde strings aan te

pakken, wordt een Series-Parallel Differentiële Vermogens Verwerking (SPDPP)-architectuur voorgesteld. Dit systeem maakt gebruik van een combinatie van SLC's en module-geïntegreerde omvormers (MIC's) die slechts een fractie van het totale vermogen verwerken. Door gebruik te maken van virtuele bussen voor zowel SLC's als MIC's, vermindert de architectuur de spannings- en vermogensbelasting op componenten, waardoor de kosteneffectiviteit en betrouwbaarheid verbeteren. Real-time simulaties bevestigen dat het systeem in staat is om het vermogensverloop te balanceren, stabiele werking te garanderen en de prestaties van PV-modules onder verschilcondities te optimaliseren.

NOMENCLATURE

List of Acronyms and their Definitions

Acronyms	Definition
2L-VSI	Two-Level Voltage Source Inverter
3L-ANPC	Three-Level Active Neutral-Point-Clamped
3L-NPC	Three-Level Neutral-Point-Clamped
ALC	Array-Level Converters
BL	Bridgeless
CCM	Continuous Conduction Mode
CIC	Cell Integrated Converters
CPSD	Cross Power Spectral Density
DAB	Dual Active Bridge
DISO	Dual-Input Single-Output
DMPPT	Distributed Maximum Power Point Tracking
DPP	Differential Power Processing
DSCC	Direct Switched-Capacitor Converter
DSFC	Double-Star Full-Bridge Cell
DSHC	Double-Star Half-Bridge Cell
EMI	Electromagnetic Interference
ESD	Energy Storage Device
FPP	Full Power Processing
GUI	Graphical User Interface
HFT	High-Frequency Transformer
I-V	Current-Voltage
KCL	Kirchhoff’s Current Law
LCOE	Levelized Cost of Energy
LPPT	Least Power Point Tracking
LSCC	Ladder-Type Switched-Capacitor Converter
MIC	Module Integrated Converters
MIMO	Multi-Input–Multi-Output
MISO	Multi-Input–Single-Output

Table 1.: List of Symbols and Definitions (continued)

Symbol	Definition
MMCI	Modular Multilevel Cascade Inverters
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
PDPP	Parallel Differential Power Processing
PI	Proportional-Integral
P&O	Perturbation and Observation
PRBS	Pseudo-Random Binary Sequence
PSD	Power Spectral Density
PV	Photovoltaic
PV2B	Photovoltaic-to-Bus
PV2PV	Photovoltaic-to-Photovoltaic
PV2VB	Photovoltaic-to-Virtual Bus
PWM	Pulse-Width Modulation
SDPP	Series Differential Power Processing
SIDO	Single-Input Dual-Output
SISO	Single-Input Single-Output
SLC	String-Level Converter
SMIC	Submodule Integrated Converters
SPDPP	Series-Parallel Differential Power Processing
SPS	Single Phase Shift
SSFC	Single-Star Full-Bridge Cell
STC	Standard Test Conditions
STATCOM	Static Synchronous Compensator
TCT	Total Cross Tied
THD	Total Harmonic Distortion
VE	Voltage Equalization
ZSC	Zero-Sequence Current
ZSV	Zero-Sequence Voltage

1

INTRODUCTION

Today, fossil-fuel-based power generators continue to be extended and modernized. These power generators burn fuel to release thermal energy which is then converted into electricity for nationwide distribution. The substances emitted during this process harm the environment, making it imperative to transition to more sustainable and eco-friendly energy sources. Solar energy is one such renewable source that plays a significant role in the modern energy mix. To convert solar energy into electricity, Photovoltaic (PV) technology is well-established and widely used. PV cells are the smallest devices responsible for converting solar energy into electricity in a PV power generators. However, their output power is so low that multiple cells need to be connected in series forming PV modules to achieve the required voltage.

Unlike traditional power generators, PV power generators can generate electricity closer to the point of consumption, providing a smarter and more convenient alternative. Currently, PV power generators focus on installing PV systems in non-residential and urban environments. In urban environments, there is significant potential for expansion, as nearly every suitable building roof and facade could eventually host PV modules. While PV technology is well-established, they are still needed to address the unique challenges posed by urban environments.

PV systems face a significant challenge of non-uniformity, especially in terms of received irradiance, in urban environments. When PV modules are connected in series, non-uniformity caused by factors such as the PV modules' orientation, tilt, and environmental conditions (e.g., shading, soiling) can result in some PV modules receiving less irradiance than others, leading them to generate less current. The current of the PV modules receiving the lowest irradiance will determine the current for the entire string. Consequently, the PV modules receiving higher irradiance will be limited by the lower current, preventing them from generating their maximum potential power. As a result, the output

power of the PV system will decrease, leading to an increase in the levelized cost of energy (LCOE). To reduce the LCOE and make PV systems more attractive to investors, thereby enabling their expansion in urban environments, it is essential to focus on efficiently extracting the maximum power from each individual PV module.

1.1. THE PROBLEM

PV system has broad applications, spanning from small-scale wearable devices to large utility-scale power stations [1–3]. The generated current and voltage from PV cells may not always meet the load's needs. Moreover, to reduce the LCOE, PV cells must work at their maximum power point (MPP), which varies with operating conditions. Therefore, PV systems must employ DC-DC and DC-AC converters to connect the PV generator to loads or the grid, ensuring efficient power delivery [4].

Fig. 1.1 illustrates the hierarchy of PV groups, starting from individual PV cells and progressing through PV submodules, modules, strings, and arrays [5–7]. PV cells, typically 20, 24, or 32 [8], are electrically interconnected to form PV submodules, which are then combined to create PV modules via lamination processes as we find them on the market. Multiple PV modules are often connected in series to create PV strings, and parallel PV string connections form PV arrays. Yet, to effectively connect these PV groups to the load or the grid and operate at MPPs, power converters are essential. These converters can operate at various levels within the PV system, including the cell, submodule, module, string, and array levels, named cell integrated converters (CIC) [9, 10], submodule integrated converters (SMIC) [11, 12], module integrated converters (MIC) [13, 14], string level converters (SLC) [15, 16], and array level converters (ALC) [17–19], respectively.

The early approaches to connecting PV arrays to the grid involved using ALCs (Fig. 1.2(a)), also known as central inverters, which connect the entire PV array to the grid [17]. However, conventional PV systems with a single ALC track only the MPP of the entire PV array, leading to mismatch losses. These losses arise due to variations in the output of PV modules caused by factors such as partial shading, differing tilt angles, dust accumulation, or PV cell degradation [20]. For instance, partial shading can lead to significant power losses across the array due to the activation of bypass diodes in parallel to the shaded PV cells. This also results in local MPPs, complicating the operation of the maximum power point tracking (MPPT) algorithm. Moreover, parallel connection of PV strings can further exacerbate mismatch-related losses by forcing PV string's voltage to operate away from their MPP [21].

To mitigate mismatch losses and optimize energy yield, various Distributed Maximum Power Point Tracking (DMPPT) architectures have been developed. DMPPT can mitigate mismatches among PV groups

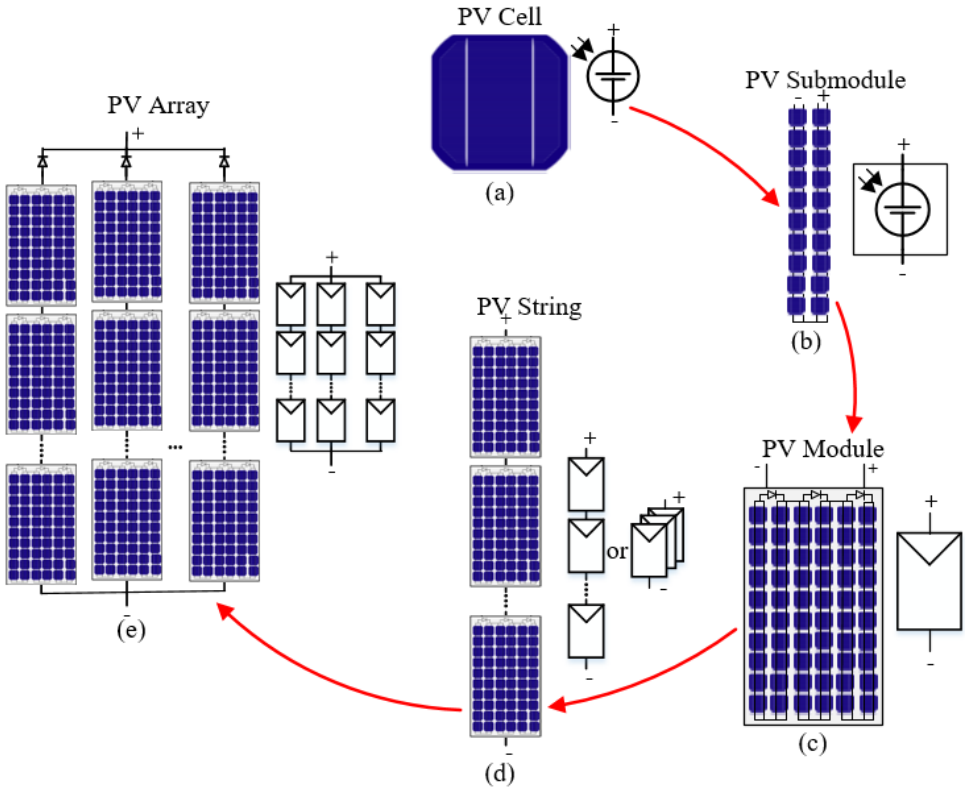

Figure 1.1.: Visual description of the various PV groups: (a) PV cell, (b) PV submodule, (c) PV module, (d) PV string, and (e) PV array.

and perform MPPT at different levels of granularity. These levels range from multi-string inverters, which track the MPP of PV strings individually (Fig. 1.2(b)), to PV optimizers or micro-inverters, which perform MPPT at the module level (detailed in Chapter 2). Although these architectures are mature, proven, and consolidated technologies with a wide variety of power converters already available in the market, they are Full Power Processing (FPP) architectures. FPP architectures increase power conversion losses, size, and cost of the converters while reducing reliability, ultimately leading to a higher LCOE [20, 22] due to two main reasons: (i) they process all the power generated by the PV groups, and (ii) PV groups voltage and current will determine the voltage and current rating for the converters' components. These two reasons will be detailed in Chapter 2.

Another challenge facing PV systems is their fluctuating power output, which is driven by the inherent intermittency of solar energy. Power output variability can complicate the coordination between supply and

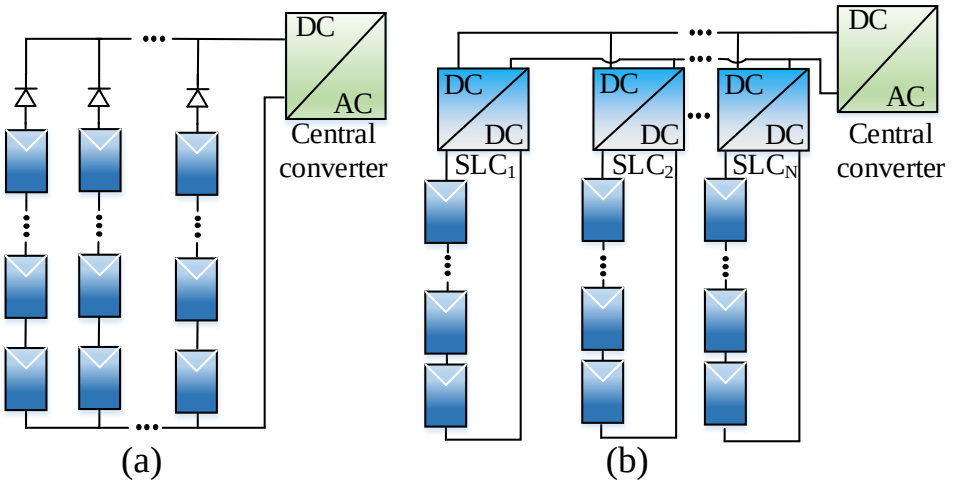

Figure 1.2.: PV system using: (a) Centralized, and (b) Multi-string architectures.

demand, making it difficult to maintain a stable power grid. In a future power system with a high penetration of PV systems, the need for additional energy storage devices (ESDs) becomes critical to effectively manage the challenges associated with intermittent energy supply.

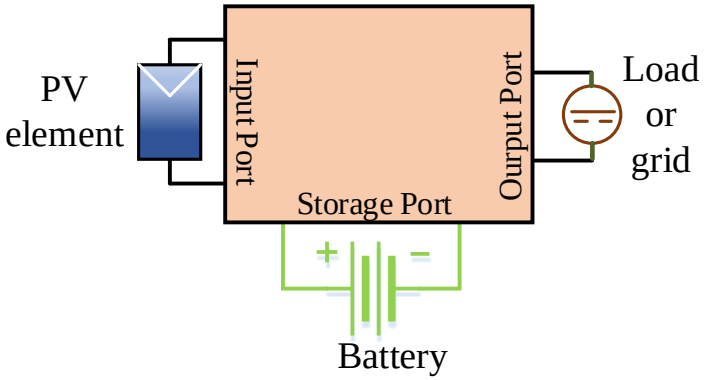

Figure 1.3.: PV system with ESDs

As illustrated in Fig. 1.3, ESDs, such as batteries, are commonly integrated into PV systems. This integration helps to stabilize the output power by storing excess energy during periods of high power generation and discharging it when power generation is low, thus enhancing the overall consistency of the system. As a result, the architecture of PV

systems must evolve to not only address mismatches among individual PV components, such as PV modules and PV strings, but also to enable the seamless integration of ESDs. This ensures that the system can effectively balance energy production with consumption, even in the face of fluctuating environmental conditions.

1.2. ONE WAY TO SOLVE THE PROBLEM

A promising concept contributing to reduce the LCOE of PV systems in the urban environment is the family of Differential Power Processing (DPP) architectures (Fig. 1.4). What distinguishes DPP architectures from other DMPPT approaches is their ability to efficiently handle mismatch conditions. In such architectures, converters are adept at processing only a portion of the generated power, allowing the bulk of the power produced by PV groups to pass through to the output without undergoing local processing. Besides, they are able to support the integration of ESDs. The following analysis illustrates the substantial potential for reducing the LCOE in PV systems using the DPP architectures instead of their FPP counterparts in the future.

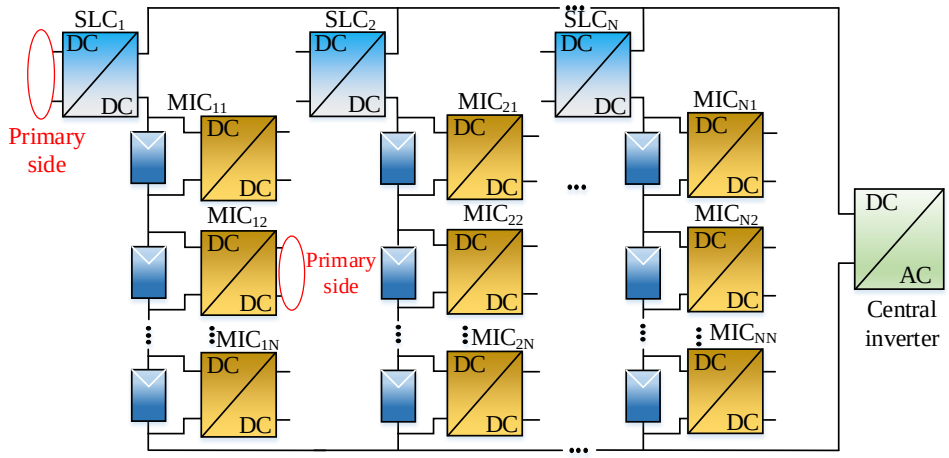

Figure 1.4.: General schematic of a DPP architecture: The primary sides can be connected to various points, including PV modules, the virtual bus, or the central inverter input. These connections and their implications will be discussed in detail in the following chapters.

1) Initial cost analysis: The complexity of the DPP architecture, particularly in terms of topologies and controllers, may be greater than that of FPP architectures. However, as described in Chapter 2, the

components' voltage and/or current ratings may be lower than those found in FPP systems, leading to reduced initial costs.

2) Financial losses due to downtime: Generally, DPP architectures have the advantage of processing only a portion of the power generated by the PV strings, allowing most of the power to be directly delivered to the output, so DPP architectures reduce stress on the components. This reduces stress on components, resulting in a higher mean time between failures (MTBF) and improved system availability, thereby minimizing financial losses associated with downtime. [23, 24].

3) Repair costs: The repair cost in DPP architectures can be reduced for two main reasons: (i) In DPP architectures, the components typically have lower voltage and current ratings compared to FPP systems, making them less expensive and (ii) the mean time to failure [25] is lower due to the high reliability resulting from the reduced stress on components.

4) Financial losses due to conversion losses: DPP architectures result in lower conversion losses by processing only a portion of the power generated by the PV strings. Consequently, as reported in [20, 22], such architectures achieve high system efficiency, which helps reduce financial losses associated with conversion losses.

These features highlight the potential to reduce the LCOE of PV systems when employing DPP architectures.

1.3. THE OBJECTIVES

The primary focus of this dissertation is to present a novel DMPPT architecture for PV systems based on DPP architectures. As detailed in subsequent chapters, DPP architectures are generally categorized into three types: SDPP (Series Differential Power Processing), PDPP (Parallel Differential Power Processing), and SPDPP (Series-Parallel Differential Power Processing). While SDPP architectures address mismatches among series-connected PV groups (typically PV modules or submodules), PDPP architectures mitigate mismatches among parallel-connected PV groups (primarily PV strings).

Compared to series connections, parallel connections of PV groups inherently experience lower power losses due to mismatches. This results in the existing literature on PDPP being relatively limited, especially when compared to SDPP. When the voltage of a PV string in a PV array drops due to temperature and irradiance differences, bypass diode activation, a short circuit in PV modules, or a module-level converter, the affected PV string's voltage changes. As a result, it differs

from the voltage of the other PV strings in the PV array. This discrepancy clamps the voltage of the other PV strings, forcing them to operate away from their MPP. Therefore, PDPP becomes an indispensable part of a PV system designed for high efficiency. Most PDPP architectures described in the literature require power electronic components tolerating the whole voltage of the PV string. To address this limitation, this dissertation focuses on developing a PDPP architecture that utilizes converters' components with voltage ratings lower than the PV strings' voltage. Furthermore, the research aims to extend this architecture into an SPDPP architecture capable of mitigating mismatches across both series- and parallel-connected PV groups. This leads to the following key research objectives:

- Is it possible to lower the voltage ratings of SLCs in PDPP architectures below the PV string voltages while still ensuring effective MPPT and high system efficiency?
- Is the proposed architecture stable and robust when using conventional Proportional–integral (PI) controllers, or does it require advanced control strategies?
- Can an energy storage device (ESD), such as a battery, be integrated into the proposed architecture, and if so, how can its charging and discharging rates be effectively controlled?
- Can the principles underlying the PDPP architecture be extended to develop a robust SPDPP system capable of eliminating mismatches across both series- and parallel-connected PV elements?

1.4. DISSERTATION OUTLINE

The outline of this dissertation is structured to address the research objectives posed in the previous section comprehensively. Before tackling these objectives, Chapter 2 lays the foundation by thoroughly reviewing DMPPT technology. It explores existing architectures, converter topologies, and control strategies, offering insights into their role in enhancing PV system performance. This chapter is crucial for understanding the advantages and novelty of the proposed SPDPP architecture.

Chapter 3 introduces the proposed architecture named PV to Virtual Bus (PV2VB) PDPP architecture, emphasizing its innovative features and benefits over conventional approaches. Key topics include the roles and responsibilities of the central converter and SLCs, SLC power ratings, and the design of the virtual bus voltage under steady-state conditions.

Chapter 4 delves into detailed modeling and dynamic analysis of the proposed PV2VB PDPP architecture, which are essential for predicting

circuit behavior under various conditions, designing robust controllers, interpreting experimental results, selecting appropriate components, and exploring new control methodologies.

Then, to address issues related to intermittency, Chapter 5 investigates the integration of batteries into the PV2VB PDPP architecture. This chapter focuses on effective energy storage management, including the control of battery charging and discharging rates.

Chapter 6 expands the proposed system into a fully realized PV2VB SPDPP architecture, enabling module-level MPPT. It provides a comprehensive explanation of the roles and functions of all converters within the system.

Finally, the conclusions of this dissertation are presented in Chapter 7, where the key findings of the research are summarized. Additionally, this chapter provides detailed recommendations for future research, identifying unexplored areas, potential challenges, and opportunities to build upon the work conducted in this study.

REFERENCES

[1] A. H. Alami *et al.* “Novel and practical photovoltaic applications”. In: *Thermal Science and Engineering Progress* 29 (2022), p. 101208.

[2] S. Karmakar and B. Singh. “Multi-MPPT 72-Pulse VSC Based High-Power Grid Interfaced Solar PV Plant With Distributed DC-Coupled Battery Energy Storage”. In: *IEEE Transactions on Energy Conversion* 39.1 (2024), pp. 37–48.

[3] P. Escobedo, M. Ntagios, D. Shakthivel, W. T. Navaraj, and R. Dahiya. “Energy Generating Electronic Skin With Intrinsic Tactile Sensing Without Touch Sensors”. In: *IEEE Transactions on Robotics* 37.2 (2021), pp. 683–690.

[4] O. Husev, D. Vinnikov, S. Kouro, F. Blaabjerg, and C. Roncero-Clemente. “Dual-Purpose Converters for DC or AC Grid as Energy Transition Solution: Perspectives and Challenges”. In: *IEEE Industrial Electronics Magazine* 18.1 (2024), pp. 46–57.

[5] X. Zhong *et al.* “A Novel Solar-Cell String Wiring of Photovoltaic Module for Reducing Lightning-Induced Overvoltage”. In: *IEEE Transactions on Electromagnetic Compatibility* 66.1 (2024), pp. 204–215.

[6] B. P. Kumar, D. S. Pillai, N. Rajasekar, M. Chakkarapani, and G. S. Ilango. “Identification and Localization of Array Faults With Optimized Placement of Voltage Sensors in a PV System”. In: *IEEE Transactions on Industrial Electronics* 68.7 (2021), pp. 5921–5931.

[7] X. Wang *et al.* “Performance Quantization and Comparative Assessment of Voltage Equalizers in Mismatched Photovoltaic Differential Power Processing Systems”. In: *IEEE Transactions on Power Electronics* 39.1 (2024), pp. 1656–1675.

[8] A. Calcabrini, M. Muttillo, R. Weegink, P. Manganiello, M. Zeman, and O. Isabella. “A fully reconfigurable series-parallel photovoltaic module for higher energy yields in urban environments”. In: *Renewable Energy* 179 (2021), pp. 1–11.

[9] A. Amoorezaei, S. A. Khajehoddin, N. Rezaei-Hosseinabadi, and K. Moez. “A Low-Cost Cell-Level Differential Power Processing CMOS IC for Single Junction Photovoltaic Cells”. In: *IEEE Transactions on Power Electronics* 36.12 (2021), pp. 13985–14001.

[10] A. Amoorezaei, S. A. Khajehoddin, and K. Moez. “A Compact Cuk-Based Differential Power Processing IC With Integrated Magnetics and Soft-Switching Controller for Maximized Cell-Level Power Extraction”. In: *IEEE Transactions on Power Electronics* 39.4 (2024), pp. 4473–4490.

[11] D. Xu *et al.* “Coupling Analysis of Differential Power Processing-Based PV System and Its Decoupling Implementation of Synchronous MPPT Control”. In: *IEEE Transactions on Industrial Electronics* 70.7 (2023), pp. 6973–6983.

[12] G. Chu, H. Wen, Y. Hu, L. Jiang, Y. Yang, and Y. Wang. “Low-Complexity Power Balancing Point-Based Optimization for Photovoltaic Differential Power Processing”. In: *IEEE Transactions on Power Electronics* 35.10 (2020), pp. 10306–10322.

[13] A. Alenezi and H. A. Hussain. “A New Control Approach for Least Processed Power Tracking Under Mismatch Conditions in PV Systems Using Differential Power Processing”. In: *IEEE Transactions on Industry Applications* 60.1 (2024), pp. 532–543.

[14] M. Kasper, D. Bortis, and J. W. Kolar. “Classification and Comparative Evaluation of PV Panel-Integrated DC–DC Converter Concepts”. In: *IEEE Transactions on Power Electronics* 29.5 (2014), pp. 2511–2526.

[15] B. Stevanović, E. Serban, S. Cóbreces, P. Alou, M. Ordonez, and M. Vasić. “DC/DC Stage Contribution to Bus Voltage in 1000V and 1500V Grid-Connected Solar Inverters”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* (2022), pp. 1–1.

[16] A. Sangwongwanich, Y. Yang, F. Blaabjerg, and D. Sera. “Delta Power Control Strategy for Multistring Grid-Connected PV Inverters”. In: *IEEE Transactions on Industry Applications* 53.4 (2017), pp. 3862–3870.

[17] B. Karanayil, S. Ceballos, and J. Pou. “Maximum Power Point Controller for Large-Scale Photovoltaic Power Plants Using Central Inverters Under Partial Shading Conditions”. In: *IEEE Transactions on Power Electronics* 34.4 (2019), pp. 3098–3109.

[18] X. Zhu *et al.* “Effects of Nonlinear MPPT Control and PV Array on Stability Analysis for a Utility-Scale PV Energy System”. In: *IEEE Transactions on Energy Conversion* 38.3 (2023), pp. 1530–1543.

[19] N. Tak, S. K. Chattopadhyay, and C. Chakraborty. “Single-Sourced Double-Stage Multilevel Inverter for Grid-Connected Solar PV Systems”. In: *IEEE Open Journal of the Industrial Electronics Society* 3 (2022), pp. 561–581.

[20] C. Olalla, C. Deline, D. Clement, Y. Levron, M. Rodriguez, and D. Maksimovic. “Performance of Power-Limited Differential Power Processing Architectures in Mismatched PV Systems”. In: *IEEE Transactions on Power Electronics* 30.2 (2015), pp. 618–631.

[21] D. Vinnikov, A. Chub, R. Kosenko, V. Sidorov, and A. Lindvest. “Implementation of Global Maximum Power Point Tracking in Photovoltaic Microconverters: A Survey of Challenges and Opportunities”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 11.2 (2023), pp. 2259–2280.

[22] K. A. Kim, P. S. Shenoy, and P. T. Krein. “Converter Rating Analysis for Photovoltaic Differential Power Processing Systems”. In: *IEEE Transactions on Power Electronics* 30.4 (2015), pp. 1987–1997.

[23] P. S. Shenoy, K. A. Kim, B. B. Johnson, and P. T. Krein. “Differential Power Processing for Increased Energy Production and Reliability of Photovoltaic Systems”. In: *IEEE Transactions on Power Electronics* 28.6 (2013), pp. 2968–2979.

[24] H. Jeong, H. Lee, Y. Liu, and K. A. Kim. “Review of Differential Power Processing Converter Techniques for Photovoltaic Applications”. In: *IEEE Transactions on Energy Conversion* 34.1 (2019), pp. 351–360.

[25] A. Nazer, S. Driss, A. M. Haddadi, and S. Farhangi. “Optimal Photovoltaic Multi-String Inverter Topology Selection Based on Reliability and Cost Analysis”. In: *IEEE Transactions on Sustainable Energy* 12.2 (2021), pp. 1186–1195.

2

CLASSIFICATION OF DMPPT ARCHITECTURES FOR PHOTOVOLTAIC SYSTEMS

In PV systems, unavoidable factors such as partial shading, non-optimal mounting angles of PV modules, and accumulation of dust result in mismatches, consequently diminishing energy yield. A promising solution to mitigate these issues is to use Distributed Maximum Power Point Tracking (DMPPT) architectures. To alleviate mismatch-related losses, many DMPPT architectures, including Full Power Processing (FPP) and Differential Power Processing (DPP), have been documented in the literature. FPP encompasses techniques like microinverters, Modular Multilevel Cascade Inverters, and DC architectures such as parallel, series, and total cross-tied. DPP variants include series DPP, parallel DPP, and series-parallel DPP architectures. Moreover, novel DMPPT architectures like hybrid and hierarchical architectures and advancements in converter topologies and control strategies continue to emerge, aiming to improve the LCOE. Each novel solution brings distinct advantages and challenges, but the extensive number of architectures, power converter topologies, and control methods have led to confusion and complexity in navigating the literature. This chapter systematically categorizes, reviews, and compares various DMPPT architectures, associated converters, and control strategies, providing a comprehensive overview of the evolving landscape of DMPPT development.

Parts of this chapter are currently under review [1].

2.1. INTRODUCTION

As briefly discussed in Chapter 1, DMPPT can minimize mismatch-related losses by enhancing the granularity of power conversion [2, 3]. The literature introduces DMPPT architectures at various levels of granularity, including string, module, submodule, and cell levels [4–14]. However, each level has limitations in addressing mismatches among PV groups with higher granularity. For instance, while SLCs can mitigate mismatches among PV strings, they are ineffective at the module level. On the other hand, CICs have low DC-AC conversion efficiency due to technological limitations in efficiently amplifying a PV cell's very low voltage. Moreover, having one converter per cell would escalate system complexity and cost. Generally, higher granularity reduces mismatch-related losses but increases power conversion losses. Thus, MIC and SMIC have got significant attention from researchers and industry.

Research on DMPPT has primarily focused on two main architectures: full power processing (FPP) [15–18] and differential power processing (DPP) [19–21]. FPP comprises AC-FPP and DC-FPP, with microinverters and multilevel cascade inverters (MMCI) belonging to the former and parallel, series, and total cross-tied (TCT) architectures to the latter. DPP is further divided into series DPP (SDPP), parallel DPP (PDPP), and series-parallel DPP (SPDPP) architectures. Also, hybrid and hierarchical DMPPT solutions have been proposed [22], leading to a plethora of new architectures. Various converter topologies and controllers have been developed for these architectures, each with unique advantages and drawbacks. The selection of the most suitable architecture depends on the specific application's requirements, such as reliability, simplicity, efficiency, and cost-effectiveness, which vary across different PV applications. Navigating the extensive literature on DMPPT architectures, converter topologies, and controllers can be confusing due to the multitude of options available. Therefore, there is a critical need for a comprehensive survey that provides a broad overview of these techniques.

As shown in Fig. 2.1, this chapter aims to fulfill this need by presenting and categorizing recent DMPPT techniques along with their associated converters and controllers. It also discusses the advantages and challenges for each architecture and gaps in the literature. This chapter begins with an overview of MPPTs at the array and string levels (Section 2.2), then explores module- and submodule-level DMPPT through FPP converters (Section 2.3). Section 2.4 delves into different DPP-based DMPPT architectures, while Section 2.5 discusses the integration of these architectures to create hybrid and hierarchical DMPPT PV systems. Finally, Section 2.6 summarizes this chapter and discusses its findings.

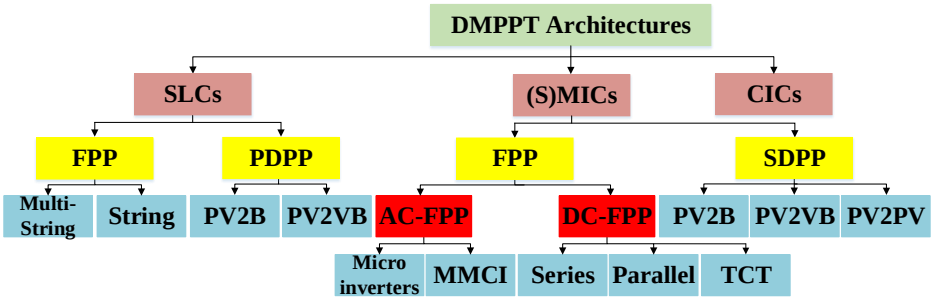

Figure 2.1.: Taxonomy of DMPPT architectures.

2.2. MPPT AT ARRAY LEVEL AND DMPPT AT STRING LEVEL

Fig. 2.2(a) shows a PV array connected to an ALC. These systems are known for their simplicity and low construction costs [12], making them attractive and widely used in open areas with uniform sunlight and minimal mismatches, as they can achieve a low LCOE. ALCs are often categorized into single-stage and double-stage topologies [14, 23]. In a double-stage topology, a DC-DC converter tracks the PV array's MPP. In contrast, a DC-AC converter keeps a fixed DC link voltage v_S. It ensures that grid requirements such as power quality, islanding operation detection, and grounding are met [13]. The high capacitance of the DC link decouples the performance of DC-DC and DC-AC converters. Conversely, a single-stage ALC integrates both DC-DC and DC-AC functions into a single converter, thus performing all duties in a unified manner [24, 25].

In DC-AC converters, maintaining a sufficiently high DC link voltage (v_S) is crucial to avoid entering the over-modulation region of PWM. In single-stage architectures, the PV array's voltage (v_{PV} in Fig. 2.2(a)) corresponds to the DC link, potentially leading to over-modulation if the PV array's MPP voltage is too low. In contrast, double-stage topologies incorporate a DC-DC converter between the PV array and the DC-AC converter, broadening the MPPT range. Additionally, the fixed DC-link voltage in double-stage architectures enables designers to optimize components for the DC-AC stage, enhancing efficiency [26–28]. However, processing power twice through both converters in double-stage architectures results in additional losses and complexity. Efforts to improve efficiency include proposals for partial power processing converters in the DC-DC stage [26, 29]. Conversely, single-stage topologies offer reduced component count, cost, and size, albeit with a variable DC link voltage [24, 25].

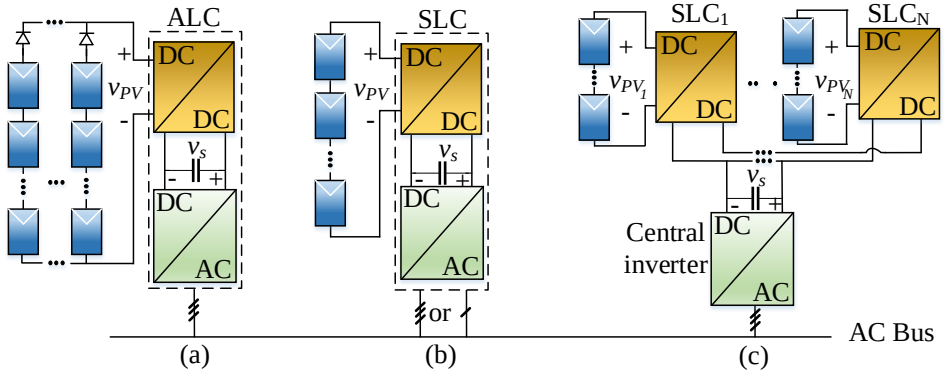

Figure 2.2.: Array- and string-level MPPT architectures. (a) MMPT at array level with a double-stage ALC, (b) DMPPT at string level with a double-stage SLC, and (c) DMPPT at string level with SLCs and a central inverter.

In array-level MPPT, mismatches within the PV array lead to the reduction of energy yield. Additionally, challenges such as high-voltage DC cables, losses in string blocking diodes, and limited scalability further diminish the effectiveness of array-level MPPT [30–32]. These obstacles can be addressed through two main string-level MPPT architectures. The first involves connecting each PV string directly to the grid via SLCs (Fig. 2.2(b)) [33], also known as string inverters, which come in both single-stage and double-stage topologies [10, 34]. Alternatively, the PV strings can be connected to a common DC link through SLCs before being connected to the grid via a central inverter, in the so-called a multi-string architectures (Fig. 2.2(c)) [11, 35, 36]. As shown in Fig. 2.3, various converter topologies, including two-level voltage source inverter (2L-VSI), three-level neutral-point-clamped (3L-NPC), T-type, and three-level active neutral-point-clamped (3L-ANPC), are commonly employed for the three-phase DC-AC stage in both SLCs and ALCs, with associated power module packages commercially available for PV applications [37, 38]. While three-level power converters offer higher efficiency, the 2L-VSI topology has higher reliability due to its lower component count [35, 39]. Notably, MMCIs, which will be discussed in Section 2.3, can be used as SLCs or ALCs.

Infineon has introduced power modules for four popular topologies used in the single-phase DC-AC stage of SLCs (Fig. 2.4) [40]. The conventional Full-Bridge topology, while simple in structure, suffers from high power losses, Total harmonic distortion (THD), and leakage current, necessitating larger cooling systems and AC filters, increasing inverter size and weight. To address these issues, other topologies

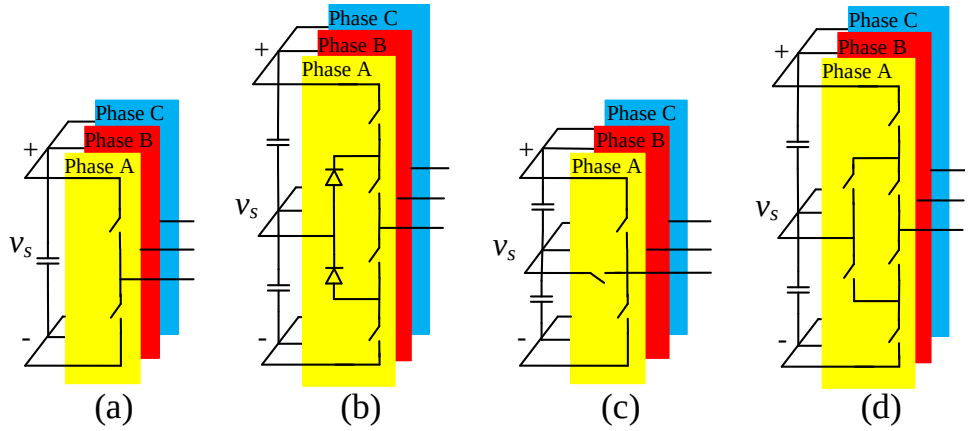

Figure 2.3.: Three-phase DC-AC stage converter topologies for SLC or ALC. (a) 2L-VSI, (b) 3L-NPC (c) T-type (d), and 3L-ANPC.

like Multilevel, HERIC, and H6 have been developed, offering reduced filter size, Electromagnetic interference (EMI), improved power quality, and higher efficiency and lower system cost, size, and weight. Further details can be found in relevant literature [40, 41].

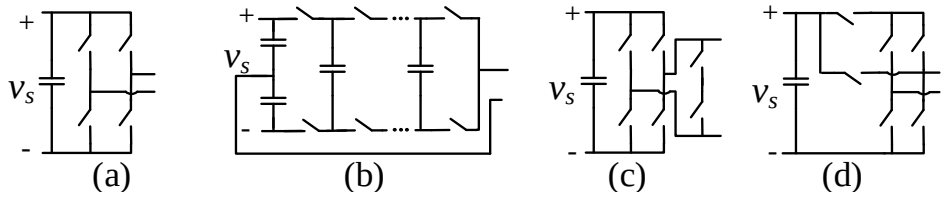

Figure 2.4.: DC-AC stage of string inverter for single-phase topologies: (a) Full-Bridge, (b) Multilevel, (c) HERIC, and (d) H6.

2.3. DMPPT AT MODULE LEVELS WITH FPP MICS

The limitations of string-level DMPPT architectures in addressing mismatches among PV modules within the same string have led to exploring module- and submodule-level DMPPT architectures as a solution. Literature highlights energy yield improvements achieved through the use of SMICs and MICs. For instance, SMA reports efficiency gains of approximately 1%-4% with microinverters compared to SLCs [42]. The report indicates that when considering cost, expenses, and reliability factors, a microinverter typically offers a shorter payback time compared to a string inverter system for PV systems under 3

kW. However, it is important to note that this is not a universal conclusion; results can vary significantly based on different testing areas and considerations. For example, another study has shown significant energy yield enhancements with SMICs and MICs, reporting increases of up to 9.13% and 4.01%, respectively, compared to SLCs [2]. This suggests that the energy yield enhancements reported in [2] are higher than those indicated by SMA, leading to different outcomes.

Besides, MICs offer better-enhanced protection, monitoring, and fault diagnosis capabilities, facilitating quicker repairs and improving system availability [43, 44]. Furthermore, MICs and SMICs help prevent system interruptions in case of a single failure, and manufacturing costs are expected to be reduced with mass production. MICs, in particular, simplify the MPPT algorithm by reducing the number of local MPPs, making them suitable for complex environments such as building-integrated PV systems. Consequently, many industrial companies have introduced and continue to innovate these technologies in the market [45–57]. The most straightforward way to implement (S)MICs is through FPP converters. A general classification of FPP solutions is presented in Fig. 2.5. They can be subdivided into two main categories: (i) AC-FPP and (ii) DC-FPP.

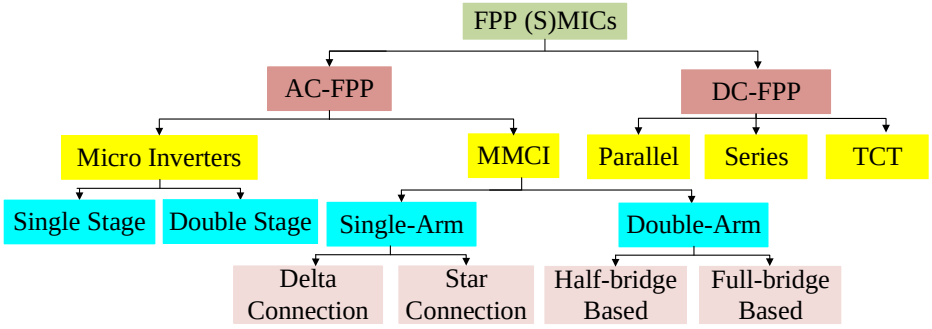

Figure 2.5.: Taxonomy of FPP (S)MICs, branching out AC-FPP and DC-FPP solutions.

2.3.1. AC-FPP

AC-FPPs convert DC input voltage to AC, allowing direct connection to the AC grid without requiring a central converter. AC-FPPs are categorized into (i) microinverters and (ii) MMCIs.

MICROINVERTERS

Microinverters represent one of the earliest approaches to achieving DMPPT at the module level, as depicted in Fig. 2.6. They offer several unique advantages, including easy attachment to the back of PV modules, independent tracking of the MPP of each module without cross-coupling effects, and resilience to failure or shading of individual modules or microinverters, ensuring continued system operation with minimal reduction in total power production [15]. Microinverters also have plug-and-play functionality, facilitating straightforward installation and maintenance of PV systems. These features enhance system flexibility, modularity, scalability, and reduce installation costs [15, 58, 59]. Such benefits have led companies [45–53] to industrialize and researchers stage [60–68] to explore and propose new microinverter topologies for this architecture.

Despite their promising advantages, microinverters face challenges such as the need for high voltage gain, which results in increased complexity and conversion losses. Moreover, in single-phase microinverters, grid power ripple flows in the DC link, causing a double line frequency ripple at the DC link voltage [69]. This disturbance in the ripple deteriorates MPPT performance and efficiency. To mitigate this issue, the use of electrolytic high-capacitance capacitors for power decoupling is essential, but these capacitors shorten the lifetime of microinverters and reduce their power density [15, 58].

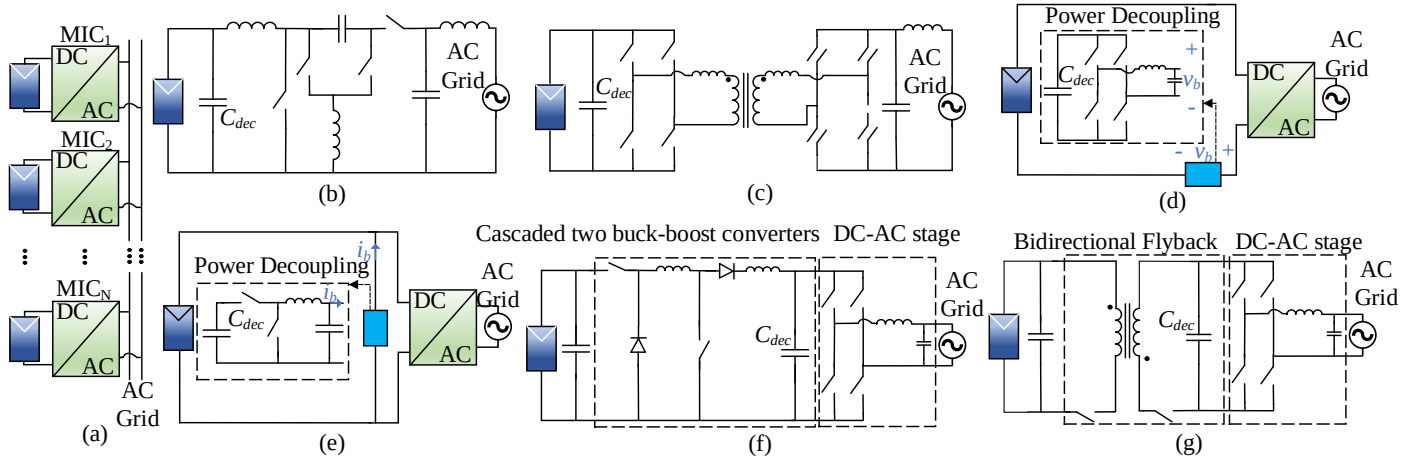

Figure 2.6.: Microinverters: (a) system's configuration and (b-h) topologies. (a) Every module is connected to the AC grid through its own MICi. (b) Non-isolated single-stage [60], (c) isolated single-stage [62], (d) isolated single-stage with series power decoupling, (e) isolated single-stage with parallel power decoupling [63, 64], (f) non-isolated double-stage [66], (g) isolated double-stage [45].

Various converter topologies have been proposed for microinverters, which can be categorized into four classes: (i) non-isolated single-stage (Fig. 2.6(b)) [60, 61], (ii) isolated single-stage (Fig. 2.6(c)) [62–64], (iii) non-isolated double stage (Fig. 2.6(f)) [65, 66], and (iv) isolated double stage topologies (Fig. 2.6(g)) [67, 68]. In single-stage topologies, one stage fulfills various microinverter duties, including MPPT, voltage amplification, current grid control, DC-AC conversion, and compliance with grid requirements. The non-isolated single-stage topology, requiring fewer components and no transformers, offers a low-cost, low-complexity, and highly efficient solution [60, 61]. However, capacitors must be decoupled on the PV modules' side, where the nominal voltage is relatively low. Thus, to enhance MPPT efficiency, voltage ripple should be limited to a small amplitude, necessitating a large decoupling capacitance in non-isolated single-stage topologies, thereby shortening their lifetime.

The literature proposes decoupling circuits for isolated single-stage microinverters, which usually come in two types [70]: series power decoupling (Fig. 2.6(d) or parallel power decoupling (Fig. 2.6(e)) [63, 64] with a PV module. These auxiliary circuits, positioned between the PV module and inverter, reduce decoupling capacitance while introducing extra components and associated power losses. They enable the replacement of high-capacitance electrolytic capacitors with high-reliability film capacitors, thereby enhancing the lifetime of microinverters [59].

In double-stage microinverters, two cascaded converters are utilized. The first stage, a DC-DC converter connected to the PV modules, handles MPPT and voltage amplification. In contrast, the second stage, a DC-AC converter, manages current grid control, DC-AC conversion, and grid requirements. In this architecture, decoupling capacitors are typically placed at the DC-Link, benefiting from its high voltage to reduce the required capacitance. Utilizing a transformer is a straightforward solution in double-stage microinverters to eliminate leakage current and meet the National Electrical Code (NEC) standard's dual-grounding requirement [71]. Moreover, isolated microinverter topologies exhibit lower THD in the output current compared to non-isolated ones [15]. Isolation with line-frequency and high-frequency transformers (HFT) are the two basic families of isolated microinverters. While HFTs offer greater efficiency, compactness, and cost-effectiveness compared to line-frequency transformers, it still introduces losses, costs, and space constraints. Thus, research also explores non-isolated double-stage topologies to reach high efficiency, compactness, and low cost. A comparison of microinverter topologies is summarized in Tabel 2.1.

Table 2.1.: Comparison of microinverters topologies

Topologies	Efficiency	Power density	Lifetime	Cost	THD
Non-isolated single-stage [60, 61]	High	High	Short	Low	Moderate
Isolated single-stage [62]	High	Moderate	Short	Moderate	Good
Isolated single-stage with decoupling circuit [63, 64]	Moderate	Moderate	Long	High	Good
Non-isolated double-stage	High	High	Long	High	Moderate
Isolated double-stage [65, 66]	Moderate	Moderate	Long	High	Good
Microinverter with low-frequency transformer [67, 68]	Low	Low	Variable*	High	Good

* *it depends on the location of the decoupling capacitor.*

MMCI

In the 1990s, MMCIs debuted for high-power motor drives, featuring multiple series-connected DC-AC inverters known as inverter cells (Fig. 2.7). These systems have advantages like reduced EMI, THD, acoustic noise, switching stress, compact AC filter size, high power density, modularity, and scalability. Many companies, including ABB, TMEIC GE, and Siemens, swiftly integrated MMCIs into various applications such as Static Synchronous Compensator (STATCOM), active power filters, and electric drives.

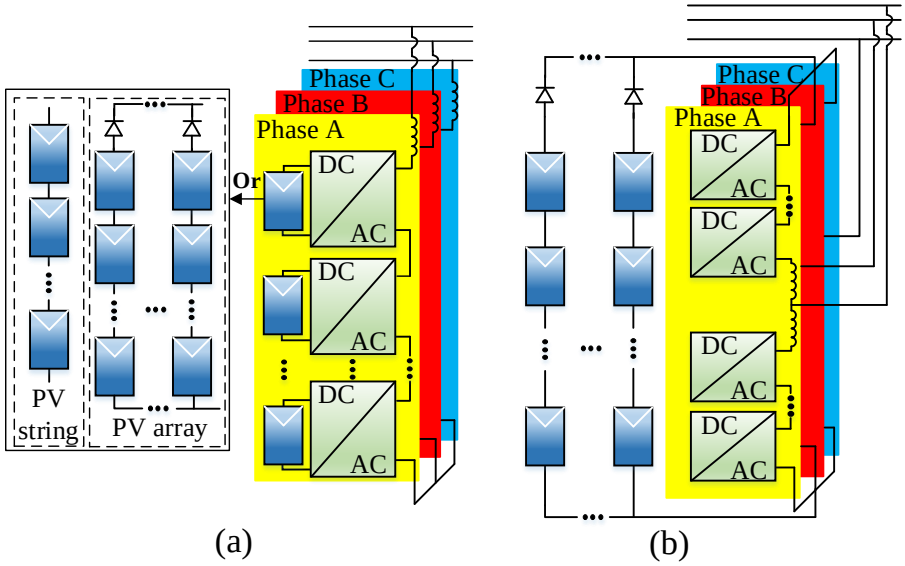

Figure 2.7.: MMCI in PV applications. (a) MMCI inverter cells as MICs, SLCs, and ALCs, and (b) MMCI as an ALC.

A key drawback of MMCIs lies in their requirement for isolated multiple DC voltage sources, necessitating complex multi-winding phase-shifted line-frequency transformers to distribute electric power among the floating inverter cells [72]. Despite this limitation, MMCIs prove beneficial for PV systems, enabling DMPPT due to the availability of multiple independent and isolated DC sources like PV modules, strings, or arrays. Additionally, as shown in Fig. 2.7 (b), MMCIs can serve as ALCs with a common bus, offering potential cost, weight, and volume savings by eliminating conventional medium voltage transformers [73, 74]. Thus, MMCIs present a promising solution for both DMPPT and ALC architectures.

MMCI architectures are classified based on the number of leg inductors

per phase. In terms of leg inductors, architectures include single-leg (Fig. 2.8 (a) and Fig. 2.8 (b)) [75–78] and double-leg (Fig. 2.8(c)) [79–81]. The appropriate inverter cell topologies for MMCIs are further categorized based on: (i) the number of power processing stages, and (ii) the use of HFTs for isolation. In medium and high-voltage PV systems, the utilization of [81] HFT [81–83] becomes indispensable due to the Maximum System Voltage specified in PV module datasheets. This voltage parameter is determined by the sum of the maximum open-circuit voltages of all PV modules within a string, typically ranging from 600V to 1500V. However, in architectures like MMCI with single-stage [76, 77] or non-isolated inverter cells [75, 84], PV modules are interconnected in series through certain switching sequences. Consequently, if the total string voltage exceeds the maximum system voltage threshold, which is common in medium- and high-voltage PV systems, not only does the PV system fail to meet standards, but it also risks damaging the PV modules [82, 83].

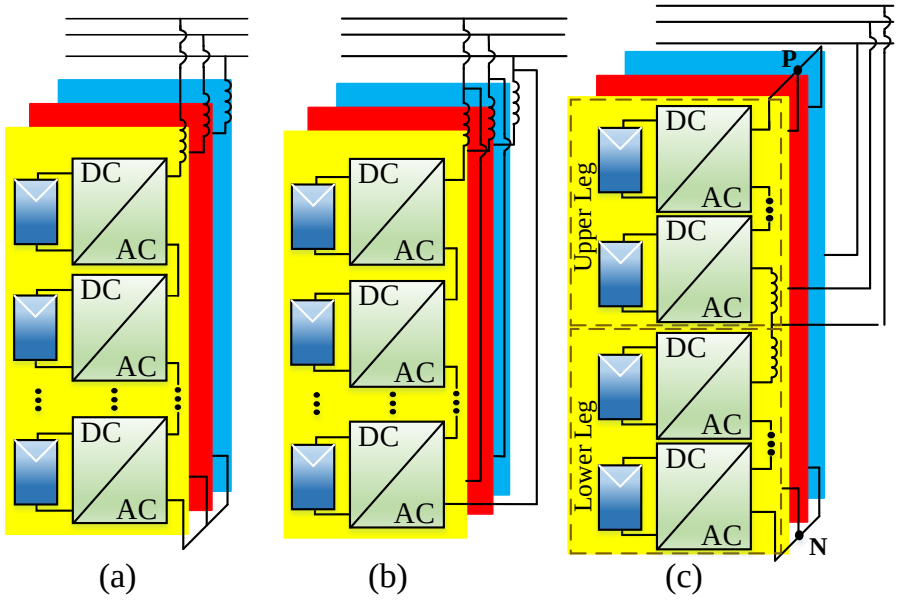

Figure 2.8.: MMCI architectures. (a) SSFC, (b) SDFC, and (c) DSFC and DSHC.

Table 2.2.: Comparison among the four MMCI architectures, assuming identical blocking voltage and power ratings for components.

Config.	Number of Switches	Number of Inverter Cells	Circulating Current	Balancing Control	Balancing Limitation	Balancing Capability
SSFC [74, 85]	N	4N	No	ZSV	Maximum available DC-link voltage	Average
SDFC [86, 87]	$\sqrt{3}N$	$4\sqrt{3}N$	Yes	ZSC	Maximum inverter cell current	Good
DSFC [88]	2N	4N	Yes	ZSV or Circulating current injection	Maximum available DC-link voltage or maximum inverter cell current	Good
DSHC [89, 90]	N	4N	Yes	ZSV or Circulating current injection	Maximum available DC-link voltage or maximum inverter cell current	Good

* *All architectures have the same grid voltage and inverter cell voltage.*

Focusing specifically on the DC-AC processing stage, as illustrated in Fig. 2.9, two main topologies are commonly used: half-bridge and full-bridge inverters. Half-bridge cells generate only zero and positive voltages, leading to a DC component in single-leg architectures. In contrast, double-leg architectures, which utilize two legs per phase, mitigate DC components and can accommodate both full-bridge and half-bridge topologies. [79, 88]. Another difference between single-leg and double-leg architectures is the presence of a common DC link, connected to the phases' upper (P) and lower (N) sides (Fig. 2.8 (c)) in double-leg architectures, enabling their application as ALC without additional components, as shown in Fig. 2.7 (b) [89]. Given that three single-leg architectures can be connected in either star or delta connection, MMCI architectures are classified into four groups [91]: (i) single-star full-bridge cell (SSFC) [74, 85], (ii) SDFC [86, 87], (iii) double-star full-bridge cell (DSFC) [88], and (iv) double-star half-bridge cell (DSHC) [89, 90]. Table 2.2 compares three-phase MMCIs based on the assumption that components with the same voltage and current ratings are used in the four architectures.

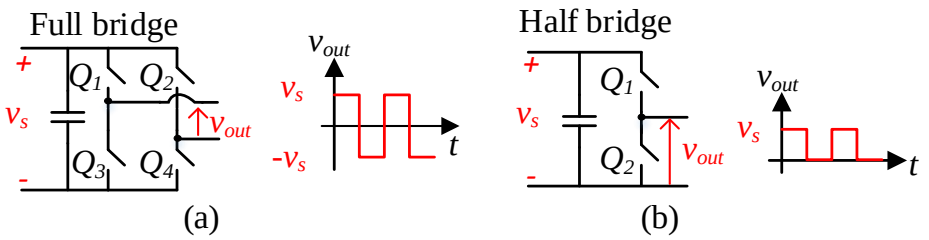

Figure 2.9.: MMCI cells. (a) Full-Bridge, and (b) half-bridge DC-AC converter topologies.

MMCIs face various challenges caused by mismatches, including power imbalances among inverter cells or phases, called inter-bridge and inter-phase power imbalances [73, 92]. Additionally, in double-star architectures, inter-leg power imbalances arise [16]. Addressing inter-phase power imbalances necessitates injecting additional Zero-sequence voltage (ZSV) or Zero-sequence current (ZSC) into each phase, with their application varying depending on the architecture. However, the severity of power imbalances dictates the injected ZSV/ZSC and subsequently impacts the inverter cell's required voltage or current rating. The SSFC architecture exhibits the narrowest range in addressing power imbalances [16, 86]. Eventually, MMCIs face the challenge of necessitating high capacitance when utilized for DMPPT, as the structure must filter the double-line frequency for each floating inverter cell, regardless of whether it is three-phase or single-phase. Therefore, their complexity is only justified when the PV plant is directly

connected to a medium-voltage grid without a transformer. However, as previously discussed, this scenario presents significant isolation coordination challenges. Consequently, despite being a research topic, the practical application of MMCIs in PV systems remains limited.

Table 2.3.: Comparison of AC-FPP/DC-FPP Architectures.

Features	**Microinverters/ Parallel DC-FPP*** [60–62, 65, 67, 68, 93, 94]	**MMCIs/ Series DC-FPP*** [32, 85–87, 95, 96]
Phase Number	Single phase	Single/or Three phase
EMI**	High	Low
AC filter size	Large	Small
Switching frequency**	High	Low
Power processing**	Full	Full
Applicable in medium-voltage PV system**	No	Yes
High gain converters**	Required	Not required
Improving efficiency of switching converters**	Challenging	Easy
Cross-Coupling Effects**	No	Yes
Availability against failure of several modules **	Excellent	Vulnerable
Flexibility	High	Low
Elements voltage rating **	High voltage	Low voltage

** While microinverters and parallel DC-FPP share similar features, MMCIs and series DC-FPP also have comparable characteristics. Therefore, the comparison of microinverters with MMCIs and parallel DC-FPP with series DC-FPP is presented in a single table.*

*** These features can be extended to compare parallel with series DC-FPP.*

In this section, we have introduced two approaches for AC-FPP: microinverters and MMCIs, each with its distinct characteristics outlined

in Tabel 2.3. MMCIs offer advantages such as generating multilevel output voltages, enabling low switching frequency, small AC filter size, and low electromagnetic interference. However, their series connection of inverter cells can lead to increased conduction loss and issues with power imbalances during mismatch conditions. On the other hand, microinverters provide benefits such as resilience to single failures or mismatch conditions, ensuring continuous operation with only a slight reduction in power production. In contrast, MMCIs require careful attention to fault detection, redundancy, and their impact on system performance to ensure that a failure of a single device does not compromise the overall system [97, 98]. Additionally, while installing microinverters is typically plug-and-play, MMCIs demand more extensive considerations such as electrical integration, control, communication, and compliance with standards like NEC. As a result, microinverters provide greater modularity and flexibility than MMCIs. Eventually, while MMCIs consist of series-connected inverter cells that necessitate low-voltage components, microinverters require high-voltage components. These factors must be considered when selecting the most suitable approach for a given PV system.

2.3.2. DC-FPP

In DC-FPP architectures, the requirement to comply with distributed AC grid connection standards—such as filtering, protection, control, and double-line frequency ripple—has been effectively addressed. However, DC-FPP architectures require a central DC-AC converter, which could potentially pose a bottleneck for the PV installation due to the single-failure-point problem [99, 100]. Generally, DC-FPP architectures can be categorized as parallel, series, and TCT architectures (Fig. 2.10).

PARALLEL DC-FPP

In a parallel DC-FPP architecture, illustrated in Fig. 2.10 (a), MICs, also known as parallel optimizers, are connected to PV modules and share a common DC bus. They have traits similar to microinverters, including immunity to the cross-coupling effect, flexibility, modularity, and scalability [32, 94]. Additionally, with only a single stage for DC-DC conversion, they require fewer components. EIQ Energy and other companies have industrialized this solution [54]. However, challenges include the need for high step-up DC-DC conversion and high efficiency. To address these challenges, literature has reported on many high step-up converters [101].

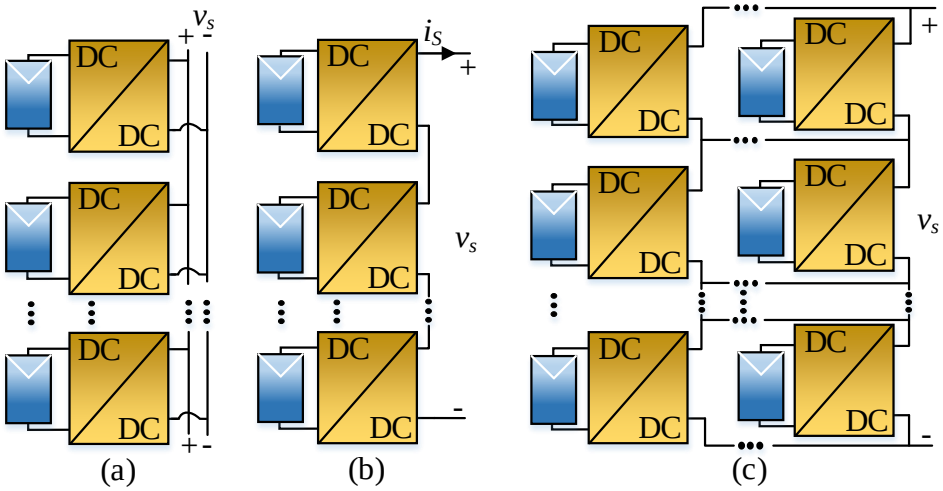

Figure 2.10.: DC-FPP architectures. (a) Parallel, (b) Series and (c) TCT.

SERIES DC-FPP

In series DC-FPP architecture, depicted in Fig. 2.10 (b). MICs, also known as series optimizers, are in series to create a DC bus. This architecture offers several benefits, including reduced voltage gain requirements for MICs due to the stack structure. This results in more efficient, smaller, less expensive, and simpler MICs than that of parallel architectures[17]. Notably, Series DC-FPP has been industrialized by several companies like SolarEdge [56], Tigo Energy [55], Taylor [102], and Xandex [57]. Converters employed in series DC-FPPs can be classified into three categories: (i) buck-based [95], (ii) boost-based [32, 96], and (iii) buck-boost-based [9, 103]. These categories differ primarily in their response to partial shading and their ability to maintain matching between the current of shaded PV modules and the string current (i_S).

During mismatch conditions, buck-based converters regulate the voltages of shaded PV modules downward, increasing their output currents to match those of unshaded PV modules. This process lowers the DC link voltage (v_S) compared to uniform operating conditions, necessitating a minimum number of PV modules per string to maintain a specified minimum DC link voltage during mismatch. Additionally, the string current must consistently exceed the currents of all PV modules to ensure that those with MPP currents higher than the string current operate at their MPP. The converters' maximum output current rating determines the maximum number of PV modules with associated buck converters per string for a given DC-bus voltage. Boost-based converters increase the voltage of unshaded PV modules, reducing their

output currents to match those of shaded modules. This results in an increase in converter output voltage. The maximum number of PV modules per string is determined by the converters' maximum output voltage for a given string voltage. However, to ensure maximum power extraction, the string current must always be lower than the currents of individual PV modules. Failure to meet this criterion may prevent PV modules with lower MPP currents from operating at their maximum power point.

In buck-based and boost-based architectures, the PV string voltage varies to achieve the MPP, so even in DC grids, an additional stage is necessary to maintain a constant output voltage equal to the DC grid voltage. Buck-boost-based converters offer a solution to this issue. Without limitations on the PV string current range, the total voltage of series-connected converters can remain constant, allowing for a wider range of PV modules per string. The upper and lower limits for the number of PV modules per string are determined by the maximum output current and voltage ratings of the MICs [9, 104]. These advantages come with typical disadvantages associated with buck-boost converters: lower converter efficiency, increased complexity, more components, and susceptibility to load variation [104].

The features of parallel and series DC-FPPs share similarities with microinverters and MMCI. Hence, the star-marked features represented in Table 2.3 can be extended to compare parallel and series DC-FPP architectures.

TCT DC-FPP

Series and parallel DC-FPP architectures have their own advantages and challenges. On the one hand, series DC-FPPs are susceptible to cross-coupling effects, potentially leading to PV modules operating away from their MPP and reducing system output power [18, 32]. On the other hand, parallel DC-FPPs are immune to cross-coupling but require high voltage step-up ratios for MICs, leading to higher voltage stress on switches and reduced conversion efficiency. To address these challenges, the recently proposed TCT DC-FPP architecture (Fig. 2.10 (c)) [18] offers a potential solution claimed reducing cross-coupling compared to series DC-FPP. However, the TCT architecture introduces complexities due to its combination of series and parallel connections among MICs, making scalability and implementation challenging.

Both non-isolated and isolated topologies can be applied to DC-FPP architectures. Non-isolated topologies include buck, boost, buck-boost, zeta, SEPIC, Ćuk, and derivatives. Isolated topologies mainly consist of forward, push-pull, flyback, half-bridge, full-bridge and resonant converters [17, 99]. Notably, it is possible to use partial power converters in the architectures shown in Fig. 2.10 to enhance overall system efficiency and reduce system costs. In this case, they are

classified as Partial Power Processing (PPP) architectures [99, 105].

2.4. SDPP (S)MICs and PDPP SLCs

In FPP architectures, while mismatch-related losses among PV modules or submodules are eliminated, the MICs handle all the power generated by the PV modules even under uniform conditions. This leads to increased power conversion losses, size, and cost of MICs. To address these issues, the concept of DPP, initially proposed for electric vehicle battery charge equalization, has been extended for PV applications. DPPs are categorized into SDPP, PDPP, and SPDPP, as depicted in Fig. 2.11. Further details on these approaches are provided in the following subsections, primarily discussing module-level MICs and occasionally SMICs depending on the focus. However, the described approaches, architectures, topologies, and methods, along with their advantages, drawbacks, and challenges, are equally relevant at both module and submodule levels.

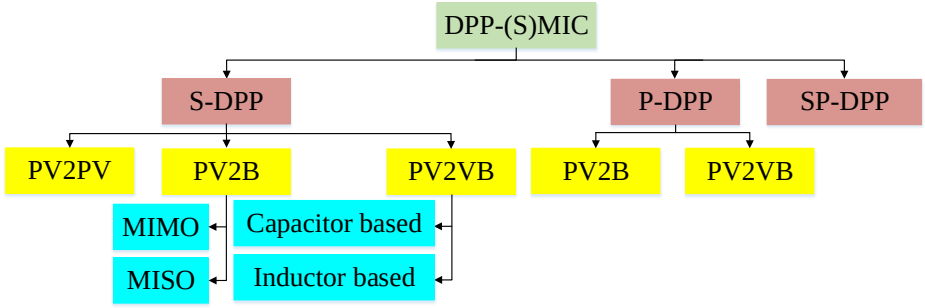

Figure 2.11.: Taxonomy of DPP architectures, branching out SDPP, PDPP, and SPDPP solutions.

2.4.1. SDPP

In SDPP architectures, depicted in Fig. 2.12(a), MICs specifically manage the differential current between individual PV modules and the overall PV string current (i_S). Under uniform conditions where there is no mismatch among PV modules, MICs remain inactive, reducing their operational load and enhancing their reliability and lifespan. During mismatch conditions, MICs only process a fraction of the power, while most of the power generated by the PV modules flows directly to the output without local processing. This offers two key advantages: firstly, it reduces MICs' operational time and increases system efficiency, even

if the efficiency of SDPP MICs is lower than FPP MICs. Secondly, it alleviates stress on components, resulting in improved reliability and lifespan. Although the concept is new, due to its advantages, SDPP has already been patented [106–108] and industrialized by the company Optivolt [109].

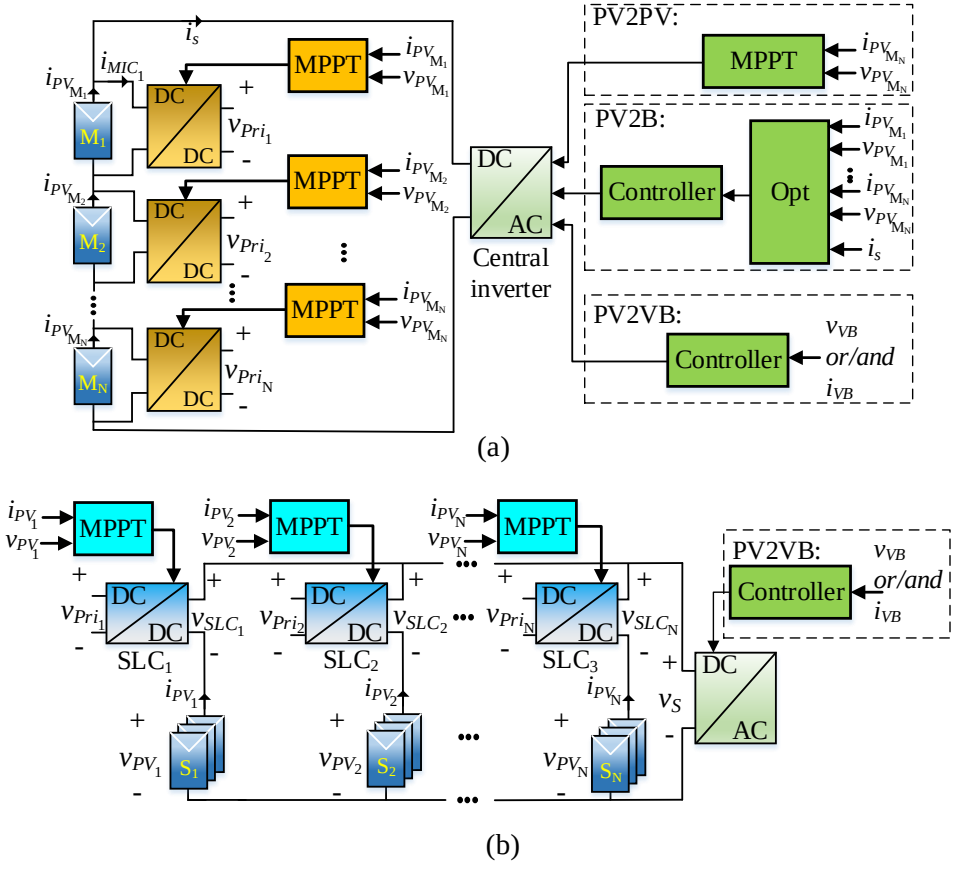

Figure 2.12.: PV systems using DPP architectures: (a) SDPP, (b) PDPP.

In SDPP architectures, the need to increase the power rating of MICs to address heightened mismatch conditions can lead to an increase in the size and cost of the MICs. However, severe mismatch conditions are rare, rendering it economically unjustifiable to increase the power rating of MICs. When MICs are assigned an infinite power rating, the current-voltage (I-V) curve at the central inverter's input simplifies, featuring only a single peak, streamlining its MPPT algorithm. Conversely, when the converter rating is restricted to a fraction of PV modules' MPP, MICs' operation is confined to nominal power during severe mismatch

conditions. This limitation prompts the appearance of local peaks in the I-V curve at the central inverter, necessitating MPPT algorithms capable of tracking the global peak and introducing mismatch losses. Thus, research endeavors to determine the optimal MIC ratings for designing SDPP PV systems [2, 110].

The ideal operation for SDPP MICs ensures each PV module operates at its true MPP. Achieving true MPP tracking often involves additional local sensors or complex communication systems, both of which come with drawbacks such as increased power losses, higher costs, reduced reliability, and added complexity [111, 112]. An alternative approach, voltage equalization (VE), forces all PV modules to operate at the same voltage level, minimizing mismatch losses. While VE methods still encounter some mismatch losses, they benefit from the low sensitivity of PV modules' MPP voltage to changes in environmental conditions, keeping modules near their MPP. Indeed, as demonstrated in [2], VE at the submodule level results in additional energy yield losses of less than 2% compared to True MPPT, even in extreme worst-case scenarios. For instance, even with a significant temperature difference of 25°C between PV submodules, power losses lower than 1.7% were achieved experimentally. Furthermore, the effects of reduced irradiance and lower temperature tend to offset each other, leading to smaller power losses in PV systems.

VE strategies can be either open-loop [113] or closed-loop [7]. Open-loop control, though simple and cost-effective, lacks the ability to limit MIC power during extreme mismatch conditions and is susceptible to inaccuracies and external disturbances. Closed-loop control offers the advantages of precise regulation but requires additional sensors or communication capabilities. The choice between VE and true MPP approaches depends on factors such as system complexity, cost, and reliability. Tabel 2.4 provides a comparison of these methods.

All DPP MICs are linked directly to PV modules. The SDPP architecture varies based on where each MIC's primary is connected, resulting in three subcategories: (i) PV2PV, (ii) PV2B, and (iii) PV2VB. These architectures will be thoroughly examined in the subsequent sub-subsections.

PV2PV

In the PV2PV architecture (Fig. 2.13(a)), each SDPP MIC's secondary is connected to a PV module, while its primary connects to the subsequent PV module in the string. It ensures that each MIC regulates the operating point of only one PV module, focusing solely on achieving MPP operation for that PV module. One advantage of this architecture is that the voltage rating of the MIC components is determined solely by the PV module's voltage. Additionally, non-isolated MICs can be utilized, improving efficiency and reducing cost and size. However, despite these benefits, this architecture faces a significant drawback known as

Table 2.4.: Comparison of VE and true MPPT.

Features	**VE**		**True MPPT**
	[7, 113]	[111, 112]	
Control	Open loop	Closed loop	Closed loop
Dynamic Performance	Quick	Medium	Slow
Complexity	Low	Medium	High
Impact on Reliability	No	Low	High
Cost	Low	Medium	High
Type of Loss	Mismatch losses	Mismatch & sensors losses	Sensors losses
Steady-state perturbation oscillation	No	No	Yes
Ability to limit processed power	No	Yes	Yes

the accumulation effect (Fig. 2.13(a)). This effect arises from power transfer occurring exclusively between adjacent PV modules, causing the MICs to process the same power multiple times as it is transferred from unshaded to shaded modules. This effect is exacerbated in longer PV strings, resulting in increased power ratings, losses, and costly MICs [110, 114].

Controlling a PV string with N PV modules requires defining N objectives, necessitating at least N actuators. In PV2PV, with $N-1$ MICs serving as actuators, an additional actuator is required. The central converter can serve as the N^{th} actuator, tracking the maximum power point of the N^{th} PV module. In the PV2PV SDPP architecture, two main MIC topologies are commonly utilized: switched-inductor [111, 112, 115–117] and resonant switched-capacitor [118–120]. The switched-inductor architecture, shown in Fig. 2.13(b), comprises two switches, one inductor, and two capacitors. In PV2PV SDPP architectures with switched-inductor topologies, when employing the VE technique for MPPT, the duty cycle of the switches must be set to 0.5, achievable without additional control mechanisms. A closed-loop controller adjusts the duty cycle for true MPP based on the PV module voltages.

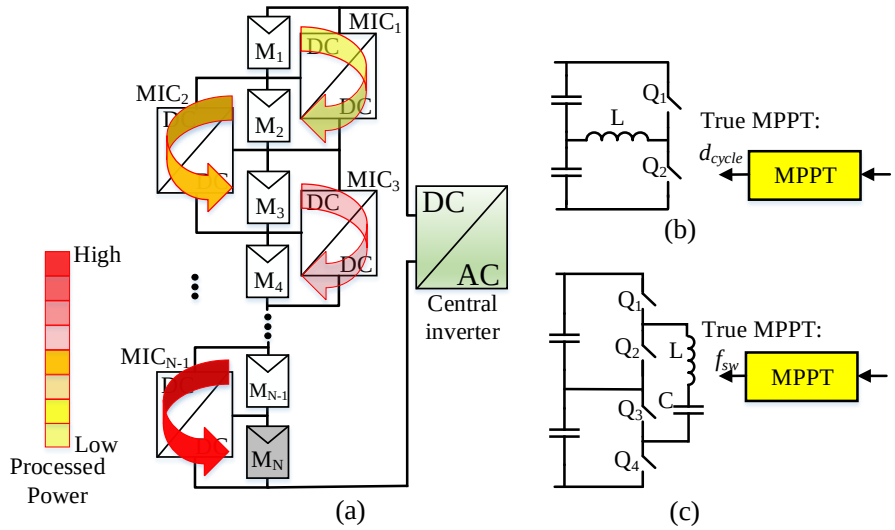

Figure 2.13.: PV2PV SDPP architecture with N PV modules. (a) Accumulation effect on MICs power processing in PV2PV SDPP with N PV modules (PV module M_N is shaded whereas the others are unshaded). (b) Switched-inductor and (c) resonant switched-capacitor MICs.

Given the widespread adoption of switched-inductor topologies, various approaches have been proposed to achieve MPPT. Starting with the centralized approach [112], it does not require local sensors but necessitates communication with the central control unit. In this method, 2^N duty ratio perturbations are required during each tracking step to locate the MPP. This becomes less practical for long PV strings due to the high number of perturbations per step, potentially leading to slower MPP tracking. Moreover, failures of the control unit or communication links could lead to malfunctions at best and complete system faults at worst. This limitation impacts the reliability of such an approach.

In [111], a distributed algorithm that relies solely on neighbor-to-neighbor communication between adjacent MICs is proposed to achieve true MPPT at the submodule level. This approach eliminates the need for a central control unit and local current sensors, enhancing reliability by removing the single point of failure. Although only N duty ratio perturbations are needed per DPP tracking step, the tracking process is slower with longer PV strings. [117] introduces a Multilevel DMPPT control for DPP-based systems, which is claimed to converge in less than

20 perturbations regardless of PV string length, improving algorithm speed. Although it reduces communication requirements compared to [112], synchronization between power converters is necessary, and local current sensing is still needed for the first MIC. Another strategy suggested in [116] is a flexible double-stage time-sharing MPPT control, ideal for SMICs, where the MIC acts as the central controller. This approach eliminates the need for communication but requires central current and voltage sensors and additional sensors in two out of three PV submodules, leading to extra costs and losses. Additionally, [121] presents a solution achieving fast transient response and accurate steady-state MPP without requiring communication between converters or distributed current sensing. However, it relies on optical cameras per PV module to estimate irradiances. Table 2.5 compares these true MPP approaches with VE.

In both LSCC [122–124] and DSCC [125, 126] topologies (depicted in Fig. 2.14(b) and Fig. 2.14(c)), a set of $2 \cdot N$ switches and $N-1$ capacitors in addition to the capacitors in parallel with PV modules are employed. These topologies operate with a fixed 50% duty cycle in a complementary manner. In LSCC, the voltage ratings of switches and capacitors match that of a single PV module, allowing for easy extension of the ladder structure by adding new rungs. This modularity aids the rapid extension of the PV string by connecting additional PV modules. However, similar to other PV2PV SDPPs, LSCC suffers from accumulation effects. To tackle this issue, DSCC is introduced, where all capacitors are connected to a common node, enabling direct power transfer between any two PV modules through two capacitors. This direct power transfer enhances efficiency but results in higher voltage stresses on capacitors, which escalate with the number of PV modules [125, 126].

A combination of switched-inductor and switched-capacitor MICs, as depicted in Fig. 2.15, is proposed by [127, 128]. In [127], switched-inductor MICs are employed for VE in a downward path, while switched-capacitor converters facilitate power transfer in an upward path. In [128], the proposed architecture combines switched-inductor and switched-capacitor MICs to form a VE. The operating principle of the VE can be categorized into two parts: (i) Charging and discharging of the inductor, similar to the switched-inductor MICs, and (ii) Charging and discharging of the capacitor, similar to the switched-capacitor MICs. While [128] reports high efficiency and reduced switch count, the solution lacks modularity.

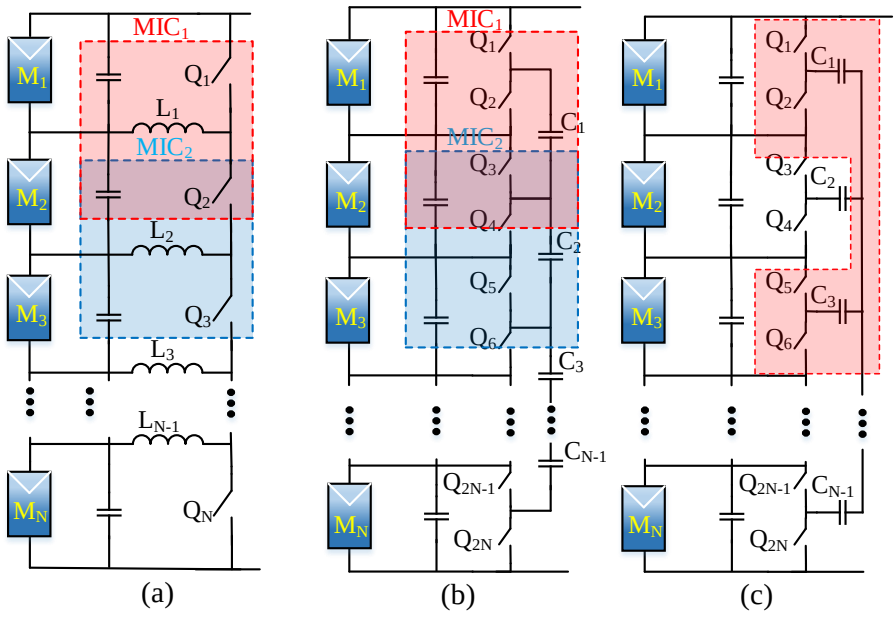

Figure 2.14.: PV2PV SDPP architecture with (a) MSBB, (b) LSCC, and (c) DSCC Converter as MICs.

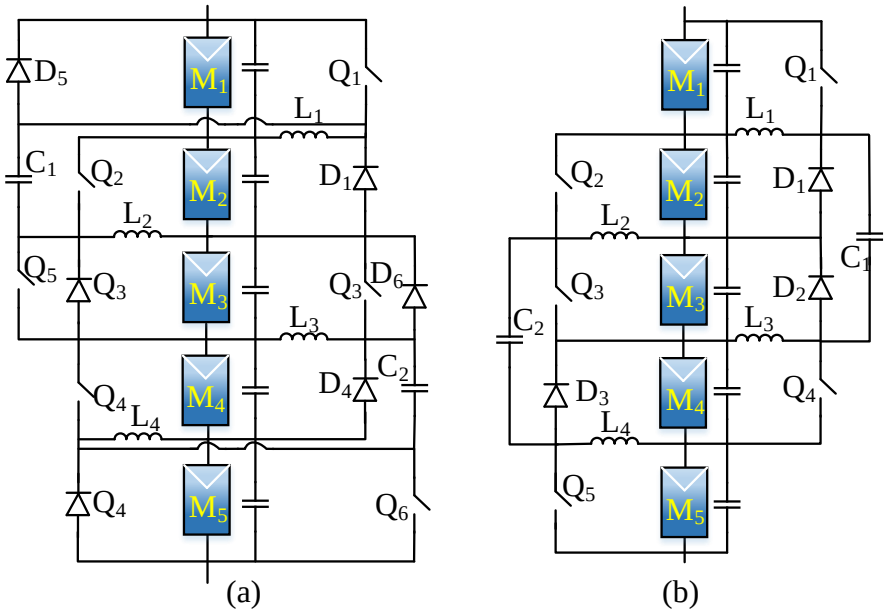

Figure 2.15.: Combination of switched-inductor and switched-capacitor MICs proposed by (a) [127], and (b) [128].

Table 2.5.: Comparison of DPP control approaches for the bidirectional switched-inductor topology in PV2PV SDPP architecture.

Features	**VE**	**Centralized [112]**	**Neighbour to Neighbour [111]**	**Time-sharing [116]**	**Multilevel MPPT [117]**	**Image-Based[121]**
Tracking	Near MPP	true MPP	true MPP	true MPP	true MPP	true MPP
Distributed algorithm	No	No	Yes	Yes	Yes	Yes
Local current/voltage sensors	No/No	No/No	No/Yes	Yes*/Yes	No**/Yes	No/Yes
Central current/voltage sensors	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes	No/No
Requiring communication	No	Yes	Yes	No	Yes	No
Algorithm tracking speed	Fastest	Slow	Slow	Slow	Medium	Fast
Steady-State Oscillation	No	Yes	Yes	Yes	Yes	No

** Some of the (S)MICs require local sensing*
*** Only the first MIC requires current sensing.*

PV2B

In the PV2B SDPP architecture, illustrated in Fig. 2.16, SDPP MIC's primaries are connected to a DC Bus, which can be either the input or output of the central converter DC-DC stage. This architecture allows N MICs and an SLC to act as actuators for a string of N PV modules, offering a degree of freedom in architecture control to reduce converter size and cost. To effectively utilize this degree of freedom, the architecture must feature bidirectional MICs. This allows some MICs to transfer power from PV to the bus, while others transfer power in the opposite direction at the optimal point [3, 7, 8, 129–131].

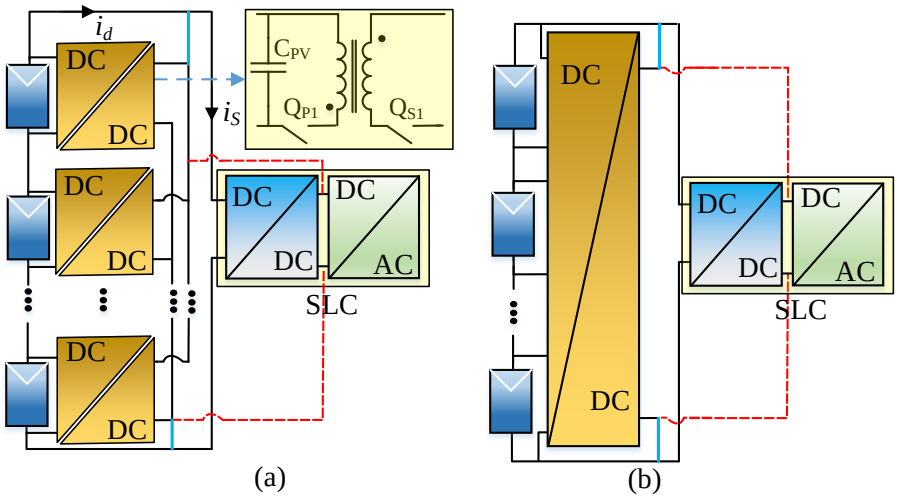

Figure 2.16.: PV2B SDPP (a) MIMO with an exemplary flyback MIC topology, and (b) MISO architectures. SDPP MICs' primary can be connected either to the input (blue continuous lines) or to the output (dashed red lines) of the DC-DC stage of the SLC.

Regarding the connection of MICs primaries, two approaches are common: direct connection to the input of the SLC's DC-DC stage [132–140] or the output of the SLC's DC-DC stage [3, 7, 129–131]. The former ties the PV string's current (i_S) to the PV modules' current, limiting the utilization of the SLC's additional degree of freedom. To utilize this degree of freedom, in [8], the output current flowing from PV modules (i_d in Fig. 2.16(a)) is controlled. The latter offers the advantage of decoupling PV modules and PV string currents, enhancing control flexibility [141]. Yet, connecting to the SLC's output results in

higher voltage requirements for the MIC components due to the typically elevated voltage level at the output of the DC-DC stage of the SLC compared to its input.

Generally, two main PV2B SDPP architectures exist: Multi-input–multi-output (MIMO) and Multi-input–single-output (MISO). MIMO requires isolated MICs to prevent short-circuiting PV modules during operation. A potential MIC topology for MIMO is the dual active full-bridge, albeit complex due to many switches. Alternatively, flyback converters, known for high voltage gain, simplicity, and galvanic isolation, are suitable. Both unidirectional [132, 142] and bidirectional [3, 7, 129–131] flyback MICs have been reported for MIMO PV2B SDPP architectures. For the latter, some control approaches divided into two levels, DMPPT and central controller, have been proposed. DMPPT, managed by the MICs, tracks the MPP of each PV module, while the central controller adjusts the PV string current for overall power optimization [3, 7, 129–131].

In the least power point tracking (LPPT) method [129, 131], the central controller aims to minimize total power processing by setting the PV string current. This technique employs independent MPPT control for each PV module, but it faces issues such as uneven power distribution in DPP converters and steady-state oscillations. The unit-minimum LPPT control [130] addresses the former problem by distributing power evenly among the converters, albeit still exhibiting steady-state oscillations. A hybrid control approach combining LPPT and power rating balancing based on VE has been proposed to mitigate oscillations [7]. However, it falls short of achieving true MPP operation of the PV modules. An improved power-rating balance control technique ensures true DMPPT using finite-state-machine-based MPPT while also providing power rating balancing but increasing complexity [3]. Moreover, a distributed digital controller has been developed to achieve DMMPT for unidirectional flyback MICs [132], but it sacrifices optimal power processing. Table 2.6 compares various MIMO PV2B SDPP architecture control techniques.

Table 2.6.: Comparison of MIMO PV2B SDPP Architectures control techniques with Bidirectional Flyback topology.

Features	**Hybrid control [7]**	**Least power point tracking [8, 129]**	**Direct power point tracking [131]**	**Unit-least power point tracking [130]**	**Improved power rating balance [3]**	**Distributed Coordination [132]**
Module level tracking	Near MPP	True MPP	True MPP	True MPP	True MPP	True MPP
Power distribution among MICs	Even	Uneven	Uneven	Even	Even	Uneven
Local current/ voltage sensing	Yes/No	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes
Central current/ voltage sensing	Yes/No	Yes/No	Yes/No	Yes/No	Yes/No	—-
Algorithm tracking speed (Module/ System level)	Fast/Fast	Slow/Medium	Medium/Fast	Slow/Medium	Medium/Fast	Fast/Fast
Interfacing between algorithms at (modules and system)	No	Yes	Yes	Yes	No	Yes
Steady-state oscillations (Module/ System level)	No/No	Yes/Yes	Yes/No	Yes/Yes	No/No	Yes/—

** This reference used unidirectional flyback topology in the architecture.*

Fig. 2.17 shows several potential MIC topologies for MISO PV2B SDPP. Examples include multi-winding transformer flyback [140], multi-stacked topologies [133, 134], and resonant-based topologies [136–139]. Literature also reported the multi-winding transformer active full-bridge [143]. While the multi-winding flyback and active full-bridge exhibit fewer switches than their MIMO counterparts, they require a multi-winding transformer, complicating implementation and scalability. In the multi-stack topology, MICs utilizing two inductors like SEPIC, Zeta, and isolated Ćuk are applicable [133, 134]. However, the Zeta-based topology necessitates a floating gate driver, and the Ćuk-based one is unfeasible without a transformer, favouring the SEPIC-based option. For resonant-based topologies, two-switch [135, 136] or four-switch [137]voltage equalizers using a resonant converter and voltage multiplier have been proposed, offering simplified architectures but suffering from limitations such as the inability to work with true MPPT algorithms, unidirectional power flow, component rating dependence on position in the PV string, and poor scalability.

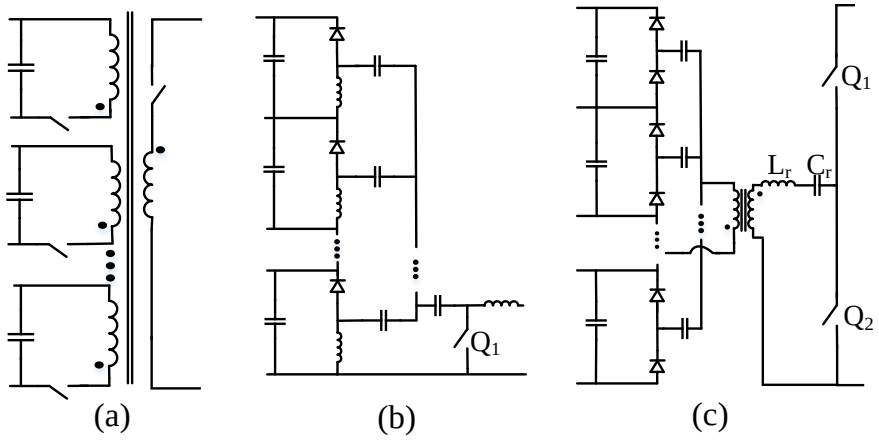

Figure 2.17.: Possible MIC's topologies for MISO PV2B SDPP. (a) Multi-winding transformer flyback, (b) Multi-stacked, and (c) Resonant-based topologies.

Unlike PV2PV architectures, PV2B avoids the accumulation effect, ensuring that MICs' maximum power ratings remain below the PV module's MPP, even in worst-case scenarios. Yet, the primary challenges in PV2B SDPP architectures revolve around high voltage step-up ratios required by MICs, posing hurdles in designing efficient and cost-effective MICs. Additionally, components on the MICs' DC Bus side face

heightened voltage stress, leading to increased power losses and costs. Moreover, scalability is limited as expanding the system with more PV modules necessitates MIC redesign. A solution to mitigate these challenges is the segmented PV2B SDPP structure [144].

PV2VB

In the PV2VB SDPP architecture, the MICs primaries and secondaries are connected to a common virtual bus and PV modules, respectively, as shown in Fig. 2.18 In this architecture, MICs connected to PV modules with high power generation inject power into the virtual bus while the others draw power. The virtual bus incorporates either capacitive or inductive storage elements. In capacitive PV2VB architectures (Fig. 2.18 (a)), bidirectional current and isolated MICs are essential to manage power flow and prevent short-circuiting among PV modules. In a PV string with N PV modules, N+1 actuators consisting of N MICs and one SLC exist; the latter enables regulation of the virtual bus voltage to maintain the power balance and stabilize its voltage, whereas the N MICs track the MPP of the N PV modules. Therefore, unlike PV2B architectures, PV2VB architectures lack extra freedom for power optimization. Moreover, capacitive PV2VB systems require high-energy storage capacity to mitigate voltage fluctuations, necessitating high-capacitance capacitors. However, PV2VB offers advantages over PV2B, such as setting an appropriate voltage for the virtual bus independently of PV module characteristics. Besides, unlike PV2PV, PV2VB architectures are unaffected by the accumulation effect. Consequently, the maximum required MICs power rating in the worst-case scenario aligns with PV2B counterpart [144]. In PV2VB SDPP architectures, bidirectional isolated MICs are required [2, 113, 145–148], and bidirectional flyback topologies are commonly preferred due to their noted advantages.

Various control strategies have been explored in the literature to achieve both VE and True MPP using flyback topologies. In one approach [113], VE with open-loop control is implemented for each SDPP converter, employing bidirectional flyback topologies with a HFT ratio of 1. Moreover, a near MPPT closed-loop control approach is introduced in another study [145], where the current flow in the MICs is regulated based on the voltage error between the primary side (PV modules) and secondary side (virtual bus) voltage with a DC gain ($i_{\text{pri}} = K(V_{\text{VB}} - V_{\text{PVi}})$). In [2], authors emphasize the importance of the DC gain for proper balancing and efficiency of MPP tracking. A similar closed-loop control strategy is proposed by [146], where the switch duty cycle is adjusted proportionally to the voltage difference between the PV modules and the virtual bus ($D_{\text{pri}} = K(V_{\text{VB}} - V_{\text{PVi}})$). Additionally, [147] suggests a distributed asynchronous algorithm to achieve True MPP, reducing cross-coupling effects among MICs with a sufficiently large bus capacitance. In [147], an approach in which an inner loop

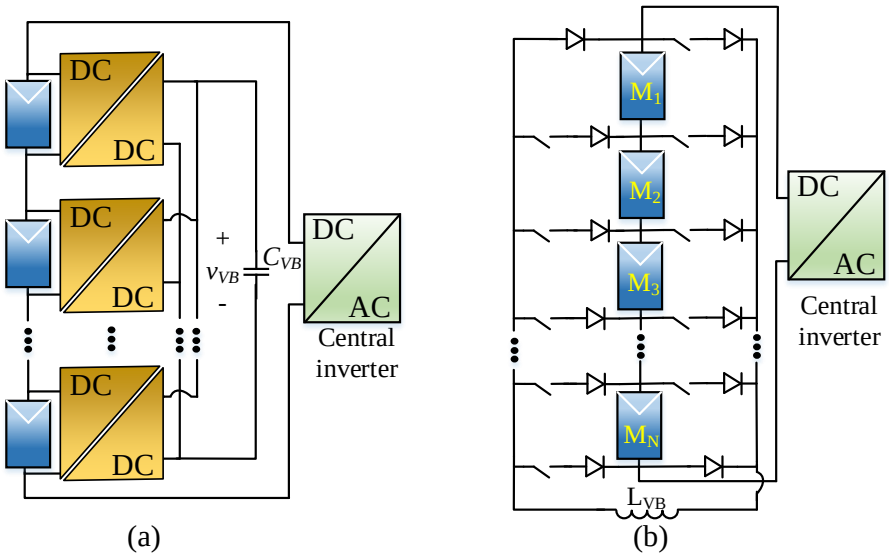

Figure 2.18.: PV2VB SDPP architecture with (a) capacitive virtual bus or (b) inductive virtual bus with corresponding appropriate MICs.

tracks the MPP of PV submodules by adjusting the operation of the MICs. In contrast, a proposed outer loop regulates the virtual bus voltage over a slower perturbation period. In all these control approaches [113, 145–147], maintaining the average power of the virtual bus at zero is crucial for achieving a constant virtual bus voltage and stable operation. A comparison among capacitive PV2VB SDPP control techniques is presented in Table 2.7. The inductive PV2VB architecture proposed in [149–151](Fig. 2.18 (b)) offers an alternative approach to capacitive PV2VB architectures. Here, unshaded PV modules charge an inductor, redistributing stored energy to support shaded PV modules by connecting them in parallel. This method allows all PV modules to operate at their MPP by providing an alternative path for excess MPP current. By replacing capacitors with inductors at the virtual bus, this architecture helps to enhance reliability. Additionally, it eliminates the need for HFTs, thereby improving both the cost-effectiveness and efficiency of the MICs. However, implementing this architecture requires highly complex control algorithms to manage switching strategies, set duty cycles, and detect shadows. In some instances, optimizing the switching architecture may be time-consuming, leading to challenges adapting to rapidly changing mismatch conditions. Moreover, the

inductor’s size depends on the length of the PV string, and the presence of diodes at both ends of the PV string can hinder scalability.

Table 2.7.: Comparison of control approaches for capacitive PV2VB SDPP Architectures with Bidirectional Flyback topology.

Features	**VE [113]**	**$i_{pri} = K \cdot (V_{VB}\text{-}V_{PVi})$ [145]**	**$D_{pri} = K \cdot (V_{VB}\text{-}V_{PVi})$ [146]**	**Distributed asynchronous MPPT [147]**
MPPT	Near MPP	Near MPP	Near MPP	True MPP
Local current/ voltage sensor	No/No	No/Yes	No/Yes	Yes/Yes
Central current/ voltage sensor	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes
Steady state perturbation oscillation*	No	No	No	Yes
Communication requirement	No	No	No	No
Algorithm tracking speed	Fast	Fast	Fast	Slow
Capacitance of Virtual Bus per SMIC	2200 uF	40 uF	66 uF	17 mF

** Here, only the oscillation arising from DMPPT controllers is considered. Any possible oscillations due to the central controller are not accounted for.*

A summary outlining the primary advantages and challenges of various SDPP architectures is presented in Table 2.8. In [2, 110], it is shown that even when considering 98% efficiency for DC-FPP converters and 90% efficiency for SDPP converters, the PV2PV, PV2B, and PV2VB architectures exhibit efficiency improvements of 0.3%, 1.6%, and 1.3%, respectively, over their FPP architecture counterparts. Furthermore, these efficiency gains are achieved while the power ratings of SDPP converters in PV2PV, PV2B, and PV2VB are 33%, 16%, and 33% of those of the DC-FPP converters. These results demonstrate the potential for reducing initial costs and improving the LCOE of PV systems through SDPP architectures.

Table 2.8.: Comparison of SDPP Architectures

Architecture	Advantages	Challenges
PV-PV [111, 112, 116, 117, 121]	1. Voltage rating depends only on PV module's voltage. 2. Allows using non-isolated converter topologies. 3. High efficiency and compact MICs.	1. Accumulation effect. 2. Cross-coupling effect.
PV2B (Bidirectional) [3, 7, 8, 129–131]	1. Extra degree of freedom to optimize size, cost, and losses. 2. No accumulation effect. 3. Low current at the MICs' DC Bus.	1. Complex converter topologies. 2. Requires high voltage gain. 3. Voltage rating depends on Bus voltage. 4. Poor scalability. 5. Cross-coupling effect.
PV2B (Unidirectional) [132–137]	1. Simpler topologies compared to Bidirectional counterpart. 2. No accumulation effect. 3. Low current at the MICs' DC Bus.	1. Unable to optimize overall power processing. 2. Requires high voltage gain. 3. Voltage rating depends on Bus voltage. 4. Poor scalability. 5. Cross-coupling effect.
PV2VB (Capacitive VB) [113, 145–147]	1. Lower component voltage rating compared to PV2B. 2. Lower power processing than PV2PV architecture (in long PV strings).	1. Requires isolated converters. 2. High-capacitance capacitors are required in Virtual Bus. 3. Cross-coupling effect.
PV2VB (Inductive VB) [149–151]	1. High reliability. 2. Allows using a non-isolated converter.	1. Complex controller. 2. Unable to cope with fast-changing mismatch conditions. 3. Cross-coupling effect.

2.4.2. PDPP

In a PV system, each PV group must operate under the same voltage when connected in parallel. However, varying operating conditions may lead to different MPP voltages, making it impossible to reach all PV groups' MPP simultaneously. As shown in Fig. 2.12 (b), PDPP architectures provide the required differential voltage between PV groups and a common bus to eliminate mismatch losses among parallel-connected PV groups. Since parallel connections suffer lower power losses due to mismatches compared to series connections, limited literature is available about PDPP, especially compared to SDPP. Nonetheless, PDPP architectures offer promising advantages over traditional FPP SLCs. They typically require lower component ratings, resulting in reduced system costs, and operate with lower primary-side voltages or secondary-side currents, thereby enhancing system efficiency [20]. It's important to note that PV string current passes through DPP converters in PDPP architectures, resulting in conduction losses even under uniform operating conditions.

Although PDPP can be implemented at various granularity levels, it is primarily associated with the SLC. The literature has introduced PV2B and, in this dissertation, PV2VB PDPP architectures; however, PV2PV architectures remain unexplored. The advantages and disadvantages of PDPP architectures closely resemble those of their SDPP counterparts. Chapter 3 will provide a concise overview of PDPP.

2.4.3. SPDPP

SDPP strings cannot be paralleled effectively due to voltage mismatch issues, reducing power production. One solution is connecting each SDPP string to a separate FPP SLC, which adds losses and cost to the system [7, 152]. Similarly, PDPP architectures face challenges in effectively connecting PV modules in series due to current mismatch issues. An emerging solution to these challenges is the SPDPP architecture, depicted in Fig. 2.19. SPDPP allows optimal power extraction from a PV array under mismatch conditions while ensuring that MICs and SLCs process only a fraction of the total power. Despite being relatively underexplored, the SPDPP concept holds promise for high-power PV systems with enhanced efficiency. Various architectures can be implemented within the SPDPP framework, for example, combining PV2PV SDPP and PV2B PDPP converters to achieve an SPDPP architecture, as demonstrated in [153, 154].

A distinct SPDPP topology, based on a modular DPP concept, has been presented in [21, 155, 156] (Fig. 2.20). This architecture enhances modularity and scalability by utilizing switched inductors in all SPDPP MICs and SLCs. However, the component ratings of the SLCs differ from those of the MICs [21]. In this architecture, PV2PV SDPP MICs are

deployed to mitigate mismatches among series-connected PV modules. At the same time, the inputs of the SLCs are connected to one of the PV modules to allow for parallel connection of PV strings. The top converter (SLC) handles the full string current and the differential voltages between the PV and bus voltage in parallel strings. Meanwhile, all other converters (MICs) manage the differential currents between the series PV modules. Moreover, to diminish cross-coupling effects among the PV modules, a novel control strategy employing a voltage inner loop and a power outer loop has been proposed for tracking the PV modules' MPP [21, 155].

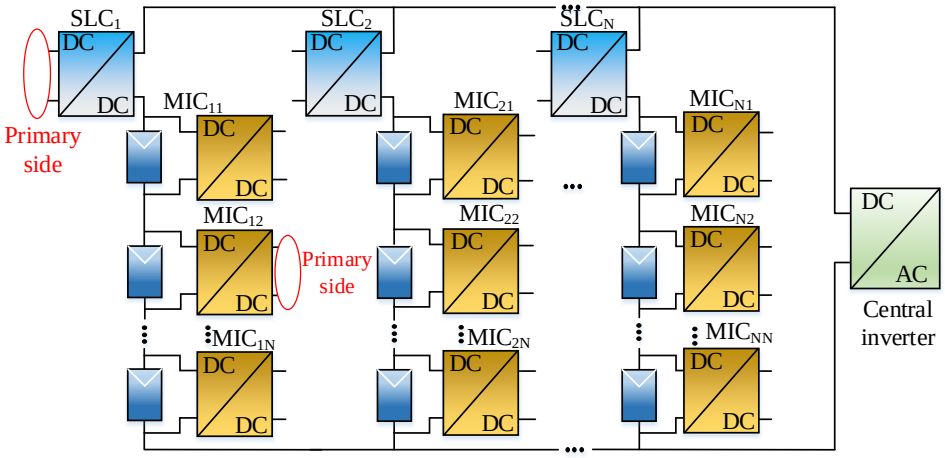

Figure 2.19.: SPDPP architecture

2.5. HYBRID & HIERARCHICAL DMPPT ARCHITECTURE

DMPPT operates at various levels within PV systems, each with unique requirements. For instance, the number of PV modules per PV string can vary based on the application, while PV modules typically consist of three fixed PV submodules. Hence, modularity and scalability are often desired at the module level rather than the submodule level. Another crucial distinction among different levels is their power and voltage ratings, resulting in varying rated voltages for SMICs, MICs, and SLCs components. These distinctions can be leveraged to devise hybrid and hierarchical DMPPT architectures that operate at different levels, streamlining the design and operation of PV systems.

Sections III and IV have provided detailed insights into various DMPPT techniques, each presenting distinct advantages and challenges. For instance, microinverters exhibit immunity to cross-coupling effects and

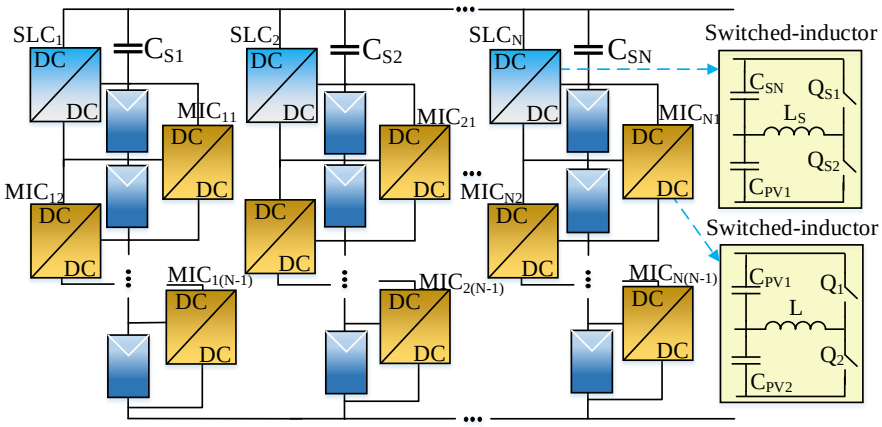

Figure 2.20.: Modular SPDPP architecture

offer robustness against MIC and PV module failures. However, they necessitate high-gain converters, with the required gain escalating as granularity increases, particularly at the submodule or cell level. Conversely, PV2PV SDPPs are more suitable when the number of PV groups is low due to the accumulation effect, such as at the level of PV submodules. To leverage the strengths of both approaches, a hybrid solution is proposed that integrates PV2PV SDPP architectures with switch inductance topology as SMICs. This architecture aims to reduce mismatch-related losses at the submodule level while incorporating microinverters as MICs to enhance modularity within the PV system (Fig. 2.21(a)) [116, 157].

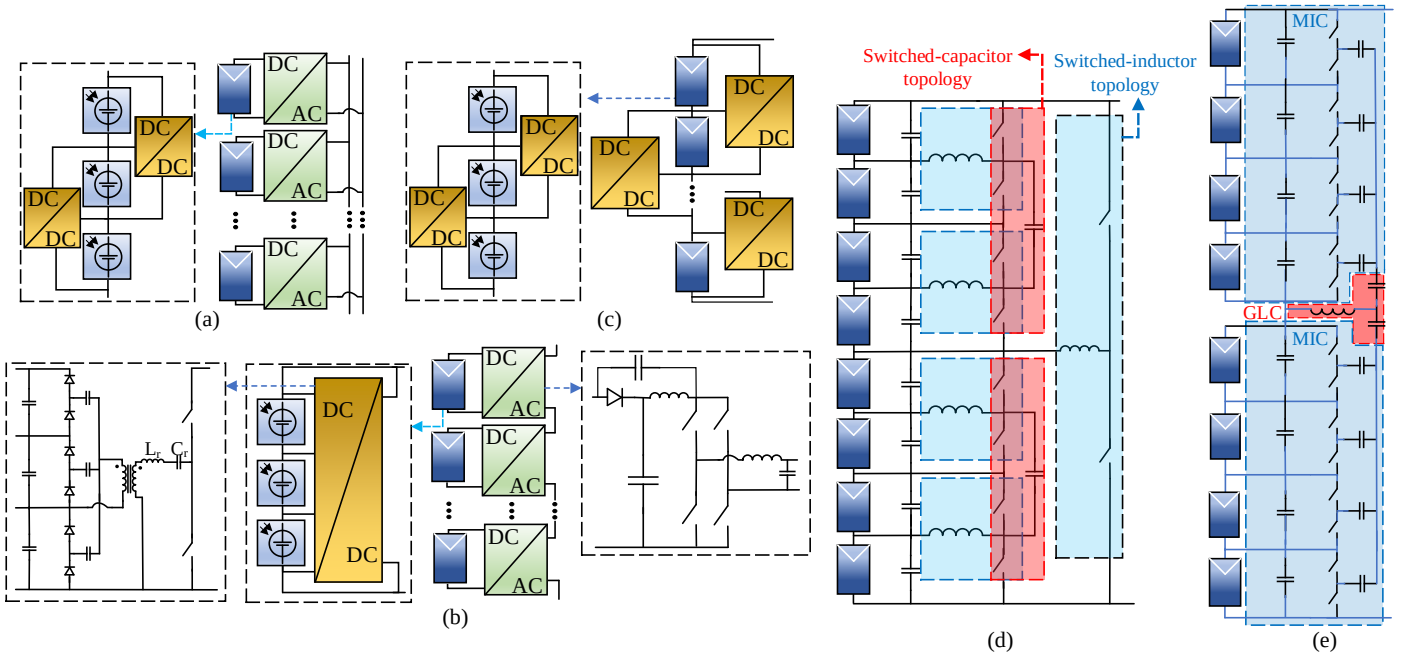

Figure 2.21.: Combination of different DMPPT techniques at different hierarchies (a) PV2PV with microinverter, (b) PV2B with MMCI, (c) PV2PV with PV2PV, hierarchies architecture proposed (d) by [22] ,and (e) [125, 126]

In architectures where PV2B SDPPs are employed as SMICs, connected directly to the PV string, challenges associated with high voltage PV string emerge. Addressing these challenges, a recent study proposed a novel approach combining MMCIs with PV2B SDPP (Fig. 2.21(b)) [158]. In this architecture, PV2B SDPPs function as SMICs, while MMCI serves as MICs, facilitating power injection into the grid. Each SDPP output is connected to an inverter cell within the MMCI. This innovative architecture mitigates the demand for high voltage gain and the need for components with elevated voltage ratings.

In [159], an architecture resembling PV2PV SDPPs is proposed, operating at both module and submodule levels (Fig. 2.21(c)). This architecture aims to alleviate accumulation effects inherent in conventional PV2PV SDPP approaches for two primary reasons. Firstly, MICs handle differential power among PV modules, while SMICs manage that of PV submodules. Additionally, SMICs associated with different PV modules operate independently, reducing overall power processing and converter ratings.

In [22], a hierarchical architecture is proposed, utilizing PV2PV SDPP switched-inductor topologies in combination with resonant switched-capacitor concepts, shown in Fig. 2.21(d). This architecture connects PV groups at different hierarchies, reducing the number of switches by sharing them between adjacent levels. However, a key limitation is its applicability only when the number of PV groups is a power of 2, leading to constraints on scalability. Moreover, varying voltage ratings across hierarchies diminish modularity, posing component selection and system design challenges.

In [125, 126], a hierarchical DMPPT approach is introduced utilizing various SDPP architectures at different levels. At the submodule level, SDPP is employed, while PV2PV SDPP architecture with DSCC MICs is used for groups of four PV modules. These groups are interconnected using either a switchless group-level converter (GLC) SDPP [125] or a modular SDPP [126] architecture (Fig. 2.21(e)).

The hierarchical DMPPT approach is innovative and offers distinct advantages, indicating significant potential for future research to delve deeper into its capabilities and applications.

2.6. SUMMARY AND FUTURE DIRECTIONS

2.6.1. SUMMARY

This chapter classifies, reviews, and compares the various state-of-the-art DMPPT architectures for PV applications, which can be applied with different levels of granularity, from string-level DMPPT down to module-, submodule-, and cell-level. In modern and customized PV systems for integration in both urban and open environments, a highly granular control of PV (sub)modules—when economically feasible—is inherently

able to minimize the effect of any non-uniformity and maximize the system's energy yield. Highly granular control is not only beneficial for those sources of non-uniformity related to the position of the sun or to the geometry of the surroundings but also to other conditions, such as fouling, soiling, and uneven degradation. Some studies [160, 161] indicate that microinverters achieve a more favorable LCOE, while other [162] suggests that string inverters can provide a lower LCOE. Generally, microinverters tend to perform better in complex or shaded environments, whereas string inverters may offer a more advantageous LCOE in simpler installations with uniform illumination over the PV modules. Fig. 2.22 (a) compares DMPTT at the string level with module-level architectures. Therefore, selecting the best-suited architecture and the required level of granularity depends strongly on the application, the characteristics of the PV system, and its expected operating conditions.

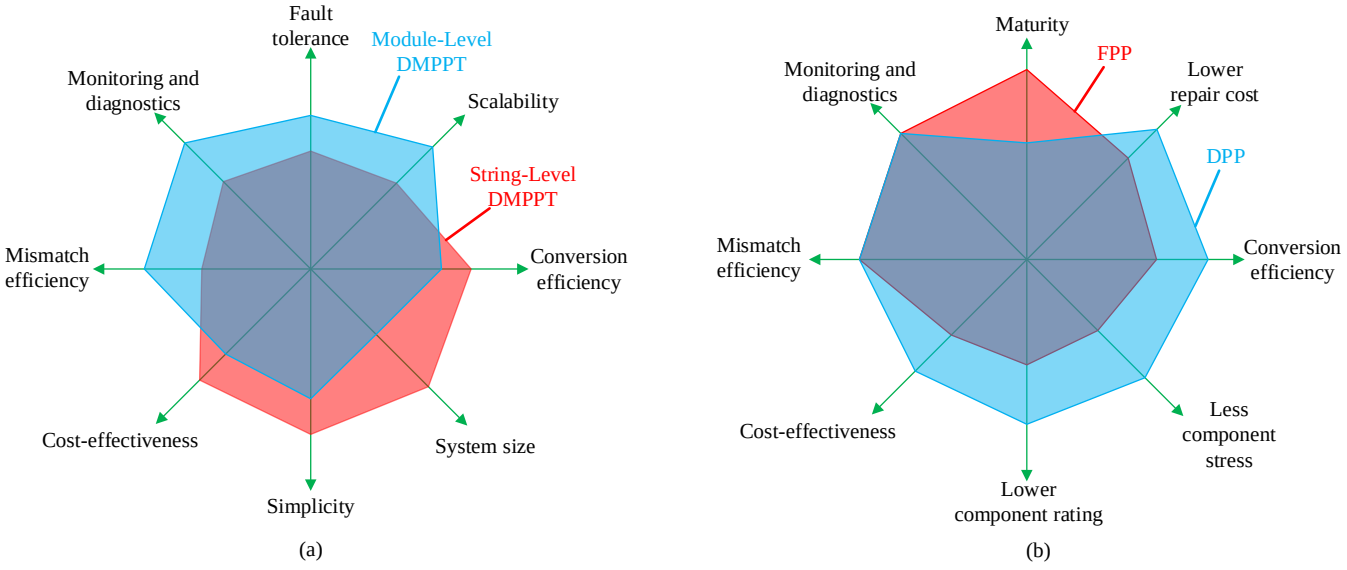

Figure 2.22.: Comparison between (a) module-level MPPT and string-level MPPT (b) FPP and DPP.

The lower level of granularity of DMPPT is the string level, in which typically string/multi-string inverters are used to control the different PV strings within a PV system independently. Like the centralized MPPT through central inverters, string-level DMPPT architectures offer advantages such as low complexity, cost-effectiveness, and high system efficiency in open environments when non-uniformities within the PV system arise mostly among different PV strings. In contrast, each string is subject to (quasi-)uniform conditions. One example of such an application is east-west-oriented PV systems installed in an open environment, which does not cast dynamic shades over the PV systems most of the day.

The efficiency of string-level DMPPT architectures significantly decreases in environments like building-integrated PV systems, where different PV modules in a PV string are subject to different operating conditions, e.g., due to substantial dynamic partial shading. Similarly, in vehicle-integrated PV applications, non-uniformities within small groups of cells may arise owing to (i) curvature of the modules, (ii) different locations of cells on the vehicle surface, (iii) movement of the vehicle and corresponding changes in the irradiation of the various cells due both the variation of the relative position of the cell with respect to the sun and dynamic shading from the varying surroundings. To increase system efficiency, the granularity of DMPPT must be increased, and module- or submodule-level architectures are preferable. MICs and SMICs have gained significant attention in the last decades to increase the energy yield in these applications. They mitigate mismatch-related losses and offer enhanced protection, monitoring capabilities, modularity, scalability, and simplification of the MPPT algorithm.

DMPPT architectures at the module and submodule levels are classified into two main categories: FPP and DPP. Focusing on FPP solutions, microinverters, and parallel DC-FPP architectures, which rely on the parallel connection of the converters' output either to the AC grid (microinverters) or to a common bus/DC grid (parallel DC-FPP), offer independent tracking of the MPP of each module without cross-coupling effects, remarkable resilience to failure, high flexibility, modularity, scalability, plug-and-play functionality, and high availability. These features make them suitable for applications in which PV modules are often subject to non-uniform conditions and high availability and low installation costs are crucial (see Table 2.3). On the other hand, the converters' output can be connected in series. The corresponding AC-FPP architectures are based on MMCIs, which generate multilevel output voltages, enabling low switching frequency, small AC filter size, and low electromagnetic interference. MMCIs are highly desirable in AC applications where high efficiency and power quality are critical (see Table 2.3). Their ability to reduce harmonic distortion, improve efficiency, and handle higher voltage levels makes them suitable

for various PV system applications, from utility-scale installations to residential and industrial uses. In applications where the PV system is connected to a common bus or a DC grid, series DC-FPP systems offer higher efficiency and cost-effectiveness than their parallel counterparts, eliminating the need for high step-up voltage converters. However, both MMCIs and series DC-FPP architectures require series-connection of the converters' output, which results in cross-coupling effects and may require more complex controllers (see Table 2.3).

As an alternative DMPPT approach, DPP architectures have attracted attention due to their ability to reduce power conversion losses, size, and cost of converters. DPP architectures are primarily divided into three groups: (i) SDPP, (ii) PDPP, and (iii) SPDPP. In DPP-based architectures, SDPP can only mitigate mismatches among series-connected PV groups. The advantages of SDPP PV2PV architecture include low voltage rating and the use of non-isolated MICs, which lead to improved efficiency and reduced cost and size. However, this architecture suffers from the so-called accumulation effect, making it undesirable for long PV strings. Yet, it may suit well PV wearable applications with low power and short PV strings. Unlike SDPP PV2PV architectures, PV2B avoids the accumulation effect but requires a high voltage rating and isolated MICs. PV2VB architecture can eliminate the accumulation effect using low voltage rating MICs, but it still requires isolated converters and extra components, mostly capacitors, at the virtual bus (see Table 2.8). On the other hand, PDPP architectures can only mitigate mismatch among PV groups connected in parallel, like string/multi-string inverters. PDPP architectures, especially PV2VB, need lower voltage SLCs and offer superior scalability, facilitating mass production compared to conventional counterparts. These features make them a suitable alternative for applications where string/multi-string inverters are typically used. SPDPP, combining the features of SDPP and PDPP, allows for optimal power extraction from PV groups connected in either series or parallel under mismatch conditions. This makes SPDPP more suitable for large PV systems in complex environments where partial shading occurs regularly. Fig. 2.22 (b) compares FPP with DPP architectures.

2.6.2. FUTURE DIRECTIONS AND EMERGING TRENDS

All those solar cells must be connected in an increasingly smart way, especially in cities, where dynamic shading through the day leads to a deterioration of conversion performance and, thus, of the LCOE. If some solar cells have been connected in parallel or series and if some of them are in shadow, the PV module generates less power, and that can affect performance if it happens for a long time. This can be improved by using DMPPT architectures, which react immediately

if an individual component is not working properly. The DMPPT can, therefore, increase the energy yield and consequently reduce the LCOE. While FPP architectures are established, proven technologies with a wide range of power converters available for both DC- and AC-FPP at the submodule, module, string, and array levels, DPP is still in the research phase. However, some initial industrial products have emerged, and the market for DPP solutions is anticipated to expand, catering to both mass production and mass customization of PV modules and systems.

In conclusion, a comprehensive analysis and classification of various DMPPT architectures have been provided, and their advantages and challenges have been discussed. Examining the associated converter topologies and controllers offers researchers valuable insights for future studies and aids designers in choosing the most suitable architecture candidates for their specific applications and needs. In the final analysis, the designers can quantitatively analyze LCOE among a few candidates and select the best architectures, corresponding topologies, and controls for that specific application.

REFERENCES

[1] A. Nazer, O. Isabella, and P. Manganiello. “A Comprehensive Classification of State-of-the-Art Distributed Maximum Power Point Tracking Architectures for Photovoltaic Systems”. In: *IEEE Open Journal of the Industrial Electronics Society,* "*Under Review*" (2025).

[2] C. Olalla, C. Deline, D. Clement, Y. Levron, M. Rodriguez, and D. Maksimovic. “Performance of Power-Limited Differential Power Processing Architectures in Mismatched PV Systems”. In: *IEEE Transactions on Power Electronics* 30.2 (2015), pp. 618–631.

[3] Y. Zhu *et al.* “Power-Rating Balance Control and Reliability Enhancement in Mismatched Photovoltaic Differential Power Processing Systems”. In: *IEEE Transactions on Power Electronics* 37.1 (2022), pp. 879–895.

[4] A. Amoorezaei, S. A. Khajehoddin, N. Rezaei-Hosseinabadi, and K. Moez. “A Low-Cost Cell-Level Differential Power Processing CMOS IC for Single Junction Photovoltaic Cells”. In: *IEEE Transactions on Power Electronics* 36.12 (2021), pp. 13985–14001.

[5] A. Amoorezaei, S. A. Khajehoddin, and K. Moez. “A Compact Cuk-Based Differential Power Processing IC With Integrated Magnetics and Soft-Switching Controller for Maximized Cell-Level Power Extraction”. In: *IEEE Transactions on Power Electronics* 39.4 (2024), pp. 4473–4490.

[6] D. Xu *et al.* “Coupling Analysis of Differential Power Processing-Based PV System and Its Decoupling Implementation of Synchronous MPPT Control”. In: *IEEE Transactions on Industrial Electronics* 70.7 (2023), pp. 6973–6983.

[7] G. Chu, H. Wen, Y. Hu, L. Jiang, Y. Yang, and Y. Wang. “Low-Complexity Power Balancing Point-Based Optimization for Photovoltaic Differential Power Processing”. In: *IEEE Transactions on Power Electronics* 35.10 (2020), pp. 10306–10322.

[8] A. Alenezi and H. A. Hussain. “A New Control Approach for Least Processed Power Tracking Under Mismatch Conditions in PV Systems Using Differential Power Processing”. In: *IEEE Transactions on Industry Applications* 60.1 (2024), pp. 532–543.

[9] M. Kasper, D. Bortis, and J. W. Kolar. “Classification and Comparative Evaluation of PV Panel-Integrated DC–DC Converter Concepts”. In: *IEEE Transactions on Power Electronics* 29.5 (2014), pp. 2511–2526.

[10] B. Stevanović, E. Serban, S. Cóbreces, P. Alou, M. Ordonez, and M. Vasić. “DC/DC Stage Contribution to Bus Voltage in 1000V and 1500V Grid-Connected Solar Inverters”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* (2022), pp. 1–1.

[11] A. Sangwongwanich, Y. Yang, F. Blaabjerg, and D. Sera. “Delta Power Control Strategy for Multistring Grid-Connected PV Inverters”. In: *IEEE Transactions on Industry Applications* 53.4 (2017), pp. 3862–3870.

[12] B. Karanayil, S. Ceballos, and J. Pou. “Maximum Power Point Controller for Large-Scale Photovoltaic Power Plants Using Central Inverters Under Partial Shading Conditions”. In: *IEEE Transactions on Power Electronics* 34.4 (2019), pp. 3098–3109.

[13] X. Zhu *et al.* “Effects of Nonlinear MPPT Control and PV Array on Stability Analysis for a Utility-Scale PV Energy System”. In: *IEEE Transactions on Energy Conversion* 38.3 (2023), pp. 1530–1543.

[14] N. Tak, S. K. Chattopadhyay, and C. Chakraborty. “Single-Sourced Double-Stage Multilevel Inverter for Grid-Connected Solar PV Systems”. In: *IEEE Open Journal of the Industrial Electronics Society* 3 (2022), pp. 561–581.

[15] K. Alluhaybi, I. Batarseh, and H. Hu. “Comprehensive Review and Comparison of Single-Phase Grid-Tied Photovoltaic Microinverters”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 8.2 (2020), pp. 1310–1329.

[16] A. I. Elsanabary, G. Konstantinou, S. Mekhilef, C. D. Townsend, M. Seyedmahmoudian, and A. Stojcevski. “Medium Voltage Large-Scale Grid-Connected Photovoltaic Systems Using Cascaded H-Bridge and Modular Multilevel Converters: A Review”. In: *IEEE Access* 8 (2020), pp. 223686–223699.

[17] Z. Liang, R. Guo, J. Li, and A. Q. Huang. “A High-Efficiency PV Module-Integrated DC/DC Converter for PV Energy Harvest in FREEDM Systems”. In: *IEEE Transactions on Power Electronics* 26.3 (2011), pp. 897–909.

[18] S. R. Pendem, S. Mikkili, and P. K. Bonthagorla. “PV Distributed-MPP Tracking: Total-Cross-Tied Configuration of String-Integrated-Converters to Extract the Maximum Power Under Various PSCs”. In: *IEEE Systems Journal* 14.1 (2020), pp. 1046–1057.

[19] A. Nazer, P. Manganiello, and O. Isabella. “A virtual bus parallel differential power processing configuration for photovoltaic applications”. In: *Mathematics and Computers in Simulation* 224, Part B (2024), pp. 49–62. issn: 0378-4754.

[20] H. Zhou, J. Zhao, and Y. Han. “PV Balancers: Concept, Architectures, and Realization”. In: *IEEE Transactions on Power Electronics* 30.7 (2015), pp. 3479–3487.

[21] C. Liu, Y. Zheng, and B. Lehman. “PV Panel to PV Panel Transfer Method for Modular Differential Power Processing”. In: *IEEE Transactions on Power Electronics* (2021), pp. 1–1.

[22] M. Z. Ramli and Z. Salam. “A Simple Energy Recovery Scheme to Harvest the Energy from Shaded Photovoltaic Modules During Partial Shading”. In: *IEEE Transactions on Power Electronics* 29.12 (2014), pp. 6458–6471.

[23] Ankit, S. K. Sahoo, S. Sukchai, and F. F. Yanine. “Review and comparative study of single-stage inverters for a PV system”. In: *Renewable and Sustainable Energy Reviews* 91 (2018), pp. 962–986.

[24] Y. Xia, M. Yu, X. Wang, and W. Wei. “Describing Function Method Based Power Oscillation Analysis of LCL-Filtered Single-Stage PV Generators Connected to Weak Grid”. In: *IEEE Transactions on Power Electronics* 34.9 (2019), pp. 8724–8738.

[25] F. E. Aamri *et al.* “Stability Analysis for DC-Link Voltage Controller Design in Single-Stage Single-Phase Grid-Connected PV Inverters”. In: *IEEE Journal of Photovoltaics* 13.4 (2023), pp. 580–589.

[26] J. W. Zapata, S. Kouro, G. Carrasco, H. Renaudineau, and T. A. Meynard. “Analysis of Partial Power DC–DC Converters for Two-Stage Photovoltaic Systems”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 7.1 (2019), pp. 591–603.

[27] Y. Hu, Y. Du, W. Xiao, S. Finney, and W. Cao. “DC-link voltage control strategy for reducing capacitance and total harmonic distortion in single-phase grid-connected PV inverters”. In: *IET Power Electronics* 8 (2014). 01/01.

[28] S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo. “Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technology”. In: *IEEE Industrial Electronics Magazine* 9.1 (2015), pp. 47–61.

[29] N. G. F. D. Santos, J. R. R. Zientarski, and M. L. d. S. Martins. “A Review of Series-Connected Partial Power Converters for DC–DC Applications”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* (2021), pp. 1–1.

[30] I. Vairavasundaram, V. Varadarajan, P. J. Pavankumar, R. K. Kanagavel, L. Ravi, and S. Vairavasundaram. “A Review on Small Power Rating PV Inverter Topologies and Smart PV Inverters”. In: *Electronics* 10.11 (2021).

[31] D. Kolantla, S. Mikkili, S. R. Pendem, and A. A. Desai. “Critical review on various inverter topologies for PV system architectures”. In: *IET Renewable Power Generation* 14.17 (2020), pp. 3418–3438.

[32] S. R. Pendem and S. Mikkili. “Assessment of Cross-coupling Effects in PV String-integrated-converters with P&O MPPT Algorithm Under Various Partial Shading Patterns”. In: *CSEE Journal of Power and Energy Systems* 8.4 (2022), pp. 1013–1028.

[33] O. Husev, D. Vinnikov, C. Roncero-Clemente, A. Chub, and E. Romero-Cadaval. “Single-Phase String Solar qZS-based Inverter: Example of Multi-Objective Optimization Design”. In: *IEEE Transactions on Industry Applications* 57.3 (2021), pp. 3120–3130.

[34] B. Stevanović, D. Serrano, M. Vasić, P. Alou, J. A. Oliver, and J. A. Cobos. “Highly Efficient, Full ZVS, Hybrid, Multilevel DC/DC Topology for Two-Stage Grid-Connected 1500-V PV System With Employed 900-V SiC Devices”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 7.2 (2019), pp. 811–832.

[35] A. Nazer, S. Driss, A. M. Haddadi, and S. Farhangi. “Optimal Photovoltaic Multi-String Inverter Topology Selection Based on Reliability and Cost Analysis”. In: *IEEE Transactions on Sustainable Energy* 12.2 (2021), pp. 1186–1195.

[36] C. Yu, H. Xu, C. Liu, Q. Wang, and X. Zhang. “Modeling and Analysis of Common-Mode Resonance in Multi-Parallel PV String Inverters”. In: *IEEE Transactions on Energy Conversion* 34.1 (2019), pp. 446–454.

[37] Semikron. *Power Electronics for Solar Inverters*. https://www.semikron-danfoss.com. Accessed on: 5th December 2024.

[38] Infineon. *Central inverter solutions*. https://www.infineon.com. Accessed on: 5th December 2024.

[39] M. Schweizer, T. Friedli, and J. W. Kolar. “Comparative Evaluation of Advanced Three-Phase Three-Level Inverter/Converter Topologies Against Two-Level Systems”. In: *IEEE Transactions on Industrial Electronics* 60.12 (2013), pp. 5515–5527.

[40] Infineon. *1-phase string inverter solutions*. https://www.infineon.com. Accessed on: 5th December 2024.

[41] K. S. Kumar, A. Kirubakaran, and N. Subrahmanyam. “Bidirectional Clamping-Based H5, HERIC, and H6 Transformerless Inverter Topologies With Reactive Power Capability”. In: *IEEE Transactions on Industry Applications* 56.5 (2020), pp. 5119–5128.

[42] S. Partlin. *String versus Micro – Which is the Right Choice?* https://www.sma-sunny.com. SMA2015, Accessed on: 5th December 2024.

[43] O. Khan and W. Xiao. “Review and qualitative analysis of submodule-level distributed power electronic solutions in PV power systems”. In: *Renewable and Sustainable Energy Reviews* 76 (2017), pp. 516–528.

[44] W. Mao, X. Zhang, R. Cao, F. Wang, T. Zhao, and L. Xu. “A Research on Power Line Communication Based on Parallel Resonant Coupling Technology in PV Module Monitoring”. In: *IEEE Transactions on Industrial Electronics* 65.3 (2018), pp. 2653–2662.

[45] TI. *Micro inverter, Products and reference designs*. 2024.

[46] Enphase. https://enphase.com. Accessed on: 5th December 2024.

[47] Siemens. *Product Catalog - US2:SMIINT215R60MC*. https://mall.industry.siemens.com. Accessed: 10th of March 2023.

[48] Hoymiles. https://www.hoymiles.com. Accessed on: 5th December 2024.

[49] Enfsolar. https://www.enfsolar.com. Accessed on: 5th December 2024.

[50] Solarpanelsplus. https://www.solarpanelsplus.com. Accessed on: 5th December 2024.

[51] Envertec. https://envertec.com. Accessed on: 5th December 2024.

[52] Influxgreen. http://www.influxgreen.com. Accessed on: 5th December 2024.

[53] SMA. *SMA Now Shipping Highly Anticipated Sunny Boy 240-US Micro Inverter*. https://www.sma-america.com. Accessed on: 5th December 2024.

[54] EIQEnergy. *VBoost*. http://eiqenergy.com/. Accessed on: 5th December 2024.

[55] TigoEnergy. *TS4-A-O*. https://www.tigoenergy.com. Accessed on: 5th December 2024.

[56] SolarEdge. *Power Optimizers*. https://www.solaredge.com. Accessed on: 5th December 2024.

[57] Xandex. https://xandex.com. Accessed on: 5th December 2024.

[58] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen. “A Review of Power Decoupling Techniques for Microinverters With Three Different Decoupling Capacitor Locations in PV Systems”. In: *IEEE Transactions on Power Electronics* 28.6 (2013), pp. 2711–2726. doi: 10.1109/TPEL.2012.2221482.

[59] R. Hasan, S. Mekhilef, M. Seyedmahmoudian, and B. Horan. “Grid-connected isolated PV microinverters: A review”. In: *Renewable and Sustainable Energy Reviews* 67 (2017). [Online]. Available: https://www.sciencedirect.com, pp. 1065–1080.

[60] A. Kumar and P. Sensarma. “New Switching Strategy for Single-Mode Operation of a Single-Stage Buck–Boost Inverter”. In: *IEEE Transactions on Power Electronics* 33.7 (2018), pp. 5927–5936.

[61] U. A. Khan, A. A. Khan, F. Akbar, and J. W. Park. “Single-Stage Single-Phase H6 and H8 Non-Isolated Buck-Boost Photovoltaic Inverters”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 10.4 (2022), pp. 4865–4878.

[62] A. K. Bhattacharjee and I. Batarseh. “Sinusoidally Modulated AC-Link Microinverter Based on Dual-Active-Bridge Topology”. In: *IEEE Transactions on Industry Applications* 56.1 (2020), pp. 422–435.

[63] D. Neumayr, G. C. Knabben, E. Varescon, D. Bortis, and J. W. Kolar. “Comparative Evaluation of a Full- and Partial-Power Processing Active Power Buffer for Ultracompact Single-Phase DC/AC Converter Systems”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 9.2 (2021), pp. 1994–2013.

[64] G. C. Christidis, A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis. “Investigation of Parallel Active Filters’ Limitations for Power Decoupling on Single-Stage/Single-Phase Microinverters”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 4.3 (2016), pp. 1096–1106.

[65] A. Sarikhani, M. M. Takantape, and M. Hamzeh. “A Transformerless Common-Ground Three-Switch Single-Phase Inverter for Photovoltaic Systems”. In: *IEEE Transactions on Power Electronics* 35.9 (2020), pp. 8902–8909.

[66] K. Chomsuwan, P. Prisuwanna, and V. Monyakul. “Photovoltaic grid-connected inverter using two-switch buck-boost converter”. In: *Conference Record of the Twenty-Ninth IEEE Photovoltaic Specialists Conference*. 2002, pp. 1527–1530.

[67] H. Wu, X. Tang, J. Zhao, and Y. Xing. “An Isolated Bidirectional Microinverter Based on Voltage-in-Phase PWM-Controlled Resonant Converter”. In: *IEEE Transactions on Power Electronics* 36.1 (2021), pp. 562–570.

[68] A. Bhattacharya, A. R. Paul, and K. Chatterjee. “A Coupled Inductor Based Ćuk Microinverter for Single Phase Grid Connected PV Applications”. In: *IEEE Transactions on Industry Applications* 59.1 (2023), pp. 981–993.

[69] N. E. Zakzouk, A. K. Abdelsalam, A. A. Helal, and B. W. Williams. “PV Single-Phase Grid-Connected Converter: DC-Link Voltage Sensorless Prospective”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 5.1 (2017), pp. 526–546.

[70] Y. Zhang, J. Xiong, P. He, and S. Wang. “Review of power decoupling methods for micro-inverters used in PV systems”. In: *Chinese Journal of Electrical Engineering* 4.4 (2018), pp. 26–32.

[71] National Fire Protection Association. *National Electrical Code 2011 (National Fire Protection Association National Electrical Code)*. Delmar Cengage Learning, 2010.

[72] B. Singh, R. Kumar, and P. Kant. “Adjustable Speed Induction Motor Drive Fed by 13-Level Cascaded Inverter and 54-Pulse Converter”. In: *IEEE Transactions on Industry Applications* 58.1 (2022), pp. 890–900.

[73] J. Tanguturi and S. Keerthipati. “Power Balancing Strategy for Cascaded H-Bridge Inverter in a Grid-Connected Photovoltaic System Under Asymmetrical Operating Conditions”. In: *IEEE Transactions on Industrial Electronics* 71.6 (2024), pp. 5853–5862.

[74] R. Sharma and A. Das. “Extended Reactive Power Exchange With Faulty Cells in Grid-Tied Cascaded H-Bridge Converter for Solar Photovoltaic Application”. In: *IEEE Transactions on Power Electronics* 35.6 (2020), pp. 5683–5691.

[75] A. Lashab *et al.* “Cascaded Multilevel PV Inverter With Improved Harmonic Performance During Power Imbalance Between Power Cells”. In: *IEEE Transactions on Industry Applications* 56.3 (2020), pp. 2788–2798.

[76] Y. Pan, A. Sangwongwanich, Y. Yang, and F. Blaabjerg. “A Phase-Shifting MPPT to Mitigate Interharmonics From Cascaded H-Bridge PV Inverters”. In: *IEEE Transactions on Industry Applications* 57.3 (2021), pp. 3052–3063.

[77] M. Bahrami-Fard, N. Moeini, M. Shahabadini, H. Iman-Eini, and M. Liserre. “A New Topology and Modulation Strategy to Suppress the Leakage Current in Transformerless Cascaded H-Bridge Inverters in PV Application”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* (2022), pp. 1–1.

[78] P. Zhao, X. He, Y. Wang, C. Qiu, and P. Han. “Hardware-Based Modulation Strategy to Suppress the Leakage Current for Transformerless Odd-Module Cascaded H-Bridge Inverter in PV System”. In: *IEEE Transactions on Power Electronics* 39.3 (2024), pp. 3655–3667.

[79] S. Barcellona, M. Barresi, and L. Piegari. “MMC-Based PV Single-Phase System with Distributed MPPT”. In: *Energies* 13.15 (2020).

[80] S. Nayak and A. Das. “A Power Balancing Strategy in a PV-Based Modular Multilevel Converter During Mismatched Power Generation”. In: *IEEE Transactions on Industrial Electronics* 71.7 (2024), pp. 7117–7125.

[81] J. Teng, X. Sun, X. Liu, W. Zhao, and X. Li. “Power Mismatches Elimination Strategy for MMC-Based Photovoltaic System and Lightweight Design”. In: *IEEE Transactions on Power Electronics* 38.9 (2023), pp. 11614–11629.

[82] U. L. U. *Standard for Flat-Plate Photovoltaic Modules and Panels*. 2004, pp. 51–57.

[83] P. McNutt, W. R. Sekulic, and G. Dreifuerst. “Solar/Photovoltaic dc Systems: Information for Electrical Workers and Firefighters”. In: *IEEE Industry Applications Magazine* 26.3 (2020), pp. 39–47.

[84] H. Katir, A. Abouloifa, E. Elbouchikhi, A. Fekih, K. Noussi, and A. E. Aroudi. “Robust Control of Cascaded H-Bridge Multilevel Inverters for Grid-Tied PV Systems Subject to Faulty Conditions”. In: *IEEE Control Systems Letters* 7 (2023), pp. 2683–2688.

[85] M. Jafari, Z. Malekjamshidi, and M. R. Islam. “Optimal Design of a Multiwinding High-Frequency Transformer Using Reluctance Network Modeling and Particle Swarm Optimization Techniques for the Application of PV-Linked Grid-Connected Modular Multilevel Inverters”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 9.4 (2021), pp. 5083–5096.

[86] Y. Yu, G. Konstantinou, C. D. Townsend, R. P. Aguilera, and V. G. Agelidis. “Delta-Connected Cascaded H-Bridge Multilevel Converters for Large-Scale Photovoltaic Grid Integration”. In: *IEEE Transactions on Industrial Electronics* 64.11 (2017), pp. 8877–8886.

[87] P. Sochor, N. M. L. Tan, and H. Akagi. “Low-Voltage-Ride-Through Control of a Modular Multilevel Single-Delta Bridge-Cell (SDBC) Inverter for Utility-Scale Photovoltaic Systems”. In: *IEEE Transactions on Industry Applications* 54.5 (2018), pp. 4739–4751.

[88] S. Rivera, B. Wu, R. Lizana, S. Kouro, M. Perez, and J. Rodriguez. “Modular Multilevel Converter for Large-Scale Multistring Photovoltaic Energy Conversion System”. In: *2013 IEEE Energy Conversion Congress and Exposition*. 2013, pp. 1941–1946.

[89] J. Yang, R. Li, K. Ma, and J. Xu. “A Distributed Multimode Control Strategy for the Cascaded DC–DC Converter Applied to MVAC Grid-Tied PV System”. In: *IEEE Transactions on Industrial Electronics* 70.3 (2023), pp. 2617–2627.

[90] S. Barcellona, M. Barresi, and L. Piegari. “MMC-Based PV Three-Phase System with Distributed MPPT”. In: *IEEE Transactions on Energy Conversion* (2022), pp. 1–1.

[91] H. Akagi. “Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)”. In: *IEEE Transactions on Power Electronics* 26.11 (2011), pp. 3119–3130.

[92] I. Marzo, A. Sanchez-Ruiz, J. A. Barrena, G. Abad, and I. Muguruza. “Power Balancing in Cascaded H-Bridge and Modular Multilevel Converters Under Unbalanced Operation: A Review”. In: *IEEE Access* 9 (2021), pp. 110525–110543.

[93] B. Chen *et al.* “A High-Efficiency MOSFET Transformerless Inverter for Nonisolated Microinverter Applications”. In: *IEEE Transactions on Power Electronics* 30.7 (2015), pp. 3610–3622.

[94] S. Ravyts, M. D. Vecchia, G. V. den Broeck, and J. Driesen. “Review on Building-Integrated Photovoltaics Electrical System Requirements and Module-Integrated Converter Recommendations”. In: *MDPI Energies* 12.8 (2019), p. 1532.

[95] R. C. N. Pilawa-Podgurski and D. J. Perreault. “Submodule Integrated Distributed Maximum Power Point Tracking for Solar Photovoltaic Applications”. In: *IEEE Transactions on Power Electronics* 28.6 (2013), pp. 2957–2967.

[96] D. R. E. Trejo, S. Taheri, J. L. Saavedra, P. Vázquez, C. H. D. Angelo, and J. A. Pecina-Sánchez. “Nonlinear Control and Internal Stability Analysis of Series-Connected Boost DC/DC Converters in PV Systems With Distributed MPPT”. In: *IEEE Journal of Photovoltaics* 11.2 (2021), pp. 504–512.

[97] W. Xiao, M. S. E. Moursi, O. Khan, and D. J. I. R. P. G. Infield. “Review of Grid-Tied Converter Topologies Used in Photovoltaic Systems”. In: *IEEE Transactions on Power Electronics* 10.10 (2016), pp. 1543–1551.

[98] P. M. Lingom, J. Song-Manguelle, D. L. Mon-Nzongo, R. C. C. Flesch, and T. Jin. “Analysis and Control of PV Cascaded H-Bridge Multilevel Inverter With Failed Cells and Changing Meteorological Conditions”. In: *IEEE Transactions on Power Electronics* 36.2 (2021), pp. 1777–1789.

[99] O. Abdel-Rahim, A. Chub, D. Vinnikov, and A. Blinov. “DC Integration of Residential Photovoltaic Systems: A Survey”. In: *IEEE Access* 10 (2022), pp. 66974–66991.

[100] D. Vinnikov, A. Chub, E. Liivik, R. Kosenko, and O. Korkh. “Solar Optiverter—A Novel Hybrid Approach to the Photovoltaic Module Level Power Electronics”. In: *IEEE Transactions on Industrial Electronics* 66.5 (2019), pp. 3869–3880.

[101] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman. “Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications”. In: *IEEE Transactions on Power Electronics* 32.12 (2017), pp. 9143–9178.

[102] T. Solar. *Taylor Solar Website*. Accessed: Nov. 7, 2024. 2023. url: https://www.taylor.solar.

[103] L. Linares, R. W. Erickson, S. MacAlpine, and M. Brandemuehl. “Improved Energy Capture in Series String Photovoltaics via Smart Distributed Power Electronics”. In: *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*. 2009, pp. 904–910.

[104] G. R. Walker and P. C. Sernia. “Cascaded DC-DC Converter Connection of Photovoltaic Modules”. In: *IEEE Transactions on Power Electronics* 19.4 (2004), pp. 1130–1139.

[105] N. G. F. d. Santos, J. R. R. Zientarski, and M. L. d. S. Martins. “A Review of Series-Connected Partial Power Converters for DC–DC Applications”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 10.6 (2022), pp. 7825–7838.

[106] K. D. Waal, H. J. Bergveld, H. C. J. Buthker, and F. A. Schoofs. *Photovoltaic Assembly and Method of Operating a Photovoltaic Assembly*. Patent, Google Patents. 2014.

[107] L. Irish. *Solar Charge Controller Adaptable for Multiple Solar Substring Chemistries and Configurations*. Patent, Google Patents. 2023.

[108] S. Ben-Yaakov, A. Cervera, A. Blumenfeld, and M. M. Peretz. *Resonant Switched-Capacitor Gyrator-Type Converter with Local MPPT Capability for PV Cells*. Patent, Google Patents. 2018.

[109] optivolt. *optivolt*. https://optivolt.com/. Accessed: 2024-11-08.

[110] K. A. Kim, P. S. Shenoy, and P. T. Krein. “Converter Rating Analysis for Photovoltaic Differential Power Processing Systems”. In: *IEEE Transactions on Power Electronics* 30.4 (2015), pp. 1987–1997.

[111] S. Qin, S. T. Cady, A. D. Domínguez-García, and R. C. N. Pilawa-Podgurski. “A Distributed Approach to Maximum Power Point Tracking for Photovoltaic Submodule Differential Power Processing”. In: *IEEE Transactions on Power Electronics* 30.4 (2015), pp. 2024–2040.

[112] S. Qin and R. C. N. Pilawa-Podgurski. “Sub-module Differential Power Processing for Photovoltaic Applications”. In: *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2013, pp. 101–108.

[113] G. Chu, H. Wen, L. Jiang, Y. Hu, and X. Li. “Bidirectional Flyback Based Isolated-Port Submodule Differential Power Processing Optimizer for Photovoltaic Applications”. In: *Solar Energy* 158 (2017), pp. 929–940.

[114] M. Kasper, D. Bortis, and J. W. Kolar. “Unified Power Flow Analysis of String Current Diverters”. In: *Electrical Engineering* 100.3 (2018), pp. 2085–2094.

[115] P. S. Shenoy, K. A. Kim, B. B. Johnson, and P. T. Krein. “Differential Power Processing for Increased Energy Production and Reliability of Photovoltaic Systems”. In: *IEEE Transactions on Power Electronics* 28.6 (2013), pp. 2968–2979.

[116] F. Wang, T. Zhu, F. Zhuo, and H. Yi. “An Improved Submodule Differential Power Processing-Based PV System With Flexible Multi-MPPT Control”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 6.1 (2018), pp. 94–102.

[117] C. Schaef and J. T. Stauth. “Multilevel Power-Point-Tracking for Variable-Conversion-Ratio Photovoltaic Ladder Converters”. In: *2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL)*. 2013, pp. 1–7.

[118] Z. Qiu and K. Sun. “A Photovoltaic Generation System Based on Wide Voltage-Gain DC-DC Converter and Differential Power Processors for DC Microgrids”. In: *Chinese Journal of Electrical Engineering* 3.1 (2017), pp. 84–95.

[119] A. Blumenfeld, A. Cervera, and M. M. Peretz. “Enhanced Differential Power Processor for PV Systems: Resonant Switched-Capacitor Gyrator Converter With Local MPPT”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 2.4 (2014), pp. 883–892.

[120] J. T. Stauth, M. D. Seeman, and K. Kesarwani. “Resonant Switched-Capacitor Converters for Sub-module Distributed Photovoltaic Power Management”. In: *IEEE Transactions on Power Electronics* 28.3 (2013), pp. 1189–1198.

[121] M. K. Al-Smadi and Y. Mahmoud. “Image-Based Differential Power Processing for Photovoltaic Microinverter”. In: *IEEE Transactions on Energy Conversion* 36.2 (2021), pp. 619–628.

[122] M. Uno and A. Kukita. “PWM Converter Integrating Switched Capacitor Converter and Series-Resonant Voltage Multiplier as Equalizers for Photovoltaic Modules and Series-Connected Energy Storage Cells for Exploration Rovers”. In: *IEEE Transactions on Power Electronics* 32.11 (2017), pp. 8500–8513.

[123] M. Uno, R. Igarashi, and Y. Sato. “Switched Capacitor-Based PWM- and Phase Shift-Controlled Multiport Converter With Differential Power Processing Capability for Standalone Photovoltaic Systems Under Partial Shading”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 9.5 (2021), pp. 6019–6032.

[124] M. Gokdag, M. Akbaba, and O. Gulbudak. “Switched-capacitor converter for PV modules under partial shading and mismatch conditions”. In: *Solar Energy* 170 (Aug. 2018), pp. 723–731.

[125] M. Uno, M. Yamamoto, H. Sato, and S. Oyama. “Modularized Differential Power Processing Architecture Based on Switched Capacitor Converter to Virtually Unify Mismatched Photovoltaic Panel Characteristics”. In: *IEEE Transactions on Power Electronics* 35.2 (2020), pp. 1563–1575.

[126] M. Uno, H. Sato, and S. Oyama. “Switched Capacitor-Based Modular Differential Power Processing Architecture for Large-Scale Photovoltaic Systems Under Partial Shading”. In: *IEEE Transactions on Energy Conversion* (2022), pp. 1–1.

[127] M. Tahmasbi-Fard, M. Tarafdar-Hagh, S. Pourpayam, and A. Haghrah. “A Voltage Equalizer Circuit to Reduce Partial Shading Effect in Photovoltaic String”. In: *IEEE Journal of Photovoltaics* 8.4 (2018), pp. 1102–1109.

[128] I. Shams, S. Mekhilef, and K. S. Tey. “Extendable Voltage Equalizer Topology with Reduced Switch Count and MPPT with Partial Shading detection capability for Long Serially Connected PV Modules”. In: *IEEE Transactions on Industry Applications* (2022), pp. 1–12.

[129] Y. Jeon, H. Lee, K. A. Kim, and J. Park. “Least Power Point Tracking Method for Photovoltaic Differential Power Processing Systems”. In: *IEEE Transactions on Power Electronics* 32.3 (2017), pp. 1941–1951.

[130] Y. Jeon and J. Park. “Unit-Minimum Least Power Point Tracking for the Optimization of Photovoltaic Differential Power Processing Systems”. In: *IEEE Transactions on Power Electronics* 34.1 (2019), pp. 311–324.

[131] G. Chu, H. Wen, Y. Yang, and Y. Wang. “Elimination of Photovoltaic Mismatching With Improved Submodule Differential Power Processing”. In: *IEEE Transactions on Industrial Electronics* 67.4 (2020), pp. 2822–2833.

[132] J. Biswas, A. M. Kamath, A. K. Gopi, and M. Barai. “Design, Architecture, and Real-Time Distributed Coordination DMPPT Algorithm for PV Systems”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 6.3 (2018), pp. 1418–1433.

[133] M. Uno and A. Kukita. “Single-Switch Voltage Equalizer Using Multistacked Buck–Boost Converters for Partially Shaded Photovoltaic Modules”. In: *IEEE Transactions on Power Electronics* 30.6 (2015), pp. 3091–3105.

[134] M. Uno and A. Kukita. “Current Sensorless Equalization Strategy for a Single-Switch Voltage Equalizer Using Multistacked Buck–Boost Converters for Photovoltaic Modules Under Partial Shading”. In: *IEEE Transactions on Industry Applications* 53.1 (2017), pp. 420–429.

[135] M. Uno and A. Kukita. “Two-Switch Voltage Equalizer Using an LLC Resonant Inverter and Voltage Multiplier for Partially Shaded Series-Connected Photovoltaic Modules”. In: *IEEE Transactions on Industry Applications* 51.2 (2015), pp. 1587–1601.

[136] M. Uno and K. Honda. “Panel-to-Substring Differential Power Processing Converter With Embedded Electrical Diagnosis Capability for Photovoltaic Panels Under Partial Shading”. In: *IEEE Transactions on Power Electronics* 36.9 (2021), pp. 10239–10250.

[137] M. Uno, H. Sato, and T. Ishikawa. “Differential Power Processing Converter Enhancing Energy Yield of Curved Solar Roofs of Plug-In Hybrid Electric Vehicles”. In: *IEEE Transactions on Vehicular Technology* 69.12 (2020), pp. 14689–14700.

[138] M. Uno, Y. Sasaki, and Y. Fujii. “Fault Tolerant Modular Differential Power Processing Converter for Photovoltaic Systems”. In: *IEEE Transactions on Industry Applications* 59.1 (2023), pp. 1139–1151.

[139] M. Uno, T. Suzuki, and Y. Fujii. “Module-to-Panel Modular Differential Power Processing Converter With Isolated DC Bus for Photovoltaic Systems Under Partial Shading”. In: *IEEE Journal of Emerging and Selected Topics in Industrial Electronics* 4.1 (2023), pp. 97–108.

[140] J. Du, R. Xu, X. Chen, Y. Li, and J. Wu. “A novel solar panel optimizer with self-compensation for partial shadow condition”. In: *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2013, pp. 92–96.

[141] H. Jeong, H. Lee, Y. Liu, and K. A. Kim. “Review of Differential Power Processing Converter Techniques for Photovoltaic Applications”. In: *IEEE Transactions on Energy Conversion* 34.1 (2019), pp. 351–360.

[142] K. Sun, Z. Qiu, H. Wu, and Y. Xing. “Evaluation on High-Efficiency Thermoelectric Generation Systems Based on Differential Power Processing”. In: *IEEE Transactions on Industrial Electronics* 65.1 (2018), pp. 699–708.

[143] T. Shimizu, M. Hirakata, T. Kamezawa, and H. Watanabe. “Generation Control Circuit for Photovoltaic Modules”. In: *IEEE Transactions on Power Electronics* 16.3 (2001), pp. 293–300.

[144] H. Jeong, S. Park, J. H. Jung, T. Kim, A. R. Kim, and K. A. Kim. “Segmented Differential Power Processing Converter Unit and Control Algorithm for Photovoltaic Systems”. In: *IEEE Transactions on Power Electronics* 36.7 (2021), pp. 7797–7809.

[145] C. Olalla, D. Clement, M. Rodriguez, and D. Maksimovic. “Architectures and Control of Submodule Integrated DC–DC Converters for Photovoltaic Applications”. In: *IEEE Transactions on Power Electronics* 28.6 (2013), pp. 2980–2997.

[146] Y. Levron, D. R. Clement, B. Choi, C. Olalla, and D. Maksimovic. “Control of Submodule Integrated Converters in the Isolated-Port Differential Power-Processing Photovoltaic Architecture”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 2.4 (2014), pp. 821–832.

[147] R. Bell and R. C. N. Pilawa-Podgurski. “Decoupled and Distributed Maximum Power Point Tracking of Series-Connected Photovoltaic Submodules Using Differential Power Processing”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 3.4 (2015), pp. 881–891.

[148] E. Candan, P. S. Shenoy, and R. C. N. Pilawa-Podgurski. “A Series-Stacked Power Delivery Architecture With Isolated Differential Power Conversion for Data Centers”. In: *IEEE Transactions on Power Electronics* 31.5 (2016), pp. 3690–3703.

[149] L. F. L. Villa, T. P. Ho, J. C. Crebier, and B. Raison. “A Power Electronics Equalizer Application for Partially Shaded Photovoltaic Modules”. In: *IEEE Transactions on Industrial Electronics* 60.3 (2013), pp. 1179–1190.

[150] L. F. L. Villa, X. Pichon, F. Sarrafin-Ardelibi, B. Raison, J. C. Crebier, and A. Labonne. “Toward the Design of Control Algorithms for a Photovoltaic Equalizer: Choosing the Optimal Switching Strategy and the Duty Cycle”. In: *IEEE Transactions on Power Electronics* 29.3 (2014), pp. 1447–1460.

[151] L. F. L. Villa, B. Raison, and J. Crebier. “Toward the Design of Control Algorithms for a Photovoltaic Equalizer: Detecting Shadows Through Direct Current Sampling”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 2.4 (2014), pp. 893–906.

[152] M. O. Badawy, S. M. Bose, and Y. Sozer. “A Novel Differential Power Processing Architecture for a Partially Shaded PV String Using Distributed Control”. In: *IEEE Transactions on Industry Applications* 57.2 (2021), pp. 1725–1735.

[153] M. Etarhouni, B. Chong, and L. Zhang. “Optimal Design of Series-Parallel Differential Power Processing Converters for Photovoltaic Array Energy Systems”. In: *EU-PVSEC Proceedings 2020*. Leeds, 2020, pp. 1181–1187.

[154] M. Etarhouni, B. Chong, and L. Zhang. “A combined scheme for maximising the output power of a Photovoltaic array under partial shading conditions”. In: *Sustainable Energy Technologies and Assessments* 50 (Mar. 2022), p. 101878.

[155] C. Liu, Y. Zheng, D. Li, and B. Lehman. “Distributed MPPT for modular differential power processing in scalable photovoltaic system”. In: *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2018, pp. 1098–1103.

[156] C. Liu, D. Li, Y. Zheng, and B. Lehman. “Modular differential power processing (mDPP)”. In: *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*. 2017, pp. 1–7.

[157] S. Qin, C. B. Barth, and R. C. N. Pilawa-Podgurski. “Enhancing Microinverter Energy Capture With Submodule Differential Power Processing”. In: *IEEE Transactions on Power Electronics* 31.5 (2016), pp. 3575–3585.

[158] M. Uno and T. Shinohara. “Module-Integrated Converter Based on Cascaded Quasi-Z-Source Inverter With Differential Power Processing Capability for Photovoltaic Panels Under Partial Shading”. In: *IEEE Transactions on Power Electronics* 34.12 (2019), pp. 11553–11565.

[159] H. J. Bergveld *et al.* “Module-Level DC/DC Conversion for Photovoltaic Systems: The Delta-Conversion Concept”. In: *IEEE Transactions on Power Electronics* 28.4 (2013), pp. 2005–2013.

[160] S. Harb, M. Kedia, H. Zhang, and R. S. Balog. “Microinverter and string inverter grid-connected photovoltaic system — A comprehensive study”. In: *2013 IEEE 39th Photovoltaic Specialists Conference (PVSC)*. 2013, pp. 2885–2890.

[161] O. A. Arráez-Cancelliere, N. Muñoz-Galeano, and J. M. Lopez-Lezama. “Performance and economical comparison between micro-inverter and string inverter in a 5, 1 kWp residential PV-system in Colombia”. In: *2017 IEEE Workshop on Power Electronics and Power Quality Applications (PEPQA)*. 2017, pp. 1–5.

[162] Z. Moradi-Shahrbabak, A. Tabesh, and G. R. Yousefi. “Economical Design of Utility-Scale Photovoltaic Power Plants With Optimum Availability”. In: *IEEE Transactions on Industrial Electronics* 61.7 (2014), pp. 3399–3406.

3

PV2VB PDPP ARCHITECTURE(STATIC ANALYSIS)

This chapter analyses the PV to virtual bus (PV2VB) Parallel Differential Power Processing (PDPP) architecture designed to mitigate the effect of mismatch among photovoltaic (PV) strings. The proposed PV2VB PDPP architecture leverages a virtual bus as the input for all string-level converters. Notably, this approach reduces components' voltage rating since the virtual bus voltage can be set lower than the main bus or PV strings voltage. In this architecture, crucial requirements for the String-Level Converters (SLCs) include the capability to generate positive and negative output voltages and to provide isolation. To fulfill these requirements, a Dual Active Bridge converter connected to a bridgeless converter is considered an SLC. In this architecture, while SLCs ensure Maximum Power Point Tracking (MPPT) for each PV string using conventional MPPT algorithms, the central converter controls the virtual bus voltage. Experimental results validate the performance of the proposed PV to virtual bus PDPP architecture with a system efficiency (excluding the power losses due to the MPPT algorithm) ranging from 96.4% to 99%.

Parts of this chapter have been published in IEEE Transactions on Industrial Electronic [1] and Mathematics and Computers in Simulation [2] journals.

3.1. INTRODUCTION

As discussed in Chapter 2, SDPP architectures regulate the differential current between individual PV modules ($i_{PV_{M_j}}$) and the PV string current ($i_{PV_{S_i}}$), effectively mitigating mismatch-related losses within series-connected PV groups (Fig. 3.1(a)). Yet, they are insufficient in addressing mismatch losses among parallel-connected PV strings [3, 4]. Thus, the concept of PDPP has emerged (Fig. 3.1 (b)) [5–13]. PDPP architectures compensate for the differential voltage between PV strings and a main bus, eliminating mismatch losses among parallel PV strings. Despite all the current from the j^{th} PV string flowing through the respective String Level Converters (SLC), the voltage across the j^{th} SLC (V_{SLC_j}) may be lower than the PV string voltage. This suggests that the power handled by the SLCs may be less than that of conventional FPP multi-string architecture, allowing for potential reduction in converter rating and conversion losses. PDPP architectures are categorized based on the connection of the primary side of the SLCs.

In PDPP architecture, with N_{PV} PV string, there are N_{PV} control objectives and $N_{PV}+1$ control actuators (N_{PV} SLCs and central converter). Consequently, i^{th} PV string operates at its MPP by adjusting the duty cycle of the i^{th} SLCs, while the additional degree of freedom from the central converter helps minimize power losses by regulating the DC Bus voltage. To the best of the authors' knowledge, only SLCs generating positive voltage have been proposed for PV2B PDPP architectures [5, 14–17]. However, with SLCs exclusively generating positive voltage, the DC Bus voltage must consistently exceed the voltage of the PV string with the highest MPP voltage. Ideally, the DC Bus voltage should match the highest actual MPP string voltage. While this assumption can reduce processed power, achieving it is challenging as it necessitates some SLCs to operate at extremely low duty ratios. To overcome this issue, the DC Bus voltage must increase, leading to a significant rise in processed power [15]. Consequently, despite the additional degree of freedom, when SLCs only operate with positive voltages, optimization of power processing remains unrealized. DPP architectures are classified based on how the primary side of the SLCs is connected. The commonly analyzed PV2B architectures are further divided into two types: PV2B-I [5–9] and PV2B-II [10–13]. In PV2B-I, the primary side of the SLCs connects to the main bus (Fig. 3.1 (c)), whereas in PV2B-II, the primary side connects directly to the PV strings (Fig. 3.1 (d)). The optimal architecture for any application is the one that results in the lowest maximum power processing losses [18].

In [10], a buck-boost converter was chosen as the SLC for the PV2B-II architecture. While these SLCs are designed to compensate for the voltage differences between the PV strings and the main bus, they must also manage the full current produced by the PV strings. This requirement necessitates that the components endure the voltage from

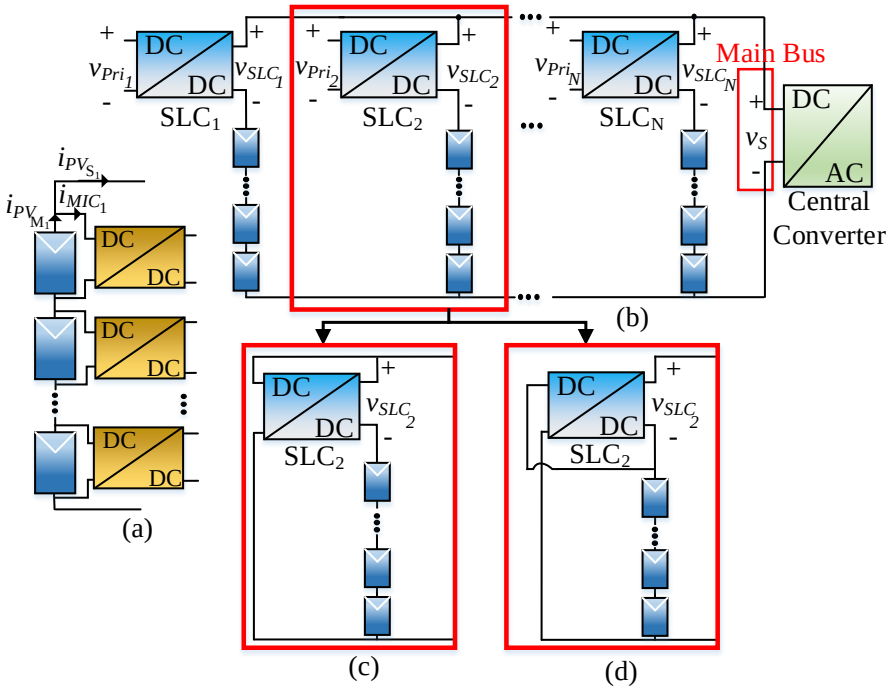

Figure 3.1.: PV system using: (a) general SDPP architecture, (b) general PDPP architecture with primary side connection to (c) main bus (PV2B-I PDPP architecture) or to (d) PV string (PV2B-II PDPP architecture)

the PV strings, leading to SLCs with power ratings similar to those of FPP converters. In [5, 9] and [11], a flyback converter is employed in both PV2B-I and PV2B-II architectures. Although flyback converters are favored for their simplicity, their application is generally restricted to power outputs of a few hundred watts. Consequently, other research [6–8, 11, 13, 19] has explored various topologies (Fig. 3.2), including series resonant converters [6], current-fed resonant push-pull converters [7], Current-fed full-bridge converters [8], and Full-bridge converters [13] to improve power handling capabilities, though this often comes at the cost of simplicity.

Although high efficiency has been reported for PV2B architectures, directly connecting SLCs to the main bus or PV strings presents three main disadvantages. Firstly, the voltage rating of SLCs is determined by the PV strings or main bus voltage. Secondly, the scalability of the PV system is limited: adding PV modules to a PV string increases the

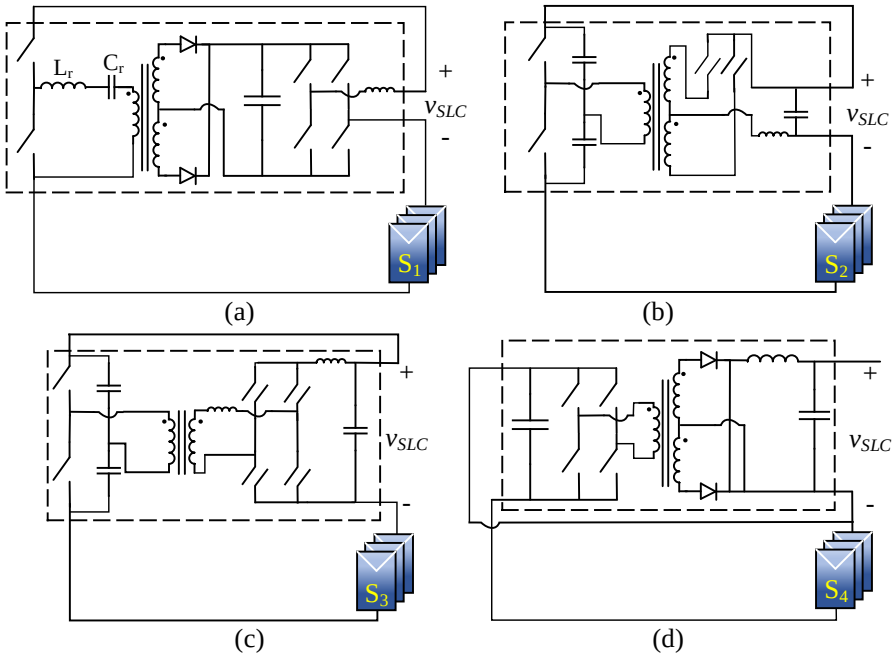

Figure 3.2.: Topology for PV2B PDPP: (a) series resonant converter [6], (b) current fed resonant push-pull [7], (c) current-fed full-bridge [8], and (d) full-bridge [13].

string's voltage, necessitating SLCs with higher voltage ratings. These first two issues also exist in FPP SLCs. Lastly, PV2B PDPP require SLCs with high voltage conversion ratio ($\frac{v_{SLC}}{v_S}$).To address the challenges of both PV2B PDPP and conventional FPP architectures, we have proposed a novel PV2VB PDPP architecture. This chapter provides a comprehensive analysis and presents experimental validations to demonstrate the performance of this architecture.

As shown in Fig. 3.3, PV2VB PDPP is a novel architecture where SLC inputs are connected to a common isolated DC bus called the virtual bus instead of the main bus. One key advantage is the flexibility to select a lower voltage for the virtual bus compared to the main bus, leading to a potential reduction in the initial and repair costs of SLCs. Additionally, the use of low-blocking voltage semiconductors in the PV2VB architecture enables the use of MOSFETs instead of IGBTs, enabling higher switching frequencies, reducing the size of passive components, and improving the converter's power density. Moreover, there will be less challenge in designing EMI/EMC filters for low-voltage converters which simplifies

compliance with electromagnetic compatibility standards [20, 21]. Besides, this architecture can mitigate the high voltage conversion ratio required for SLCs in PV2B architectures.

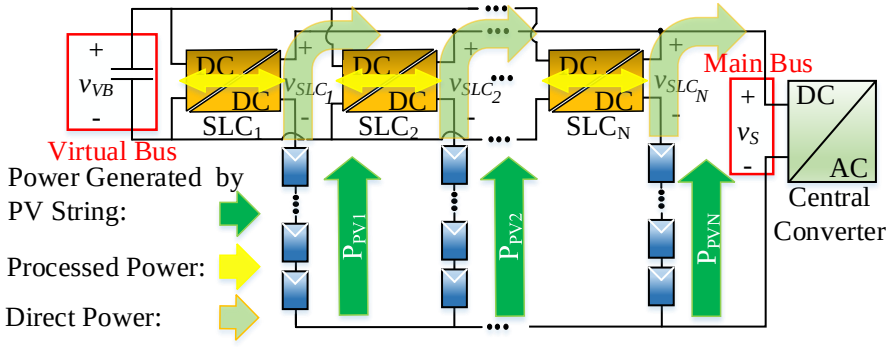

Figure 3.3.: PV systems using the proposed PV2VB PDPP architecture.

This innovative architecture also offers superior scalability compared to conventional counterparts. In the proposed PV2VB architecture, the SLC input voltage corresponds to the virtual bus voltage, not the PV string nor the main bus voltage. Therefore, the proposed architecture offers flexibility to incorporate new PV modules into strings, making it a more adaptable and versatile solution. This scalability enables its use for a wide range of PV string lengths, facilitating mass production and lowering manufacturing costs. A comparison between PV2B and proposed PV2VB PDPP architectures is presented in Table. 3.1.

The proposed architecture performs string-level Maximum Power Point Tracking (MPPT) while processing only a fraction of the power generated by PV strings. The power the SLCs process varies based on environmental conditions, PV module specifications, string length, and the number of PV strings in operation. To address this variability, this chapter introduces a power flow analysis method. This method simplifies determining SLC power processing under different scenarios with multiple PV strings and helps identify the required power rating for SLCs under predefined environmental conditions or worst-case shading scenarios.

The remainder of this chapter is structured as follows: Section 3.2 provides an in-depth analysis of the steady-state operation of both the central converter and SLCs and elucidates their respective control objectives. Section 3.3 derives the equations governing the processed power to determine SLCs rating and compare it with the conventional FPP architectures. Section 3.4 describes the different

operational regions of the PV2VB PDPP architecture. Finally, Section 3.5 presents experimental results that validate the architecture's capability for string-level MPPT, substantiating its inherent advantages.

Table 3.1.: Comparison of PDPP Architectures

Ref.	Architecture	SLCs topology	Bidirectional SLCs	Isolated SLCs	CVR[1]	Scalability	VCR[2]	Power level	Reported efficiency (%)
[5]	PV2B-I	Flyback	No	Yes	High/low[3]	Low	High	50 W	89-97
[6]	PV2B-I	Series resonant converter	No	Yes	High/low	Med	Med	4 kW	97.75-98.82
[7]	PV2B-I	Current fed resonant push-pull	Yes	Yes	High/low	Low	High	2.2 kW	97.8-98.8
[8]	PV2B-I	Current-fed full-bridge	Yes	Yes	High/low	Low	High	2.2 kW	95.5-98.2
[9]	PV2B-I	Flyback	No	Yes	High/low	Low	High	25 W	98.5
[10]	PV2B-II	Buck-boost	No	No	High	Low	High	3.5 kW	96-98.9
[11]	PV2B-II	Flyback	No	Yes	High/low	Low	High	100 W	70-90
[12]	PV2B-II	Full-bridge	No	Yes	High/low	Low	High	821 W	98-99
[13]	PV2B-II	Full-bridge/ Push-pull	Yes	Yes	High/low	Low	High	750 W	98.6-99.58
[13]	PV2B-II	Full-bridge	No	Yes	High/low	Low	High	750 W	98.8
Prop	**PV2VB**	**DAB/BL**	**Yes**	**Yes**	**Low**	**High**	**Low**	**4 kW**	**96.4-99**

1: CVR: Components' voltage rating. 2: VCR: Voltage conversion ratio. 3: High/low: There exist components with high and low voltage ratings

3.2. OVERVIEW OF THE PV2PV PDPP ARCHITECTURE

As shown in Fig. 3.3, in the proposed PV2VB PDPP architecture, SLCs inputs are connected to a shared, isolated DC bus called the virtual bus. To ensure smooth and stable operation, maintaining a power balance within the virtual bus is essential to prevent fluctuations in its voltage. Thus, while certain PV strings inject energy to the virtual bus through the SLCs, others must draw energy from it. This architecture has two primary objectives: (i) maintaining the virtual bus voltage at a constant level, a task overseen by the central converter, and (ii) independently tracking the Maximum Power Point (MPP) of each PV string, a responsibility entrusted to the SLCs. The subsequent subsections will provide an in-depth description of the converters and their respective control principles.

3.2.1. CENTRAL CONVERTER

In a PV2VB PDPP architecture, the central converter regulates the main bus voltage (v_S) by its duty cycle. However, this control action is aimed at ensuring the stability of the virtual bus voltage (v_{VB}). This subsection delves into understanding the relationship between the main bus and virtual bus voltage. Two assumptions are considered for the sake of simplicity: (i) lossless converters, and (ii) the capacitive virtual bus is the main storage element in the system. Then, the power relationship for the PV2VB architecture can be derived as follows:

$$p_{VB} = p_{\text{out}} - p_{\text{in}} \tag{3.1}$$

In the context of the proposed architecture, p_{VB}, p_{out}, and p_{in} represent the instantaneous virtual bus power, power delivered to the main bus, and power generated by the PV strings, respectively; these values can be computed as follows:

$$p_{VB} = C_{VB} \cdot v_{VB} \cdot \frac{dv_{VB}}{dt} \tag{3.2}$$

$$p_{\text{out}} = v_S \cdot i_S = v_S \cdot \sum_{j=1}^{N_{PV}} i_{\text{PV}_j} \tag{3.3}$$

$$p_{\text{in}} = \sum_{j=1}^{N_{PV}} v_{\text{PV}_j} \cdot i_{\text{PV}_j} \tag{3.4}$$

Where C_{VB}, i_S, v_{PV_j}, i_{PV_j}, and N_{PV} are virtual bus capacitance, main bus current, j^{th} PV string's current, j^{th} PV string's voltage, and number of PV strings, respectively; the following equation can be obtained by substituting Equations (3.4)– (3.6) in Equation (3.1):

$$p_{VB} = \frac{dv_{VB}}{dt} \cdot C_{VB} \cdot v_{VB} = \sum_{j=1}^{N_{PV}} v_{\mathrm{PV}_j} \cdot i_{\mathrm{PV}_j} - v_S \cdot i_S \tag{3.5}$$

While it may appear that there are numerous actuators to regulate virtual bus power, it is important to note that PV strings' current and voltages are controlled by SLCs to make PV strings operate at their MPPs. Besides, the main bus current is inherently equal to the summation of the individual PV strings' currents. Thus, the sole variable available for controlling virtual bus power and, consequently, virtual bus voltage is the main bus voltage. When the average power of the virtual bus is maintained at zero, the following equation is derived:

$$P_{VB} = 0 \implies V_S^* = \frac{\sum_{j=1}^{N_{PV}} V_{\mathrm{PV}_j} \cdot I_{\mathrm{PV}_j}}{\sum_{j=1}^{N} I_{\mathrm{PV}_j}}, \quad V_{VB} = \text{const} \tag{3.6}$$

Where V_S^* is the equilibrium main bus voltage at which the virtual bus voltage is constant. It should be noted that capital letters indicate steady-state values of the variables. Combining Equation (3.5) and (3.6), the following equation, which describes the instantaneous rate of change of virtual bus voltage as a function of bus voltage can be derived:

$$\frac{dv_{VB}}{dt} = \frac{\sum_{j=1}^{N_{PV}} V_{\mathrm{PV}_j} \cdot I_{\mathrm{PV}_j}}{C_{VB} \cdot v_{VB}} \cdot \left(1 - \frac{v_S}{V_S^*}\right) \tag{3.7}$$

Equation (3.7) shows the virtual bus voltage rises when the main bus voltage drops below the equilibrium level, and vice versa. Realizing this control mechanism and ensuring the effective integration of it with MPPT algorithms in the architecture necessitates a careful approach. To prevent interference between the controller and to enable the MPPT algorithms to autonomously seek the MPP of the PV string, it is recommended to implement a discrete controller whose sampling time exceeds the perturbation period of the MPPT algorithms. This design consideration ensures that the MPPT algorithms have the required independency for their operation, unburdened by premature or conflicting control actions from the central controller. Such harmony is needed for maintaining precise MPP tracking and overall PV system performance.

3.2.2. SLCs

In the PV2VB PDPP architecture, the primary goal of SLCs is to ensure that PV strings operate at their MPP. To accomplish this, SLCs must also establish a path for the efficient transfer of power to and from the virtual

bus. It is possible to apply a variety of topologies as the SLCs as long as they exhibit three crucial features. Firstly, they must operate effectively within both the first and fourth quadrants of the Voltage-Current (V-I) curve. To elaborate further, the output voltage of the j^{th} SLCs can be expressed as:

$$v_{\mathrm{SLC}_j} = v_S - v_{\mathrm{PV}_j} \tag{3.8}$$

By substituting Equation (3.8) into Equation (3.5), in steady state we have:

$$P_{VB} = \sum_{j=1}^{N_{PV}} V_{\mathrm{SLC}_j} \cdot I_{\mathrm{PV}_j} = \sum_{j=1}^{N_{PV}} P_{\mathrm{SLC}_j} = 0 \tag{3.9}$$

This means that the total output power of all SLCs sums to zero, indicating that SLCs solely facilitate power exchange among themselves. Furthermore, given that I_{PV_j} is consistently positive, Equation (3.9) shows that some SLCs must produce negative output voltage while others must generate positive output voltage to maintain a constant virtual bus voltage during steady-state operation. Secondly, to fulfill the requirements of the architecture, SLCs must function as voltage-source converters to enable their connection to the virtual bus. Eventually, isolation is imperative to enable independent control of PV strings' voltage and to ensure the current from the i^{th} PV string exclusively flows through the i^{th} SLC.

A bidirectional flyback converter followed by a bridgeless (BL) converter (Fig. 3.4 (a)) has been proposed and simulated [2]. While bidirectional flyback converters are well-suited owing to their attributes like simplicity and galvanic isolation, their use is typically limited to power outputs up to a few hundred watts. Beyond this power level, it is advisable to explore alternative topologies better suited for higher-power applications [22]. This study focuses on bidirectional flyback with Dual Active Bridge (DAB) converters as the first stage of the SLCs due to their suitability for high-power applications, while the second stage remains unchanged (Fig. 3.4 (b)).

As depicted in Fig. 3.4 (b), the proposed topology for the SLCs comprises two stages: a DAB converter followed by a BL converter whose performance is decoupled by intermediate bus capacitors. The second stage of the SLC topology is the BL converter, providing both negative and positive output voltage essential for PV strings to operate at their MPP, as well as a current path for the PV string current (Fig. 3.5). Switches are controlled using conventional Carrier Frequency Pulse Width Modulation, and the duty cycle of the BL converter in the j^{th} SLC (d_{BL_j}) is determined by the MPPT algorithm. As shown in Fig. 3.5, during the ON state of the switches, the voltage polarity before the j^{th} LC output filter ($V_{SLC_{BF_j}}$), aligns with the j^{th} intermediate bus voltage

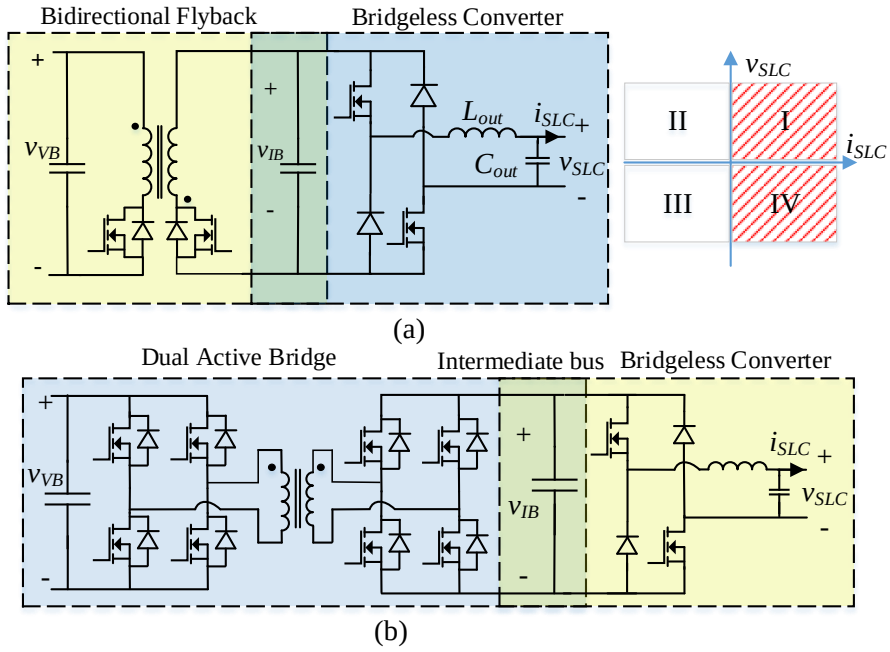

Figure 3.4.: Proposed SLCs topology for PV2VB PDPP architecture: (a) A bidirectional flyback converter followed by a BL converter, (b) A DAB converter followed by a BL converter.

(v_{IB_j}), leading to the intermediate bus capacitor discharge with power equal to:

$$p_{C_{IB_{j_1}}} = v_{\mathrm{IB}_j} \cdot i_{\mathrm{PV}_j} \tag{3.10}$$

Conversely, when the switches are OFF,the BL converter inverts the intermediate bus voltage, and the capacitor is charged.

$$p_{C_{IB_{j_2}}} = v_{\mathrm{IB}_j} \cdot \left(-i_{\mathrm{PV}_j}\right) \tag{3.11}$$

Considering Equation (3.10) and (3.11), the average power over a switching period (T_{sw}) of intermediate bus capacitor the BL converter will be:

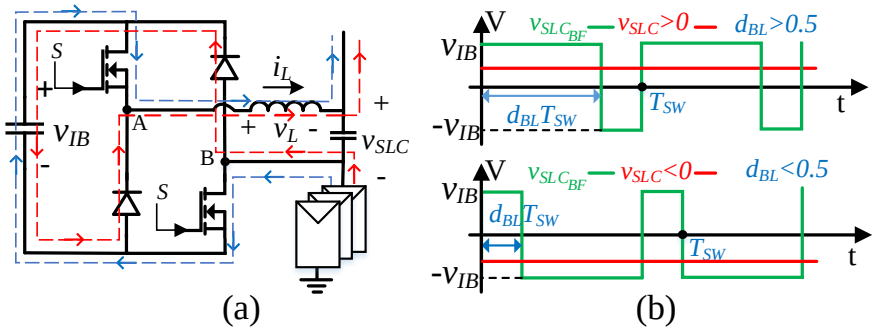

Figure 3.5.: Operation of the BL converter. (a) Topology. Blue dashed line: operation during ON-state, Red dashed line: operation during OFF-state, and (b) its waveforms. The voltage difference between point A and B is the voltage of BL converters before LC filter ($V_{SLC_{BF_j}}$).

$$P_{C_{IB_j}} = \frac{1}{T_{sw}} \int_0^{d_{BL_j} \cdot T_{sw}} p_{C_{IB_{j1}}}\, dt + \frac{1}{T_{sw}} \int_{d_{BL_j} \cdot T_{sw}}^{(1-d_{BL_j}) \cdot T_{sw}} p_{C_{IB_{j2}}}\, dt$$
$$= (2d_{BL_j} - 1) \cdot V_{IB_j} \cdot I_{PV_j} = V_{SLC_j} \cdot I_{PV_j} \qquad (3.12)$$

Where $P_{C_{IB_j}}$ is the power transferred from/to the intermediate bus to/from the string. To make the average power flow from the virtual bus to the string, which corresponds to adding a positive voltage to the PV string, it is essential to maintain a duty cycle greater than 0.5 in the BL converter. When the duty cycle falls below this threshold, the direction of the average power flow reverses, moving from the PV string back to the virtual bus, and a negative voltage is added to the PV string.

To ensure the stability of the intermediate bus voltage (v_{IB}), DAB converters facilitate the transfer of power between the virtual bus and an intermediate bus, primary and secondary sides, respectively. While various modulation techniques are available for DAB converters, this study employs single-phase shift (SPS) modulation [23]. In SPS modulation, all switches operate at a constant frequency with a duty cycle of 50%, and the diagonal switches switch ON and OFF in unison, resulting in a square wave output. The power transfer is controlled by adjusting the phase shift (φ) between two ac voltage waveforms across the windings of the isolation transformer. The relationship between the phase shift (φ) and the DAB average output power (P_{DAB}) is expressed as

follows: To transfer the energy from the virtual bus to the intermediate bus, the DAB converter's primary side leads its secondary side ($\varphi > 0$). If the energy transfer direction is reversed, the primary side bridge lags the secondary ($\varphi < 0$) (Fig. 3.5). In other words, power flows from the leading to the lagging bridge.

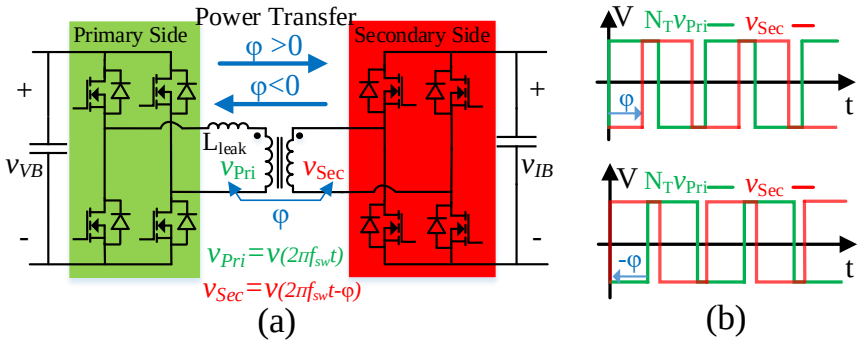

Figure 3.6.: DAB Converter Operation. (a) Topology, and (b) its waveforms.

$$P_{\mathrm{DAB}} = \frac{V_{\mathrm{VB}} \cdot V_{\mathrm{IB}} \cdot \varphi \cdot (\pi - \varphi)}{N_{\mathrm{T}} \cdot f_{\mathrm{sw}} \cdot L_{\mathrm{leak}}} \tag{3.13}$$

Where, N_T, f_{sw}, L_{leak} are the DAB transformer ratio, switching frequency, and leakage inductance, respectively. A controller like a Proportional-Integral (PI) controller receives the error value of the intermediate capacitor voltage and adjusts the phase shift accordingly to ensure that the necessary power for the BL stage is supplied:

$$P_{\mathrm{DAB}_j} = P_{\mathrm{BL}_j} = P_{\mathrm{C_{IB}}_j} \tag{3.14}$$

3.3. PROCESSED POWER AND CONVERTER RATING

The power processed by converters represents a crucial parameter with implications for systems' efficiency, availability, and cost. In a PV system based on PDPP architectures, part of the power generated by the PV strings is processed by the SLCs, which determine the power, voltage, and current rating of these converters.

3.3.1. DAB CONVERTERS PROCESSED POWER

In the PV2VB architecture, the primary objective of DAB converters is to maintain a constant voltage across the intermediate bus through controlled power exchange. This critical function ensures stability within the system. The power transferred between the virtual bus and jth intermediate bus results in the processed power by the associated DAB converter, which considering Equation (3.14), is equal to:

$$P_{\mathrm{DAB}_j} = P_{\mathrm{BL}_j} = V_{\mathrm{SLC}_j} \cdot I_{\mathrm{PV}_j} = (V_S - V_{\mathrm{PV}_j}) \cdot I_{\mathrm{PV}_j} \tag{3.15}$$

by considering Equation (3.6) in the steady-state condition ($P_{VB} = 0$) and substituting it into Equation (3.15), we have:

$$P_{\mathrm{DAB}_j} = \left(\frac{\sum_{j=1}^{N_{\mathrm{PV}}} V_{\mathrm{PV}_j} \cdot I_{\mathrm{PV}_j}}{\sum_{j=1}^{N_{\mathrm{PV}}} I_{\mathrm{PV}_j}} - V_{\mathrm{PV}_j} \right) \cdot I_{\mathrm{PV}_j} \tag{3.16}$$

As shown by Equation (3.16), the processed power of the j^{th} DAB is not exclusively dependent on the current and voltage of its own PV string but also depends on the current and voltage of other PV strings. In a PV system consisting of N_{PV} PV strings, let k of these PV strings be shaded, producing voltage and currents of:

$$\begin{aligned} I_{\mathrm{PV}_j}\big|_{j=1,2,\ldots,k} &= I_{\mathrm{PV}_{\mathrm{sh}}}, \\ V_{\mathrm{PV}_j}\big|_{j=1,2,\ldots,k} &= V_{\mathrm{PV}_{\mathrm{sh}}} \end{aligned} \tag{3.17}$$

The remaining unshaded strings generate a current and a voltage of:

$$\begin{aligned} I_{\mathrm{PV}_j}\big|_{j=k+1,\ldots,N_{\mathrm{PV}}} &= I_{\mathrm{PV}_{\mathrm{un}}}, \\ V_{\mathrm{PV}_j}\big|_{j=k+1,\ldots,N_{\mathrm{PV}}} &= V_{\mathrm{PV}_{\mathrm{un}}} \end{aligned} \tag{3.18}$$

Considering Equations (3.16) — (3.18), the power processed by DAB converters connected to the shaded and unshaded PV strings are determined by Equations (3.19) and (3.20), respectively:

$$P_{\mathrm{DAB}_{\mathrm{sh}}} = \frac{(N_{\mathrm{PV}} - k) \cdot I_{\mathrm{PV}_{\mathrm{un}}} \cdot (V_{\mathrm{PV}_{\mathrm{un}}} - V_{\mathrm{PV}_{\mathrm{sh}}})}{\left((N_{\mathrm{PV}} - k) \cdot I_{\mathrm{PV}_{\mathrm{un}}} + k \cdot I_{\mathrm{PV}_{\mathrm{sh}}}\right)} \cdot I_{\mathrm{PV}_{\mathrm{sh}}} \tag{3.19}$$

$$P_{\mathrm{DAB}_{\mathrm{un}}} = \frac{k \cdot I_{\mathrm{PV}_{\mathrm{sh}}} \cdot (V_{\mathrm{PV}_{\mathrm{sh}}} - V_{\mathrm{PV}_{\mathrm{un}}})}{\left((N_{\mathrm{PV}} - k) \cdot I_{\mathrm{PV}_{\mathrm{un}}} + k \cdot I_{\mathrm{PV}_{\mathrm{sh}}}\right)} \cdot I_{\mathrm{PV}_{\mathrm{un}}} \tag{3.20}$$

Fig. 3.7 (a) and Fig. 3.8 (a), generated using Equation (3.19), depict the impact of voltage and current variations among PV strings on the processed power of DAB converters connected to shaded PV arrays. On the other hand, Fig. 3.7 (b) and Fig. 3.8 (b), based on Equation (3.20), illustrate the same effect on the processed power of DAB converters

connected to unshaded PV strings. It is important to note that in the figures, the sign of normalized powers indicates the direction of power flow: a positive sign signifies power transfer from the virtual bus to the PV string, while a negative sign indicates the opposite.

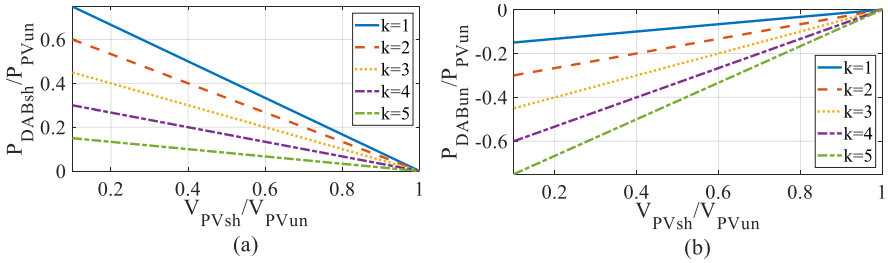

Figure 3.7.: Influence of voltage difference among PV strings on processed power of DAB converters (a) connected to the shaded PV strings, and (b) connected to the unshaded PV strings ($N_{PV} = 6$, $\frac{I_{PV_{sh}}}{I_{PV_{un}}} = 1$).

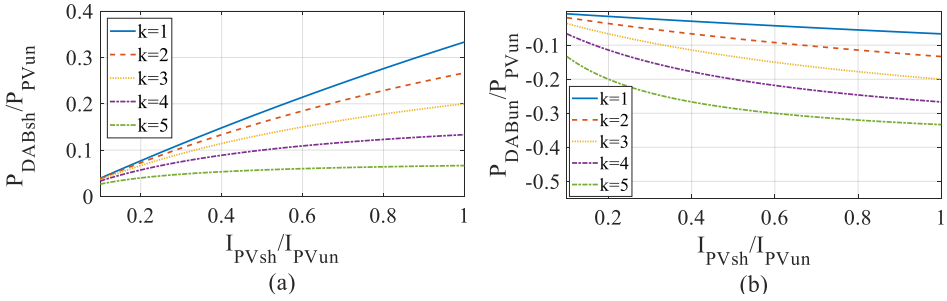

Figure 3.8.: Influence of current difference among PV strings on processed power of DAB converters (a) connected to the shaded PV strings (b) connected to the unshaded PV strings ($N_{PV} = 6$, $\frac{V_{PV_{sh}}}{V_{PV_{un}}} = 0.6$).

As previously discussed, the DPP architectures in PV systems are designed to reduce processed power as the severity of mismatch conditions decreases. When the difference between shaded and unshaded voltages approaches 0 ($\frac{V_{\mathrm{PV_{sh}}}}{V_{\mathrm{PV_{un}}}} \rightarrow 1$), it signifies a decrease in the severity of shading within the PV system. This reduction in shading severity leads to a decrease in both $P_{DAB_{sh}}$ and $|P_{\mathrm{DAB_{un}}}|$, as illustrated in Fig. 3.7.

As depicted in both Fig. 3.7 (a) Fig. 3.8 , an increase in the number of

shaded PV strings (k) consistently leads to a reduction in $P_{DAB_{sh}}$ and a concurrent increase in $|P_{\mathrm{DAB_{un}}}|$. This behavior is attributed to the main bus voltage. As the number of shaded PV strings rises, the influence of the shaded PV string voltage becomes more pronounced, causing main bus voltage to approach the shaded PV string voltage while moving further away from the unshaded PV string voltage. Consequently, given that P_{DAB_j} is proportional to the difference between the main bus voltage and the voltage of the jth PV string, as per Equation (3.15), $P_{DAB_{sh}}$ decreases, while $|P_{\mathrm{DAB_{un}}}|$ increases. Furthermore, as illustrated in Fig. 3.7 and Fig. 3.8, $P_{DAB_{un}}$ is negative, while $P_{DAB_{sh}}$ is positive. This emphasizes the power transfers from the unshaded PV strings to the virtual bus, while the shaded strings draw power from the virtual bus. Fig. 3.8 demonstrates an increase in current leads to higher processed power output for all DAB converters, whether connected to shaded or unshaded PV strings. To delve deeper into this observation, we can turn to Equation (3.6), which describes the balancing of the bus voltage as a weighted average of all PV strings' voltages, with the PV string currents serving as the weighting factors. This means that a PV string with a higher current exerts a more substantial influence on the bus voltage.

In scenarios where the voltages of PV strings remain constant, an increase in the current of shaded PV strings pushes the bus voltage closer to the voltage of the shaded PV string while simultaneously moving it further away from the unshaded PV strings' voltage. This initially might suggest that $P_{DAB_{sh}}$ decreases, while $|P_{\mathrm{DAB_{un}}}|$ increases. However, it is essential to recognize that the impact of increasing the shaded PV strings' current outweighs the effects of the mentioned phenomenon on $P_{DAB_{sh}}$. Thus, both $P_{DAB_{sh}}$ and $|P_{\mathrm{DAB_{un}}}|$ experience an increase.

To define the power rating of the converters, the worst-case practical scenario should be considered. The theoretical worst-case scenario occurs when $I_{PV_{sh}}$ equals $I_{PV_{un}}$ and $V_{PV_{sh}}$ equals 0, with k equal to 1. Considering Equation (3.19), the ratio of the DAB converters' power rating to the PV string's peak power, with the latter defining the power rating of FPP SLCs in multi-string architectures, is:

$$\frac{P_{\mathrm{DAB}}}{I_{\mathrm{PV_{un}}} \cdot V_{\mathrm{PV_{un}}}} = \frac{N_{\mathrm{PV}} - 1}{N_{\mathrm{PV}}} \tag{3.21}$$

Equation (3.21) reveals that when the PV string count is 2, 3, 4, or ∞, the power rating of DAB converters is 50%, 66%, 75%, and 100% of that of FPP converters, respectively for the theoretical worst-case scenario. However, this scenario is exceedingly stringent and rarely, if ever, occurs. Thus, DAB converters can be designed with power ratings as a fraction of the PV string's peak power, reducing both size and cost.

3.3.2. BL CONVERTERS

BL converters have distinct ratings compared to DAB converters, and determining their rating is a straightforward process. BL converters must continually provide a path for the current from their associated PV string, and this characteristic defines the current rating of the BL converters. Additionally, the voltage of the intermediate buses plays a role in determining the voltage rating of the components within the BL converters. Since there is flexibility in choosing the voltage of the intermediate buses, it becomes feasible to opt for a voltage lower than the PV string voltage. Consequently, the component rating of the BL converter can be lower than the PV strings rating, which defines the power rating of FPP SLCs.

3.4. DESIGN SLC'S VOLTAGE

Restricting the virtual bus and intermediate bus voltage to a fraction of the PV strings' voltage offers several advantages associated with a low voltage converter. However, it can lead to ineffective MPPT during severe shading scenarios since this voltage defines the SLC maximum voltage ($\pm V_{SLC_{max}}$). Fig. 3.9 illustrates five operational regions of PV2VB PDPP architecture, which analysis allows an understanding of the importance of selecting an appropriate virtual bus and intermediate bus voltage to ensure effective functionality.

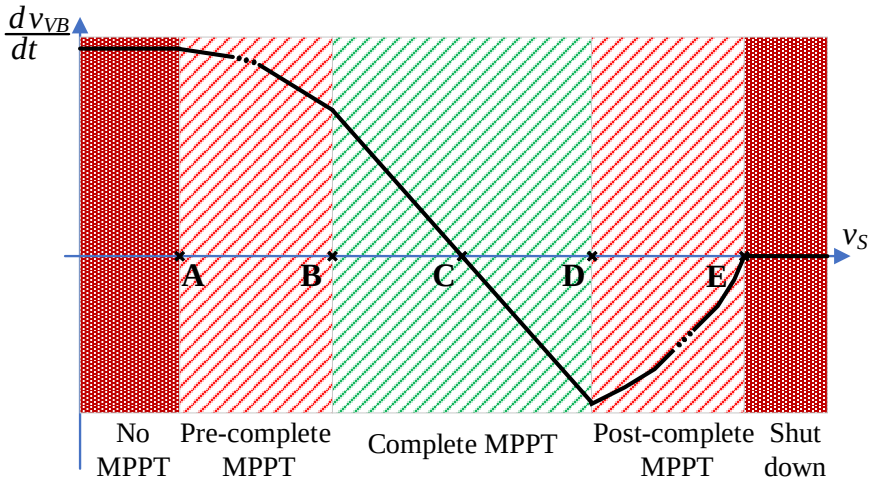

Figure 3.9.: Operational regions of the PV2VB PDPP architecture.

1) In region 1, called No MPPT, the main bus voltage falls within the range of:

$$0 \leq v_s < A = \left(V_{\mathrm{PV}_{\mathrm{MPP}_{\min}}} - V_{\mathrm{SLC}_{\max}}\right), \quad V_{\mathrm{PV}_{\mathrm{MPP}_{\min}}} > V_{\mathrm{SLC}_{\max}} \tag{3.22}$$

Where ($V_{\mathrm{PV}_{\mathrm{MPP}_{\min}}}$) is the minimum MPP voltage amongst all PV strings. Such a low v_s results in all SLCs operating at their maximum inverted voltage ($-V_{\mathrm{SLC}_{\max}}$). Therefore, none of the PV strings operate at their MPP, but instead, their voltages align with the voltage specified by the SLCs:

$$v_{\mathrm{PV}_i} = V_{\mathrm{SLC}_{\max}} + v_s \tag{3.23}$$

So PV strings operate within their constant current region on their I-V curves, continuously charging the virtual bus. Assuming a perfectly constant current, the instantaneous rate of change of the virtual bus voltage can be expressed as:

$$\frac{dv_{\mathrm{VB}}}{dt} = \frac{V_{\mathrm{SLC}_{\max}} \sum_{i=1}^{N_{\mathrm{PV}}} I_{\mathrm{SC}_{\mathrm{PV}_i}}}{C_{\mathrm{VB}} \cdot v_{\mathrm{VB}}} \tag{3.24}$$

where $I_{\mathrm{SC}_{\mathrm{PV}_i}}$ represents the short-circuit current of the i^{th} PV string. This indicates that the virtual bus voltage is consistently increasing, leading to a lack of equilibrium point in this region. Moreover, none of the PV strings are operating at their MPP.

2) As v_s increases and reaches point A, the architecture enters the region Pre-complete MPPT:

$$A = \left(V_{\mathrm{PV}_{\mathrm{MPP}_{\min}}} - V_{\mathrm{SLC}_{\max}}\right) \leq v_s < \left(V_{\mathrm{PV}_{\mathrm{MPP}_{\max}}} - V_{\mathrm{SLC}_{\max}}\right) = B \tag{3.25}$$

where $V_{\mathrm{PV}_{\mathrm{MPP}_{\max}}}$ is the maximum MPP voltage amongst all PV strings. At point A, the PV string with the lowest voltage initiates MPPT while maintaining its SLC voltage within the permitted range. In contrast, other PV strings still remain in the constant current region of their I-V curves. With the gradual increase of the main bus voltage, PV strings sequentially begin operating at their respective MPP.In this region, N_1 PV strings with MPP voltage lower than ($v_s - V_{SLC_{max}}$) achieve their MPP, while N_2 PV strings with MPP voltage higher than ($v_s - V_{SLC_{max}}$) remain in their constant current region of I-V curve. Simultaneously, the continuous charging of the virtual bus persists according to the following rate of change:

$$\frac{dv_{\mathrm{VB}}}{dt} = \frac{\sum_{i=1}^{N_1} \left((V_{\mathrm{MPP}_i} - v_s) \cdot I_{\mathrm{MPP}_i}\right) + V_{\mathrm{SLC}_{\max}} \cdot \sum_{i=1}^{N_2} I_{\mathrm{SC}_i}}{C_{\mathrm{VB}} \cdot v_{\mathrm{VB}}}, \quad N_1 + N_2 = N_{\mathrm{PV}} \tag{3.26}$$

In this region, although some PV strings may operate at their MPP, the absence of an equilibrium point persists due to the continuous charging of the virtual bus.

3) When v_s rises and stays within the following range:

$$B = \left(V_{\mathrm{PV}_{\mathrm{MPP}_{\max}}} - V_{\mathrm{SLC}_{\max}}\right) \leq v_s < \left(V_{\mathrm{PV}_{\mathrm{MPP}_{\min}}} + V_{\mathrm{SLC}_{\max}}\right) \tag{3.27}$$

The architecture enters in Complete MPPT region where all PV strings can work at their MPP. Based on the voltage of the main bus, the virtual bus can be charged or discharged by the following rate of change:

$$\frac{dv_{\mathrm{VB}}}{dt} = \frac{\sum_{i=1}^{N_{\mathrm{PV}}} \left((V_{\mathrm{MPP}_i} - v_s) \cdot I_{\mathrm{MPP}_i}\right)}{C_{\mathrm{VB}} \cdot v_{\mathrm{VB}}} \tag{3.28}$$

In this region, the equilibrium point, point C, where all strings work at their MPP and virtual bus voltage remains constant, exists.

4) In the Post-complete MPPT region, when the voltage surpasses point D:

$$D = \left(V_{\mathrm{PV}_{\mathrm{MPP}_{\min}}} + V_{\mathrm{SLC}_{\max}}\right) \leq v_s < \left(V_{\mathrm{PV}_{\mathrm{OC}_{\max}}} + V_{\mathrm{SLC}_{\max}}\right) \tag{3.29}$$

an increase in v_s results in a rise in the voltage of the PV string with the lowest MPP voltage, causing it to no longer operate at its MPP. With further escalation of v_s, more PV strings deviate from their MPP, some even reaching the open circuit state. In essence, within this region, N_3 PV strings reach the open circuit voltage, N_4 PV strings operate at $(v_s - V_{\mathrm{SLC}_{\max}})$, which is between their open circuit voltage and their MPP voltage, and N_5 PV strings operate at their MPP. Consequently, the virtual bus undergoes continuous discharge described by the rate:

$$\frac{dv_{\mathrm{VB}}}{dt} = \frac{-V_{\mathrm{SLC\_max}} \cdot \sum_{i=1}^{N_4} I_{\mathrm{PV}_i} + \sum_{i=1}^{N_5} \left((V_{\mathrm{MPP}_i} - v_s) \cdot I_{\mathrm{MPP}_i}\right)}{C_{\mathrm{VB}} \cdot v_{\mathrm{VB}}} \tag{3.30}$$

Where $N_3 + N_4 + N_5 = N_{PV}$. The PV strings at open circuit voltage no longer contribute to discharging the virtual bus, and this region has no equilibrium point.

5) Once the voltage exceeds point E, all PV strings operate at an open circuit, resulting in no current flow within the circuit (Shut-down region). Thus, there's no energy transfer through the circuit, leading to a zero change rate of the virtual bus voltage. The system displays all five regions only when point A is positive and points B, C, D, and E are sequentially positioned (0 < A < B <C < D < E). However, the focus and interest lie on the complete MPPT region, where an equilibrium point exists. Therefore, point D must be positioned to the right of Point B, which means that:

$$V_{\mathrm{SLC}_{\mathrm{max}}} \geq \frac{V_{\mathrm{PV}_{\mathrm{MPP}_{\mathrm{max}}}} - V_{\mathrm{PV}_{\mathrm{MPP}_{\mathrm{min}}}}}{2} \tag{3.31}$$

Based on Equation (3.31), it is possible to increase the MPPT range $[V_{PV_{MPP_{min}}}, V_{PV_{MPP_{max}}}]$ by increasing the virtual bus or intermediate bus voltage, since they define $V_{SLC_{max}}$. Furthermore, ensuring that the main bus voltage does not surpass point E is crucial. Failure to do so might lead to controller failure and an inability to reach the desired equilibrium point (point C). On the contrary, regarding the virtual bus's charging/discharging, no specific constraint exists on the minimum main bus voltage limit. Yet, for the central converter to function properly, its input voltage must exceed a certain threshold, imposing a minimum limit.

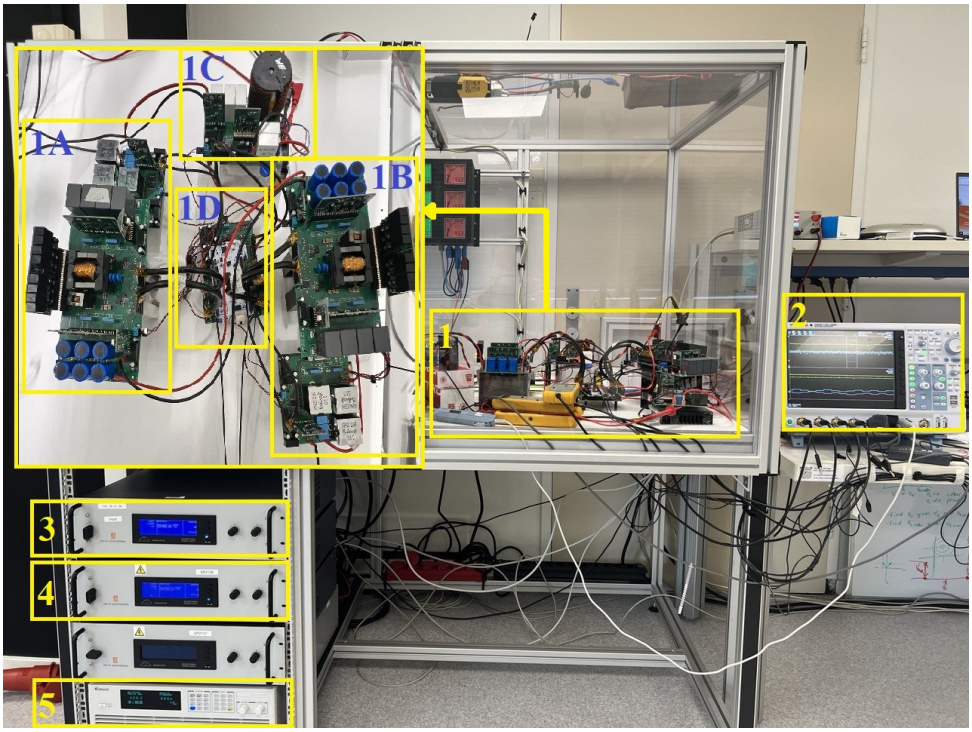

Figure 3.10.: Photograph of the PV2VB PDPP architecture prototype. 1A: SLC1, 1B: SLC2, 1C: Central converter, 1D: Micro controller, 2: YOKOGAWA DLM5038 oscilloscope, 3 and 4: SM1500-CP-30 Bi-directional DC Power Supplies, 5: 6210H-600S Programmable DC Power Supply.

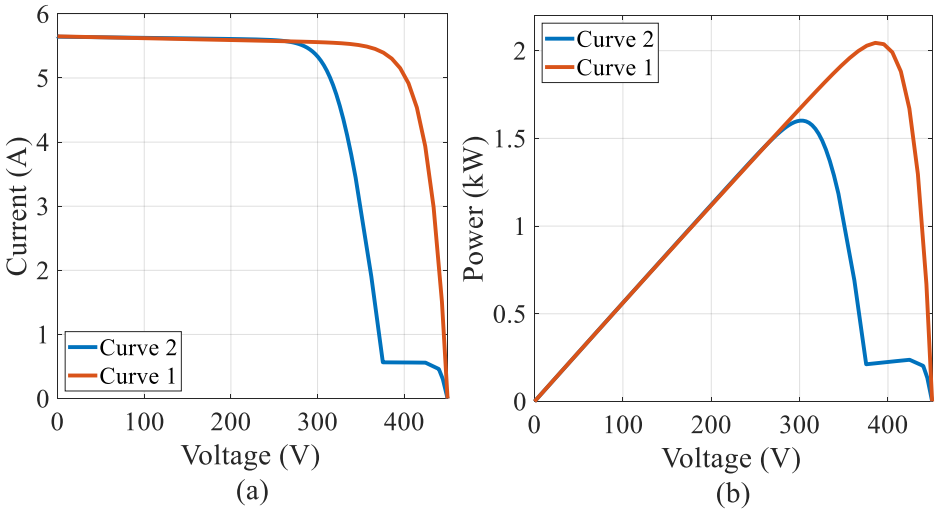

Figure 3.11.: PV string's (a) I-V curves (b) P-V curves used in the experiments.

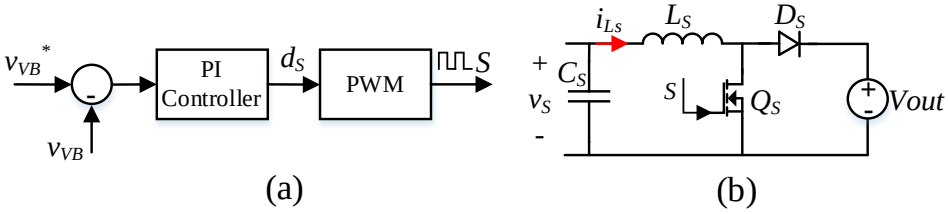

Figure 3.12.: The DC-DC stage of the central inverter (a) Block diagram of the controller (b) Topology.

3.5. EXPERIMENTAL RESULTS

This section highlights the ability of the proposed architecture to perform MPPT at the string level without processing the full power generated by the PV strings. While the proposed PV2VB PDPP architecture prototype is depicted in Fig. 3.10, its detailed electrical specifications and component values are summarized in Table 3.2. Indoor experiments utilized one 6210H-600S programmable DC supply as one PV string and two SM1500-CP-30 Bi-directional DC Power Supplies as the other PV string and the DC output voltage of the central converter (V_{out} in Fig. 3.12). Evaluation of the system's operation and performance was based on two different PV string curves shown in Fig. 3.12. I-V curve 1 represents a uniform PV string, while I-V curve 2 represents a PV string

operating under partially shaded conditions.

Table 3.2.: Electrical Specifications and Component Parameters of the System.

Category	Parameter	Symbol	Value
Electrical	PV System Rated Power	P_{sys}	3.9 kW
Specifications	Virtual Bus Voltage	V_{VB}	200 V
	MPP Voltage	V_{MPP}	390 V
	MPP Current	I_{MPP}	5 A
	SLC Rated Current	I_{SLC}	5 A
	SLC Rated Voltage	V_{SLC}	200 V
	Number of PV Strings	N_{PV}	2
	Switching Frequency	f_{sw}	100 kHz
Component	Virtual Bus Capacitance	C_{VB}	11.2 mF
Parameters	BL Inductance	L_{BL}	660 µH
	BL Capacitor	C_{BL}	3 µF
	DAB Leakage Inductor	L_{DAB}	22 µH
	Boost Inductor	L_S	510 µH
	Bus Capacitor	C_S	6.6 µF

3.5.1. STRING-LEVEL MPPT

In the proposed architecture, the central converter regulates the virtual bus voltage, while the SLCs track the MPP of the PV strings. Three scenarios were examined to evaluate system performance. In all scenarios, PV string 2 consistently exhibits I-V curve 1. On the other hand, PV string 1 transitions from generating I-V curve 1 to 2 in Scenario I, whereas in Scenario II, it reverts from I-V curve 2 to 1. Lastly, Scenario III was considered to verify the performance of the proposed PV2VB PDPP architecture under irradiance variations. In this scenario, both PV strings are subject to uniform conditions, hence they exhibit I-V curves similar to I-V curve 1 (with a single power peak). However, while PV string 2 consistently generates I-V curve 1, which represents the case of a PV string under 1000 W/m² irradiance, the irradiance over PV string 1 decreases over time to 700 W/m² and then to 500 W/m², before

increasing back to 1000 W/m². These scenarios represent more severe conditions than typically encountered in practice, as realistic shadowing patterns tend to vary at a slower rate.

The points A to E, explained in Section 3.4, vary depending on the operating point of the PV strings. For instance, if both PV strings generate according to Curve I, the approximate voltages at points A, B, C, D, and E will be 190 V, 190 V, 390 V, 590 V, and 650 V, respectively. However, if PV string 1 follows Curve II and PV string 2 follows Curve I, the voltages at points A, B, C, D, and E will be approximately 100 V, 190 V, 345 V, 500 V, and 650 V, respectively. These values are approximate, as power conversion losses have not been considered in the calculations of Section 3.4.

CENTRAL CONVERTER

Here, a boost converter among various possible topologies has been chosen as the central converter to regulate the virtual bus voltage via a PI controller with a sampling time of 60 ms (Fig. 3.12). It controls the virtual bus by controlling its input voltage, which is the main bus voltage. Fig. 3.13, Fig. 3.14, and Fig. 3.15 illustrate the central converter's capability to control the virtual bus voltage via the main bus voltage. In Fig. 3.13, Scenario I is depicted, demonstrating that after transitioning from I-V Curve 1 to Curve 2, the virtual bus reaches the desired value of 200 V in about 1 second. This is achieved by decreasing the main bus voltage according to Equation (3.6) after PV string 1 changes from I-V curve 1 to I-V curve 2.

On the other hand, upon implementing Scenario II, the main bus voltage increases and reverts to its initial state (see Fig. 3.14). Additionally, as depicted in Fig. 3.14 and expected from Equation (3.6), when both PV strings have identical MPP voltages (uniform condition), the main bus voltage closely matches that of the PV strings.

The irradiance level primarily influences the current generated by the PV string, exhibiting a linear relationship. In Scenario III, the irradiance over PV string 1 changes from 1000 W/m² to 700 W/m², then to 500 W/m², back to 700 W/m², and finally returns to 1000 W/m² at 0.6, 2.7, 4.9, and 6.7 seconds, respectively. As depicted in Fig. 3.15, the SLCs can track the MPP rapidly, while the central controller adjusts the virtual bus voltage more gradually. This indicates that the slower response of the central controller does not adversely affect the MPPT dynamic efficiency.

SLC CONVERTERS

A 1:1 conversion is feasible, allowing symmetrical implementation with low-voltage devices on both the primary and secondary sides of the DAB converter. The primary ports of DAB converters are connected in parallel. In turn, the distribution of the virtual bus capacitor at the inputs

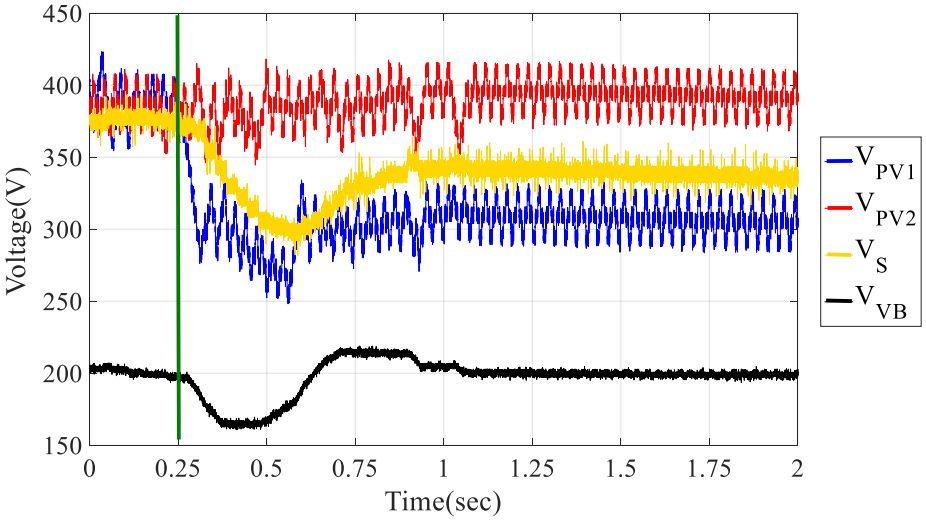

Figure 3.13.: Voltage waveforms. Scenario I: PV string 2 stays at I-V curve 1, whereas PV String 1 transitions from I-V curve 1 to I-V curve 2 at 0.25 s.

of the DAB converters is possible. Similar to industrial FPP multi-string inverters [24], in the proposed PV2VB PDPP architecture, SLCs can be integrated within the same inverter unit. Here, SLC_1 is connected to the partially shaded PV string, while SLC_2 is connected to the unshaded PV string. Fig. 3.16 shows that the DAB converter phase shift related to SLC_1 (DAB_1) is positive, indicating power is drawn from the virtual bus and transferred to PV string 1. Conversely, the phase shift of the DAB converter related to SLC_2 (DAB_2) is negative, signifying that PV string 2 injects power to the virtual bus, compensating for the power being drawn by string 1.

The task of finding the MPP of PV strings falls upon the BL converters. Here, a Perturb and Observe (P&O) algorithm with a perturbation period of 15 ms and a perturbation step size of a duty cycle of 3.5% is employed. Fig. 3.13, Fig. 3.14, and Fig. 3.15 prove the system's ability to independently find the MPP of both PV strings with the typical behavior of P&O MPPT. When transitioning from I-V curve 1 to I-V curve 2, the MPP voltage of PV string 1 shifts from 390 V to 300 V, while PV string 2 remains at the same voltage level, as no changes are affecting PV string 2. Moreover, as illustrated in Fig. 3.17, the BL converter associated with SLC1 exhibits a duty cycle higher than 0.5, indicating that, according to Equation (3.12), it provides a positive voltage to deliver power from the intermediate bus to the string. The other BL converter operates

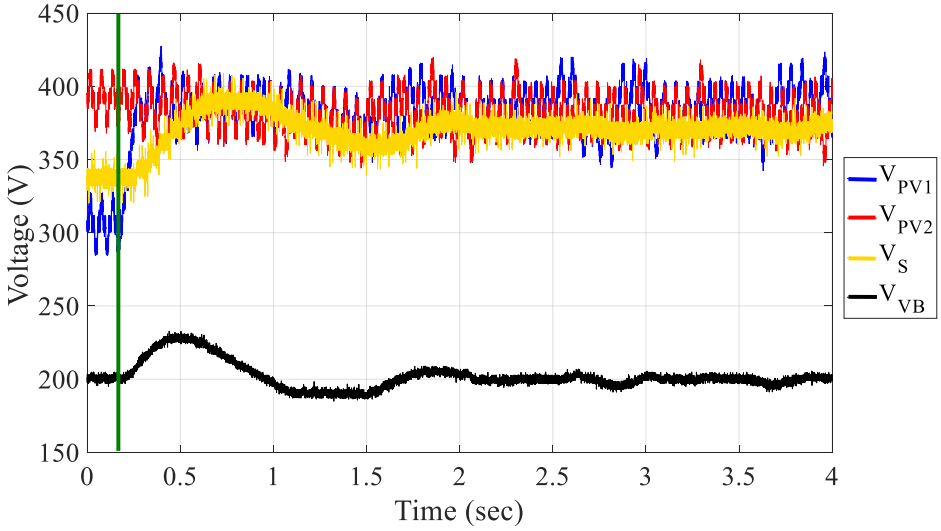

Figure 3.14.: Voltage waveforms. Scenario II: PV string 2 stays at I-V curve 1, whereas PV string 1 transitions from I-V curve 2 to I-V curve 1 at 0.2 s.

oppositely, transferring power from the unshaded PV string to the virtual bus. Thus, power can be efficiently exchanged with the virtual bus through the SLCs, ensuring stability at the desired voltage. Finally, Fig. 3.16 and Fig. 3.17 reveal that the switches of the DAB and BL converters only need to withstand the virtual bus voltage of 200 V, even though the system operates under 390 V.

3.5.2. DAB CONVERTERS PROCESSED POWER

To analyze the power processed by the DAB converters, the MPP voltage of PV string 2 is kept constant at 390 V while varying the MPP voltage of PV string 1 from 280 V to 390 V. The current of both PV strings is kept at 5.3 A. In another experiment, the MPP voltages of PV string 1 and 2 are kept constant at 300 V and 390 V, respectively, and the current of PV string 2 is kept at 5.3 A while varying the MPP current of PV string 1 from 1 A to 5.3 A. Fig. 3.18 shows that the power processed by the DAB1, as determined by experimental results, closely aligns with the values predicted by Equation (3.19). These results serve as validation for the equation and the explanations provided in Section III.

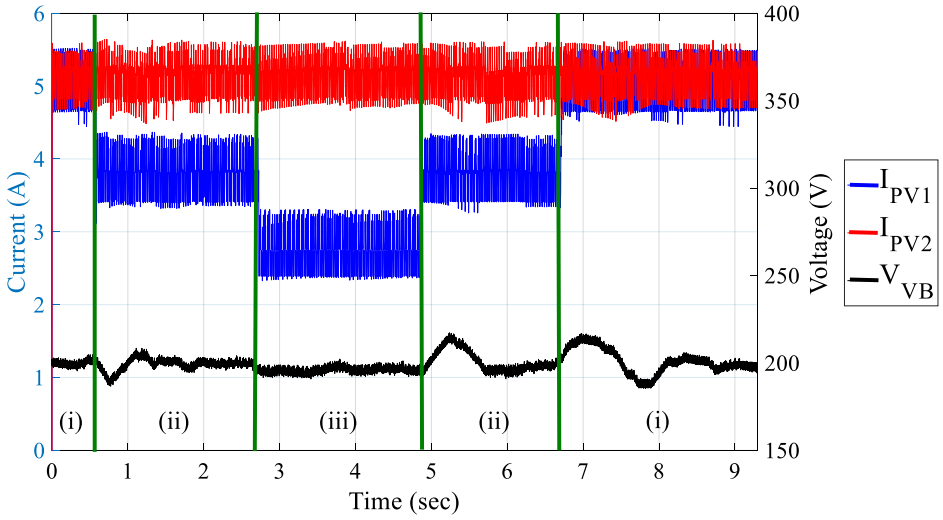

Figure 3.15.: Voltage and Current waveforms. Scenario III: PV string 2 stays at I-V curve 1, whereas PV string 1 transitions from I-V curve 1 with 1000 W/m² to 700 W/m² and then to 500 W/m², before increasing back to 1000 W/m². (i) 1000 W/m², (ii) 700 W/m², and (iii) 500 W/m².

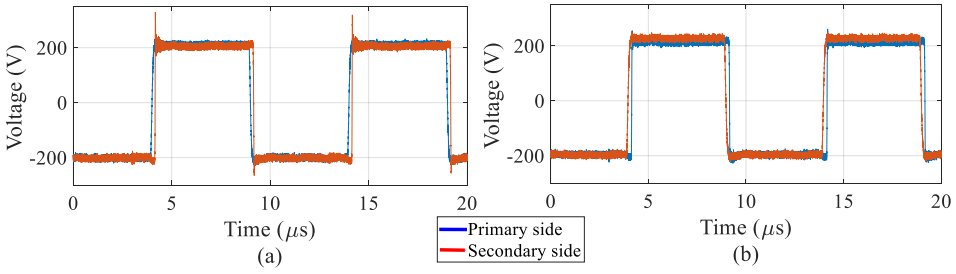

Figure 3.16.: DAB operation. (a) DAB_1 (b) DAB_2. Primary and secondary sides refer to the sides connected to the virtual bus and intermediate bus, respectively.

3.5.3. CONVERSION EFFICIENCY OF THE PV2VB PDPP ARCHITECTURE

The efficiency of the SLCs was measured under the following conditions: 200 V input (virtual bus) voltage, load voltage between -55 V and 55 V, and varying load current between 1 A and 5 A. Fig. 3.19 illustrates that, under these conditions, the average efficiency of a single SLC

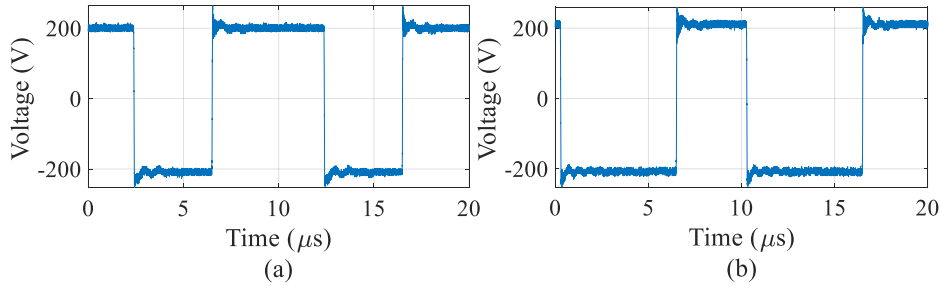

Figure 3.17.: The voltage of BL converters before LC filter (a) BL_1, and (b) BL_2.

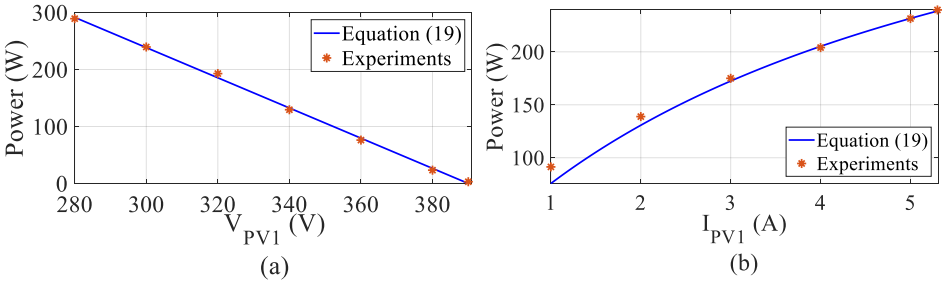

Figure 3.18.: Influence of (a) voltage difference between PV string 1 and PV string 2 ($I_{PV_1} = I_{PV_2} = 5.3\,A$, $V_{PV_2} = 390\,V$) and (b) current difference between PV string 1 and PV string 2 ($V_{PV_1} = 300\,V$, $V_{PV_2} = 390\,V$, $I_{PV_2} = 5.3\,A$) on processed power of DAB_1 (connected to the partially shaded PV string).

ranges from 84.4% to 95.1%. Similarly, the efficiency of the PV2VB PDPP architecture was measured, with the SLCs in the same conditions mentioned before. This is achieved by keeping PV string 2 constant at 390 V and 5.3A while adjusting the MPP voltage of PV string 1 from 280 V to 390 V, corresponding to the SLC voltage range of -55V to 55V. The averaged measured conversion efficiency of the PV2VB PDPP architecture shows an efficiency ranging from 96.4% to 97.2%. These results confirm that the system efficiency (excluding the power losses due to the MPPT algorithm) exceeds that of a single SLC. Notably, when no mismatches occur among PV voltage strings, deactivating the SLCs results in 99% system efficiency. The high system efficiency, combined with the other advantages of the PV2VB PDPP architecture, demonstrates significant potential to reduce the levelized cost of energy (LCOE). Ultimately, The central converter consistently adjusts the main

bus voltage to maintain a steady virtual bus voltage, irrespective of the number of PV strings. Each SLC operates independently to track the MPP of its respective PV string. Therefore, adding more PV strings does not introduce additional complexity from a control standpoint.

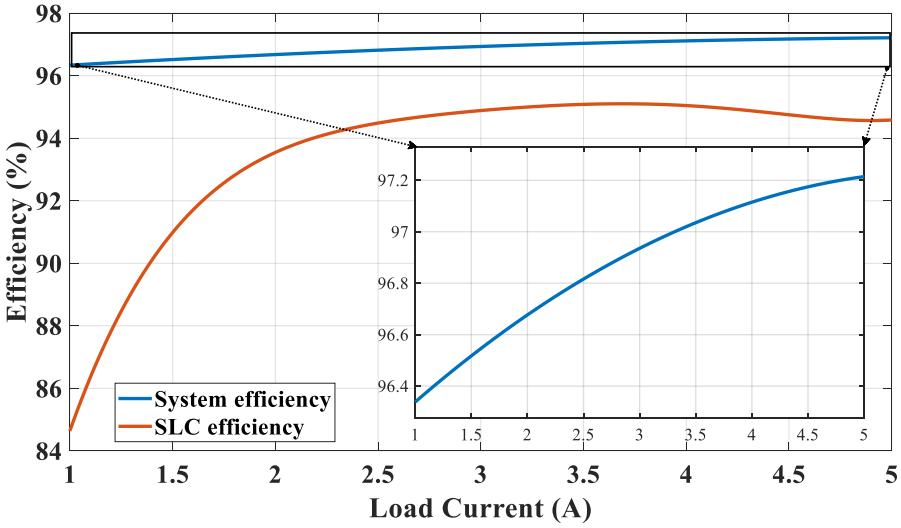

Figure 3.19.: Averaged system and a single SLC efficiency for load voltage from -55V to 55V as a function of load current.

3.6. CONCLUSION

This chapter presented a novel PV2VB PDPP architecture designed specifically for string-level MPPT. The innovation laid in the architecture where integrates SLCs with a capacitive virtual bus and a dual-loop control strategy. In this approach, SLCs operated in a swift inner loop for MPPT, while a central converter (e.g., boost converter) effectively regulated the virtual bus voltage. The static performance of both the central converter and SLCs was thoroughly analyzed, revealing the SLC requirement in being able to operate in the first and fourth quadrants of the V-I curve. To address this, the chapter suggested using a DAB converter followed by a BL converter. The study demonstrated that SLCs handle a fraction of the power generated by the PV strings and need to tolerate lower voltages. The experimental results confirmed the performance and theoretical explanations outlined in the sections detailing the MPPT of the proposed PV to virtual bus PDPP architecture at string level with efficiency from 96.4% to 99%.

REFERENCES

[1] A. Nazer, O. Isabella, and P. Manganiello. “PV to Virtual Bus Parallel Differential Power Processing Architecture for Photovoltaic Systems”. In: *IEEE Transactions on Industrial Electronics* (2024), pp. 1–11.

[2] A. Nazer, P. Manganiello, and O. Isabella. “A virtual bus parallel differential power processing configuration for photovoltaic applications”. In: *Mathematics and Computers in Simulation* 224, Part B (2024), pp. 49–62. issn: 0378-4754.

[3] C. Liu, Y. Zheng, and B. Lehman. “PV Panel to PV Panel Transfer Method for Modular Differential Power Processing”. In: *IEEE Transactions on Power Electronics* (2021), pp. 1–1.

[4] H. Jeong, H. Lee, Y. Liu, and K. A. Kim. “Review of Differential Power Processing Converter Techniques for Photovoltaic Applications”. In: *IEEE Transactions on Energy Conversion* 34.1 (2019), pp. 351–360.

[5] H. Zhou, J. Zhao, and Y. Han. “PV Balancers: Concept, Architectures, and Realization”. In: *IEEE Transactions on Power Electronics* 30.7 (2015), pp. 3479–3487.

[6] Y. D. Kwon, F. D. Freijedo, T. Wijekoon, and M. Liserre. “Series Resonant Converter-Based Full-Bridge DC–DC Partial Power Converter for Solar PV”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 12.2 (2024), pp. 1719–1729.

[7] N. Yadav *et al.* “Performance Evaluation of Step-Up/Down Partial Power Converters Based on Current-Fed DC-DC Topologies”. In: *IEEE Transactions on Industry Applications* (2024), pp. 1–13.

[8] N. Yadav, N. Hassanpour, A. Chub, A. Blinov, and D. Vinnikov. “Improved Maximum Power Point Tracking Algorithm for Step-Up/Down Partial Power Converters Operating Around Zero Partiality”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 12.2 (2024), pp. 1984–1994.

[9] N. A. Meineri, I. Santana, and I. G. Zurbriggen. “Ultra-Fast MPPT for Residential PV Systems With Low DC-Link Capacitance and Differential Power Processing”. In: *IEEE Transactions on Power Electronics* (2024), pp. 1–10.

[10] M. S. Agamy *et al.* “An Efficient Partial Power Processing DC/DC Converter for Distributed PV Architectures”. In: *IEEE Transactions on Power Electronics* 29.2 (Feb. 2014), pp. 674–686.

[11] J. W. Zapata, S. Kouro, G. Carrasco, and H. Renaudineau. “Step-up partial power dc-dc converters for two-stage PV systems with interleaved current performance”. In: *Energies* 11.2 (2018), p. 357.

[12] J. W. Zapata, S. Kouro, G. Carrasco, H. Renaudineau, and T. A. Meynard. “Analysis of Partial Power DC–DC Converters for Two-Stage Photovoltaic Systems”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 7.1 (2019), pp. 591–603.

[13] J. R. R. Zientarski, M. L. d. S. Martins, J. R. Pinheiro, and H. L. Hey. “Series-Connected Partial-Power Converters Applied to PV Systems: A Design Approach Based on Step-Up/Down Voltage Regulation Range”. In: *IEEE Transactions on Power Electronics* 33.9 (2018), pp. 7622–7633.

[14] H. Lee and K. A. Kim. “Comparison of photovoltaic converter configurations for wearable applications”. In: *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*. 2015, pp. 1–6.

[15] H. Lee and K. A. Kim. “Design Considerations for Parallel Differential Power Processing Converters in a Photovoltaic-Powered Wearable Application”. In: *Energies* 11.12 (2018).

[16] H. Lee and K. A. Kim. “Differential power processing converter design for photovoltaic wearable applications”. In: *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*. 2016, pp. 463–468.

[17] S. M. K. S and C. Chakraborty. “Differential Power-processing with Built-in Energy Storage for Multi-String Grid Interactive PV System”. In: *2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*. 2020, pp. 1–6.

[18] N. G. F. d. Santos, J. R. R. Zientarski, and M. L. d. S. Martins. “A Review of Series-Connected Partial Power Converters for DC–DC Applications”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 10.6 (2022), pp. 7825–7838.

[19] F. E. Aamri *et al.* “Stability Analysis for DC-Link Voltage Controller Design in Single-Stage Single-Phase Grid-Connected PV Inverters”. In: *IEEE Journal of Photovoltaics* 13.4 (2023), pp. 580–589.

[20] I. F. Kovačević, T. Friedli, A. M. Muesing, and J. W. Kolar. “3-D Electromagnetic Modeling of EMI Input Filters”. In: *IEEE Transactions on Industrial Electronics* 61.1 (2014), pp. 231–242.

[21] J. Espina, J. Balcells, A. Arias, and C. Ortega. “Common Mode EMI Model for a Direct Matrix Converter”. In: *IEEE Transactions on Industrial Electronics* 58.11 (2011), pp. 5049–5056.

[22] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman. “Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications”. In: *IEEE Transactions on Power Electronics* 32.12 (2017), pp. 9143–9178.

[23] H. Wang and et al. “Universal Phase-Shift Modulation Scheme and Efficiency Optimization for Modular Multiactive Bridge Converter”. In: *IEEE Transactions on Industrial Electronics* 71.7 (2024), pp. 7312–7321.

[24] SUNGROW. *Datasheet: SG250HX V1.5.4*. https://en.sungrowpower.com. Accessed: 5th December 2024. 2024.

4

PV2VB PDPP ARCHITECTURE (DYNAMIC ANALYSIS)

This chapter presents a comprehensive dynamic analysis by deriving a small-signal model of the PV2VB PDPP architecture based on its state space model. Subsequently, the corresponding transfer functions and frequency response are obtained, offering valuable insights into the dynamic behavior of the architecture. To validate the accuracy of the derived model, the frequency response will also be achieved by observing data from both PLECS simulation and experiment through system identification. Besides, this chapter discusses the design considerations of the discrete controllers' parameters for both virtual and intermediate bus voltages and studies the stability of the architecture.

Since this chapter contains numerous equations with multiple states, inputs, and outputs, precise symbolization is essential. To enhance readability, we have included a nomenclature in Table. 4.1 at the beginning of the chapter to assist the reader in case of any uncertainties.

Parts of this chapter have been published in [1].

Table 4.1.: List of Symbols and Definitions

Symbol	Definition
A	State matrix
B	Input matrix
C	Output matrix
C_{BL}	BL converter output LC filter capacitor
C_S	Main bus capacitor
D	Feedthrough matrix
$d_{BL}(t)$	BL converter switch status
$d_S(t)$	Central switch status
f_{clock}	PRBS clock frequency
f_{PRBS}	Frequency range of the generated PRBS
f_{sw}	SLCs and central converter switching frequency
$f_{PV}(v_{PV})$	PV current-voltage (I-V) characteristic equation
$i_{BL_L}(t)$	BL converter inductor current
$i_{DAB_L}(t)$	DAB converter's load current
$i_{PV}(t)$	PV string current
$i_{pri}(t)$	Primary side current of the DAB converter
$i_{sec}(t)$	Secondary side current of the DAB converter
L_{BL}	BL converter output LC filter inductor
L_{DAB}	DAB converter leakage inductor
L_S	Boost inductor
N_{PV}	Total number of PV strings
N_{PRBS}	PRBS length
N_T	Transformer turn ratio of the DAB converter
$p_{DAB}(t)$	Output power of DAB converter
$p_{in}(t)$	Total power generated by the PV strings

Table 4.1.: List of Symbols and Definitions (continued)

Symbol	Definition
$p_{\text{out}}(t)$	Output power of the system
$p_{\text{VB}}(t)$	Virtual bus power
r_{PV}	Small-signal resistance of a PV string
$S_{\text{v}}(\omega)$	PSD of noise (v)
$S_{\text{u}}(\omega)$	PSD of input (u)
$S_{\text{yu}}(\omega)$	CPSD of input (u) and output (y)
T_{IB}	Intermediate bus voltage PI controller sampling time
T_{MPPT}	Perturbation period of MPPT algorithm
T_{VB}	Virtual bus PI controller sampling time
$v_{\text{BL}_{\text{L}}}(t)$	BL converter inductor voltage
$v_{\text{IB}}(t)$	Intermediate bus voltage
V_{out}	Output voltage of boost converter
$v_{\text{PV}}(t)$	PV string voltage
$v_{\text{S}}(t)$	Main bus voltage
$v_{\text{SLC}_{\text{BF}}}(t)$	SLC's output voltage before LC filter
$v_{\text{SLC}_{\text{i}}}(t)$	SLC's output voltage
$v_{\text{VB}}(t)$	Virtual bus voltage
$z(t)$	A generic instantaneous variable
$\overline{z}(t)$	Moving average of $z(t)$ over one switching period
$\tilde{z}(t)$	Small-signal term of $\overline{z}(t)$
Z	Constant equilibrium value
$Z(s)$	Variable in Laplace domain
$\phi(t)$	Phase shift between the primary side and secondary side of the DAB converter

4.1. INTRODUCTION

In Chapter 3, an analysis of the steady-state operation of both the central converter and SLCs in the PV2VB PDPP architecture is provided, along with a description of their control objectives, duties, power ratings, and the design of the virtual bus voltage under steady-state conditions. However, in power electronic systems, the ability to deal with and control the consequences of unavoidable disturbances or errors that may drive circuits beyond their design specifications is crucial [2]. These perturbations encompass variations and uncertainties in source, load, or circuit parameters, disruptions in switching times, and – especially in PV systems – the MPPT algorithm. Hence, in the PV2VB PDPP architecture, precise control of both the SLCs and the central converter is crucial to maintain system robustness against disturbances and parameter variations and ensure optimal performance. Therefore, understanding the system's dynamic behavior through accurate modeling is essential for effective integration with other systems, proper component selection, and the exploration and development of new control methods [2, 3].

This chapter provides comprehensive system modeling and control design guidelines for the PV2VB PDPP architecture. Initially, a mathematical model of the architecture is derived using the state-space method and small-signal modeling in Section 4.2. This section details the process, starting with the large-signal model equations, followed by their linearization, and concluding with the development of the architecture's state-space model. System identification [4–6] is then performed using data from both PLECS simulations and experiments to verify the accuracy of the mathematical model in representing the system's behavior, as described in Section 4.3. The PV2VB PDPP architecture features two types of controllers: (i) the central controller, which adjusts the virtual bus voltage, and (ii) distributed controllers, which ensure the effective performance of the SLCs. Section 4.4 covers the requirements and guidelines for these controllers. Based on these requirements and the validated mathematical model, PI controllers are designed as examples. The design process focuses on critical parameters such as phase margin, bandwidth, and settling time. Section 4.5 presents experiments conducted on a prototype with two SLCs connected to separate PV strings, each rated at 2 kW, 400 V, and 5 A, to validate the controller designs.

4.2. STATE SPACE MODEL OF THE PV2VB PDPP ARCHITECTURE

A detailed analysis of the steady-state operation of the PV2VB DPP architecture can be found in Chapter 3. Here, the focus is on deriving the equations governing the operation of the PV strings, the

SLCs, and the central converter and creating a state-space model of the PV2VB PDPP architecture.

4.2.1. PV STRING MODEL

When addressing PV cells, a range of equivalent circuits of varying complexity and accuracy have been proposed in the existing literature. Among these, the single-diode model depicted in Fig. 4.1(a) is widely recognized as the prevalent large signal model for PV cells [7]. A PV string consists of several PV cells connected in series, so extending the model to PV strings is possible. This model inherently yields a nonlinear current-voltage equation for the PV string, which can be linearized around a specific operating point.

$$i_{PV}(t) = f_{PV}(v_{PV}(t)) \rightarrow \tilde{i}_{PV}(t) = \frac{-1}{r_{PV}} \cdot \tilde{v}_{PV}(t),\ r_{PV} = -\frac{1}{\frac{\partial f_{PV_i}}{\partial \tilde{v}_{PV}(t)}\Big|_{\tilde{v}_{PV}(t)=V_{PV}}}. \quad (4.1)$$

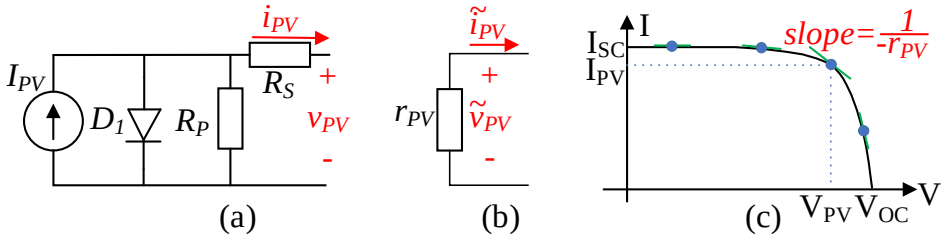

Figure 4.1.: A PV string (a) large signal model, (b) small signal equivalent circuit, and (c) exemplary I-V curve.

This linearized model is depicted in Fig. 4.1(b). Besides, as shown in Fig. 4.1(c), $(-\frac{1}{r_{PV}})$ is the slope of the PV string I-V curve at a given operating DC point (I_{PV} , V_{PV}), and it is assumed to be frequency-independent at sufficiently low frequencies [8].

4.2.2. AVERAGED LARGE SIGNAL MODEL OF THE POWER CONVERTERS

Given that SLCs and the central converter operate as PWM converters, averaging over a switching period is performed to derive the models of the power converters.

SLCS MODEL

In the PV2VB PDPP architecture in this study, the SLCs consist of a DAB converter followed by a BL converter (Fig. 3.4 (b)). The DAB converter's primary side connects to the virtual bus, while its secondary side is connected to the BL converter. An Intermediate Bus between the two converters decouples their operation. The second stage of the SLC topology is the BL converter, located between the PV string and the main bus. It provides both positive and negative output voltages necessary for PV strings to operate at MPP and ensures a current path for the PV string as discussed in Chapter 3.

For DAB converters, an averaged equivalent circuit and the respective mathematical model are introduced in [9] considering an SPS modulation (see Fig. 3.6). The average output power of a DAB converter can be expressed as [9]:

$$\overline{p}_{DAB}(t) = \frac{\overline{v}_{VB}(t) \cdot \overline{v}_{IB}(t) \cdot \varphi(t) \cdot (1 - 2 \cdot \varphi(t))}{N_T \cdot f_{sw} \cdot L_{DAB}}, \tag{4.2}$$

The average values of input and output currents over one switching period are used to describe the characteristics of the current. In a lossless DAB converter, the primary and secondary side power are equal and obtained by:

$$\overline{p}_{DAB}(t) = \overline{i}_{\text{pri}}(t) \cdot \overline{v}_{VB}(t) = \overline{i}_{\text{sec}}(t) \cdot \overline{v}_{IB}(t) \tag{4.3}$$

So, the average currents for both the primary and secondary sides will be:

$$\overline{i}_{pri}(t) = \frac{\overline{v}_{IB}(t) \cdot \varphi(t) \cdot (1 - 2 \cdot \varphi(t))}{N_T \cdot f_{sw} \cdot L_{DAB}}, \tag{4.4}$$

$$\overline{i}_{sec}(t) = \frac{\overline{v}_{VB}(t) \cdot \varphi(t) \cdot (1 - 2 \cdot \varphi(t))}{N_T \cdot f_{sw} \cdot L_{DAB}}. \tag{4.5}$$

The average load current of the DAB converter ($\overline{i}_{\text{DAB}_L}$) is determined by the behavior of the BL converter. When the BL converter operates in CCM, during the ON state of the BL converter switches, the current in the intermediate bus flows upwards (Fig. 3.5), drawing energy from the intermediate bus. Conversely, during the switch's OFF state, the current direction reverses, with energy being returned to the intermediate bus (Fig. 3.6). Consequently, the average current over a complete switching cycle can be calculated by:

$$\overline{i}_{\text{DAB}_L}(t) = \left(2 \cdot \overline{d}_{BL}(t) - 1\right) \cdot \overline{i}_{\text{BL}_L}(t) \tag{4.6}$$

By using Equations (4.4)–(4.6), it is possible to establish a large signal average model for the DAB converter, as illustrated in Fig. 4.2. To complete the SLC model, the BL converter must also be analyzed. As

far as the output voltage of the SLCs before the LC filter ($\overline{v}_{\mathrm{SLC}_{BF}}$) is concerned, no significant transients are present, except for the negligible effects during the switching period. Therefore, the BL converter can be modelled by its LC filter and a voltage source with an average voltage value equal to:

$$\overline{v}_{\mathrm{SLC}_{BF}}(t) = \left(2 \cdot \overline{d}_{BL}(t) - 1\right) \cdot \overline{v}_{IB}(t). \tag{4.7}$$

Equations (4.6) and (4.7) show that to let average power flow from the intermediate bus to the PV string, the BL converter's duty cycle must be above 0.5. If the duty cycle drops below this threshold, the power flow reverses, moving from the PV string to the intermediate bus. Since the direction of power flow is determined by the duty cycle (d_{BL}) and not by any structural change in the SLCs, the mathematical models remain consistent throughout both power flow directions. The ultimate step in obtaining an average large-signal equivalent circuit of SLCs involves combining the DAB and BL converters models, resulting in the circuit depicted in Fig. 4.2.

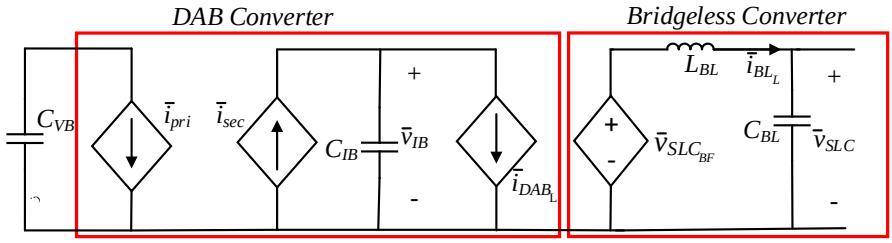

Figure 4.2.: Averaged large signal model of an SLC (a DAB followed by a BL converter).

The equivalent circuit of Fig. 4.2 can be used to obtain a state-space representation of the SLCs, with the state variables being $\overline{v}_{SLC}(t)$, $\overline{v}_{IB}(t)$, $\overline{i}_{\mathrm{BL}_L}(t)$, and the inputs being $\overline{d}_{BL}$, $\varphi(t)$, which control the operation of the switches in both DAB and BL converters. Noting that the average voltage of the i^{th} PV string $\overline{v}_{PV_i}(t)$ is equal to:

$$\overline{v}_{PV_i}(t) = \overline{v}_S(t) - \overline{v}_{\mathrm{SLC}_i}(t) \tag{4.8}$$

the state equations of the state-space model for the i^{th} SLC are:

$$\frac{\partial \overline{v}_{\mathrm{SLC}_i}(t)}{\partial t} = \frac{\bar{i}_{\mathrm{BL}_{L_i}}(t) - \bar{i}_{PV_i}(t)}{C_{BL}} = \frac{\bar{i}_{\mathrm{BL}_{L_i}}(t) - f_{PV_i}(\overline{v}_S(t) - \overline{v}_{\mathrm{SLC}_i}(t))}{C_{BL}}$$
$$= g_{1_i}(\bar{i}_{\mathrm{BL}_{L_i}}(t), \overline{v}_S(t), \overline{v}_{\mathrm{SLC}_i}(t)) \quad (4.9)$$

$$\frac{\partial \overline{v}_{\mathrm{IB}_i}(t)}{\partial t} = \frac{\overline{v}_{VB}(t) \cdot \varphi_i(t) \cdot (1 - 2 \cdot \varphi_i(t))}{N_T \cdot f_{sw} \cdot L_{DAB} \cdot C_{IB}} - \frac{(2 \cdot \overline{d}_{\mathrm{BL}_i}(t) - 1) \cdot \bar{i}_{\mathrm{BL}_{L_i}}(t)}{C_{IB}}$$
$$= g_{2_i}(\bar{i}_{\mathrm{BL}_{L_i}}(t), \overline{v}_{VB}(t), \varphi_i(t), \overline{d}_{\mathrm{BL}_i}(t)) \quad (4.10)$$

$$\frac{\partial \bar{i}_{\mathrm{BL}_{L_i}}(t)}{\partial t} = \frac{\overline{v}_{\mathrm{IB}_i}(t) \cdot (2 \cdot \overline{d}_{\mathrm{BL}_i}(t) - 1) - \overline{v}_{\mathrm{SLC}_i}(t)}{L_{BL}}$$
$$= g_{3_i}(\overline{v}_{\mathrm{SLC}_i}(t), \overline{v}_{\mathrm{IB}_i}(t), \overline{d}_{\mathrm{BL}_i}(t)) \quad (4.11)$$

CENTRAL CONVERTER MODEL

In order to establish a complete model for the architecture, it is necessary to consider the central converter equations in the state-space form. As a representative topology, a boost converter has been selected, whose state variables are $\bar{i}_{L_s}(t)$ and $\overline{v}_S(t)$, whereas $\overline{d}_s(t)$ is the input variable. It should be noted that the input current of the boost converter is the summation of the PV strings currents (Fig. 4.3). Ultimately, by formulating the relevant equations for both the switch-on and switch-off states and subsequently averaging them over a switching cycle, we can successfully derive the boost converter equations for the state-space model:

$$\frac{\partial \overline{v}_S(t)}{\partial t} = \frac{\sum_{i=1}^{N_{PV}} \bar{i}_{PV}(t) - \bar{i}_{L_s}(t)}{C_s} = \frac{\sum_{i=1}^{N_{PV}} f_{PV_i}(\overline{v}_S(t) - \overline{v}_{\mathrm{SLC}_i}(t)) - \bar{i}_{L_s}(t)}{C_s}$$
$$= g_4(\overline{v}_{\mathrm{SLC}_i}(t) \mid i = \{1 \ldots N_{PV}\}, \overline{v}_S(t), \bar{i}_{L_s}(t)) \quad (4.12)$$

$$\frac{\partial \bar{i}_{L_s}(t)}{\partial t} = \frac{\overline{v}_S(t) - V_{\mathrm{out}}(1 - \overline{d}_s(t))}{L_s} = g_5(\overline{v}_S(t), \overline{d}_s(t)) \quad (4.13)$$

Here, it is assumed that the dynamic behavior of $\overline{v}_{\mathrm{out}}$ is negligible and does not significantly influence the overall architecture dynamics. This assumption is based on two common scenarios. First, when the output

is connected to a DC grid, V_{out} is firmly regulated. Second, when the output is connected to an AC inverter stage, a large capacitor is typically used to decouple the dynamics of the AC inverter from the DC-DC stage. Therefore, for analysis in this thesis, it is considered a constant value (V_{out}).

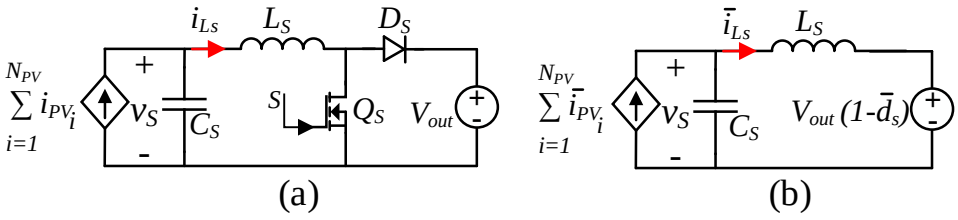

Figure 4.3.: Boost converter: (a) schematic, and (b) averaged large signal model.

4

VIRTUAL BUS

The architecture has one more state variable: $\overline{v}_{VB}$. To determine the related state equation, a KCL must be applied at the virtual bus node:

$$\frac{d\overline{v}_{VB}(t)}{dt} = \frac{\sum_{i=1}^{N_{PV}} \overline{v}_{\mathrm{IB}_i}(t)\cdot\varphi_i(t)\cdot(1-2\cdot\varphi_i(t))}{N_T\cdot f_{sw}\cdot L_{DAB}\cdot C_{VB}} = g_6\left(\overline{v}_{\mathrm{IB}_i}(t)\Big|_{i=1}^{N_{PV}}, \varphi_i(t)\Big|_{i=1}^{N_{PV}}\right) \tag{4.14}$$

4.2.3. STEADY-STATE SOLUTION

In small-signal analysis, the equations are linearized around an operating point, and the constant equilibrium values of the state or input variables appear in the model. Thus, when considering a desired operating point defined by parameters such as $V_{\mathrm{PV_{MPP}}_i}$, $I_{\mathrm{PV_{MPP}}_i}$, V_{out}, and V_{IB_i}, where $V_{\mathrm{PV_{MPP}}_i}$ and $I_{\mathrm{PV_{MPP}}_i}$ represent MPP voltage and current of i^{th} PV string, determining the equilibrium values for both state and input variables is crucial to finalize the model. These are achieved by:

$$V_S = \frac{\sum_{i=1}^{N_{PV}} V_{\mathrm{PV_{MPP}}_i}\cdot I_{\mathrm{PV_{MPP}}_i}}{\sum_{j=1}^{N_{PV}} I_{\mathrm{PV_{MPP}}_i}} \tag{4.15}$$

$$V_{\mathrm{SLC}_i} = V_S - V_{\mathrm{PV_{MPP}}_i}, \quad I_{\mathrm{BL}_{L_i}} = I_{\mathrm{PV_{MPP}}_i} \tag{4.16}$$

$$D_{\mathrm{BL}_i} = \frac{V_{\mathrm{SLC}_i}}{2\cdot V_{\mathrm{IB}}} + 0.5 \tag{4.17}$$

$$\Phi_i \cdot (1 - 2 \cdot \Phi_i) = \frac{V_{\text{SLC}_i} \cdot I_{\text{PV}_{\text{MPP}_i}} \cdot N_T \cdot f_{sw} \cdot L_{DAB}}{V_{VB} \cdot V_{\text{IB}_i}} \tag{4.18}$$

$$D_S = \frac{V_{\text{out}} - V_S}{V_{\text{out}}} \tag{4.19}$$

The averaged large-signal model developed in subsection 4.2.2 allows to calculate these equations by imposing all the derivatives equal to zero.

4.2.4. LINEARIZATION AND SMALL SIGNAL MODEL

The large-signal model derived in subsection 4.2.2 can be linearized around an operating point to derive a small signal model of the PV2VB PDPP architecture. The process of linearization involves expanding Equations (4.9)–(4.14) through a Taylor series expansion, focusing on linear terms.

$$\frac{\partial \tilde{v}_{\text{SLC}_i}(t)}{\partial t} = \frac{\partial g_{1_i}}{\partial \bar{v}_{\text{SLC}_i}(t)} \tilde{v}_{\text{SLC}_i}(t) + \frac{\partial g_{1_i}}{\partial \bar{i}_{\text{BL}_{L_i}}(t)} \tilde{i}_{\text{BL}_{L_i}}(t) + \frac{\partial g_{1_i}}{\partial \bar{v}_S(t)} \tilde{v}_S(t) \tag{4.20}$$

$$\frac{\partial \tilde{v}_{\text{IB}_i}(t)}{\partial t} = \frac{\partial g_{2_i}}{\partial \bar{i}_{\text{BL}_{L_i}}(t)} \tilde{i}_{\text{BL}_{L_i}}(t) + \frac{\partial g_{2_i}}{\partial \bar{v}_{VB}(t)} \tilde{v}_{VB}(t) + \frac{\partial g_{2_i}}{\partial \varphi_i(t)} \tilde{\varphi}_i(t) + \frac{\partial g_{2_i}}{\partial \bar{d}_{\text{BL}_i}(t)} \tilde{d}_{\text{BL}_i}(t) \tag{4.21}$$

$$\frac{\partial \tilde{i}_{\text{BL}_{L_i}}(t)}{\partial t} = \frac{\partial g_{3_i}}{\partial \bar{v}_{\text{SLC}_i}(t)} \tilde{v}_{\text{SLC}_i}(t) + \frac{\partial g_{3_i}}{\partial \bar{v}_{\text{IB}_i}(t)} \tilde{v}_{\text{IB}_i}(t) + \frac{\partial g_{3_i}}{\partial \bar{d}_{\text{BL}_i}(t)} \tilde{d}_{\text{BL}_i}(t) \tag{4.22}$$

$$\frac{\partial \tilde{v}_S(t)}{\partial t} = \sum_{i=1}^{N_{PV}} \frac{\partial g_4}{\partial \bar{v}_{\text{SLC}_i}(t)} \tilde{v}_{\text{SLC}_i}(t) + \frac{\partial g_4}{\partial \bar{v}_S(t)} \tilde{v}_S(t) + \frac{\partial g_4}{\partial \bar{i}_{L_s}(t)} \tilde{i}_{L_s}(t) \tag{4.23}$$

$$\frac{\partial \tilde{i}_{L_s}(t)}{\partial t} = \frac{\partial g_5}{\partial \bar{v}_S(t)} \tilde{v}_S(t) + \frac{\partial g_5}{\partial \bar{d}_s(t)} \tilde{d}_s(t) \tag{4.24}$$

$$\frac{\partial \tilde{v}_{VB}(t)}{\partial t} = \sum_{i=1}^{N_{PV}} \frac{\partial g_{6_i}}{\partial \bar{v}_{\text{IB}_i}(t)} \tilde{v}_{\text{IB}_i}(t) + \sum_{i=1}^{N_{PV}} \frac{\partial g_{6_i}}{\partial \varphi_i(t)} \tilde{\varphi}_i(t) \tag{4.25}$$

The coefficients of Equations (4.20)–(4.25) are obtained by taking the corresponding derivatives from Equations (4.9)–(4.14) (Find their elements coefficients in the Appendix A). The generalized form of a

linearized state space model, designed to extract the desired transfer function, can be expressed as follows:

$$\begin{cases} \frac{\partial \tilde{x}(t)}{\partial t} = A\tilde{x}(t) + B\tilde{u}(t) \\ \tilde{y}(t) = C\tilde{x}(t) + D\tilde{u}(t) \end{cases} \tag{4.26}$$

In PV2VB PDPP architectures, each SLC contributes three state variables, the central converter adds two state variables, and the last state variable is the virtual bus voltage $\tilde{v}_{VB}$.Thus, the system comprises a total of $(3N_{\text{PV}} + 3)$ state variables. Regarding input and output variables, each SLC encompasses two input variables ($\tilde{d}_{BL}$ and $\tilde{\varphi}(t)$), and the central converter introduces one input variable ($\tilde{d}_S$). Thus, the total number of input variables amounts to $(2N_{\text{PV}} + 1)$. The main control goal revolves around regulating the intermediate bus voltage of each SLC and virtual bus voltage, meaning there will be $(N_{\text{PV}} + 1)$ output variables. Therefore, the state, input, and output vectors are respectively defined as follows:

$$\tilde{x}(t) = \begin{bmatrix} \tilde{v}_{\text{SLC}_1}(t) \\ \tilde{v}_{\text{IB}_1}(t) \\ \tilde{i}_{\text{BL}_{L_1}}(t) \\ \vdots \\ \tilde{v}_{\text{SLC}_{N_{PV}}}(t) \\ \tilde{v}_{\text{IB}_{N_{PV}}}(t) \\ \tilde{i}_{\text{BL}_{L_{N_{PV}}}}(t) \\ \tilde{v}_S(t) \\ \tilde{i}_{L_S}(t) \\ \tilde{v}_{VB}(t) \end{bmatrix} \tag{4.27}$$

$$\tilde{u}(t) = \begin{bmatrix} \tilde{\varphi}_1(t) \\ \tilde{d}_{\text{BL}_1}(t) \\ \vdots \\ \tilde{\varphi}_{N_{PV}}(t) \\ \tilde{d}_{\text{BL}_{N_{PV}}}(t) \\ \tilde{d}_{\text{BL}_{PV}}(t) \\ \tilde{d}_S(t) \end{bmatrix} \tag{4.28}$$

$$\tilde{y}(t) = \begin{bmatrix} \tilde{v}_{\text{IB}_1}(t) \\ \vdots \\ \tilde{v}_{\text{IB}_{N_{PV}}}(t) \\ \tilde{v}_{VB}(t) \end{bmatrix} \tag{4.29}$$

Matrix $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, $\boldsymbol{D}$ can be obtained from Equations (4.20)–(4.25) (Find their elements in the Appendix A). Eventually, based on the linearized Equations (4.20)–(4.25), the small signal equivalent circuit of the architecture is shown in Fig. 4.4.

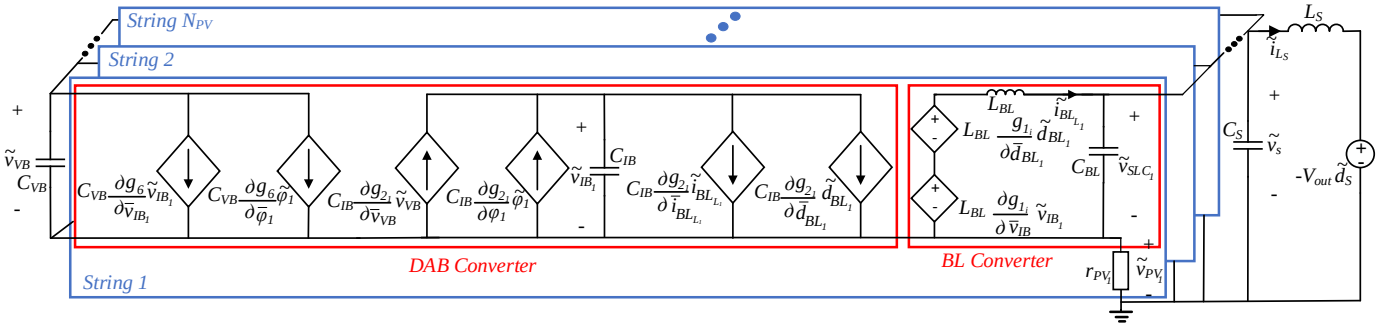

Figure 4.4.: Averaged small signal model of the PV2VB PDPP architecture.

4.3. SYSTEM IDENTIFICATION BASED ON OBSERVED DATA

In this section, the actual transfer function of the PV2VB PDPP architecture has been evaluated through system identification, aiming at validating the mathematical model developed in the previous section. System identification methods are usually divided into parametric [10] and nonparametric methods [11]. Here, the latter is more desired since for a fair validation the system must be considered as a black box where the dynamics are totally unknown. Nonparametric method includes: correlation analysis [4, 12], transient-response analysis [13], and frequency response, Fourier, or spectral analysis [11]. To obtain frequency insights—crucial for understanding system behavior and designing an effective controller—off-line spectral analysis [14] is utilized.

4.3.1. NON-PARAMETRIC SYSTEM IDENTIFICATION PROCEDURE

For system identification, after the system reaches a steady state, it is perturbed by an ad-hoc informative small signal. An informative input should be persistently exciting, i.e. it contains sufficiently diverse frequencies and excites desired modes and dynamics of the system [4, 5]. PRBS is a proper input for system identification since it contains a wide range of frequencies and is easy to implement. The PRBS is a periodic, deterministic, binary signal with white noise-like properties and is generated by a difference equation [5]. After PRBS is generated, it is possible to change it to two desired levels $\{-a, +a\}$, and the sequence is periodic with a length of:

A standard PRBS has a maximum frequency determined by its clock frequency and a bandwidth determined by its length. Therefore, its frequency range is as follows:

$$N_{\text{PRBS}} = 2^n - 1 \tag{4.30}$$

A standard PRBS has a maximum frequency determined by its clock frequency and a bandwidth determined by its length. Therefore, its frequency range is as follows:

$$\frac{f_{\text{Clock}}}{N_{\text{PRBS}}} < f_{\text{PRBS}} < \frac{f_{\text{Clock}}}{2} \tag{4.31}$$

Therefore, the clock frequency should be selected so that the PRBS signal can effectively excite the desired system dynamics. Additionally, the PRBS length must be long enough to provide reliable results, but overly long sequences can lead to challenges such as increased data complexity and extended test durations. For the PRBS magnitude $\{-a, +a\}$, a larger amplitude is beneficial to improve the signal-to-noise ratio when injected into the duty cycle of the central converter. However,

to ensure linear system behavior, the PRBS amplitude must remain low. Once the excitation input is applied to the system, the input/output data are collected and pre-processed to deal with drift, trends, offset, outliers, missing data, and so on. Afterwards, power spectral analysis is performed to identify the frequency response of the system.

For small-signal disturbances, a power converter can be regarded as a linear time-invariant discrete-time system, where the following relationships among the input PSD, output PSD, and CSPD exist [5, 12, 15]:

$$S_y(\omega) = |H(e^{i\omega})|^2 \cdot S_u(\omega) + S_v(\omega) \tag{4.32}$$

$$S_{yu}(\omega) = H(e^{i\omega}) \cdot S_u(\omega) \tag{4.33}$$

Where $H(e^{i\omega})$ is the input-to-output frequency response and, for discrete input and output signals, the CPSD and the cross-covariance R_{yu} between input and output are:

$$S_{yu}(\omega) = \sum_{m=-\infty}^{\infty} R_{yu}(m) \cdot e^{-i2\pi m\omega}, R_{yu}(m) = \sum_{n=1}^{\infty} \tilde{u}(m) \cdot \tilde{y}(n+m) \tag{4.34}$$

Whereas the PSDs and auto-covariance R_u and R_y of the two signals can be calculated as:

$$S_z(\omega) = \sum_{m=-\infty}^{\infty} R_z(m) \cdot e^{-i2\pi m\omega}, R_z(m) = \sum_{n=1}^{\infty} \tilde{z}(m) \cdot \tilde{z}(n+m) \tag{4.35}$$

Where z is either the input signal u or the output signal y. The estimates are then formed as:

$$H(e^{i\omega}) = \frac{S_{yu}(\omega)}{S_u(\omega)}, S_v(\omega) = S_y(\omega) - \frac{|S_{yu}(\omega)|^2}{S_u(\omega)} \tag{4.36}$$

Thus, in the spectral analysis, by using post-processed measured samples of both input and output, input and output PSDs and their CPSD are calculated by Equations (4.32)–(4.35). Afterward, the transfer function of the system is estimated using Equation (4.36).

Note that here, (i) system identification is performed in an open loop, (ii) the PRBS signal is generated by the *idinput()* function in MATLAB, and (iii) the non-parametric identification procedure presented above is applied through the *spafdr()* function in MATLAB.

4.3.2. VALIDATION THROUGH CIRCUIT SIMULATIONS

The first validation of the model has been performed through PLECS simulations. A PV2VB PDPP architecture with specification shown in Table. 3.2 has been simulated in PLECS. The system initially operates in a closed-loop mode until it achieves steady-state conditions with both PV strings at their MPPs (Table. 4.2). Then, the architecture transitions to an open-loop mode. During this phase, a PRBS signal is added to the duty cycle of the central converter, and the virtual bus voltage is measured. The PRBS signal parameters are presented in Table. 4.3 and have been chosen based on the considerations discussed in subsection 4.3.1. The $D_S(s)$ to $V_{VB}(s)$ transfer function has been evaluated using the non-parametric identification procedure presented above, and the Bode plots are shown in Fig. 4.5. Using the same procedure, a PRBS signal with amplitudes of {-0.004, 0.004} is applied to the phase shift of each DAB converter, one at a time. The $\Phi_S(s)$ to $V_{IB_i}(s)$ transfer function is then evaluated, and the Bode plots are shown in Fig. 4.6.

Table 4.2.: Operating Point for System Identification.

Symbol	Value	Symbol	Value	Symbol	Value
$V_{\mathrm{PV}_{\mathrm{MPP}_1}}$	267 V	$I_{\mathrm{PV}_{\mathrm{MPP}_1}}$	5.3 A	V_{IB_1}	200 V
$V_{\mathrm{PV}_{\mathrm{MPP}_2}}$	400 V	$I_{\mathrm{PV}_{\mathrm{MPP}_2}}$	5.3 A	V_{IB_2}	200 V
V_{out}	450 V	V_{VB}	200 V		

Table 4.3.: PRBS Signal Parameters.

Parameter	Symbol	PLECS Simulation	Experiment
Clock frequency	f_{Clock}	50 kHz	100 Hz
Length	N_{PRBS}	131071	2047
Amplitude (central converter)	a_{d_S}	$\{-0.01, 0.01\}$	$\{-0.015, 0.015\}$
Amplitude (DAB converter)	$a_{\phi_{\mathrm{DAB}}}$	$\{0.004, 0.004\}$	$\{-0.001, 0.001\}$

The architecture with two PV stings has nine state variables, which lead to nine poles. As shown in Fig. 4.5, the $D_S(s)$ to $V_{VB}(s)$ transfer function has three zeros and nine poles; moreover, it is possible to identify on the Bode plot two dominant poles defining the dynamic of

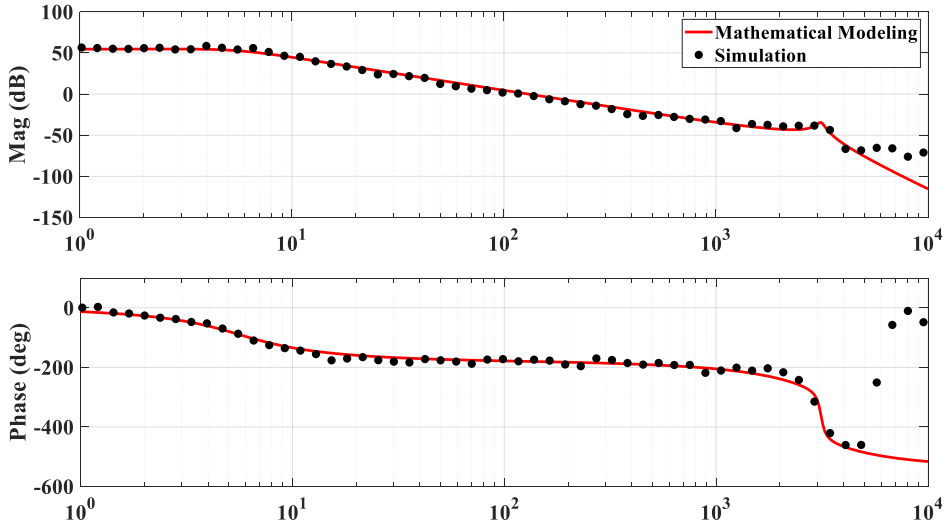

Figure 4.5.: $D_S(s)$ to $V_{VB}(s)$ transfer function. The input used for system identification is a two-period 17-bit PRBS with clock frequency of 50 kHz.

the system. On the other hand, Fig. 4.6 shows that $\Phi_S(s)$ to $V_{IB_i}(s)$ transfer functions at high frequencies resemble those of independent DAB converters [16], with the zeros located very close to the poles, effectively canceling each other out. This indicates that the virtual bus and intermediate bus capacitors are sufficiently large to decouple the performance of the DAB converters from other parts of the architecture. The differences between the Bode plots of DAB1 and DAB2 arise from their different operating points. While DAB1 transfers power from the virtual bus to the intermediate bus, DAB2 transfers power from the intermediate bus to the virtual bus.

Fig. 4.5 and Fig. 4.6 validate the mathematical model presented in section II. Indeed, the Bode plot was estimated from PLECS simulations through system identification (dots), and the one was calculated from the mathematical model (solid lines). Discrepancies between the mathematical model and simulation results for the $D_S(s)$ to $V_{VB}(s)$ transfer function appear at frequencies above $0.05 \cdot f_{sw}$. This is due to the function's strong low-pass characteristic (resulting in nearly -70 dB attenuation), combined with the limited duty cycle variation {-0.01, 0.01} and significant attenuation. As a result, the simulation struggles to capture high-frequency dynamics above $0.05 \cdot f_{sw}$. Nevertheless, all system poles and zeros, and the system's overall dynamic behavior, are accurately captured within this frequency range of $0.05 \cdot f_{sw}$.

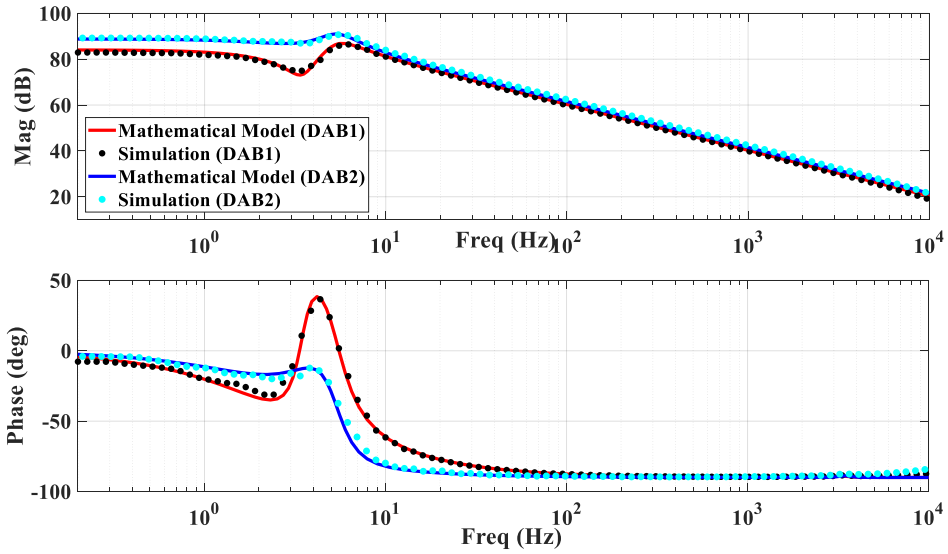

Figure 4.6.: $\Phi_S(s)$ to $V_{IB_i}(s)$ transfer functions. The input used for system identification is a two-period 17-bit PRBS with clock frequency of 50 kHz.

4.3.3. EXPERIMENTAL VALIDATION

Similar to the steady-state experiments presented in Chapter 3, the indoor experiments utilized one 6210H-600S programmable DC power supply to emulate one PV string, and two SM1500-CP-30 bidirectional DC power supplies to emulate the other PV string and the DC output voltage of the central converter (V_{out} in Fig. 3.12). Additionally, to enhance the stability and maintain a more constant V_{out}, extra capacitors were added at that point.

The digital controller was implemented using an STM32H723 advanced Arm®-based 32-bit MCU (see Fig. 3.10 in Chapter 3). PRBS signal is applied by the microcontroller and was injected to the boost duty cycle. Then, the virtual bus voltage was measured and collected by a YOKOGAWA DLM5038 oscilloscope. Although the microcontroller includes PI controllers for closed-loop output voltage regulation, the experiments for system identification were conducted in an open loop. The input and output data collected by the oscilloscope were transmitted to a computer for offline processing in the MATLAB/Simulink environment. The architecture parameters and the system's operating point remain the same as in the PLECS simulation example in Table. 3.2 (Chapter 3) and Table. 4.2, but the PRBS parameters are different (Table. 4.3).

The spectral analysis method described in subsection 4.3.1 is used to

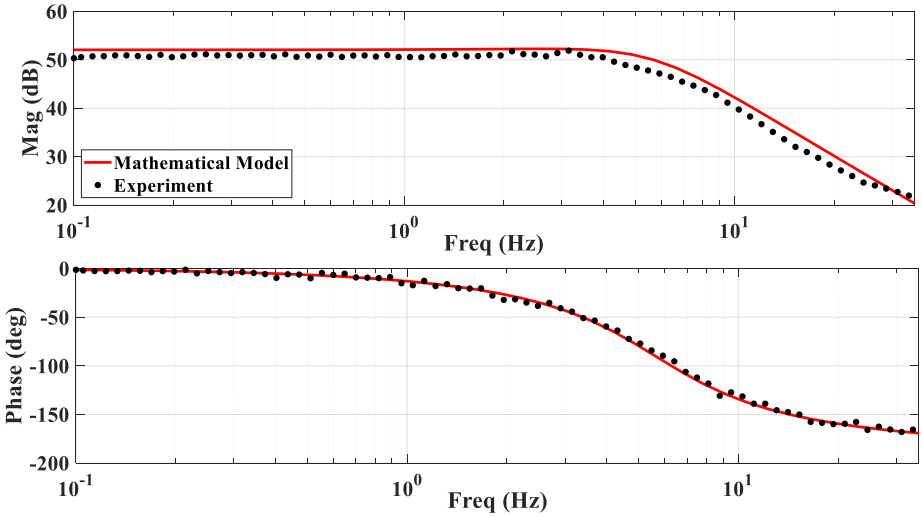

Figure 4.7.: $D_S(s)$ to $V_{VB}(s)$ transfer function. The input used for system identification is a two-period 11-bit PRBS with clock frequency of 100 Hz.

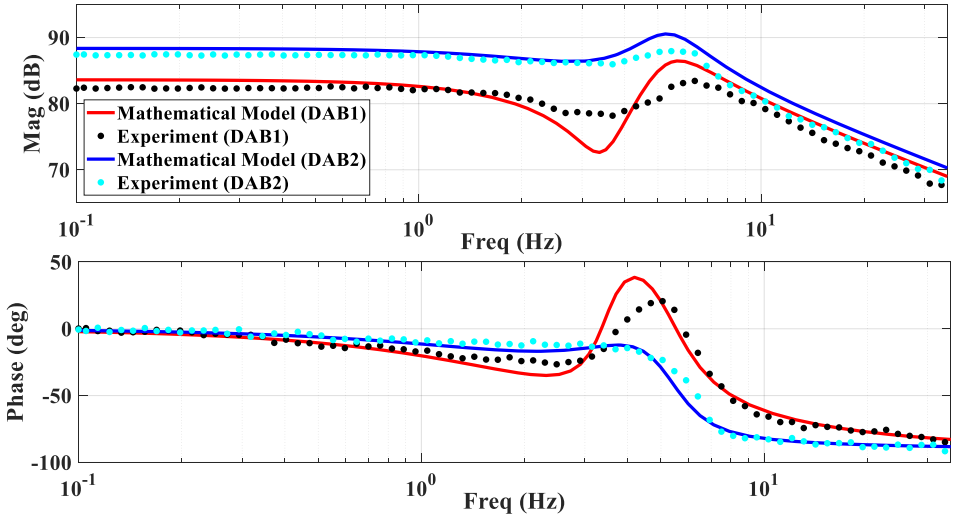

Figure 4.8.: $\Phi_S(s)$ to $V_{IB_i}(s)$ transfer functions. The input used for system identification is a two-period 11-bit PRBS with a clock frequency of 100 Hz.

identify the $D_S(s)$ to $V_{VB}(s)$ transfer function of the architecture. The PRBS was stored in the microcontroller and injected into the duty cycle of the central converter. Using the same procedure, the Bode plots of the $\Phi_S(s)$ to $V_{IB_i}(s)$ transfer functions were obtained experimentally. Fig. 4.7 and Fig. 4.8 compare the frequency response obtained from the mathematical model with the experimental results from system identification. A small discrepancy exists between the experimental results and the mathematical model, likely due to (i) PV emulator limitations, (ii) the simplified mathematical model, (iii) component tolerances, (iv) differential probe attenuation, or a combination of these factors. However, the analysis shows a good alignment between responses across the tested frequency range, validating the proposed mathematical model of the PV2VB PDPP architecture. Note that, due to their slow transient response, PV emulators cannot accurately represent PV strings at high frequencies, limiting the experimental results to less than 50 Hz. However, for DAB converters, the experimental results (Fig. 4.8) effectively capture the transition band, which is the critical part of the Bode plot. Additionally, as discussed in Section 4.4, for the $D_S(s)$ to $V_{VB}(s)$ transfer function (Fig. 4.7), the low-frequency band is the most important for controller design.

In the PV2VB PDPP architecture's normal operation, tracking the MPP of PV strings is crucial and achieved via MPPT algorithms. The widely used P&O algorithm adjusts the duty cycle of BL converters, causing periodic perturbations in the PV string's operating point at regular intervals, known as the perturbation period. These perturbations induce oscillations on the virtual bus, which an 11.2 mF virtual bus capacitor can mitigate in the proposed prototype. However, this capacitor attenuates frequency content in its voltage response to the PRBS signal and decreases the signal-to-noise ratio. Thus, although for system identification, a 1.2 mF capacitor has been utilized at the virtual bus the controllers are designed for a virtual bus capacitance of 11.2 mF in Section 4.4.

4.4. CONTROLLER DESIGN CONSIDERATIONS

Fig. 4.9 illustrates the PV2VB PDPP architecture alongside its control structures. In this architecture, the central converter regulates the virtual bus voltage by adjusting the main bus voltage, while the primary responsibility of the SLCs is to track the MPP of the PV strings. Although the BL converter handles MPP tracking, fluctuations in the intermediate bus voltages can adversely affect the performance of MPP tracking. Thus, the DAB converter must effectively regulate these intermediate bus voltages to ensure stable and efficient operation. Considering a search-based MPPT algorithm like P&O, the system inherently has two categories of feedback (error-based) control loops: one central

converter controller and N_{PV} DAB converter controllers (Fig. 4.9). The first control loop is the central converter controller aiming to maintain the voltage of the virtual bus at the desired level by controlling the duty cycle of the boost converter. The second controller governs the DAB converters, focusing on regulating intermediate bus voltages through the DAB converters' phase shifts. Thus, two types of transfer functions are our interest: (i) $D_S(s)$ to $V_{VB}(s)$ (s) and (ii) $\Phi_S(s)$ to $V_{IB_i}(s)$:

$$G_{V_{VB}/D_S}(s) = \frac{V_{VB}(s)}{D_S(s)}\Bigg|_{\begin{cases}\Phi_j(s)=0, & j=1,\ldots,N_{PV}\\ D_{BL_j}(s)=0, & j=1,\ldots,N_{PV}\end{cases}} \tag{4.37}$$

$$G_{i_{V_{IB_i}/\Phi_i}}(s) = \frac{V_{IB_i}(s)}{\Phi_i(s)}\Bigg|_{\begin{cases}\Phi_j(s)=0, & j=1,\ldots,N_{PV},\, j\neq i\\ D_{BL_j}(s)=0, & j=1,\ldots,N_{PV}\\ D_S(s)=0\end{cases}} \tag{4.38}$$

Both voltage control loops are essential for maintaining the voltages within specified limits, ensuring system stability, and improving system performance. Here an indirect technique has been used for designing discrete PI controllers; so initially, the continuous-time controllers are designed in the s-domain by using MATLAB SISOtool. Then, based on the continuous-time controller, the discrete-time controller is calculated by Tustin transformation.

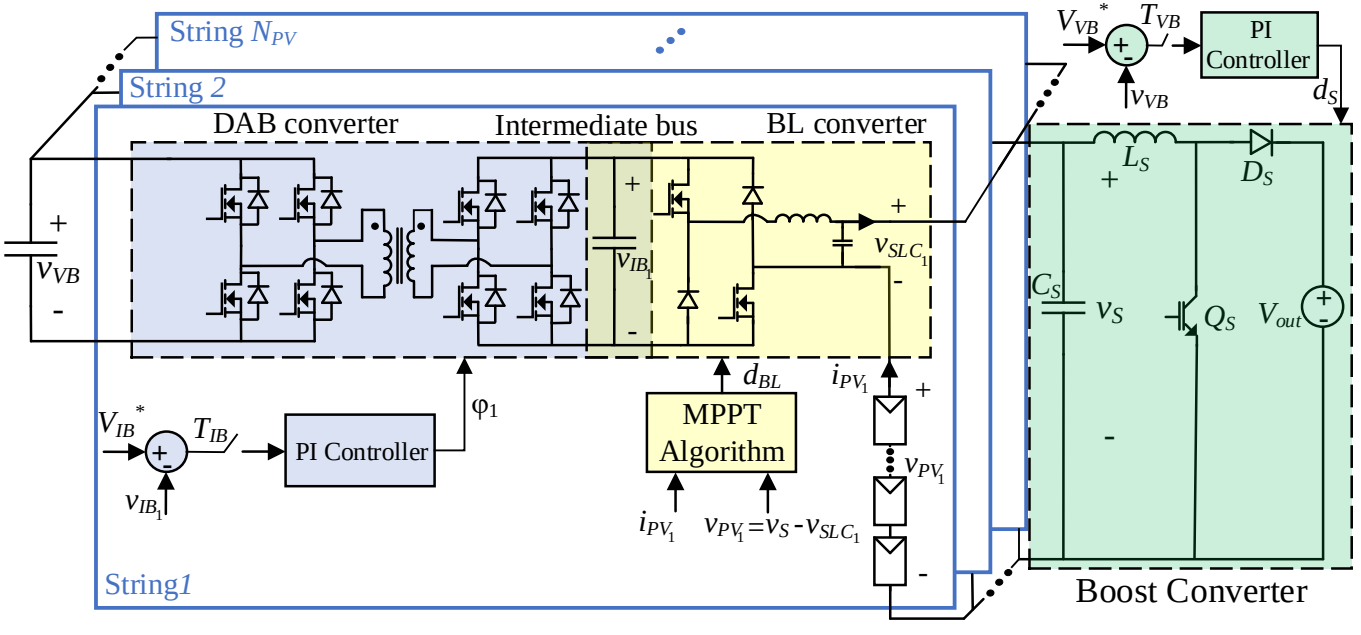

Figure 4.9.: PV2VB PDPP architecture with its control loop block diagrams.

4.4.1. CENTRAL CONVERTER CONTROLLER

To prevent interference between the central controller and to enable the MPPT algorithms to autonomously seek the MPP of the PV string, it is preferable to increase the sampling time of the central PI controller to minimize its interference with the MPPT algorithm as follow:

$$T_{VB} = 4 \cdot m \cdot T_{MPPT} \qquad \text{where } m = 1, 2, \ldots \tag{4.39}$$

However, if the sampling period is too long, the discrete-time PI controller may not yield satisfactory results. In practical terms, for a broad range of systems, the sampling period is typically chosen to be at most half of the slowest time constant [17]. The slowest time constant in the architecture is 300 ms, with parameters outlined in Table. 3.2 (except for C_{VB}, which is 11.2 mF) and a 15 ms for the perturbation period of the MPPT algorithm T_{MPPT} has been chosen. Therefore, a sampling time of 60 ms, which is equal to 4 times T_{MPPT}, is selected for the central controller. In this chapter, the criteria for designing the PI controller parameters of the central converter are phase margin and bandwidth. A phase margin of approximately 60 degrees is considered for the compensated system to ensure a reasonable stability margin and mitigate the effects of uncertainties and variations – such as dynamic resistance of PV strings r_{PV} – in the system. Additionally, to achieve satisfactory accuracy, the sampling time of the discrete-time PI controller must be 20 times faster than the highest bandwidth frequency [17]. Hence, a bandwidth of 1 Hz is chosen for designing the central converter's PI controller.

4.4.2. DAB CONVERTERS CONTROLLERS

In contrast to the central converter controller, there is no specific lower limit for the sampling time of DAB converters. Hence, the sampling frequency of the PI controller can be set as fast as the switching frequency of the DAB converter, which is 100 kHz, to enhance response time and reduce phase lag in the system. The criteria for designing the DAB converters PI controllers are phase margin and settling time. It is preferable for the settling time of the intermediate bus voltages to be lower than the perturbation period of the MPPT algorithm ($T_{IB} < T_{MPPT}$) to minimize interference. As for the central converter PI controller, a phase margin of approximately 60 degrees is considered. Lastly, the parameters of the controllers are designed for the architecture with the parameters outlined in Table. 3.1 (except for C_{VB}, which is 11.2 mF) and the operating point specified in Table. 4.2. The controllers' parameters are shown in Table. 4.4.

Table 4.4.: Controllers Parameters

Parameter	Symbol	Value
Central Controller		
Sampling Time	T_{VB}	60 ms
Proportional Coefficient*	$K_{p_{VB}}$	0.003
Integral Coefficient	$K_{I_{VB}}$	0.015
DAB Controllers		
Sampling Time	T_{IB}	10 µs
Proportional Coefficient	$K_{p_{IB}}$	0.0005
Integral Coefficient	$K_{I_{IB}}$	0.01

* $K_p + \frac{K_I}{s}$, *where* K_p *is the Proportional Coefficient and* K_I *is the Integral Coefficient.*

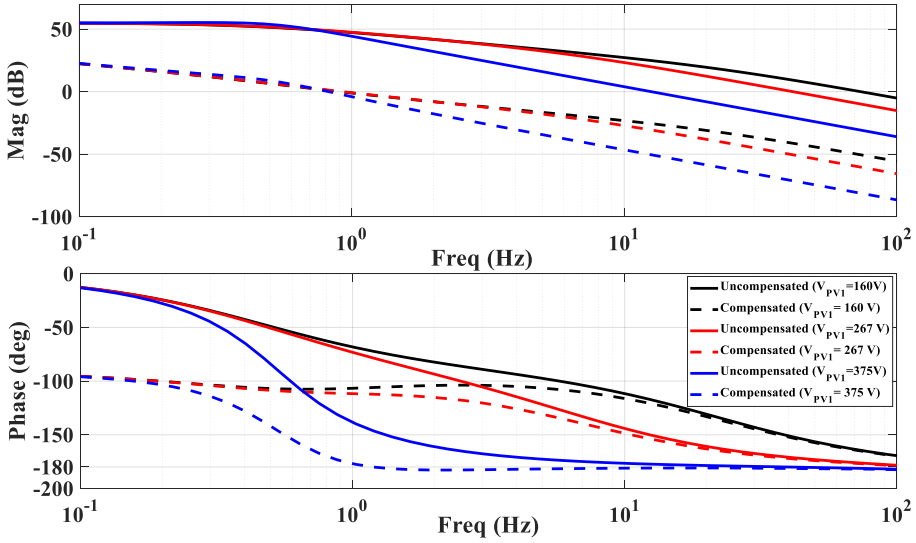

Figure 4.10.: Bode plot of the compensated and uncompensated open-loop $D_S(s)$ to $V_{VB}(s)$ transfer function at different operating points.

4.4.3. STABILITY ANALYSIS

Fig. 4.10 presents the Bode plot for the open-loop $D_S(s)$ to $V_{VB}(s)$ transfer function, both compensated and uncompensated, at three

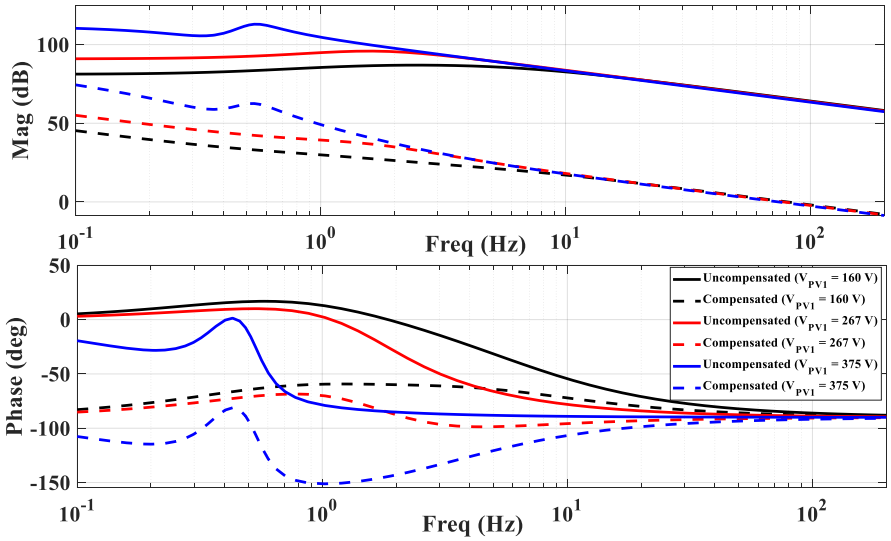

Figure 4.11.: Bode plot of the compensated and uncompensated open-loop $\Phi_S(s)$ to $V_{IB_i}(s)$ transfer function at different operating points.

different PV String 1 voltages (V_{PV_1}). The remaining operating point variables are detailed in Table. 4.2. As illustrated in Fig. 4.10 , when the PV String 1 voltage is equal to 267 V, the phase margin of the compensated $D_S(s)$ to $V_{VB}(s)$ transfer function is approximately 60 degrees (indicated by the red dashed line). When the voltage of PV String 1 decreases from 267 V to 160 V, a slight increase in the phase margin is observed, suggesting improved stability with greater mismatches between PV strings. Conversely, when the voltage increases from 267 V to 375 V, the phase margin decreases, leading to reduced system stability. This poor stability occurs because, at a PV string voltage of 375 V, the phase of the uncompensated transfer function (blue solid line) drops sharply near the selected bandwidth frequency. This behavior arises as increased voltage in PV String 1 reduces mismatch among PV strings, lowering the power processed by the SLCs. Note that low power operation of SLCs can also result from reduced PV string current. While lowering the bandwidth could mitigate this issue, it would also result in a slower transient response at other operating points. Therefore, for central converters, gain scheduling or other advanced control strategies such as Model Predictive Control (MPC) and Sliding Mode Control (SMC) are recommended to enhance performance, stability, and adaptability [18].

Fig. 4.11 shows the Bode plot for the open-loop $\Phi_S(s)$ to $V_{IB_i}(s)$

transfer function, both compensated and uncompensated, evaluated at the same operating points as in Fig. 4.10. The phase margin of uncompensated transfer function remains at 90 degrees across all three operating points, and the bandwidth, which defines the speed of the transient response, stays around 70 Hz. Thus, a simple PI controller can be sufficient for DAB converters across different operating points.

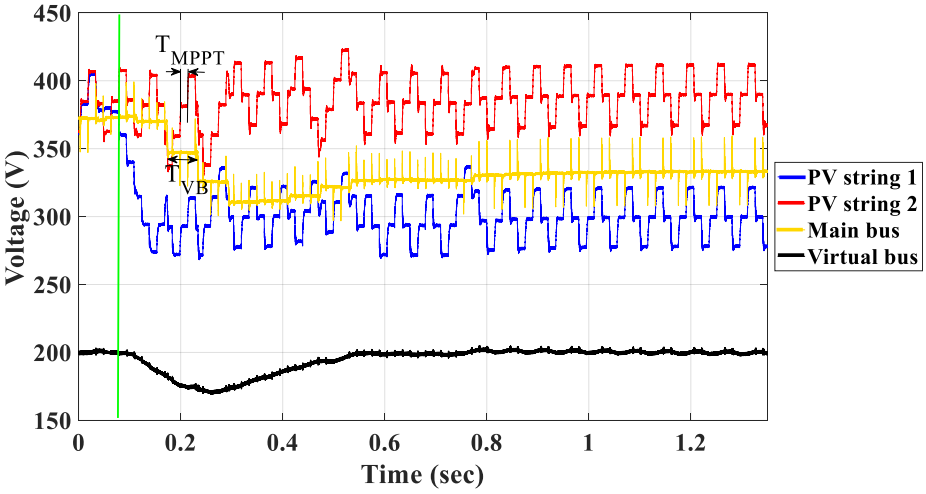

Figure 4.12.: Voltage waveforms in the PV2VB PDPP architecture. PV string 2 stays at I-V curve 1, whereas PV string 1 transitions from I-V curve 1 to I-V curve 2 after 0.07 s, highlighted with the green line.

4.5. EXPERIMENT RESULTS

To evaluate the performance of the PI controllers and their capability to manage disturbances, two different PV string curves, as shown in Fig. 3.11, are utilized. The operating point of PV string 1 experiences a significant and abrupt drop from 390 V to 300 V as it transitions from generating I-V curve 1 to I-V curve 2 at 70 ms (highlighted with a vertical green line in Fig. 4.12), whereas PV string 2 continues generating I-V curve 1. Fig. 4.12 illustrates that the central controller with a sampling time of 60 ms can effectively handle the disturbances, restoring the virtual bus to its initial state within less than 600 ms by determining a new operating voltage for the main bus. Simultaneously, the MPPT algorithm ensures that PV strings operate at their MPP. Fig. 4.12 proves the system's ability to independently find the MPP of both PV strings

with the typical behavior of P&O algorithm, with a perturbation period of 15 ms and a perturbation step size of 5% applied to the duty cycle.

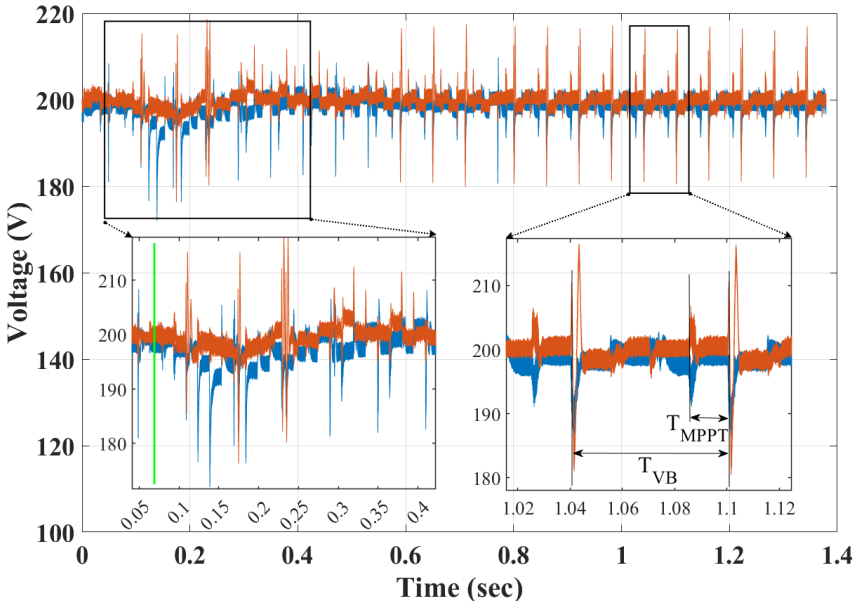

Figure 4.13.: Transition of intermediate bus voltages in the PV2VB PDPP architecture (blue: V_{IB_1}, red: V_{IB_2}).

Fig. 4.13 depicts the intermediate bus voltages of the architecture. The PI controllers of the DAB converters demonstrate their effectiveness in managing disturbances, successfully bringing back the intermediate bus voltages to 200 V after the abrupt change in the operating conditions of PV string 1. Additionally, the PI controller is capable of handling disturbances caused by the MPPT algorithm and central converter within 15 ms. It ensures that disturbances on intermediate bus voltages do not interfere with the operation of the MPPT and central controller.

4.6. CONCLUSION

This chapter provided a thorough analysis of the dynamic behavior of the PV2VB PDPP architecture and its mathematical model, crucial for designing and tuning controllers. The mathematical model was validated through system identification based on the data acquired from both PLECS simulation and experiments, ensuring its applicability in real-world scenarios. Considering the control requirements, the controller parameters were designed with a settling time of 15 ms,

which corresponds to the MPPT perturbation period, for the DAB controllers, a bandwidth of 1 Hz for the central converter's PI controller, and a phase margin of 60 degrees for both. The transient response and system stability were validated through experimental tests. These tests confirmed the system's stability, demonstrating the central controller's ability to stabilize the virtual bus voltage to the desired level within 0.6 seconds, while the intermediate bus voltages settled within 15 milliseconds.

REFERENCES

[1] A. Nazer, O. Isabella, and P. Manganiello. “Dynamic Analysis of Photovoltaic to Virtual Bus Parallel Differential Power Processing Architecture”. In: *IEEE Transactions on Industrial Electronics* (2025), pp. 1–12.

[2] J. G. Kassakian, D. J. Perreault, G. C. Verghese, and M. F. Schlecht. *Principles of Power Electronics*. Cambridge University Press, 2023.

[3] D. d. Giudice, A. Brambilla, D. Linaro, and F. Bizzarri. “Modular Multilevel Converter Impedance Computation Based on Periodic Small-Signal Analysis and Vector Fitting”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 69.4 (2022), pp. 1832–1842.

[4] B. Miao, R. Zane, and D. Maksimovic. “System identification of power converters with digital control through cross-correlation methods”. In: *IEEE Transactions on Power Electronics* 20.5 (2005), pp. 1093–1099.

[5] L. Ljung. “System identification”. In: *Signal analysis and prediction*. Springer, 1998, pp. 163–173.

[6] H. Gietler *et al.* “on-Time Mismatch Based System Identification Technique for Buck Converters”. In: *IEEE Transactions on Industrial Electronics* 67.9 (2020), pp. 7898–7908.

[7] M. G. Villalva, J. R. Gazoli, and E. R. Filho. “Comprehensive Approach to Modeling and Simulation of Photovoltaic Arrays”. In: *IEEE Transactions on Power Electronics* 24.5 (2009), pp. 1198–1208.

[8] L. Qin, S. Xie, C. Yang, and J. Cao. “Dynamic Model and Dynamic Characteristics of Solar Cell”. In: *2013 IEEE ECCE Asia Downunder*. Australia, June 2013, pp. 659–663.

[9] S. Shao *et al.* “Modeling and Advanced Control of Dual-Active-Bridge DC–DC Converters: A Review”. In: *IEEE Transactions on Power Electronics* 37.2 (2022), pp. 1524–1547.

[10] G. Rojas-Dueñas, J. R. Riba, and M. Moreno-Eguilaz. “Nonlinear Least Squares Optimization for Parametric Identification of DC–DC Converters”. In: *IEEE Transactions on Power Electronics* 36.1 (2021), pp. 654–661.

[11] A. Congiu, E. Bodano, and M. Barbaro. “A ΔΣ Dithering-Amplification-Based Identification Technique for Online SMPS”. In: *IEEE Transactions on Power Electronics* 31.8 (2016), pp. 5992–6001.

[12] P. Manganiello, M. Ricco, G. Petrone, E. Monmasson, and G. Spagnuolo. “Optimization of Perturbative PV MPPT Methods Through Online System Identification”. In: *IEEE Transactions on Industrial Electronics* 61.12 (2014), pp. 6812–6821.

[13] D. Maksimovic. “Computer-aided small-signal analysis based on impulse response of DC/DC switching power converters”. In: *IEEE Transactions on Power Electronics* 15.6 (2000), pp. 1183–1191.

[14] M. Al-Greer, M. Armstrong, M. Ahmeid, and D. Giaouris. “Advances on System Identification Techniques for DC–DC Switch Mode Power Converter Applications”. In: *IEEE Transactions on Power Electronics* 34.7 (2019), pp. 6973–6990.

[15] P. Manganiello, M. Ricco, E. Monmasson, G. Petrone, and G. Spagnuolo. “On-line optimization of the P&O MPPT method by means of the system identification”. In: *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*. 2013, pp. 1786–1791.

[16] D. Wang, B. Nahid-Mobarakeh, and A. Emadi. “Second Harmonic Current Reduction for a Battery-Driven Grid Interface With Three-Phase Dual Active Bridge DC–DC Converter”. In: *IEEE Transactions on Industrial Electronics* 66.11 (2019), pp. 9056–9064.

[17] P. N. Paraskevopoulos. *Modern control engineering*. CRC Press, 2017.

[18] Q. Xu, N. Vafamand, L. Chen, T. Dragičević, L. Xie, and F. Blaabjerg. “Review on Advanced Control Technologies for Bidirectional DC/DC Converters in DC Microgrids”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 9.2 (2021), pp. 1205–1221.

5

INTEGRATION OF BATTERY INTO PV2VB PDPP ARCITECTURE

This chapter demonstrates the capabilities of the proposed PV2VB PDPP architecture for PV/battery applications. The architecture enables the integration of a battery at the virutal bus and manages its power while performing MPPT on the PV strings. In the architecture, the battery is positioned at the virtual bus, acting as the input for all SLCs. Component voltage ratings can be reduced by selecting a lower voltage for the battery at the virtual bus than the PV string or the main bus voltages. While these SLCs track each PV string's MPP, the central converter manages battery charging and discharging. Experimental results confirm the performance and effectiveness of the proposed PV2VB PDPP architecture, achieving efficiencies between 95.5% and 99%.

5.1. INTRODUCTION

As mentioned in Chapter. 1, PV systems produce fluctuating and unreliable power due to their inherent intermittency. To address this issue, energy storage devices (ESDs) are commonly used alongside PV systems to stabilize output and enhance system reliability [2, 3]. As the penetration of PV systems increases, integrating them with ESDs becomes essential for grid connectivity. Amongst different ESD technologies, batteries are attracting much attention owing to advancements in battery technology, economies of scale in manufacturing, significant cost reductions, and efficiency improvements. Fig. 5.1 shows different PV/Battery architectures connected to a DC grid [4–9].

Parts of this chapter are currently under review [1].

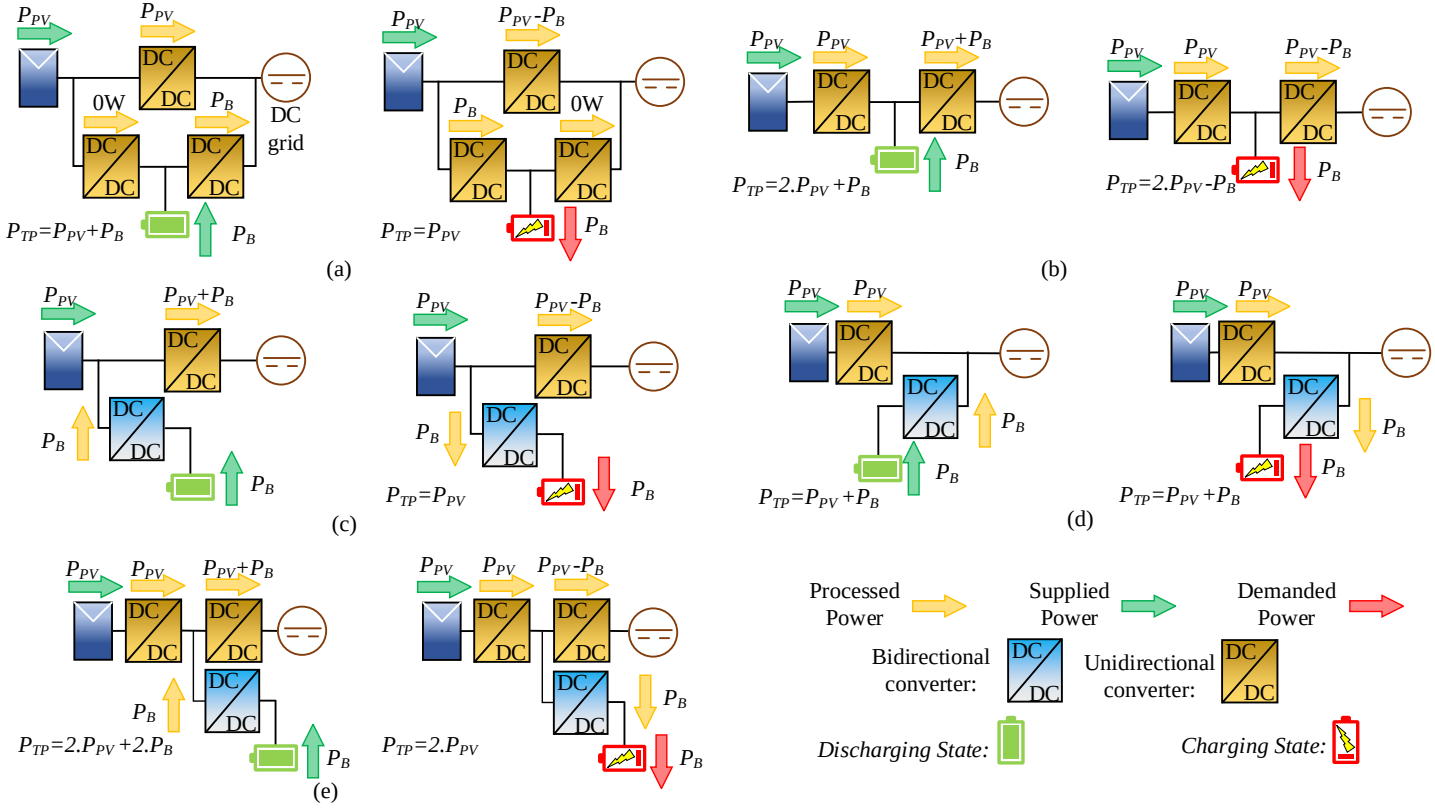

Figure 5.1.: Four topological PV/Battery architectures with indication of the power flow distribution. a) 3U, b) 2U, (c) 1U1B-I, d) 1U1B-II, and d) 1B2U architectures.

In a PV/Battery architecture, along with two independent control variables, at least three power transmission branches exist: PV to load (PV-L), PV to battery (PV-B), and battery to load (B-L). Notably, the average power transmitted through the PV-L branch is typically significantly larger than that transmitted through the other two branches. Based on power transmission paths, PV/Battery architectures can be typically categorized into four different architectures (Fig. 5.1): (i) 3U, consisting of three unidirectional DC-DC converters [10, 11]. (ii) 2U, consisting of two unidirectional DC-DC converters [12, 13] (iii) 1B1U, consisting of one bidirectional and one unidirectional DC-DC converter [14–17]. (iv) 1B2U, consisting of one bidirectional and two unidirectional DC-DC converters [18, 19].

In the 3U architecture (Fig. 5.1(a)), power transmission for each branch is achieved using a unidirectional two-port DC-DC converter, each with at least one independent control variable. Allocating one path for PV-L (high power) and another for PV-B/B-L (low power) allows the architecture to process less power overall (P_{TP}), resulting in high efficiency. However, the presence of three unidirectional DC-DC converters and three controllers increases the complexity and cost of the system and control. To reduce the complexity of the number of DC-DC converters, 2U architectures use the same path for all three power transmission branches (Fig. 5.1(b)). However, in this architecture, the power produced by the PV groups is processed twice to reach the load through the PV-L branch, which has high power. This not only deteriorates efficiency but also increases converters' costs due to the requirement for two high-power DC-DC converters.

To address the issues of 2U architectures, in the 1B1U architectures, the PV-L power is only processed through one unidirectional DC-DC converter. Depending on the connection of the bidirectional DC-DC converter to either the PV or the load port, two different 1B1U architectures are possible: (i) 1B1U-I [14, 15] (Fig. 5.1(c)) and (ii) 1B1U-II [16] Fig. 5.1(d)). Although the B-L power may be processed twice in 1B1U-I, it does not increase the processed power, unlike in 2U architectures, since B-L power is lower than PV-L power, and there are still only two DC-DC converters as in 2U. Considering both charging and discharging states, neither 1B1U-I nor 1B1U-II demonstrates a significant advantage over the other in total processed power. 1B1U-I has a strong ability to adapt to variations in the output port. In contrast, in the 1B1U-II architectures, the PV port is well-regulated with a dedicated bidirectional converter to adapt to changes in the output voltage/power of PV modules caused by different weather conditions. Unlike 1B1U-I, where the load is regulated solely by the unidirectional converter, 1B1U-II regulates the load voltage using either the unidirectional or bidirectional converter. This increases controller switching between operation modes, leading to control complexity. Moreover, for AC grid

connection, unlike 1B1U-II [20], 1B1U-I allows the integration of the unidirectional DC-DC converters' duties into the DC-AC inverters [14], improving cost and efficiency. Eventually, the literature has reported on the 1B2U architectures [21] (Fig. 5.1 (e)). This architecture suffers from several drawbacks. These include high architecture and control complexity, increased processed power, lower efficiency, and higher costs than other architectures.

Based on the abovementioned analysis, the architectures' main characteristics are summarized in Table. 5.1. The 1B1U-I architecture generally offers the best overall performance. However, it still has three main downsides. First, in applications with a higher PV voltage than the battery voltage, the unidirectional converters in the 1B1U-I architecture must tolerate the high PV voltage. This requirement leads to increased losses and system costs. In addition, if the PV part consists of PV strings and additional PV modules must be added to a PV string, the converters must be replaced to handle the new PV string voltage. This necessity decreases the scalability of the architecture. Last but not least, it is not feasible to extend the architecture to systems with multiple PV strings and independently track the MPP of each PV string.

Table 5.1.: Comparison of PV/Battery Architectures.

Feature	**3U**	**2U**	**1U1B-I**	**1U1B-II**	**1B2U**
Architecture Complexity	Poor	Good	Ave	Ave	Poor
Cost	High	High	Ave	Ave	High
Control Complexity	Poor	Good	Good	Poor	Poor
Efficiency	High	Low	High	High	Low
Processed Power	Low	High	Low	Low	High

This chapter aims to detail a new system based on the PV2VB PDPP architecture. This architecture is closely aligned with the 1B1U-I architecture and retains all its advantages. Yet, it fully exploits the benefits of the PV2VB PDPP architecture to remove the weakness of 1B1U-I architectures, such as (i) components requiring low blocking voltage in the bidirectional converter, leading to high efficiency and the advantages of low-voltage converters, (ii) higher scalability compared to existing architectures, and (iii) ability to performed string-level MPPT.

The remainder of this chapter is structured as follows: Section 5.2 introduces the proposed architectures for a single PV string, extends the architecture for multiple PV strings, and provides an in-depth analysis of the steady-state operation of both the central converter and SLCs, outlining their respective control objectives. Section 5.3 elaborates on

all possible operational states of the architecture. Section 5.4 discusses the battery charging and discharging rate and the operational regions in which the architecture can function. Section 5.5 presents experimental results to validate the system's performance.

5.2. OPERATION OF THE PROPOSED PV2VB PDPP ARCHITECTURE

5.2.1. FOR A SINGLE PV STRING

In 1B1U-I architectures, the bidirectional converter operates in parallel with the PV string, adding or subtracting current to manage battery power injection or withdrawal. In contrast, the proposed architecture design utilizes a bidirectional converter that adds or subtracts surplus voltage to the PV string voltage to manage battery power injection or withdrawal (Fig. 5.2). Consequently, this bidirectional converter must generate both positive and negative voltages, operating within the first and fourth quadrants of the V-I curve, making a BL converter (Fig. 3.5) a suitable option.

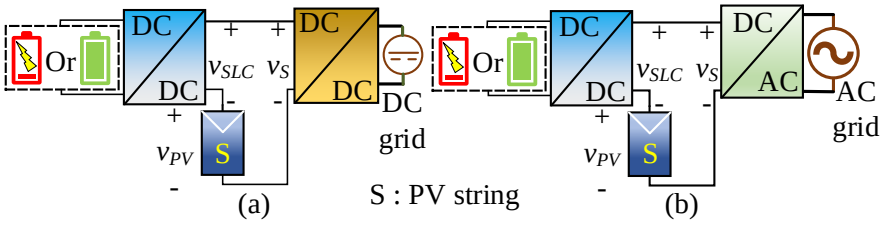

Figure 5.2.: Proposed architectures for a single PV string connected to (a) DC, and (b) AC grids. ochre and blue DC-DC blocks represent unidirectional and bidirectional DC-DC converters, respectively.

As discussed in Chapter 3, in the BL converter, during the switches' ON state, the voltage before the LC output filter (v_{IB}) polarity aligns with the intermediate bus voltage, discharging the capacitor. When the switches are OFF, the BL converter inverts the intermediate bus voltage, charging the capacitor. Predominantly maintaining the switches in the ON state during each switching period results in a positive voltage being added to the PV string, thus allowing average power flow from the battery to the string and vice versa. While the BL converter provides a straightforward solution, it does not offer isolation between the battery and the PV strings. Depending on the topologies chosen for the bidirectional and

unidirectional converters, the architecture can be non-isolated, partially isolated, or fully isolated.

Generally, two independent control variables are required for PV/Battery architectures to charge and discharge with given profiles and MPPT. Traditionally, the bidirectional converter is used as an actuator to perform battery charging/discharging, while the unidirectional converter tracks the MPP of the PV string. However, in the proposed design, the bidirectional converter is used to perform MPPT, while the unidirectional converter controls the operation of the battery. The advantages will become apparent in the next subsection when discussing the proposed architecture with multiple PV strings.

5.2.2. FOR MULTIPLE PV STRINGS

As shown in Fig. 5.3, to extend the proposed architectures for multiple PV strings, the storage ports can be paralleled as well as the grid ports while each PV port is independently connected to a PV string. Then, it is possible to integrate all the unidirectional DC-DC converters, common among architectures, into a single central converter. Finally, the architecture shown in Fig. 5.3 is PV2VB PDPP architecture. With N_{PV} PV strings, this architecture has $N_{PV}+1$ control objectives (N_{PV} PV strings and one battery), N_{PV} bidirectional converters (referred to as SLCs), and one unidirectional converter (referred to as the central converter), resulting in $N_{PV}+1$ actuators. As mentioned previously, the SLCs primarily provide the required differential voltage between the PV strings and the main bus voltage to independently track each PV string's MPP. These SLCs are interconnected to a shared storage port, also known as the virtual bus, where the batteries are placed.

CENTRAL CONVERTER

The central converter controller is an actuator that provides battery profile control, which is done by regulating the main bus voltage. If the assumption of lossless converters is considered for the sake of simplicity, the following relationship can be derived for the proposed architecture:

$$p_{\text{out}} = p_{\text{in}} + p_B \tag{5.1}$$

In the PV2VB PDPP architecture context, p_B, p_{out}, and p_{in} represents the battery power, the power delivered to the main bus, and the power generated by the PV strings, respectively. These powers can be computed as follows:

$$p_{\text{out}} = v_S \cdot i_S = v_S \cdot \sum_{i=1}^{N_{\text{PV}}} i_{\text{PV}_i} \tag{5.2}$$

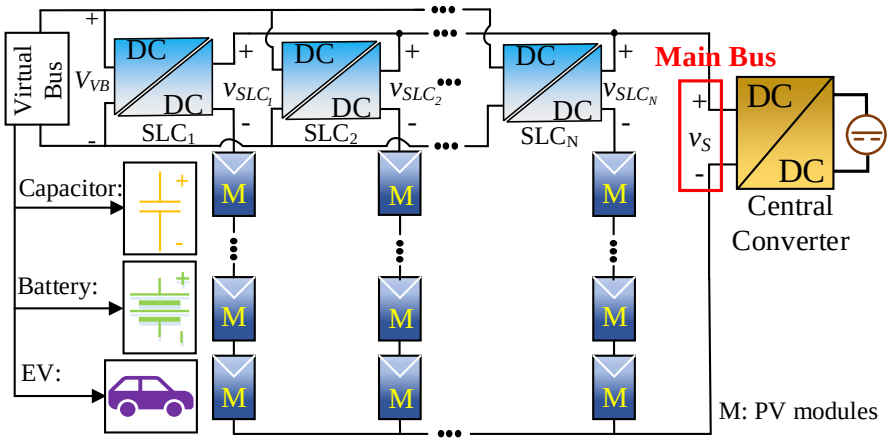

Figure 5.3.: Proposed PV2VB PDPP architecture for multiple PV strings. ochre and blue DC-DC blocks represent unidirectional and bidirectional DC-DC converters, respectively.

$$p_{\text{in}} = \sum_{i=1}^{N} v_{\text{PV}_i} \cdot i_{\text{PV}_i} \tag{5.3}$$

Where v_s, i_s, v_{PV_i}, and i_{PV_i} are the main bus voltage, the main bus current, the i^{th} PV string's voltage, and the i^{th} PV string's current, respectively. The following steady-state equation can be obtained by substituting equations (5.2) and (5.3) in equations (5.1):

$$P_B = V_S \cdot \sum_{i=1}^{N_{\text{PV}}} I_{\text{PV}_i} - \sum_{i=1}^{N_{\text{PV}}} \left(V_{\text{PV}_i} \cdot I_{\text{PV}_i} \right) \tag{5.4}$$

In equation (5.4) and the rest of the chapter, capital letters indicate the steady-state value of the variables. Achieving steady-state operation involves ensuring that PV strings operate at their MPP, with the main bus voltage as the sole actuator to control the charging and discharging of the battery. Specifically, PV strings must maintain constant current and voltage at their MPP. Consequently, the main bus current, which equals the summation of the PV strings' current, also remains constant. Thus, an increase in the main bus voltage signifies a greater energy demand, resulting in either a reduced battery charging rate or an increasing discharging rate. The output voltage of the i^{th} SLC can be expressed as:

$$V_{\mathrm{SLC}_i} = V_S - V_{\mathrm{PV}_i} \tag{5.5}$$

By substituting equation (5.5) in equation (5.4), we have:

$$P_B = \sum_{i=1}^{N_{\mathrm{PV}}} V_{\mathrm{SLC}_i} \cdot I_{\mathrm{PV}_i} \tag{5.6}$$

Given that I_{PV_i} is consistently positive, equation (5.6) shows that SLCs must generate negative and positive output voltage to charge and discharge the battery. To clarify further, if the i^{th} SLC generates a negative output voltage, the associated PV string assists in charging the battery. Conversely, the string discharges the battery when the output voltage is positive. A block diagram of the architecture and the central controller is shown in Fig. 5.4. A desired algorithm sets the reference for the battery current/voltage. When the current/voltage reference point is defined, it is compared with the actual battery current/voltage, and the errors go to the central controller, which provides an appropriate signal for the central converter to set the proper main bus voltage; then, according to equation (5.4), the desired current/voltage of the battery will be obtained. Most charging/discharging methods, such as constant current, constant voltage, constant current-constant voltage, multistage constant charging, and varying current charging methods [22, 23], can be applied to the PV2VB PDPP architecture.

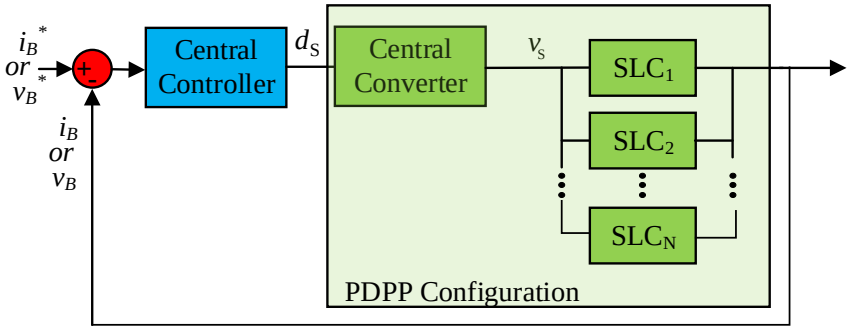

Figure 5.4.: Block diagram of the central controller approach for battery charging/discharging.

SLCs

When the architecture is extended for multiple PV strings, the SLCs must include an additional feature: isolation. This isolation is essential to

prevent the current from the PV strings from circulating through incorrect paths. Therefore, a DAB converter followed by a BL converter, with capacitors forming an intermediate bus to decouple their performance illustrated in Fig. 3.4 are employed. The architecture has at least partial isolation between the battery and PV strings within the system. This isolation is crucial for onboard battery chargers to ensure double fault protection and enhance user safety in plug-in hybrid electric vehicles [24].

5.3. THE PROPOSED ARCHITECTURE STATES

Generally, when the system directs power from one port to the other two, the architecture operates in Single-Input Dual-Output (SIDO) mode. In Dual-Input Single-Output (DISO) mode, power flows from two ports to the remaining one. When a port does not participate, the architecture is in Single-Input Single-Output (SISO) mode. Table. 5.2 shows the operation modes and port statuses.

The proposed architecture does not allow for the simultaneous operation of PV and grid as input, making the DISO-II mode outlined in Table. 5.2 unfeasible within this framework. In SISO-I mode, the central converter is bypassed, allowing the PV string to connect directly to the input of the SLCs and charge the battery. Since the maximum voltage of the SLCs is lower than the nominal MPP voltage of the PV string, the PV string will not operate at its MPP. However, this limitation is not necessarily a disadvantage, as in other architectures, where in this mode the power output is constrained by the battery's demand, which may also prevent the PV strings from operating at their MPP. To enable SISO-IV mode, the PV string must be bypassed (Fig. 5.7), allowing the battery to supply power directly to the grid.

If the central converter is bidirectional, it is possible to operate in SISO-III mode through this architecture; however, this aspect falls outside the scope of this thesis. Therefore, this section mainly focuses on the architecture operation in SIDO-I, DISO-I, and SISO-II modes. These subsets of operation modes result in the architecture possibly operating in eight distinct states, outlined in Table. 5.3.

Generally, the power delivered to the virtual bus from the i^{th} PV string (P_{PV_i2VB}) and the battery charging rate (P_B) is given by:

$$P_{PV_i2VB} = (V_S - V_{\mathrm{PV}_i}) \cdot I_{\mathrm{PV}_i} \tag{5.7}$$

$$P_B = \sum_{i=1}^{N_{\mathrm{PV}}} \left((V_S - V_{\mathrm{PV}_i}) \cdot I_{\mathrm{PV}_i} \right) \tag{5.8}$$

Table 5.2.: Operation Modes of PV/Battery Architectures

Mode	Input	Output	Proposed System Ability
SIDO	PV	Battery & Grid	Yes
DISO	PV & Battery	Grid	Yes
	PV & Grid	Battery	No
SISO	PV	Battery	Limited[1]
	PV	Grid	Yes
	Grid	Battery	Yes[2,3]
	Battery	Grid	Yes[3]

1: PV strings may not work at their MPP in this mode.
2: If the central converter is bidirectional.
3: Bypassing the PV strings and reconfiguring the architecture (Fig. 5.7).

Table 5.3.: States of PV2VB PDPP Architecture Based on Battery Status and Mismatches Among PV String MPP Voltages.

Battery Status	**Charging**			**Resting**		**Discharging**		
MPP Voltage Mismatches	No	Yes	Yes	No	Yes	No	Yes	Yes
SLCs Voltage	Negative	Negative	Both	0*	Both	Positive	Positive	both
State	1	2	3	4	5	6	7	8
Operation Mode	SIDO-I			SISO-II		DISO-I		

* In practice, the SLCs operate with a slightly negative voltage to compensate for their losses.

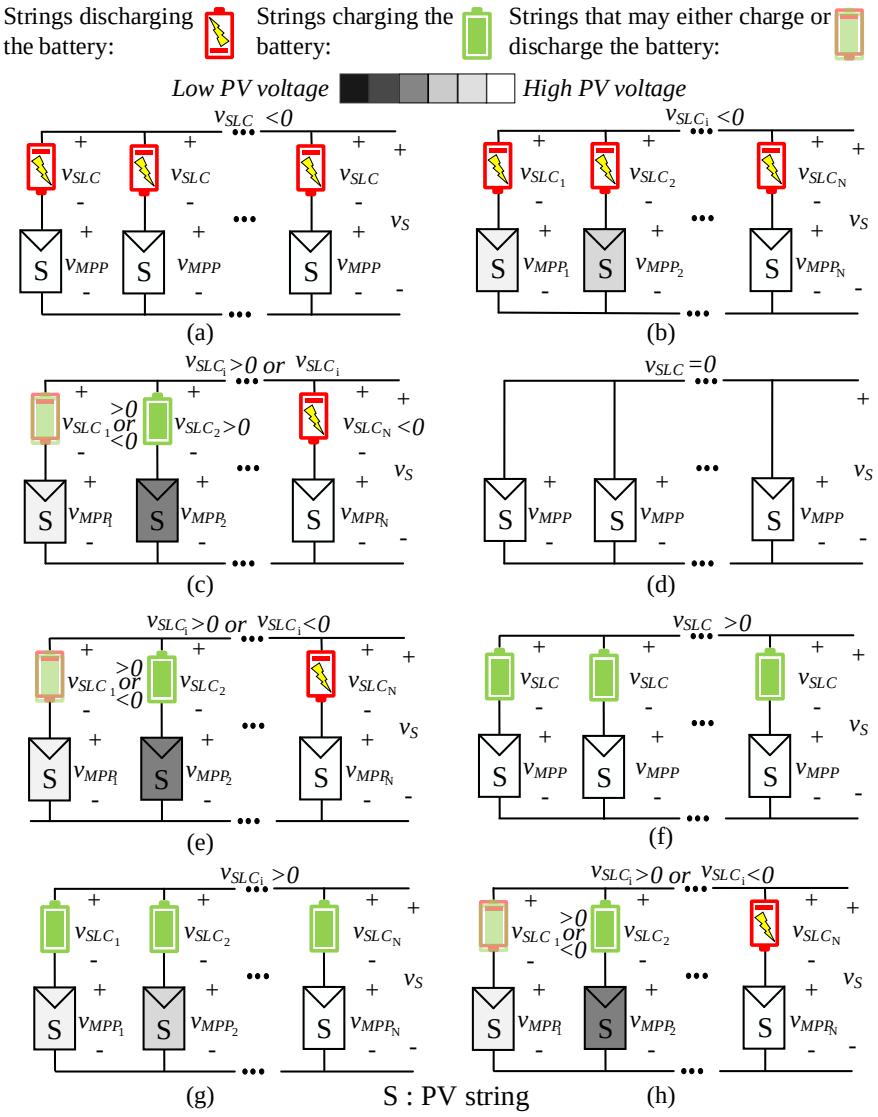

Figure 5.5.: Simplified PV2VB PDPP architecture when the architecture is in state (a) 1, (b) 2, (c) 3, (d) 4, (e) 5, (f) 6, (g) 7, (h) 8

STATE 1

As shown in Fig. 5.5(a), in state 1, it is assumed that there are no mismatch conditions among the MPP voltages of the PV strings and that the battery is being charged. In this scenario, the central controller acts as an actuator for battery charging, setting the main bus voltage lower than the PV string voltages to produce a negative SLC voltage. Therefore, this architecture can direct the power flow toward the battery, with the charging rate determined by the control input reference. Thus, Equation (5.7) and Equation (5.8) become:

$$P_{PV_i2VB} = (V_S - V_{\text{MPP}}) \cdot I_{\text{MPP}_i}, \quad V_S < V_{\text{MPP}} \tag{5.9}$$

$$P_B = (V_S - V_{\text{MPP}}) \cdot \sum_{i=1}^{N_{\text{PV}}} I_{\text{MPP}_i}, \quad V_S < V_{\text{MPP}} \tag{5.10}$$

Where I_{MPP_i} represents the MPP current of the i^{th} PV string and V_{MPP_i} is the MPP voltage of all PV strings. In this state, the contribution of each PV string to the power supplied to the battery is directly proportional to its current.

STATE 2

In state 2, it is assumed that while the battery is being charged, there are small mismatches among the MPP voltages of the PV strings (Fig. 5.5(b)). Therefore, the contribution of each PV string depends not only on its current but also on its voltage. If PV string currents are equal, those with higher voltage contribute more to charging the battery. To explain more, according to Equation (5.5), the summation of each PV string voltage and its corresponding SLCs voltage are equal to each other since the architecture only has a unique main bus voltage; therefore, a high MPP voltage of a PV string means that its SLC must generate negative voltage with higher amplitude. Therefore, the higher the voltage and current, the higher its contribution to charging the battery. In this state, the Equations (5.7) and (5.8) will be modified to:

$$P_{PV_i2VB} = (V_S - V_{\text{MPP}_i}) \cdot I_{\text{MPP}_i}, \quad V_S < V_{\text{MPP}_i} \tag{5.11}$$

$$P_B = \sum_{i=1}^{N_{\text{PV}}} (V_S - V_{\text{MPP}_i}) \cdot I_{\text{MPP}_i}, \quad V_S < V_{\text{MPP}_i} \tag{5.12}$$

Where V_{MPP_i} represents the MPP voltage of the i^{th} PV string.

STATE 3

As depicted in Fig. 5.5(c), increasing mismatches among the MPP voltages of PV strings cause some strings to produce voltages so low that they can no longer transfer power to the virtual bus to assist in charging the battery. Instead, these strings draw energy from the virtual bus to operate at their MPP. Thus, the SLCs associated with those PV strings produce positive voltage while others generate negative voltage. However, on average, the battery is still being charged. The equations describing this state are the same as equations (5.7) and (5.8), with all PV strings operating at MPP.

STATE 4

In this state, the battery is resting, and there are no mismatches among PV string MPP voltages. Therefore, SLCs ideally generate zero voltage or can be shut down as shown in Fig. 5.5(d), allowing the central converter to track the MPP of all PV strings. Since SLCs are still operational, they practically generate a low negative voltage to compensate for their losses. To elaborate further, since both the DAB and BL converters introduce losses, the system perceives these losses as a small load. As a result, even when the battery is in a resting state, the SLCs continue to supply power to compensate for the light load created by these losses. Eventually, the equations for this state are:

$$P_{PV_i2VB} = P_B = 0, \quad V_S \approx V_{\text{MPP}} \tag{5.13}$$

STATE 5

As depicted in Fig. 5.5(e), when the battery is resting, but there are mismatches among PV string MPP voltages, to ensure smooth and stable operation, some PV strings with higher MPP voltage inject energy to the virtual bus through the SLCs, while others draw energy from it. While the battery remains connected to the virtual bus, it is not actively involved in any energy exchange; instead, the parallel capacitor, typically situated in that position for power smoothing and stabilization, facilitates the power exchange among the PV strings. The equation for this state will be:

$$P_{PV_i2VB} = (V_S - V_{\text{MPP}_i}) \cdot I_{\text{MPP}_i}, \quad P_B = 0 \tag{5.14}$$

$$V_S = \frac{\sum_{i=1}^{N_{\text{PV}}} V_{\text{MPP}_i} \cdot I_{\text{MPP}_i}}{\sum_{i=1}^{N_{\text{PV}}} I_{\text{MPP}_i}} \tag{5.15}$$

STATE 6

As illustrated in Fig. 5.5(f), in state 6, we assume that the MPP voltages of the PV strings are all equal and the battery is discharging. In this context, the central controller operates as an actuator for the battery discharge process, establishing the discharge rate according to the control input reference. Therefore, the power injected from the battery to each string is calculated by:

$$P_{PV_i2VB} = (V_S - V_{\text{MPP}}) \cdot I_{\text{MPP}_i}, \quad V_S > V_{\text{MPP}} \tag{5.16}$$

$$P_B = (V_S - V_{\text{MPP}}) \cdot \sum_{i=1}^{N_{\text{PV}}} I_{\text{MPP}_i}, \quad V_S > V_{\text{MPP}} \tag{5.17}$$

In this state, the main bus voltage is higher than all PV strings voltages, resulting in positive SLCs voltage, so the direction of power flow is towards the strings.

STATE 7

When there are small mismatches among PV string voltages while the battery is being discharged, the system will be in state 7 (Fig. 5.5(g)). In this state, the contribution of each string to discharge the battery depends on their current and voltage. In fact, considering only voltage, the string with the lower MPP voltage has a higher contribution to discharge the battery since a lower MPP voltage means SLCs must generate positive voltage with a higher amplitude. In this state:

$$P_{PV_i2VB} = (V_S - V_{\text{MPP}_i}) \cdot I_{\text{MPP}_i}, \quad V_S > V_{\text{MPP}_i} \tag{5.18}$$

$$P_B = \sum_{i=1}^{N_{\text{PV}}} \left((V_S - V_{\text{MPP}_i}) \cdot I_{\text{MPP}_i} \right), \quad V_S > V_{\text{MPP}_i} \tag{5.19}$$

STATE 8

Eventually, as the mismatches among PV string voltages increase, some PV string voltages decrease to a point where they push the main bus voltage down so that the main bus voltage becomes lower than some PV string voltages (Fig. 5.5(h)). Thus, some PV strings inject energy into the virtual bus. In other words, some SLCs produce positive voltage while others generate negative voltage. However, on average, the battery still provides energy to the system. The equations describing this state are the same as Equations (5.7) and (5.8), with all PV strings operating at MPP.

5.4. THE RATE OF BATTERY CHARGE AND DISCHARGE

In Section 5.3, different states in which the architecture can operate are presented, defined mainly by weather conditions and the battery charging/discharging state. However, the architecture can only fulfill the expected duties if the SLC voltage ratings are properly designed. Therefore, an analysis similar to Chapter 3, where the virtual bus consists solely of capacitors, is required to design the PV/battery system properly.

Let $V_{PV_{MPP_{min}}}$ and $V_{PV_{MPP_{max}}}$ be the minimum and maximum MPP voltage, respectively. If the SLC maximum voltage ($V_{SLC_{max}}$) is selected properly, five regions emerge, separated by points A, B, D, and E (Fig. 5.6):

$$\begin{aligned} A &= (V_{\mathrm{PV}_{\mathrm{MPP}_{\mathrm{min}}}} - V_{\mathrm{SLC}_{\mathrm{max}}}), \quad B = (V_{\mathrm{PV}_{\mathrm{MPP}_{\mathrm{max}}}} - V_{\mathrm{SLC}_{\mathrm{max}}}) \\ D &= (V_{\mathrm{PV}_{\mathrm{MPP}_{\mathrm{min}}}} + V_{\mathrm{SLC}_{\mathrm{max}}}), \quad E = (V_{\mathrm{PV}_{\mathrm{OC}_{\mathrm{max}}}} + V_{\mathrm{SLC}_{\mathrm{max}}}) \end{aligned} \tag{5.20}$$

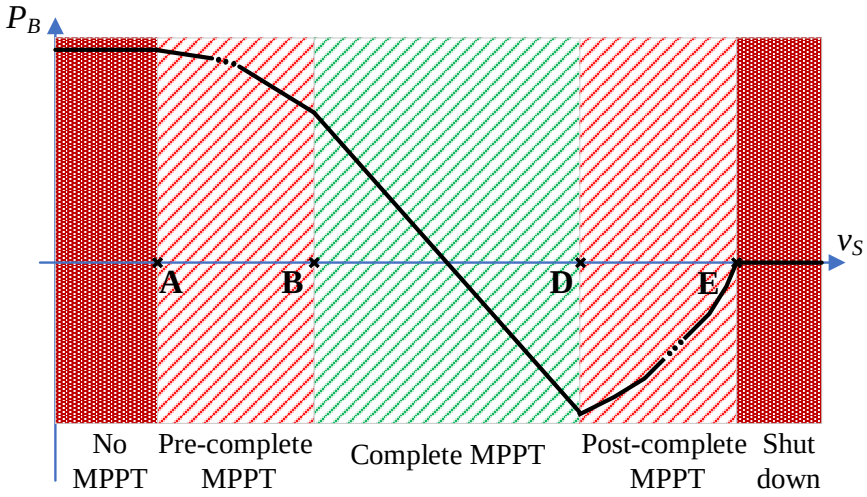

Figure 5.6.: The rate of the battery charging/discharging.

In the first two regions, a low v_s causes all or some SLCs to operate at their maximum inverted voltage ($-V_{SLC_{max}}$). Consequently, none of the PV strings operate at their MPP (No MPPT region), or a subset (N_1) operates at their MPP while the remaining N_2 PV strings do not (Pre-complete MPP region). In these regions, the battery is being continuously charged:

$$P_B = \sum_{i=1}^{N_{\text{PV}}} \left(V_{\text{SLC}_{\text{max}}} \cdot I_{\text{MPP}_i} \right), \quad 0 \leq v_s < A \tag{5.21}$$

$$P_B = \sum_{i=1}^{N_1} \left((V_{\text{MPP}_i} - v_s) \cdot I_{\text{MPP}_i} \right) + V_{\text{SLC}_{\text{max}}} \cdot \sum_{i=1}^{N_2} I_{\text{SC}_i}, \quad A \leq v_s < B \tag{5.22}$$

On the other hand, in the last two regions (beyond point D), v_s is so high that some PV strings no longer operate at their MPP. In essence, within the Post-complete MPP region, N_3 PV strings reach the open circuit voltage, N_4 PV strings operate at ($v_s - V_{SLC_{max}}$), which is between their open circuit voltage and their MPP voltage, and N_5 PV strings operate at their MPP. In these regions, the battery is being discharged:

$$P_B = -V_{\text{SLC}_{\text{max}}} \cdot \sum_{i=1}^{N_4} I_{\text{PV}_i} + \sum_{i=1}^{N_5} \left((V_{\text{MPP}_i} - v_s) \cdot I_{\text{MPP}_i} \right), \quad D \leq v_s < E \tag{5.23}$$

At point E, all PV strings reach their open-circuit voltage, producing no power. Between points B and D is the desired operating region, called "Complete MPPT", where all PV strings work at MPP:

$$P_B = \sum_{i=1}^{N_{\text{PV}}} \left((V_{\text{MPP}_i} - v_s) \cdot I_{\text{MPP}_i} \right), \quad B \leq v_s < D \tag{5.24}$$

To ensure the existence of this region, point D must be positioned to the right of Point B, which means:

$$V_{\text{SLC}_{\text{max}}} \geq \frac{V_{\text{PV}_{\text{MPP}_{\text{max}}}} - V_{\text{PV}_{\text{MPP}_{\text{min}}}}}{2} \tag{5.25}$$

In the Complete MPPT region, the architecture can effectively track the PV string MPP and manage battery charging/discharging rates as per Equation (5.4). A specific range for the rate of battery charging/discharging is depicted in Fig. 5.6. When mismatches are minimal, where $V_{PV_{MPP_{max}}}$ is close or equal to $V_{PV_{MPP_{min}}}$, the absolute maximum rate of battery charging/discharging can be achieved by:

$$P_B = \pm \sum_{i=1}^{N_{\text{PV}}} \left(V_{\text{SLC}_{\text{max}}} \cdot I_{\text{MPP}_i} \right) \tag{5.26}$$

Based on equations (5.25) and (5.26), increasing $V_{SLC_{max}}$ allows for a greater MPPT range, which is the difference between $V_{PV_{MPP_{max}}}$ and $V_{PV_{MPP_{min}}}$, enhancing the system's capability to handle more severe mismatch conditions and increasing the absolute maximum rate of

battery charging/discharging. Equation (5.26) reveals that the battery charging or discharging rate depends on the PV string currents. In SISO-IV, the PV string current does not flow, so utilizing the battery to supply the grid or vice versa becomes unfeasible. To address the issue, bypassing the PV strings and activating the switches of the BL converters can reconfigure the system, as depicted in Fig. 5.7, enabling SISO-III and SISO-IV modes.

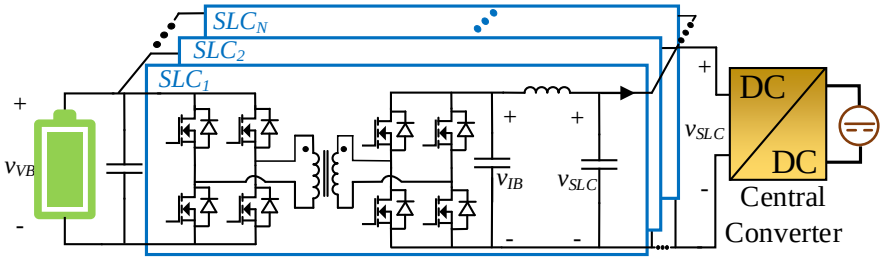

Figure 5.7.: The reconfigured PDPP architecture during low sun irradiance and battery discharging, such as at night.

5.5. EXPERIMENTAL RESULTS

This section emphasizes the proposed architecture's capability to effectively perform MPPT at the string level while managing the battery charging and discharging rate. Fig. 3.10 presents the proposed PV2VB PDPP architecture prototype featuring two PV strings for PV/Battery applications. In the new experiment, the third SM1500-CP-30 Bi-directional DC Power Supply, turned off during the experiment in Chapter 3, has been utilized as the battery. Detailed electrical specifications and component values are summarized in Table. 3.2.

5.5.1. STRING LEVEL MPPT AND BATTERY CHARGING/DISCHARGING

The operation of the proposed architecture with two PV strings has been verified through experimental tests. In the experiments, a Perturb and Observe (P&O) algorithm with a perturbation period of 20 ms and a duty cycle perturbation step size of 5% is employed. Each PV string generates 390V and 5.3 A under Standard Test Conditions (STC). Here, a boost converter among various possible topologies has been chosen as the central converter to perform the energy management of the battery via a PI controller with a sampling time of 80 ms (Fig. 5.8). As shown in Table. 5.4, the battery charging/ discharging states and mismatches

among PV strings are selected to ensure that the simulated PV system experiences all the mentioned states. The virtual bus is emulated as a stack of batteries with a voltage of 200V, which defines the voltage rating of the SLCs.

Table 5.4.: Experimental Operation Points for the Architecture

State	Battery Charge Rate	PV String 1 MPP Point	PV String 2 MPP Point	Main Bus Voltage*
State 1	-480 W	380 V / 5.3 A	380 V / 5.3 A	334 V
State 2	-480 W	350 V / 5.3 A	380 V / 5.3 A	320 V
State 3	-240 W	270 V / 5.3 A	380 V / 5.3 A	302 V
State 4	0 W	380 V / 5.3 A	380 V / 5.3 A	380 V
State 5	0 W	350 V / 5.3 A	380 V / 5.3 A	365 V
State 6	480 W	380 V / 5.3 A	380 V / 5.3 A	425 V
State 7	480 W	350 V / 5.3 A	380 V / 5.3 A	410 V
State 8	240 W	290 V / 5.3 A	380 V / 5.3 A	357 V

*: Expected main bus voltage based on Equation (5.4).

Initially, PV strings operate under uniform STC conditions, and the battery is being charged at a rate of 480 W. The system is in state 1, as shown in Fig. 5.8, with the main bus voltage below both PV string voltages. It results in both SLCs generating negative voltages, meaning that both PV strings contribute to charging the battery. After around 1.3 seconds, a small mismatch is introduced between the PV strings while the battery continues to charge at 480 W. This transition moves the system to state 2, where the main bus voltage remains below both PV string voltages. As a result, SLCs still generate negative voltages, and PV strings continue to charge the battery. At 4.4 sec, a significant mismatch is applied between the PV strings, and the battery is charging at 240 W, moving the system into state 3. Therefore, the main bus voltage is lower than the PV string 2 voltage but higher than the PV string 1 voltage. This means PV string 1 no longer contributes to injecting energy to the virtual bus and instead draws power from it to operate at its MPP.

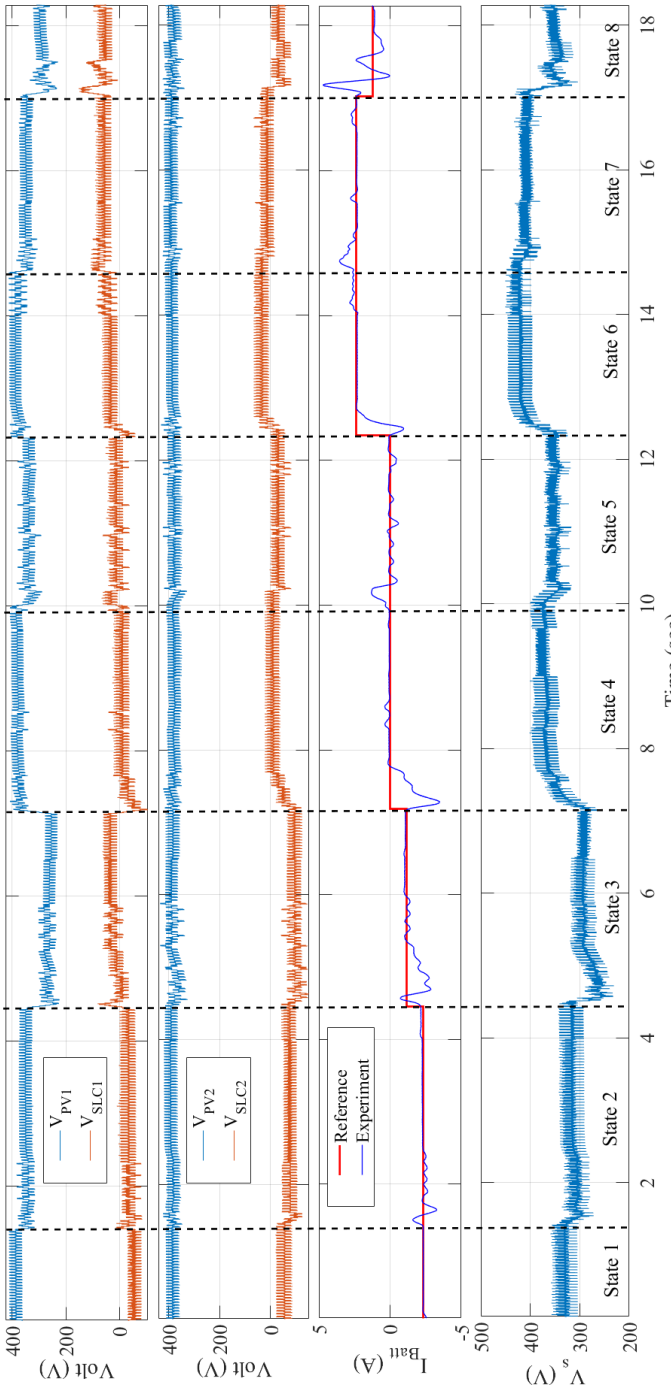

Figure 5.8.: Experimental results of the PDPP architecture in different operation states based on operation points shown in Table. 5.4

At 7.2 seconds, the battery rests with no mismatches and minor mismatches between PV strings voltage applied at 9.9 sec. As shown in Fig. 5.8, the SLCs generate a voltage close to zero when there are no mismatches. Although it is expected that SLCs generate absolute zero voltage based on equation 5.4, a small negative voltage has been generated because of the converter's losses. When mismatches occur, some SLCs generate positive voltage while others generate negative voltage, resulting in zero average power on the virtual bus, allowing the battery to rest.

In the next approximately four seconds, the battery starts discharging, directing power to the output. When there are no or minor mismatches among the PV string voltages, the SLCs generate positive voltage. Since the output current of SLCs is positive, the battery power can pass to the output. However, at 17 seconds, a significant mismatch among PV string voltages occurs. Therefore, the SLC corresponding to PV string 2, which has the higher voltage, generates negative voltage, resulting in PV string 2 sending power to the virtual bus to maintain its MPP.

Ultimately, experiments verify that the architecture can set an appropriate main bus voltage to charge, discharge, or rest the battery, facilitating effective energy management while tracking the MPP of PV strings.

5.5.2. PV2VB PDPP ARCHITECTURE EFFICIENCY

This subsection analyzes the efficiency of the proposed architecture. The efficiency of the SLCs was measured under the following conditions: 200 V input (virtual bus) voltage, load voltage between -55 V and 55 V, and varying load current between 1 A and 5 A. Fig. 5.9 shows that under these conditions, the average efficiency of a single SLC ranges from 84.4% to 95.1%. Similarly, the efficiency of the PV2VB PDPP architecture with an integrated battery was measured with the SLCs under the same conditions. PV string 2 was kept constant at 380 V and 5.3 A, while the battery current was adjusted from -3 A to 3 A and PV string 1 current (called a load current) from 1 A to 5 A. Efficiency was measured at over 130 different operating points. The yellow region in Fig. 5.9 illustrates the system efficiency across these points, encompassing all discussed states and demonstrating a range from 95.5% to 97.5%. The average measured conversion efficiency of the architecture as a function of PV string 1 current shows efficiency ranging from 96.3% to 97%. These results confirm that the system efficiency always exceeds that of a single SLC. Notably, when the system is in state 4, it is possible to deactivate the SLCs, resulting in a system efficiency of 99%.

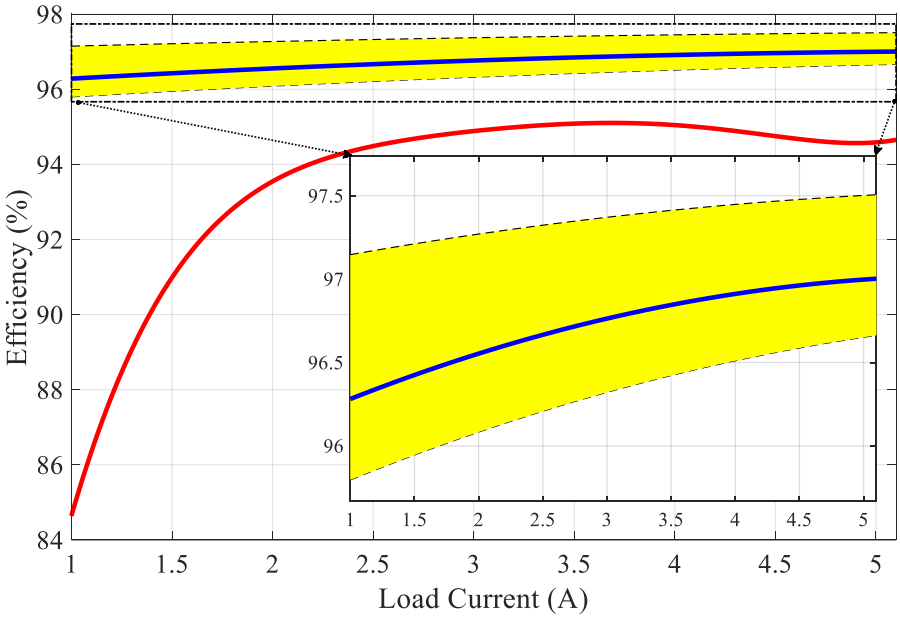

Figure 5.9.: Averaged system efficiency (Blue line) and a single SLC efficiency (Red line) as a function of load current.

5.6. CONCLUSION

This chapter detailed a novel PV2VB PDPP-based architecture specifically designed for string-level MPPT while efficiently managing battery charging and discharging. In this architecture, the SLCs operate in fast loops to independently track MPPT, while a central converter, such as a boost converter, manages the battery in a slower loop. By exploring all possible system operational states across different battery charge/discharge rates, the architecture is shown to function effectively in modes such as SIDO-I, DISO-I, SISO-I, SISO-II, SISO-III, and SISO-IV. Experimental results validate the architecture's performance and theoretical foundations, demonstrating string-level MPPT with system efficiency between 95.5% and 99%.

REFERENCES

[1] A. Nazer, O. Isabella, H. Vahedi, and P. Manganiello. “Integration of Battery into Photovoltaic to Virtual Bus Parallel Differential Power Processing Architecture”. In: *IEEE Transactions on Industrial Electronics,* "*Under Review*" (2025).

[2] G. G. Farivar *et al.* “Grid-Connected Energy Storage Systems: State-of-the-Art and Emerging Technologies”. In: *Proceedings of the IEEE* 111.4 (2023), pp. 397–420.

[3] X. Liu, X. Liu, Y. Jiang, T. Zhang, and B. Hao. “Photovoltaics and Energy Storage Integrated Flexible Direct Current Distribution Systems of Buildings: Definition, Technology Review, and Application”. In: *CSEE Journal of Power and Energy Systems* 9.3 (2023), pp. 829–845.

[4] A. A. Abdalla, M. S. E. Moursi, T. H. M. El-Fouly, and K. H. A. Hosani. “Reliant Monotonic Charging Controllers for Parallel-Connected Battery Storage Units to Reduce PV Power Ramp Rate and Battery Aging”. In: *IEEE Transactions on Smart Grid* 14.6 (2023), pp. 4424–4438.

[5] V. Jain, B. Singh, and Seema. “A Grid Connected PV Array and Battery Energy Storage Interfaced EV Charging Station”. In: *IEEE Transactions on Transportation Electrification* 9.3 (2023), pp. 3723–3730.

[6] P. Nambisan and M. Khanra. “Optimal Energy Management of Battery Supercapacitor Aided Solar PV Powered Agricultural Feed Mill Using Pontryagin’s Minimum Principle”. In: *IEEE Transactions on Power Electronics* 37.2 (2022), pp. 2216–2225.

[7] Z. Zhang *et al.* “High-Efficiency Silicon Carbide-Based Buck-Boost Converter in an Energy Storage System: Minimizing Complexity and Maximizing Efficiency”. In: *IEEE Industry Applications Magazine* 27.3 (2021), pp. 51–62.

[8] Z. Wang *et al.* “Topology Analysis and Review of Three-Port DC–DC Converters”. In: *IEEE Transactions on Power Electronics* 35.11 (2020), pp. 11783–11800.

[9] G. Wang *et al.* “A Comprehensive Review of Integrated Three-Port DC–DC Converters With Key Performance Indices”. In: *IEEE Transactions on Power Electronics* 39.5 (2024), pp. 6391–6408.

[10] S. S. Dobakhshari *et al.* “A New Soft-Switched Three-Port DC/DC Converter With High Voltage Gain and Reduced Number of Semiconductors for Hybrid Energy Applications”. In: *IEEE Transactions on Power Electronics* 35.4 (2020), pp. 3590–3600.

[11] T. Qian *et al.* “A Boost-Type Three-Port Resonant Forward Converter With Flexible Power Flow Path Optimization for PV Systems”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 70.1 (2023), pp. 161–165.

[12] B. Zhang *et al.* “Novel topology and control of a non-isolated three port DC-DC converter for PV-battery power system”. In: *2017 20th International Conference on Electrical Machines and Systems (ICEMS)*. 2017, pp. 1–6.

[13] X. Sun *et al.* “A PWM and PFM Hybrid Modulated Three-Port Converter for a Standalone PV/Battery Power System”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 3.4 (2015), pp. 984–1000.

[14] O. M. Akeyo *et al.* “The Design and Analysis of Large Solar PV Farm Configurations With DC-Connected Battery Systems”. In: *IEEE Transactions on Industry Applications* 56.3 (2020), pp. 2903–2912.

[15] Z. Saadatizadeh *et al.* “High-Frequency Three-Port DC–DC Converter With Zero-Voltage Switching Operation”. In: *IEEE Transactions on Industrial Electronics* 71.1 (2024), pp. 537–548.

[16] L. Senapati *et al.* “A Systematic Approach to Synthesize a Non-Isolated TPCC With Fully Reconfigurable Structure for RES”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 69.7 (2022), pp. 3314–3318.

[17] H. Aljarajreh *et al.* “A Method of Seamless Transitions Between Different Operating Modes for Three-Port DC-DC Converters”. In: *IEEE Access* 9 (2021), pp. 59184–59195.

[18] K. Li *et al.* “Research on Multi-mode Control Strategy of High-Power Three-port Photovoltaic DC Converter”. In: *2021 International Conference on Advanced Electrical Equipment and Reliable Operation (AEERO)*. 2021, pp. 1–6.

[19] K. Wang *et al.* “Topology-Level Power Decoupling Three-Port Isolated Current-Fed Resonant DC-DC Converter”. In: *IEEE Transactions on Industrial Electronics* 69.5 (2022), pp. 4859–4868.

[20] H. Hasabelrasul *et al.* “Two-Stage Converter Standalone PV-Battery System Based on VSG Control”. In: *IEEE Access* 10 (2022), pp. 39825–39832.

[21] R. K and R. Kalpana. “An Isolated Dual-Input Half-Bridge DC–DC Boost Converter With Reduced Circulating Power Between Input Ports”. In: *IEEE Canadian Journal of Electrical and Computer Engineering* 45.1 (2022), pp. 68–76.

[22] K. Liu *et al.* “A brief review on key technologies in the battery management system of electric vehicles”. In: *Frontiers of Mechanical Engineering* 14.1 (2019), pp. 47–64.

[23] K. K. Duru *et al.* “Critical Insights Into Fast Charging Techniques for Lithium-Ion Batteries in Electric Vehicles”. In: *IEEE Transactions on Device and Materials Reliability* 21.1 (2021), pp. 137–152.

[24] S. S. Williamson *et al.* “Industrial Electronics for Electric Transportation: Current State-of-the-Art and Future Challenges”. In: *IEEE Transactions on Industrial Electronics* 62.5 (2015), pp. 3021–3032.

6

FULLY PV2VB SPDPP FOR PV SYSTEMS

This chapter extends the proposed PV2VB PDPP architecture to a novel architecture termed PV2VB SPDPP, which effectively mitigates mismatches in both series-connected PV modules (i.e., current mismatches) and parallel-connected PV strings (i.e., voltage mismatches). The proposed architecture employs a combination of SLCs and module-integrated converters (MICs) that process only a fraction of the total power. The chapter comprehensively describes how the virtual bus voltage is balanced through mathematical power flow equations, ensuring stable and efficient operation. Finally, the effectiveness of the architecture is validated through real-time simulation results with two RT PLECS boxes, demonstrating its ability to address mismatch issues and optimize the performance of photovoltaic systems.

6.1. INTRODUCTION

As discussed in Chapter 2, SDPP architectures are designed to address mismatches among series-connected PV modules, while PDPP architectures focus on eliminating mismatches among parallel-connected PV strings. By integrating SDPP and PDPP architectures, SPDPP architectures have been developed to mitigate mismatches across both series- and parallel-connected PV groups. Depending on the combination of SDPP and PDPP configurations and the connection methods employed for the primary sides of MICs and SLCs, various SPDPP architectures can be implemented, each offering distinct advantages and facing unique challenges.

Some parts of this chapter are currently under review [1], while other parts have already been published in [2].

In Chapter 2-5, we introduced and detailed a novel architecture for PDPP systems. To fully address mismatches among PV modules, the proposed PDPP must be combined with an SDPP architecture. As discussed in Chapter 2, there are three main SDPP architectures: PV2PV, PV2B, and PV2VB. Since one of our primary objectives is to reduce the voltage rating of the converters, PV2B is not considered, leaving PV2PV and PV2VB as the viable options.

In [3, 4], a distinct SPDPP topology was introduced based on the PV2PV SDPP concept. This architecture improves modularity and scalability by utilizing switched inductors in all SPDPP MICs and SLCs. However, the accumulation effect limits the effectiveness of this architecture in longer PV strings. To explain more, in PV2PV SDPP, power transfer occurs solely between adjacent PV modules, MICs must process power multiple times to transfer it from unshaded to shaded modules, leading to a significant drawback known as the accumulation effect [5]. Before delving into the explanation of the proposed fully PV2VB SPDPP architecture, Section 6.2 first outlines the significant disadvantages of the accumulation effect in PV2PV SDPP systems and strategies to mitigate it. This sets the stage for clarifying the necessity and advantages of using PV2VB SDPP architecture in fully developed PV2VB SPDPP architecture.

The remainder of this chapter is structured as follows: Section 6.2 explores the performance and power flow of the conventional and hierarchical PV2PV SDPP architectures. Section 6.3 outlines the overall structure of the SPDPP architecture, including the associated MICs, SLCs, and central converter, and explains the role of each within the system. Section 6.4 details the control loops of the SLCs and central converter, providing an in-depth analysis of the system's steady-state operation. Section 6.5 discusses the considerations required to design PV2VB SPDPP architecture. Section 6.6 presents real time simulation with two RT PLECS boxes, validating the architecture's performance and highlighting its inherent advantages.

6.2. ACCUMULATION EFFECT IN PV2PV SDPP ARCHITECTURE

As shown in Fig. 2.13, the conventional PV2PV SDPP architecture faces an issue known as the accumulation effect, occurring when SDPP converters repeatedly transfer power between adjacent PV submodules, resulting in increased total power processing and converter power ratings, reducing efficiency, especially in long PV strings [5]. To mitigate this effect, hierarchical PV2PV SDPP offers additional paths for power transfer [6, 7]. This section explores the performance and power flow of the conventional and hierarchical PV2PV SDPP architecture. Since this section contains numerous equations with multiple states, inputs, and

outputs, precise symbolization is essential. To enhance readability, we have included a nomenclature in Table. 6.1 to assist the reader in case of any uncertainties.

Table 6.1.: List of Symbols and Definitions

Symbol	Description
K_i	Number of PV groups of i^{th} hierarchy
$N_{SDPP_{H_i}}$	The total number of SDPPs at the i^{th} hierarchy
N_{SDPP}	The total number of SDPPs
$N_{\ \mathrm{PV_{SM}}}$	The total number of PV submodules
$I_{SDPP_{(H_i-m_j)}}$	j^{th} SDPP converter at the m^{th} cluster of PV groups of ith hierarchy
$I_{SDPP_{(H_i-m_j)}}$	The current of j^{th} SDPP converter at the m^{th} cluster of PV group of i^{th} hierarchy
$I_{\ \mathrm{PVG}(H_i-m_j)}$	The current of the j^{th} PV group of the m^{th} cluster of PV groups of i^{th} hierarchy
$V_{\ \mathrm{PVG}(H_i-m_j)}$	The voltage across the j^{th} PV group of the m^{th} cluster of PV groups of i^{th} hierarchy
$P_{\ \mathrm{PVG}(H_i-m_j)}$	The power generated by the j^{th} PV group of the m^{th} cluster of PV groups of i^{th} hierarchy
$P_{\mathrm{PVG}(H_i-m_j),MPP}$	The absolute maximum power that can be generated by the j^{th} PV group of the m^{th} cluster of PV groups of i^{th} hierarchy. (The notation is also used for voltage and current)
I_{SDPP_j}	The current of the j^{th} SDPP converter in conventional PV2PV architecture
$I_{PV_{SM}}$	The current of PV submodules
P_{SDPP}	Power processed by an SDPP converter in conventional PV2PV architecture
V_{SDPP}	Voltage across an SDPP converter in conventional PV2PV architecture
I_{SDPP}	Current passing through an SDPP converter in conventional PV2PV architecture
V_{PV_M}	PV module voltage
V_s	String voltage
K_{sh_i}	Shading factor of i^{th} hierarchy

6.2.1. HIERARCHICAL PV2PV SDPP ARCHITECTURE

Hierarchical PV2PV SDPP architecture, shown in Fig. 6.1, is made of Z hierarchies. The innermost PV groups are PV submodules, consisting only of electrically connected PV cells and not embedding any SDPP converters. The PV groups of the second hierarchy are PV modules, each consisting of K_1 PV submodules and $(K_1 - 1)$ SDPP converters. Next hierarchy employs $(K_2 - 1)$ hierarchy-dedicated SDPP converters connected to the K_2 PV modules. Similarly, the n^{th} hierarchy is made of K_n PV groups and $(K_n - 1)$ SDPP converters. In this architecture, the number of SDPP converters at the i^{th} hierarchy is given by:

$$N_{\mathrm{SDPP}_{H_i}} = (K_i - 1) \cdot \prod_{j=i+1}^{Z} K_j \tag{6.1}$$

The total number of SDPP converters (N_{SDPP}) is the sum of all SDPP converters at all levels:

$$N_{\mathrm{SDPP}} = N_{\mathrm{SDPP}_{H_1}} + \cdots + N_{\mathrm{SDPP}_{H_i}} + \cdots + N_{\mathrm{SDPP}_{H_Z}} \tag{6.2}$$

Eventually, by substituting Equation (6.1) into Equation (6.2) for a submodule-level DMPPT in hierarchical PV2PV SDPP with $N_{PV_{SM}}$ PV submodules, there are in total $(N_{PV_{SM}} - 1)$ SDPP converters.

$$N_{\mathrm{SDPP}} = N_{\mathrm{PV}_{SM}} - 1 \tag{6.3}$$

Using the central converter as the additional actuator, the system has $N_{PV_{SM}}$ actuators, enough to control $N_{PV_{SM}}$ PV submodules. SDPP converters process power during mismatch conditions, transferring it between shaded and unshaded PV groups. Comparative analysis of models and architectures is vital since losses, cost, and size are directly tied to the total processed power and vary among architectures. For simplicity, two assumptions are made: (i) all SDPP converters are lossless, and (ii) all PV submodules operate at the same voltage, ensuring near-MPP operation due to the low sensitivity of PV voltage to mismatch.

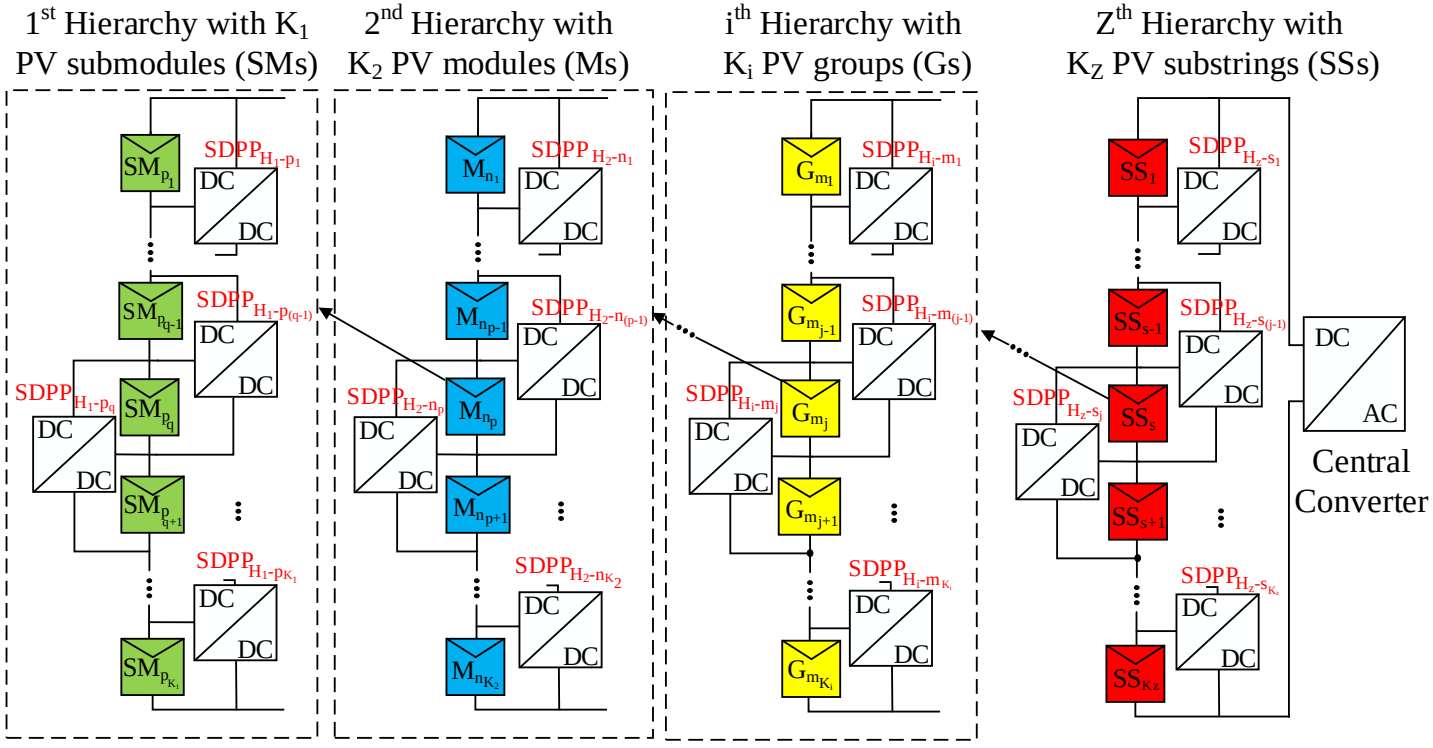

Figure 6.1.: Hierarchical PV2PV SDPP architecture.

Here, an analysis of the power processed by the SDPP converters at the m^{th} cluster of PV groups of i^{th} hierarchy is performed (see Fig. 6.2). The current of the topmost SDPP converter, denoted as $SDPP_{(H_i-m_1)}$, is obtained through the application of Kirchhoff's rules on Cut-Set 1:

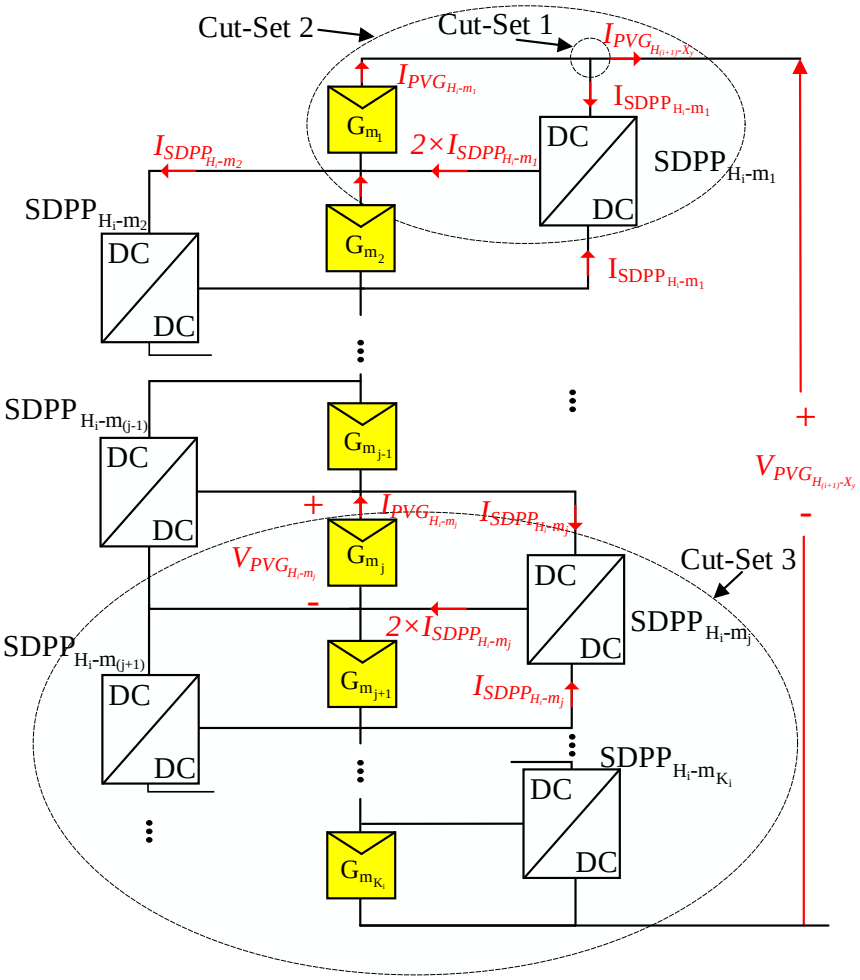

Figure 6.2.: m^{th} cluster of PV groups of i^{th} hierarchy with its corresponding SDPP converters.

$$I_{SDPP_{(H_i-m_1)}} = I_{PVG(H_i-m_1)} - I_{PVG(H_{(i+1)}-X_y)} \tag{6.4}$$

Considering Cut-Set 2, the second SDPP current is given by:

$$I_{SDPP_{(H_i-m_2)}} = I_{PVG_{(H_i-m_2)}} + I_{SDPP_{(H_i-m_1)}} - I_{PVG_{(H_{(i+1)}-x_y)}} \tag{6.5}$$

Subsequently, utilizing Cut-Set 3, the j^{th} SDPP current is expressed as:

$$I_{SDPP_{(H_i-m_j)}} = I_{PVG_{(H_i-m_j)}} + I_{SDPP_{(H_i-m_{j-1})}} - I_{PVG_{(H_{(i+1)}-x_y)}} \tag{6.6}$$

In Equation (6.6), a recurrence relation emerges. Upon solving, the following equation is derived for the j^{th} SDPP current:

$$I_{SDPP_{(H_i-m_j)}} = \sum_{n=1}^{j} I_{PVG_{(H_i-m_n)}} - j \cdot I_{PVG_{(H_{(i+1)}-x_y)}} \tag{6.7}$$

To eliminate $I_{PVG_{(H_{(i+1)}-x_y)}}$ in Equation (6.7), the power balance for the cluster is redefined under the assumption of no losses:

$$P_{PVG_{(H_{(i+1)}-x_y)}} = \sum_{n=1}^{K_i} P_{PVG_{(H_i-m_n)}} \tag{6.8}$$

Which may be rewritten as:

$$V_{PVG_{(H_{(i+1)}-x_y)}} \cdot I_{PVG_{(H_{(i+1)}-x_y)}} = \sum_{n=1}^{K_i} \left(V_{PVG_{(H_i-m_n)}} \cdot I_{PVG_{(H_i-m_n)}} \right) \tag{6.9}$$

The voltage across all PV groups at the m^{th} cluster of PV groups of i^{th} hierarchy is calculated as:

$$V_{PVG_{(H_{(i+1)}-x_y)}} = \sum_{n=1}^{K_i} V_{PVG_{(H_i-m_n)}} \tag{6.10}$$

Due to the equality of voltages across all PV groups, we have:

$$V_{PVG_{(H_i-m_1)}} = \cdots = V_{PVG_{(H_i-m_{K_i})}} = \frac{V_{PVG_{(H_{(i+1)}-x_y)}}}{K_i} \tag{6.11}$$

By substituting Equations (6.10) and (6.11) into Equation (6.9), the current $I_{PVG_{(H_{(i+1)}-x_y)}}$ is expressed in terms of PV groups' currents:

$$I_{PVG_{(H_{(i+1)}-x_y)}} = \frac{\sum_{n=1}^{K_i} I_{PVG_{(H_i-m_n)}}}{K_i} \tag{6.12}$$

Equation (6.12) indicates that the current of the PV group in the next related hierarchy ($I_{PVG_{(H_{(i+1)}-x_y)}}$) is equal to the average current of PV groups belonging to the m^{th} cluster of PV groups in the i^{th} hierarchy. By

substituting Equation (6.12) into Equation (6.7), the desired expression is obtained for:

$$I_{SDPP_{(H_i-m_j)}} = \frac{K_i - j}{K_i} \cdot \sum_{n=1}^{j} I_{PVG_{(H_i-m_n)}} - \frac{j}{K_i} \cdot \sum_{n=j+1}^{K_i} I_{PVG_{(H_i-m_n)}} \tag{6.13}$$

Equation (6.13) reveals that the currents of SDPP converters only depend on the operation of PV groups in the same cluster and hierarchy. In other words, each cluster is treated as an independent entity, and the operation of the SDPP converters within a cluster is not influenced by factors such as partial shading of PV groups outside the cluster itself. Thus, the hierarchical architecture limits the accumulation effect among SDPP converters belonging to the same cluster of the same hierarchy. Further details will be discussed in next subsection.

6.2.2. HIERARCHICAL VERSUS CONVENTIONAL PV2PV SDPP CONVERTER RATING

Equation (6.13) can be applied to both hierarchical and conventional PV2PV systems to determine the converter rating. For the conventional system with $N_{PV_{SM}}$ PV submodules, the expression becomes:

$$I_{SDPP_{m_j}} = \frac{(N_{\mathrm{PV}_{SM}} - j)}{N_{\mathrm{PV}_{SM}}} \cdot \sum_{n=1}^{j} I_{\mathrm{PV}_{SM_n}} - \frac{j}{N_{\mathrm{PV}_{SM}}} \cdot \sum_{n=j+1}^{N_{\mathrm{PV}_{SM}}} I_{\mathrm{PV}_{SM_n}} \tag{6.14}$$

If Equation (6.13) is multiplied by the voltage of SDPPs converters ($\frac{V_s}{N_{PV_{SM}}}$), it is possible to calculate the power processed by the j^{th} SDPP converter as:

$$P_{SDPP_j} = \frac{(N_{\mathrm{PV}_{SM}} - j)}{N_{\mathrm{PV}_{SM}}} \cdot \sum_{n=1}^{j} P_{\mathrm{PV}_{SM_n}} - \frac{j}{N_{\mathrm{PV}_{SM}}} \cdot \sum_{n=j+1}^{N_{\mathrm{PV}_{SM}}} P_{\mathrm{PV}_{SM_n}} \tag{6.15}$$

The maximum value of Equation (6.15) determines the SDPP converters' power rating, with the worst-case scenario considered, as outlined in [5], where the first (or second) half of PV submodules ($j = \frac{N_{PV_{SM}}}{2}$) are shaded, each with a maximum power generation of ($K_{sh} \times P_{PV_{SM},\mathrm{MPP}}$) per PV submodule, while the other half remains unshaded. In this case, the SDPP converter at the boundary between the shaded and unshaded sections of the PV string processes the largest amount of power. The power flow through the SDPP converter connecting these two sections is then expressed as:

$$P_{SDPP,\max} = \frac{N_{PV_{SM}}}{4} \cdot P_{PV_{SM},\mathrm{MPP}} \cdot (1 - K_{\mathrm{sh}}) \tag{6.16}$$

$$I_{SDPP,\max} = \frac{N_{PV_{SM}}}{4} \cdot I_{PV_{SM},\mathrm{MPP}} \cdot (1 - K_{sh}) \tag{6.17}$$

$$V_{SDPP,\max} = \frac{2 \cdot V_s}{N_{\mathrm{PV}_{SM}}} = 2 \cdot V_{\mathrm{PV}_{SM},\mathrm{MPP}} \tag{6.18}$$

As shown in Equations (6.16)–(6.18), the power and current rating of the SDPP converters depend on the total number of PV submodules, and their voltage rating is contingent on the voltage of the PV submodules.Utilizing Equations (6.13) and (6.16)–(6.18), the ratings of the converters in the i^{th} hierarchy is evaluated as in Equations (6.19)–(6.21):

$$P_{SDPP_{(H_i-m)},\max} = \frac{K_i}{4} \cdot P_{\mathrm{PVG}_{(H_i-m)},\mathrm{MPP}} \cdot (1 - K_{\mathrm{sh}_i}) \tag{6.19}$$

$$I_{SDPP_{(H_i-m)},\max} = \frac{K_i}{4} \cdot I_{\mathrm{PVG}_{(H_i-m)},\mathrm{MPP}} \cdot (1 - K_{\mathrm{sh}_i}) \tag{6.20}$$

$$V_{SDPP_{(H_i-m)},\max} = \frac{2 \cdot V_{\mathrm{PVG}_{(H_{(i+1)}-m)},\mathrm{MPP}}}{K_i} \tag{6.21}$$

In the j^{th} hierarchy, each PV group consists of $\prod_{j=1}^{i-1} K_j$ PV submodules, thus:

$$P_{\mathrm{PVG}_{(H_i-m),\mathrm{MPP}}} = \prod_{j=1}^{i-1} K_j \cdot P_{\mathrm{PV}_{SM},\mathrm{MPP}} \tag{6.22}$$

The absolute maximum MPP current of PV groups is:

$$I_{\mathrm{PVG}_{(H_i-m)},\mathrm{MPP}} = I_{\mathrm{PV}_{SM},\mathrm{MPP}} \tag{6.23}$$

The voltage of the whole cluster is:

$$V_{\mathrm{PVG}_{(H_{(i+1)}-m)},\mathrm{MPP}} = V_{\mathrm{PV}_{SM},\mathrm{MPP}} \cdot \prod_{j=1}^{i} K_j \tag{6.24}$$

By substituting Equations (6.22)–(6.24) into equations (6.19)–(6.21), the expressions become:

$$P_{SDPP_{(H_i-m)},\max} = \frac{\prod_{j=1}^{i} K_j}{4} \cdot P_{\mathrm{PV}_{SM},\mathrm{MPP}} \cdot (1 - K_{\mathrm{sh}_i}) \tag{6.25}$$

$$I_{SDPP_{(H_i-m)},\max} = \frac{K_i}{4} \cdot I_{\mathrm{PV}_{SM},\mathrm{MPP}} \cdot (1 - K_{\mathrm{sh}_i}) \tag{6.26}$$

$$V_{SDPP_{(H_i-m)},\max} = 2 \cdot V_{\mathrm{PV}_{SM},\mathrm{MPP}} \cdot \prod_{j=1}^{i-1} K_j \tag{6.27}$$

The power rating of SDPPs depends on all PV submodules within the hierarchy, leading to a higher power rating for outer SDPP converters. However, the required power rating of hierarchical SDPPs across all hierarchies is lower than that of conventional PV2PV SDPPs, except for the Z^{th} hierarchy, which remains equal. This is due to the limited accumulation effect among PV groups in the same cluster and hierarchy. Furthermore, SDPP converters' current rating only depends on the number of PV groups within the given hierarchy, while their voltage rating depends on the voltage of each PV group.

By adjusting equations (6.25)–(6.27), the component ratings for the Z^{th} hierarchy are as follows:

$$P_{SDPP_{(H_z-m)},\max} = \frac{N_{PV_{SM}}}{4} \cdot P_{PV_{SM},\mathrm{MPP}} \cdot (1 - K_{\mathrm{sh}_z}) \tag{6.28}$$

$$I_{\mathrm{SDPP}_{(H_z-m)},\max} = \frac{K_z}{4} \cdot I_{PV_{SM},\mathrm{MPP}} \cdot (1 - K_{\mathrm{sh}_z}) \tag{6.29}$$

$$V_{\mathrm{SDPP}_{(H_z-m)},\max} = \frac{V_s}{K_z} = 2 \cdot V_{SM,\mathrm{MPP}} \cdot \prod_{j=1}^{Z-1} K_j \tag{6.30}$$

As evident in Equations (6.28)–(6.30), the power rating of SDPPs for the Z^{th} hierarchy depends on the total number of PV submodules. The power rating of hierarchical PV2PV SDPPs at this hierarchy is the same as that of conventional PV2PV, but the differences lie in their current and voltage ratings. The former requires switches with higher voltage but lower current than the latter. The primary advantage of this hierarchy is the reduction in conduction losses compared to conventional PV2PV SDPP systems.

Again, by adjusting Equations (6.25)–(6.27), the power ratings of converters for the first hierarchy are given by:

$$P_{SDPP_{(H_1-m)},\max} = \frac{K_1}{4} \cdot P_{PV_{SM},\mathrm{MPP}} \cdot (1 - K_{\mathrm{sh}_1}) \tag{6.31}$$

$$I_{SDPP_{(H_1-m)},\max} = \frac{K_1}{4} \cdot I_{PV_{SM},\mathrm{MPP}} \cdot (1 - K_{\mathrm{sh}_1}) \tag{6.32}$$

$$V_{SDPP_{(H_1-m)},\max} = \frac{2 \cdot V_{PV_M}}{K_1} = 2 \cdot V_{PV_{SM},\mathrm{MPP}} \tag{6.33}$$

As demonstrated in Equations (6.31)–(6.33), the voltage rating of hierarchical PV2PV SDPPs at the first hierarchy is the same as that of conventional PV2PV systems. However, the current and power ratings are significantly decreased. This reduction is attributed to the accumulation effect being limited among the PV submodules inside each PV module.

We consider a PV string composed of nine PV modules to compare component ratings between hierarchical and conventional architectures. Each PV module comprises 3 PV submodules, resulting in 27 PV submodules per PV string. We analysed three architectures: (i) conventional PV2PV, (ii) two-hierarchy PV2PV SDPP ($K_1 = 3, K_2 = 9$), and (iii) three-hierarchy PV2PV SDPP ($K_1 = 3, K_2 = 3, K_3 = 3$). Table. 6.2 illustrates a significant reduction in the power rating of the inner SDPPs compared to the conventional structure. For instance, in the three-hierarchy PV2PV SDPP, only two converters with the same power rating as the conventional one are required, while the remaining 24 converters have substantially lower power ratings. This is due to the mitigation of the accumulation effect, resulting in reduced processed power in the hierarchical structure.

PROCESSED POWER

The second benefit of the accumulation effect's limitation is the reduced processed power. The three architectures introduced in the previous subsection are examined to demonstrate this. With 27 PV submodules operating at their maximum power point voltage of 26.63 V and current of 7.9 A, the total processed power in the three architectures is evaluated based on the number of shaded PV submodules. Shading locations can vary within the PV string, occurring at the top, bottom, or middle. Utilizing 100,000 runs in the Matlab environment, shading locations are randomly selected with the shading factor of 0.5, and the total power processed by all converters in steady-state is computed. The resulting averages are depicted in Fig. 6.3 for the three architectures. Due to the accumulation effect, the conventional PV2PV structure exhibits the highest total processed power. Notably, the most challenging scenario occurs when half of the PV submodules are shaded, resulting in the peak total processed power across all three architectures. Furthermore, an increase in hierarchies corresponds to reduced processed power. In architectures with more hierarchies, power is processed fewer times, but this reduction becomes less pronounced as the accumulation effect weakens.

Table 6.2.: Comparison between hierarchical and conventional PV2PV SDPP: converter ratings and count.

Parameter	Conventional PV2PV	Hierarchical PV2PV				
		Two Hierarchies		Three Hierarchies		
		First	Second	First	Second	Third
Voltage Rating	1 p.u	1 p.u	3 p.u	1 p.u	3 p.u	9 p.u
Current Rating	1 p.u	1/9 p.u	1/3 p.u	1/9 p.u	1/9 p.u	1/9 p.u
Power Rating	1 p.u	1/9 p.u	1 p.u	1/9 p.u	1/3 p.u	1 p.u
Converter Count	26	18	8	18	6	2

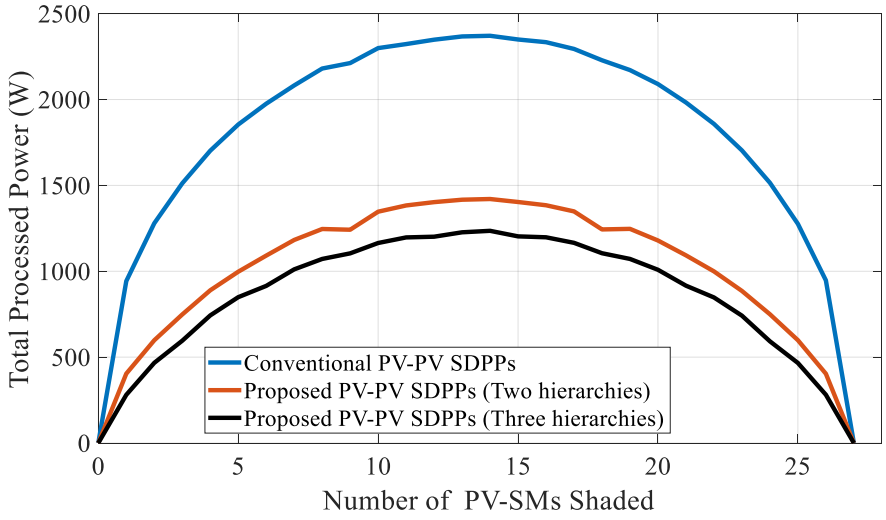

Figure 6.3.: Total processed power as a function of the number of shaded PV submodules in different architectures.

To elaborate on mitigating the accumulation effect, consider a hierarchical PV2PV SDPP architecture with two levels: module and submodule hierarchies. As illustrated in Fig. 6.4(a), when mismatches occur among PV modules, only the converters at the module level activate, while those at the submodule level remain inactive. Conversely, if mismatches arise among PV submodules (Fig. 6.4(b)), the submodule-level converters engage, with the module-level converters staying off. Finally, as shown in Fig. 6.4(c), when mismatches exist at both levels, only the converters that provide the shortest path for power transmission activate, optimizing power flow efficiency.

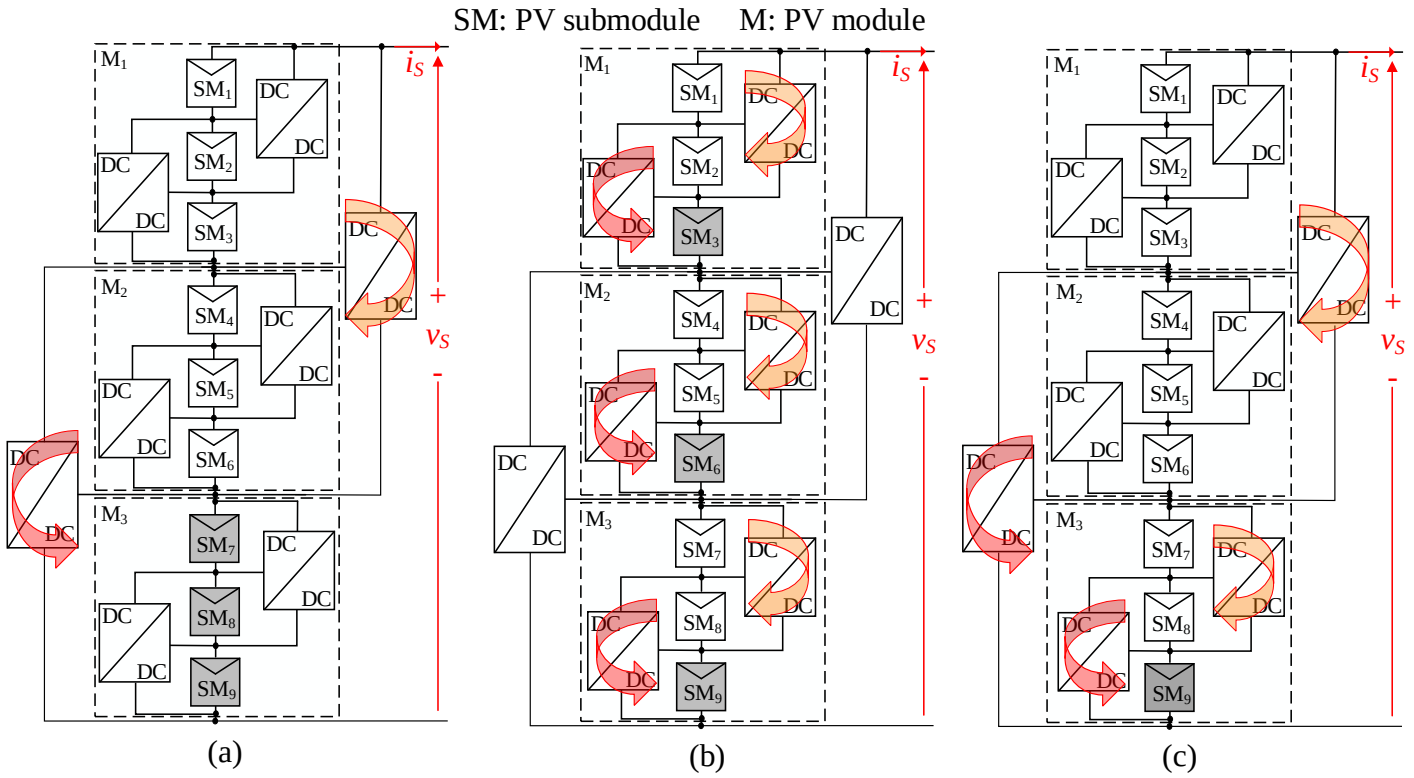

Figure 6.4.: Hierarchical PV2PV SDPP architecture with two hierarchies (a) Mismatches among PV modules, (b) mismatches among PV submodules, and (c) mismatches among PV modules (M) and PV submodules (SM).

6.2.3. SIMULATION RESULTS

This subsection performs dynamic simulations in Matlab/Simulink to verify the proposed structure's ability to limit accumulation effects among SDPPs across (i) different hierarchical levels and (ii) the same hierarchical level but within different outer hierarchies. This simulation uses a PV string comprising 27 PV submodules, each with an MPP voltage and current of 26.63 V and 7.9 A, respectively. As shown in Fig. 6.5(c), three hierarchical PV2PV SDPPs control their voltages at different levels: the first hierarchy involves PV submodules, the second hierarchy PV modules, and the third hierarchy PV substrings. Four scenarios are defined to examine this architecture further to evaluate hierarchical PV2PV SDPPs with three levels (see Table. 6.3). The simulation initially sets all PV submodules under uniform conditions, where each receives full illumination (1000 $\frac{W}{m^2}$). After 0.1 seconds, the irradiance conditions outlined in Table. 6.3 are applied.

In the first scenario, one PV submodule in each PV module is shaded, causing mismatch solely among PV submodules. Fig. 6.6 illustrates that only SDPP converters at the submodule hierarchy transfer power among PV submodules. In this scenario, one of the three PV submodules within each PV module is shaded, so all PV modules and PV strings produce the same current. In other words, the mismatch only exists among PV submodules, with no mismatch between PV modules and PV substrings. Consequently, as shown in Fig. 6.6, only the SDPP converters in the first hierarchy actively transfer power among PV submodules, while those in the second and third hierarchies do not process power. In the second scenario, one PV module within each PV substring is uniformly shaded, leaving the others unshaded. This means no mismatch exists within the PV submodules or PV substring groups. As depicted in Fig. 6.7, only the SDPP converters in the second hierarchy operate, while those in other hierarchies remain inactive. In the third scenario, the mismatch occurs solely among PV substrings. As shown in Fig. 6.8, only the SDPP converters in the third hierarchy are active, with all others shut down. These results confirm that the accumulation effect is effectively mitigated across different hierarchies. Additionally, Fig. 6.6–6.8 demonstrates that SDPP converters in outer hierarchies handle more power, requiring components with ahigher power rating. In the fourth scenario, only the bottommost PV submodule is shaded, leading to mismatches among PV submodules, PV modules, and PV substrings. Fig. 6.9 indicates that converters in the affected PV groups operate, while others are shut down.

These simulation results prove the efficacy of hierarchical PV2PV SDPP in limiting the accumulation effect.

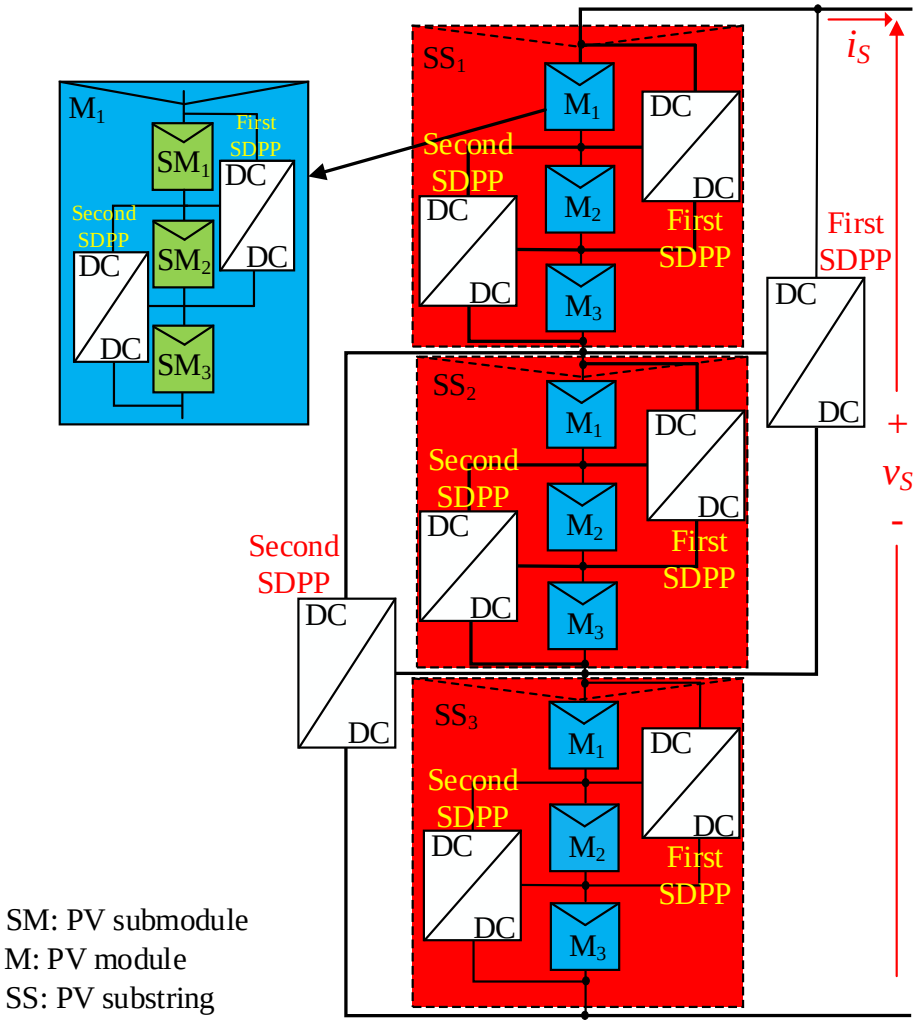

Figure 6.5.: Simulated Hierarchical PV2PV SDPP architecture.

Table 6.3.: Test Cases for 27 PV submodules, 9 PV modules, and 3 PV substrings. Numbers and colors indicate the location and the hierarchy in the PV string.

PV Substring	**1**									**2**									**3**								
PV Module	1			2			3			1			2			3			1			2			3		
PV Submodule	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3
Scenario 1																											
Scenario 2																											
Scenario 3																											
Scenario 4																											
$1000\,\frac{W}{m^2}$	$500\,\frac{W}{m^2}$																										

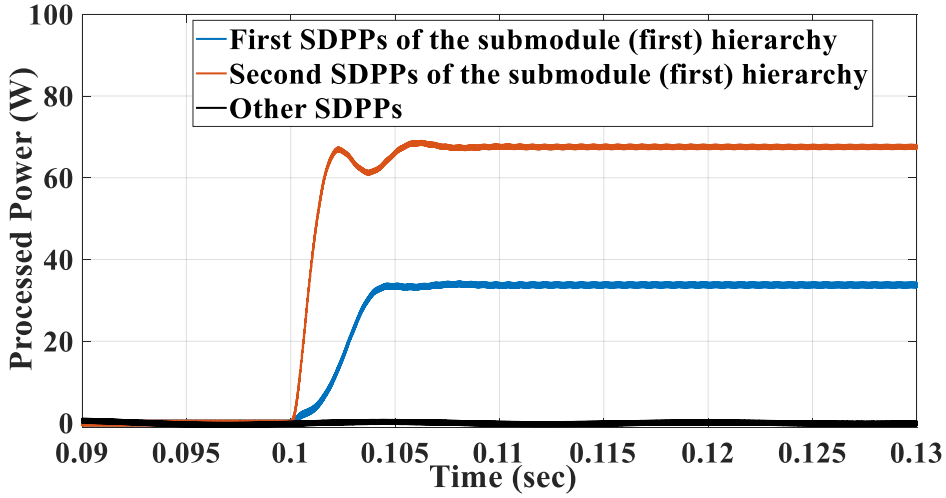

Figure 6.6.: Power Processed by the SDPP converters in Scenario 1.

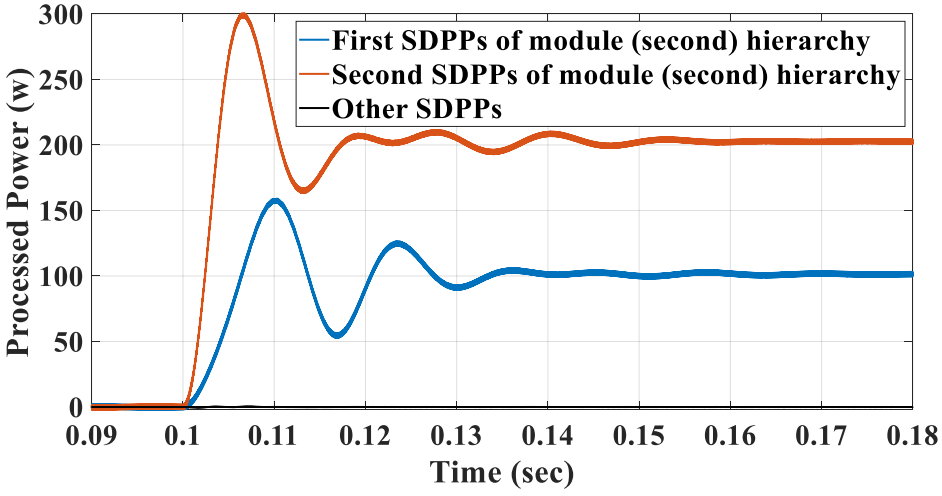

Figure 6.7.: Power Processed by the SDPP converters in Scenario 2.

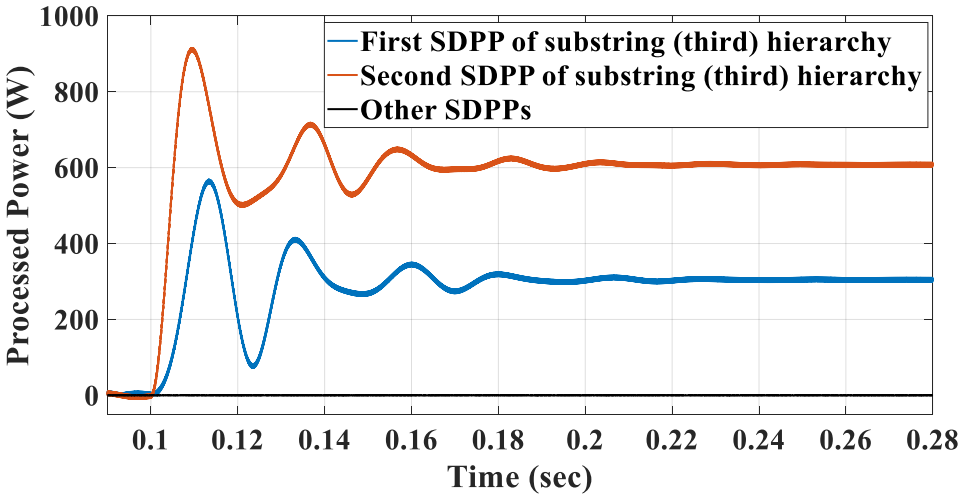

Figure 6.8.: Power Processed by the SDPP converters in Scenario 3.

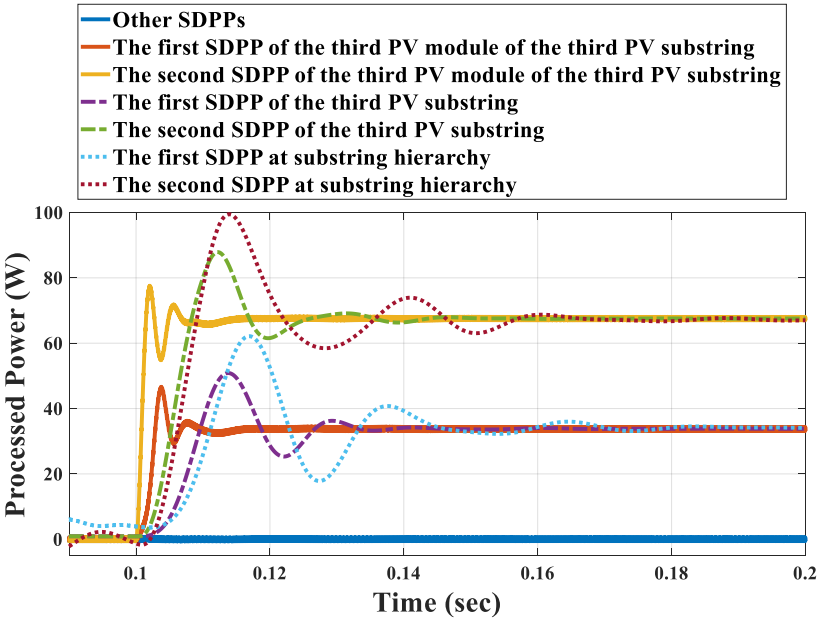

Figure 6.9.: Power Processed by the SDPP converters in Scenario 4.

6.3. OVERVIEW OF THE PROPOSED PV2VB SPDPP ARCHITECTURE

As discussed in Section 6.2, although the hierarchical PV2PV SDPP can mitigate the accumulation effect, it still has two major drawbacks: (i) the use of high-voltage-rated components in the outer hierarchies and (ii) a lack of modularity due to varying voltage and power ratings across hierarchies. To overcome these issues, PV2VB SDPP, which does not suffer from these limitations, has been selected for the SDPP part of the SPDPP architecture.

In the PV2VB SPDPP architecture, the primary sides of the SLCs and MICs are connected to the virtual buses, as shown in Fig. 6.10. When the architecture has N_S PV strings, each consisting of N_M PV modules, there will be $N_{SM} = N_S \times N_M$ PV modules, N_S module-level virtual buses, and one string-level virtual bus. This means the total number of objectives is:

$$N_T = N_{\mathrm{SM}} + N_{\mathrm{S}} + 1 \tag{6.34}$$

Therefore, N_T actuators are required to control all the objectives. To achieve this, the architecture includes N_{SM} MICs, N_S SLCs, and one central converter. The roles of each component within the architecture, their requirements, and potential topologies will be discussed in detail in the following subsections.

6.3.1. MICS

In this architecture, the primary sides of the MICs are connected to the module-level virtual buses, while the secondary sides are directly connected to the PV module terminals. The primary ports of MICs are connected in parallel. In turn, distributing the module-level virtual bus capacitor at the inputs of MICs is possible. Similar to the PV2VB SDPP architectures detailed in Chapter 2, subsection 2.4.1, the MICs in this setup are tasked with tracking the MPP of their respective PV modules and adhere to similar requirements.

6.3.2. SLCS

In the PV2VB SPDPP architecture, like the PV2VB PDPP architecture, the SLCs' primary sides connect to the string-level virtual bus, while their secondary sides are located between the PV string and the main bus. The primary goal of SLCs is to ensure that the module-level virtual buses are balanced. To achieve this, SLCs control the module-level virtual buses by manipulating the string currents. Besides, SLCs must add or subtract differential voltage between the main bus and the MPP voltage of their respective PV strings. It means SLCs connected to the PV strings

with high voltage must generate negative voltage, while the others are positive. Since the currents of PV strings are always positive (upward in Fig. 6.10), SLCs connected to the PV strings with high voltage inject the power to the string-level virtual bus, while the others extract the power from the string-level virtual bus. In other words, SLCs must also establish a path for efficient power transfer to and from the string-level virtual bus.

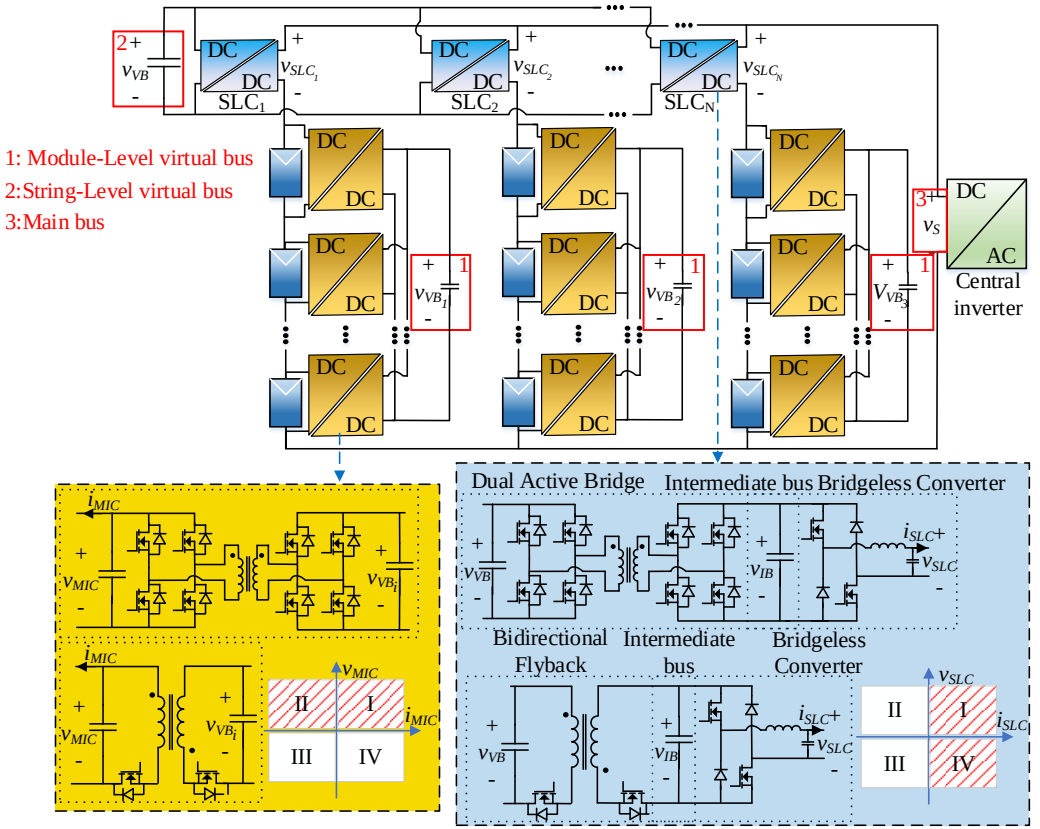

Figure 6.10.: Schematic of the proposed PV2VB SPDPP architecture with their possible associated SLCs and MICs topologies.

As also discussed in Chapter 3, various topologies can be utilized for SLCs as long as they incorporate three key features. Firstly, they must be capable of operating efficiently in both the first and fourth quadrants of the V-I curve, as previously discussed. Additionally, isolation is critical to allow independent voltage control of each PV string and to ensure that the current from the i^{th} PV string is confined to flow through its respective i^{th} SLC. To explain more, it is considered the case that the DAB converters (isolated DC-DC converter stage) have been removed and only utilize BL converters (non-isolated DC-DC converter stage) as SLCs. Furthermore, it is considered a scenario where PV strings 1 and 2 generate currents with magnitudes I_{SLC_1} and I_{SLC_2}, respectively. Ideally, I_{SLC_1} must flow through SLC1, and I_{SLC_2} must flow through SLC2, as depicted in Fig. 6.11 (a) below. However, due to, e.g., minor differences in the SLC parameters, which can be attributed to factors such as parasitic elements, the current from PV string 2 might instead flow through SLC1 (Fig. 6.11 (b)). This situation is undesirable as it leads to increased losses, thermal stress, and the power rating of the SLCs. It should be noted that this imbalance can occur with changing switching sequences, not just in the example provided above. Therefore, employing isolated topologies ensures that the current from the i^{th} PV string exclusively flows through the i^{th} SLC, maintaining system balance and efficiency.

BF converters are well-suited for the first stage of SLCs due to their simplicity and ability to provide galvanic isolation. However, their use is typically restricted to power levels of a few hundred watts. For higher power levels, exploring alternative topologies better suited for such applications becomes necessary while it is possible to keep using BL converters for the second stage (Fig. 6.10).

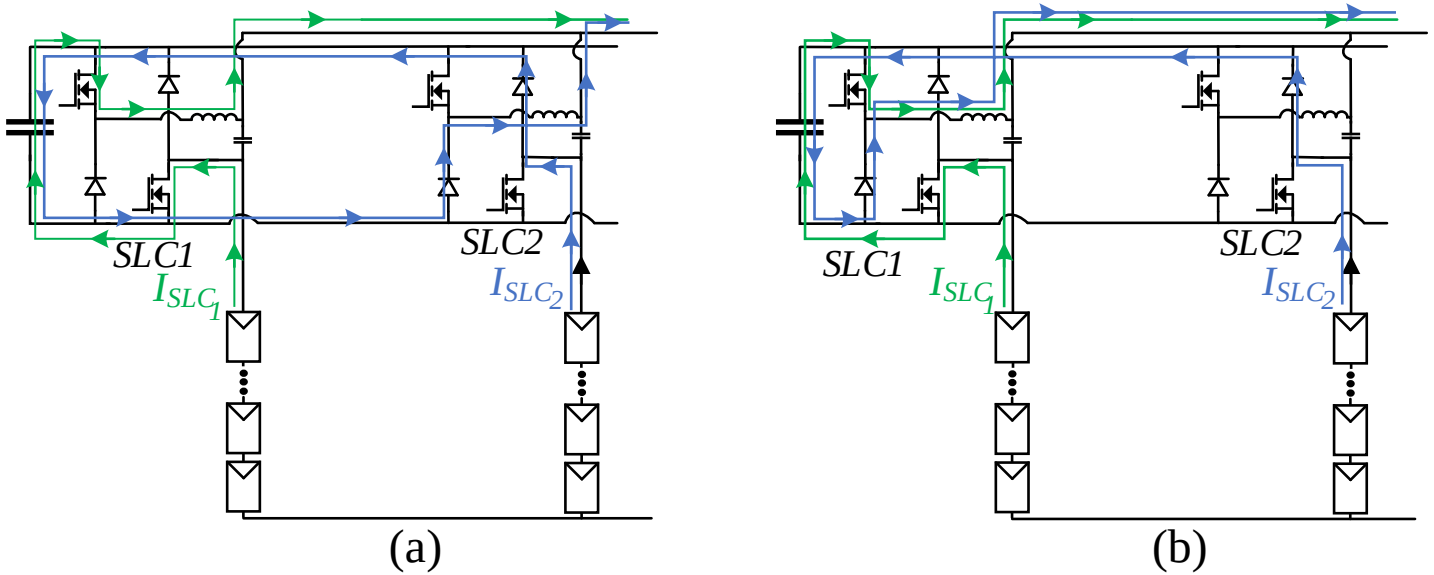

Figure 6.11.: The direction of the currents generated by PV strings in PV2VB PDPP architecture with non-isolated SLCs: (a) Ideal current path, and (b) Non-ideal practical current path.

6.3.3. CENTRAL CONVERTER

In a PV2VB SPDPP architecture, the central converter plays a crucial role in regulating the string-level virtual bus voltage by adjusting the main bus voltage. Specifically, the string-level virtual bus voltage (v_{VB}) is controlled through manipulation of the main bus voltage. The central converter can be either a DC-DC or DC-AC converter, depending on whether it is connected to a DC or AC grid. Unlike the SLCs and MICs, the central converter does not need to adhere to any specific requirements.

6.4. CONTROL STRATEGY FOR THE PROPOSED PV2VB SPDPP ARCHITECTURE

In the PV2VB SPDPP architecture, while ensuring MPP for all PV modules, it is crucial to maintain the module-level and string-level virtual bus voltages at a constant level. Achieving this requires various control loops, as illustrated in Fig. 6.12. The following subsections will explain the controllers and their operating principles, supported by mathematical equations.

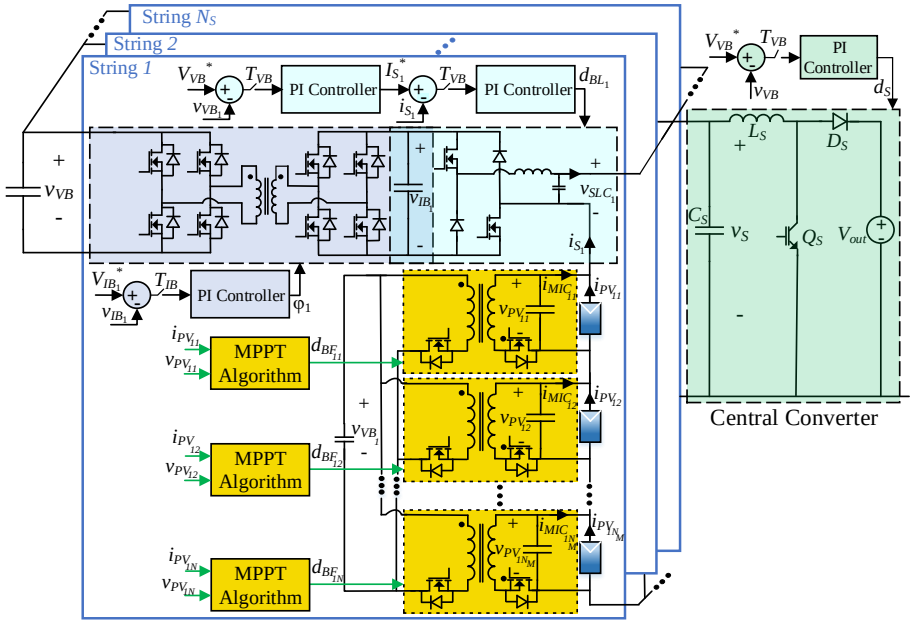

Figure 6.12.: PV2VB SPDPP architecture with the associated central converter, SLCs, and MICs topologies considered in this study and required control loop and MPPT blocks.

6.4.1. MICS

In the PV2VB SPDPP architecture, the primary function of the MICs is to ensure that each PV module operates at its MPP. To achieve this, the i^{th} MIC of the j^{th} PV string continuously monitors the voltage ($v_{PV_{ij}}$) and current ($i_{PV_{ij}}$) of its corresponding PV module, as depicted in Fig. 6.12. The chosen MPPT algorithm then adjusts the control variables to track the module's MPP. However, the output voltage of the MICs, which defines the PV module's operating voltage, is closely linked to the module-level virtual bus voltage. Thus, regulating and stabilizing the virtual bus voltage is critical to prevent interference with the MPPT algorithm and ensure consistent performance.

6.4.2. SLCS

In a PV2VB SPDPP architecture, the SLCs manage their output current (i_{SLC}) to maintain system performance. However, the primary objective of this control mechanism is to stabilize the module-level virtual bus voltages (v_{VB_j}). This section explores the connection between the output current of the j^{th} SLCs output current (i_{SLC_j}) and j^{th} module-level virtual bus voltage (v_{VB_j}). For simplicity, it is assumed that the converters are lossless. Based on these assumptions, the power relationship within the architecture can be derived as follows:

$$p_{\mathrm{VB}_j} = p_{\mathrm{out}_j} - p_{\mathrm{in}_j} \tag{6.35}$$

In the context of the proposed architecture, p_{VB_j}, p_{out_j}, and p_{in_j} represent the instantaneous j^{th} module-level virtual bus power, power delivered to the j^{th} string, and power generated by the PV modules of the j^{th} string, respectively; these values can be computed as follows:

$$p_{\mathrm{VB}_j} = C_{\mathrm{VB}_M} \cdot v_{\mathrm{VB}_j} \cdot \frac{dv_{\mathrm{VB}_j}}{dt} \tag{6.36}$$

$$p_{out_j} = v_{PV_{S_j}} \cdot i_{\mathrm{SLC}_j} = \sum_{i=1}^{N_M} v_{\mathrm{PV}_{ij}} \cdot i_{\mathrm{SLC}_j} \tag{6.37}$$

$$p_{\mathrm{in}_j} = \sum_{i=1}^{N_M} v_{\mathrm{PV}_{ij}} \cdot i_{\mathrm{PV}_{ij}} \tag{6.38}$$

Where C_{VB_M} and $v_{PV_{S_j}}$ represent module-level virtual bus capacitance and summation of PV modules voltage of j^{th} string, respectively; the

following equation can be obtained by substituting equations (6.36)–(6.38) in equation (6.35):

$$p_{VB_j} = \frac{dv_{VB}}{dt} \cdot C_{VB_M} \cdot v_{VB_j} = \sum_{i=1}^{N_M} v_{PV_{ij}} \cdot i_{PV_{ij}} - v_{PVS_j} \cdot i_{SLC_j} \tag{6.39}$$

It's crucial to recognize that MICs govern the current and voltage of PV modules to ensure they operate at their MPPs. Additionally, v_{PVS_j} naturally corresponds to the sum of the individual PV module voltages in the j^{th} string. Therefore, the only controllable variable for managing the module-level virtual bus power—and by extension, the module-level virtual bus voltage—is the SLC current. When the average power of the virtual bus at the module level is kept at zero, the following equation is obtained:

$$P_{\mathrm{VB}_j} = 0 \rightarrow I^*_{\mathrm{SLC}_j} = \frac{\sum_{i=1}^{N_M} V_{\mathrm{MPP}_{ij}} \cdot I_{\mathrm{MPP}_{ij}}}{\sum_{i=1}^{N_M} V_{\mathrm{MPP}_{ij}}}, \quad V_{\mathrm{VB}_j} = \mathrm{const} \tag{6.40}$$

Where $I^*_{SLC_j}$ is the equilibrium SLC current at which the module-level virtual bus voltage is constant. It is important to note that capital letters represent the steady-state values of the variables. By combining Equations (6.39) and (6.40), the following equation can be derived, which describes the instantaneous rate of change of the virtual bus voltage as a function of the SLC output current:

$$\frac{dv_{\mathrm{VB}_j}}{dt} = \frac{\sum_{i=1}^{N_M} V_{\mathrm{MPP}_{ij}} \cdot I_{\mathrm{MPP}_{ij}}}{C_{\mathrm{VB}_M} \cdot v_{\mathrm{VB}}} \cdot \left(1 - \frac{i_{\mathrm{SLC}_j}}{I^*_{\mathrm{SLC}_j}}\right) \tag{6.41}$$

Equation (6.41) shows the virtual bus voltage rises when the SLC output current voltage drops below the equilibrium level and vice versa. Both topologies proposed for the SLCs consist of two stages, with their performance decoupled by an intermediate bus capacitor, referred to as the decoupling capacitor. When DAB converters are employed as the first stage, the voltage of this intermediate bus is regulated by controlling the phase shift (φ) between the two AC voltage waveforms across the windings of the isolation transformer, using a closed-loop controller. Power is transferred from the leading bridge to the lagging bridge based on this phase shift.

6.4.3. CENTRAL CONVERTER

In the PV2VB SPDPP architecture, the central converter regulates the main bus voltage (v_S) through its duty cycle. However, this regulation primarily aims to stabilize the string-level virtual bus voltage (v_{VB}), as

shown in Fig. 6.12. Using a procedure similar to Chapter 3, the following equation is derived:

$$P_{\text{VB}} = 0 \rightarrow V_S^* = \frac{\sum_{j=1}^{N_S} V_{PV_{S_j}} \cdot I^*_{\text{SLC}_j}}{\sum_{j=1}^{N_S} I^*_{\text{SLC}_j}},\ V_{\text{VB}} = \text{const} \tag{6.42}$$

Where V_S^* represents the equilibrium main bus voltage, at which the string-level virtual bus voltage remains constant. Additionally, the instantaneous rate of change of the string-level virtual bus voltage as a function of the main bus voltage can be derived as follows:

$$\frac{dv_{\text{VB}}}{dt} = \frac{\sum_{j=1}^{N_S} V_{PV_{S_j}} \cdot I_{\text{SLC}_j}}{C_{\text{VB}_S} \cdot v_{\text{VB}}} \cdot \left(1 - \frac{v_S}{V_S^*}\right) \tag{6.43}$$

where C_{VB_S} represents the string-level virtual bus capacitance. Equation (6.43) indicates that the string-level virtual bus voltage increases when the main bus voltage drops below the equilibrium level, and decreases when the main bus voltage exceeds the equilibrium level.

6.5. DESING CONSIDERATIONS FOR THE PROPOSED PV2VB SPDPP ARCHITECTURE

6.5.1. MODULE-LEVEL VIRTUAL BUSES AND MICS RATING

Since the primary side of the MICs is connected to the module-level virtual bus, the voltage rating of the primary side components is dependent on the module-level virtual bus voltage. Selecting a very low voltage for the module-level virtual bus increases the required capacitance as the maximum allowable voltage ripple decreases [8]. Additionally, low virtual bus voltage results in higher conduction losses for the DPP converters due to increased current. Conversely, selecting a very high module-level virtual bus voltage requires components with higher voltage ratings, leading to increased costs and switching losses. To achieve a 1:1 conversion ratio and allow for symmetrical implementation on both the primary and secondary sides of the MICs, it is recommended that the module-level virtual bus voltage be set close to the nominal MPP voltage of the PV modules, denoted as V_{MPP_n}. MICs in a string are activated when a current mismatch occurs among the PV modules within that string. In the worst-case scenario, the power rating of the MICs is equal to:

$$\frac{P_{\text{MIC}}}{I_{\text{MPP}_n} \cdot V_{\text{MPP}_n}} = \frac{N_M - 1}{N_M} \tag{6.44}$$

Where I_{MPP_n} represents the nominal MPP current of the PV modules. However, such extreme mismatch conditions are rare. The impact of reduced MIC ratings in the SDPP architecture has been studied in detail over long-term scenarios in [9].

6.5.2. STRING-LEVEL VIRTUAL BUS AND SLCS RATING

In the architecture, the primary sides of SLCs first stage are connected to the string-level virtual bus, while the secondary sides are linked to the intermediate bus voltage. Consequently, the voltage rating of the first stage (DAB or BF converters) is determined by the voltage at the intermediate bus. Similar to MICs, to maintain a 1:1 conversion ratio and facilitate symmetrical implementation on both the primary and secondary sides of the first stage, it is advisable to select the string-level virtual bus voltage to be close to the intermediate bus voltage (V_{IB_j}). In contrast to MICs, SLCs begin processing power when voltage mismatches occur among PV strings. A comprehensive power rating analysis of SLCs can be found in Chapter 3.

In the SPDPP architecture, unlike the PV2VB PDPP architecture, the voltage differences between PV strings are generally insignificant, particularly when DMPPT is implemented at the submodule level. In this scenario, there are no bypass diodes to circumvent a PV submodule, and the effects of irradiance mismatch or temperature variation on submodule-level MPP tracking are relatively minor. As a result, the voltage discrepancies between strings will not be as pronounced as in the PV2VB PDPP architecture when all PV modules are functioning. This allows for selecting a string-level virtual bus voltage lower than that in the PV2VB PDPP architecture.

However, suppose short-circuited PV modules occur within a PV string, resulting in a drop in the string voltage. In that case, the SLCs must generate sufficient voltage to compensate for the differential voltage between the main bus voltage and the PV string voltage to ensure operation at the MPP. Therefore, selecting a very low voltage for the string-level virtual bus is not advisable. Ultimately, selecting the appropriate string-level virtual bus voltage primarily depends on fault conditions rather than shading.

While BF converters are preferred for MICs, the situation differs for SLCs, which may require higher power ratings. BF converters are typically limited to power outputs of a few hundred watts, making them less suitable for SLCs. As a result, DAB converters are favored for this application. In this study, BF converters are employed for the MICs, while DAB converters are utilized for the first stage of the SLCs.

6.5.3. CONTROLLERS

Assuming a search-based MPPT algorithm like P&O, the architecture incorporates three distinct control loops: (i) a central controller that regulates the string-level virtual bus voltage, (ii) SLC controllers that adjust the module-level virtual bus voltages, and (iii) controllers that manage the intermediate bus voltage within an SLC, as illustrated in Fig. 6.12. In contrast to the third controller, the first two controllers, which regulate the main bus voltage and string current, may inadvertently disrupt the operation of the MPPT algorithm. Therefore, achieving a harmonious control mechanism that effectively integrates with the MPPT algorithms requires a thoughtful approach. To mitigate interference between the SLC controllers and the MPPT algorithm, it is advisable to extend the sampling times of these controllers. This can be expressed mathematically as follows:

$$T_{\mathrm{VB}} = T_{\mathrm{VB}_M} = \lceil 4 \cdot m \cdot T_{\mathrm{MPPT}} \rceil_{m=1,2,\ldots} \tag{6.45}$$

Where T_{VB}, T_{VB_M}, and T_{MPPT} represent the sampling time of the string-level virtual bus controller, the sampling time of the module-level virtual bus controller, and the perturbation period of the MPPT algorithm, respectively. By designing the controllers with these increased sampling times, the MPPT algorithms can operate independently without being hindered by premature or conflicting control actions from the controllers. This careful coordination is essential for maintaining accurate MPP tracking and optimizing the overall performance of the PV system.

6.6. REAL TIME SIMULATION RESULTS

This section highlights the ability of the proposed PV2VB SPDPP architecture to perform MPPT at the module level while maintaining constant module-level and string-level virtual bus voltages. Fig. 6.13 illustrates the real time simulation setup, consisting of two PLECS RT-Box-2 for the real time simulation model. The electrical specifications and component values of the architecture are summarized in Table. 6.4. As shown in Fig. 6.14, the evaluated architecture connects two PV strings to two SLCs, each comprising six series-connected PV modules equipped with an associated MIC. To assess the architecture's overall performance, two distinct tests were conducted: (i) partial shading, with an emphasis on evaluating the performance of the MICs, and (ii) PV modules bypassed, highlighting the functionality and effectiveness of the SLCs.

6.6.1. MISMATCHES CURRENT AMONG PV MODULES

In scenario I, all PV modules initially operate under uniform conditions. This is followed by a partial shading scenario, as illustrated in Fig. 6.14.

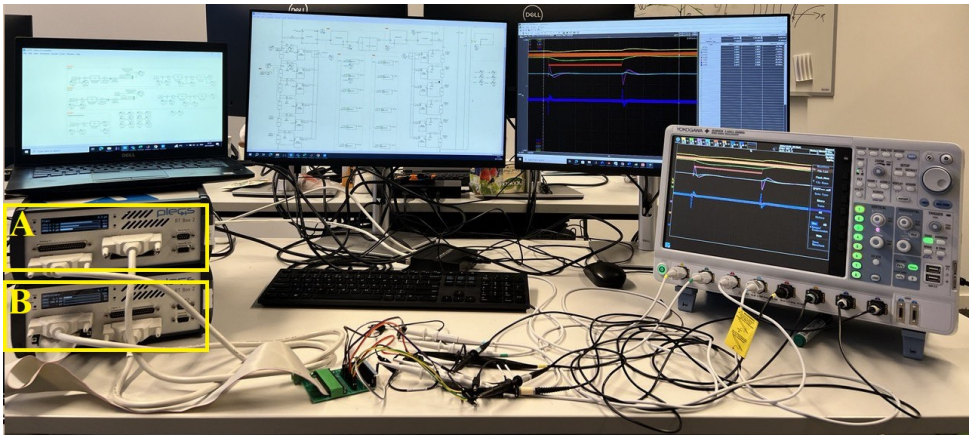

Figure 6.13.: Real time simulation setup with two PLECS RT-Box-2 (A) Plant and (B) controller real time simulations.

Table 6.4.: Electrical Specifications and Component Parameters of the System

Parameter	SYMBOL	VALUE
PV system rated power	P_{sys}	4 kW
String-level virtual bus voltage	V_{VB}	200 V
Module-level virtual bus voltage	V_{VB_j}	70 V
MPP voltage of the PV module	V_{MPP}	64 V
MPP current of the PV module	I_{MPP}	5.3 A
MPPT algo perturbation period	T_{MPPT}	5 ms
Sampling Time of Controllers	$T_{\text{VB}}, T_{\text{VB}_M}$	20 ms
String-level virtual bus capacitance	C_{VB}	10 mF
Module-level virtual bus capacitance	C_{VB_M}	40 mH
Switching frequency	f_{SW}	10 kHz
Discretization time step of real-time simulation	T_{disc}	6.25μs

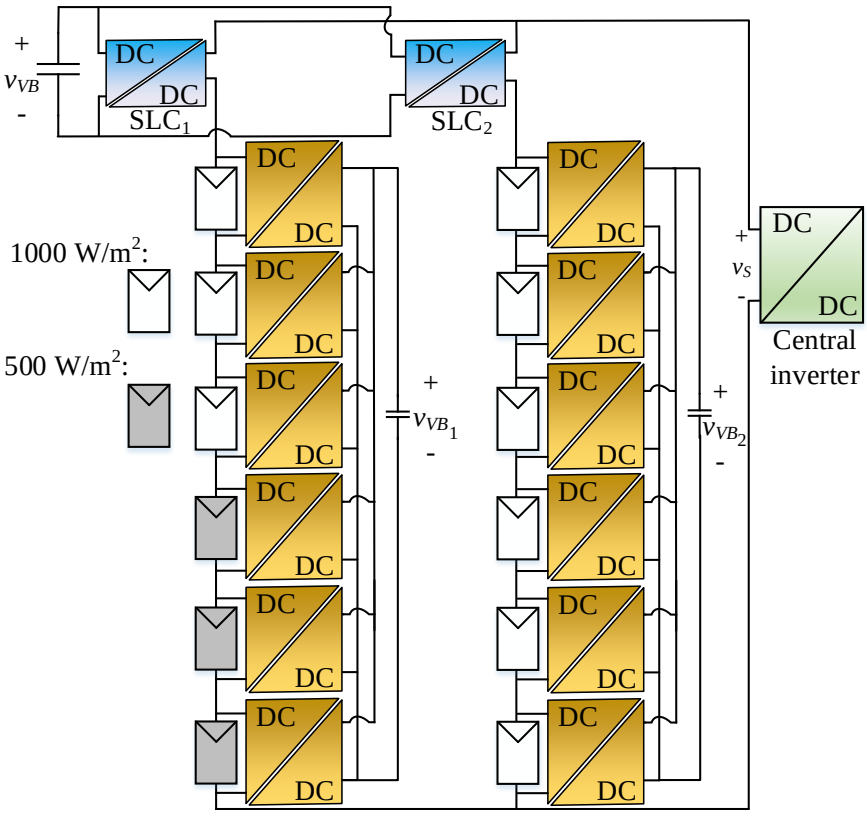

Figure 6.14.: Evaluated PV2VB SPDPP architecture in RT PLECS boxes.

After 10 seconds, the system is restored to uniform conditions to evaluate the architecture's overall performance, particularly focusing on the performance of the MICs. During this assessment, there is no voltage mismatch between string 1 and string 2.

Fig. 6.15 illustrates the voltage waveforms of the module-level virtual buses, the string-level virtual bus, and the main bus during scenario I. The results demonstrate that the controllers effectively maintain the virtual bus voltages at module and string levels. After each disturbance, the voltages successfully return to their desired values. Furthermore, the following observations are noted:

Module-Level Virtual Buses: In String 1, current mismatches among the PV modules result in voltage variations on the associated module-level virtual buses. In contrast, as no mismatches occur in String 2, its module-level virtual bus remains largely unaffected.

String-Level Virtual Bus: Since there are no mismatches among the PV string voltages, the string-level virtual bus voltage remains stable and unaffected by disturbances.

Main Bus Voltage: The main bus voltage closely follows the value predicted by Equation (6.42), thereby validating the mathematical model presented. These findings confirm the system's capability to manage voltage dynamics effectively under the given conditions.

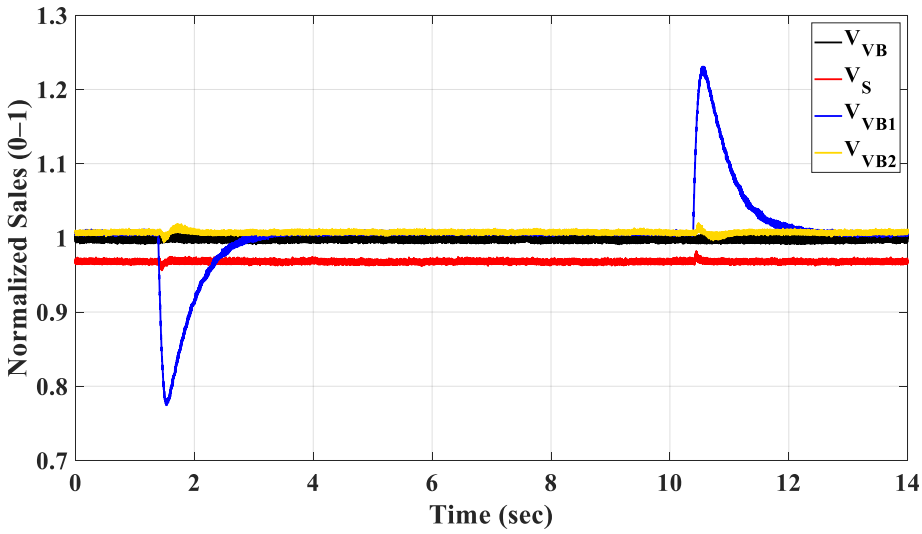

Figure 6.15.: Normalized voltage waveform (V_{VB_1}&V_{VB_2}, V_{VB}, and V_S are normalized by 70 V, 200V, and 400 V, respectively). Scenario I: PV modules transitions from uniform condition to current mismatch conditions shown in Fig. 6.14, and then return to the uniform condition.

Fig. 6.16 presents the current of a shaded PV module ($I_{PV_{sh}}$) and an unshaded PV module ($I_{PV_{ush}}$). The figure demonstrates that the architecture can effectively track the MPP of PV modules during transitions. Key observations include:

Tracking MPP: The MPP currents of both shaded and unshaded PV modules adjust appropriately during transitions, highlighting the architecture's ability to adapt to varying shading conditions and maintain optimal power extraction.

Impact of Mismatches in String 1: Mismatches only occur in string 1, leading to changes in its current (I_{SLC_1})as determined by Equation (6.41). This adjustment ensures the module-level virtual bus voltage remains constant at 70 V. In contrast, the current of string 2 (I_{SLC_2}) remains unaffected, as no mismatches are present in string 2. Together, Fig. 6.15

and Fig. 6.16 confirm the effective performance of the PV2VB SPDPP architecture in handling current mismatches among PV modules while maintaining system stability and efficient operation.

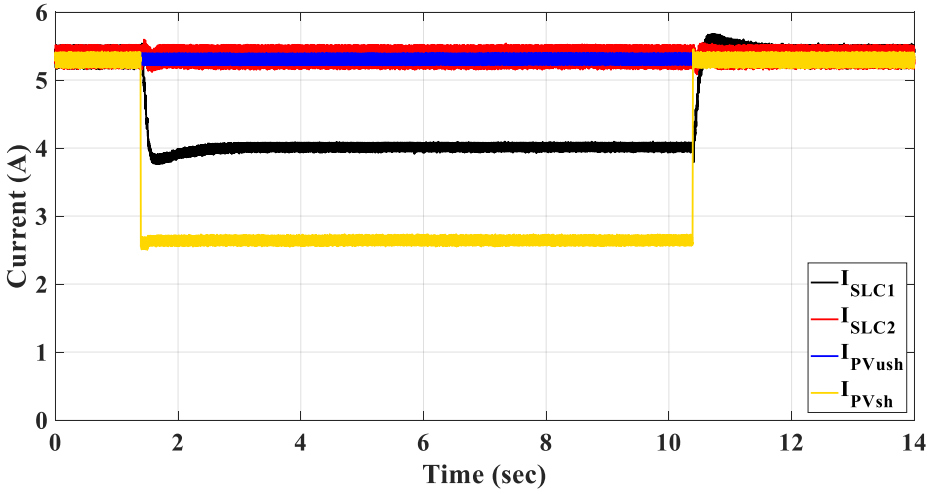

Figure 6.16.: Current waveform. Scenario I: PV modules transition from uniform condition to current mismatch conditions shown in Fig. 6.14, and then return to the uniform condition.

6.6.2. VOLTAGE MISMATCHES AMONG PV STRINGS

In Scenario II, mismatches among PV string voltages are introduced to assess the system's response and performance. In this scenario, initially, all PV modules operate under uniform conditions, ensuring no mismatches in the system. Then, at approximately 2.3 seconds, three out of six PV modules in string 1 transition to generate an I-V curve 2 (as shown in Fig. 6.17), while the remaining modules generate an I-V curve 1. This results in a voltage mismatch between String 1 and String 2. Finally, after 10 seconds, all PV modules return to their uniform conditions, eliminating the voltage mismatch. This scenario is designed to evaluate the PV2VB SPDPP architecture's ability to manage voltage mismatches among PV strings dynamically and maintain stable system performance during transitions.

Fig. 6.18 illustrates the voltage waveforms of the module-level virtual buses, string-level virtual bus, and main bus during scenario II. The voltage mismatches in PV modules of string 1 lead to observable variations in all virtual buses. This is expected, as the mismatch creates

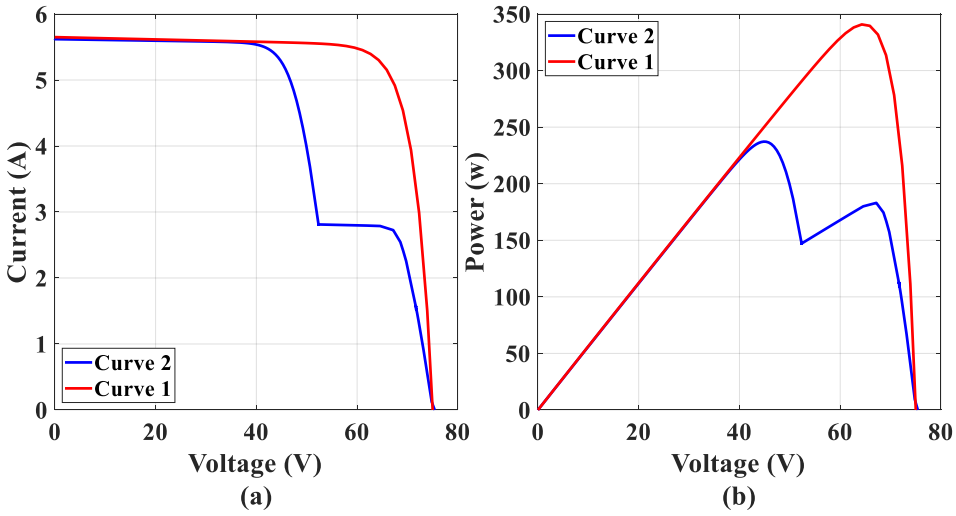

Figure 6.17.: PV module. (a) I-V curves. (b) P-V curves were used in the real time simulation.

voltage imbalances between the two strings. Moreover, the module-level virtual bus associated with string 1 experiences more pronounced voltage variation due to the localized nature of the mismatches within this string. Besides, Fig. 6.18 shows the despite the disturbances, the system effectively restores the string-level virtual bus voltages to the desired value of 200 V by manipulating the main bus voltage according to Equation (6.42). Fig. 6.18 thus validates the ability of the PV2VB SPDPP architecture to manage and mitigate the effects of voltage mismatches effectively.

Fig. 6.19 illustrates that both strings operate at 385 V under uniform conditions. However, when a mismatch occurs, string 1 and string 2 operate at 385 V and 330 V, respectively, which correspond to the summation of the MPP voltages of their associated PV modules. This demonstrates that the proposed architecture effectively handles voltage mismatches between strings. Furthermore, according to Equation (6.40), since the global MPP current of the PV modules remains unchanged before and after introducing the mismatch, the equilibrium currents in the strings also remain constant. This observation is validated through real time simulation. As shown in Fig. 6.18 and Fig. 6.19, the architecture exhibits rapid MPP tracking while gradually adjusting the virtual bus voltages. This behavior indicates that the slower response of the central controller does not compromise MPPT efficiency.

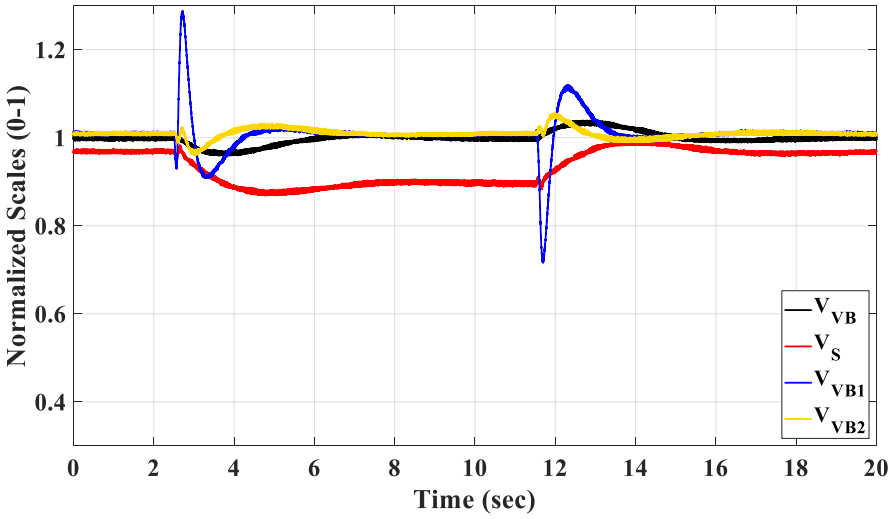

Figure 6.18.: Normalized voltage waveform (V_{VB_1}&V_{VB_2}, V_{VB}, and V_S are normalized by 70 V, 200V, and 400 V, respectively). Scenario II: three PV modules in string 1 from uniform condition to voltage mismatch conditions shown in Fig. 6.17, and then return to the uniform condition.

6.7. CONCLUSION

This chapters delve into a novel PV2VB SPDPP architecture for photovoltaic systems, designed to effectively mitigate both current and voltage mismatches among PV modules and strings. The study thoroughly elaborates on the system's mathematical framework and control methods, detailing the requirements for SLCs, MICs, controllers, and the overall architecture. Real time simulations validate the architecture's performance, demonstrating its ability to maintain stable module-level and string-level virtual bus voltages while efficiently tracking the MPP of PV modules.

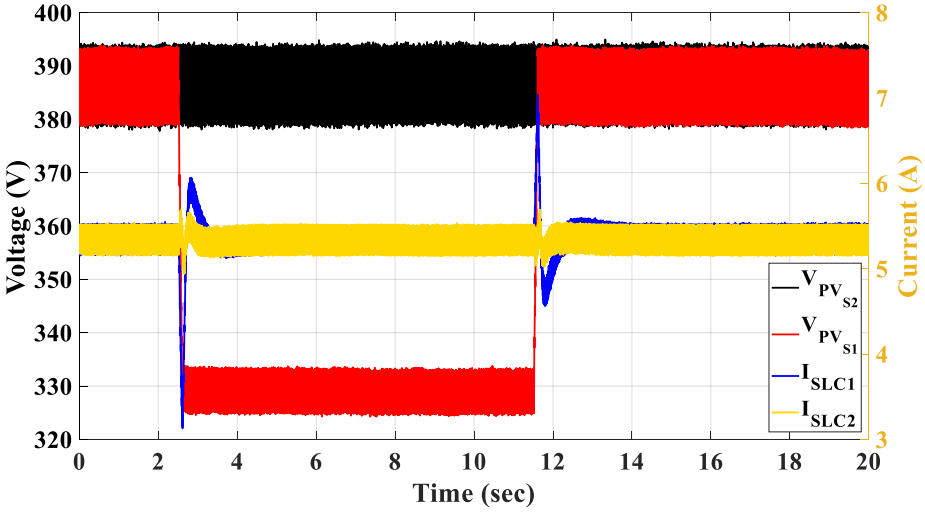

Figure 6.19.: Voltage and current of string waveform. Scenario II: three of PV modules in a string transition from uniform condition to voltage mismatch conditions shown in Fig. 6.17, and then return to the uniform condition.

REFERENCES

[1] A. Nazer, O. Isabella, H. Vahedi, and P. Manganiello. “Photovoltaic to Virtual Bus Series-Parallel Differential Power Processing for Photovoltaic systems”. In: *IEEE Open Journal of the Industrial Electronics Society,* "*Under Review*" (2025).

[2] A. Nazer, P. Manganiello, and O. Isabella. “Hierarchical PV to PV Series Differential Power Processing for Photovoltaic Applications: Power Flow and Converter Rating Analysis”. In: *Mathematics and Computers in Simulation* (2025).

[3] C. Liu, Y. Zheng, D. Li, and B. Lehman. “Distributed MPPT for modular differential power processing in scalable photovoltaic system”. In: *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2018, pp. 1098–1103.

[4] C. Liu, Y. Zheng, and B. Lehman. “PV Panel to PV Panel Transfer Method for Modular Differential Power Processing”. In: *IEEE Transactions on Power Electronics* (2021), pp. 1–1.

[5] M. Kasper, D. Bortis, and J. W. Kolar. “Unified Power Flow Analysis of String Current Diverters”. In: *Electrical Engineering* 100.3 (2018), pp. 2085–2094.

[6] H. J. Bergveld *et al.* “Module-Level DC/DC Conversion for Photovoltaic Systems: The Delta-Conversion Concept”. In: *IEEE Transactions on Power Electronics* 28.4 (2013), pp. 2005–2013.

[7] K. D. Waal, H. J. Bergveld, H. C. J. Buthker, and F. A. Schoofs. *Photovoltaic Assembly and Method of Operating a Photovoltaic Assembly*. Patent, Google Patents. 2014.

[8] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg. “A Review of Single-Phase Grid-Connected Inverters for Photovoltaic Modules”. In: *IEEE Transactions on Industry Applications* 41.5 (2005), pp. 1292–1306.

[9] C. Olalla, C. Deline, D. Clement, Y. Levron, M. Rodriguez, and D. Maksimovic. “Performance of Power-Limited Differential Power Processing Architectures in Mismatched PV Systems”. In: *IEEE Transactions on Power Electronics* 30.2 (2015), pp. 618–631.

7

CONCLUSION AND OUTLOOK

7.1. CONCLUSION

This dissertation presents advancements in the field of DPP architectures for PV systems, addressing critical challenges related to mismatch mitigation, efficiency, and system scalability. The proposed innovations have been thoroughly validated through modeling, simulation, and experimental testing, achieving the research objectives outlined in Chapter 1.

After a review of MPPT architectures (Chapter 2), in Chapter 3, a novel PV2VB PDPP architecture was successfully designed and implemented. By leveraging a virtual bus with a lower voltage than the main bus or PV strings, the architecture achieved reduced component voltage ratings without compromising performance. In Chapter 3, we demonstrated that SLCs need to generate both negative and positive voltage. Since the direction of the SLCs' output current is determined by the PV strings, and the current in a PV string is always outward, the SLCs must operate in the first and fourth quadrants of the V-I curve. Additionally, to prevent current circulation and unbalanced current distribution among SLCs, they must be isolated. Finally, as they are connected to the capacitive virtual bus, they must function as voltage source converters. Considering these requirements, a DAB converter followed by a BL converter was selected as the SLC topology. Experimental results demonstrated high system efficiency (excluding the power losses due to the MPPT algorithm), ranging from 96.4% to 99%, despite the SLCs having an efficiency range of 84.5% to 95%. These results confirm the feasibility and effectiveness of the design.

In Chapter 4, comprehensive dynamic modeling and small-signal analysis of the PDPP architecture provided valuable insights into its behavior. For modeling, three assumptions are made for simplicity: (i) the converters are considered lossless, (ii) the PV strings' small-signal model is assumed to be frequency-independent (purely resistive) at sufficiently

low frequencies, and (iii) the dynamic behavior of V_{out} is assumed to be negligible. These assumptions are also applied in simulations, so there exists a high similarity between system identification through simulation and the mathematical model. However, in experiments, these assumptions are not entirely valid, leading to small and acceptable discrepancies in the results of system identification through experiments and the mathematical model. Then, using the obtained mathematical model, the control strategies for stabilizing the virtual and intermediate bus voltages were optimized. Additionally, it was observed that while a simple PI controller is sufficient for DAB converters across a wide range of operations, the central converter requires an advanced controller to ensure fast and robust system operation. Experimental validation confirmed rapid voltage stabilization - within 0.6 seconds for the virtual bus and 15 milliseconds for intermediate bus voltages - enabling reliable MPPT for all PV strings under varying conditions.

In Chapter 5, the successful integration of a battery into the PV2VB PDPP architecture was achieved, enabling not only efficient energy storage and management but also maintaining the system's string-level DMPPT. In this architecture, the battery is positioned at the virtual bus. Unlike conventional architectures, where adding a battery requires additional power electronic converters, the proposed PV2VB PDPP architecture eliminates this need. In other words, the power electronic components remain unchanged, whether the battery is integrated or not, maintaining the same system configuration. This architecture enables the SLCs to operate at a voltage rating lower than that of the PV string, reducing component stress and improving overall system efficiency. The central converter is crucial in managing the battery's charging and discharging processes, ensuring optimal power distribution across the system. Through a comprehensive analysis of various operational states, the system's functionality was validated across different battery charge and discharge rates. The architecture effectively supports multiple operating modes, including SIDO-I, DISO-I, SISO-I, SISO-II, SISO-III, and SISO-IV. Experimental results further confirm the system's robustness, demonstrating string-level MPPT with an impressive efficiency range of 95.5% to 99%. By integrating the battery, the PV2VB PDPP architecture is better equipped to handle variations in solar irradiation, ensuring stable and continuous power delivery while improving energy management capabilities.

In Chapter 6, the research was further extended to develop a fully realized PV2VB SPDPP architecture capable of effectively mitigating power mismatches in both series-connected PV modules and parallel-connected PV strings. Chapter 6 begins by presenting a detailed mathematical analysis of the limitations of conventional and hierarchical PV2PV SDPP architectures, demonstrating that their inherent accumulation effect makes them unsuitable candidates for the

SDPP part of the SPDPP system. This theoretical foundation underscores the necessity for an alternative approach. To address these challenges, a novel PV2VB SPDPP architecture was proposed by integrating PV2VB SDPP with PV2VB PDPP. This architecture helps enhance the system's ability to manage mismatches while maintaining high operational efficiency. In this architecture, the combined use of SLCs and MICs enables module-level MPPT while simultaneously reducing power and voltage stress on individual components. Furthermore, Chapter 6 provides a comprehensive discussion of the architecture's control objectives, architecture actuators, and specific operational roles of the MICs, SLCs, and the central converter. Their coordinated functionality is essential for ensuring the stable operation of the system under varying environmental and load conditions. Finally, real-time simulations were conducted to validate the effectiveness of the proposed SPDPP architecture. The results confirm its ability to balance the virtual bus voltages while achieving module-level MPPT, thereby ensuring stable and efficient performance across diverse operational scenarios.

7.2. OUTLOOK

Based on the collective findings presented in this dissertation, several recommendations for future research are proposed, with references to specific chapters.

CHAPTER 3

- The innovation of this work lies in its architectural design. As detailed in this dissertation, the PV2VB PDPP architecture itself provides significant advantages over conventional solutions, making it a promising candidate for market adoption. However, to demonstrate the architecture's effective operation, robust and well-known DAB and bridgeless converters have been utilized as SLCs.These converters employ 10 active switches, potentially increasing the initial cost. To address this, developing new single-stage topologies as SLCs for the proposed architecture could be a promising direction to reduce costs while maintaining performance.

- In the PV2VB PDPP architecture, the central PI controller is responsible for setting an appropriate voltage to balance the virtual bus energy over a sampling period, thereby maintaining a constant virtual bus voltage. However, due to the discrete nature of the central controller and its higher sampling time compared to the MPPT perturbation period (see equation (4.39)), its limited visibility can result in oscillations on the virtual bus (Fig. 7.1). To mitigate this, selecting an appropriate virtual bus capacitance becomes critical to minimizing the magnitude of these voltage oscillations

and ensuring that system performance is not disrupted during the sampling time. By modifying equation (3.5), the following expression for virtual bus power can be derived:

$$p_{\mathrm{VB}}(t) = \sum_{i=1}^{N_{\mathrm{PV}}} v_{\mathrm{DPP}_i}(t) \cdot i_{\mathrm{PV}_i}(t) \tag{7.1}$$

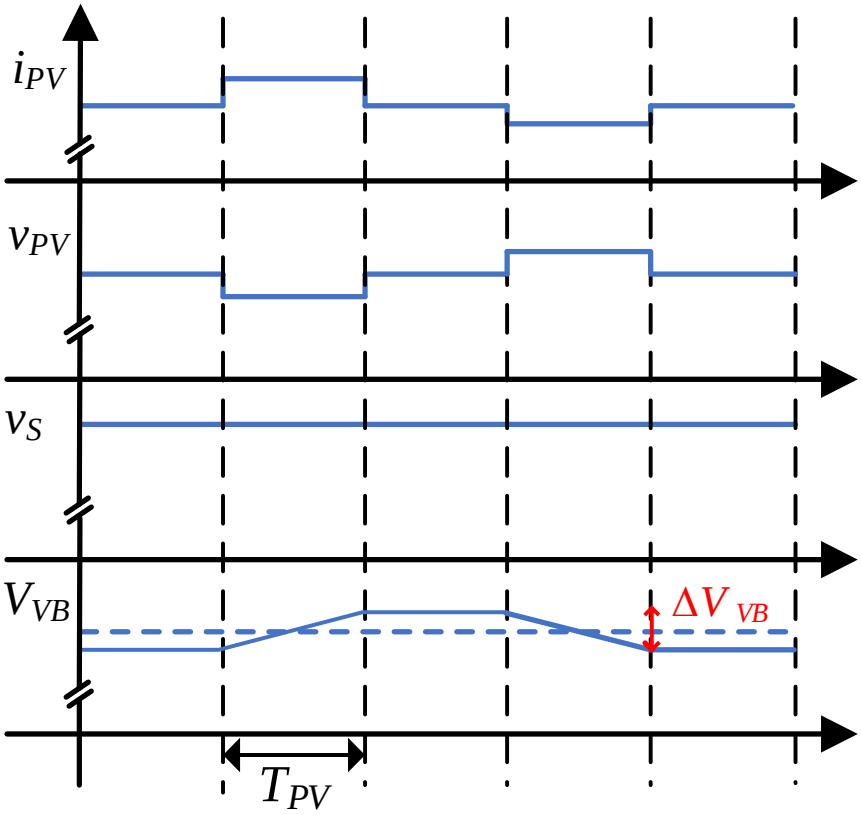

Figure 7.1.: Oscillation in the virtual bus voltage originates from oscillations in the MPPT process

Ideally, if there were no oscillation, the equation would be modified as follows:

$$P_{\mathrm{VB_{MPP}}} = \sum_{i=1}^{N_{\mathrm{PV}}} V_{\mathrm{DPP_{MPP}}_i} \cdot I_{\mathrm{PV_{MPP}}_i} = 0 \tag{7.2}$$

In practical scenarios, even though the virtual bus energy over a sampling period of the PI controller ($\Delta E^{+}_{\mathrm{VB}_{\mathrm{T_{VB}}}}$) is expected to be zero, as shown by:

$$\Delta E^{+}_{\mathrm{VB}_{\mathrm{T_{VB}}}} = \int_{0}^{T_{\mathrm{VB}}} p_{\mathrm{VB}}(t)\,dt = 0 \tag{7.3}$$

It is important to note that due to the influence of the MPPT algorithm, the virtual bus energy exhibits oscillations. During a single perturbation period, it may either charge ($\Delta E^{+}_{\mathrm{VB}_{\mathrm{MPPT_{PP}}}}$), rest ($\Delta E^{\circ}_{\mathrm{VB}_{\mathrm{MPPT_{PP}}}}$), or discharge ($\Delta E^{-}_{\mathrm{VB}_{\mathrm{MPPT_{PP}}}}$) the virtual bus energy as follows:

$$\Delta E_{\mathrm{VB}_{\mathrm{3PP}}} = \underbrace{\int_{0}^{T_{\mathrm{PV}}} p^{+}_{\mathrm{VB}}(t)\,dt}_{E^{+}_{\mathrm{VB}_{\mathrm{MPPT_{PP}}}}} + \underbrace{\int_{0}^{T_{\mathrm{PV}}} p^{\circ}_{\mathrm{VB}}(t)\,dt}_{E^{\circ}_{\mathrm{VB}_{\mathrm{MPPT_{PP}}}}} + \underbrace{\int_{0}^{T_{\mathrm{PV}}} p^{-}_{\mathrm{VB}}(t)\,dt}_{E^{-}_{\mathrm{VB}_{\mathrm{MPPT_{PP}}}}} = 0 \tag{7.4}$$

$$\Delta E^{+}_{\mathrm{VB}_{\mathrm{MPPT_{PP}}}} = T_{\mathrm{PV}} \sum_{i=1}^{N_{\mathrm{PV}}} \left((V_{\mathrm{DPP}_{\mathrm{MPP}_i}} - \Delta V_{\mathrm{DPP}_i}) \times (I_{\mathrm{PV}_{\mathrm{MPP}_i}} + \Delta I_{\mathrm{DPP}_i}) \right) \tag{7.5}$$

$$\Delta E^{\circ}_{\mathrm{VB}_{\mathrm{MPPT_{PP}}}} = T_{\mathrm{PV}} \sum_{i=1}^{N_{\mathrm{PV}}} \left(V_{\mathrm{DPP}_{\mathrm{MPP}_i}} \times I_{\mathrm{PV}_{\mathrm{MPP}_i}} \right) = 0 \tag{7.6}$$

$$\Delta E^{-}_{\mathrm{VB}_{\mathrm{MPPT_{PP}}}} = T_{\mathrm{PV}} \sum_{i=1}^{N_{\mathrm{PV}}} \left((V_{\mathrm{DPP}_{\mathrm{MPP}_i}} + \Delta V_{\mathrm{DPP}_i}) \times (I_{\mathrm{PV}_{\mathrm{MPP}_i}} - \Delta I_{\mathrm{DPP}_i}) \right) \tag{7.7}$$

The overall energy ($\Delta E_{\mathrm{VB}_{\mathrm{3PP}}}$) must be compensated by the energy of the virtual bus capacitor, so :

$$\Delta E^{+}_{\mathrm{VB}_{\mathrm{MPPT_{PP}}}} = \Delta E^{+}_{C_{\mathrm{PV}}} = \frac{1}{2} C_{\mathrm{VB}} \left(V^{2}_{\mathrm{VB}_{\mathrm{Max}}} - V^{2}_{\mathrm{VB}_{\mathrm{Min}}} \right) = C_{\mathrm{VB}} V_{\mathrm{VB}} \Delta V_{\mathrm{VB}} \tag{7.8}$$

However, the overall energy ($\Delta E_{\mathrm{VB}_{\mathrm{3PP}}}$) is unknown. Therefore, it is important to explore and understand the energy balance during MPPT further to optimize the PV2VB PDPP architecture performance.

CHAPTER 4

For the dynamic analysis, three assumptions are made for simplicity: (i) the converters are considered lossless, (ii) the PV strings' small-signal model is assumed to be frequency-independent (purely resistive) at sufficiently low frequencies, and (iii) the dynamic behavior of V_{out} is assumed to be negligible, with no significant influence on the overall architecture dynamics. Future studies can incorporate these effects to develop a more precise dynamic model.

CHAPTER 5

- In Chapter 5, the development of the PV2VB PDPP architecture model with capacitors placed on the virtual bus was carried out. However, the dynamic behavior of a battery significantly differs from that of a single capacitor, including charge diffusion, internal resistance variations, and state-of-charge (SoC) dependency, which influences its voltage and current characteristics over time. Given these fundamental differences, it is recommended that a dynamic analysis of the PV2VB PDPP architecture be conducted when applied to PV/Battery systems. This will facilitate the refinement of controller parameters, ensuring optimal energy harvesting from the PV source and seamless power management within the system.
- Future work should investigate the compatibility of the proposed architecture with the charging and discharging profiles required by various real-world battery systems employing different energy storage technologies.

CHAPTER 6

The proposed PV2VB SPDPP architecture is one example based on the PV2VB concept. As shown in the Fig. 7.2-7.4, there are theoretically other PV2VB SPDPP architectures with their own pros and cons.

- Fig. 7.2 illustrates a PV2VB SPDPP architecture with a single virtual bus for the primary side of all SLCs and MICs. This design requires only a single central virtual bus and eliminates the need for bidirectional converters in the SLCs, as power exchange is facilitated through the MICs. In this architecture, each MIC can track the MPP of the PV modules, and the central converter can regulate the virtual bus voltage; therefore, the SLCs can optimize *the performance of each string*, similar to PV2B structures. However, it suffers from excessive wiring and potentially complex control since SLCs and MICs exchange energy through a shared virtual bus.
- Fig. 7.3 presents a PV2VB SPDPP architecture with one virtual bus for the primary side of all SLCs and another for all MICs. While this

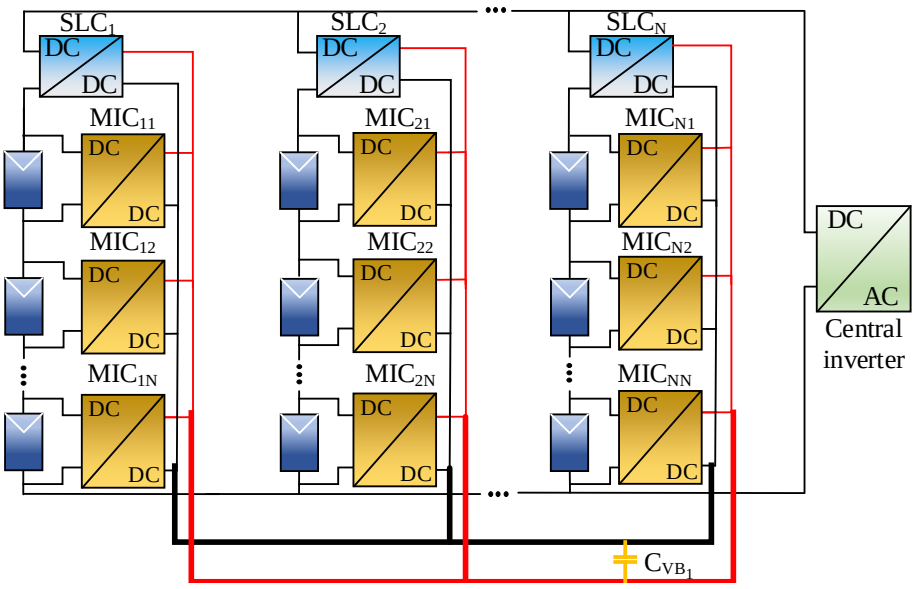

Figure 7.2.: A PV2VB SPDPP architecture with a single virtual bus for the primary side of all SLCs and MICs

architecture only requires two virtual buses and is less complex in terms of wiring compared to Fig. 7.2, it still has a relatively complex control system since all MICs exchange energy with a single virtual bus. Additionally, it requires bidirectional converters for the SLCs.

- Fig. 7.4 shows a PV2VB SPDPP architecture with N virtual buses for N strings. This design reduces control complexity and simplifies wiring compared to the previous solutions, making it more practically feasible. It also offers high modularity and does not require bidirectional converters for the SLCs. However, it needs N separate virtual buses for a system with N PV strings.
- Finally, it should be noted that, due to limitations in available equipment—such as the need for additional PV emulators to accurately replicate the behavior of PV modules—we restricted our validation to real-time simulations for the proposed PV2VB SPDPP architecture. Nevertheless, experimental testing on a physical prototype is essential for future work to provide stronger validation of the proposed PV2VB SPDPP architecture.

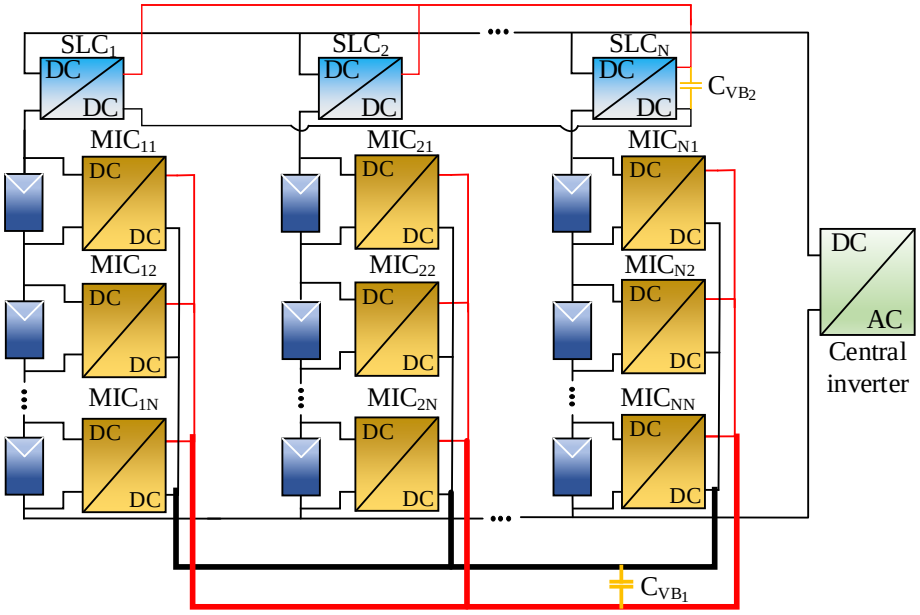

Figure 7.3.: A PV2VB SPDPP architecture with one virtual bus for the primary side of all SLCs and another for all MICs

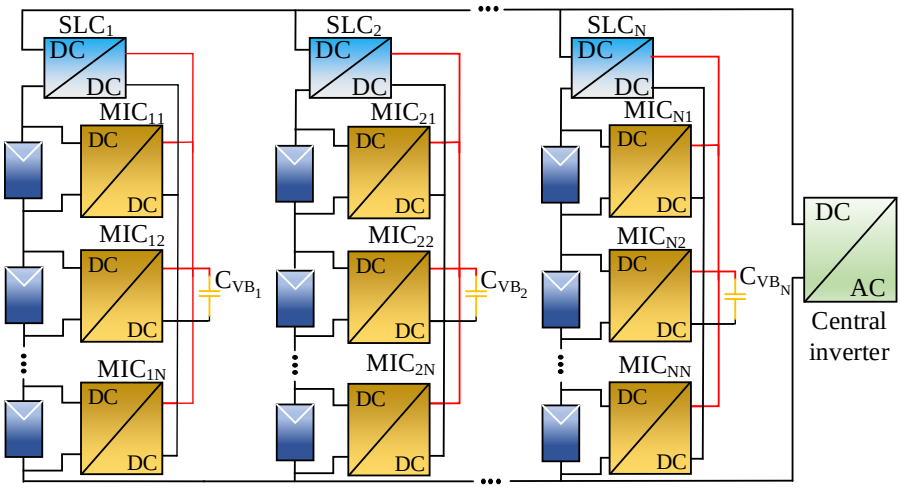

Figure 7.4.: A PV2VB SPDPP architecture with N virtual buses for N strings

A

COEFFICIENTS FOR DYNAMIC EQUATIONS

Taking into account Equations (4.9)–(4.14), the coefficients for the linearized equations (4.20)–(4.25) can be obtained in the following manner:

$$\frac{\partial g_{1_i}}{\partial \bar{v}_{\mathrm{SLC}_i}(t)} = \frac{-1}{C_{\mathrm{BL}} \cdot r_{\mathrm{PV}_i}} \tag{A.1}$$

$$\frac{\partial g_{1_i}}{\partial \bar{i}_{\mathrm{BL}_{L_i}}(t)} = \frac{1}{C_{\mathrm{BL}}} \tag{A.2}$$

$$\frac{\partial g_{1_i}}{\partial \bar{v}_S(t)} = \frac{1}{C_{\mathrm{BL}} \cdot r_{\mathrm{PV}_i}} \tag{A.3}$$

$$\frac{\partial g_{2_i}}{\partial \bar{i}_{\mathrm{BL}_{L_i}}(t)} = \frac{-(2 \cdot D_{\mathrm{BL}_i} - 1)}{C_{\mathrm{BL}}} \tag{A.4}$$

$$\frac{\partial g_{2_i}}{\partial \bar{v}_{\mathrm{VB}}(t)} = \frac{\varphi_i \cdot (1 - 2 \cdot \varphi_i)}{N_T \cdot f_{\mathrm{sw}} \cdot L_{\mathrm{DAB}} \cdot C_{\mathrm{BL}}} \tag{A.5}$$

$$\frac{\partial g_{2_i}}{\partial \varphi_i(t)} = \frac{V_{\mathrm{VB}} \cdot (1 - 4 \cdot \varphi_i)}{N_T \cdot f_{\mathrm{sw}} \cdot L_{\mathrm{DAB}} \cdot C_{\mathrm{BL}}} \tag{A.6}$$

$$\frac{\partial g_{2_i}}{\partial \bar{d}_{\mathrm{BL}_i}(t)} = \frac{-2 \cdot I_{\mathrm{BL}_i}}{C_{\mathrm{BL}}} \tag{A.7}$$

$$\frac{\partial g_{3_i}}{\partial \bar{v}_{\mathrm{SLC}_i}(t)} = \frac{-1}{L_{\mathrm{BL}}} \tag{A.8}$$

$$\frac{\partial g_{3_i}}{\partial \bar{v}_{\mathrm{IB}_i}(t)} = \frac{2 \cdot D_{\mathrm{BL}_i} - 1}{L_{\mathrm{BL}}} \tag{A.9}$$

A

$$\frac{\partial g_{3_i}}{\partial \bar{d}_{\mathrm{BL}_i}(t)} = \frac{2 \cdot V_{\mathrm{BL}_i}}{L_{\mathrm{BL}}} \tag{A.10}$$

$$\frac{\partial g_4}{\partial \bar{v}_{\mathrm{SLC}_i}(t)} = \frac{1}{C_s \cdot r_{\mathrm{PV}_i}} \tag{A.11}$$

$$\frac{\partial g_4}{\partial \bar{v}_S(t)} = \frac{-1}{C_s \cdot \sum_{t=1}^{N_{\mathrm{PV}}} r_{\mathrm{PV}_i}} \tag{A.12}$$

$$\frac{\partial g_4}{\partial \bar{i}_{L_s}(t)} = \frac{-1}{C_s} \tag{A.13}$$

$$\frac{\partial g_5}{\partial \bar{v}_S(t)} = \frac{1}{L_s} \tag{A.14}$$

$$\frac{\partial g_5}{\partial \bar{d}_s(t)} = \frac{V_{\mathrm{out}}}{L_s} \tag{A.15}$$

$$\frac{\partial g_6}{\partial \bar{v}_S(t)} = \frac{V_{\mathrm{IB}_i} \cdot (1 - 4 \cdot \varphi_i)}{N_T \cdot f_{\mathrm{sw}} \cdot L_{\mathrm{DAB}} \cdot C_{\mathrm{BL}}} \tag{A.16}$$

$$\frac{\partial g_{6_i}}{\partial \bar{v}_{\mathrm{IB}_i}(t)} = \frac{-\varphi_i \cdot (1 - 2 \cdot \varphi_i)}{N_T \cdot f_{\mathrm{sw}} \cdot L_{\mathrm{DAB}} \cdot C_{\mathrm{VB}}} \tag{A.17}$$

Then, state Matrix **A** is:

$$A = \begin{bmatrix} A_{11} & A_{12} & \cdots & A_{1N_{\mathrm{PV}}} & A_{1(N_{\mathrm{PV}}+1)} \\ A_{21} & A_{22} & \cdots & A_{2N_{\mathrm{PV}}} & A_{2(N_{\mathrm{PV}}+1)} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ A_{N_{\mathrm{PV}}1} & A_{N_{\mathrm{PV}}2} & \cdots & A_{N_{\mathrm{PV}}N_{\mathrm{PV}}} & A_{N_{\mathrm{PV}}(N_{\mathrm{PV}}+1)} \\ A_{(N_{\mathrm{PV}}+1)1} & A_{(N_{\mathrm{PV}}+1)2} & \cdots & A_{(N_{\mathrm{PV}}+1)N_{\mathrm{PV}}} & A_{(N_{\mathrm{PV}}+1)(N_{\mathrm{PV}}+1)} \end{bmatrix} \tag{A18}$$

$$A_{ii} \mid i = \{1, \ldots, N_{\mathrm{PV}}\} = \begin{bmatrix} \frac{\partial g_{1_i}}{\partial \bar{v}_{\mathrm{SLC}_i}(t)} & \frac{\partial g_{1_i}}{\partial \bar{i}_{\mathrm{BL}_{L_i}}(t)} & \frac{\partial g_{1_i}}{\partial \bar{v}_S(t)} \\ \frac{\partial g_{2_i}}{\partial \bar{v}_{\mathrm{SLC}_i}(t)} & \frac{\partial g_{2_i}}{\partial \bar{i}_{\mathrm{BL}_{L_i}}(t)} & \frac{\partial g_{2_i}}{\partial \bar{v}_{\mathrm{VB}}(t)} \\ \frac{\partial g_{3_i}}{\partial \bar{v}_{\mathrm{SLC}_i}(t)} & \frac{\partial g_{3_i}}{\partial \bar{i}_{\mathrm{BL}_{L_i}}(t)} & \frac{\partial g_{3_i}}{\partial \bar{v}_{\mathrm{IB}_i}(t)} \end{bmatrix} \tag{A19}$$

$$A_{ij} \mid i = \{1, \ldots, N_{\mathrm{PV}}\}, j = \{1, \ldots, N_{\mathrm{PV}}\}, i \neq j = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}_{3 \times 3} \tag{A20}$$

$$A_{i(N_{\mathrm{PV}}+1)} \mid i = \{1, \ldots, N_{\mathrm{PV}}\} = \begin{bmatrix} 0 \\ 0 \\ \frac{\partial g_{3_i}}{\partial \bar{v}_S(t)} \end{bmatrix}_{3\times 1} \tag{A21}$$

$$A_{(N_{\mathrm{PV}}+1)i} \mid i = \{1, \ldots, N_{\mathrm{PV}}\} = \begin{bmatrix} \frac{\partial g_4}{\partial \bar{v}_{\mathrm{SLC}_i}(t)} \\ 0 \\ 0 \end{bmatrix}_{3\times 1} \tag{A22}$$

$$A_{(N_{\mathrm{PV}}+1)(N_{\mathrm{PV}}+1)} = \begin{bmatrix} \frac{\partial g_4}{\partial \bar{v}_S(t)} & \frac{\partial g_4}{\partial \bar{i}_{L_S}(t)} & 0 \\ \frac{\partial g_5}{\partial \bar{v}_S(t)} & 0 & \frac{\partial g_5}{\partial \bar{d}_S(t)} \\ \frac{\partial g_6}{\partial \bar{v}_S(t)} & 0 & 0 \end{bmatrix} \tag{A23}$$

$$B = \begin{bmatrix} B_{11} & B_{12} & \cdots & B_{1N_{\mathrm{PV}}} & B_{1(N_{\mathrm{PV}}+1)} \\ B_{21} & B_{22} & \cdots & B_{2N_{\mathrm{PV}}} & B_{2(N_{\mathrm{PV}}+1)} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ B_{N_{\mathrm{PV}}1} & B_{N_{\mathrm{PV}}2} & \cdots & B_{N_{\mathrm{PV}}N_{\mathrm{PV}}} & B_{N_{\mathrm{PV}}(N_{\mathrm{PV}}+1)} \\ B_{(N_{\mathrm{PV}}+1)1} & B_{(N_{\mathrm{PV}}+1)2} & \cdots & B_{(N_{\mathrm{PV}}+1)N_{\mathrm{PV}}} & B_{(N_{\mathrm{PV}}+1)(N_{\mathrm{PV}}+1)} \end{bmatrix} \tag{A24}$$

While input matrix **B** is:

$$B_{ii} \mid i = \{1, \ldots, N_{\mathrm{PV}}\} = \begin{bmatrix} 0 & 0 \\ \frac{\partial g_{2_i}}{\partial \phi_i(t)} & \frac{\partial g_{2_i}}{\partial d_{\mathrm{BL}_i}(t)} \\ \frac{\partial g_{3_i}}{\partial \phi_i(t)} & \frac{\partial g_{3_i}}{\partial d_{\mathrm{BL}_i}(t)} \end{bmatrix}_{3\times 2} \tag{A24}$$

$$B_{ij} \mid i = \{1, \ldots, N_{\mathrm{PV}}\}, j \neq i = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}_{3\times 3} \tag{A25}$$

$$B_{i(N_{\mathrm{PV}}+1)} \mid i = \{1, \ldots, N_{\mathrm{PV}}\} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}_{3\times 1} \tag{A27}$$

$$B_{(N_{\mathrm{PV}}+1)(N_{\mathrm{PV}}+1)} = \left[\frac{\partial g_5}{\partial \bar{d}_S(t)}\right]_{1\times 1} \tag{A28}$$

Output matrix **C** is:

$$C = \begin{bmatrix} C_{11} & C_{12} & \cdots & C_{1N_{\mathrm{PV}}} & C_{1(N_{\mathrm{PV}}+1)} \\ C_{21} & C_{22} & \cdots & C_{2N_{\mathrm{PV}}} & C_{2(N_{\mathrm{PV}}+1)} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ C_{N_{\mathrm{PV}}1} & C_{N_{\mathrm{PV}}2} & \cdots & C_{N_{\mathrm{PV}}N_{\mathrm{PV}}} & C_{N_{\mathrm{PV}}(N_{\mathrm{PV}}+1)} \\ C_{(N_{\mathrm{PV}}+1)1} & C_{(N_{\mathrm{PV}}+1)2} & \cdots & C_{(N_{\mathrm{PV}}+1)N_{\mathrm{PV}}} & C_{(N_{\mathrm{PV}}+1)(N_{\mathrm{PV}}+1)} \end{bmatrix} \tag{A29}$$

A

$$C_{ii} \mid i = \{1, \ldots, N_{\mathrm{PV}}\} = \begin{bmatrix} 1 & 0 \end{bmatrix}_{1\times 2} \tag{A31}$$

$$C_{i(N_{\mathrm{PV}}+1)} \mid i = \{1, \ldots, N_{\mathrm{PV}}\} = \begin{bmatrix} 0 \end{bmatrix}_{1\times 1} \tag{A32}$$

$$C_{ij} \mid i = \{1, \ldots, N_{\mathrm{PV}}\}, j \neq i = \begin{bmatrix} 0 & 0 & 0 \end{bmatrix}_{1\times 3} \tag{A33}$$

$$C_{(N_{\mathrm{PV}}+1)i} \mid i = \{1, \ldots, N_{\mathrm{PV}}\} = \begin{bmatrix} 0 & 0 & 0 \end{bmatrix}_{1\times 3} \tag{A35}$$

And feedthrough matrix **D** is zero.

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LIST OF PUBLICATIONS

1. A. Nazer, P. Manganiello, and O. Isabella. “A virtual bus parallel differential power processing configuration for photovoltaic applications”. In: Mathematics and Computers in Simulation 224, Part B (2024), pp. 49–62. issn: 0378-4754.

2. A. Nazer, O. Isabella, and P. Manganiello. “PV to Virtual Bus Parallel Differential Power Processing Architecture for Photovoltaic Systems”. In: IEEE Transactions on Industrial Electronics (2024), pp. 1–11.

3. A. Nazer, O. Isabella, and P. Manganiello. “Dynamic Analysis of Photovoltaic to Virtual Bus Parallel Differential Power Processing Architecture”. In: IEEE Transactions on Industrial Electronics (2025), pp. 1–12.

4. A. Nazer, O. Isabella, and P. Manganiello. “A Comprehensive Classification of State-of-the-Art Distributed Maximum Power Point Tracking Architectures for Photovoltaic Systems”. In: IEEE Open Journal of the Industrial Electronics Society, "**Under Review**" (2025).

5. A. Nazer, O. Isabella, H. Vahedi, and P. Manganiello. “Integration of Battery into Photovoltaic to Virtual Bus Parallel Differential Power Processing Architecture”. In: IEEE Transactions on Industrial Electronics, "**Under Review**" (2025).

6. A. Nazer, O. Isabella, H. Vahedi, and P. Manganiello. “Photovoltaic to Virtual Bus Series-Parallel Differential Power Processing for Photovoltaic systems”. In: IEEE Open Journal of the Industrial Electronics Society, "**Under Review**" (2025).

7. A. Nazer, P. Manganiello, and O. Isabella “Hierarchical PV to PV Series Differential Power Processing for Photovoltaic Applications: Power Flow and Converter Rating Analysis”. In: Mathematics and Computers in Simulation, (2025).

CURRICULUM VITæ

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Afshin Nazer earned his bachelor's degree in Electrical Engineering from Ferdowsi University of Mashhad in 2016. Subsequently, in 2018, he completed his master's degree in Power Electronics and Electric Machines Engineering at the University of Tehran, Tehran, Iran. Then, for more than two years, he served as a research assistant at the University of Tehran, concentrating on the analysis, design, and control of power converters for solar array simulator applications. His research primarily focused on analyzing, designing, modeling, and controlling switching converters for photovoltaic (PV) systems to mitigate mismatch-related losses among PV elements. In 2021, he joined the Photovoltaic Materials and Devices (PVMD) group at Delft University of Technology, Delft, the Netherlands. His work there involved the analysis, design, modeling, and control of switching converters for PV systems, with an emphasis on reducing mismatch losses among PV elements to enhance overall system efficiency.

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