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Publication date
2019

Document Version
Final published version

Published in
2019 13th European Conference on Antennas and Propagation (EuCAP)

Heat Transfer Enhancement in Passively Cooled 5G Base Station Antennas Using Thick Ground Planes

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***Abstract*—The thermal and electromagnetic effects of varying the ground plane thickness and aperture size of the 5G integrated base station antennas are investigated. A double-sided PCB structure is designed with antennas and digital beamforming chips on the opposite sides. Fully-passive cooling is achieved by using fanless CPU coolers attached to the chips. The simulation results indicate that as compared to the standard counterparts, much better cooling performance can be achieved using relatively thick ground planes with extended aperture sizes, with no significant effect on the electromagnetic properties.**

***Index Terms*—active integrated antenna, base station antenna, fifth generation (5G), millimeter-wave communication, passive cooling, thick ground plane.**

I. Introduction

The fifth generation (5G) base station antenna arrays are expected to handle multiple data streams and serve multiple mobile users simultaneously using the same frequency band. Generation of multiple flexible beams towards the users with sufficiently low cross-beam interference requires fully-digital beamforming. Active electronically scanned arrays (AESA's) with digital beamforming have been widely used in such applications as military radar [1], satellite communications [2], radio astronomy [3] and are very likely to be used in the future 5G communication systems [4].

In fully-digital beamforming, each antenna element has its own transceiver and data converters that are integrated into the beamforming chips. In this case, high integration density and increased complexity of the front-end circuitry lead to increased heat dissipation, and thus more complicated thermal management strategies. Besides, being high-volume markets, 5G antenna arrays require low-cost passive cooling methods

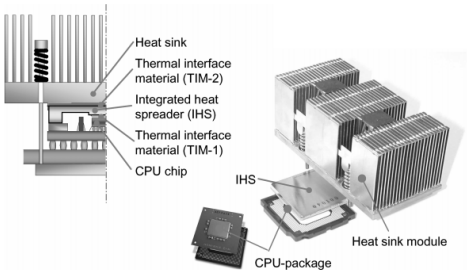


Fig. 1. CPU processor package of Fujitsu Primepower2500 (taken from [6])

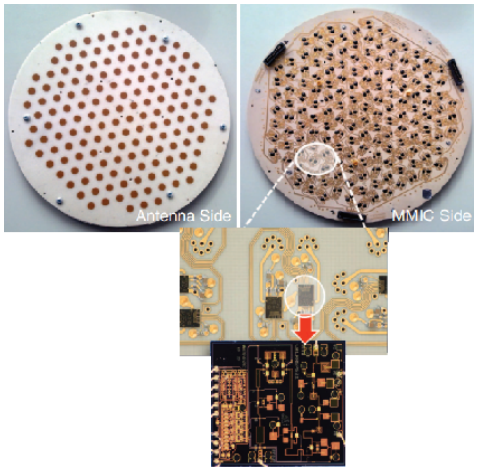


Fig. 2. A double-sided antenna PCB with a core chip, from the New Automotive Tracking Antenna for Low-Cost Innovative Applications (NATALIA) project (taken from [8])

that do not work with electricity. These methods include the use of heat sinks that are in contact with air, heat pipes and heat spreaders. Despite being less effective than the active counterparts (fans or liquid pumps), such passive cooling techniques are more energy-efficient, reliable and cheaper [5].

Considering their advantages, fanless CPU coolers (an example is given in Fig. 1) have recently been proposed for array cooling in low-cost and low-profile planar 5G AESA's [7] for which the antennas and chips are located at opposite sides of the board (see Fig. 2 for an example). Furthermore, following the work on heat source layout optimization [9], sparse antenna (or chip) array topologies have been investigated for cooling extension in 5G antennas [7], [10], [11]. It was seen that fanless CPU coolers are able to remove most of the heat from the chips, while topology optimization can provide additional cooling by increasing the surface area around each antenna element. However, the work in [7] has focused on thin (35 um copper) ground planes, which mimics scenarios where each source creates a hot-spot at the corresponding chip position. In fact, a thick ground plane can be used to aid in heat transfer by increasing the thermal conductivity of the substrate and spreading the hot-spots [12], [13].

In this paper, the aim is to investigate the extent of cooling

enhancement in passively cooled (by a fanless CPU cooler) planar AESA's with increased ground plane thickness. The effect of aperture size on the maximum temperature of the array is also investigated. Section II presents the electromagnetic and thermal model of the chip-integrated antenna array. Section III provides and discusses the simulation results. Section IV concludes the paper.

II. EM and Thermal Model

For the electromagnetic (EM) model, Rogers RT5880 is used as the substrate material. Copper is used for the feeding pin, feed line and ground plane. A 50 Ω feeding microstrip line is designed on the chip substrate. The patch is excited by a feeding pin by vertically connecting the patch to the feeding line, as in [14]. Although it may present manufacturing reliability problems, designing a pin-fed patch is easier compared to a non-contact transition in the case of having thick ground planes [15]. The decreasing active input resistance and increasing reactance of pin-fed elements (see Fig. 9) can easily be compensated by adjusting the patch dimensions (smaller width and larger length, see Fig. 10). For aperture coupling, on the other hand, the coupling decays with ground plane thickness, while increasing the slot length to compensate the decay may lead to high back lobes. An aluminum heat sink plate is also placed at the back of the array, representing the CPU cooler. The EM model for a unit cell is given in Fig. 3.

The thermal model used in the paper is the two-resistor model whose guidelines are reported in [16]. The chips are modeled as aluminum blocks with insulated sides. Heating power (P_h) is applied to the chip. Heat transfer coefficients (H.T.C's) for the naturally cooled substrate-to-air surfaces (h_{air}) and for the heat sink (h_{hs}) (CPU cooler) at the chip case are defined. Thermal resistances for junction-to-case node and junction-to-board node are also defined to be used in the conduction-based thermal solver CST MPS. Copper heat spreader pins are used to connect the patch and chip to the ground plane. The thermal model for a unit cell structure is given in Fig. 4.

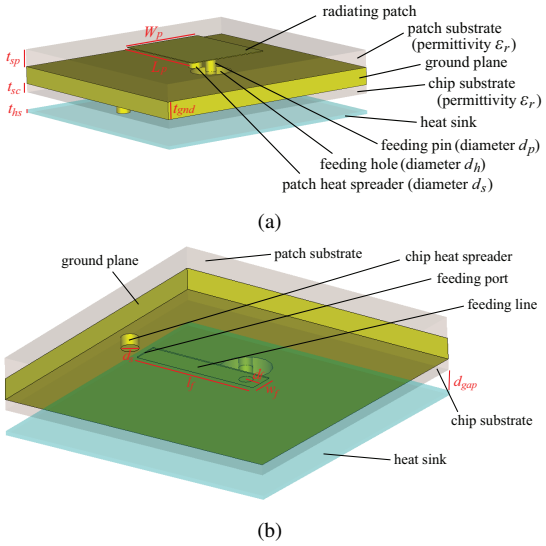


Fig. 3. EM design parameters in a unit cell, (a) top view, (b) bottom view.

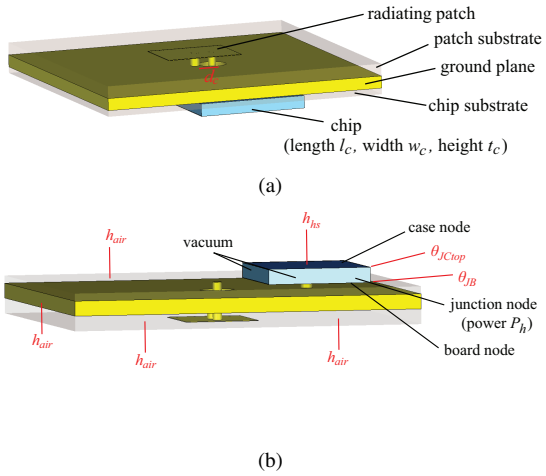


Fig. 4. Thermal design parameters in a unit cell, (a) top view, (b) bottom view.

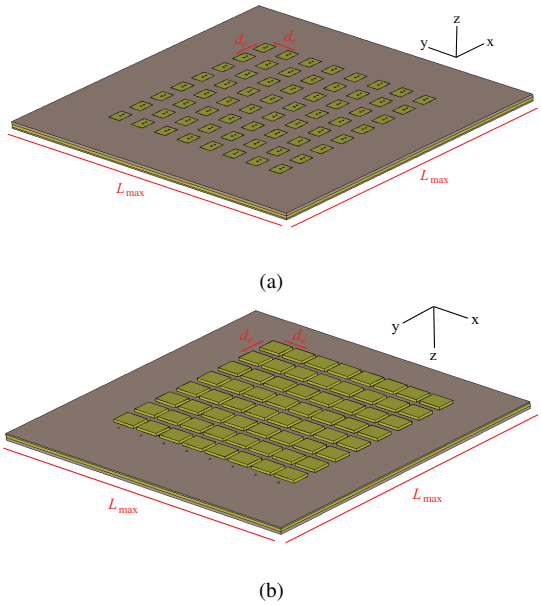


Fig. 5. 8x8 integrated antenna array model, (a) patch side, (b) chip side.

The designed 8x8 integrated antenna array (formed by the unit cells) is shown in Fig. 5. A list of all the EM and thermal design parameters (based on the values in [7]) is provided in Table I.

III. Array Simulation Results

In this part, EM and thermal simulation results are given in two separate sections.

A. Thermal Simulation Results

First, t_{gnd} is varied between 0.05 mm and 2 mm by taking $L_{\max} = 5\lambda_0$. The maximum temperature in the 8x8 array ($T_{\max}$) (maximum junction temperature) is plotted in Fig. 6. It

TABLE I
LIST OF DESIGN PARAMETERS USED IN CST MWS & MPS

Parameter definition	Symbol	Value
Center frequency	f_0	28.5 GHz
Relative permittivity of the substrates	ϵ_r	2.2
Patch width	W_p	2.50 mm
Patch length	L_p	3.20 mm
Feed line width	w_f	0.6 mm
Feed line length	l_f	3.1 mm
Chip block width	w_c	3.5 mm
Chip block length	l_c	4.5 mm
Patch substrate thickness	t_{sp}	0.508 mm
Chip substrate thickness	t_{sc}	0.254 mm
Heat sink plate thickness	t_{hs}	0.5 mm
Chip block height	t_c	0.5 mm
Ground plane thickness	t_{gnd}	0.05 mm to 2 mm
Feeding pin diameter	d_p	0.32 mm
Feeding hole diameter	d_h	1.2 mm
Heat spreader diameter	d_s	0.4 mm
Feeding pin offset	d_f	0.4 mm
Chip offset relative to the patch	d_c	0.75 mm
Inter-element spacing	d_e	$0.5\lambda_0$
Heat sink plate offset	d_{gap}	0.5 mm
Dissipated power per chip	P_h	2 W
H.T.C of the heat sink	h_{hs}	1000 W/m^{2}K
H.T.C of air	h_{air}	10 W/m^{2}K
Junction-to-case thermal resistance	θ_{JCtop}	10 W/mK
Junction-to-board thermal resistance	θ_{JB}	15 W/mK
Maximum aperture edge length	$L_{\max}$	$5\lambda_0$ to $20\lambda_0$
Ambient temperature	T_{amb}	25^{o}C

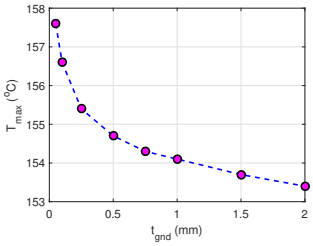


Fig. 6. $T_{\max}$ for varying t_{gnd} when $L_{\max}$ = $5\lambda_0$.

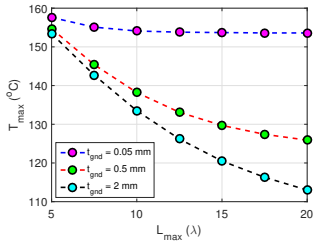


Fig. 7. $T_{\max}$ at several t_{gnd} values for varying $L_{\max}$.

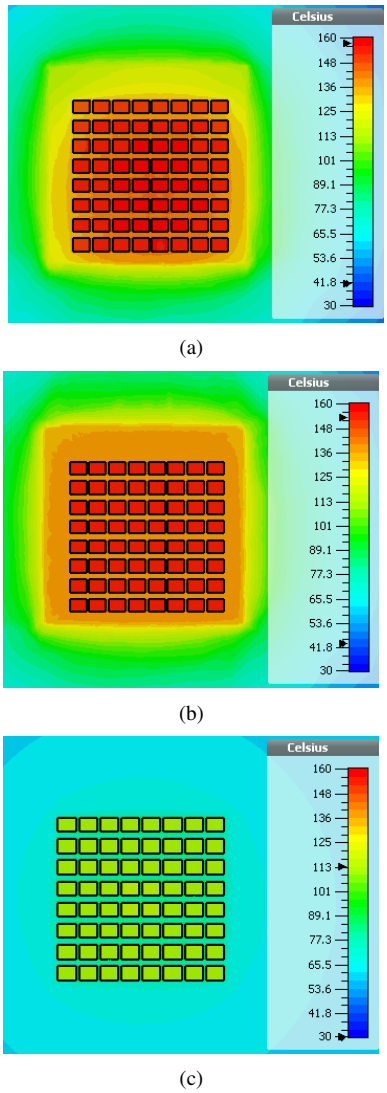
TABLE II
EFFECTIVE SUBSTRATE THERMAL CONDUCTIVITIES (k_t) IN LATERAL (x, y) AND VERTICAL (z) DIRECTIONS WITH VARYING t_{gnd}

t_{gnd} (mm)	k_{tx} (W/mK)	k_{ty} (W/mK)	k_{tz} (W/mK)
0.05	24.88	24.88	0.21
0.1	46.70	46.70	0.23
0.25	99.21	99.21	0.27
0.5	159.00	159.00	0.33
0.75	199.01	199.01	0.40
1	227.67	227.67	0.46
1.5	265.98	265.98	0.59
2	290.42	290.42	0.72

is seen that $T_{\max}$ decreases by about 4^{o}C when t_{gnd} increases from 0.05 mm to 2 mm.

Next, $L_{\max}$ is varied between $5\lambda_0$ and $20\lambda_0$ and $T_{\max}$ is plotted in Fig. 7 for several t_{gnd} values. It is seen that for the thinnest ground plane (t_{gnd} = 0.05 mm), increasing $L_{\max}$ does not help decrease $T_{\max}$ since heat gets trapped around the chip and creates a hot-spot. On the other hand, for thicker ground planes, the heat generated at the chip can be spread to the sides of the array, which is then removed from the array surface. Since surface area increases with $L_{\max}$, the best cooling performance is achieved when t_{gnd} = 2 mm and $L_{\max}$ = $20\lambda_0$. The increase in lateral (k_{tx}, k_{ty}) and vertical (k_{tz}) effective thermal conductivities with t_{gnd} is given in Table II. The values are obtained using the formulas given in [17]. Note that the conductivities will be slightly larger in the model compared to the theoretical values due to the heat spreader vias.

Sample temperature distributions for t_{gnd} = 0.05 mm & $L_{\max}$ = $5\lambda_0$, t_{gnd} = 2 mm & $L_{\max}$ = $5\lambda_0$ and t_{gnd} = 2 mm & $L_{\max}$ = $20\lambda_0$ are shown in Fig. 8(a), Fig. 8(b) and Fig.



(a)

(b)

(c)

Fig. 8. Sample temperature distributions with passive CPU cooling for the 8x8 regular square array along the horizontal cut in the middle of the conducting blocks representing the junctions, (a) t_{gnd} = 0.05 mm & $L_{\max}$ = $5\lambda_0$, (b) t_{gnd} = 2 mm & $L_{\max}$ = $5\lambda_0$, (c) t_{gnd} = 2 mm & $L_{\max}$ = $20\lambda_0$.

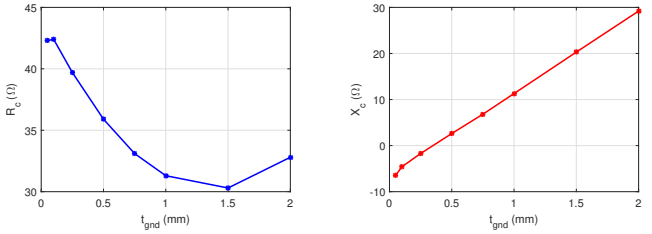
8(c), respectively. It can be seen that in Fig. 8(b), the heat is more spread along the aperture which decreases $T_{\max}$ about 4^oC compared to Fig. 8(a). In Fig. 8(c), $T_{\max}$ becomes about 45^oC less since the aperture size is much larger, where the heat can be naturally removed.

B. EM Simulation Results

In Section III-A, it is observed that increasing t_{gnd} and $L_{\max}$ helps in cooling. In this section, first, the EM performances of the two arrays with t_{gnd} = 0.05 mm & $L_{\max}$ = $5\lambda_0$ and t_{gnd} = 2 mm & $L_{\max}$ = $20\lambda_0$ are compared in terms of active S-parameters to see if it is possible to achieve antenna matching with the design parameters given in Table I. The results are given in Fig. 10.

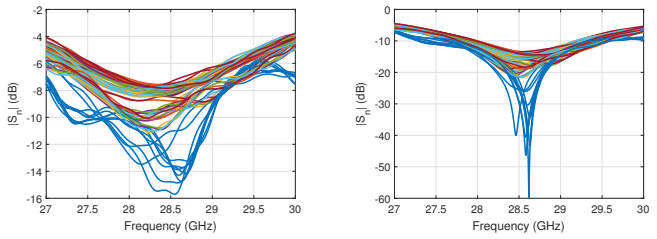
From Fig. 10, it can be inferred that due to the change in mutual coupling, the matching of the array becomes much worse when the thick ground plane is used. This effect can be compensated by changing the dimensions of the patch. Modifying the patch dimensions to L_p = 3.26 mm, W_p = 1.80 mm allows us to achieve good matching with no significant impact on the cooling performance (see Table III).

Next, the full EM performance of the designed 8x8 arrays with the worst and the best cooling performance are given in terms of the active reflection coefficients, total efficiency, mutual couplings for a center element and radiation pattern. The broadside beam and scanned (towards θ_s = -π/9, ϕ_s = π/4) beam results of the array with the lowest t_{gnd} and $L_{\max}$



(a) (b)

Fig. 9. Active impedance of a center element at f_0 with varying t_{gnd} for $L_{\max}$ = $5\lambda_0$, L_p = 3.20 mm, W_p = 2.50 mm, (a) resistance, (b) reactance.

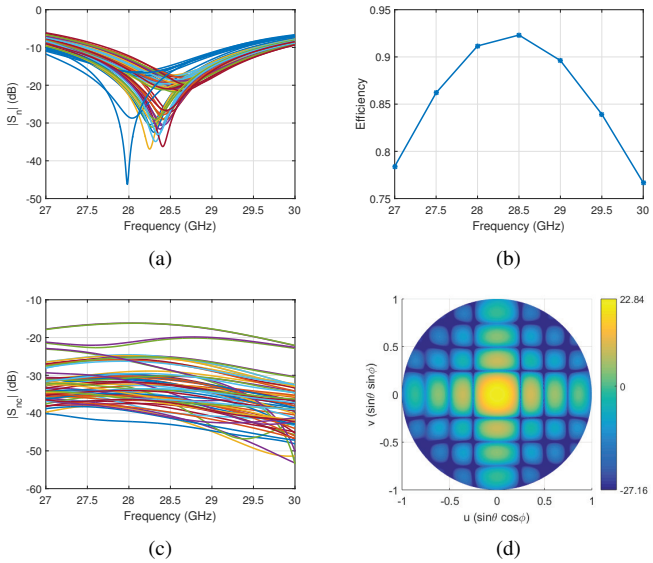


(a) (b)

Fig. 10. Active S-parameters with t_{gnd} = 2 mm & $L_{\max}$ = $20\lambda_0$, (a) L_p = 3.20 mm, W_p = 2.50 mm, (b) L_p = 3.26 mm, W_p = 1.80 mm.

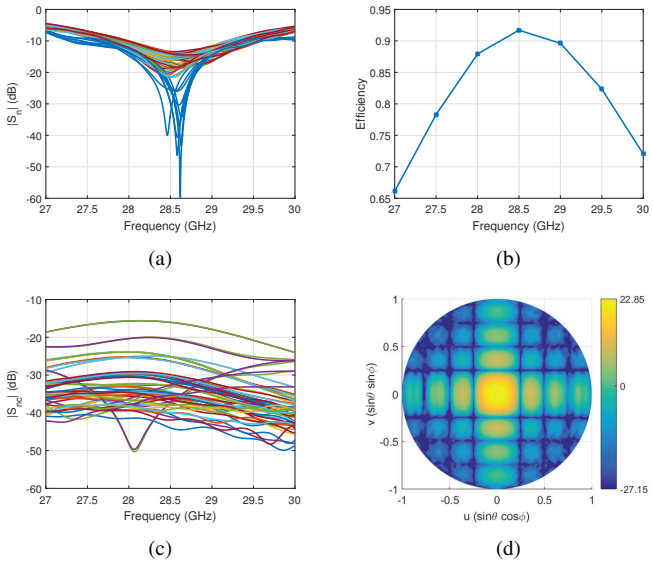
TABLE III
PATCH DIMENSION EFFECT ON $T_{\max}$ WITH t_{gnd} = 2 MM FOR VARYING $L_{\max}$

$L_{\max}$ (λ_0)	$T_{\max}$ (^{o}C) (L_p = 3.20 mm, W_p = 2.50 mm)	$T_{\max}$ (^{o}C) (L_p = 3.26 mm, W_p = 1.80 mm)
5	153.4	153.7
7.5	142.7	142.9
10	133.5	133.6
12.5	126.2	126.2
15	120.5	120.6
17.5	116.3	116.4
20	113.0	113.0



(a) (b) (c) (d)

Fig. 11. EM performance results for the 8x8 broadside array with t_{gnd} = 0.05 mm & $L_{\max}$ = $5\lambda_0$, L_p = 3.20 mm, W_p = 2.50 mm, (a) active S-parameters, (b) total efficiency, (c) mutual couplings of a center element, (d) realized gain.



(a) (b) (c) (d)

Fig. 12. EM performance results for the 8x8 broadside beam array with t_{gnd} = 2 mm & $L_{\max}$ = $20\lambda_0$, L_p = 3.26 mm, W_p = 1.80 mm, (a) active S-parameters, (b) total efficiency, (c) mutual couplings of a center element, (d) realized gain.

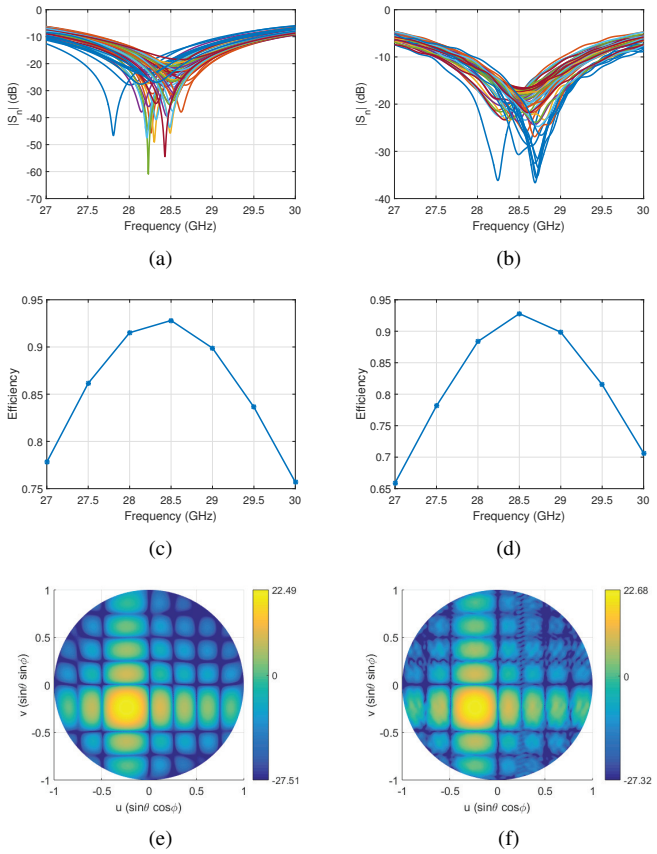


Fig. 13. EM performance results for the 8x8 scanned beam (θ_s = -π/9, ϕ_s = π/4) array with t_{gnd} = 0.05 mm & $L_{\max}$ = 5λ_0, L_p = 3.20 mm, W_p = 2.50 mm, (a) active S-parameters, (c) total efficiency, (e) realized gain; and with t_{gnd} = 2 mm & $L_{\max}$ = 20λ_0, L_p = 3.26 mm, W_p = 1.80 mm, (b) active S-parameters, (d) total efficiency, (f) realized gain.

(thus the worst thermal performance) are given in Fig. 11 and Fig. 13, respectively. Fig. 12 and Fig. 13 present the EM performance of the array with the largest t_{gnd} and $L_{\max}$ (thus the best thermal performance) for the broadside and scanned (towards θ_s = -π/9, ϕ_s = π/4) beam, respectively.

Overall, it can be seen that similar EM performance can be achieved with the proposed thick ground plane and extended aperture size antenna as compared to the thin ground plane, standard aperture size counterpart. The advantage of increasing t_{gnd} and $L_{\max}$ appears in the cooling performance due to increased effective thermal conductivity of the substrate and substrate-to-air surface area.

IV. Conclusion

An active integrated, passively cooled patch antenna array with a thick ground plane and an extended aperture size has been proposed for 5G base stations with fully-digital beamforming capabilities.

A double sided PCB has been designed with patch antennas on one side and transceiver chips on the other side. For the EM simulations, a microstrip feeding line with a vertical pin transition to the patch has been realized. The thermal simulations have been performed following the two-resistor model and assuming that there is a fanless CPU cooler sinking the heat from the chips.

An 8x8 array of patches and chips has been simulated using an electromagnetic and a thermal solver. From the thermal aspect, it has been found out that increasing the ground plane thickness leads to an increase in the effective thermal conductivity of the substrate, which helps to spread the hot-spots that are formed in the vicinity of the chip to a larger aperture area. Besides, increasing this aperture size contributes to the cooling since the surface area that is in contact with air gets larger.

Acknowledgment

This research was conducted as part of the NWO-NXP Partnership Program on Advanced 5G Solutions within the project titled “Antenna Topologies and Front-end Configurations for Multiple Beam Generation”. More information: www.nwo.nl.

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