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Integrated Cryo-CMOS Temperature Sensors for Quantum Control ICs

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***Abstract*—This work presents an experimental study of different components (resistors, diodes, transistors) in a standard 40-nm bulk CMOS process for their suitability as integrated cryogenic temperature sensors down to a temperature of 4.2 K. It was found that most devices can be employed as sensors down to temperatures of approximately 50 K, below which non-ideal effects such as non-linear behaviour and decreased sensitivity start to dominate. The Dynamic-Threshold MOS (DTMOS) was found to be a very promising candidate for its linearity, low forward-voltage-drop and sensitivity down to 8 K. Moreover, as previous research indicated that cryogenic self-heating raises the local chip temperature to tens of Kelvins already at moderate power levels, the aforementioned sensing limitations at very low temperatures are expected to be of less importance in realistic applications. The results presented in this work contribute to the further integration of classical cryo-CMOS control electronics and qubits, towards a fully scalable quantum computer.**

I. Introduction

Quantum computation holds the promise of enormous computing power, enabling certain computations that are unsolvable by even the largest super-computers of today. To reach such performance, this new computing paradigm exploits quantum effects in quantum bits (qubits), which need to be cooled to deep-cryogenic temperatures for proper operation and therefore reside in dilution refrigerators.

Although information is processed in the quantum world, classical electronics are still required for the control and readout of the qubit states. The number of qubits in state-of-the-art quantum computers is still limited, allowing even an individual cable for each qubit to carry signals to and from the room-temperature equipment. However, orders of magnitude more qubits are required for any useful computation, making this scheme impractical from a wiring point of view. To overcome this scaling problem, a cryogenic controller has been proposed that brings the functionality of the room-temperature equipment into the dilution refrigerator, close to the qubits [1].

Dilution refrigerators have little cooling power at deep-cryogenic temperatures (e.g., 14 µW at 20 mK in a Bluefors XLD), so severe power constraints are posed upon the cryogenic controller, for it not to destroy the qubit states by raising their temperature. To ensure operation within a safe thermal envelope, schemes such as clock throttling and dynamically enabling/disabling of circuit blocks can be employed. However, those techniques would require an accurate monitoring of the die temperature, thus asking for integrated temperature sensors operating at cryogenic temperatures. In typical room-temperature applications, those sensors are based on BJTs, which do not properly operate at cryogenic temperatures [2].

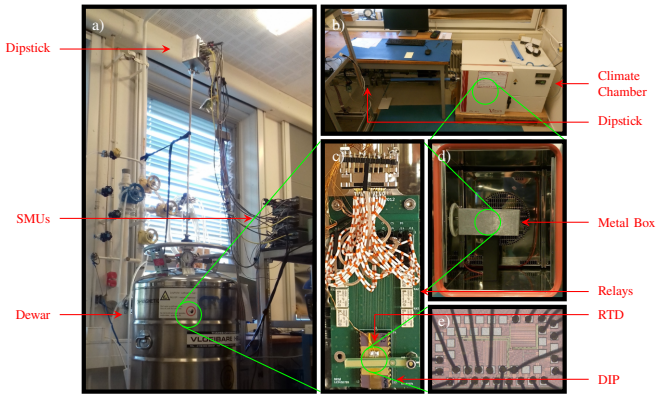

Fig. 1. Measurement setup: a) dipstick in LHe dewar; b) dipstick in climate chamber; c) PCB at the end of the dipstick; d) climate chamber internal view; e) die micrograph

Alternatively, resistors and transistors can be employed [3], but no extensive cryogenic characterization for such devices is available.

This work, therefore, presents the experimental characterization of standard CMOS components, to discuss their suitability and performance as potential cryogenic temperature sensors.

II. Test Structures and Measurement Setup

All characterized devices were fabricated in a 1.1 V, 40-nm bulk CMOS process. The data presented in this work originated from dedicated test structures present on different test chips, which were designed with cryogenic characterization in mind. Techniques such as Kelvin connections for mitigation of parasitic resistances and signal guarding to allow measurement of extreme low currents were employed.

A dipstick and dewar containing liquid Helium were used to characterize the structures at cryogenic temperatures, while a climate chamber enabled measurements up to 80 °C.

The measurement setup is depicted in Fig. 1. The temperature of the test chip was monitored by a Cernox temperature sensor clamped to the ceramic DIP chip carrier. Relays (Omron G6K-series) enabled the electrical isolation and selection of different test structures while being at cryogenic temperatures, both of which can be seen in Fig. 1a. A micrograph indicating one of the bonded test chips is shown in Fig. 1e, which was also used in [4].

Keithley Source Measurement Units (SMU) were tasked for the electrical characterization and temperature sensor read-

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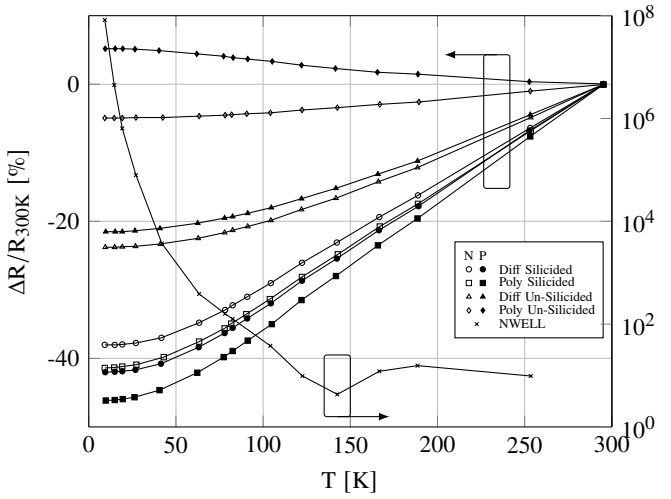

Fig. 2. Change in resistance relative to T = 300 K for different types of resistors.

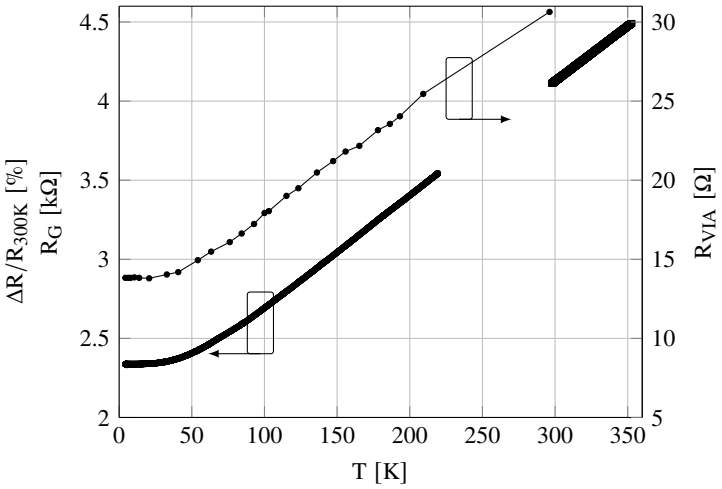

Fig. 3. Measured resistance of a M1-M2 VIA and of a W/L=10μm/40nm MOSFET gate.

out. An in-depth description of the diode and MOSFET gate test structures can be found in [4]. More background on the MOSFET structures is available in [5], [6]. The remainder of structures is described in Section III.

III. Experimental Results and Discussion

The temperature sensing capability and performance of the measured structures is presented and discussed in this section.

Resistors. Three different resistor types were characterized, both with and without silicide, as shown in Fig. 2. The resistors were placed in arrays as per the MOSFETs in [5].

Diffused and poly resistors show highly linear PTC behaviour down to 70 K, below which their temperature sensitivity starts to decrease for all devices. Silicided devices exhibit the highest sensitivity (0.17 %/K) above this temperature, followed by unsilicided diffused (0.095 %/K) and poly devices (0.021 %/K). The resistivity saturation at deep-cryogenic temperatures can be ascribed to impurity-limited electron mean-free path lengths, and is compatible with metallic behaviour [7]. The complementary behaviour of the P-poly device is most likely due to grain-boundary effects dominating in these low-doped devices [8].

The NWELL resistance shows highly non-linear response due to freeze-out, also reported in [9], and therefore has limited use for temperature sensing applications.

MOSFET Gate. The measured N-MOSFET gate resistance as a function of temperature is plotted in Fig. 3. A description of the structure and its measurement can be found in [4]. The gate resistance has a response in line with the resistors presented in Fig. 2 (including a resistance saturation below 50 K), with a sensitivity of 0.17 %/K.

One particularly interesting application of this structure is the direct measurement of the MOSFET channel temperature, also known as gate thermometry [4].

VIA. The temperature dependence of a single M1-M2 VIA is plotted in Fig. 3. As expected, the VIA exhibits similar behaviour compared to the other resistive devices shown, with a temperature sensitivity of 0.21 %/K. Although VIAs allow very local temperature sensing due to their size, the VIA resistance is relatively low and was found to be susceptible to reliability issues between thermal cycles, complicating their use as sensors.

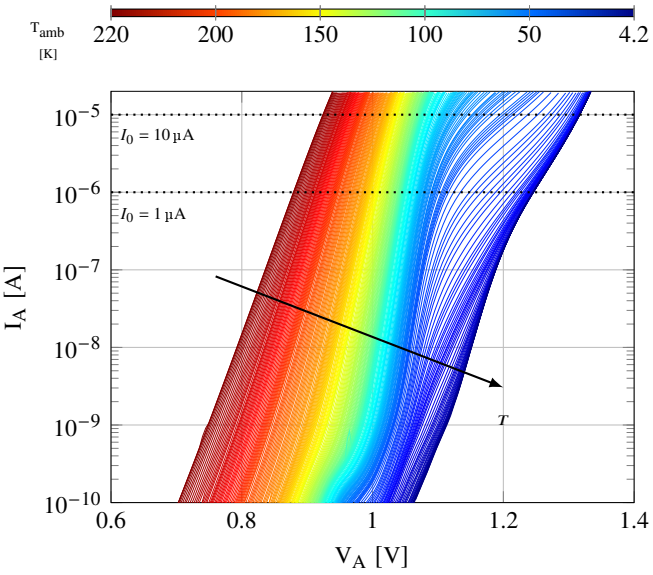

Fig. 4. I-V characteristics of a typical P+/NWELL diode as a function of temperature. Constant-current operation indicated by the dotted lines.

Diodes. As diodes form the basis of semiconductors, their deployment as temperature sensing device is very attractive.

The I-V characteristics of a typical P+/NWELL diode at different cryogenic temperatures are plotted in Fig. 5. This device has been described in more detail in [4].

These diodes maintain exponential behaviour down to 150 K, below which the curves start to deviate, especially in the high current regime. Below 70 K, carrier freeze-out increases the series resistance of the diode, thereby significantly increasing the voltage drop and temperature sensitivity in this temperature

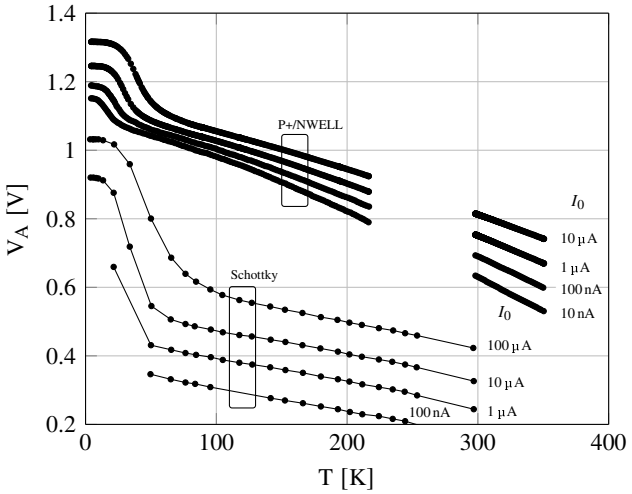

Fig. 5. Diode voltage V_A as function of temperature and excitation current I_0 for a P+/NWELL and experimental Schottky diode.

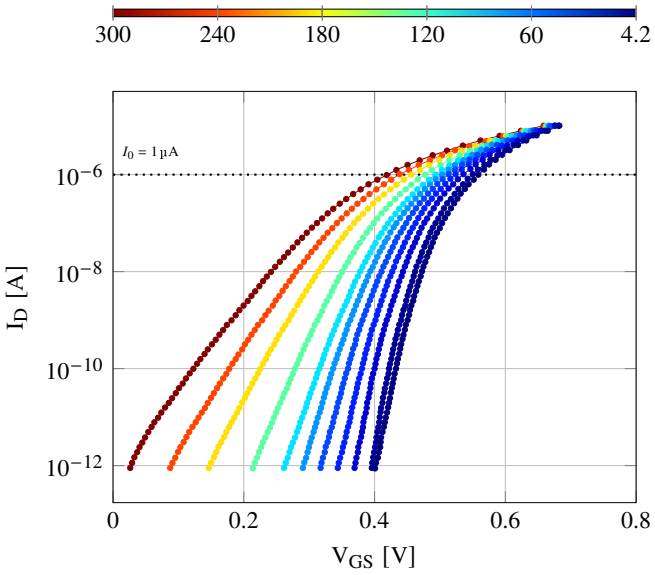

Fig. 6. I-V curves of a diode-connected DTMOS device as a function of temperature. Constant-current operation indicated by the dotted line.

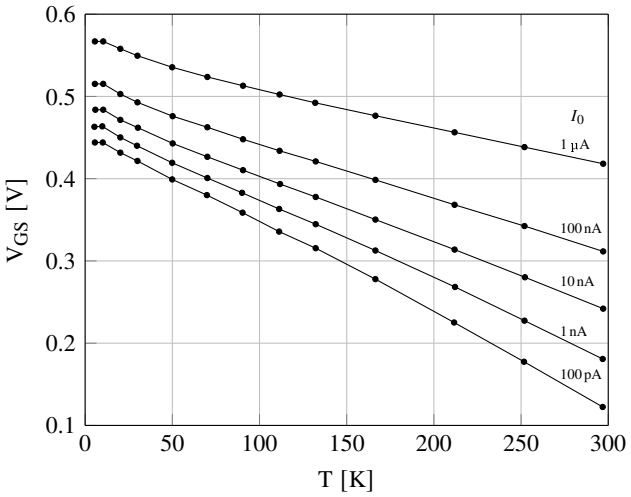

Fig. 7. Voltage developed across the diode-connected DTMOS biased at different constant currents I_0 as a function of temperature.

regime [10]. However, at deep-cryogenic temperatures below 10 K, the curves start to compress and show little temperature dependence.

Diodes are often biased with a constant current I_0 when used as temperature sensors, as indicated in Fig. 4 by the dotted lines. The voltage developed across the diode V_A is then a measure of the diode temperature.

V_A as a function of temperature for different values of I_0 has been plotted in Fig. 5 for two types of devices.

The P+/NWELL diode has a linear response down to approximately 60 K with a sensitivity ranging between 1.25 and 1.8 mV/K, both depending on I_0. By tuning I_0, both the saturated V_A and linear region can be pushed to lower temperatures at the expense of worse noise performance. One drawback of these devices is the high V_A in the deep-cryogenic regime, exceeding the 1.1 V supply rail.

Although not available in the adopted process, an experimental Schottky diode was taped-out by removing an implant layer, creating a local Schottky contact. The measured response of this device can be found in Fig. 5. The behaviour is similar to its P+/NWELL counterpart, with a highly linear region down to 100 K and a sensitivity of 0.9 mV/K. However, as expected from Schottky devices, their V_A lies significantly lower compared to the other diode. V_A keeps within the supply rail over the full temperature range, simplifying design of the read-out circuit.

DTMOS. Connecting the gate and bulk contacts of a MOSFET together, forms a Dynamic-Threshold MOSFET (DTMOS), which finds its use in low-power applications [11]. The I-V curves of a diode-connected (bulk and gate connected to drain) DTMOS measured at different temperatures can be found in Fig. 6.

Compared to the curves in Fig. 4, two advantages over the traditional P+/NWELL diode are apparent: the DTMOS maintains exponential behaviour down to deep-cryogenic temperatures and the voltage drop V_{GS} is significantly lower, as also reported in [2].

Following the same constant-current bias scheme as employed before, the temperature response of V_{GS} is found as shown in Fig. 7. Indeed, the advantages of this device are also visible in this plot, as V_{GS} lies below 600 mV over the full temperature range, while maintaining high linearity and sensitivity (0.9 mV/K) down to approximately 8 K.

MOSFETs. The low-temperature operation of MOSFETs has gained a lot of coverage due to the recent developments in quantum computation, and its operation has been widely reported on.

Due to its versatile operation, this work limits itself to the discussion of the extracted temperature dependence of the main device parameters, as shown in Fig. 8. It can be recognized that all these parameters exhibit a saturating behaviour at deep-cryogenic temperatures. It can be stated that the MOSFET DC-behaviour, to a first order, is temperature insensitive below approximately 40 K.

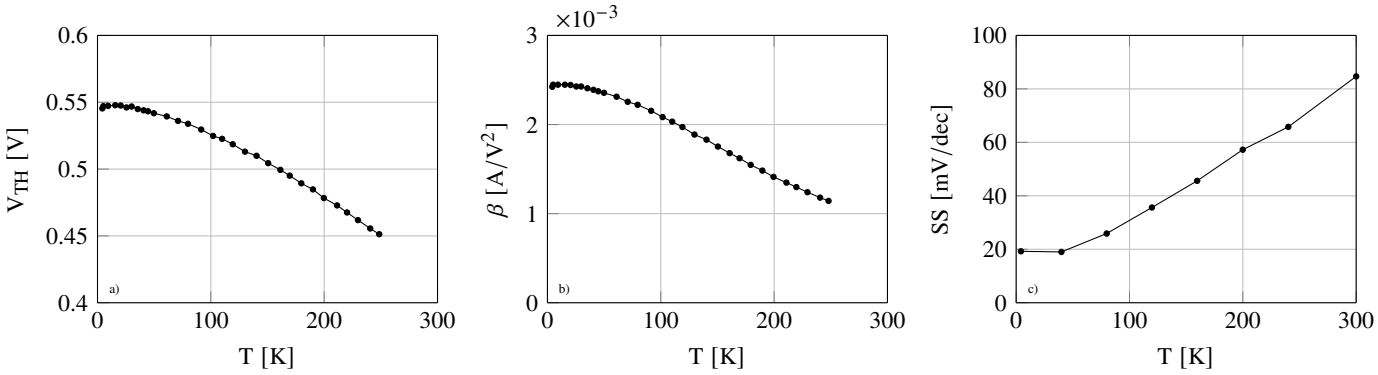

Fig. 8. Behaviour of 3 main device parameters of a W/L = 1.2μ/400n NMOS as function of temperature: a) threshold voltage; b) current factor and c) subthreshold slope.

Apart from the static operation of the other devices discussed in this work, the MOSFETs allows temperature sensing through dynamic schemes, such as ring oscillators, which convert temperature directly into frequency.

Apart from the above-mentioned properties, integrated cryo-sensors should have extreme-low power operation and a high level of integration. Although all sensors presented have a decreased sensitivity at deep-cryogenic temperatures, cryogenic self-heating was reported to raise the chip temperature significantly [4], [12]. This alleviates this sensor limitation by increasing the lowest temperature to be sensed.

In order to take full advantage of these components, a variability study and analysis of different read-out architectures should be performed, which lie beyond the scope of this work.

A table summarizing the most important sensor parameters can be found in Table I.

TABLE I
OVERVIEW OF DIFFERENT COMPONENTS.

Type	T^a_{min} [K]	S_T	V^b_{max} [V]
Resistor Sil/Un-Sil	50/50	0.17/0.095 %/K	-
Gate	50	0.17 %/K	-
VIA	40	0.21 %/K	-
P+/NWELL	12	1.8 mV/K	1.31
Schottky	15	0.9 mV/K	1.03
DTMOS	8	0.9 mV/K	0.56

[a] Temperature at which S_T falls below 90 %.

[b] Maximum voltage drop over full temperature range.

IV. Conclusion

Different standard 40-nm bulk CMOS components were characterized over a wide temperature range to assess their potential use as integrated cryogenic temperature sensors for cryogenic quantum processor controllers.

It was shown that most devices can be employed down to a temperature of approximately 50 K, below which sensitivity and/or linearity starts to severely deteriorate.

In particular, it was shown that the use of DTMOS has a lot of potential by virtue of its high linearity, usability down to 8 K and low voltage drop, enabling the use of low-power read-out circuits.

Moreover, cryogenic self-heating was reported to raise the local chip temperature by tens of Kelvins, already at very low power dissipation. This mitigates the lowest required operational temperature for the sensors, thus allowing the use of the sensors characterized in this work.

The experimental study presented here forms the basis for the next step in realizing integrated temperature sensors for scalable quantum computing exploiting cryo-CMOS as platform for the electronic controller. However, also beyond quantum applications, these data can be used for the design of cryogenically compatible smart-sensor-systems, suitable for both terrestrial and extra-terrestrial applications.

References

[1] F. Sebastiano, H. Homulle, B. Patra, R. Incandela, J. van Dijk, L. Song, M. Babaie, A. Vladimirescu, and E. Charbon, "Cryo-CMOS Electronic Control for Scalable Quantum Computing," in *54th DAC*, 2017, pp. 1–6.

[2] H. A. R. Homulle, F. Sebastiano, and E. Charbon, "Deep-Cryogenic Voltage References in 40-nm CMOS," *SSCL*, vol. 1, pp. 110–113, 2018.

[3] K. Makinwa, "Smart Temperature Sensors in Standard CMOS," *Procedia Engineering*, vol. 5, pp. 930–939, 2010.

[4] P. A. 't Hart, M. Babaie, A. Vladimirescu, and F. Sebastiano, "Characterization and Modeling of Self-Heating in Nanometer Bulk-CMOS at Cryogenic Temperatures," *JEDS*, vol. 9, pp. 891–901, 2021.

[5] P. A. 't Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and Modeling of Mismatch in Cryo-CMOS," *JEDS*, vol. 8, pp. 263–273, 2020.

[6] P. A. 't Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Subthreshold Mismatch in Nanometer CMOS at Cryogenic Temperatures," *JEDS*, vol. 8, pp. 797–806, 2020.

[7] A. R. Alt and C. R. Bolognesi, "Temperature Dependence of Annealed and Nonannealed HEMT Ohmic Contacts Between 5 and 350 K," *TED*, vol. 60, no. 2, pp. 787–792, 2013.

[8] M. Raman, T. Kifle, E. Bhattacharya, and K. Bhat, "Physical Model for the Resistivity and Temperature Coefficient of Resistivity in Heavily Doped Polysilicon," *TED*, vol. 53, no. 8, pp. 1885–1892, 2006.

[9] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures," *JEDS*, vol. 6, pp. 996–1006, 2018.

[10] Y. Shwarts, V. Borblik, N. Kulish, V. Sokolov, M. Shwarts, and E. Venger, "Silicon Diode Temperature Sensor Without a Kink of the Response Curve in Cryogenic Temperature Region," *Sensors and Actuators A: Physical*, vol. 76, no. 1, pp. 107–111, 1999.

[11] F. Assaderaghi, "DTMOS: Its Derivatives and Variations, and their Potential Applications," in *ICM 2000*, 2000, pp. 9–10.

[12] A. A. Artanov, E. A. Gutiérrez-D, A. R. Cabrera-Galicia, A. Kruth, C. Degenhardt, D. Durini, J. Méndez-V, and S. Van Waasen, "Self-Heating Effect in a 65 nm MOSFET at Cryogenic Temperatures," *TED*, vol. 69, no. 3, pp. 900–904, 2022.