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A 4.5 nV/√Hz Capacitively-Coupled Continuous-Time Sigma-Delta Modulator with an Energy-Efficient Chopping Scheme

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***Abstract*— When chopping is applied to a continuous-time sigma-delta modulator (CTΣΔM), quantization noise fold-back often occurs, leading to increased in-band noise. This can be prevented by employing a return-to-zero digital-to-analog converter (RZ DAC) in the modulator's feedback path and arranging the chopping transitions to coincide with its return-to-zero phases. In this paper, this technique has been extended and implemented in an energy-efficient CTΣΔM intended for the readout of Wheatstone bridge sensors. To achieve a wide common-mode input range, the modulator's summing node is implemented as an embedded capacitively-coupled instrumentation amplifier (CCIA) which can be readily combined with a highly linear 1-bit capacitive RZ DAC. Measurements show that the proposed chopping scheme does not suffer from quantization noise fold-back and also allows a flexible choice of chopping frequency. When chopped at one-tenth of the sampling frequency, the modulator achieves 15 ppm INL, 4.5 nV/√Hz input-referred noise and a state-of-the-art noise efficiency factor (NEF) of 6.1.**

***Index Terms*—Chopping; quantization noise fold-back; energy-efficient; capacitively-coupled instrumentation amplifier; continuous-time delta-sigma modulator; Wheatstone bridge sensor; readout.**

I. Introduction

Continuous-time sigma-delta modulators (CTΣΔMs) can achieve high resolution and energy efficiency, since they do not suffer from the kT/C noise limitations of discrete-time modulators [1]. Consequently, they are often used for the high resolution readout of Wheatstone bridge sensors, e.g. μK-resolution temperature sensors [1], and mPa-resolution differential pressure sensors [2]. Since the output of such sensors is often at the mV-level, such modulators also require low offset, 1/*f* noise and drift [1,2].

In low bandwidth applications such as sensor readout, offset and 1/*f* noise can both be suppressed by the application of dynamic offset-cancellation techniques such as chopping and auto-zeroing [3]. Being a continuous-time technique, chopping can be readily implemented in a CTΣΔM, usually by chopping its first integrator. However, this approach is complicated by the fact that the signal applied to the input chopper then contains large amounts of high frequency quantization noise. This will be chopped, i.e. multiplied by a square-wave, causing some of it to fold back to low frequencies, and thus degrading the modulator's in-band noise [1].

To avoid quantization noise fold-back in a chopped CTΣΔM, several approaches have been proposed. The first is to chop the CTΣΔM at its sampling frequency f_s [2]. This is simple and effective, but often means that the chopping frequency f_{chop} will be higher than necessary, i.e. than the modulator's input-referred 1/*f* noise corner. This, in turn, will result in lower input impedance and amplifier gain, as well as higher current noise and residual offset [3,4,5].

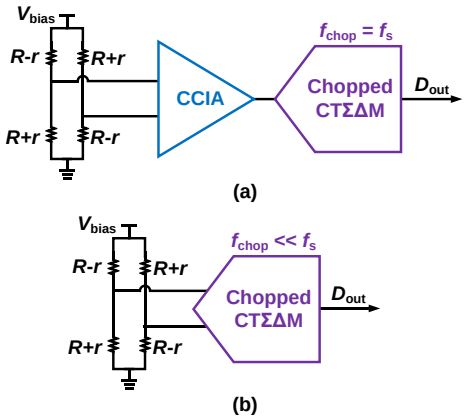

Fig. 1. Bridge readout (a) with a CCIA followed by a CTΣΔM chopped at f_s (b) with a stand-alone CTΣΔM and $f_{chop} << f_s$.

To mitigate these drawbacks, a low-offset instrumentation amplifier (IA) is often inserted in front of a ΣΔM (Fig. 1a) [2,3,6]. In [2], a capacitively-coupled IA (CCIA) was combined with a CTΣΔM, which was then chopped at f_s. Although this approach results in excellent performance, it requires the design of two high-performance circuits.

An alternative approach is to set $f_{chop} << f_s$ and reduce the quantization noise at the modulator's input, either by using a multi-bit digital-to-analog converter (DAC) [7,8], or by filtering the output of a 1-bit DAC with an analog low-pass filter [1], or a finite impulse response (FIR) filter [9,10]. The readout architecture can then be simplified as shown in Fig. 1b [1,7,8,10]. However, this approach requires a more complex DAC or feedback path, often resulting in lower energy-efficiency [1,7,10] or lower linearity [8] compared to the designs reported in [2,3]. Moreover, lowering f_{chop} leads to larger chopper ripple, which may then require a high-order decimation filter or reduce the modulator's useful bandwidth [7,10].

In [11], we proposed a simple approach to prevent quantization noise fold-back in a chopped CTΣΔM by arranging the chopping transitions to coincide with the return-to-zero (RZ) phases of a resistive RZ DAC. Simulations show that this approach works well and also allows f_{chop} to be flexibly chosen to match the modulator's 1/*f* corner frequency. In this paper, we extend this approach to a CTΣΔM with a RZ capacitive DAC (CDAC) and present measurement results to demonstrate its effectiveness. Intended for Wheatstone bridge readout, the modulator achieves a wide CM input range by using an embedded capacitively-coupled instrumentation amplifier (CCIA) to sum the input signal and the output of the CDAC. Measurement results show that compared to other capacitively-coupled (CC) CTΣΔMs [7,10], the resulting design achieves state-of-the-art energy-efficiency and linearity.

II. Chopped CC-CTΣΔM

A. Chopping in a CTΣΔM with a 1-bit RZ DAC

In a CTΣΔM with a resistive non-return-to-zero (NRZ) DAC and an active OTA-RC first integrator (Fig. 2), the signal at the integrator's summing node is given by

$$V_{sum} \cong \frac{V_{in} + V_{DAC}}{2 + G_m \cdot R_{in}}, \quad (1)$$

where $R_{in} = R_{DAC}$, V_{in} is the input signal, V_{DAC} is the wide-band feedback DAC signal, and G_m is the transconductance of the OTA. As described in [9], quantization noise fold-back occurs because the OTA's input capacitors C_p need to be rapidly charged and discharged by V_{sum} whenever the choppers change state, which means that the quantization noise component of V_{DAC} is effectively sampled at $2f_{chop}$. The resulting fold-back can be minimized by ensuring that $2f_{chop}$ coincides with the notches of a FIR-DAC [9].

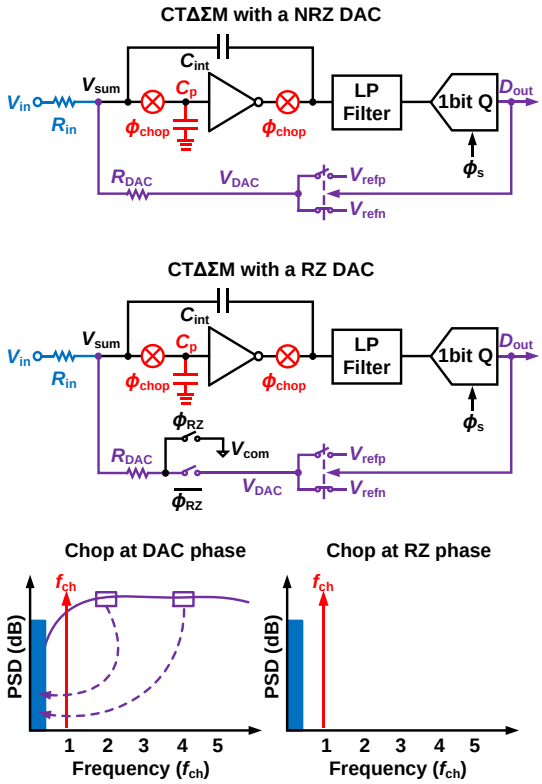

Fig. 2. Chopping in CTΣΔMs.

Alternatively, quantization noise fold-back can be prevented by ensuring that V_{sum} is free of quantization noise at the chopping transitions, i.e. by ensuring that V_{DAC} is zero (Fig. 2) [11]. This condition can be met with the help of a RZ DAC. In this case, V_{sum} is given by

$$V_{sum} \cong \begin{cases} \dfrac{V_{in} + 2V_{DAC}}{3 + G_m \cdot R_{in}}, & \phi_{RZ} = 0 \\ \dfrac{V_{in}}{1 + G_m \cdot R_{in}}, & \phi_{RZ} = 1 \end{cases}, \quad (2)$$

where $R_{in} = 2R_{DAC}$, $\phi_{RZ} = 1$ corresponds to the RZ phase. Compared to the use of a FIR-DAC, this results in a simpler implementation. A further advantage is that the chopping period can now be adjusted in steps of $1/f_s$, allowing f_{chop} to be optimally chosen with respect to the OTA's $1/f$ noise corner.

B. CCIA inside the CTΣΔM Loop

Open-loop integrators, such as Gm-C integrators or the combination of a Gm stage and a current-controlled oscillator (CCO) [1,7,8,10,12], are usually more energy-efficient than closed-loop RC integrators. However, they have a much smaller linear range, typically only a few tens of millivolts and so are not compatible with the large output swing of a 1-bit DAC. To reduce this, multi-bit DACs and extra filtering can be used in the modulator's feedback path [7,8,10,12]. Moreover, the linearity of an open-loop Gm stage can be improved by source-degeneration, although this comes at the expense of increased noise, i.e. reduced energy efficiency [1].

Alternatively, the virtual ground of an energy-efficient CCIA can be used as the continuous-time summing node of a CTΣΔM. Due to the local feedback provided by the CCIA, the voltage swing at its virtual ground will be quite small, and so it is compatible with the use of a 1-bit DAC. The gain of the CCIA will suppress the noise contributions of the modulator's succeeding stages, and so the modulator's noise will still be dominated by a single stage. The requirements on CCIA's gain accuracy and linearity are quite relaxed, since it is within the modulator's overall feedback loop.

III. Circuit Implementation

Fig. 3 shows the simplified block diagram of the proposed CTΣΔM. A CCIA is embedded in a 2nd order CTΣΔM with a 1-bit RZ CDAC and 2 MHz sampling frequency. To suppress their $1/f$ noise and offset, both the CCIA and the first integrator are chopped at 200 kHz during the RZ phase of the DAC. As in [2], the CCIA's input chopper is driven capacitively, which allows it to handle input common-mode (CM) voltages of up to 3.3 V, even though the CCIA itself is powered from a 1.8 V supply. An extra DAC (C_{DAC1}) compensates for systematic bridge offset, thus maximizing the modulator's useful dynamic range. In an extension of the approach described in [2], a multi-path positive feedback network (C_{pf}, C_{DAC-C} and C_{DAC2}) supplies most of the current required to charge the input capacitors C_{in} of the CCIA, thus boosting the modulator's input impedance.

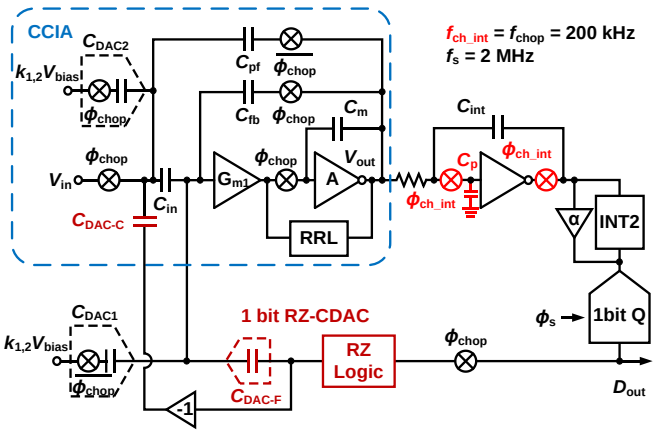

Fig. 3. The proposed CC-CTΣΔM.

A. CCIA

To drive the resistive load of the first integrator, the CCIA is based on a two-stage Miller-compensated amplifier. It employs a PMOS input pair to achieve a low 1/*f* noise corner (100 kHz). The closed loop gain of the CCIA is set to 50×, providing sufficient suppression for the noise of the modulator's succeeding stages.

Monte Carlo simulations show that the input referred offset of the amplifier can be as high as 1.5 mV (3σ) without chopping. This offset is comparable to the input signal, and so the resulting chopper ripple may overload the modulator. To prevent this, a ripple-reduction-loop (RRL) is used to suppress the initial offset [3].

B. RZ CDAC

The operation of the RZ logic is illustrated in Fig. 4. The DAC's output voltage V_{out}, is reset to V_{cm} when ϕ_{RZ} is high. When ϕ_{RZ} is low, V_{out} is either pulled up to V_{refp} or pulled down to V_{refn} depending on the chopped bitstream, $\phi_{chop} \cdot bs$. The resulting tri-level voltage is then transferred via $C_{DAC\text{-}F}$ to the virtual ground of the CCIA, counterbalancing the input signal, which is transferred via C_{in}.

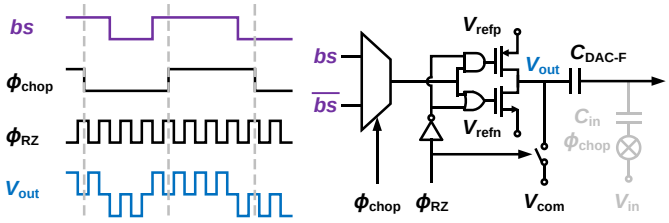

Fig. 4. The simplified chopped RZ CDAC (single-end) and its timing diagram.

C. Multipath Input Impedance Boosting Scheme

Like the CCIA in [2], the input impedance Z_{in} of the CC-CTΣΔM would normally be defined by the switched-capacitor resistance associated with C_{in}, which is a few hundred kilo-Ohms at f_{chop} = 200 kHz. To boost Z_{in}, an auxiliary circuit must supply the charge Q_{in} that is required to charge and discharge C_{in} during every chopping transition. This can be done either by using a capacitively-coupled positive feedback path [2,4], or an auxiliary pre-charge path [6]. However, the later method requires active buffers, which will limit the input CM range of the CC-CTΣΔM and thus negate one of the main advantages of using a CCIA as its input stage.

In a normal CCIA, a positive feedback path between its input and output can provide the required compensation charge, Q_{com}. This is given by [4]

$$Q_{com} = C_{pf} V_{out} \approx C_{in} V_{in} = Q_{in} . \quad (3)$$

In general, V_{in} consists of two parts, the useful bridge signal, V_{sig} and the unwanted bridge offset, V_{os}. In the proposed modulator (Fig. 4), V_{os} will be cancelled by C_{DAC1} before amplification and so cannot be extracted from V_{out}. Moreover, V_{out} contains the DAC signal which should not be fed to the CCIA input.

To generate the required offset compensating charge Q_{os} and DAC charge Q_{DAC}, a multipath input impedance boosting scheme is used. As shown in Fig. 3, it consists of two extra digital controlled paths (C_{DAC2} and $C_{DAC\text{-}C}$) as well as the conventional analog positive feedback path via C_{pf}. The resulting compensation charge Q_{com} is then given by:

$$Q_{com} = C_{pf} V_{out} + Q_{os} - Q_{DAC} \approx Q_{in} . \quad (4)$$

IV. Measurement Results and Comparison

The CC-CTΣΔM has been implemented in 0.18 µm CMOS technology. It occupies an active area of 0.75 mm^2 as shown in Fig. 5. With f_s = 2 MHz and f_{chop} = 200kHz, it consumes 1.2 mA from a 1.8 V supply.

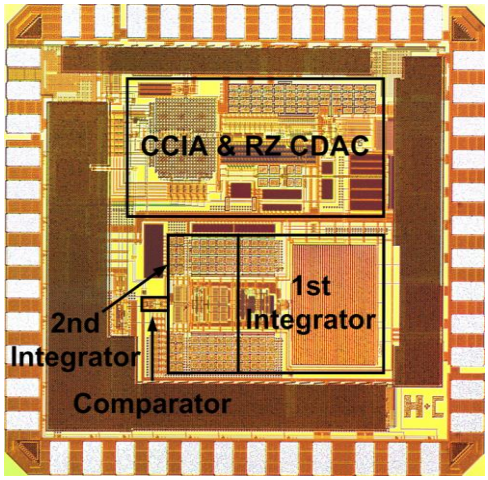

Fig. 5. Die micrograph of the CC-CTΣΔM.

To verify the effectiveness of the proposed chopping scheme, the chopping transitions of the CCIA and the 1st integrator can be arranged to coincide with either the RZ or the DAC phases of the CDAC. As shown in Fig. 6, when the CCIA is chopped during the DAC phase, severe quantization noise fold-back can be observed. It should be noted that in this case the modulator is also overloaded by chopper ripple. This is because the RRL now senses chopped quantization noise as well as up-modulated offset ripple and so fails to settle properly.

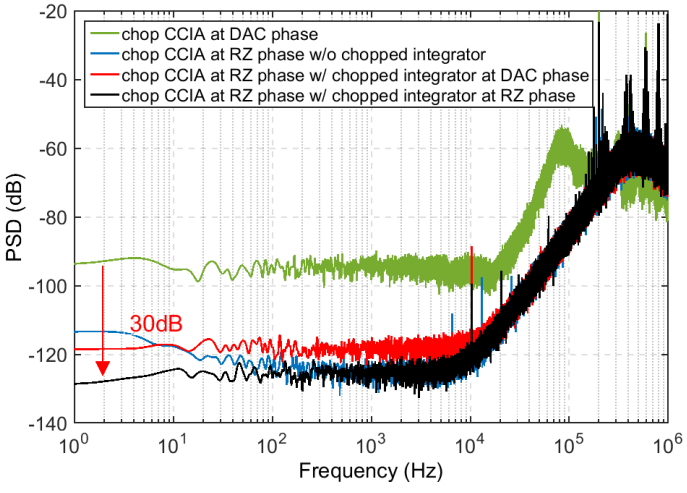

Fig. 6. Measured bitstream PSD when CCIA is chopped during DAC phase (green), during RZ phase (blue), then with 1st integrator chopped during DAC phase (red), and with first integrator chopped during RZ phase (black).

Chopping the CCIA during the RZ phase reduces the in-band noise floor by about 30 dB, to 4.5 nV/√Hz as shown in Fig. 6. The associated 200 Hz 1/*f* noise corner can be reduced to about 0.05 Hz by also chopping the first integrator. The bitstream spectra are also shown when the 1st integrator is chopped during the RZ and DAC phases. It can be seen that despite the CCIA's gain (50×), chopping during the RZ phase still produces significant improvements, reducing the input-referred in-band noise by 8 dB.

To qualify the modulator as a bridge readout, 10 samples were measured. As shown in Fig. 7a, it achieves a relative gain error of 0.2% and a measured INL of 15 ppm over the full input range (Fig. 7b). To capture the effects of finite input impedance, a voltage source with a 2 kΩ impedance (the impedance of the targeted Wheatstone bridge sensor) was used for the INL measurements. As in [2], the multipath input impedance boosting scheme boosts the input impedance of the modulator by a factor of 5 to about 1.2 MΩ.

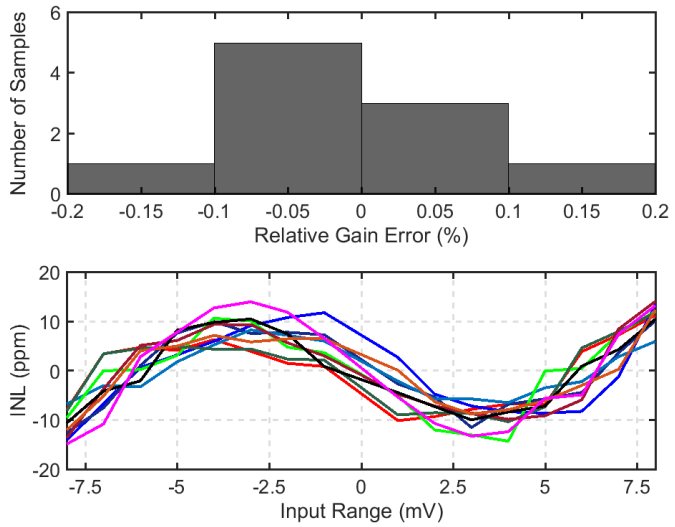

Fig. 7. Mreasured relative gain accuracy of 10 samples (a), Measured INL of 10 samples (b).

TABLE I. the State-of-the-Art Bridge Readout ICs

	[1]	[2]	[7]	[10]	This work
Architecture	Gm-C CTΣΔM	CCIA+ CTΔΣM	CC-CTΔΣM	CC-CTΔΣM	CC-CTΔΣM
Year	2012	2017	2017	2017	2017
Input stage	PMOS	PMOS	PMOS	PMOS	PMOS
Technology	0.7 µm	0.18 µm	40 nm	0.18 µm	0.18 µm
Supply Voltage (V)	5	1.8	1.2	1.8	1.8
Current (mA)	0.24	1.2	0.0175	0.070	1.2
±Input range (mV)	40	10+120(DC)	50	40	8+120(DC)
CM Input Range (V)	0–2.5	0–3.3	0–1.2	0–1.8	0–3.3
INL (ppm)	15	28	79*	84*	< 15
Offset (µV)	1	7	300	50	< 72
Offset Drift (nV/ºC)	--	12.5	--	--	12.3
Input noise density (nV/√Hz)	20	3.7	140	98	4.5
NEF	12	5.0	22.6	31.9	6.1

* Estimated from THD.

In Table I, the CC-CTΣΔM's performance is summarized and compared with that of other state-of-the-art bridge readout ICs. Compared to other ADCs designed for bridge readout, it achieves the best INL and noise efficiency factor (NEF). Compared to [2], which employs a separate CCIA as a pre-amplifier, its offset is relatively high, mainly due to the interaction between the mismatch of the differential CDAC capacitors (about 0.36%) and the 1.8 V reference voltage. However, it is negligible compared to the millivolt-level offset of typical Wheatstone bridge sensors. It is also quite stable, with an offset drift of < 12.5 nV/ºC, and so can be well tolerated in many applications.

Conclusions

In this paper, we show, via measurement results, that quantization noise fold-back caused by chopping a CTΣΔM can be greatly suppressed by chopping during the return-to-zero phases of a RZ DAC. The proof-of-concept modulator employs a novel architecture in which a CCIA is used as the summing node of a CTΣΔM, thus enabling the use of a simple 1-bit RZ CDAC to achieve both energy-efficiency (NEF = 6.1) and high linearity (INL < 15 ppm).

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