17 GHz RF Front-Ends for Low-Power Wireless Sensor Networks

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***Abstract*—A 17 GHz low-power radio transceiver front-end implemented in a 0.25 μm SiGe:C BiCMOS technology is described. Operating at data rates up to 10 Mbit/s with a reduced transceiver turn-on time of 2 μs, gives an overall energy consumption of 1.75 nJ/bit for the receiver and 1.6 nJ/bit for the transmitter. The measured conversion gain of the receiver chain is 25–30 dB into a 50 Ω load at 10 MHz IF, and noise figure is 12$\pm$0.5 dB across the band from 10 to 200 MHz. The 1-dB compression point at the receiver input is $-$37 dBm and IIP_3 is $-$25 dBm. The maximum saturated output power from the on-chip transmit amplifier is $-$1.4 dBm. Power consumption is 17.5 mW in receiver mode, and 16 mW in transmit mode, both operating from a 2.5 V supply. In standby, the transceiver supply current is less than 1 μA.**

***Index Terms*—BAW resonator, energy/bit, energy efficiency, low-power radio, radio transceiver front-end, SiGe BiCMOS technology, wireless sensor networks.**

I. Introduction

A wireless sensor network (WSN) consists of physically-small sensor nodes networked together by a common protocol. They may be embedded unobtrusively in their environment, and are typically distributed in order to monitor their surroundings (e.g., measuring temperature, or motion detection, etc.). WSNs enable applications ranging from outdoor environmental monitoring of air, water or soil, to home automation (e.g., smart houses) and inventory control in factories or warehouses [1]. The combination of computing, wireless communication and sensing technologies required may be implemented as a system-on-a-chip (SoC) or in a single package (SiP). The radio transceiver is typically more power-hungry than other sub-systems in a sensing node (e.g., sensor interface), thereby placing severe restrictions on the duty cycle or 'on time' of the wireless connection when operated from a battery. For example, a node could transmit one kilobyte of data over a distance of 100 meters or execute 3 million instructions with 3 J of energy [1]. This work aims at a radio transceiver implementation suitable for monolithic integration with energy efficiency on the order of 1 nJ/bit in order to maximize battery lifetime.

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State-of-the-art low-power radios are compared in data rate, power consumption and the resultant energy/bit in Fig. 1. The energy/bit is used as a benchmaking metric of energy efficiency. Some of the early WSN transceiver examples were focussed on minimizing the total power consumed rather than energy efficiency [2], [3]. Better efficiency is achieved when the absolute power consumption and data rate requirements are traded-off in order to optimize the average energy/bit. In applications such as acoustic tracking and detection, the always "on" wake-up receiver [4] and passive direct conversion receiver (DCR) [5] shown in Fig. 1 are good candidates due to their microwatt power consumption (i.e., 52 μW and 330 μW) in continuous operation at low data rates. In other WSN applications, lower average data throughput is required and transceivers can be cycled on and off in order to realize microwatt levels of power consumption on-average (i.e., a duty-cycled transceiver). Robust modulation schemes and receiver architectures, which require milliwatt levels of power consumption, may be used in a duty-cycled transceiver to achieve more reliable RF performance at the desired average power dissipation. For example, a 800 bit/s super-regenerative (SR) transceiver [6] and the 10 Mbit/s 17 GHz radio proposed in this work are duty-cycled transceivers aimed at different WSN applications and data rates (see Fig. 1). Both of them achieve 2 nJ/bit energy efficiency, which is more than one order of magnitude less than conventional transceivers such as Bluetooth or Zigbee transceivers.

Intelligent WSNs which can gather large volumes of data using a small form factor radio and having years of lifetime without battery recharging or replacement are required for wearable or implantable health monitoring (i.e., homecare) devices [7]. Although low data rate radio can always be used when in-node data compression is employed before transmission, a data rate that matches the volume of data for transmission (e.g., Mbit/s rates for video sources) may lead to higher energy efficiency with less hardware, as described in [8] and [9]. The latest reported motes for wireless image sensor networks compress the raw data in-node before transmission at 250 kbit/s by a Zigbee compliant radio. The resultant energy/bit is as high as 90 nJ/bit [10]. Energy efficiency may be improved by more than an order of magnitude if a Mbit/s data rate radio is adopted.

This paper presents a low-power radio transceiver suitable for short-range WSN applications requiring multi-Mbit/s data rates. The 17 GHz unlicensed band available in Europe [11] is chosen for this study due to the 200 MHz available spectrum, few potential interferers, small antenna size, good indoor propagation properties over a short range, and potential for integration in silicon VLSI technologies. The low-power radio architecture proposed in this work does not require a standard PLL (thereby

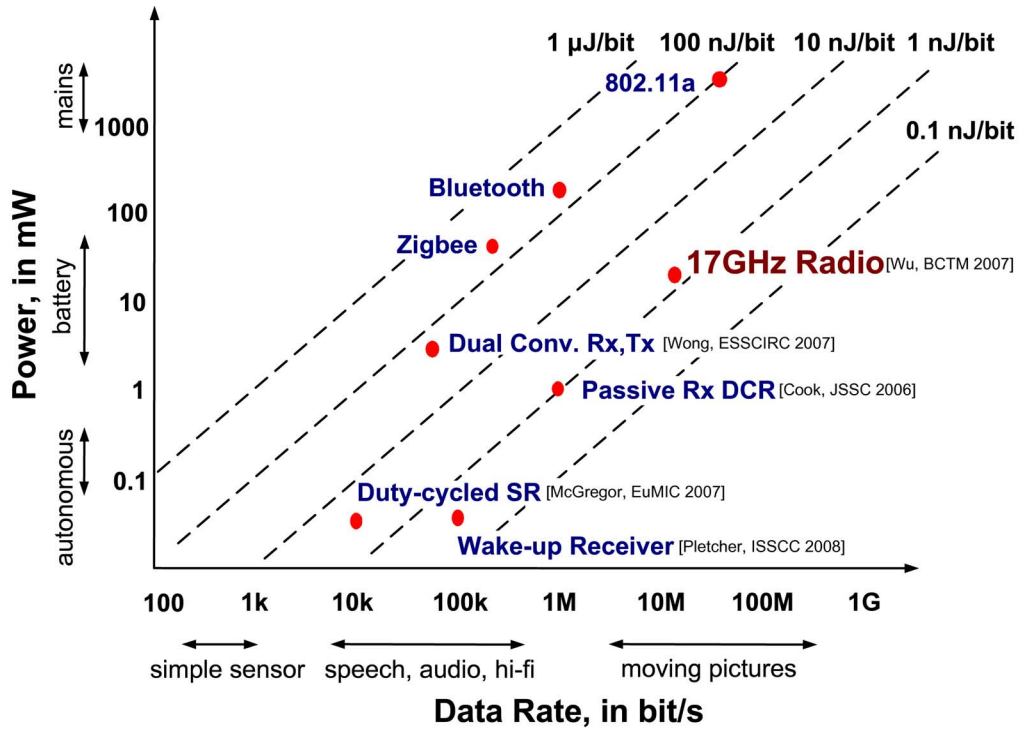


Fig. 1. Energy/bit for state-of-the-art low-power radios.

reducing turn-on time to $\sim$ 2 μs), supports a 10 Mbit/s data rate, and demonstrates an energy/bit requirement for the transceiver as low as 2 nJ/bit (see Fig. 1). The prototype receiver and transmitter front-ends are implemented in a production SiGe:C BiCMOS technology (NXP Semiconductors QUBiC4X) with 130 GHz peak f_{T} and 140 GHz f_{max}, respectively, for the NPN bipolar transistor [12].

Section II of the paper describes the 17 GHz ultra low-power radio architecture and system specifications. Implementation details of the transceiver are presented in Section III, including design details of the LNA, mixer, 8-phase LO signal generator and IF transimpedance amplifier in the receiver chain, and the frequency doubler and transmit amplifier (PA) in the transmitter chain. Measurement results for both receiver and transmitter prototypes are then presented in Section IV.

II. Radio Architecture and System Considerations

This section begins with a brief comparison of four low-power transceiver architectures, emphasizing the receiver side. The benefits of the direct conversion architecture are shown to outweigh potential disadvantages in a WSN application. A low-power transceiver based on direct conversion and intended for operation in the 17 GHz band is then described, including its desired specifications and a radio link budget analysis.

A. Low-Power Radio Architecture Comparison

Energy demand dominates the design considerations for a low-complexity transceiver aiming at wireless sensor network applications, where operating time from a limited energy source is paramount. In order to minimize power consumption, the range of the wireless link and the transmit and receive duty cycles must be constrained. The duty cycle of the transmitter may be low, whereas the receiver duty cycle must be larger in order to permit acquisition of data from nodes that arrive asynchronously, or at random intervals. Conventional high performance radio receivers employing the super-heterodyne architecture require off-chip interfaces and separate packaging of frequency selective filters, which results in higher power consumption (e.g., driving a 50 Ω interface), increased cost, and limitations on physical size. Two other receiver architectures used in low-power applications are the super-regenerative [13]–[15] and power detection architecture [16]. The super-regenerative receiver requires a high-Q (up to 1000) off-chip resonator in order to achieve high sensitivity, and may be sensitive to frequency pulling by interfering signals and wiring parasitics when implemented at 17 GHz. Additionally, it can suffer from slow settling time when a high-Q resonator is used, and thus is typically limited to data rates of hundreds of kbit/s [15]. The envelope detector-based receiver architecture on the other hand, does not require a frequency synthesizer and then the receiver can be turned on quickly. However, it can be sensitive to wideband RF interference unless a high-Q (up to 100) RF channel select filter is used. Such a filter is difficult to integrate on-chip with adequate dynamic range and power consumption in the low-mW range.

The proposed architecture for a wireless sensor receiver shown in Fig. 2 uses direct conversion from RF to baseband, but retains the advantage of a low-intermediate frequency (low-IF) architecture. The direct conversion receiver performs channel selection at baseband, thereby eliminating multiple stages of frequency conversion and intermediate frequency

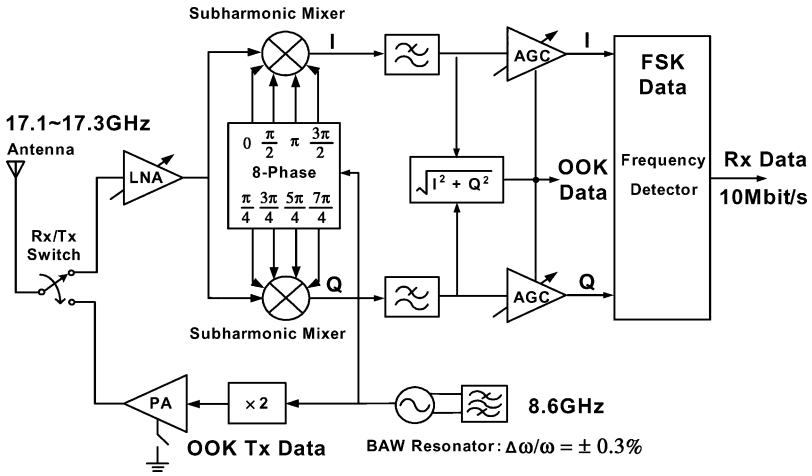


Fig. 2. Proposed 17 GHz transceiver architecture.

filtering and gain stages. This can result in lower power operation, less chip area and the potential for higher integration of the transceiver in a monolithic implementation [17]–[19].

The primary drawbacks of direct conversion from RF to baseband, which are flicker noise and DC offset interfering with the baseband signal detection circuits, are addressed at the system level for the design proposed here. Frequency-shift keying (FSK) is adopted, where signalling frequencies are selected which are above the flicker noise (i.e., 1/f) corner frequency. The DC offset arising from self-mixing between the local oscillator (LO) signal and its leakage to the RF input or the antenna is avoided by using a subharmonic mixer, in which the local oscillator is set at one-half of the RF frequency. The bipolar devices in the BiCMOS technology used for this work have a much lower 1/f corner than their CMOS equivalents (i.e., approx. 200 kHz). The analog FSK demodulator can be desensitized to any DC offset when it is operated at a higher frequency. Thus, advantages of the low-IF receiver architecture are incorporated in order to simplify integration on-chip.

B. 17 GHz WSN Radio Architecture and Modulation Schemes

In order to minimize the turn-on time and overall power consumption of the radio transceiver, a PLL is not used (see Fig. 2). Instead, an 8.6 GHz bulk acoustic wave (BAW) resonator generates a low phase noise reference that is used as the LO signal in both the receiver and transmitter [20]. The upper limit of BAW technology at the present time is close to 10 GHz [21], so the local oscillator is set to one-half of the 17.2 GHz RF. Subharmonic mixers driven by multi-phase LO inputs are employed for I/Q down-conversion between the LNA output and IF stage, separating the LO and RF frequencies by a factor of two. Although the second harmonic of the LO may be generated by circuit non-linearities, it is attenuated by the differential topologies employed for most of the circuit blocks on-chip. After down-conversion, a low-pass filter (LPF) and automatic gain control (AGC) IF amplifier perform channel selection and signal amplification prior to demodulation. OOK (on/off keying) and FSK demodulation can both be supported in the receiver chain and implemented in the analog domain in order to conserve power. Square root detection of the I/Q signal amplitudes demodulates an OOK signal, while an analog frequency discriminator (see Fig. 2) realizes FSK demodulation.

On the transmitter side, a frequency doubler is used to generate a 17.2 GHz carrier signal from the 8.6 GHz local oscillator. OOK modulation is implemented by direct amplitude modulation of the transmitter bias current using the baseband data, which can be more energy-efficient than FSK or other more elaborate modulation schemes [16].

The capability for both FSK and OOK may be further exploited in a master-slave (asymmetrical) system [22]. For example, assume that a slave node first transmits an OOK signal. The master device locks onto this transmission and re-transmits an FSK signal with the desired data encoded onto its carriers. The master is able to continuously listen and search for the slave's transmission in both time and frequency spaces because it does not have to be battery powered (i.e., it can be supplied from the mains). This work provides a prototype transceiver solution for the slave nodes.

C. Link Budget and Transceiver Specifications

The specifications of the proposed 17 GHz low-power transceiver are summarized in Table I. Operating a data link in the 17 GHz band is a compromise between data rate and range, as described in [23]. The frequency allocation close to 17 GHz in Europe can support a 20 Mbit/s data rate and propagate up to 50 meters according to the analysis in [24], making it suitable for many indoor applications.

Studies of radio wave propagation indoors at 17 GHz have shown that the received power level decays at a rate equal to that of free space propagation (or less) with increasing distance from the transmitter for line of sight scenarios (i.e., path loss exponent $\alpha = 1.3$–2.0) [24]. A margin of 20 dB is included in the link budget to account for signal fading, which may be caused by obstructions such as thick concrete walls, metal objects, or other bodies positioned between the transmitter and receiver.

To realize a bit-error rate (BER) of 10^{-3} at a data rate of 10 Mbit/s (e.g., 20 MHz channel bandwidth), the signal-to-noise ratio (SNR) at the input to the (coherent) OFSK demodulator should be at least 11 dB, if a 2 dB implementation

TABLE I
17 GHz LOW-POWER RADIO SYSTEM SPECIFICATIONS

Link radius	10 m
Network configuration	Master-slave asymmetrical link
Modulation schemes	Rx: OFSK & OOK; Tx: OOK
Data rate	10 Mbit/s (20 MHz BW)
Bit error rate (BER)	10^{-3} (without forward error correction)
Antenna	Single-ended patch antenna (4 mm × 4 mm @ 17 GHz)
Tx/Rx antenna gain	5 dBi
Frequency reference	BAW resonator at 8.6 GHz (±0.3% absolute frequency accuracy)
Receiver sensitivity	-80 dBm
Receiver system NF	10 dB
Receiver IIP_3	> -30.5 dBm
Transmitter P_{out}	> 0 dBm
Transceiver power budget	< 50 mW in total

margin is assumed. The noise figure (NF) of the receiver is related to the link parameters by the equation [25]

$$\mathrm{NF\,(dB)} = P_{\mathrm{rx}}\,(\mathrm{dBm}) + 174\,(\mathrm{dBm}) - \mathrm{SNR\ (dB)} - 10\log_{10}\mathrm{BW\,(dB)} \quad (1)$$

where P_{rx} is the receiver sensitivity, -174 dBm is the thermal noise power of a 50 Ω source in a 1 Hz bandwidth, and BW is the channel bandwidth.

The required transmitter output power (P_{tx}) is given by

$$P_{\mathrm{tx}}\,(\mathrm{dBm}) = P_{\mathrm{rx}}\,(\mathrm{dBm}) - G_{\mathrm{tx}}\,(\mathrm{dB}) - G_{\mathrm{rx}}\,(\mathrm{dB}) + 10\log_{10}\frac{4\pi^2 d^{\alpha}}{\lambda^2}\,(\mathrm{dB}) + 20\,(\mathrm{dB}) \quad (2)$$

where G_{tx} and G_{rx} are the gains of the receive and transmit antennas, respectively (5 dB in this case), λ is the free-space wavelength (1.76 cm at 17 GHz), d is the maximum distance between receiver and transmitter (assume 10 m), α is the path loss exponent (assume $\alpha = 2$ in free space), and 20 dB is the assumed fade margin. Considering the constraint on power consumption for both receiver and transmitter in the WSN applications, there are trade-offs between receiver sensitivity, receiver NF and transmitter output power, as shown in Fig. 3. If a transmitter output power of 2 dBm are selected, according to Fig. 3(b), the required receiver noise figure is about 10 dB, and the resulted receiver sensitivity is better than -80 dBm from Fig. 3(a) (i.e., the target in Table I).

The strongest possible interferers in the 17 GHz band are most likely to be generated by nearby nodes in the same network. Assuming a minimum distance between transceivers of 1 meter in the WSN, an interfering signal strength of -47 dBm is expected from the nearest node. An input referred third-order intercept point (IIP_3) better than -30 dBm is therefore required for the receiver in order to preserve the desired SNR at the demodulator in the presence of this level of interference.

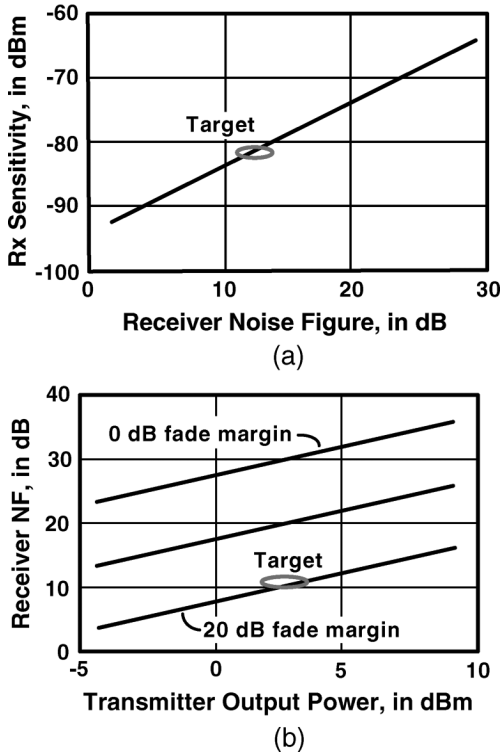


Fig. 3. (a) Receiver sensitivity versus receiver NF for 10^{-3} BER. (b) Receiver NF versus transmitter output power for 10 m radio link.

III. TRANSCEIVER RF FRONT-END IMPLEMENTATION

The 17 GHz receiver front-end prototype consists of a single-ended LNA, subharmonic in-phase (I) and quadrature (Q) mixers, and an 8-phase LO signal generator with buffers. Each mixer drives its own IF transimpedance amplifier. On the transmit side, an LO frequency doubler and Class-AB transmit amplifier are implemented.

A. Low-Noise Amplifier (LNA)

The LNA (refer to the schematic of Fig. 4) consists of inductively degenerated cascode Q_1 and Q_2, driving resonant tank L_{o} and $C_{\mathrm{o1-2}}$, a propotional to absolute temperature (PTAT) biasing circuit [detailed in Fig. 4(b)], and a simple current-steering gain control circuit implemented using Q_3 and M_1. Inductors L_{B} (250 pH) and L_{E} (50 pH) are selected together with the emitter width of Q_1 in order to realize noise and impedance matching simultaneously. Scaling input transistor Q_1 ($0.4\ \mu\mathrm{m} \times 10.3\ \mu\mathrm{m}$) brings the real part of the optimum source impedance for minimum noise figure (i.e., $\mathrm{Re}[Z_{\mathrm{opt}}]$) close to 50 Ω at 17 GHz. Gyration of the emitter impedance of L_{E} in series with the base resistance of Q_1 sets the real part of the input impedance to 50 Ω thereby matching $\mathrm{Re}[Z_{\mathrm{in}}]$ within the desired operating range (17.1–17.3 GHz). The inductor L_{B} connected in series with the base is made series resonant with the input loop to set the imaginary part of the input impedance. Cascode transistor Q_2 suppresses the voltage gain of Q_1 and isolates the receiver input from the LNA output as required for a direct conversion receiver. The $C_{\mathrm{o1-2}}$ are used in the test structure of LNA to match the output impedance to 50 Ω for measurement, whereas in the receiver testchip, the output of

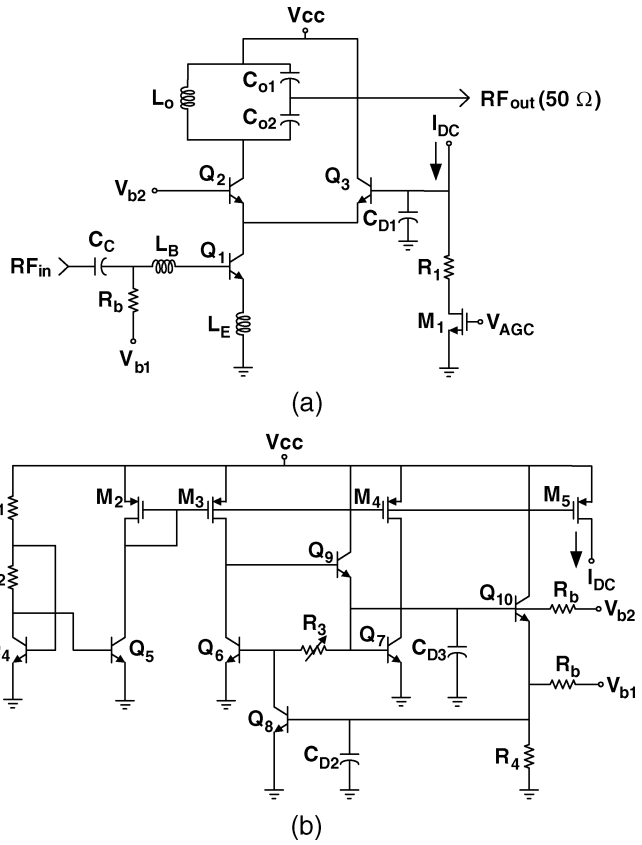


Fig. 4. (a) 17 GHz LNA with gain control. (b) PTAT bias circuit for LNA.

the LNA is tapped from the collector of Q_2 and AC coupled to the mixer RF input.

For biasing, a current peaking circuit formed by Q_4, Q_5, R_1, and R_2 generates a current that is independent of supply $V_{\rm CC}$ that is then mirrored to other branches of the circuit by pMOS transistors M_2 to M_5. The currents in M_3 and M_4 are in a ratio of 1:2, and are forced into transistors Q_6 and Q_7, respectively. The $V_{\rm BE}$ difference between Q_6 and Q_7 generates a PTAT current through resistor R_3. This same PTAT current is supplied by the collector of transistor Q_8 and is mirrored to RF input transistor Q_1 by voltage $V_{\rm b1}$ to provide constant gm for Q_1. The value of the PTAT current is set by R_3 and the ratio of Q_6 and Q_7 emitter areas (in this case 1:2), and it can be controlled by making R_3 a variable resistor.

Given the wide dynamic range of the RF input signal, the gain of the receiver must be variable in order to maintain a relatively constant signal amplitude at the demodulator input. A simple high-gain/low-gain control is added to the LNA as part of the overall gain control scheme. In the high-gain mode, transistor Q_3 is turned-off completely and RF current from Q_1 flows via Q_2 into the load. In the low-gain mode, transistor Q_3 diverts a portion of the RF current thereby reducing the LNA gain. The state of Q_3 (i.e., either on or off) is controlled by nMOS transistor M_1 working as a voltage-controlled resistor. The bias current for M_1 is derived from the drain of M_5 in Fig. 4(b).

B. Subharmonic Mixer With Output Transimpedance IF Amplifier

The schematic diagram of the single-balanced I/Q mixer is shown in Fig. 5. It operates in subharmonic mode [26], [27] and is driven by eight polyphase LO signals generated by a filter and interpolation network operating at one-half of the RF input frequency (i.e., approx. 8.6 GHz). Quadrature LO signals drive each single-balanced mixing pair (e.g., Q_2 to Q_5 in Fig. 5) and thus two groups of quadrature LO signals are needed to drive the I and Q mixers. A 45° phase shift between the quadrature LOs driving each mixer is required to realize quadrature down-conversion of the RF input to the mixer outputs. A common-emitter (CE) input stage converts the RF voltage from the LNA output to a current for down-conversion. In order to improve the mixer linearity and conversion gain, input transistor Q_1 is inductively degenerated and its bias current is set at 1.5 mA. In order to reduce the LO drive-voltage, current bleeding resistor R_0 is added to maintain a 150 μA bias current through each transistor in the mixer quads. As the RF path is single-ended, the I and Q mixers can share the same CE input stage. The degeneration inductance used is equal in value to the inductance of the LNA load.

The IF transimpedance amplifier (TIA) improves the receiver conversion gain and mixer linearity by suppressing voltage swing at the IF output at the expense of 0.5 mA current consumption for each amplifier. The TIA schematic diagram is shown in Fig. 6. The time constant of the feedback network formed by resistor $R_{\rm f}$ (2 kΩ) in parallel with $C_{\rm f}$ (3 pF) sets the closed-loop bandwidth of the TIA to 20 MHz, and the conversion gain of the mixer to approximately 20 dB. IF current from the mixer first flows into differential input transistors Q_1 and Q_2 and is amplified by the AC current gain, β. A gain boosting stage consisting of positive feedback core Q_3 to Q_6 further increases the open loop current gain of the opamp above 60 dB. The emitter area of Q_{5-6} is four times the area of Q_{3-4}, further enhancing the current gain. Low-pass filtering via R_3 and C_1 reduces the loop gain at high frequency to ensure stability. Transistor Q_7 together with R_1 and R_2 form a common-mode control loop which forces the bias current to track the input bias current.

C. 8-Phase LO Generator

A three-stage polyphase filter generates the quadrature LO signals on-chip (see Fig. 7). There are three poles in the filter (located at 6.2, 8.6, and 12.0 GHz) in order to realize an in-band amplitude and phase mismatch within 3%. The filter is designed for equiripple response in the stopband and flat amplitude response in the passband. Additional poles improve the bandwidth and tolerance to filter component variations at the expense of higher attenuation. A resistive interpolation network (refer to Fig. 7(b)) following the polyphase filter generates the 8 phases required to drive the LO inputs of the I and Q subharmonic mixers. Choosing resistor R_3 as

$$R_3 = (2\sqrt{2}+2)R_2 = 4.83R_2 \tag{3}$$

equalizes the amplitudes and gives a 45° phase shift between the sequential outputs. The impedance level of the interpolation network is approximately 1 kΩ, which does not substantially load the polyphase filter or the mixer LO ports. In order to compensate for attenuation of the LO in the polyphase and interpolation networks, a buffer is added between the LO input and the polyphase filter to provide a 500 mV peak swing (single-ended)

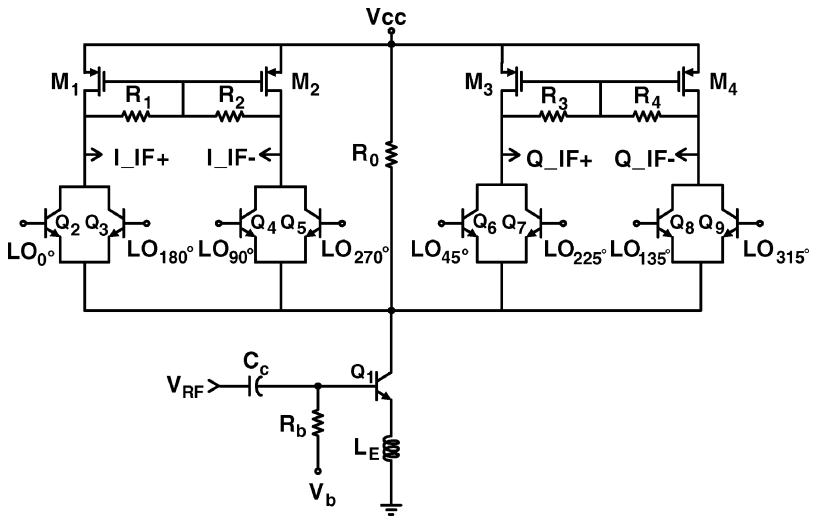


Fig. 5. Schematic of subharmonic mixer.

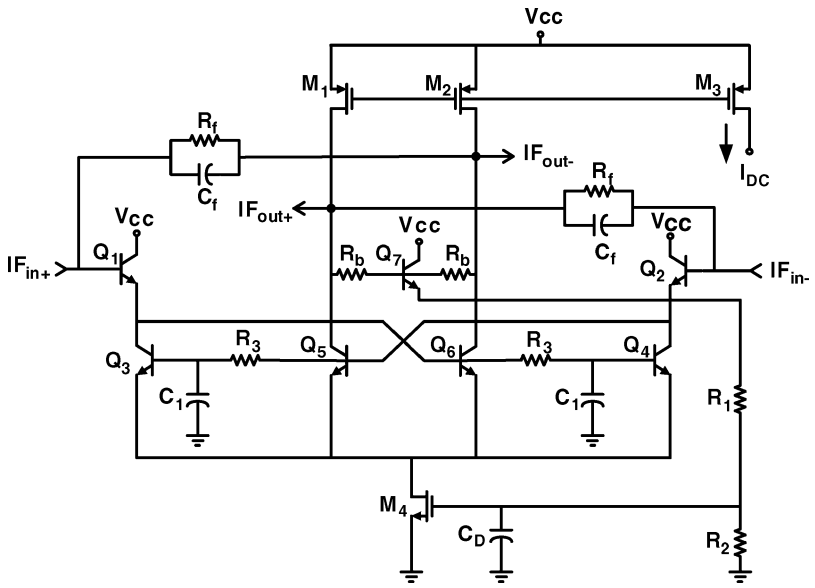


Fig. 6. Schematic of output IF transimpedance amplifier.

at its output. The input impedance of the polyphase filter is set at 200 Ω to minimize loading of the LO buffer. The physical layout of the I/Q path, polyphase filter, and interpolation network is kept as symmetric as possible in order to equalize amplitudes and minimize any mismatch between I and Q local oscillator signals.

D. Transmitter RF Front-End

The circuit schematic diagram of the direct up-conversion transmitter shown in Fig. 8 consists of two parts: a frequency doubler and a transmit amplifier (PA). Transistors Q_1 and Q_2 are biased at cut-off (i.e., Class-B) and form a balanced frequency doubler. Q_1 and Q_2 rectify the 8.6 GHz LO signal (i.e., $f_{RF}/2$), resulting in a strong second harmonic component across the tank $L_{\rm o} - C_{\rm o}$ which is tuned to resonate at 17.2 GHz. Emitter follower Q_4 buffers the signal from the tank to output driver transistor, Q_6.

The final transmit amplifier stage is biased in Class-AB mode in order to realize sufficient linearity and efficiency [28]. Cascode amplifier Q_6/Q_7 produces approximately 0 dBm output power. This satisfies the WSN link budget, while providing sufficient isolation between the antenna and the transmitter so that stability problems caused by on-chip ground bounce are avoided. The AC ground present at the base terminal of common-base transistor (Q_7) provides a low-impedance path for holes generated by impact ionization in the base to flow directly to ground without causing thermal runaway or avalanching of the collector current [29].

The bias circuit for the transmit amplifier is similar to the bias circuit for LNA, shown in Fig. 4(b). Thus, the emitter current of Q_6/Q_7 is also PTAT as the case of LNA to provide constant gm, thus stable gain. On/off keying of the transmitter is realized using nMOS switches (i.e., M_1 to M_3 in Fig. 8) connected in series with the biasing path, which modulate the amplitude of the transmitter output directly.

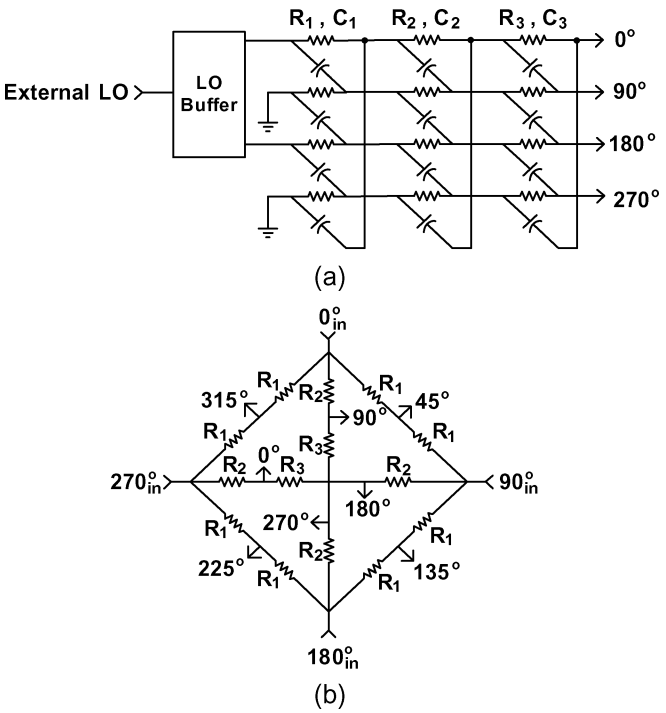


Fig. 7. Schematic of 8-phase LO generator. (a) Polyphase filter generating quadrature LO signals. (b) Interpolation network generating 8-phase LO signals.

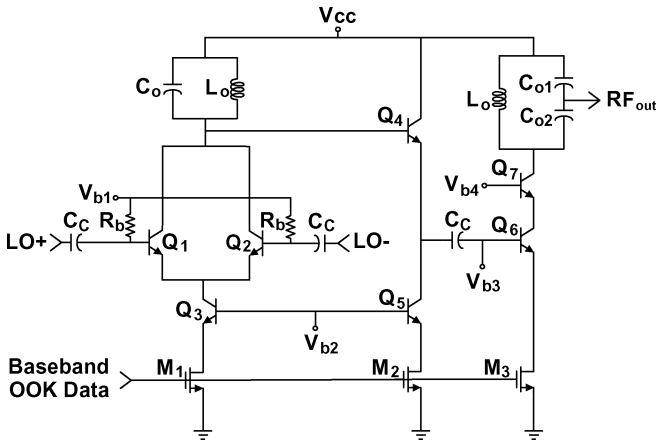


Fig. 8. Schematic of 17 GHz transmitter.

IV. Experimental Results

The receiver and the transmitter prototypes (see Fig. 9) are implemented in NXP-Semiconductors' QUBiC4X SiGe:C BiCMOS technology. The NPN bipolar transistor features a peak f_T of 130 GHz and f_{max} of 140 GHz, which provides sufficient gain margin for RF circuit design at 17 GHz. The breakdown voltages of 2 V $(\mathrm{BV_{CEO}})$ and 6 V $(\mathrm{BV_{CBO}})$ are sufficient for designing circuits operating from a 2.5 V supply voltage. Thanks to low capacitive coupling to the substrate and the 3 μm thick top metal layer, poly-shielded on-chip inductors of less than 500 pH have a Q-factor above 20 at 17 GHz and self-resonant frequency above 100 GHz. In addition, a 5 $\mathrm{fF}/\mu\mathrm{m}^2$ MIM capacitor between the top two metal layers is provided, offering a high specific capacitance combined with low parasitic resistance. The following results were measured

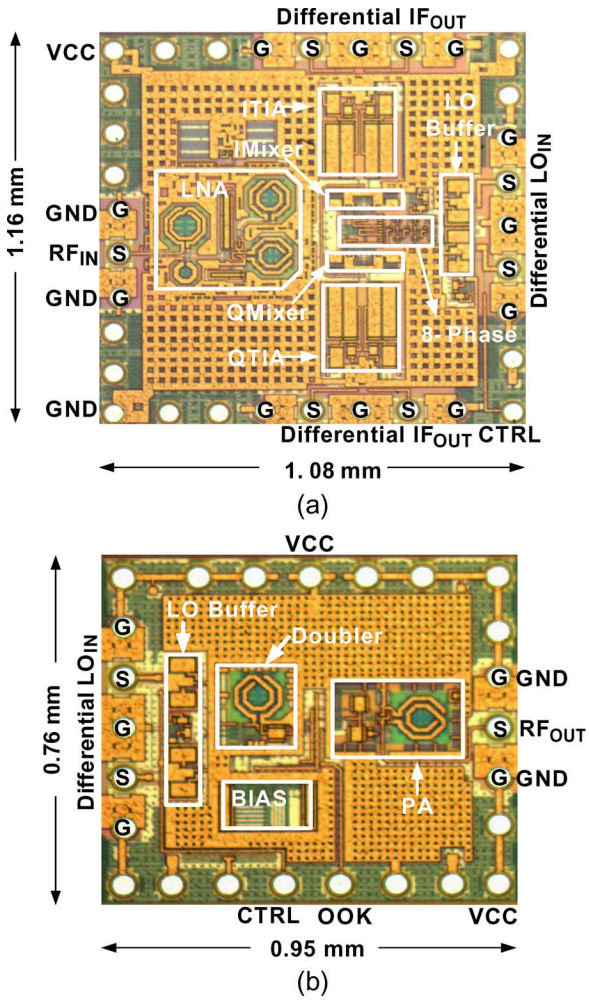


Fig. 9. Photomicrographs of receiver and transmitter. (a) Receiver. (b) Transmitter.

using on-wafer probing and the key performance parameters of the receiver and the transmitter testchips are summarized in Table II and Table III, respectively.

The LNA was characterized stand-alone using a separate test structure. The 2-port S-parameters for the LNA measured from 12 to 18 GHz are shown in Fig. 10. Peak gain (i.e., $|\mathrm{S_{21}}|$) is observed at 15.7 GHz, which is 1.5 GHz below the design value of 17.2 GHz. It is likely that stray coupling between the output tank (L_o and C_o in Fig. 4(a)) and a 300 μm long top metal trace that connects the circuit output to a bondpad causes the change in frequency response. The response of the Rx testchip (i.e., LNA, mixer and IF stage together on the same chip) peaks at 17.2 GHz, as the output connection required by the stand-alone LNA testchip and its associated parasitic effects are not present. The peak $|\mathrm{S_{21}}|$ of the stand-alone LNA is about 12 dB with a minimum noise figure of 3.25 dB at 15.7 GHz, while the gain of the LNA is expected to increases to about 16 dB when it is embedded in the receiver.

The gain of the LNA is insensitive to the supply voltage variation, and can be controlled by the voltage at the gate of MOS transistor M_1 in Fig. 4. When the supply voltage is swept from 2 to 3 V, the LNA power gain only changes from 11.9 to 12.22 dB.

TABLE II
RECEIVER FRONT-END PERFORMANCE COMPARISON

Reference	[15]	[16]	[17]	[18]	This work
Freq., GHz	2.4	0.9	2.4	2.4	17
Technology	0.13 µm CMOS	0.18 µm CMOS	0.13 µm CMOS	0.18 µm CMOS	0.25 µm CMOS
Architecture	Super-Regenerative	Envelope Detection	Direct Conv.	Direct Conv.	Direct Conv.
Area, mm^2	1	1.82	~ 1	2.32	1.25
Data rate, kbit/s	500	1,000	333	100	10,000
NF, dB	-	15	28	10.2	12
Voltage gain, dB	-	17 ~ 45	47	30.5	26.7 into 50 Ω load
Input P_{-1dB}, dBm	-	-	-	-31	-37
IIP_3, dBm	-	-	-21	-	-25
P_{Rx}, mW	2.8	0.5 ~ 2.5	3.4	0.5	17.5
$P_{Rx,ave}$, µW	5.6	0.5 ~ 2.5	10.2	5	1.75

TABLE III
TRANSMITTER FRONT-END PERFORMANCE COMPARISON

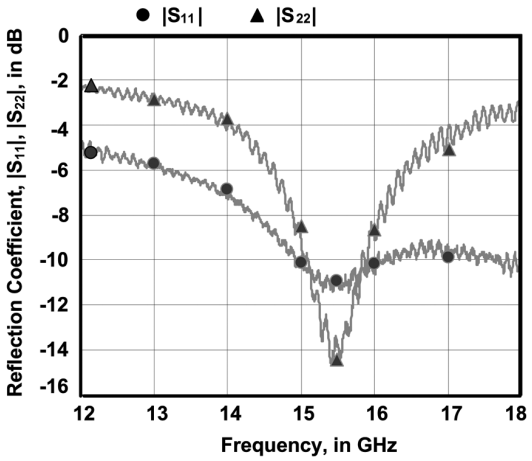
Reference	[2]	[31]	[32]	[33]	This work
Freq.,GHz	0.9	1.9	2.4	2.4	17
Technology	0.25 µm CMOS	0.13 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.25 µm SiGe:C
Modulation	FSK	OOK	QPSK	OQPSK	OOK
Architecture	Direct Conv.	Injection locked	Direct Conv.	Direct Conv.	Direct Conv.
Area, mm^2	~ 0.4	0.4	1.5	>2	0.72
Data rate, kbit/s	100	156	250	250	10,000
P_{rad}, mW	0.25	1	1	1	0.73
P_{Tx}, mW	1.3	1.8	3.6	18	16
$P_{Tx,ave}$, µW	13	11	14.4	72	1.6

The receiver noise figure is measured with an Agilent N8975A noise figure analyzer. The 2.45 dB cable loss and 0.25 dB probe loss at 17 GHz RF input are de-embedded from the measured data (shown in Fig. 11). A NF of ∼12 dB is measured from 10 MHz to 200 MHz, which agrees to within 1 dB with simulation results. The measured conversion gain of the RF chain including the response of the TIA is 26.7 dB at 10 MHz into 50 Ω load (refer to Fig. 11) and a further 9.6 dB increase is expected when loaded by a higher impedance, which agrees well with simulation. The IIP_3 of −25 dBm is obtained from the interpolation of the two-tone test results (see Fig. 12) with RF input power changing from −60 to −30 dBm (RF input signals at 17.01 and 17.012 GHz, respectively). The input-referred 1-dB compression point is −37 dBm from Fig. 12.

Performance of the prototype receiver is summarized in Table II and compared to other circuits reported from the recent literature. To compare receivers operating at different frequencies and data rates, the average receiver power ($P_{\mathrm{Rx,ave}}$)

$$P_{\mathrm{Rx,ave}} = P_{\mathrm{Rx}} \times \frac{\text{Packet size} \times \text{Number of packets/s}}{\text{Data rate}} \quad (4)$$

is used, where P_{Rx} is the power consumption of the receiver. Assuming 1 kbit/packet and 1 packet/s, the resulted $P_{\mathrm{Rx,ave}}$ is 1.75 μW for this work, which is less than one-half of the power consumed by the direct conversion CMOS receivers reported in [17] and [18]. The 200 MHz of spectrum available in the 17 GHz band permits multi-Mbit/s data rates, which enables favorable energy/bit performance despite higher absolute power consumption. Other major receiver benchmarks listed in Table II (e.g., NF, IIP_3, and conversion gain) compare favorably to other implementations reported in the literature to date.



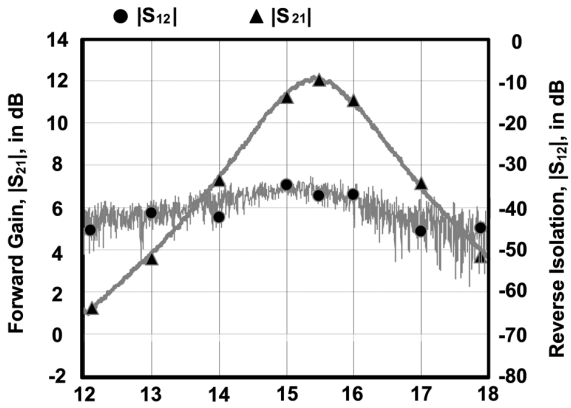


Fig. 10. (a) Measured LNA $|S_{11}|$ and $|S_{22}|$ versus frequency. (b) Measured LNA $|S_{12}|$, $|S_{21}|$ versus frequency.

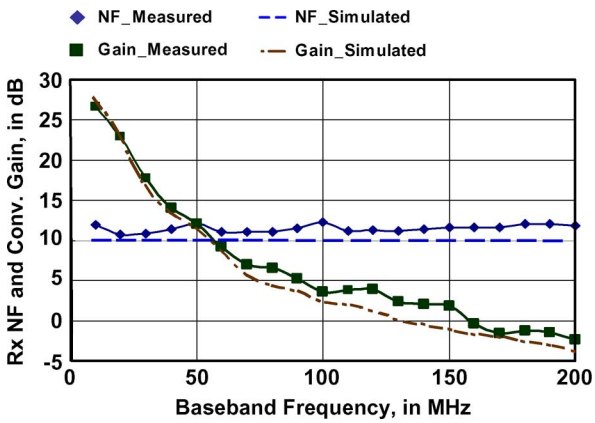


Fig. 11. Measured receiver conversion gain and NF.

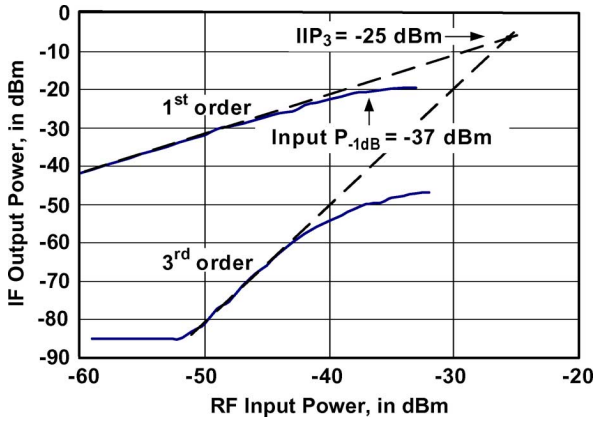


Fig. 12. Measured receiver IIP_3 and input $P_{1\mathrm{dB}}$.

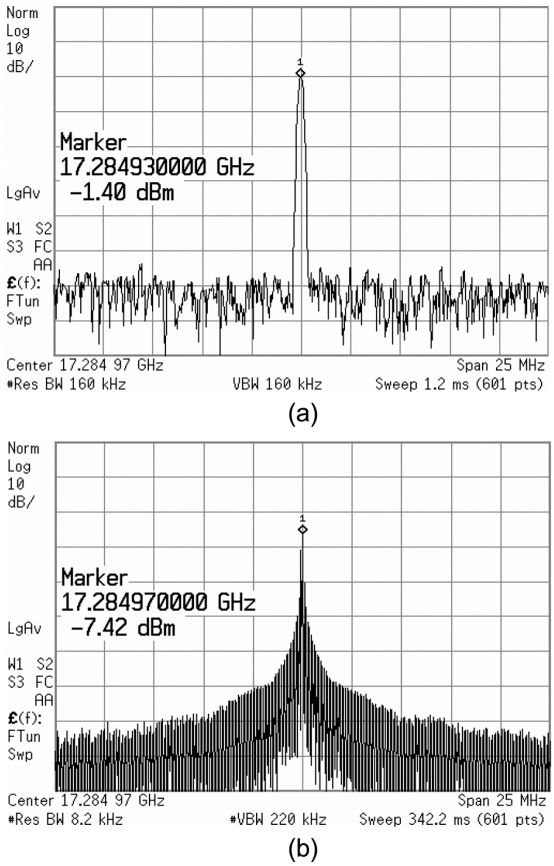


Fig. 13. (a) Measured PA output spectrum without modulation. (b) Measured PA output spectrum with 25 kbit/s OOK modulation.

The transmitter power amplifier (PA) is measured on-wafer operating at a center frequency of 17.285 GHz. The output spectrum at a maximum output power of −1.4 dBm is shown in Fig. 13(a). A non-return-to-zero (NRZ) repetitive data pattern was applied to the OOK input of the PA in order to study the transmit spectrum. Fig. 13(b) shows the output spectrum for a 25 kbit/s OOK modulation, where the spectral spreading and modulation envelope conform to expectations. A plot of the output power versus swept input power showing the PA compression characteristic is presented in Fig. 14. The 1-dB compression point at the output is at −5 dBm after accounting for a cable loss of 2.79 dB in the measurement set-up. The linear power gain of the PA is 7.5 dB.

The detected output signal envelope is identical to the original baseband OOK data applied at the transmitter as shown in Fig. 15. Switching time is on the order of nanoseconds, which is fast enough to support a data rate up to 10 Mbit/s.

The measured performance of the 17 GHz transmitter demonstrator is compared to other low-power implementations gath-

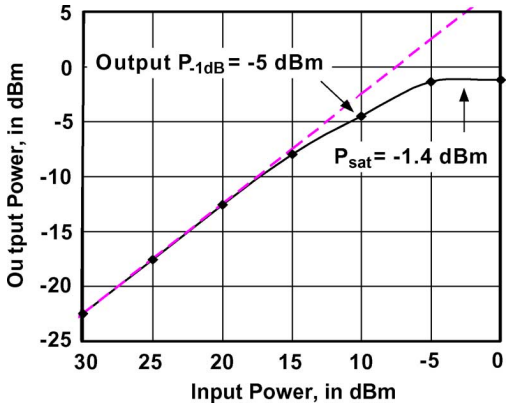


Fig. 14. Measured PA power transfer characteristic at 17.28 GHz.

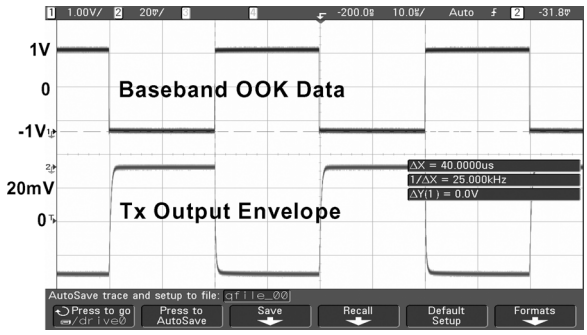


Fig. 15. Tx output signal envelope versus baseband OOK data (time scale in 10 μs/div).

ered from the recent literature in Table III. The average transmitter power consumption $(P_{Tx,ave})$ is defined in a similar way as $P_{\mathrm{Rx,ave}}$ on the receiver side in order to compare transmitters with different operating frequencies and data rates. This work achieves $P_{Tx,ave}$ (1.6 μW), which is less than one-half of the power consumed by the reported direct conversion low-power transmitters for WSNs seen in the literature to date.

Photomicrographs of the receiver (Rx) and transmitter (Tx) testchips are shown in Fig. 9. The Rx testchip has an area of 1.16×1.08 mm^2 and the Tx is 0.95×0.76 mm^2 in size (including bondpads in both cases). The total power consumption measured from a 2.5 V supply is 17.5 mW in receive mode and 16 mW in transmit mode. This corresponds to an energy efficiency of 1.75 nJ for Rx and 1.6 nJ for Tx (not including the LO) at a bit rate of 10 Mbit/s. It is estimated that a total energy efficiency of 2 nJ/bit is achievable in either Rx or Tx modes when the LO generation is fully integrated onto the chip.

A. Future Work

The Rx and Tx will be integrated on the same chip and packaged. An on-chip Tx/Rx switch with at least 20 dB Rx/Tx isolation and about -1 dB insertion loss will result in 1 dB degradation of the Rx noise figure. Packaging parasitics also need to be addressed at the circuit design level. A 24 pin thin, small leadless package (TSLP-24) and flip-chip interconnect shortens the length of the signal paths, thereby reducing signal reflection and losses at 17 GHz due to impedance mismatch [30]. The parasitic inductance of one flip-chip bump can implement the 50 pH degeneration inductor (i.e., L_{E} in Fig. 4) in the LNA.

V. Conclusions

A 17 GHz low-power radio front-end suitable for indoor vision-enabled WSN applications has been presented. Low-power operation is based on the minimization of energy/bit, rather than absolute power consumption of the transceiver. The homodyne architecture with LO running at one-half of the RF center frequency minimizes overall power consumption.

The entire 17 GHz transceiver prototype (excluding baseband) consumes less than 20 mW in full operation, corresponding to an energy consumption of approximately 2 nJ/bit at 10 Mbit/s data rate. The receiver testchip, which consists of LNA, I/Q downconverting mixer and transimpedance IF amplifiers, consumes 17.5 mW in operation, or 1.75 nJ/bit at a receive data rate of 10 Mbit/s. Measured conversion gain and noise figure at 20 MHz IF is 25 dB and 12 dB, respectively. Conversion gain up to 40 dB is expected when the baseband output is loaded by a higher impedance rather than a 50 Ω measurement system. The OOK transmit amplifier employs frequency doubling to generate the 0.73 mW 17 GHz RF carrier and consumes 1.6 nJ/bit when operated at 10 Mbit/s.

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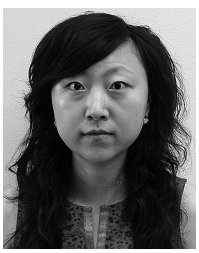

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