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## 23.5 A Sub-1V 810nW Capacitively-Biased BJT-Based Temperature Sensor with an Inaccuracy of $\pm 0.15^\circ\text{C}$ ( $3\sigma$ ) from $-55^\circ\text{C}$ to $125^\circ\text{C}$

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BJT-based temperature sensors are widely used because they can achieve excellent accuracy after 1-point calibration. However, they typically dissipate  $\mu\text{W}$ s of power and require supply voltages above 1V [1]. Although sensors based on DTMOSTs [2,3], capacitively biased (CB) diodes and BJTs [4,5] have demonstrated sub-1V operation, this comes at the expense of accuracy. This paper presents a sub-1V CB BJT-based temperature sensor that achieves a 1-point-trimmed inaccuracy of  $0.15^\circ\text{C}$  ( $3\sigma$ ) from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ , which is  $4\times$  better than the CB BJT state-of-the-art [4]. It also achieves a resolution FoM of  $0.34\text{pJ}\cdot\text{K}^2$ , which is  $6.8\times$  better than that of state-of-the-art BJT-based sensors with a similar accuracy [1,6], (Fig. 23.5.6).

Figure 23.5.1 (left) shows the operating principle of a CB diode. A sampling capacitor  $C_s$  is first charged to the supply voltage and then discharged across the diode. After a short settling time (tens of ns), the residual voltage  $V_D$  on  $C_s$  will be solely determined by the diode's I/V characteristic and will be a supply-independent logarithmic function of time [4,5]. If the discharging time  $t_1$  is fixed, the resulting voltage  $V_{D1}$  will be complementary to absolute temperature (CTAT). A proportional-to-absolute-temperature (PTAT) voltage  $\Delta V_D$  can then be generated by subtracting the output of two CB diodes ( $V_{D1}-V_{D2}$ ) with a fixed discharging-time ratio ( $t_2/t_1$ ). Compared to the current-source biasing used in conventional PTAT generators, capacitive biasing requires very little headroom and enables sub-1V operation even at low temperatures [5].

As shown in Fig. 23.5.1, opening switch  $S_1$  stops the discharge and simultaneously samples  $V_D$  on the capacitor  $C_s$  [4,5]. However, the on-resistance ( $R_{on}$ ) of  $S_1$  increases the settling time required for  $V_D$  to become supply-independent, while the voltage drop across  $R_{on}$  adds a PVT-dependent error to  $V_D$ . Although both effects can be mitigated by using a large switch, its charge injection and leakage will then become significant error sources.

In this work, the discharging time is set by switching the base of a CB PNP (Fig. 23.5.1 bottom right). Compared to switching its emitter [4], this reduces switch current by a factor  $(1+\beta)$ , where  $\beta$  is the BJT's current gain. Furthermore, since the switch is now connected to ground rather than to  $V_{BE}$ , low  $R_{on}$  can be achieved with a small switch, thus mitigating errors due to charge injection and leakage. At the end of the sampling phase, the PNP can be turned off by switching its base to a higher cut-off voltage  $V_B$ .

As in [4], the sampled voltages  $V_{BE}$  and  $\Delta V_{BE}$  generated by CB PNP pairs are applied to a charge-balancing  $\Delta\Sigma$  modulator to obtain a digital representation of temperature. To facilitate sub-1V operation, the modulator's 1<sup>st</sup> integrator is built around an inverter-based pseudo-differential amplifier. The single-ended operation of the integrator is illustrated in Fig. 23.5.2. Initially,  $C_s$  (4pF) is charged to  $V_{DD}$  by turning on  $SW_{1,2}$  (Fig. 23.5.2, top left), while the inverter-based amplifier is auto-zeroed to mitigate its offset and  $1/f$  noise. Next,  $SW_1$  is turned off and  $SW_3$  is turned on, causing  $C_s$  to discharge via the PNP and  $SW_{2,3}$  (Fig. 23.5.2, top right). Then  $SW_{2,3}$  are opened to stop the discharge and sample  $V_{BE}$  on  $C_s$  (Fig. 23.5.2, bottom left). At the sampling moment, the voltage drop across  $SW_3$  due to the PNP's base current is negligibly small, while the PVT-dependent voltage drop across  $SW_2$  does not affect the sampled  $V_{BE}$ . In contrast to [4], an additional switch  $SW_4$  is used to ensure that the voltage drop across  $SW_2$  does not corrupt the sampled offset on the auto-zeroing capacitor  $C_{AZ}$ . Finally,  $SW_{4,6}$  are closed to transfer the sampled  $V_{BE}$  on  $C_s$  to the integration capacitor  $C_{INT}$ , and the base of the PNP is connected to  $V_B$  ( $\sim V_{BE}$ ) to ensure that it is turned off in a supply-independent manner (Fig. 23.5.2, bottom right).  $V_B$  is generated by an auxiliary CB PNP (not shown), which is shared by all CB PNP pairs.

To maximize the sensor's energy efficiency,  $\Delta V_{BE}$  should be maximized, subject to accuracy considerations, by biasing the PNPs at the largest possible current-density ratio (CDR). This is usually done by combining several unit current sources and/or PNPs, which then need complex dynamic-element-matching schemes to mitigate mismatch [1]. In the case of capacitive biasing, however, the PNP current is set by the discharging time, and so the CDR can be accurately defined by using a clock divider to set the discharge-time ratio ( $t_2/t_1$ ) of two CB PNPs [4]. To mitigate charge redistribution errors, the sampling capacitors  $C_s$  (4pF, MIM) are made much larger than the parasitic capacitors of the PNPs and switches (tens of fF). This choice also ensures good matching, low  $kT/C$  noise and mitigates the effect of switch charge injection. A time ratio of 32 ( $t_1=1\mu\text{s}$ ,  $t_2=32\mu\text{s}$ ) is chosen to achieve a good balance between energy-efficiency and accuracy.

The block diagram of the sensor is shown in Fig. 23.5.3. It consists of 3 pairs of CB PNPs, which are connected to a 1-bit 2<sup>nd</sup>-order  $\Delta\Sigma$  modulator. By controlling the timing of each CB pair (Fig. 23.5.3 bottom left), differential charges proportional to either  $V_{BE}$  or  $\Delta V_{BE}$  can be transferred to the 1<sup>st</sup> integrator. When the output bitstream (BS) is 0, all

the CB pairs are configured to transfer a charge proportional to  $3\Delta V_{BE}$ , while when the BS is 1, one of them is configured to generate  $-V_{BE2}$ , thus transferring a charge proportional to  $2\Delta V_{BE}-V_{BE2}$ . CB-pair mismatch is mitigated by rotating the pair used to generate  $-V_{BE2}$ . The resulting BS average  $\mu$  is then  $3\Delta V_{BE}/V_{BE1}$ , which varies from about 0.2 to 0.9 over the military temperature range ( $-55^\circ\text{C}$  to  $125^\circ\text{C}$ ). Compared to [4], where  $\Delta V_{BE}/V_{BE1}$  is digitized, the proposed charge-balancing scheme makes better use of the ADC's dynamic range, reducing the input-referred quantization error and offset by  $3\times$ . Although  $\mu$  is a non-linear function of temperature, it can be linearized by computing  $\mu_{lin}=\alpha\cdot\mu/((\alpha+\alpha_{trim})\cdot\mu+3)$ , where  $\alpha$  is a digital constant and  $\alpha_{trim}$  implements a PTAT trim that corrects the spread of  $V_{BE1}$ .

One half of the auto-zeroed inverter-based amplifier used in the 1<sup>st</sup> integrator is shown in (Fig. 23.5.3 bottom right). During the auto-zero phase, its bias current (160nA) is set by a constant-gm bias generator via an NMOS current mirror, and the gate voltages of  $M_{N1}$  and  $M_{P1}$  are stored on capacitors  $C_{AZN,P}$  ( $\sim 17\text{pF}$ ), respectively. These capacitors are sized such that the integrator's input noise is dominated by the  $kT/C$  noise of the CB pairs. During the integration phase, the cascode transistors  $M_{P2}$  and  $M_{N2}$  ensure high DC gain ( $\sim 80\text{dB}$ ). Compared to the inverter-based amplifier in [4], this simplified biasing scheme reduces the amplifier's minimum supply voltage from  $2V_{GS}+V_{DSAT}$  to  $V_{GS}+2V_{DSAT}$ , thus enabling sub-1V operation with normal VT transistors. The 2<sup>nd</sup> integrator uses a scaled version of this amplifier and draws only 40nA.

To prevent CDR errors, and hence  $\Delta V_{BE}$  errors, the leakage current of the associated switches at high temperatures should be minimized. To achieve both low leakage and low  $R_{on}$  with a sub-1V supply,  $SW_{3,6}$  are implemented with HVT NMOS transistors driven by clock boosters [4]. To mitigate PNP mismatch and the residual offset of the modulator, system-level low-frequency chopping (CHL) is applied. Since the output voltage of the CB pairs is set by clock timing, the input chopper is implemented by simply swapping the appropriate timing signals in the digital domain, thereby avoiding the need for extra analog switches.

The sensor was fabricated in a standard  $0.18\mu\text{m}$  CMOS process and occupies  $0.25\text{mm}^2$  (Fig. 23.5.7). It consumes 810nW (620nW analog, 190nW digital) from a 0.95V supply at room temperature, which increases to  $2\mu\text{W}$  at  $125^\circ\text{C}$  due to the PTAT bias current and leakage (Fig. 23.5.4 top left). All the required timing signals are generated on-chip from a 1MHz external clock. The sinc<sup>2</sup> decimation filter and the linearization of  $\mu$  were implemented off-chip. Circuit-level simulations show that their on-chip implementation would only dissipate an additional 80nW.

As shown in Fig. 23.5.5 (left), the output of 20 chips in ceramic DIL packages was characterized from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . As expected, their BS average  $\mu$  is a non-linear function of temperature. After linearization with a fixed  $\alpha$  ( $\approx 7.3$ ), the sensor achieves a batch-calibrated inaccuracy of  $\pm 0.45^\circ\text{C}$  ( $3\sigma$ ). This improves to  $\pm 0.15^\circ\text{C}$  ( $3\sigma$ ) after a 1-point PTAT trim, corresponding to a relative inaccuracy (RIA) of 0.17% (Fig. 23.5.5, right). Over a 0.95V to 1.4V supply range, the sensor achieves a maximum power-supply sensitivity (PSS) of  $0.2^\circ\text{C}/\text{V}$  from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  (Fig. 23.5.4 top right).

Figure 23.5.4 (bottom left) shows the FFTs of the sensor's bitstream at different temperatures, with the modulator operating in free-running mode. In a conversion time of 128ms, it achieves a  $kT/C$ -limited resolution of  $1.8\text{mK}_{\text{rms}}$  at room temperature, and less than  $2.1\text{mK}_{\text{rms}}$  over temperature (bottom right). This corresponds to a resolution FoM of  $0.34\text{pJ}\cdot\text{K}^2$  at room temperature, and less than  $0.53\text{pJ}\cdot\text{K}^2$  over temperature, making it one of the most energy-efficient BJT-based sensors reported to date.

The sensor's performance is summarized in Fig. 23.5.6 and compared to state-of-the-art BJT-based temperature sensors with similar accuracy and/or power consumption. This is the only sub-1V precision temperature sensor (RIA  $<0.2\%$ ) among the sensors listed in the table. Compared to other CB sensors [3,4,5], it achieves the best accuracy ( $\times 4$ ) and PSS ( $\times 1.3$ ). Compared to conventional designs with fixed-current biasing [1,2,6], this work achieves sub-1V operation, similar accuracy, and state-of-the-art energy efficiency ( $\times 6.8$ ).

### Acknowledgement:

We would like to thank Pieter Harpe for technical discussions and Zu-yao Chang, Lukasz Pakula for measurement support.

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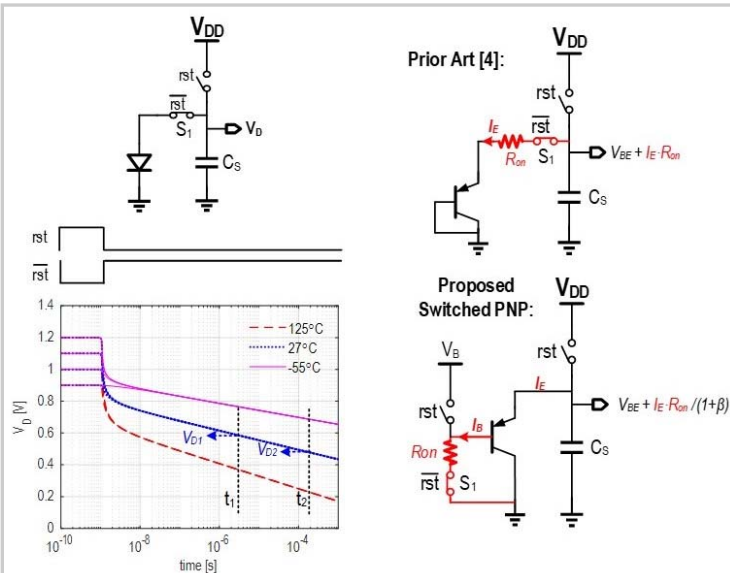


Figure 23.5.1: Working principle of the capacitively-biased diode (left); comparison of the prior art in [4] and the proposed base-switching PNP (right).

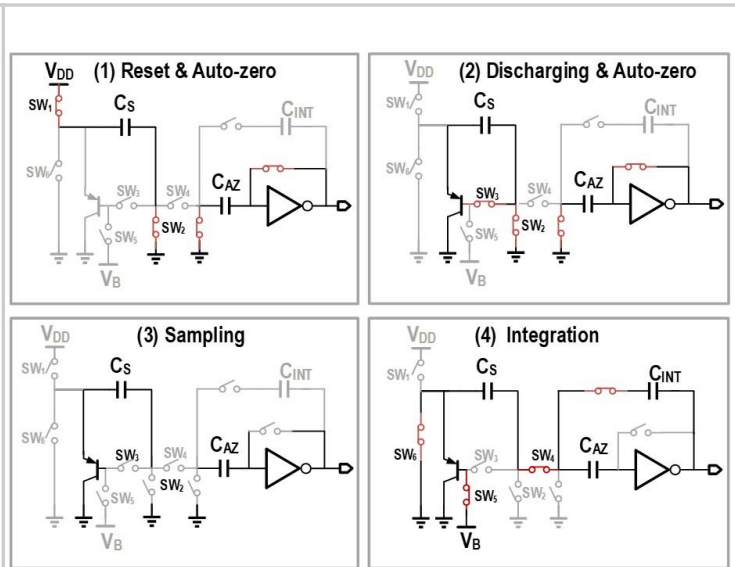


Figure 23.5.2: SC integrator with embedded CB PNP and its operating phases.

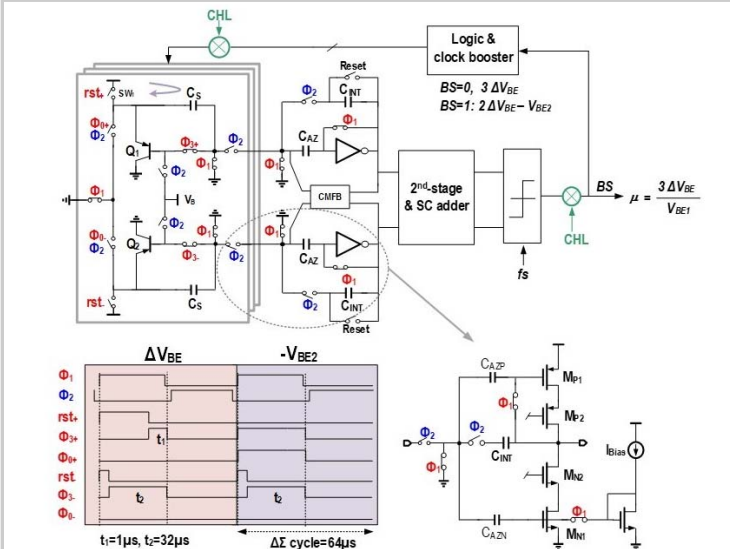


Figure 23.5.3: Simplified diagram of the proposed CB-PNP-based temperature sensor (top) and its timing diagram (bottom left); proposed AZ inverter-based amplifier (bottom right).

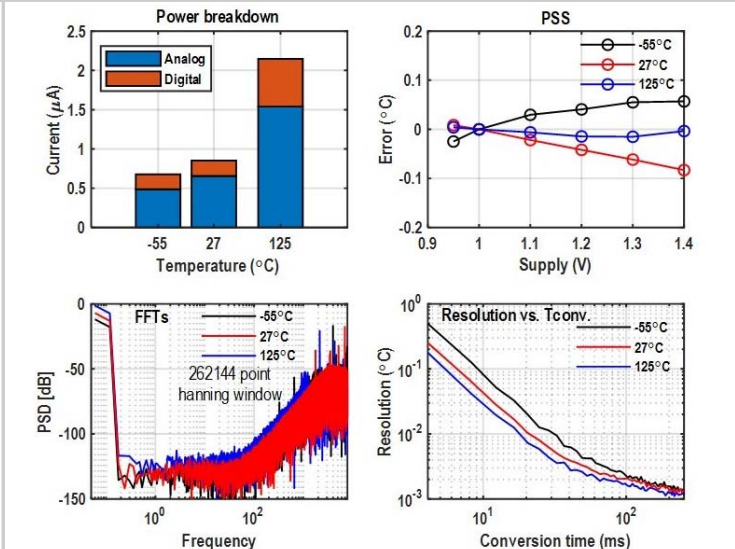


Figure 23.5.4: Supply current over temperature (top left); PSS over temperature (top right). FFTs of the bitstream in free-running mode (bottom left); resolution vs. conversion time (bottom right) over temperature.

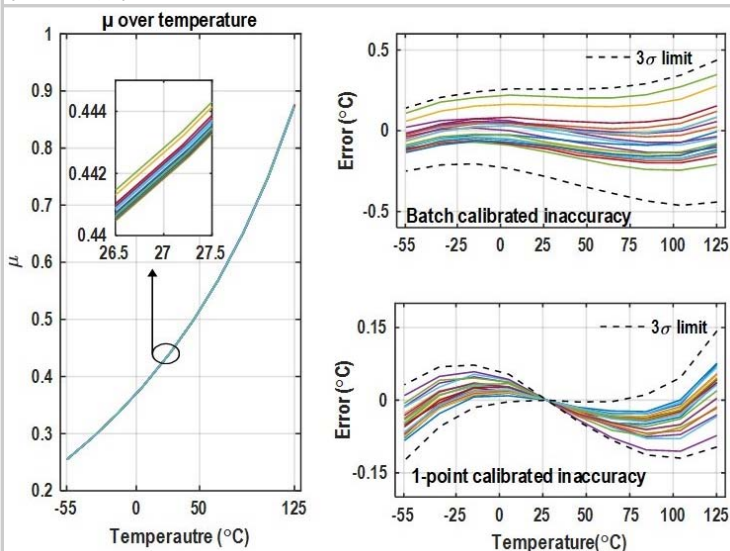


Figure 23.5.5: Measured bitstream average  $\mu$  of 20 chips over temperature (left); inaccuracy after batch calibration (top right) and 1-point PTAT calibration (bottom right).

|                                     | Capacitive biasing |                    |                   |               | Current-source biasing |                       |                    |
|-------------------------------------|--------------------|--------------------|-------------------|---------------|------------------------|-----------------------|--------------------|
|                                     | This work          | SSCL'21 [4]        | SSCL'19 [5]       | CICC'20 [3]   | JSSC'17 [1]            | ISSCC'14 [2]          | VLSI'22 [6]        |
| Technology                          | 180nm              | 55nm               | 16nm              | 28nm          | 160nm                  | 160nm                 | 180nm BCD          |
| Type                                | PNP<br>DT $\Delta$ | PNP<br>DT $\Delta$ | Bulk Diode<br>SAR | DTMOST<br>OSC | PNP<br>DT $\Delta$     | DTMOST<br>DT $\Delta$ | NPN<br>DT $\Delta$ |
| Area [mm <sup>2</sup> ]             | 0.25               | 0.021              | 0.0025            | 0.017         | 0.16                   | 0.085                 | 0.058              |
| Supply [V]                          | 0.95-1.4           | 1-1.3              | 0.85-1            | 0.85-1.15     | 1.5-2                  | 0.85-1.2              | 1.25               |
| T. Range [°C]                       | -55 to 125         | -55 to 125         | -15 to 105        | -10 to 90     | -55 to 125             | -40 to 125            | -15 to 85          |
| 3 $\sigma$ error [°C]               | $\pm 0.45$ (0)     | $\pm 1.4$ (0)      | $+1.5$ -2.0 (0)   | $\pm 2.0$ (0) | $\pm 0.4$ (0)          | $\pm 1$ (0)           | $\pm 0.4$ (0)      |
| (Trim point)                        | $\pm 0.15$ (1)     | $\pm 0.6^*$ (1)    |                   | $\pm 0.9$ (1) | $\pm 0.06^*$ (1)       | $\pm 0.4$ (1)         | $\pm 0.15$ (1)     |
| R.IA[%]                             | 0.5 (0)            | 1.6 (0)            | 2.9 (0)           | 4 (0)         | 0.44 (0)               | 1.3 (0)               | 0.8 (0)            |
| (Trim point)                        | 0.17 (1)           | 0.67 (1)           |                   | 1.8 (1)       | 0.07 (1)               | 0.5 (1)               | 0.3 (1)            |
| Power [ $\mu$ W]                    | 0.81               | 2.2                | 18                | 33.75         | 6.9                    | 0.6                   | 0.21               |
| Tconv [ms]                          | 128                | 6.4                | 0.013             | 0.1           | 5                      | 6                     | 50                 |
| Res. [mK]                           | 1.8                | 15                 | 300               | 10.2          | 15                     | 63                    | 15                 |
| PSS[°C/V]                           | 0.2                | 3.7                | 1.5               | 0.27          | 0.01                   | 0.45                  | 0.07               |
| Res. FoM**<br>[pJ·K <sup>-2</sup> ] | 0.34               | 3.1                | 21                | 0.36***       | 7.8                    | 14.1                  | 2.3                |

\*With systematic error correction. \*\* Res. FoM=(Energy/conversion)\*(Resolution)<sup>2</sup> \*\*\* Needs an additional frequency to digital converter

Figure 23.5.6: Performance summary and comparison with the state-of-the-art.

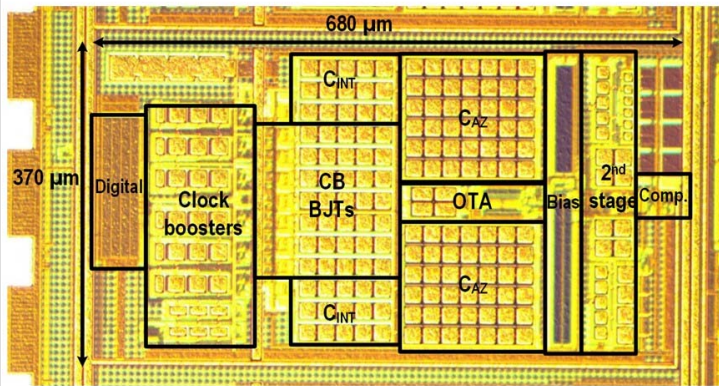


Figure 23.5.7: Die micrograph.