The design of a 16*16 pixels CMOS image sensor with 0.5 e^-_{RMS} noise

Master of Science Thesis

Qiang Yao (4186176)

June 2013

Faculty of Electrical Engineering, Mathematics and Computer Science

Delft University of Technology

The project of this thesis was in cooperation with Caeleste CVBA.
Their support and assistance are hereby gratefully acknowledged.

The design of a 16*16 pixels CMOS image sensor with 0.5 e^-_{RMS} noise

Qiang Yao (4186176)

Supervisor: prof. dr. ir. Albert J.P. Theuwissen

In Partial Fulfillment of the Requirements

For the Degree of Master of Science in Electrical Engineering at Delft University of Technology

June 2013

Faculty of Electrical Engineering, Mathematics and Computer Science

Delft University of Technology

Abstract

Low noise image sensors can see images by just a few photons have a wide application in both the scientific and economic fields.

This thesis presents a design of a 16*16 pixels CMOS image sensor with a target noise level in the order of 0.5 electrons RMS in 0.18μm technology, which has a potential to catch a large amount of low light imaging market.

First the novel 5T pinned photodiode low noise pixel is shown as well as the method cycling pMOS transistor well voltage between accumulation and inversion to shape the spectrum of flicker noise like white noise and to be decreased by oversampling.

Then the readout circuitry with the sigma-delta ADCs and bidirectional digital counters are described. Correlated double sampling and oversampling technology are executed to decrease the quantization noise and thermal noise.

At last, the system simulation, noise simulation results are given as well as the PCB test system.

Keywords: low noise, CMOS image sensor, sigma-delta ADC, digital counter

Table of Contents

List of Figures

List of Tables

Acknowledgements

I would like to extend my deeply gratitude to all those, who have helped me during my thesis work. Without their support and assistance, I could not have reached present stage.

First of all, I would like to express my sincere gratitude to Prof. Albert Theuwissen, my supervisor at TU Delft, for his instructive guidance and responsible supervision of my thesis research. He has helped me in every step of the thesis writing, thanks for his inspiring advices and valuable suggestions.

High tribute shall be paid to Prof. Bart Dierickx, my daily supervisor at Caeleste, for his constant encouragement and guidance through my research work. Without his illuminating instructions, this thesis could not have reached present form. And special thanks for his trust on my research ability.

I would also like to express my heartfelt thanks to my colleagues at Caelsete: Patrick Henckes, Benoit Dupont, Arnaud Defernez, Peng Gao, Dirk Uwaerts and so on, who are tutors in my research and friends in my life.

I am deeply indebted to all the other tutors and teachers at TU Delft for their patient education during my two-year study.

Finally, I would like to express my gratitude to my beloved parents who have always been supporting and understanding me.

Chapter 1 Introduction

Noise is a major specification item in all image sensors. Low noise is needed to have the capability to see an image based on just a few photons. This is fueled by a large amount of applications in the scientific domain and industrial vision markets. This thesis design work is a research effort to improve on a previous single-pixel 0.5 noise electrons RMS [1.1] endeavor by Caeleste CVBA. We create a small (16*16 pixels), but complete image sensor with a presumable noise level in the order of 0.5 electrons RMS. The device has several first-offs, as a novel way of oversampling with a sigma-delta ADC, correlated double sampling and other methods to decrease the noise.

At the start of this introductory chapter, the motivation of this work is briefly discussed. Then a short introduction of state of the art low noise image sensors follows, as well as the analysis of their advantages and drawbacks. Furthermore, a concise description of this thesis work is performed. Finally, the organization of the thesis is presented.

1.1 Motivation

Low noise is synonymous with more sensitivity and higher dynamic range and is mandatory in very low light imaging. Low noise image sensors have a wide application not only in the scientific domain, but also in the economic field.

In the scientific domain, there is a strong need for low noise image sensors in medical, industrial and astronomical applications. E.g. fluorescence imaging technology, the technique used for the realization of minimally invasive spatiotemporal mapping of function and structure of cellular and neural systems [1.2]; industrial machining and wind tunnel aerodynamic research with high speed imaging technology; quests for the origins of the universe research with high definition astronomical telescopes, all require the lowest possible noise level.

In the Business-to-Consumer markets, consumers' demand for a low noise high-end camera goes on for decades. Professional and semi-professional photography, night photography, high speed sport photography and cinematography are huge global markets.

1.2 State of the art low light image sensors

State of the art low light image sensors based on integration mode hit the fundamental limits of the transistors noise due to the 1/f noise of the source follower. Inherent pixel noise

sources such as kTC noise are typically cancelled by CDS circuitry, but state of the art integration pixels have the noise levels in the range of 1 to 2 electrons RMS, which does not satisfy nowadays scientific and industrial demands. Going further in noise reduction demands a technological breakthrough.

Amongst competitive methods aiming at the same goal, one can name Electron Multiplying CCD (EMCCD) and Avalanche Photodiode circuits (APD).

When using the EMCCD technology, before the signals are read out, the signal electrons are gradually multiplied in an output CCD section with high electric fields between the CCD stages, which can rapidly decrease the readout noise to sub-electron order [1.3] [1.4] [1.5]. However the EMCCD requires a high operation voltage (around 50V), which makes it complex and expensive to integrate and very few foundries can produce it. Moreover, EMCCD ages over time, and has excess Fano noise; its SNR (signal-to-noise ratio) is inferior when not in the dark. Because of the drawbacks mentioned above, the EMCCD is only applied in a limited scientific field, where price and complexity play a smaller role.

The APD (Avalanche Photodiode) / SPAD (Single Photon Avalanche Diode) is a photodiode biased beyond its breakdown voltage, and this breakdown will only happen triggered by the absorption of a photon. This breakdown can be used in photon counting [1.3]. An APD requires an operation voltage above 20V, which makes it complex to get an image out of it. What's more, its low fill factor and high dark current make it unsuitable for classic imaging applications, which require high fill factor and long integration time.

1.3 This thesis work

In this thesis work, we use a relatively standard CMOS process, 4.0V analog and 3.3V digital power supplies, 5T pixel structure.

The pixel structure has 4 nMOSFETs and 1 pMOSFET. The pMOSFET is cycled between accumulation and inversion, and we sample the pixel output signal during inversion once per cycle. The cycling reduces the 1/f noise's correlation time to less than cycling period; makes its noise spectrum in the low frequency region like white noise. And this white noise could be reduced by oversampling subsequently [1.1].

In the readout circuitry, we design column-level sigma-delta ADCs oversampling the pixel output signals to decrease the general noise, and digital counters to realize the output digitization.

Table 1-1 lists state of the art integration pixel performances comparing with measured demonstrators at Caeleste and this thesis work.

Table 1-1 State of the art pixel performances versus Caeleste's demonstrators and this work

	Technology	Noise level in e^- (RMS)
Commercial available	CCD (non EMCCD)	<2
	CMOS	<1.5
R&D (Caeleste)	Single-pixel	<0.5
	This work	<0.5 presumably

This design has a bit complex driving request, and its pixel contains a pMOSFET, which decreases the fill factor of the pixel a little. But considering its good low noise performance, it has the potential to catch a large amount of low light imaging market.

1.4 Organization

The thesis presents the basic mechanism and circuit realization of a CMOS image sensor with the target of 0.5 noise electrons RMS, which is proper for low light imaging application. Besides the introductory chapter, the following parts of the thesis are arranged in four chapters.

Chapter 2 briefly discusses the noise principles in a CMOS image sensor, as well as the pixel and readout circuitry structures. Chapter 3 gives a comprehensive analysis of the circuitry implementation of the whole system as well as the operations of different architectures. In chapter 4, the details of the schematic simulations and noise simulations are shown, as well as the PCB test system design. Chapter 5 contains a conclusion of the thesis and a discussion of the future research.

1.5 References

[1.1] Dierickx, B.; Ahmed, N. and Dupont, B., "A 0.5 noise electrons RMS CMOS pixel," Caeleste's scientific publication, www.caeleste.be, Dec. 2011.

[1.2] Murari, K.; Etienne-Cummings, R.; Thakor, N.V.; Cauwenberghs, G., "A CMOS In-Pixel CTIA High-Sensitivity Fluorescence Imager," Biomedical Circuits and Systems," IEEE Transactions on , vol.5, no.5, pp.449,458, Oct. 2011.

[1.3] Compiled by Dierickx, B., "The Image Sensor Lexicon ©," www.caeleste.be, Jul. 2010.

[1.4] Yang Shaohua; Guo Ming'an; Li Binkang; Xia Jingtao; Wang Qunshu; Sun Fengrong, "Design of High Resolution High Sensitivity EMCCD Camera," Intelligent System Design and Engineering Application (ISDEA), 2012 Second International Conference on , pp.1212,1216, Jan. 2012.

[1.5] "Electron-multiplying CCD", http://en.wikipedia.org/wiki/Charge-coupled_device#Electron-multiplying_CCD, Apr. 2013.

Chapter 2 Background

As noise is a very critical specification in low noise image sensors, firstly a concise discussion about noise principles in CMOS image sensors will be presented in section 2.1. And then in section 2.2, an overview of the CMOS pixel architectures will be shown. At last, the readout circuitry structures of image sensors will be explained in section 2.3.

2.1 Noise principles in image sensors

Electronic noise is a time domain random fluctuation of an electrical signal [2.1]. As for image sensors, noise can be defined as the difference between theoretical pixel signal and experiment measured pixel signal.

There are many different kinds of noise sources in image sensors. Whether the noise changes over time or in space, they can be classified into two sorts: temporal noise and spatial noise.

Temporal noise, which varies over time, includes kTC noise, 1/f noise, RTS noise, photon shot noise, dark current shot noise, power supply noise, substrate noise, ADC quantization noise, etc. [2.2].

Spatial noise, which is stable over time, but varies over different pixels within a imager, includes dark fixed pattern noise, light fixed pattern noise, column fixed pattern noise, row fixed pattern noise, dark signal non-uniformity, photo response non-uniformity, defect pixels, dead and hot pixels, etc. [2.2].

At pixel level, the most important noise sources are thermal noise and flicker noise (1/f noise) in MOS transistors. So we focus on these two noise sources firstly.

2.1.1 Thermal noise

Thermal noise in an MOSFET can be modeled by a current source between the drain and source terminals with a spectral density [2.3]:

$$\overline{I_n^2}=4kT\gamma g_m \tag{2-1}$$

where I_n is the noise current in amplitude spectral density, k is the Boltzmann constant, T is the absolute temperature in Kelvin, g_m is the transconductance of the MOSFET, γ is a coefficient derived to be equal to 2/3 for long-channel transistors in saturation region, and maybe larger for submicron MOSFET [2.3].

Thermal noise in the pixel can be reduced or almost cancelled by correlated double sampling (CDS), oversampling, reducing the operation temperature, decreasing the circuit bandwidth, increasing the MOSFET drain current I_D to increase g_m.

2.1.2 Flicker noise

Flicker noise is thought to be generated by the random capture and emission of charge by the trapping centers at the interface between the gate oxide and the underlying silicon [2.4]. The flicker noise spectral density is typically modeled as a voltage source in series with the MOSFET gate and roughly given by [2.3]:

$$\overline{V_n^2}=\frac{K}{C_{ox}*W*L}*\frac{1}{f}\ [V^2/Hz] \tag{2-2}$$

where V_n is the noise voltage in amplitude spectral density, K is a technology and MOS transistor type specific coefficient, on the order of $10^{-25}V^2F$, C_{ox} is the oxide capacitance per unit area of the MOS transistor, W and L are the width and length of the MOS transistor, f is the frequency. At a determined bandwidth, the integrated noise can be calculated like this:

$$V_{RMS}=\sqrt{\int_{f_{low}}^{f_{high}}\overline{V_n^2}*df}\approx\sqrt{\frac{K}{C_{ox}*W*L}*\ln(f_{high}/f_{low})} \tag{2-3}$$

where V_{RMS} is the root mean square integrated noise voltage, f_{high} and f_{low} are the highest and lowest frequencies of the frequency band. If the technology node, type and size of the MOSFET are determinate, the coefficient $\frac{K}{C_{ox}*W*L}$ could be treated as a constant, the variation of V_{RMS} is only influenced by $\sqrt{\ln(f_{high}/f_{low})}$. Because of its math characteristic, the variation of $\sqrt{\ln(f_{high}/f_{low})}$ is limited. Using technologies such as low pass filtering, high pass filtering, correlated double sampling (CDS) can only decrease V_{RMS} by a factor of 3 to 5.

Other design methods used to reduce the flicker noise are: using large size devices (large W and L); using pMOSFETs instead of nMOSFETs, because pMOSFETs' K constants are smaller; using buried channel MOSFETs instead of surface channel MOSFETs, which keeps the carriers at some distance from the oxide-silicon interface [2.3].

2.1.3 Photon shot noise

Besides the two significant noise sources mentioned above, we also need to pay attention to a hard physics fundamental noise, which cannot be avoided in image sensors: photon shot noise. When the photodiode is exposed to light for a period of time, photons reach the photodiode

sensing region and generate electron-hole pairs. The number of photons is statistical and can be described by Poisson statistics [2.2]. The photon shot noise obeys the formula:

$$Q_{noise}/q=\sqrt{Q_{signal}/q} \tag{2-4}$$

where Q_{noise} is the noise charge, Q_{signal} is the signal charge, q is the unit charge.

If we ignore other noise sources, the SNR (signal-to-noise ratio) of a photon-shot-noise-limited image sensor is:

$$SNR=\frac{Q_{signal}/q}{Q_{noise}/q}=\sqrt{Q_{signal}/q} \tag{2-5}$$

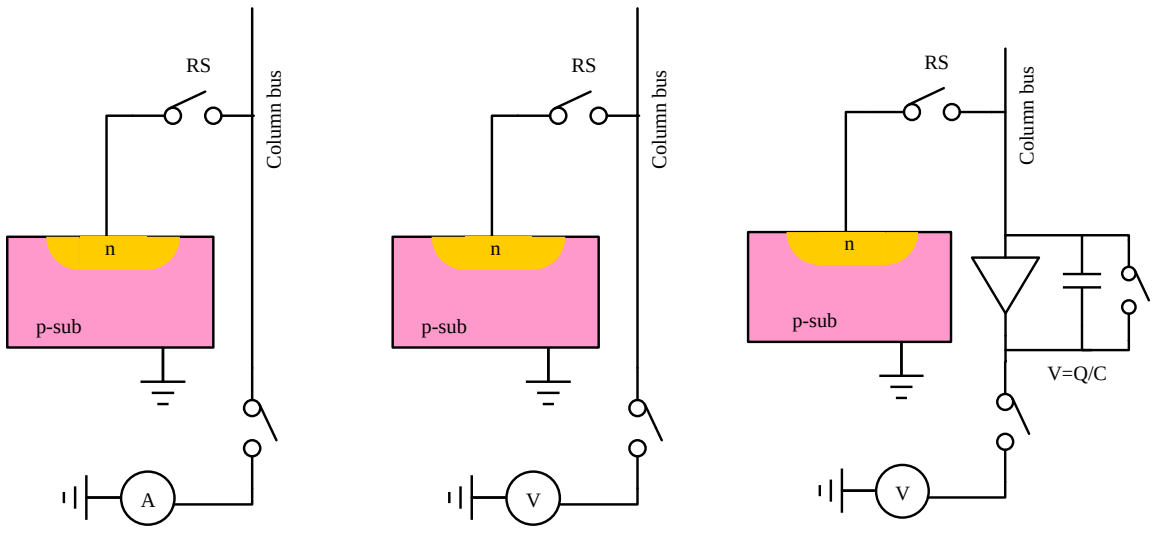
This formula leads to a rule of thumb: a minimum signal-to-noise ratio of 40 dB or more is needed for consumer image sensors, translated into 10,000 electrons per pixel [2.2].

Because there is no method to decrease the photon shot noise, all we can increase the SNR by reaching a fill factor and quantum efficiency as high as possible.

2.2 Overview of pixel structures

2.2.1 Passive pixel

In 1960s, Weckler & Noble tried to use diodes and switches to make equivalents of the Vidicon tubes and created the so-called passive pixel. In Figure 2.1, passive pixel structures with three operation methods are shown.



(a) (b) (c)

Figure 2.1 Passive pixel structures with three operation methods

Figure 2.1(a) shows a passive pixel with a galvanometer. When the readout switch (RS) is closed, the galvanometer measures the instantaneous current generated by the photodiode. However, an instantaneous current measurement is not accurate, and the galvanometer is difficult to realize in the integrated circuitry. Figure 2.1(b) presents a passive pixel with a voltmeter. Unfortunately, the large parasitic capacitor on the column bus submerges the photodiode signal easily. Figure 2.1(c) shows a pixel with an external integrator. The operation principle is like this: first, we reset the integrator to clear the previous signal, then close the readout switch (RS) and let the charge of the photodiode integrate on the integrator capacitor. Subsequently, the voltage of the integrator capacitor is read out. The quality of the image is poor; the reasons are the large kTC noise generated by the parasitic capacitor on the column bus and the parasitic light sensitivity of the switches.

2.2.2 Active pixel

Two decades after the passive pixel structure was invented, the active pixel emerged, which applied an amplifier inside the pixel structure. The three MOSFETs (3T) active pixel contains a photodiode, a reset switch (RST), an nMOSFET source-follower and a readout switch (RS), which is shown in Figure 2.2. The operation of the active pixel is like this: first, we reset the photodiode by the reset switch, and then expose the photodiode to light, at last read out the signal after the source-follower.

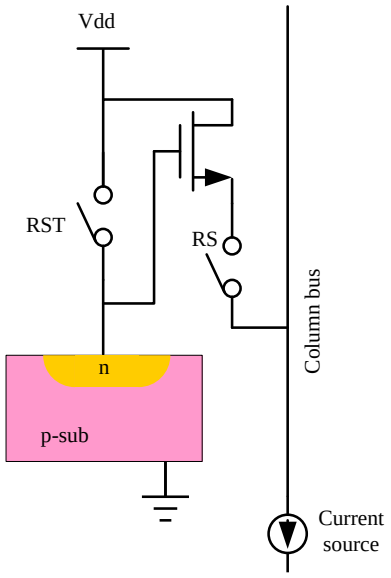


Figure 2.2 The active pixel structure

Thanks to the source-follower, the influence of parasitic capacitor is decreased. But the kTC noise generated by resetting the photodiode still remains, and a lower fill factor and a pixel-to-pixel mismatch are apparent.

2.2.3 Pinned photodiode pixel

To cancel the kTC noise of resetting the photodiode, the pinned photodiode pixel technology was introduced. A four MOSFETs (4T) pinned photodiode pixel structure is shown in Figure 2.3 [2.5]. A pinned photodiode is a fully depleted buried diode, whose n region is fully depleted. It has a lower dark current, because the extra p^+ shallow implanted layer on the top shields the diode from the Si/SiO2 interface.

From Figure 2.3, we find that comparing with the 3T active pixel, the 4T pinned photodiode pixel has an extra transfer gate. Its operation principle is described like this: firstly, the transfer gate is off; we close the reset switch (RST) to remove the signal from the last cycle; after reset, we measure the signal from FD (floating diffusion node), as S_{reset}; and then the charge generated by photoelectric effect is stored in the pinned photodiode; then we close the transfer gate, the charge transfers from photodiode to FD; after transfer, we measure the signal on FD again, and name it $S_{transfer}$. At last, we calculate $S_{transfer}$- S_{reset} as the pixel signal, which is the so-called correlated double sampling (CDS). Through CDS, we can compensate for the kTC noise of the reset operation almost completely.

Moreover, the pinned photodiode is fully depleted; when the transfer gate closes, all the charge on the pinned photodiode will move to FD rapidly, leaving the pinned photodiode empty. Therefore, there is no kTC noise in the pinned photodiode [2.2].

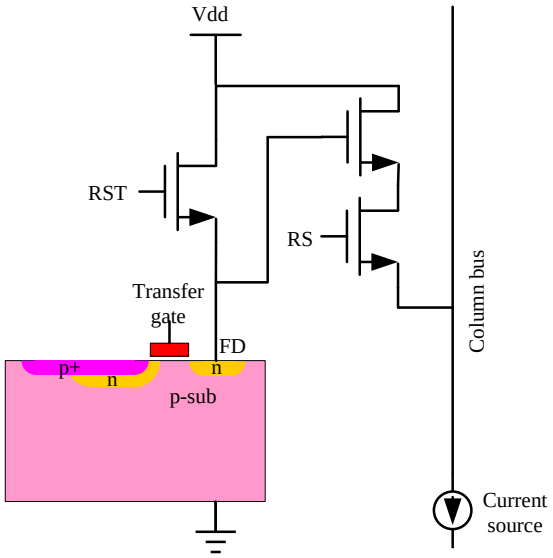


Figure 2.3 The 4T pinned photodiode pixel structure

With the obvious advantages mentioned above, the pinned photodiode technology is widely used in image sensor design. And in this thesis work, the pinned photodiode technology is adopted with several novel modifications, which will be introduced in the next chapter.

Comparing with the 3T passive pixel, the fill factor of the standard 4T pinned photodiode pixel is lower, because it has more light insensitive components, for instance, the transfer gate, the source follower. To solve this problem, a shared pixel structure may be applied, e.g. the shared 1.75T pinned photodiode pixel. See Figure 2.4.

In Figure 2.4, four pixels share one reset switch, one source follow and one select switch, having on the average 1.75 transistors per pixel, which improves the fill factor apparently.

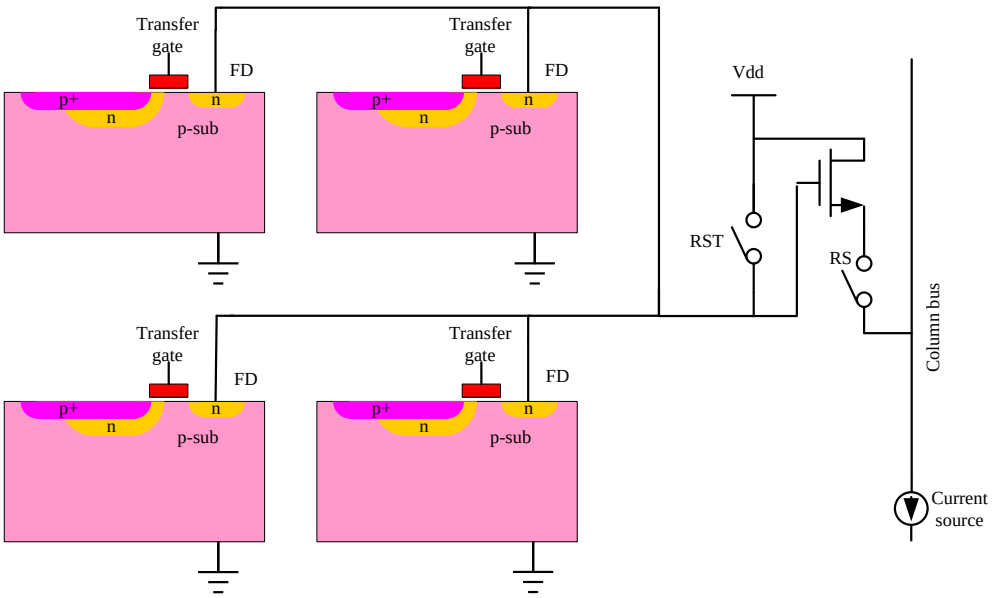


Figure 2.4 The shared 1.75T pinned photodiode pixel

2.3 Readout circuitry structures

After the brief discussion of the pixel structures, let's focus on the readout circuitry structures in image sensors. Normally the readout circuitry comprises a row decoder, a column decoder for addressing the pixels, and the analog-to-digital converters (ADCs) for signal processing. In today's CMOS technology, the ADCs are often integrated on chip to decrease noise and provide a digital interface [2.6]. Based on the hierarchy, the ADCs can be classified into three levels: chip-level ADCs, column-level ADCs and pixel-level ADCs.

2.3.1 Readout circuitry with the chip-level ADC

Figure 2.5 shows the block diagram of an image sensor with a chip-level ADC; the whole pixel array signals are read out and processed in series by one unique ADC. The readout circuitry with the chip-level ADC is more concise, high fill factor and chip area saving, comparing with the circuitry applying column-level ADCs, pixel-level ADCs. And because all pixels share the unique ADC, there is no ADC offset, which makes the readout signals more unified [2.7]. However, the readout circuitry with the chip-level ADC has a drawback: low readout speed. The required frequency bandwidth of the chip-level ADC is proportional to $N_R*N_C*R_f$, where N_R is the number of rows, N_C is the number of columns and R_f is the frame rate [2.6].

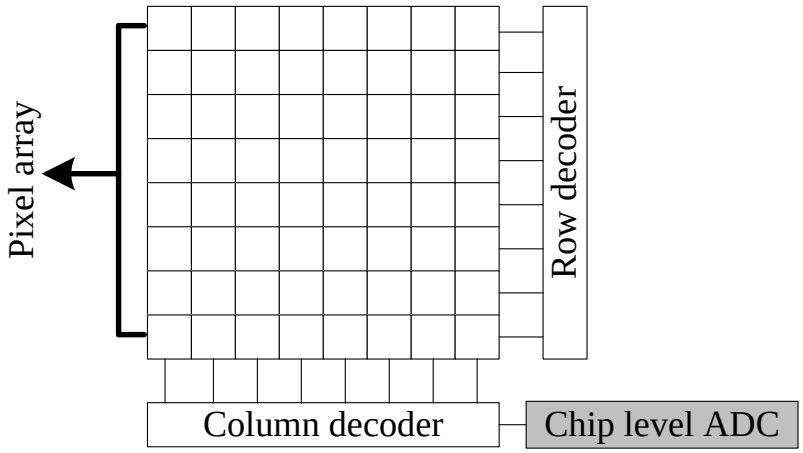


Figure 2.5 An image sensor with a chip-level ADC

2.3.2 Readout circuitry with column-level ADCs

For the image sensor with column ADCs, the pixel signals are processed row by row through the parallel ADCs. Its block graph is shown in Figure 2.6. The readout speed of the circuitry with column-level ADCs is much faster than the circuitry with the chip-level ADC. And its fill factor, chip area and power consumption are acceptable comparing with the later introduced readout circuitry with pixel-level ADCs. The readout circuitry with column-level ADCs is widely used in high-resolution low-cost cameras [2.8]. In this thesis work, a readout circuitry with column-level ADCs is applied.

And when we use this kind of circuitry structure, we need to pay attention to its column fixed-pattern noise (column FPN), which is caused by the offset and gain mismatch of column ADCs [2.7].

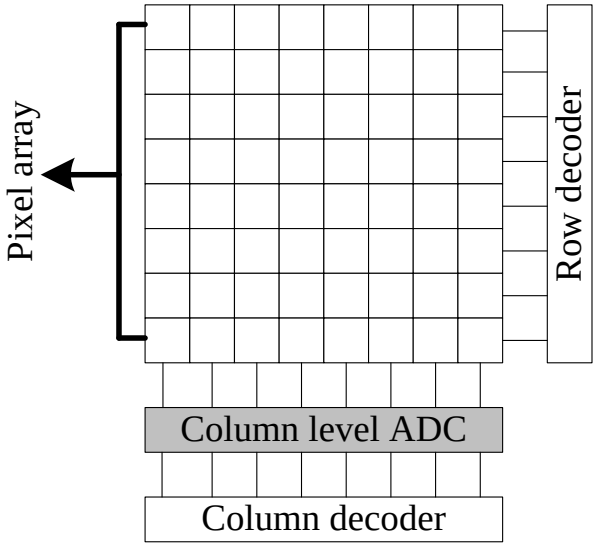


Figure 2.6 An image sensor with column-level ADCs

2.3.3 Readout circuitry with pixel-level ADCs

The image sensor with pixel-level ADCs is shown in Figure 2.7. In this architecture, each pixel has its own ADC inside. The whole pixel array signals could be processed synchronously, thus the signal processing speed is rather rapid. The price to pay is the large area and power consumption for the in-pixel ADCs. Therefore, there is a trade-off between pixel size (resolution) and fill factor.

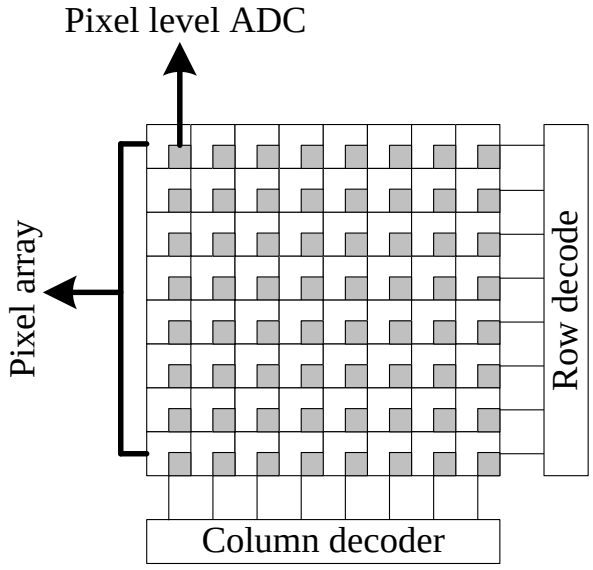


Figure 2.7 An image sensor with pixel-level ADCs

2.4 References

[2.1] “Noise (electronics)”, http://en.wikipedia.org/wiki/Noise_(electronics), Apr. 2013.

[2.2] Theuwissen, A., “CMOS image sensors: State-of-the-art and future perspectives,” Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European , pp.21,27, Sept. 2007.

[2.3] Razavi, B., Design of Analog CMOS Integrated Circuits. Boston: McGraw-Hill, pp. 209,218, 2001.

[2.4] Kirton, M. J. and Uren, M.J., “Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/f) noise,” Advances in Physics, vol. 38, No. 4, pp. 367,468, 1989.

[2.5] Guidash, R.M.; Lee, T.-H.; Lee, P. P K; Sackett, D. H.; Drowley, C.I.; Swenson, M.S.; Arbaugh, L.; Hollstein, R.; Shapiro, F.; Domer, S., “A 0.6 /spl mu/m CMOS pinned photodiode color imager technology,” Electron Devices Meeting, 1997. IEDM '97. Technical Digest., International , pp.927,929, Dec. 1997.

[2.6] Takayanagi, I. and Nakamura, J., “High-Resolution CMOS Video Image Sensors,” Proceedings of the IEEE, Vol. 101, No. 1, pp.61,73, Jan. 2013.

[2.7] Guo, J., “DLL Based Single Slope ADC For CMOS Image Sensor Column Readout,” Master Thesis, Delft University of Technology, Electrical Engineering, Mathematics and Computer Science, Microelectronics & Computer Engineering, The Netherlands, 2011.

[2.8] Snoeij, M.F.; Theuwissen, A.; Makinwa, K.; Huijsing, J.H., “A CMOS Imager with Column-Level ADC Using Dynamic Column FPN Reduction,” Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International, pp.2014,2023, Feb. 2006.

Chapter 3 System analysis and circuitry implementation

After the concise discussion of the noise principles and an overview of the pixel and readout circuitry structures in the second chapter, a detailed analysis and circuitry implementation of the whole system will be presented in this chapter. Firstly, the pixel design is explained in section 3.1. And then the readout circuitry analysis is shown in section 3.2.

3.1 Low noise pixel design

3.1.1 Pixel structure

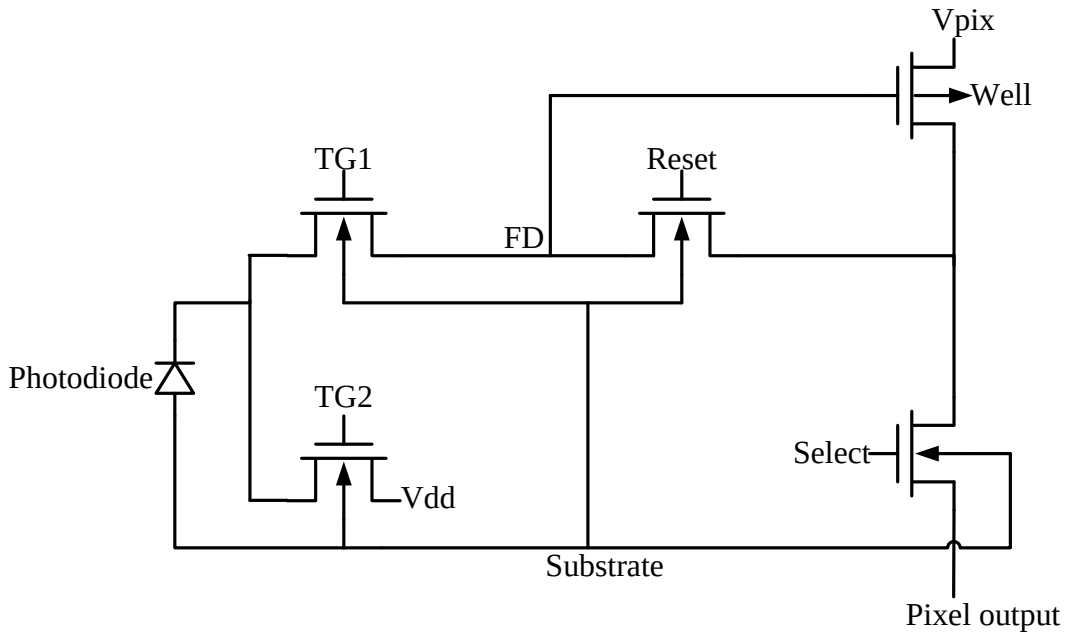


Figure 3.1 The pixel structure [3.1]

The pixel structure is shown in Figure 3.1. It's a special 5T pinned photodiode pixel, including four switches (two nMOS transistor switches and two transfer gate switches) and one pMOS transistor. There are two novel creations in this pixel structure comparing with the standard 4T pinned photodiode pixel structure. Firstly, we use a pMOS transistor working as an amplifier instead of the nMOS transistor working as the source-follower. In standard CMOS technology, all the nMOS transistors share the unique substrate (the p-well), while the pMOS transistors could have separate bulk regions (the separate n-wells), which are easy to control independently. Through the proper operation of the pMOS transistor substrate voltage, we can reduce its flicker noise, which will be explained detailed in section 3.1.2. And with

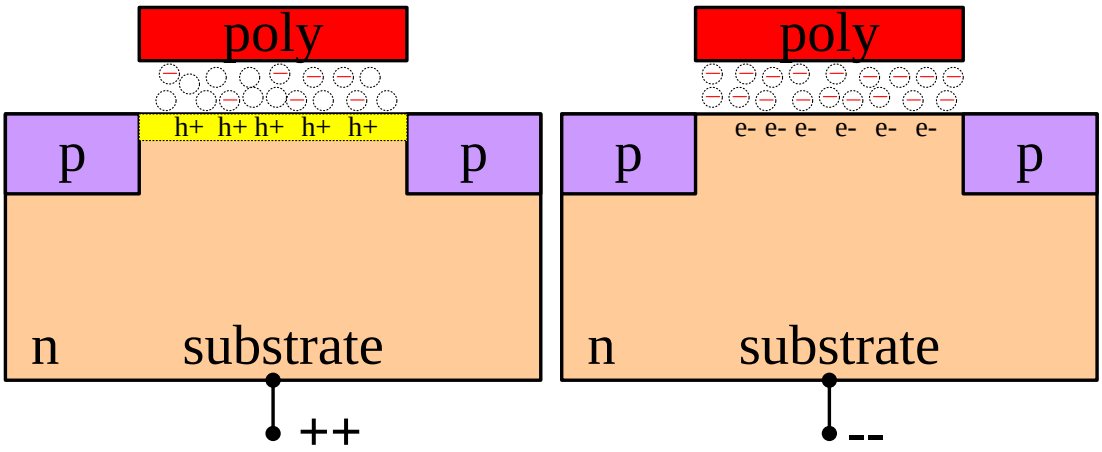
this pMOSFET and its parasitic capacitors, we can adjust the pixel output signal by regulating pMOSFET source driving voltage Vpix, which will also be introduced in section 3.1.2. Secondly, we apply two transfer gates (TG1 and TG2). The function of TG1 is the same as the transfer gate in the standard 4T pinned photodiode pixel to control the transfer of the photo-charge, while TG2 is used as a shutter for adjusting the photodiode's integrating time.

3.1.2 Pixel operation and methods to reduce noise

As discussed in chapter 2, at pixel level, the most significant noise sources are thermal noise and flicker noise in the MOS transistors. Thermal noise in the pixel can be reduced or almost cancelled by correlated double sampling (CDS) and oversampling. But flicker noise is difficult to reduce, because the normal methods used to reduce flicker noise cost too much. For example, using large size devices (large W and L), which consumes a lot of chip area.

In this thesis, we apply a novel method to decrease the flicker noise. Flicker noise is thought to be generated by the random capture and emission of charge by the trapping centers at the interface between the gate oxide and the underlying silicon [3.2]. For a pMOS transistor, when it is biased in inversion state, the traps in the Si/SiO2 interface are partly filled with electrons, which are shown in Figure 3.2(a) [3.1]. The traps interact with the inversion layer by capturing and emitting charge, and the interacting time varies from less than nanoseconds to longer than days. These interactions generate the flicker noise.

When the pMOS transistor is biased in accumulation state, the Fermi-level of the internal silicon is higher than the Fermi-level of the interface states, the traps (interface states) in the Si/SiO2 interface are fully filled by the electrons, which are shown in Figure 3.2(b) [3.1]. And in accumulation state, the Fermi-level of internal silicon is higher than that in inversion state, thus the time constants of charge capture and emission are much shorter than those in inversion state, which means when the pMOS transistor is biased in accumulation state, its flicker noise in low frequency is much lower than that in inversion state.



(a) Inversion state (b) Accumulation state

Figure 3.2 Traps in pMOS transistor Si/SiO2 interface

While for MOS transistors, the accumulation state is not a working state. We need to cycle the pMOS transistor between accumulation and inversion. In each cycle, the pMOS transistor is biased in accumulation state first, the traps in the Si/SiO2 interface are pressured to be fully filled, like a refreshed state, the traps' memory is erased, and then the pMOS transistor is biased in inversion state, the fully filled traps interact with the inversion layer rapidly. All the capture and emission with the time constants larger than the cycling period are cancelled, thus the traps' correlation time is limited to less than the cycling period. If we sample the signal once or less than once per cycling period in inversion state, the noise in the sampled signals is uncorrelated. The spectrum of the noise becomes "white". Then we can use oversampling to reduce this noise component as well [3.1]. The sequence diagrams of the pMOSFET well voltage (substrate voltage) cycling and pixel output sampling are shown in Figure 3.3.

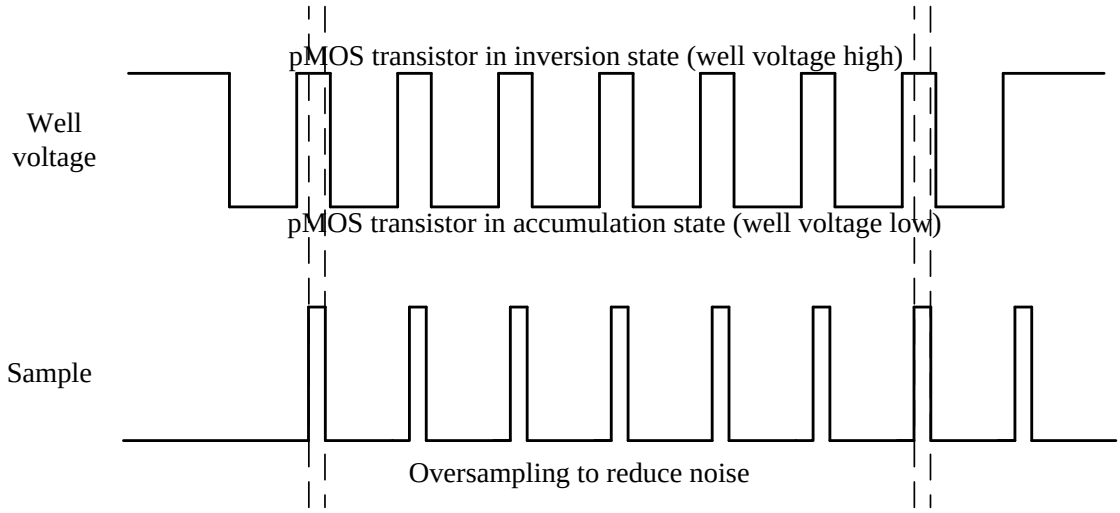


Figure 3.3 The sequence diagrams of pMOSFET well voltage cycling and pixel output sampling

After the analysis of the method to reduce the flicker noise, now we focus on the ways to reduce thermal noise. First, we apply CDS (correlated double sampling) technology. The timing diagram of CDS is shown in Figure 3.4. The operation principle is like this: firstly, we reset the pixel to remove the signal from previous operations, and then we cycle the pMOSFET well voltage, sample the pixel output signal (Pixel output node in Figure 3.1) four times (assuming four times is suitable for decreasing the flicker noise to a proper range) to get the sampling results: A, B, C, D. Later, we close the transfer gate to let the charge integrated in the pinned photodiode transfer to FD (floating diffusion node). Then we cycle the pMOSFET well voltage, sample the pixel output signal four times again to get another four sampling results: E, F, G, H. At last, we use the average of E, F, G, H to subtract the average of A, B, C, D. The final result that we get, represents the pixel signal accurately.

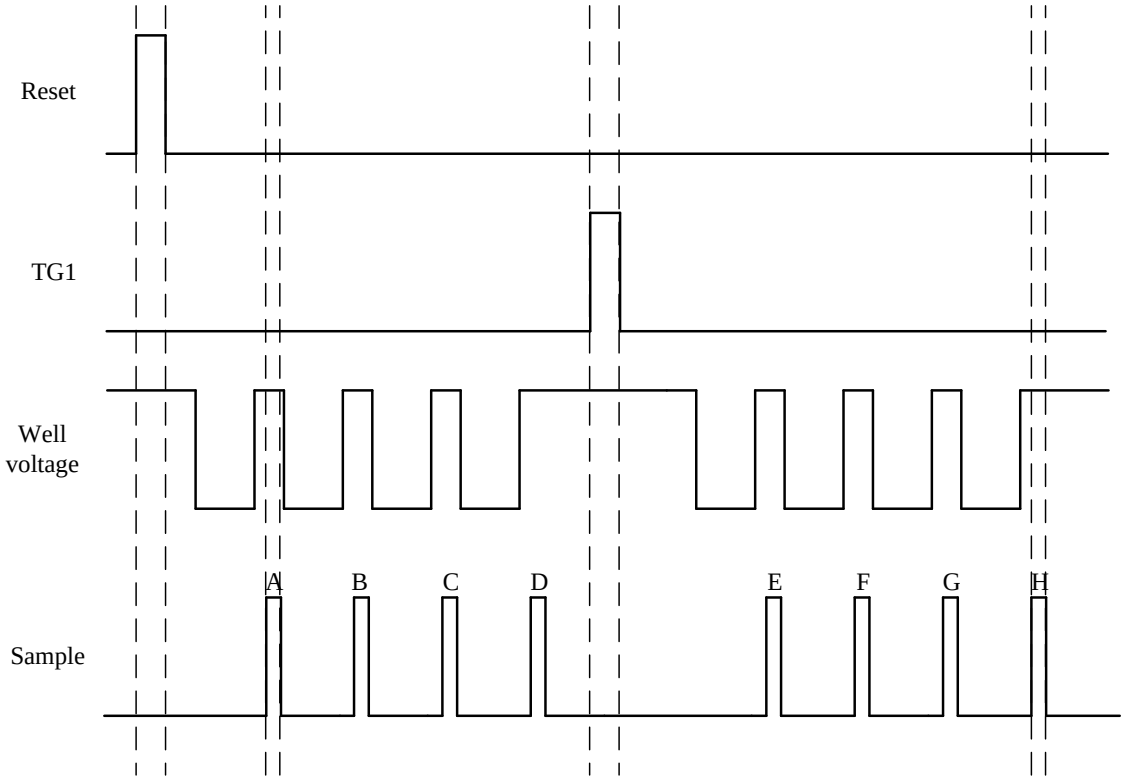


Figure 3.4 The timing diagram of CDS

Besides the application of CDS, we apply oversampling technology at the same time. The four times pMOS well voltage cycling and pixel output sampling are the applications of oversampling, they help to reduce the pixel thermal noise and the shaped flicker noise.

In this pixel structure, we apply two transfer gates (TG1 and TG2). In normal situation, charge generated in the pixel is collected by the pinned photodiode. We keep TG2 off and use TG1 to transfer the charge from photodiode to the floating diffusion node. But when the input light signal is too large, the charge generated in the pixel could not be stored in the photodiode; it will travel to the neighboring pixel, this is the so-called pixel blooming. In order to prevent this circumstance, we operate TG2 to emit part of the charge to power line Vdd and adjust the charge integrating time of photodiode. The timing plots of the two transfer gates operations are shown in Figure 3.5.

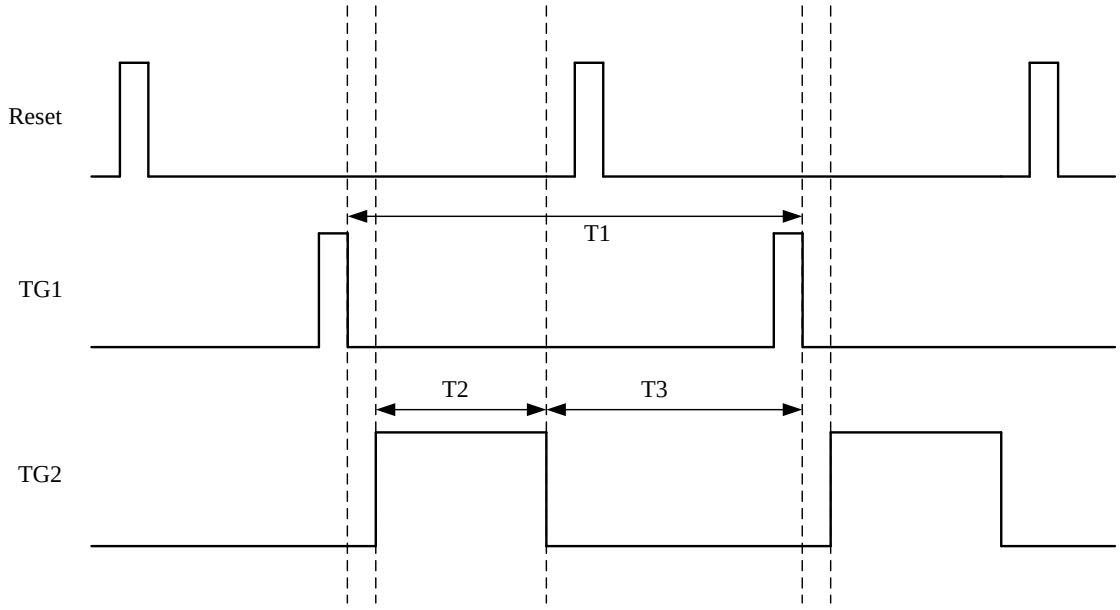


Figure 3.5 The timing plots of the two transfer gates operations

In normal state, the TG2 is off and the charge integrating time is T1. While if the light is too intense, and the photodiode generates too much charge; we turn TG2 on in time period T2, the charge integrating time is decreased to time period T3. The change of charge integrating time can adjust the pixel detection range, for example, if the lightness is uniform, we can switch TG2 on in time period T2, and then the pixel detection range is T1/T3 times of the normal situation (TG2 is off).

In pixel structure, the pMOS transistor, its parasitic gate drain overlapping capacitor Cgd, gate source overlapping capacitor Cgs, and the floating diffusion node capacitor Cfd work together as a capacitive amplifier. We can control pixel output signal through the adjustment of the pMOS transistor source driving voltage Vpix, which can provide a proper input signal range for the following readout circuitry. Figure 3.6 shows the structure of the capacitive amplifier, Vcolumn is the pixel output voltage, Vpix is the pMOS transistor source driving voltage, Vfd is the floating diffusion node voltage. Before we adjust Vpix, these voltages obey these formulas:

$$Vfd*Cfd+(Vfd-Vpix)*Cgs+(Vfd-Vcolumn)*Cgd= Qbefore \quad (3\text{-}1)$$

$$(Vfd-Vpix)*A=Vcolumn-Vpix \quad (3\text{-}2)$$

where Qbefore is the total charge on the floating diffusion node before the adjustment of Vpix. A is the gain of the capacitive amplifier.

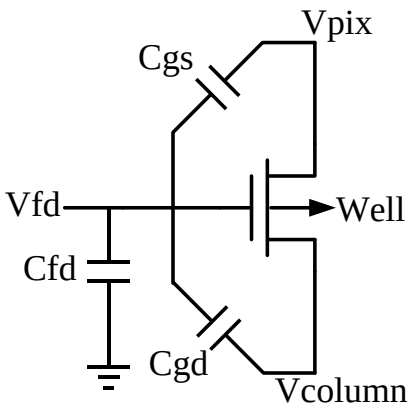


Figure 3.6 The pMOS capacitive amplifier

After we adjust Vpix to Vpix1, we find that Vfd changes to Vfd1, Vcolumn changes to Vcolumn1. These voltages obey these formulas:

$$Vfd1 *Cfd+(Vfd1-Vpix1)*Cgs+(Vfd1-Vcolumn1)*Cgd= Qafter \quad (3\text{-}3)$$

$$(Vfd1-Vpix1)*A=Vcolumn1-Vpix1 \quad (3\text{-}4)$$

where Qafter is the total charge on the floating diffusion node after the adjustment of Vpix.

Because the adjustment of Vpix doesn't inject or remove the charge on the floating diffusion node, we have the charge conservation formula:

$$Qbefore=Qafter \quad (3\text{-}5)$$

Assuming the gain of the capacitive amplifier is infinite and synthesizing formulas (3-1)~(3-5), we have these results:

$$\Delta Vfd=\Delta Vpix \quad (3\text{-}6)$$

$$\frac{\Delta Vcolumn-\Delta Vpix}{\Delta Vpix}=\frac{Cfd}{Cgd} \quad (3\text{-}7)$$

where ΔVfd is Vfd1-Vfd, ΔVpix is Vpix1-Vpix, Δ Vcolumn is Vcolumn1- Vcolumn.

The floating diffusion node capacitor Cfd is larger than the pMOS transistor parasitic gate drain overlapping capacitor Cgd, so we can add a small adjustment to pMOS transistor source driving voltage Vpix to get a proper pixel output voltage Vcolumn, which will be used in the next chapter's simulations.

3.1.3 Layout of the pixel

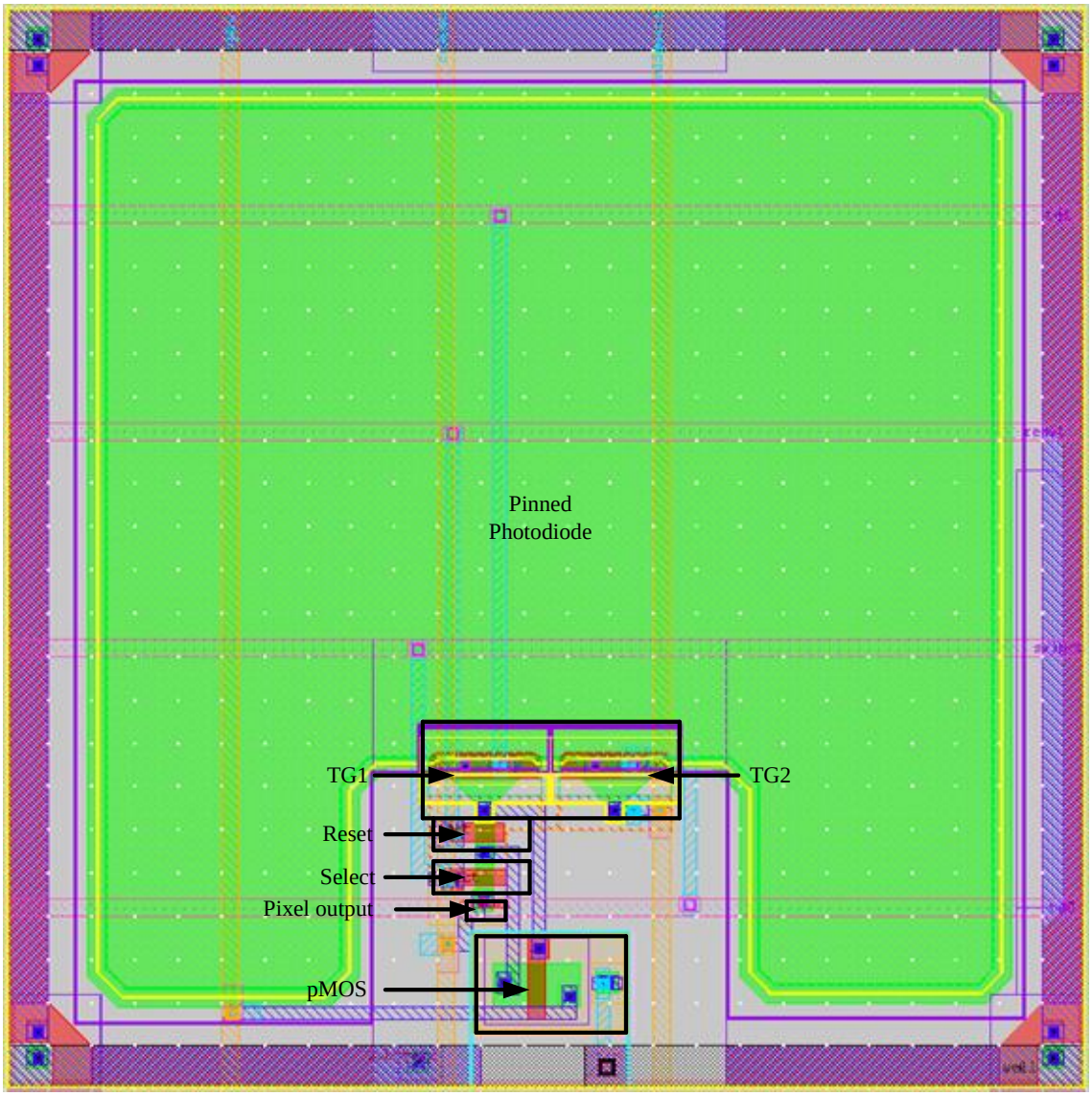


Figure 3.7 The layout of the pixel

Figure 3.7 shows the layout of the pixel. The layout is designed for 0.18μm backside illuminated technology. But in this multiple project wafer tape-out and for the test runs, we use normal frontside illuminated 0.18μm technology. The scale of the pixel is 25*25μm^2, and some Caeleste's proprietary solutions are used to solve the image lag problem.

3.2 Readout circuitry design

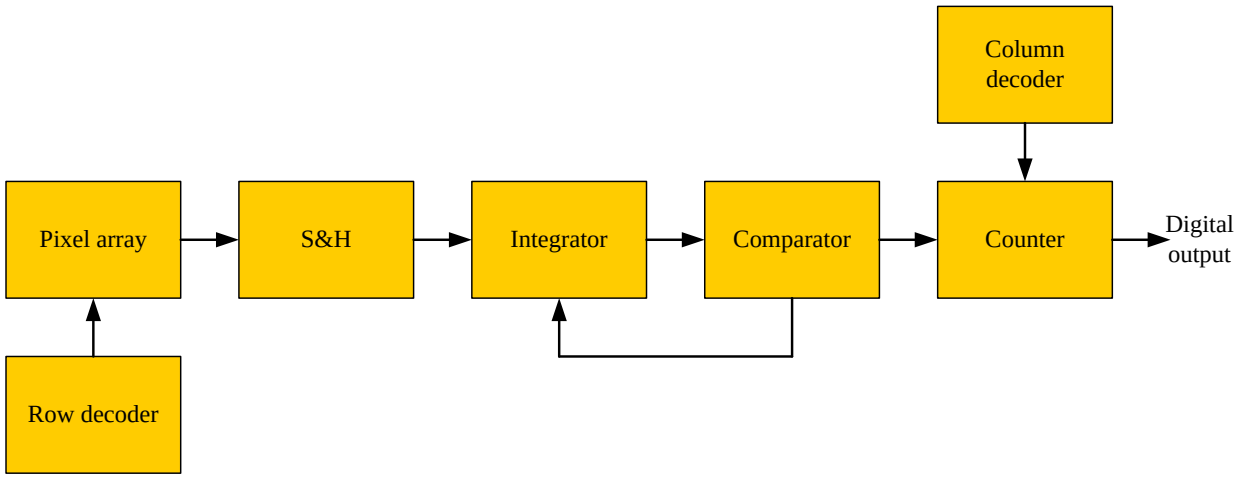


Figure 3.8 The topology of readout circuitry

Figure 3.8 shows the topology of the readout circuitry. Firstly, the row decoder chooses one row of pixels from the pixel array, whose signals will be sampled and held by a row of S&H circuitry. Then the held signals are integrated by the integrators. The output signals of the integrators are handled by a row of comparators. The comparators also generate feedback signals to adjust the integrators. At last, the digital counters process the comparators' output signals and output the digital signals in series under the control of column decoder.

And the readout circuitry could also be treated as the first-order sigma-delta ADCs with digital counters, their structures are shown in Figure 3.9.

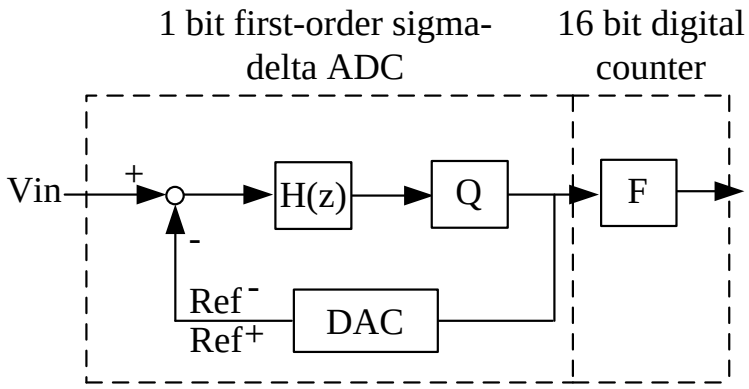


Figure 3.9 The structure of first-order sigma-delta ADC with digital counter

where Vin is the input signal of ADC, H(z) is the integrator, Q is the quantizer, F is the decimate filter. Ref^+ and Ref^- are the positive and negative feedbacks.

3.2.1 S&H and integrator circuitry

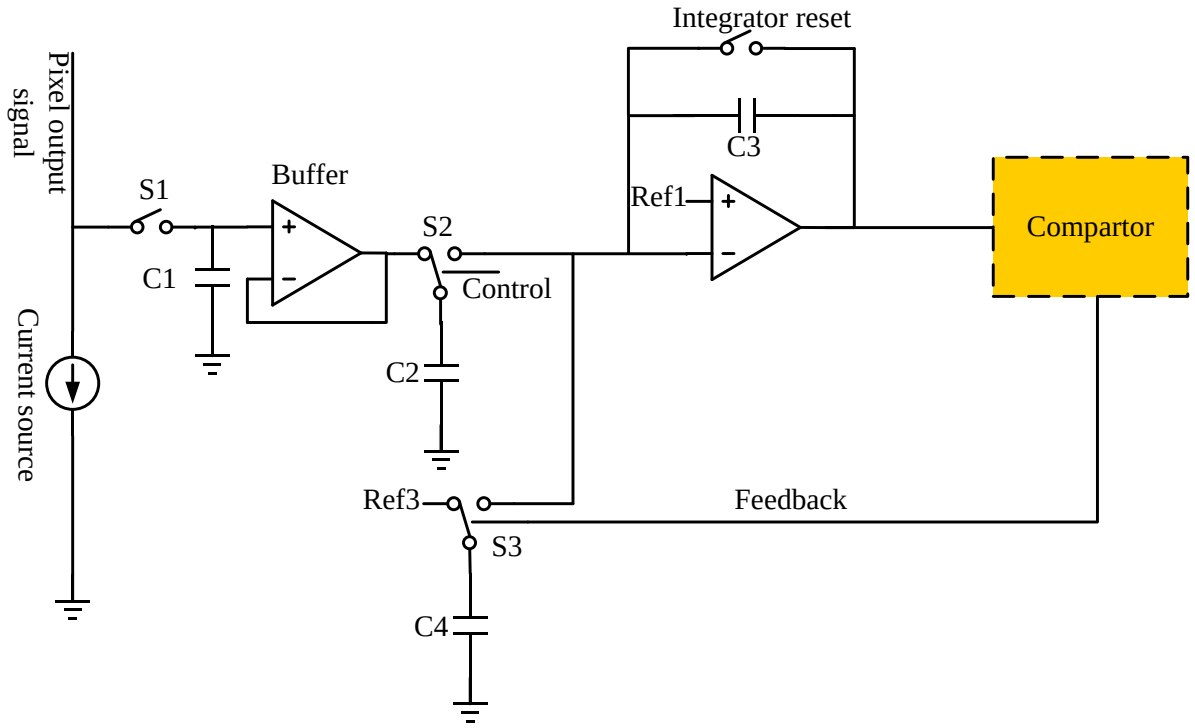


Figure 3.10 The S&H and integrator circuitry

Figure 3.10 shows the S&H and integrator circuitry. Firstly, switch S1 and capacitor C1 sample and hold the pixel output signal. The timing diagram of switch S1 is shown in Figure 3.11.

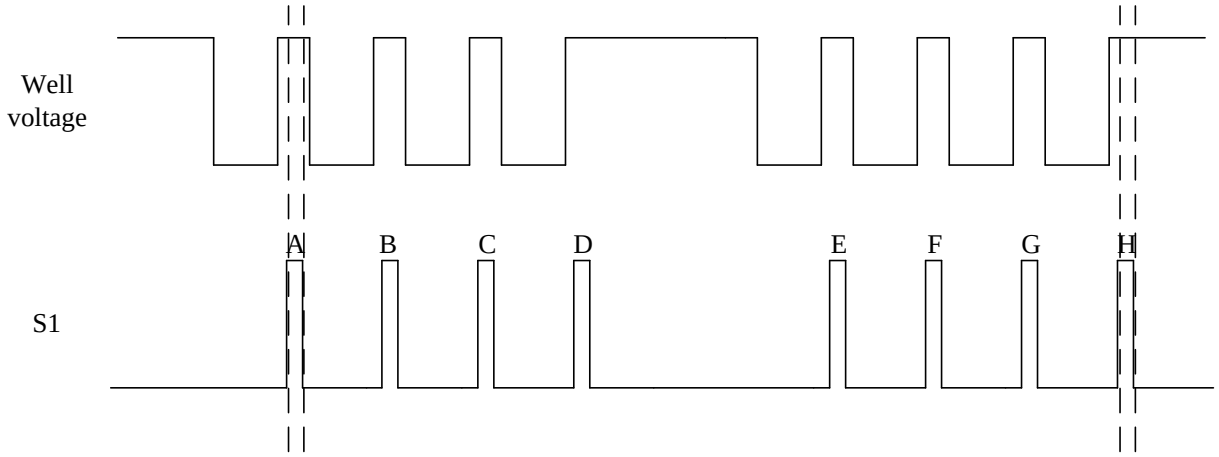


Figure 3.11 The timing diagram of switch S1

Then after the buffer, there is a four-port switch S2, which has one fixed node, two movable nodes, and a control port. A capacitor C2 is connected to S2's fixed node. We add a control signal on the control port to cycle the fixed node between the two movable nodes to first store

the after-buffer signal on C2 and then transfer it to the integrator. This stored signal could be treated as the combination of the input signal Vin of the ADC and the positive reference signal Ref^{+} of the DAC shown in Figure 3.9. In order to reduce the general noise, we use switch S2 to oversample the after-buffer signal. The timing diagram of S2 oversampling is shown in Figure 3.12.

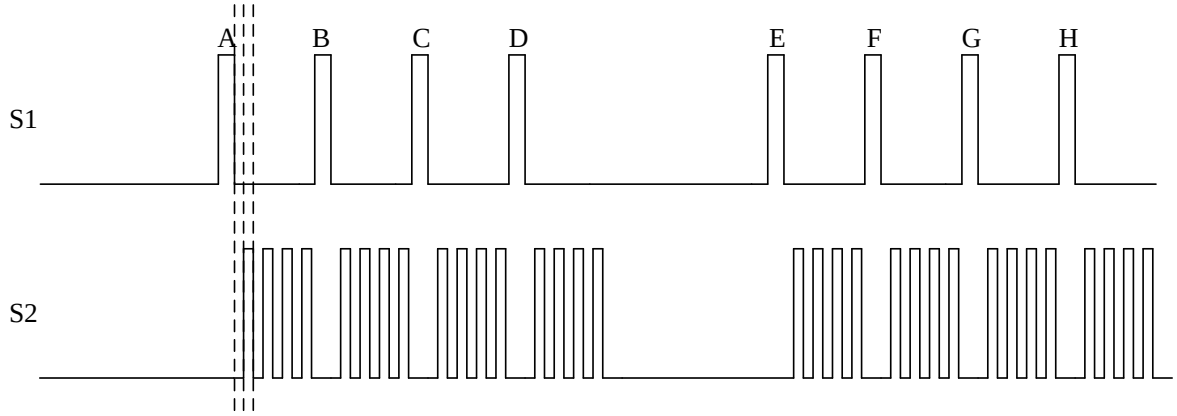


Figure 3.12 The timing diagram of S2 oversampling

After oversampling, the signal is integrated on the integrator capacitor C3, and there is an integrator reset switch, which is used to reset the integrator capacitor at the beginning of each period. The output signal of the integrator is handled by the comparator later. The comparator transfers the signal from the analog domain to the digital domain, which will be explained in detail in section 3.2.2. The comparator generates a feedback signal to cycle the other four-port switch S3. The fixed node of S3 connects to the capacitor C4, and its two movable nodes connect to the DC reference Ref3 and the input of the integrator shown in Figure 3.10. The capacitor C4 first stores the DC reference signal Ref3 and then transfers it to the input of the integrator. The DC reference signal Ref3 could be treated as the negative reference signal Ref^{-} of the DAC shown in Figure 3.9; it causes the toggle of the integrator output, which will be explained in section 3.2.2. Figure 3.13 shows the sequence diagrams of the integrator output signal and the comparator feedback signal.

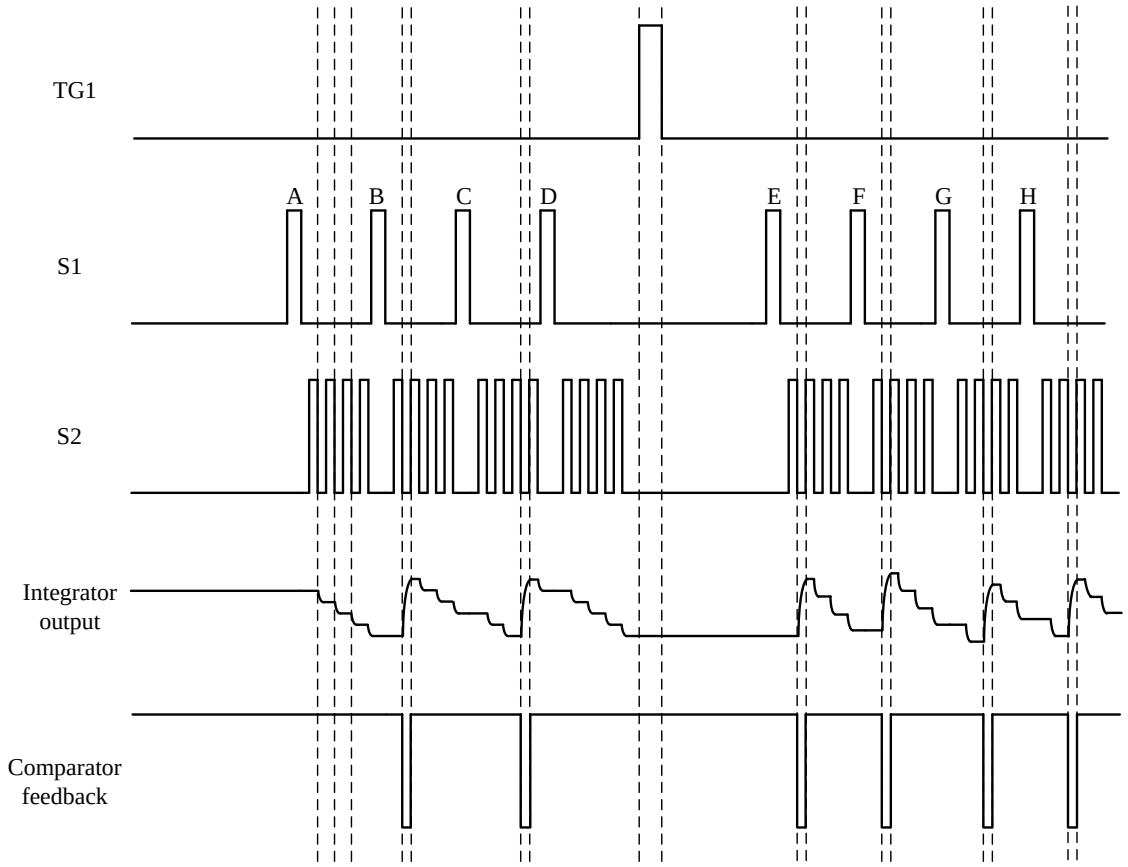


Figure 3.13 The sequence diagrams of the integrator output and comparator feedback signals

Each time when switch S2 cycles, the charge stored on C2 transfers to the integrator capacitor C3, which causes the voltage drop of integrator output signal. The voltage drop obeys the formula:

$$Qtrans=(Vinp-Vinn)*C2=\Delta Vout*C3$$

$$\Longrightarrow \quad \Delta Vout=(Vinp-Vinn)*C2/C3 \tag{3-8}$$

where Qtrans is the charge transferred from C2 to C3, Vinp is the non-inverting input of the integrator amplifier, Vinn is the inverting input of the integrator amplifier. C2 is the oversample and hold capacitor before the integrator, which is shown in Figure 3.10, C3 is the integrator capacitor, and ΔVout is the voltage drop of the integrator output.

From formula (3-8), we find that the larger Vinn, the larger integrator output voltage drop, which is also shown in Figure 3.13: after TG1 pulse, |ΔVout| becomes larger.

3.2.2 Comparator circuitry

After the S&H and integrator circuitry, the following comparator compares the integrator output signal with the DC reference signal Ref2 shown in Figure 3.14 to transfer the analog signal to the digital signal. The comparator circuitry contains a two-stage amplifier and a D flip-flop and some logical circuitry. The topology diagram of comparator circuitry is shown in Figure 3.14.

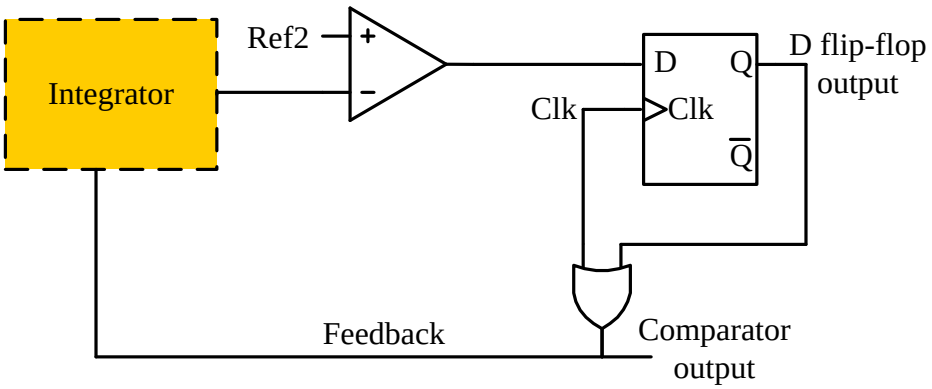


Figure 3.14 The topology diagram of comparator circuitry

The output signal of integrator is first handled by a two-stage amplifier. The amplifier treats the integrator output signal and the DC reference signal Ref2 as its two inputs, and magnifies the difference of these two inputs. Since the two-stage amplifier has a large gain, the output signal of the amplifier looks like a square wave, which is shown in Figure 3.15.

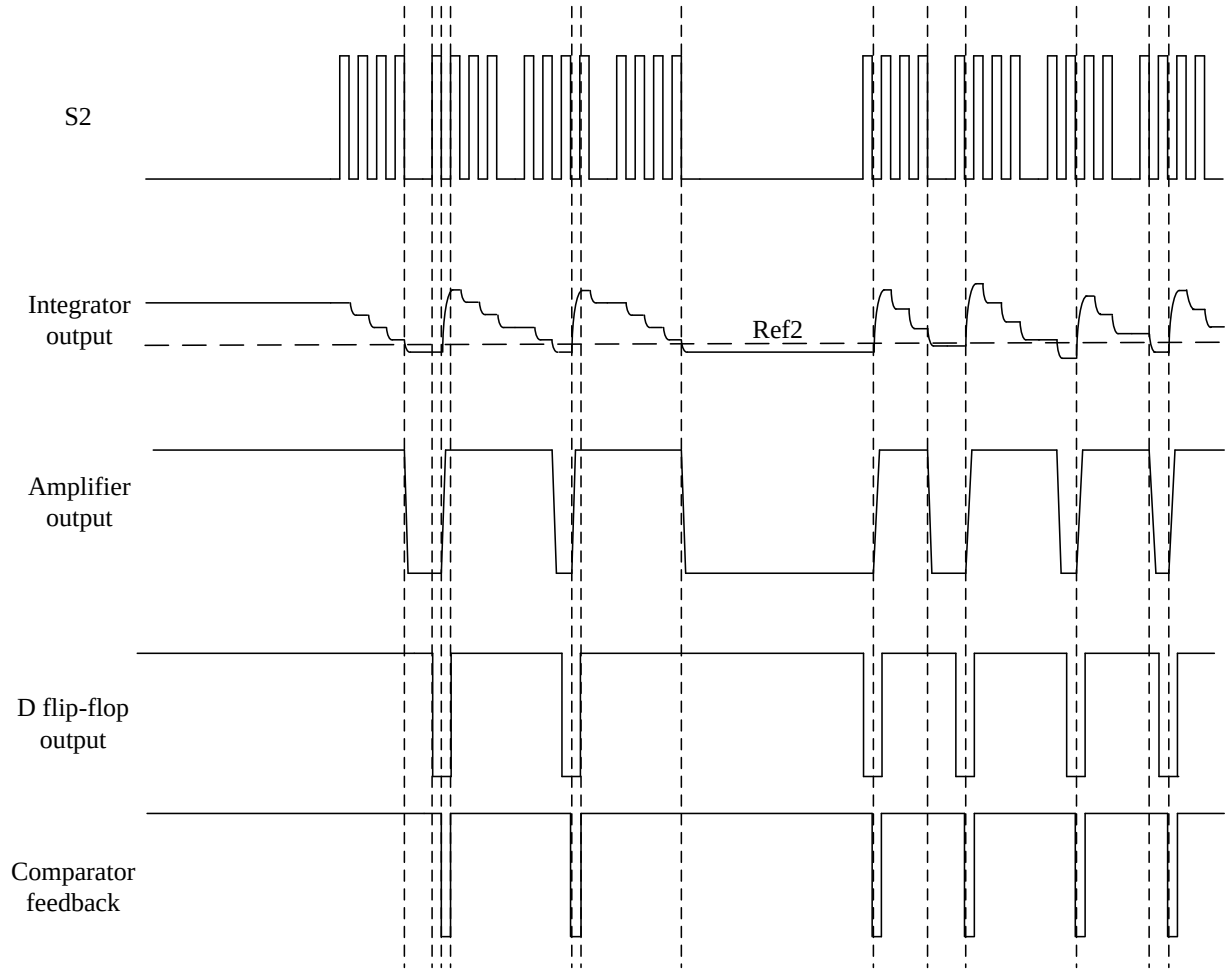


Figure 3.15 The timing diagrams of the signals in the comparator circuitry

The circuitry implementation of the two-stage amplifier is shown in Figure 3.16. The first stage is a pMOS differential amplifier. The transistor M1 works as a pMOS current source, M2 and M3 are the two pMOS differential inputs, M4 and M5 are the nMOS active loads. The second stage is a common source amplifier. The transistor M6 works as a pMOS current source, M10 is the nMOS input. And the special nMOS transistor M7 is used to limit the drain to source voltage Vds of M10. The nMOS transistor with a large drain to source voltage may generate photons, which should be avoided in the image sensor design. The nMOS transistors M8 and M9 connected as diodes are applied to limit the input voltage of the second stage.

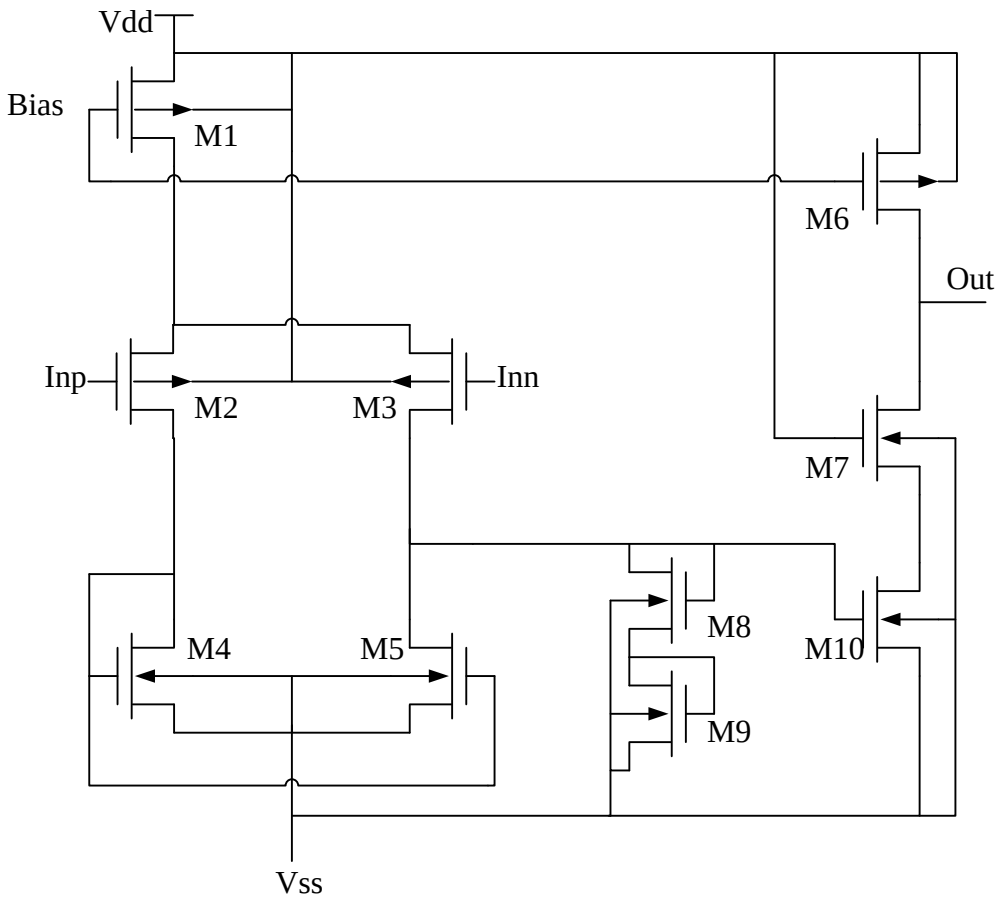


Figure 3.16 The two-stage amplifier circuitry

The output signal of the amplifier is processed by a D flip-flop; the timing diagram of the D flip-flop output is shown in Figure 3.15. The D flip-flop in this thesis is a master-slave rising edge-triggered D flip-flop, which contains two D latches. When the rising edge of the clock comes, the D flip-flop transfers its captured input signal D to its output Q. The clock of this D flip-flop is synchronized with the clock of switch S2 in Figure 3.10. The gate-level implementation of the D flip-flop is shown in Figure 3.17. From Figure 3.15, we can see comparing with the output signal of the amplifier, the D flip-flop output has one S2 clock period delay, and it can keep the signal for one S2 clock period, which is necessary for charge transfer.

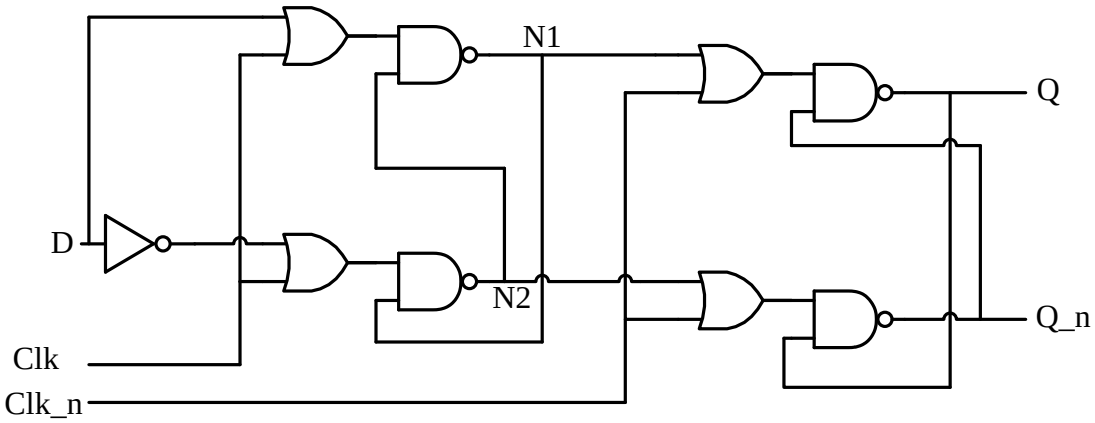


Figure 3.17 The gate-level implementation of the D flip-flop

In Figure 3.17, the operation principle of the D flip-flop is like this: first, when the Clk is low, Q and Q_n keep their values; the value of D transfers to N2, and the value of $\overline{D}$ transfers to N1. Then when the Clk changes to high, N1 and N2 keep their values; the value of N2 transfers to Q, and the value of N1 transfers to Q_n. Therefore, we can see D transfers to Q at the rising edge of Clk.

And in this design, the D flip-flop output is followed by an OR gate (this OR gate is a design redundancy, we will delete it in the next generation design), the other input of the OR gate is the S2 control clock, the output of the OR gate is the comparator feedback signal, which is also the comparator output signal. As shown in Figure 3.15, when the integrator output is higher than Ref2, the output of the D flip-flop keeps high; only when the integrator output becomes lower than Ref2, the D flip-flop output will fall down at the following rising edge of the S2 control clock, and keep down for a S2 control clock period. When the D flip-flop output goes down, at the following falling edge of the S2 control clock, the comparator feedback signal will fall down as well. And then it rises up at the following rising edge of the S2 control clock. Therefore, the toggle of the integrator output only happens at several falling edges of the S2 control clock. And the charge transfer between the capacitor C2 and integrator capacitor C3 happens at each falling edge of S2 control clock. So Ref^+, Ref^- should obey formula (3-9). Considering about the characteristics of the ADC, the DAC reference signals Ref^+, Ref^- (Ref3), ADC input signal Vin, pixel output signal Vcolumn and integrator amplifier DC reference Ref1 obey these formulas:

$$2*(Ref^+ - Ref1) = Ref1 - Ref^- \quad (3\text{-}9)$$

$$Ref^+ - Ref1 > |Vin| \quad (3\text{-}10)$$

$$Vcolumn = Vin + Ref^{+} \tag{3-11}$$

$$Ref^{-} = Ref3 \tag{3-12}$$

And in this design, all the capacitors are n-well CMOS capacitors. So we need to properly forward bias these capacitors to keep them working in linear region (forward biased over 0.3V). So the comparator feedback DC reference Ref3 and the two-stage amplifier DC reference Ref2 obey these formulas:

$$Ref3 > 0.3V \tag{3-13}$$

$$Ref1 - Ref2 > 0.3V \tag{3-14}$$

And considering about the two-stage amplifier structure, the Ref2 should also obey this formula:

$$Ref2 > 0.2V \tag{3-15}$$

These formulas will be used in the circuitry system setting, which will be presented in the next chapter.

3.2.3 Digital counter circuitry

From the explanation above, we conclude that, first, the photo-charge generated in photodiode is converted to the pixel output signal; and then the amplitude of the pixel output signal is transformed to the voltage drop step of the integrator output in the integrator circuitry, the higher pixel output voltage, the larger integrator output voltage drop step; at last, the voltage drop step is mapped to the turning speed of the comparator output in the comparator circuitry. Now we need to design a digital counter to take count of the turning of the comparator output.

In this thesis, we design a 16 bit bidirectional counter to take count of the turning of the comparator output signal and also to apply CDS technology. Before photo-charge is transferred, we count in one direction, and after the charge is transferred, we count in the other direction. The residual value on the counter represents the charge generated on the photodiode (pixel signal).

Figure 3.18 shows the structure diagram of a 3 bit bidirectional counter [3.3]. And its sequence diagram is shown in Figure 3.19. Its operation principle is like this: first, we reset the counter to clean the signal from the last cycle. And then we keep Up/Down control signal

high to let the circuitry counts in “up” direction at each falling edge of the clock. Later, we keep Up/Down control signal low, at each falling edge of clock, the circuitry counts in “down” direction. In this thesis, we create a 16 bit digital counter, whose head and tail parts are the same as the 3 bit bidirectional counter, but the middle part is 14 times repetition of the middle part of the 3 bit bidirectional counter (which is shown in the dashed box of Figure 3.18). We use the comparator output signal as the counter clock signal.

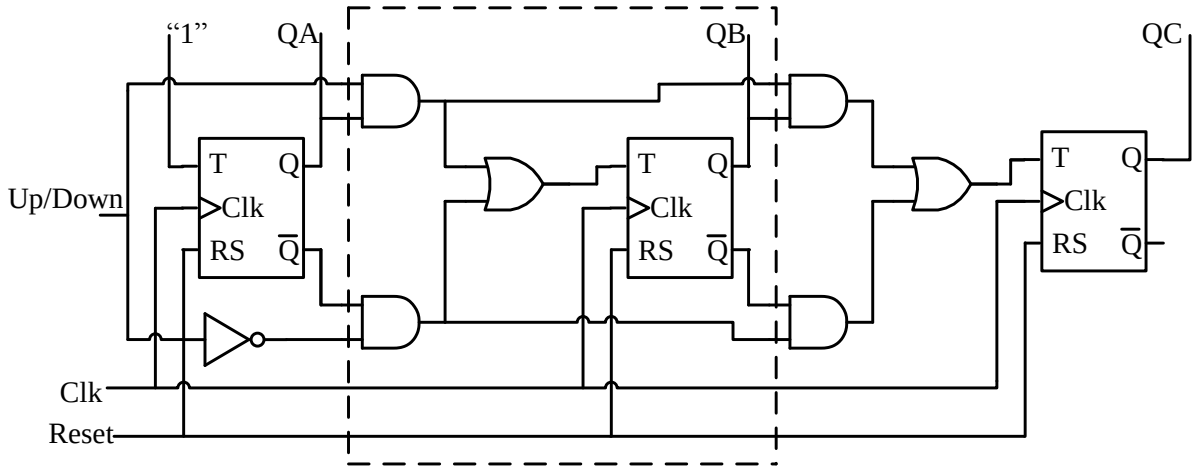


Figure 3.18 The 3 bit bidirectional digital counter structure

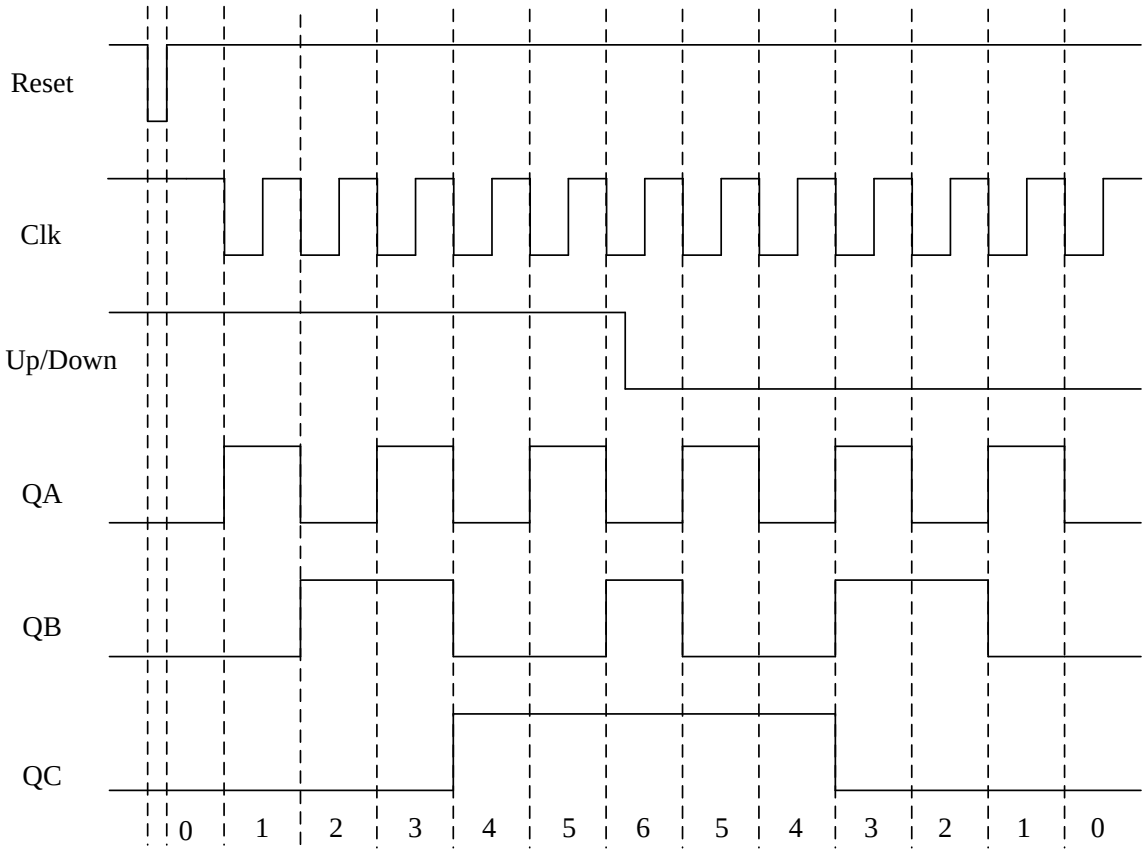


Figure 3.19 The sequence diagram of the 3 bit bidirectional counter

The digital counter applies a series of T flip-flops. The truth table of the T flip-flop is shown in Table 3-1. The gate-level implementation of the T flip-flop is shown in Figure 3.20 [3.4]. The T flip-flop applied here is a master-slave falling edge-triggered T flip-flop with reset, which contains two T latches. The operation principle of this T flip-flop is like this: The T signal is always high. At the reset moment, we keep the reset signal low and Clk signal high to reset Q to low, Q_n, M1 and M2 to high. After reset, because the Clk signal is high, M2 changes to low. From then on, at each rising edge of the Clk, M1 and M2 toggle once, Q and Q_n keep their values. And at each falling edge of the Clk, M1 and M2 keep their values, Q and Q_n toggle once.

Table 3-1 The truth table of T flip- flop

T	Q	Qnext
0	0	0
0	1	1
1	0	1
1	1	0

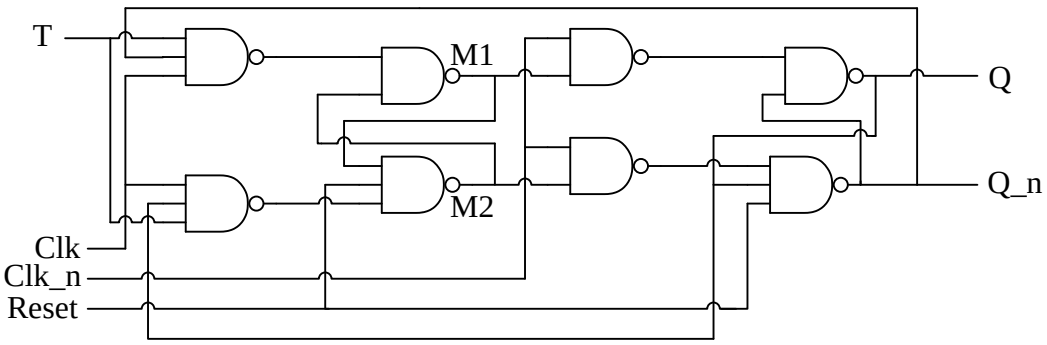


Figure 3.20 The gate-level implementation of the T flip-flop

3.2.4 Row and column decoder circuitry

In the readout circuitry, we also need to use row decoder to address the pixel rows, and the column decoder to arrange the digital counters to export their output signals in series. In this thesis, we use 4-input AND gates and inverters to realize the 4 bit decoder, whose structure is shown in Figure 3.21.

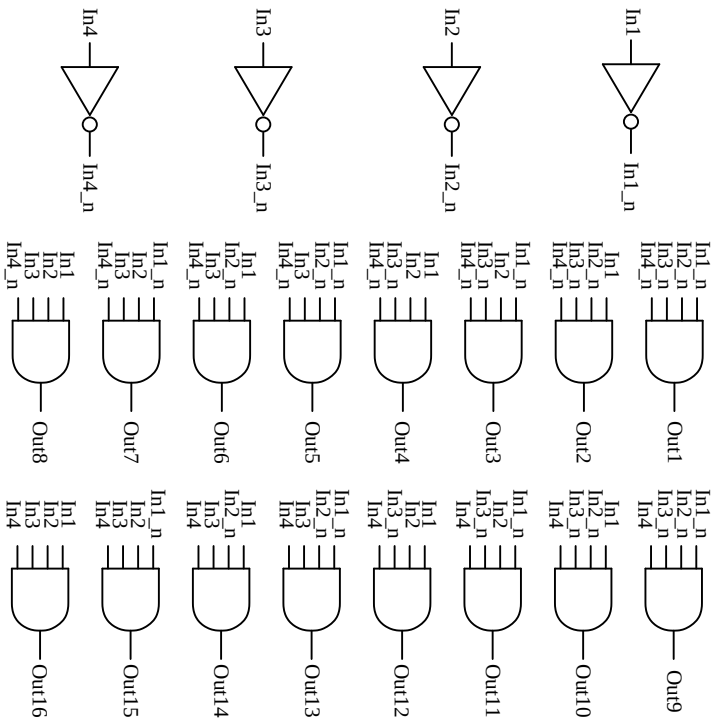


Figure 3.21 The 4 bit decoder structure

For example, if In1 and In3 are low, In2 and In4 are high, and then all of the output signals of the decoder are low except Out11, which means row 11 or column 11 is chosen.

3.2.5 Layout of whole circuitry

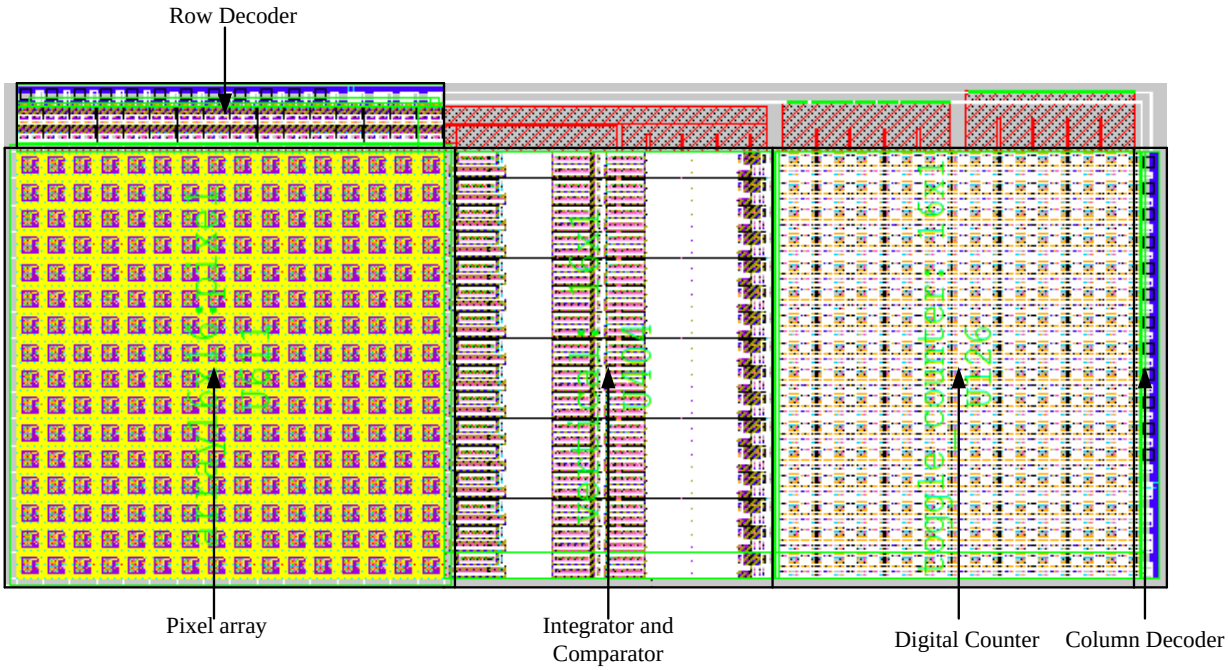


Figure 3.22 The layout of whole circuitry

The layout of the whole circuit is shown in Figure 3.22, with the length of 1075μm, the width of 470μm.

3.3 References

[3.1] Dierickx, B.; Ahmed, N. and Dupont, B., "A 0.5 noise electrons RMS CMOS pixel," Caeleste's scientific publications, www.caeleste.be, Dec. 2011.

[3.2] Kirton, M. J.; and Uren, M.J., "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/f) noise," Advances in Physics, vol. 38, No. 4, pp. 367,468, 1989.

[3.3] "Bidirectional Counters", http://www.electronics-tutorials.ws/counter/count_4.html, Apr. 2013.

[3.4] "The JK Flip-Flop", http://www.play-hookey.com/digital/sequential/jk_nand_flip-flop.html, Apr. 2013.

Chapter 4 Simulations and PCB Test System

In this chapter, first, the pixel simulation and the unit electron photo-charge simulation are presented to show the influence of a unit electron photo-charge on the pixel output signal. Then the system simulation with one pixel is explained as well as the noise transient simulation. At last, the PCB test system is briefly discussed.

4.1 Pixel simulation and unit electron photo-charge simulation

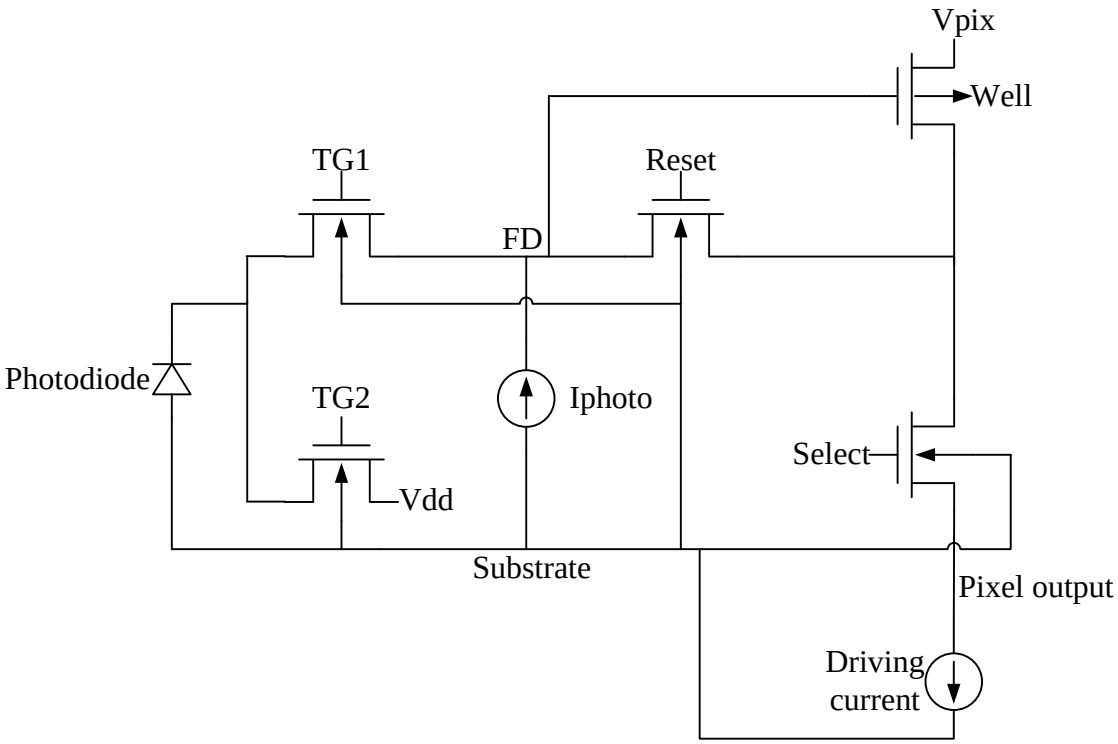


Figure 4.1 Pixel simulation schematic

Figure 4.1 shows the schematic of pixel simulation. The power supply voltage Vdd is 4.0V, and the substrate voltage is 0V. A current source added at the pixel output node provides a driving current for the pMOS transistor. The other current source Iphoto integrating in period Tint (integrated charge is Qcharge= Iphoto*Tint) is used to simulate the photo-charge transfer from the photo-diode to the floating diffusion node (FD). Transfer gates TG1 and TG2 are keep off. The pixel simulation results in one pixel cycle (130μs, from 390μs to 520μs) are shown in Figure 4.2.

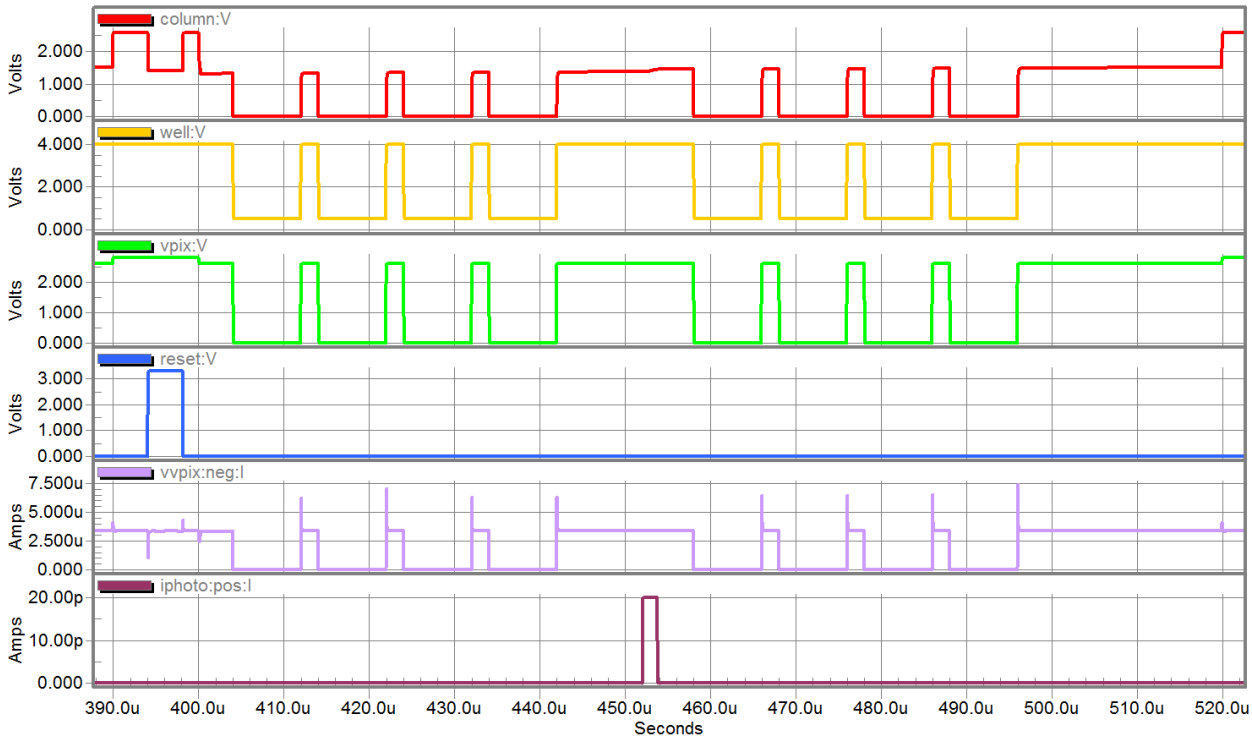


Figure 4.2 The pixel simulation results [Y axes] versus time [X axis] in one pixel cycle. The first trace: the pixel output voltage, second trace: the pMOS well voltage, third trace: the pMOS transistor source driving voltage, fourth trace: the pixel reset signal, fifth trace: the current through the pMOS transistor, the last trace: the photocurrent Iphoto. We can see one pixel cycle has two halves (RESET and SIGNAL halves), and each half shows four pMOS well voltage pulses.

From Figure 4.2, we find when the photocurrent Iphoto pulse comes (which means photo-charge transfers from photo-diode to the floating diffusion node), the pixel output voltage increases a bit. And at the beginning of the cycle, we set the pMOS transistor source driving voltage at 2.8V, and then after the pixel reset, we change it to 2.61V to adjust the pixel output signal at a proper value; the adjustment method is described in section 3.1.2. Each time when the pMOS well voltage is low, the pMOS transistor is in accumulation state; we set the pMOS transistor source driving voltage at 0V to save power.

And in this work, we want to design a pixel array with presumably 0.5 electrons RMS noise. Therefore, as a crucial criterion for further noise measurement, we need to know the influence of a unit electron photo-charge on the pixel output signal.

As explained in the pixel simulation, we apply the photocurrent Iphoto integrating in period Tint to simulate the photo-charge transfer from photodiode to floating diffusion node. Here we use different photocurrents (Iphoto2=100fA, Iphoto3=1pA, Iphoto4=10pA, Iphoto5=20pA) integrating in the same period Tint (Tint=1.6μs) to simulate $1e^-$, $10e^-$, $100e^-$, $200e^-$ photo-charge transfers and compare them with the “no photo-charge” situation

(Iphoto1=0A, Tint=1.6μs). Figure 4.3 shows the pixel output signals with different photo-charge transfers in one pixel cycle (130μs, from 260μs to 390μs).

And this work is designed for very low light applications, for example, the astronomic telescope. The maximum detection range of the pixel is smaller than 200 electrons.

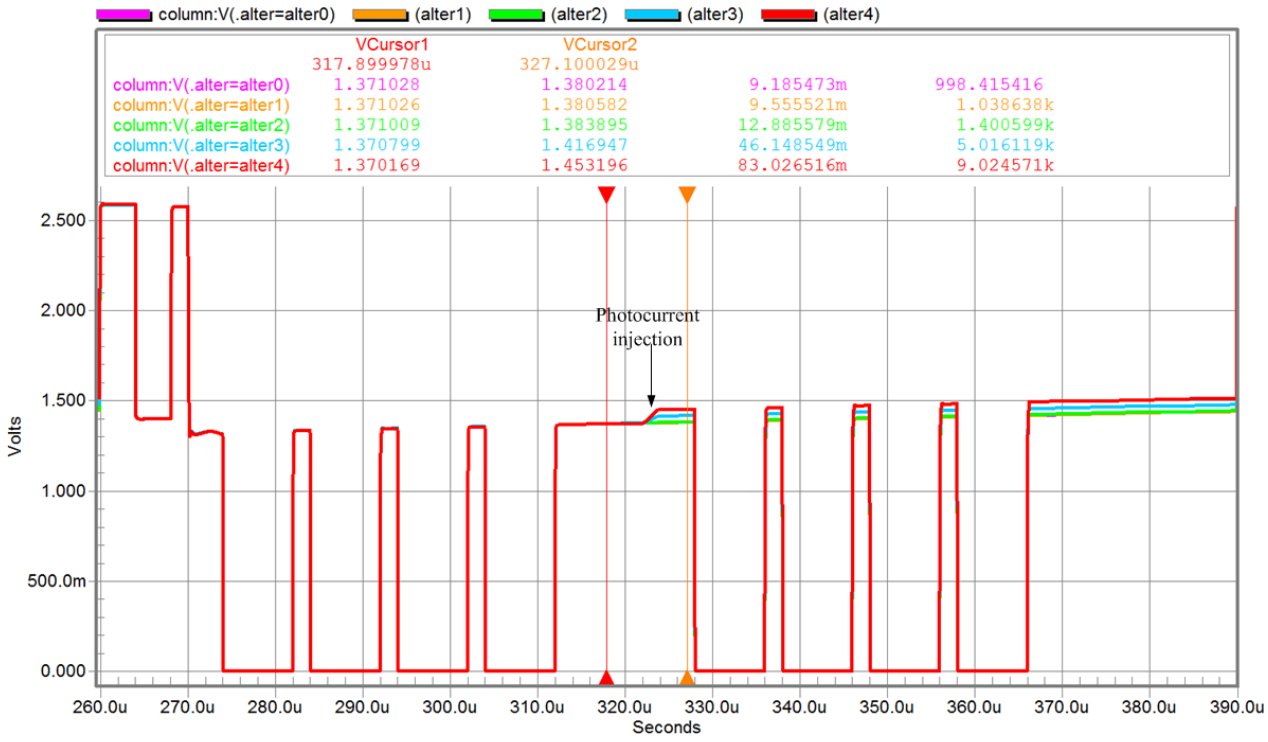


Figure 4.3 The pixel output signals with different photo-charge transfers in one pixel cycle. The purple trace: the pixel output signal with 0e$^-$ transfer, orange trace: the pixel output signal with 1e$^-$ transfer, green trace: the pixel output signal with 10e$^-$ transfer, blue trace: the pixel output signal with 100e$^-$ transfer, red trace: the pixel output signal with 200e$^-$ transfer. The differences between these five traces are small, so we measure their values before and after photo-charge transfers (Iphoto injection), and show them in Table 4-1.

Table 4-1 Results and compare of pixel output signals with different photo-charge transfers

Situation	Qcharge (e$^-$)	Pixel output before Iphoto injection(V)	Pixel output after Iphoto injection(V)	Pixel output change (mV)*	Output difference (mV) *	Output difference per electron (mV)*
1	0	1.371028	1.380214	9.185473	--	--
2	1	1.371026	1.380582	9.555521	0.370	0.370
3	10	1.371009	1.383895	12.88558	3.700	0.370
4	100	1.370798	1.416947	46.14855	36.96	0.370
5	200	1.370169	1.453196	83.02652	73.84	0.369

*"Pixel output change" is the pixel output difference before and after photo-charge transfer. "Output difference" is the "Pixel output change" difference between this situation and the reference, situation 1. "Output difference per electron" is the "Output difference" over the number of transferred photo-charge.

From Table 4-1, we find the influence of a unit electron photo-charge on the pixel output signal is around 0.370mV. And through this simulation, we find two problems that need to be paid attention to: first, the leakage current of the transistors in the pixel because of the non-perfection of the SPICE models, the leakage current phenomenon is shown in Figure 4.4. The purple trace in Figure 4.4 is the pixel output signal with no photo-charge transfer. We find the pixel output voltage increasing slowly with time. Second, comparing the pixel output signals before photo-charge transfers in Table 4-1, we find there are some variations in these five situations, which may be caused by the signals in the previous period. Thus during system circuitry simulation, we need to consider the output range of pixel output signal, and use CDS technology to solve these problems.

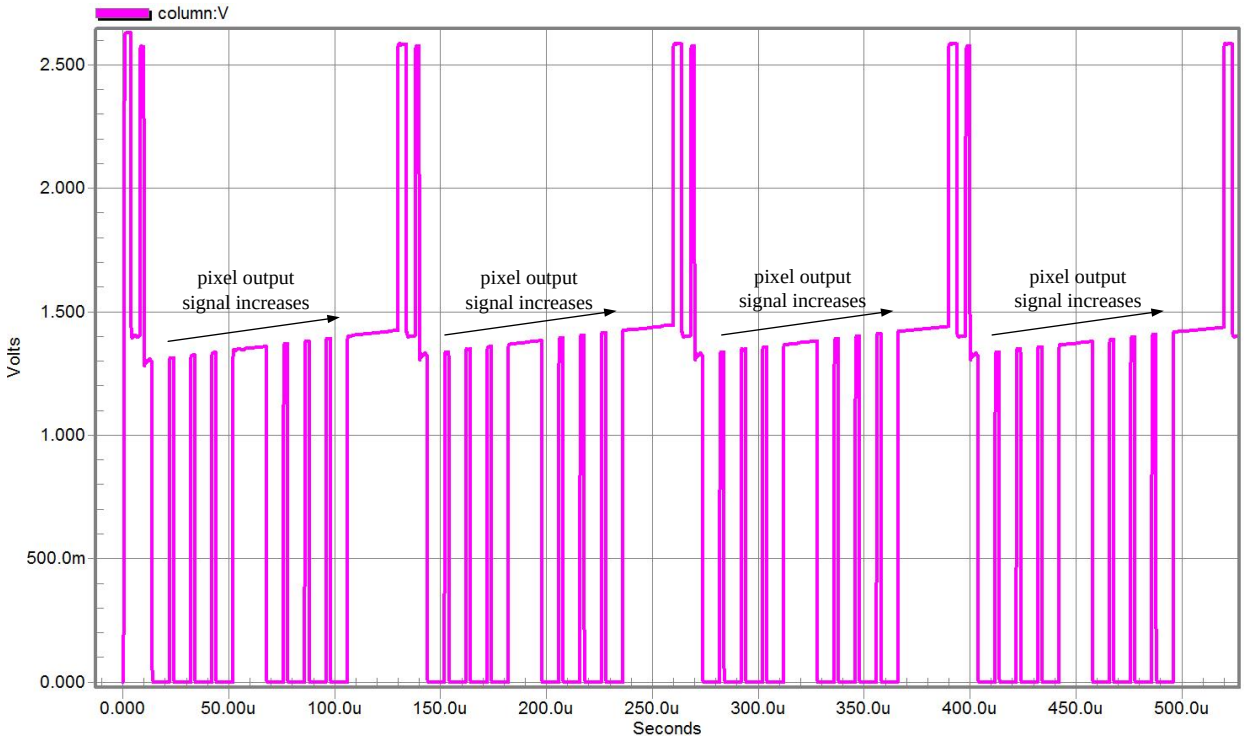


Figure 4.4 The pixel output signal with no photo-charge transfer in four cycles (0μs-520μs). We can see the increasing of pixel output signal with time in each cycle.

4.2 System simulation

The circuitry system includes the pixel array, the ADCs, the digital counters, the row and column decoders, which are shown in Figure 4.5.

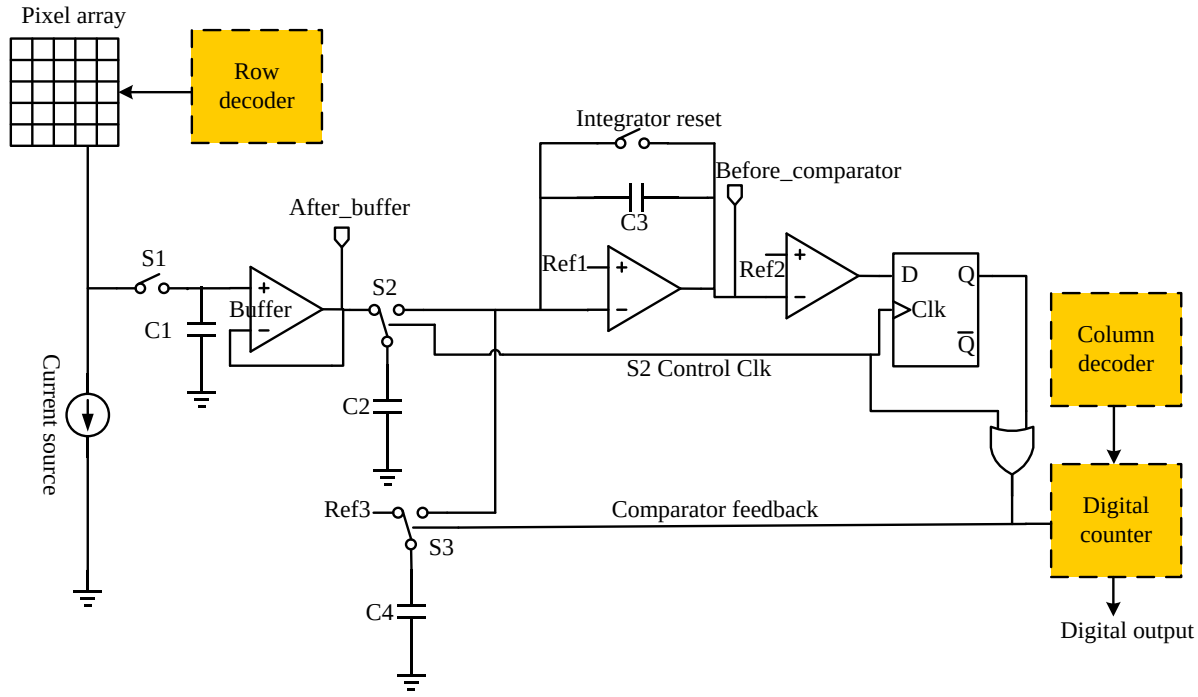


Figure 4.5 The diagram of the circuitry system

In the system simulation, we need to consider the integrator amplifier DC reference: Ref1, the two-stage amplifier in comparator DC reference: Ref2, and the comparator feedback DC reference: Ref3. As well as the ADC input signal Vin, and DAC reference signals Ref^{+}, Ref^{-}. As discussed in section 3.2.2. These voltages obey formulas (3-9) ~ (3-15).

Synthesizing these formulas and considering the leakage current, the variations of pixel output voltage problems described in the last section, we choose such circuitry setting data for the system simulation, which is shown in Table 4-2. And the system simulation assumptions and conditions are shown in Table 4-3.

Table 4-2 The circuitry setting data

VDDA (V)*	4.0	VDDD (V)*	3.3
Vcolumn (V)*	1.35~1.85	Vin (V)	-0.25~+0.25
Ref1 (V)	1.25	Ref^{+} (V)	1.6
Ref2 (V)	0.5	Ref^{-} (V)	0.55
Ref3 (V)	0.55		

*VDDA is the analog power supply, VDDD is the digital power supply and Vcolumn is the pixel output signal, which could be treated as the combination of the ADC input signal Vin and the DAC reference signal Ref^{+}.

Table 4-3 System simulation assumptions and conditions

Circuitry simulated	1 pixel in the full imager (1 pixel* and pixel biasing + ADC and ADC biasing + digital counter + decoders)

Simulator	Tanner S-spice and T-spice
Spice model	SPICE models of 0.18μm technology
Sequence simulated	4 frames; each frame is 130μs and divided into two halves (RESET and SIGNAL halves, using CDS technology); each half has 4 samples separated by 4 pMOS well voltage pulses; each pMOS well voltage pulse followed by 16 sigma-delta ADC oversamples

*In order to make the simulation time acceptable, we using one pixel instead of the whole pixel array to do the system simulation.

With the circuitry setting data, simulation assumptions and conditions, we can do the system simulation, the simulation results are shown in Figure 4.6~Figure 4.11.

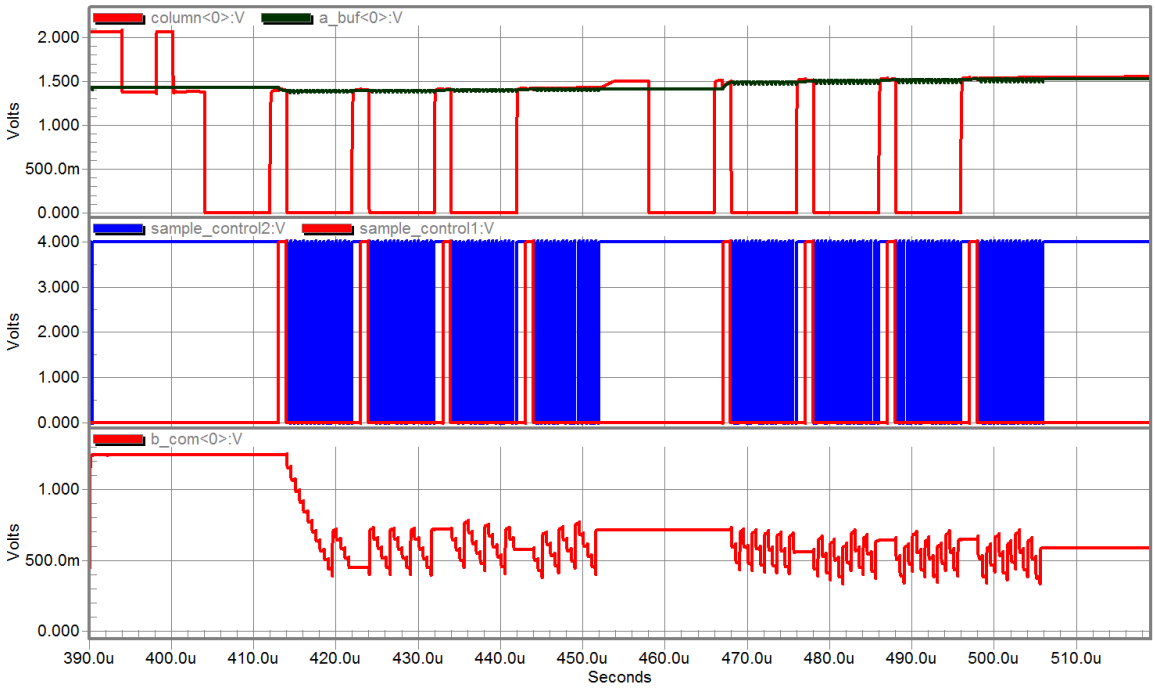


Figure 4.6 The system simulation results, viewing the S&H circuitry, in one frame (130μs, from 390μs to 520μs). Upper trace: red: the pixel output signal, black: the after S&H buffer signal. Middle trace: red: the S&H signal, blue: the sigma-delta ADC oversample signal, which is the S2 control signal in Figure 4.5. Lower trace: the integrator output signal

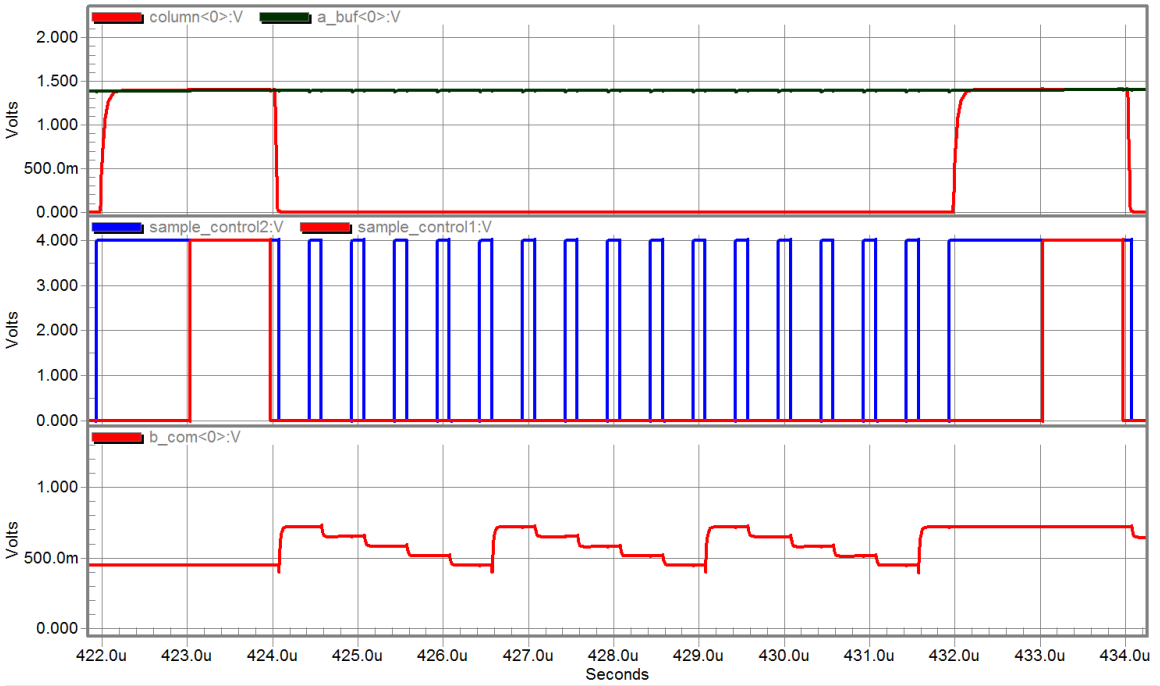


Figure 4.7 The enlarged view of Figure 4.6. Upper trace: red: the pixel output signal, black: the signal after S&H buffer. Middle trace: red: the S&H signal, blue: the sigma-delta ADC oversample signal. Lower trace: the integrator output signal. This period holds two pMOS well voltage pulses, and therein we have 16 sigma-delta ADC oversamples

The after S&H buffer signal samples the pixel output signal when the S&H signal pulse comes, and holds the value till the next S&H signal pulse. And at each falling edge of the sigma-delta ADC sample (the S2 control signal in Figure 4.5), charge on capacitor C2 (shown in Figure 4.5) transfers to the integrator capacitor C3, and causes the voltage drop of the integrator output; this is detailed shown in Figure 4.7, the enlarged view of Figure 4.6.

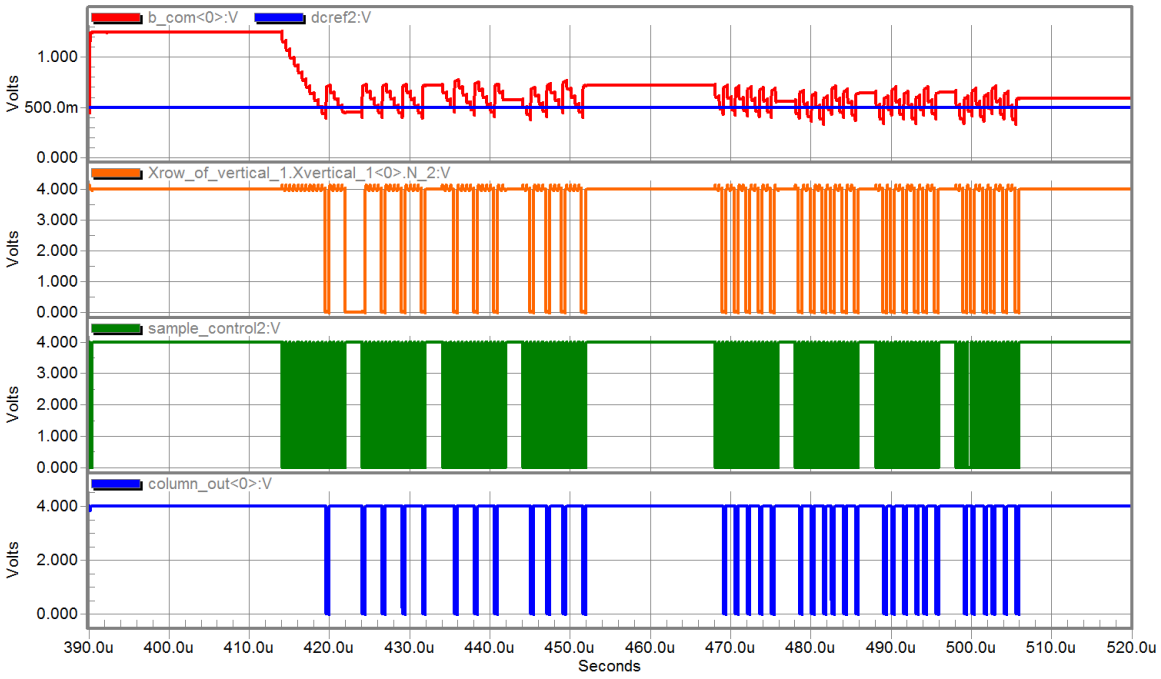


Figure 4.8 The system simulation results, viewing the comparator circuitry, in one frame (130µs, from 390µs to 520µs). First trace: red: the integrator output signal, blue: the DC reference of the two-stage amplifier in comparator: Ref2. Second trace: the D flip-flop output signal. Third trace: the sigma-delta ADC sample signal. Last trace: the comparator output signal

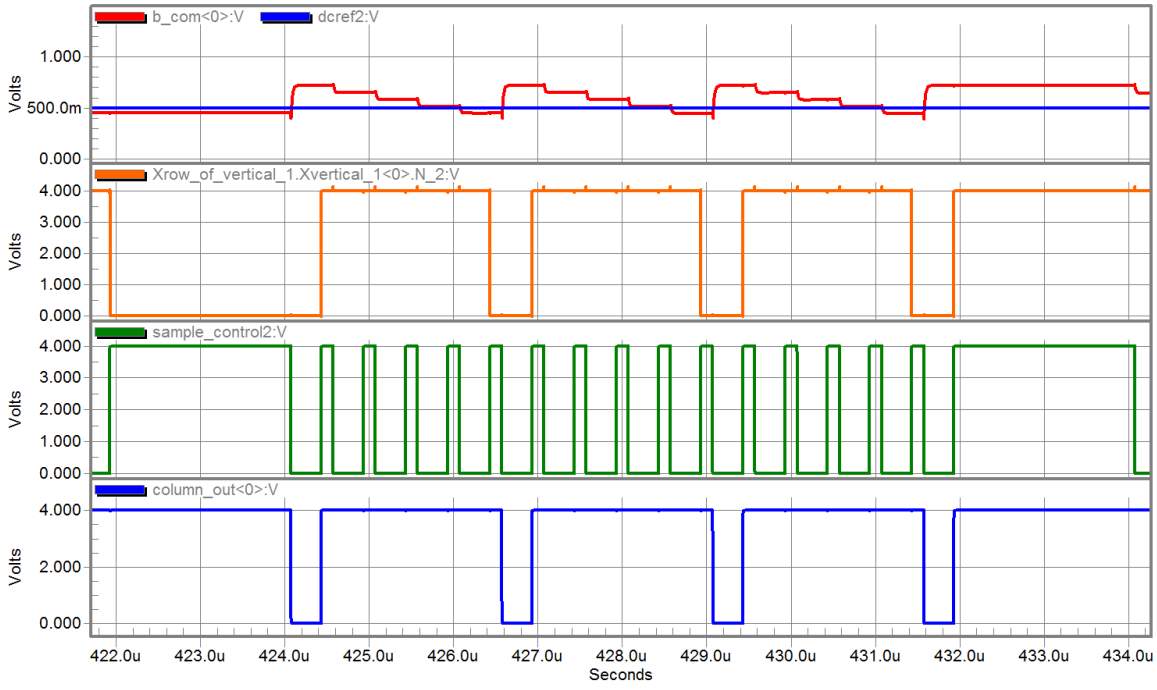


Figure 4.9 The enlarged view of Figure 4.8. First trace: red: the integrator output signal, blue: the DC reference of the two-stage amplifier in comparator: Ref2. Second trace: the D flip-flop output signal. Third trace: the sigma-delta ADC sample signal. Last trace: the comparator output signal. This period holds two pMOS well voltage pulses, and therein we have 16 sigma-delta ADC samples

In Figure 4.8 and Figure 4.9, we can see when the integrator output signal falls lower then Ref2, at the following rising edge of the S2 control signal (the sigma-delta ADC sample signal), the D flip-flop output signal falls down, and keep down for one S2 control clock period. And when the D flip-flop output signal falls down, at the next falling edge of the S2 control signal, the comparator output signal falls down as well, and then it rises up at the following rising edge of the S2 control signal. Because the comparator output signal is also the comparator feedback signal, the falling down of the comparator output signal causes a toggle of the integrator output. All those information is detailed shown in Figure 4.9, the enlarged view of Figure 4.8.

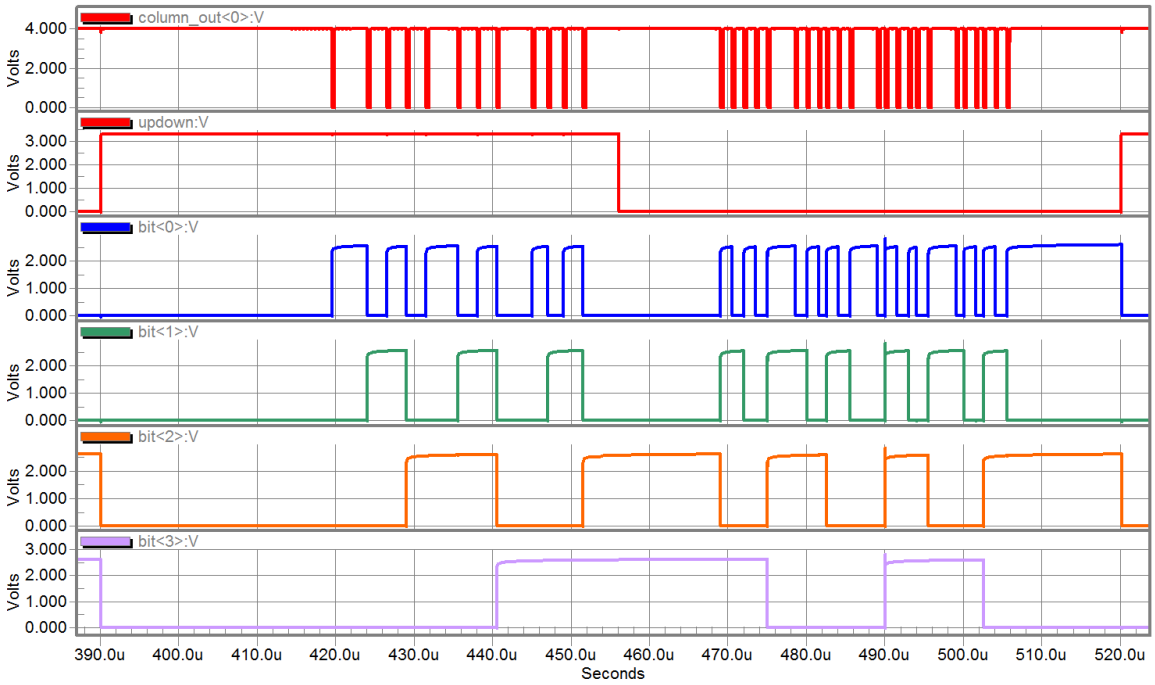


Figure 4.10 The system simulation results, viewing the digital counter circuitry, in one frame with 200 photo-charge transfer (130μs, from 390μs to 520μs). First trace: the comparator output signal. Second trace: the Up/Down control signal. Third trace: the lowest bit of digital counter output. Fourth trace: the second lowest bit of digital counter output. Fifth trace: the third lowest bit of digital counter output. Last trace: the fourth lowest bit of digital counter output.

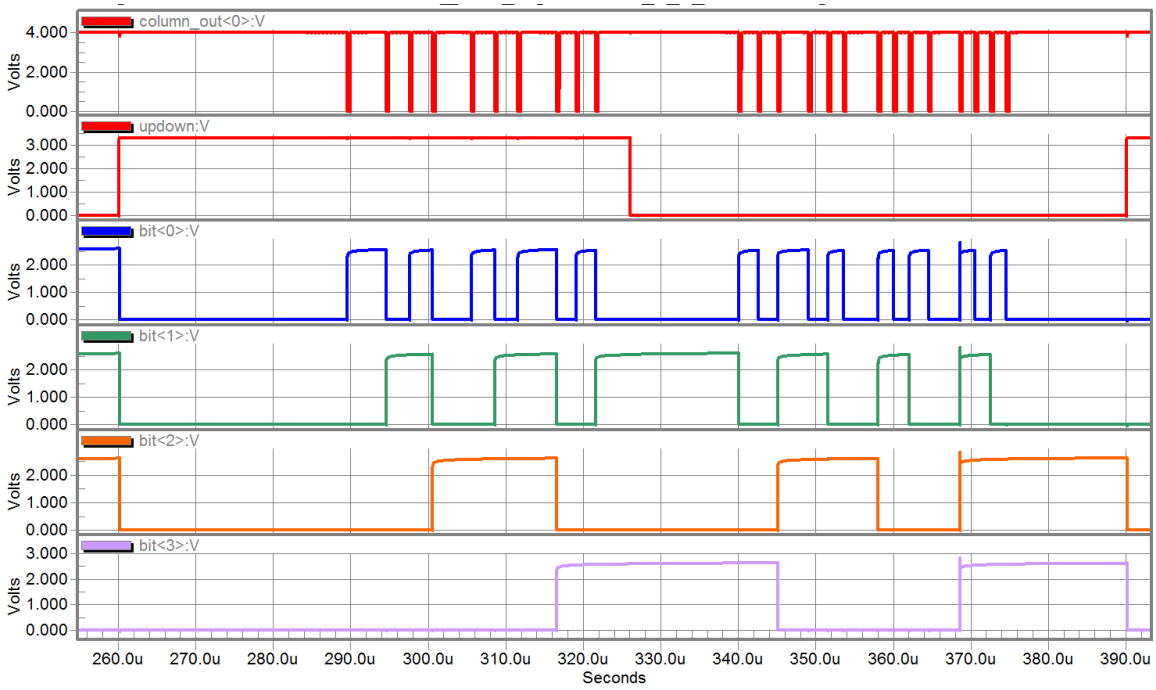


Figure 4.11 The system simulation results, viewing the digital counter circuitry, in one frame with 0 photo-charge transfer (130μs, from 260μs to 390μs). First trace: the comparator output signal. Second trace: the Up/Down control signal. Third trace: the lowest bit of digital counter output. Fourth trace: the second lowest bit of digital counter output. Fifth trace: the third lowest bit of digital counter output. Last trace: the fourth lowest bit of digital counter output.

In Figure 4.10 and Figure 4.11, we can see when the Up/Down control signal is high, at each falling edge of the comparator output signal, the digital counter output adds 1. As the Up/Down control signal becomes low, the digital counter output subtracts 1 at the falling edge of the comparator output signal. We keep the Up/Down control signal high at the beginning, and turn it to low after the photo-charge transfer. The final result of digital counter output maps to the number of photo-charge (Qcharge). For example, in Figure 4.10, the Qcharge is $200e^-$, at the end of the frame, the digital counter lowest 4 bits outputs are 0101, (so 1111,1111,1111,0101 in 16 bits) which mean "-11" in decimal domain. And in Figure 4.11, the Qcharge is $0e^-$, at the end of the frame, the digital counter lowest 4 bits outputs are 1100, (so 1111,1111,1111,1100 in 16 bits) which mean "-4" in decimal domain. So digital output "-11" maps to $200e^-$ photo-charge, and digital output "-4" maps to $0e^-$ photo-charge.

Of course, "-11" maps to $200e^-$, "-4" maps to $0e^-$, such resolution is not enough. This is due to the system simulation assumptions and conditions in Table 4-3. In the reality one, we will increase the sigma-delta ADC sample number to improve the resolution. At the same time, the increased the sigma-delta ADC sample number helps to decrease the quantization noise. In this design, we want to reach $0.5e^-$ RMS noise level, so the quantization noise of the

sigma-delta ADC should be smaller than 0.5e$^-$. The 1 bit first-order sigma-delta ADC obeys these formulas [4.1]:

$$\text{Noise } [V^2] = \frac{V_{LSB}{}^2}{12} * \frac{\pi^2}{3OSR^3} \tag{4-1}$$

$$\text{Signal } [V^2] = \frac{2^{2N} V_{LSB}{}^2}{8} \tag{4-2}$$

$$SNR_{\text{quantization}}\,[dB] = 10\log\left(\frac{9}{2\pi^2} 2^{2N} OSR^3\right)$$

$$SNR_{\text{quantization}}\,[dB] \approx -3 + 6*N + 9*\log_2(OSR) \tag{4-3}$$

where Noise is the total quantization noise power of the first order sigma-delta ADC; Signal is the total signal power of a sine wave; V_{LSB} is the least significant bit (LSB) voltage; OSR is the over sampling ratio; N is the number of bits in quantizer, in this design, N=1; $SNR_{\text{quantization}}$ is the signal-noise-ratio only considering the quantization noise.

The input range of the ADC is from 1.35 to 1.85V, and the influence of the unit electron photo-charge on pixel output signal is around 0.370mV. We know the quantization noise of the ADC should be less than 0.5e$^-$. So the least significant bit (LSB) of the ADC should be around 0.09mV, and its SNR could be calculated like this: (1.85V-1.35V)/0.09mV=5556, which is around 75dB. With formula (4-3), N=1 and SNR=75dB, we get the OSR is about 256, which means after each pMOS well voltage pulse, there should be 256 sigma-delta ADC samples.

4.3 Noise simulation

The output signals of this thesis system circuitry are digital signals, which cannot be used to do noise transient simulation. So we create a similar analog output circuitry, which is shown in Figure 4.12.

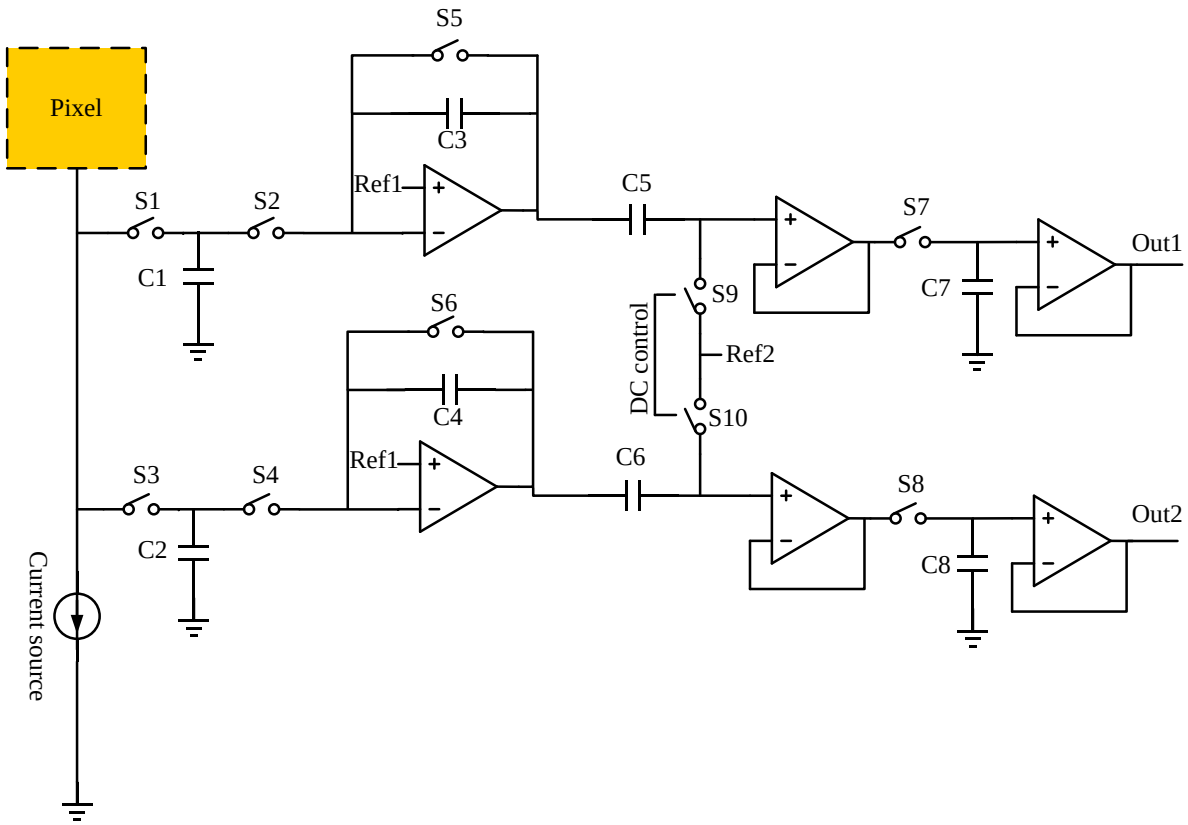


Figure 4.12 The analog output circuitry used for noise simulation

The whole circuitry could be separated into an upper and down two mirrored parts. In the upper part, the switch S1 samples the pixel output signal, and the signal is held by the capacitor C1. Then through the switch S2, the signal is integrated on the integrator capacitor C3. After four times of integrating, the switch S7 samples the integrator output signal, and stores it on C7. The down part has the same functions as the upper part except its switch S3 samples the pixel output signal after the photo-charge transfer. Switches S5 and S6 are used to reset the integrators; capacitors C5 and C6 are used for AC coupling. Switches S9 and S10 are applied to provide a proper DC voltage for the buffers. At last, we use Out2 to subtract from Out1 to realize correlated double sampling. The timing diagrams of switches in Figure 4.12 are shown in Figure 4.13

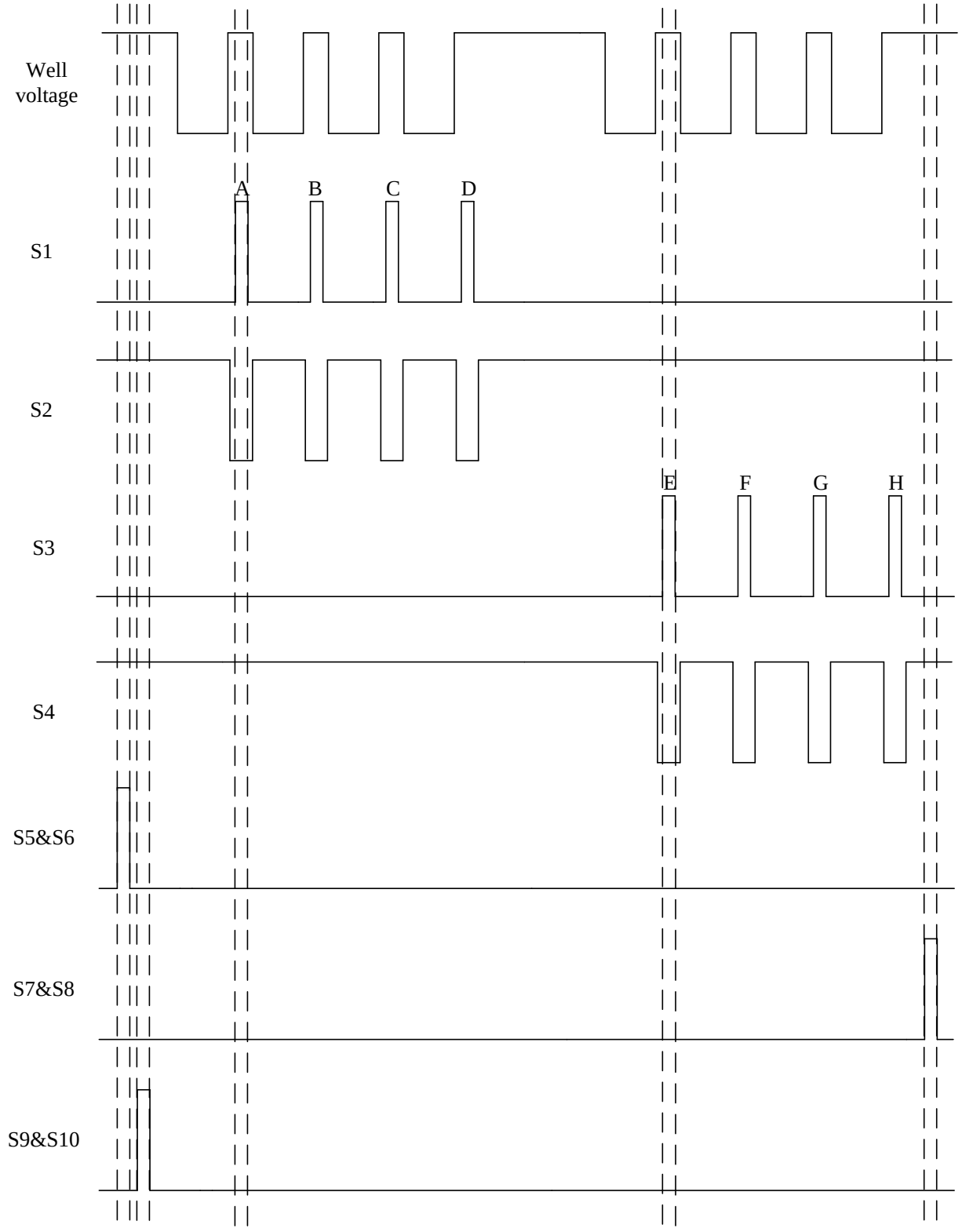


Figure 4.13 The timing diagrams of switches in Figure 4.12

The inputs and biasing of the pixel are the same as the pixel simulation setting in section 4.1.

Using noise transient simulations, we can measure the noise in the whole system. And we could fix the pixel output voltage to make the pixel noise free, and measure the readout circuitry noise. The noise simulation assumptions and conditions are shown in Table 4-4. And the noise simulation results are shown in Table 4-5.

Table 4-4 The noise simulation assumptions and conditions

Circuitry simulated	1 pixel + pixel biasing + S&H and integrator circuitry+ readout circuitry biasing
Simulator	Mentor ELDO
Spice model	SPICE models of 0.18μm technology. Separate 1/f and thermal noise simulations
Sequence simulated	Last frame of a sequence of 4; each frame is divided into two halves (RESET and SIGNAL halves); each half has 4 samples separated by 4 pMOS well voltage pulses. No ADC (oversampling) involved.

Table 4-5 The noise simulation results of different parts of the circuitry

	Whole circuit	Readout circuit	Pixel array*
RMS-Thermal(mV)	0.419	0.161	0.387
RMS-Thermal (e^-)*	1.13	0.435	1.05
RMS-1/f(mV)	0.274	0.071	0.265
RMS-1/f(e^-)*	0.741	0.192	0.716

*Pixel array noise is calculated by $\sqrt{Noise_{whole}^2 - Noise_{readout}^2}$; and one electron maps to 0.370mV pixel output signal.

From Table 4-5, we find the pixel thermal noise is around $1e^-$, and the flicker noise is around $0.7e^-$. We can see in the analog output circuitry used for noise simulation, the pixel output signal is integrated on the integrator capacitor directly after S&H without oversampling. While in the thesis work, we use sigma-delta ADC to oversample the after S&H buffer signal more than 200 times to decrease the ADC quantization noise and circuit thermal noise. So the real thermal noise in the thesis circuitry will nearly be completely cancelled. And in the Mentor ELDO noise transient simulation, the 1/f noise models do not include the effect of accumulation/inversion cycling. The results must thus be considered as a kind of "upper limit" of the target value.

With the knowledge of the noise mechanism discussed in section 3.1.2, we know that after accumulation/inversion cycling, the flicker noise in the sampled signal is becoming uncorrelated and could be decreased by oversampling. So the real 1/f noise in the thesis circuitry will also be much lower.

4.4 PCB test system

Figure 4.14 shows the structure of the PCB testing system. It includes power supplies providing power for the whole PCB, chip under test, external ADC for processing the pixel output signals in the case that the internal ADCs of the chip do not work, FPGA for decoding sequences and controlling chip, external ADC and processing chip, external ADC outputs, local memory for storing sequences from PC, PC for generating testing sequences.

The PCB is designed and manufactured by Caeleste system partners with my inputs.

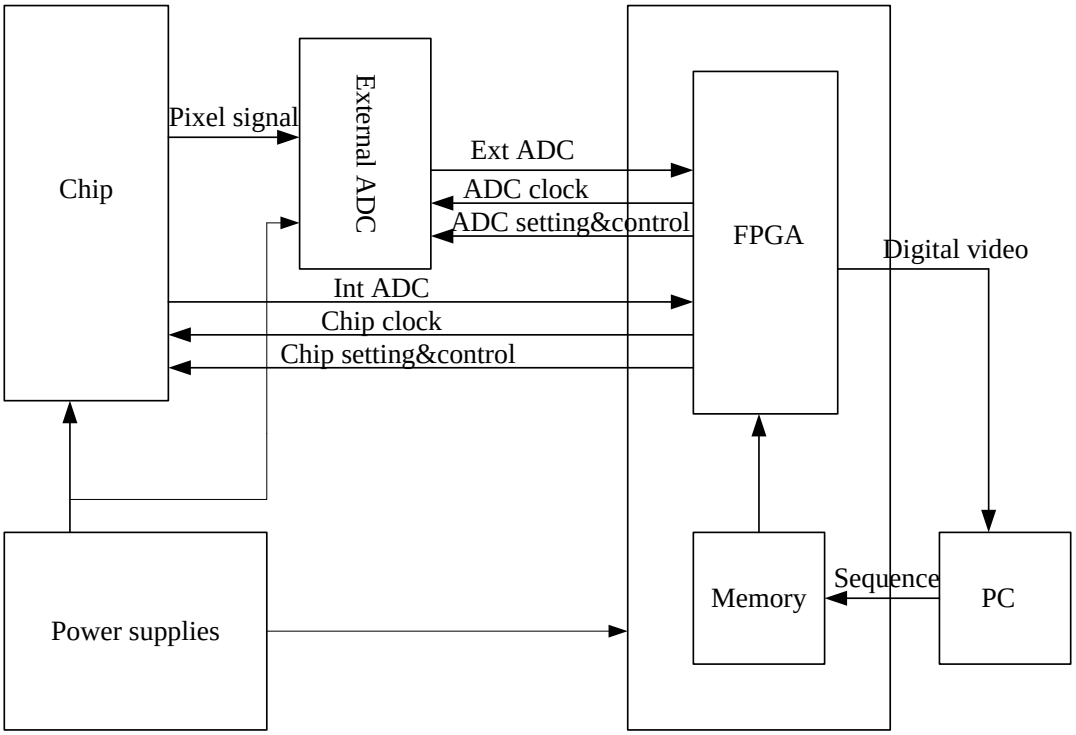


Figure 4.14 The structure of the PCB testing system

The operation principle is like this: first, offline, a PC program generates the test sequence and stores it in the local memory on the PCB. During operation, the FPGA reads the local memory and generates the controlling and clock signals for the chip and the external ADC. Then the chip and the external ADC operate their functions and give back their outputs to the FPGA. Finally, the FPGA processes these outputs and transfers the digital video to the PC.

The PCB schematic and layout are shown in Figure 4.15 and Figure 4.16. The PCB layout has 6 layers with the area of 150*150mm^2.

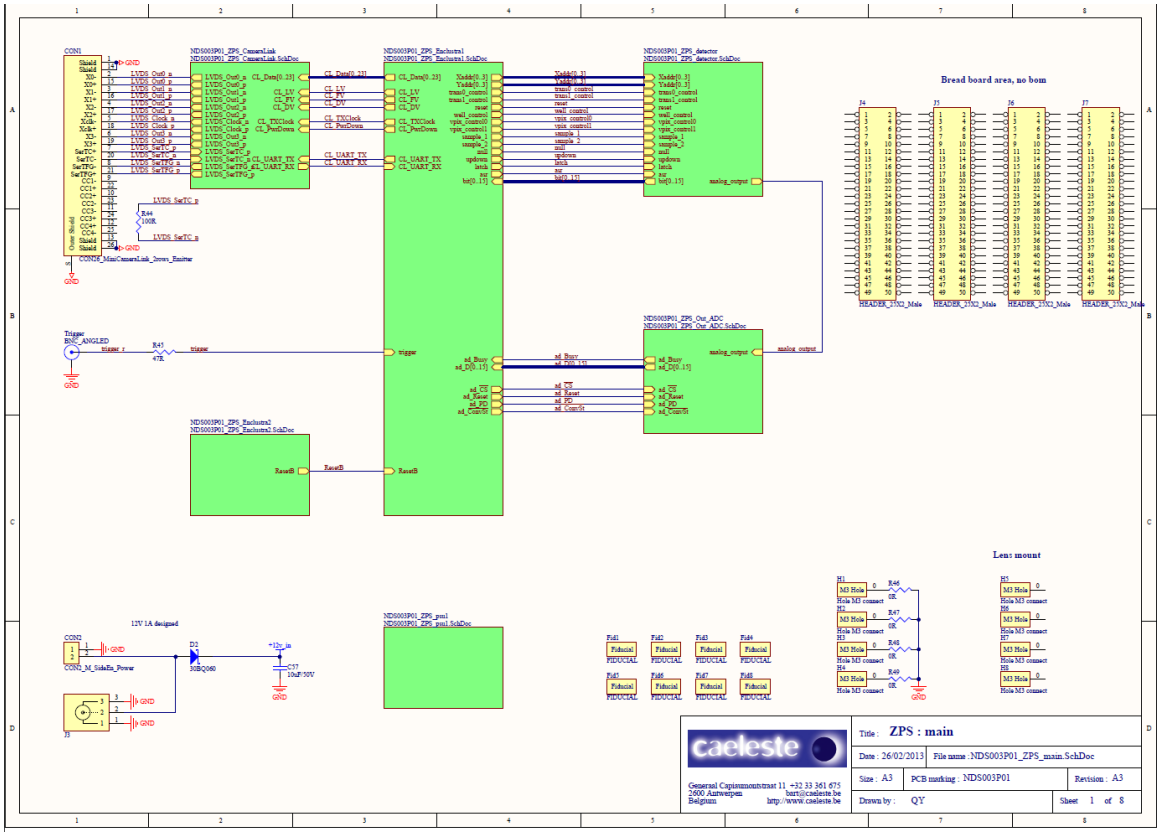


Figure 4.15 The PCB schematic

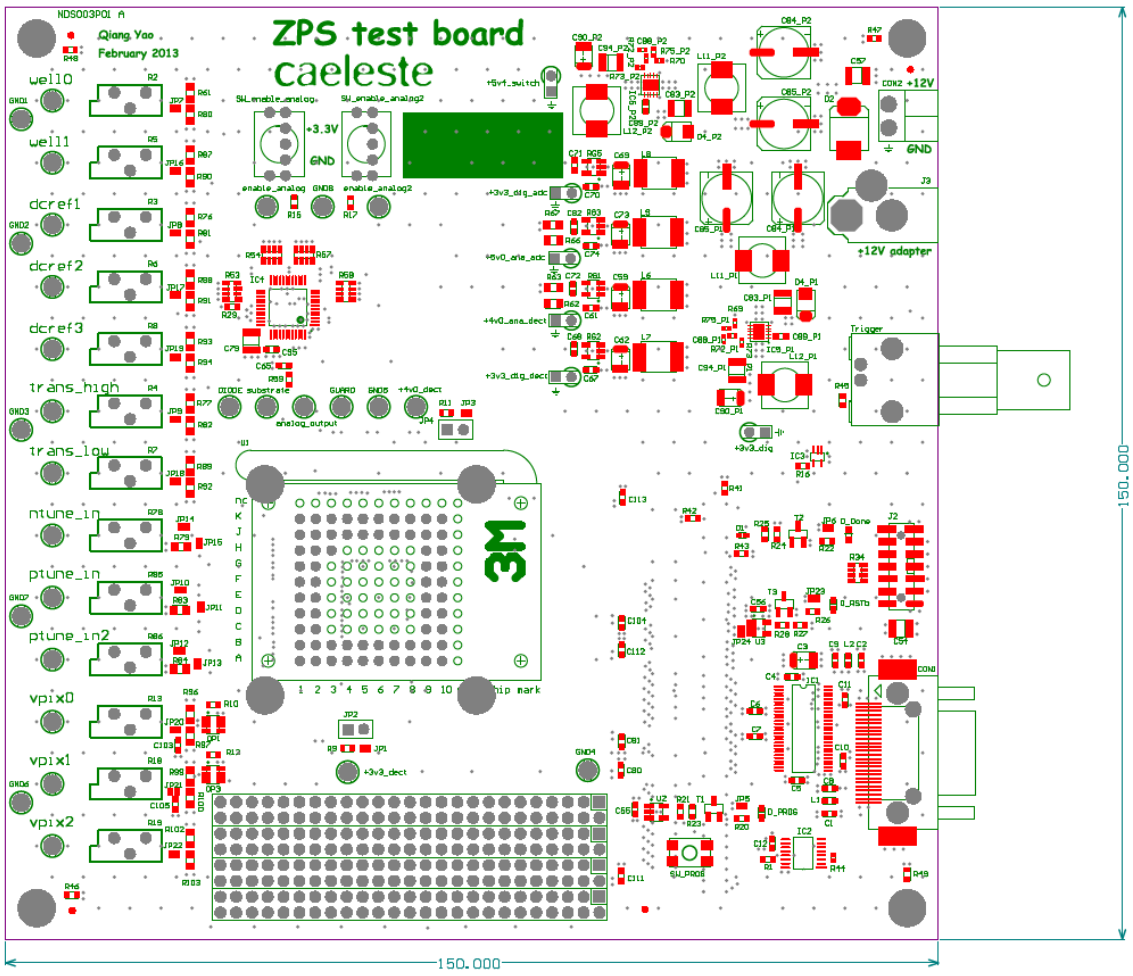


Figure 4.16 The PCB layout face side

The PCB test planning:

- May 2013: PCB test system is finished.
- Sept. 2013: ICs are expected to return from foundry and assembly.
- Sept. 2013: First silicon operation.

4.5 References

[4.1] M. Pelgrom, Analog to Digital Conversion. Springer Dordrecht Heidelberg London New York, 2010, pp185, 336.

Chapter 5 Conclusion

5.1 Contributions of this thesis work

During this thesis I and my colleagues at Caeleste designed a 16*16 pixels image sensor with a target 0.5 e^-_{RMS} noise in 0.18μm technology. The novelties of this design are:

- The novel 5T pinned photodiode pixel. The pMOS transistor well voltage is cycled between accumulation and inversion to make the flicker noise in the signal uncorrelated and allowing to be decreased by oversampling.
- The 1 bit first-order sigma-delta ADC with 75dB SNR to process the pixel output signal. It executes correlated double sampling (CDS), and oversampling to decrease most noise sources such as quantization noise and thermal noise.
- The 16 bit bidirectional digital counter realizes the output digitization.

My contributions where, amongst others:

- The major part of the schematic design and layout design of the 16*16 pixels imager.
- Extensive simulations of pixel, ADC and the whole circuitry.
- Verification using LVS and DRC.
- Making datasheet and part of the test plan.
- Part of the PCB schematic design and assistance during the whole PCB design.
- Making part of the test sequences generating program.

5.2 Future work

The design was taped out in May 2013. We expect the chip back in several months. The PCB test system is ready, and the test sequences for the test system are completed. We will test the chip when it comes back. And apart from the test work, there is potential future research:

- Firstly, Monte Carlo simulations on the pixel transistors. We would like to quantify the mismatch of the pMOS transistors in the pixel array and explore the methods to calibrate this mismatch.

- Secondly, in this work, we designed the 1-bit first-order sigma-delta ADC, and find that the required over sampling ratio (OSR) is large; we would like to apply other ADCs (2nd order ΣΔ) and explore alternative ADC concepts.
- Lastly, understanding the noise mechanism in micro-devices and explore additional and complementary methods to reduce the noise.