A 0.5e$^-_{rms}$ Temporal Noise CMOS Image Sensor With Gm-Cell-Based Pixel and Period-Controlled Variable Conversion Gain

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A 0.5e^-_{rms} Temporal-Noise CMOS Image Sensor with Charge-Domain CDS and Period-Controlled Variable Conversion-Gain

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***Abstract*— This paper introduces a proof-of-concept low-noise CMOS image sensor (CIS) intended for photon-starved imaging applications. The proposed architecture is based on a charge-sampling pixel featuring in-pixel amplification to reduce its input-referred noise. With the proposed technique, the structure realizes a period-controlled variable conversion factor at pixel-level. This enables the conversion factor and the noise-equivalent number of electrons to be tunable according to the application without any change in hardware. The obtained noise performance is comparable to the state-of-the-art low-noise CIS, while this work employs a simpler circuit, without suffering from dynamic range limitations. The device is fabricated in a low-cost, standard CIS process.**

I. INTRODUCTION

This paper introduces a proof-of-concept low-noise CMOS image sensor (CIS) intended for photon-starved imaging applications. The proposed architecture is based on a charge-sampling pixel featuring in-pixel amplification to reduce its input-referred noise. Compared to a fixed-gain in-pixel amplifier [1], the charge-sampling pixel realizes a variable-conversion-gain, overcoming the trade-off between input-referred noise, which benefits from high gain, and dynamic range (DR), which benefits from low gain. The pixel's gain is varied in a period-controlled manner which enables a compact layout, whose pitch (11 µm) is about 15× less than [2], which also employs a pixel-level variable-gain amplifier. Unlike previous low-noise CIS architectures [3-8], the charge-sampling pixel does not require the use of an advanced CIS technology, or a column-level amplifier and correlated multiple sampling (CMS). The new method simplifies the system and decreases the row read-out time. Measurement results show that the charge-sampling pixel effectively realizes a period-controlled conversion factor and achieves a 0.5 e^-_{rms} temporal noise level within a 10 µs row read-out time.

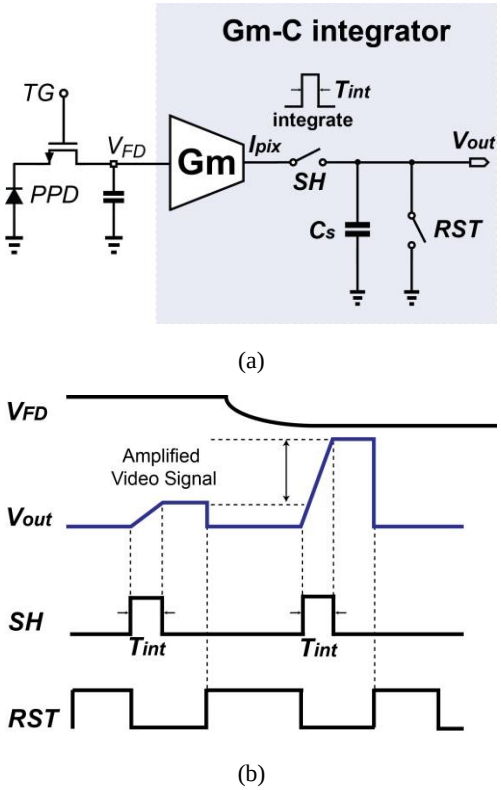

Fig. 1 Charge-sampling pixel (a) architecture (b) timing diagram.

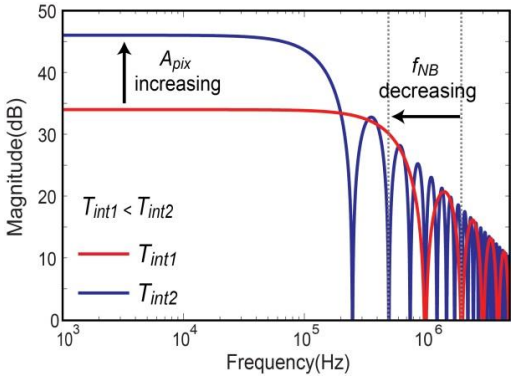

Fig.2 Transfer function of the charge-sampler

II. Operating Principle

The operating principle of the charge-sampling pixel is shown in Fig. 1. The pixel consists of a pinned-photodiode (PPD) followed by a trans-conductance (Gm) cell, which, together with the sample-and-hold (S/H) capacitors, acts like a Gm-C integrator. Instead of using a source follower to buffer the voltage from the floating diffusion (FD) node onto the S/H capacitors, the proposed architecture first converts the FD node voltage V_{FD} into a current $I_{pix} = G_m V_{FD}$, where G_m is the trans-conductance of the Gm-cell. This current is then integrated on the S/H capacitors with capacitance C_s during a programmable time window T_{int}, at the end of which the resulting voltage can be sampled. This process is often referred to as charge-domain sampling.[9]. It effectively amplifies the voltage on the FD node with a period-controlled gain $A_{pix} = G_m T_{int}/C_s$. Furthermore, the integrate-and-sample operation realizes a 1st order sinc low-pass filtering response with the noise bandwidth of $f_{NB} = 1/2T_{int}$. As conceptually shown in Fig. 2, when A_{pix} increases, f_{NB} decreases, thus reducing wide-band noise in the same way as a 1st order low-pass filter realized by the source-follower-S/H capacitor combination present in a typical CIS. In addition, compared to a 1st order low-pass filter with the same f_{NB}, a 1st order sinc filter achieves better attenuation of high frequency noise thanks to the multiple notches appearing at a repetition rate of $f_s = 1/T_{int}$.

II. Sensor Implementation

The implementation details of the charge-sampling pixel in a CIS and the associated timing diagram are shown in Fig. 3. Similar to [4], the proposed architecture uses a common-source stage as a pixel-level Gm-cell. During the reset phase, with the help of a column-wise shared current source I_{col}, the reset level at the FD node and the DC operating point of the common-source transistor M_{cs} are defined in a self-biased manner by switching on the reset transistor M_{rst}. After that, the Gm-cell is configured as an open-loop amplifier by switching off M_{rst}. It then produces currents I_r and I_s, which are proportional to the reset level and the signal level, before and after the charge transfer from the PPD to the FD node, respectively. These two currents charge the CDS S/H capacitor banks during a period T_{int}. After CDS, a period-controlled amplified video signal is obtained with this CDS charge-sampling method. To enhance the overall linearity, the Gm-C integrator's time constant $(R_{o,Gm} \times (C_{S/H} + C_p))$ is designed to be much longer than $T_{int}/2\pi$, where $R_{o,Gm}$ is the output impedance of the Gm-cell, $C_{S/H}$ is the capacitance of the S/H capacitors and C_p is the parasitic capacitance of the column net. In order to boost $R_{o,Gm}$, an adequate gate voltage V_{cas} is applied during the row select state of the pixel, allowing M_{rs} to operate as a cascode transistor [1]. Also, a high-impedance current-source I_{col} is used as the load of the common-source stage. The design is implemented in a 0.18 µm 1P4M CIS process. A micrograph of the proof-of-concept die is shown in Fig. 4, with the main functional blocks highlighted.

III. Measurement

Fig. 5 shows the measured conversion factor $CG \times A_{pix}$ of the fabricated charge-sampling pixel, where CG is the conversion gain at FD node. To separately investigate the gain factor A_{pix} of the charge-sampling pixel, we also measure the CG of an unity-gain pMOS source follower (SF) based reference 4T-pixel as a comparison, in which the FD node is laid out with the same area as the proposed pixel. Note that the CG of the SF-based pixel is measured as 55µV/e^-, which indicates that the nominal value A_{pix} of the charge-sampling pixel is around 30. This is in good agreement with the simulated value of 32. The measurement results show that the pixel level conversion factor can be programmable from 90 µV/e^- to 1.6 mV/e^- with a charging period from 200 ns to 4 µs.

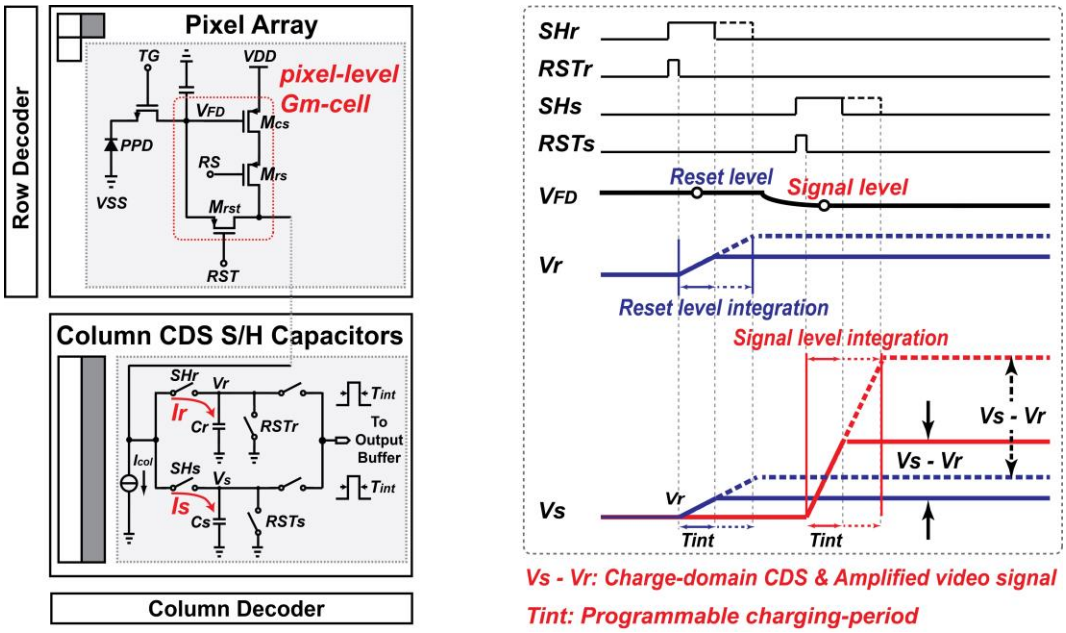

Fig.3 Circuit schematic and timing diagram of the charge-sampling pixel.

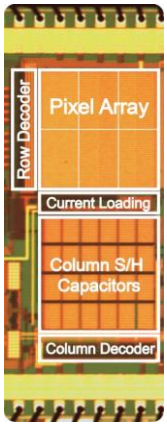

Fig.4 Microphotograph of the proposed CIS

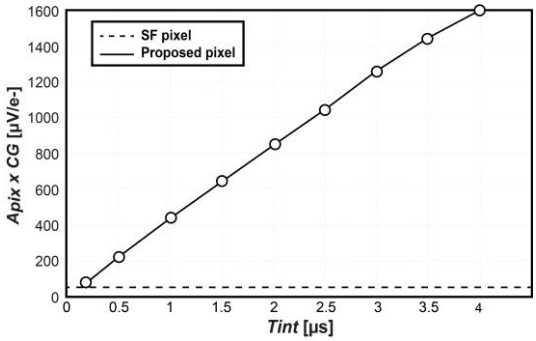

Fig. 5 Measured dynamic range of the charge sampling pixel as a function of the charging period T_{int}

Fig. 6 shows the measured input-referred noise of the proposed pixel as a function of T_{int}. The noise-reduction tendency initially is proportional to $1/T_{int}$ and later becomes proportional to $1/\sqrt{T_{int}}$. This result indicates that the charge-sampling pixel not only reduces the noise originating from the exceeding circuits connected at the back of the pixel, but also suppresses the thermal noise generated by the pixel-level circuit as a result of noise-bandwidth reduction. At T_{int} = 4 μs, the pixel achieves an input-referred noise of 0.51 e^-_{rms}. The inset of Fig. 7 shows the corresponding noise histogram.

Fig. 7 shows the DR as a function of T_{int}. The highest linear DR exceeds 68dB at T_{int} = 200 ns, and remains above 60dB at T_{int} = 4 μs. In addition to the single exposure linear DR, the proposed pixel provides a calculated potential linear dynamic range of 86dB using typical multiple exposure methods thanks to the embedding of an adjustable-gain function.

Tab.1 summarize the performance of the proposed charge-sampling pixel with comparison to the reported prior works on low-noise CIS. Our CIS achieves a noise level of 0.5 e^-_{rms} which is 1.4 to 1.7 times lower than the state-of-the-art with the conventional SF based pixel and the open-loop voltage amplification pixel.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

	This work	ISSCC'11[1]	ISSCC'12 [5]	VLSI'15 [6]	JSSC'16 [7]
Process	180nm CIS	180nm CIS	180nm CIS	180nm CIS	180nm CIS
Pixel size [μm^2]	11×11	11×11	10×10	5.5×5.5	6.5×6.5
Fill factor [%]	50	50	33	---	40
Temporal read-out noise [e^-_{rms}]	0.5	0.86	0.7	0.5	0.48
CG (or CF) [$\mu V/e^-$]	90~1600	300	45	240	160
Row read-out time [µs]	10	15	1600	143	25

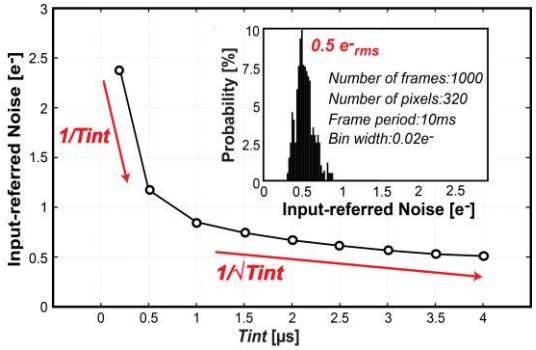

Fig. 6 Measured input-referred noise of the charge sampling pixel as a function of the charging period T_{int}, and the noise histogram at T_{int} = 4 µs.

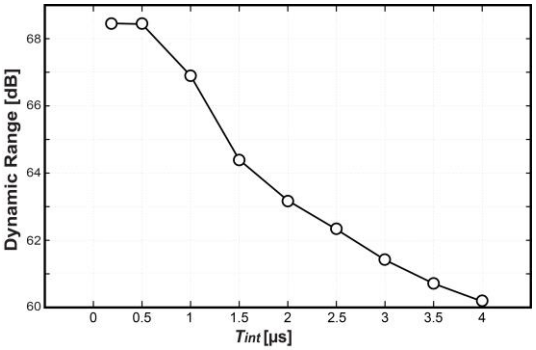

Fig. 7 Measured dynamic range of the charge sampling pixel as a function of the charging period T_{int}.

IV. CONCLUTION

A CIS targeted for low noise applications has been presented in this paper. With the proposed technique, the structure realizes the period-controlled variable conversion gain at pixel-level. This enables the conversion gain and the noise-equivalent number of electrons to be tuneable according to the application without any change in hardware. The obtained noise performance is comparable to the state-of-the-art low-noise CIS, while this work employs a simpler circuit, without suffering from dynamic range limitations, and is fabricated in a low-cost, standard CIS process.

ACKNOWLEDGMENT

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