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Optical MEMS die-attach warpage analysis and mitigation via thermoelastic modeling and in-situ micro-Raman spectroscopy characterization

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ABSTRACT

Optical micro-electromechanical systems (MEMS) demand exceptional precision, yet warpage during the die attach process on printed circuit boards can compromise performance. Here, a three-dimensional thermoelastic analytical model has been developed based on Fourier heat conduction and supported beam theory. This model facilitates the in-situ calibration of solder parameters via confocal micro-Raman spectroscopy, ensuring that the simulated dynamic evolution of warpage during soldering aligns closely with digital image correlation experiments. The results show consistence with Finite Element Method with error less than 1 % and time saving more than 60 %. Orthogonal experimental analysis further reveals that substrate thickness and thermal expansion coefficient variations are the primary factors affecting warpage, while chip area has a negligible role. Given the practical challenges in reducing substrate thickness, a stress-balancing strategy incorporating an additional transition layer is proposed, which is effectively validated with a high-resolution three-dimensional profilometer. This work provides valuable insights into the predictive modeling and warpage behavior characterization, directly supporting improved mitigation strategies in the die attach process.

1. Introduction

Optical Micro-Electro-Mechanical Systems (MEMS) integrate MEMS technology with optical techniques, transforming conventional optics into “dynamic optics” and paving the way for intelligent optical systems [1]. Unlike electronic MEMS, optical MEMS demand significantly higher packaging precision [2]. Warpage resulting from thermal expansion coefficient (CTE) mismatch between materials is a persistent challenge throughout the lifecycle of MEMS devices. Fig. 1 shows the warpage results of two materials with different CTE. The stress generated at the connection between the two layers during temperature changes would pose a threat to reliability, such as cracking and peeling [3]. Dramatic temperature changes occur during both the application and manufacture processes. The high temperatures during the die attach process represent the first occasion that the chip faces thermal stress challenges. Previous studies have identified differences between adhesive materials and chips as the main cause of such warpage [4,5]. The surface stress and warpage of the chip generated during the die attach process are detrimental to the subsequent packaging and application of the device.

Various analytical methods have been employed to assess temperature, stress, and strain distributions [6,7], including the transfer matrix method [8], finite difference method (FDM) [9], and finite element method (FEM) [10–12]. The analytical solutions can produce continuous output results and achieve high accuracy, but only effective for problems with well-defined boundary conditions. FDM and FEM are well-suited for solving complex thermo-mechanical models. The elastic–plastic torsion problems of prismatic bars with complex cross-sections could be solved through the generalized finite difference method (GFDM) [13]. By applying the Krylov Delay Correction (KDC) technique to accelerate meshless GFDM, the three-dimensional coupled thermoelastic problem can be solved efficiently and accurately [14]. FEM combined with mechanical theory, such as first-order beam theory,

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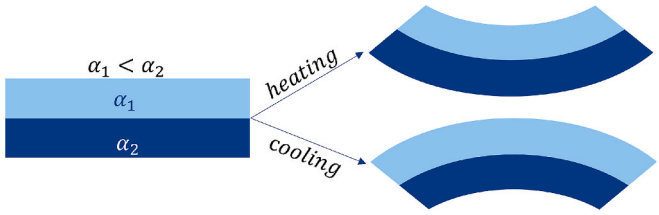

Fig. 1. Schemes of warpage caused by CTE mismatch.

can solve the complex porous problems [15]. However, FEM and FDM can accommodate such complexities but demand substantial computational resources and often introduce numerical errors when modeling continuous physical fields (such as stress and deformation).

Non-contact optical techniques are the primary experimental methods for measuring chip warpages [16,17]. Techniques such as Moiré fringe interferometry, optical interferometry (including Twyman-Green (TG), Fizeau (FIFI), and electronic speckle pattern interferometry (ESPI)), and laser scanning have been widely used [18–20]. Although Moiré fringe interferometry is popular, it faces challenges related to sample transparency and uniformity. TG provides high resolution but requires exceptionally flat surfaces, whereas FIFI has similar advantages yet is limited by sample size. Additionally, ESPI is highly sensitive to ambient lighting conditions [21–23]. Laser profilometry, which scans surfaces with a laser to measure warpage, is constrained by scanning time, signal acquisition accuracy, and spatial resolution [24]. Moreover, the demands of chip miniaturization and high-density integration, along with limited response speeds, further hinder high-frequency, real-time data acquisition.

To address these challenges, we construct a predictive model based on thermoelastic theory that considers warpage in multilayer structures (comprising the chip, solder layer, and substrate) during MEMS chip mounting. This continuous thermoelastic model accurately delineates thermal deformation and stress distribution across each layer. In this study, in-situ confocal micro-Raman spectroscopy is integrated for monitoring the solder state, while digital image correlation (DIC) facilitates real-time tracking of warpage. The proposed model reliably predicts warpage evolution, as validated by experimental results. Furthermore, an orthogonal experimental design highlights substrate thickness and thermal expansion mismatches are the primary factors influencing warpage, while chip thickness is a secondary factor and chip area has minimal impact. Considering the practical challenges of reducing substrate thickness, a stress-balancing transition layer is introduced and its effectiveness is confirmed through high-resolution three-dimensional (3D) profilometry. Overall, these findings provide a systematic approach to warpage prediction and control, contributing to process optimization and enhanced device reliability.

2. Analytical modeling and parameter calibration

2.1. 3D thermoelastic modeling for laminated structures

During reflow soldering, rapid temperature changes are the primary cause of warpage. The die-attach process can be simplified as a three-layer structure, as shown in Fig. 2(a). A coordinate system is established at the bottom surface of the substrate, with mechanically constrained regions indicated by shaded areas. The temperatures at the top and bottom surfaces of the laminated packaging are set as T (x, y), which is consistent with the thermal profile shown in Fig. 2(b).

Considering that the thickness of the entire structure is much smaller than its length and width, heat dissipation from the four walls is neglected. For laminated structures composed of different materials, we rigorously enforce continuity of both temperature and its gradients across the interfaces. Therefore, the analytical temperature description can be expressed as follows:

$$\begin{aligned} T(x,y,z) = A_0 + B_0 z + \sum_{m=1}^{\infty} cos(\lambda x)[A_1 cosh(\lambda z) + B_1 sinh(\lambda z)] \\ + \sum_{n=1}^{\infty} cos(\delta y)[A_2 cosh(\delta z) + B_2 sinh(\delta z)] \\ + \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} cos(\lambda x) cos(\delta y)[A_3 cosh(\beta z) + B_3 sinh(\beta z)] + T_{air} \end{aligned} \tag{1}$$

where, A_i (i = 0, 1, 2, 3) and B_i (i = 0, 1, 2, 3) are the coefficients determined by the boundary conditions.

The integrated mathematical framework that combines thermal conduction with thermal stress analysis is presented in Fig. 3. The modeling process begins with the establishment of a 3D temperature distribution. By applying the Fourier transform, complex spatial thermal conduction equations are converted into simpler frequency-domain computations, effectively reducing the dimensionality of the problem. This approach illustrates the heat flow through materials with varying temperatures, and the heat transfer which causes materials to expand or contract, ultimately leading to stress.

To analyze the mechanical behavior of the i-th layer with thickness ($h^{(i)}$) and CTE ($\alpha^{(i)}$), the temperature difference is ΔT. $G^{(i)}$ is the shear modulus, and $\lambda^{(i)}$ is the Lame constant. δ_{ij} is the Kronecker delta. The length and width of the structure are a and b. The normal stress is $\sigma_{ij}^{(i)}$. The displacements (u, v, w) in tensor form is $u_i^{(i)}$. The constitutive equation in tensor form is as follows:

$$\sigma_{ij}^{(i)} = \mu^{(i)}(u_{i,j}^{(i)} + u_{j,i}^{(i)}) + [\lambda^{(i)} u_{k,k}^{(i)} - \alpha^{(i)}(3\lambda^{(i)} + 2\mu^{(i)})\Delta T]\delta_{ij} \tag{2}$$

where, $\mu^{(i)} = G^{(i)}$. Eq. (2) establishes a coupling model between the thermal field and mechanical stress, quantifying the deformation effects induced by thermal expansion of materials. According to linear thermal stress theory, the strain tensor components are linear functions of the stress tensor components and the strain tensor components generated by temperature variations. The stress tensor calculation mathematically characterizes internal material stresses, incorporating the coefficient of thermal expansion and reference temperature.

The thermal boundary conditions for the laminated plate are as follows:

$$\begin{aligned} T^{(i)}(0,y,\overline{z}) = T_i(a,y,\overline{z}) = 0 \\ T^{(i)}(x,0,\overline{z}) = T^{(i)}(x,b,\overline{z}) = 0 \end{aligned} \tag{3}$$

The following are the boundary conditions for a supported plate:

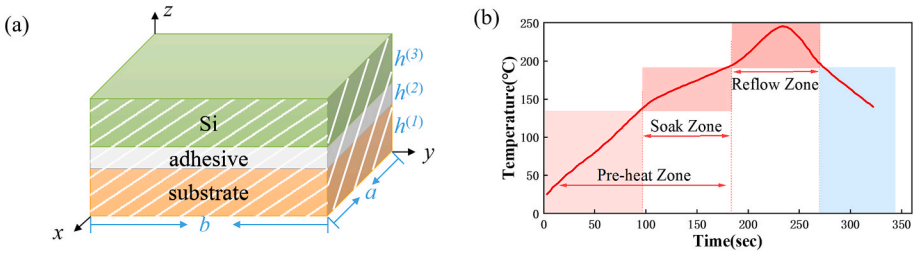

Fig. 2. MEMS modeling: (a) scheme; (b) thermal profile.

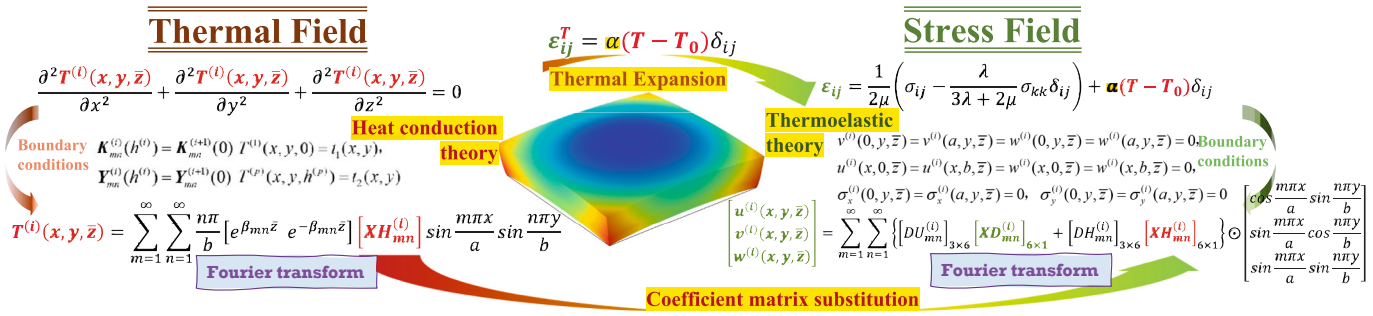

Fig. 3. Basic theoretical framework of the proposed thermoelastic prediction model.

$$\begin{aligned}
\sigma_x^{(i)}(0,y,\bar{z}) &= \sigma_x^{(i)}(a,y,\bar{z}) = 0,\\
\sigma_y^{(i)}(x,0,\bar{z}) &= \sigma_y^{(i)}(x,b,\bar{z}) = 0,\\
v^{(i)}(0,y,\bar{z}) = v^{(i)}(a,y,\bar{z}) &= w^{(i)}(0,y,\bar{z}) = w^{(i)}(a,y,\bar{z}) = 0,\\
u^{(i)}(x,0,\bar{z}) = u^{(i)}(x,b,\bar{z}) &= w^{(i)}(x,0,\bar{z}) = w^{(i)}(x,b,\bar{z}) = 0
\end{aligned} \tag{4}$$

To satisfy the boundary conditions above, the general solution for the displacement field of the i-th structure can be derived to be the following:

$$\begin{aligned}
u^{(i)}(x,y,\bar{z}) &= \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} U_{mn}^{(i)}(\bar{z})\cos\frac{m\pi x}{a}\sin\frac{n\pi y}{b},\\
v^{(i)}(x,y,\bar{z}) &= \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} V_{mn}^{(i)}(\bar{z})\sin\frac{m\pi x}{a}\cos\frac{n\pi y}{b},\\
w^{(i)}(x,y,\bar{z}) &= \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} W_{mn}^{(i)}(\bar{z})\sin\frac{m\pi x}{a}\sin\frac{n\pi y}{b}
\end{aligned} \tag{5}$$

where, $U_{mn}^{(i)}$, $V_{mn}^{(i)}$ and $W_{mn}^{(i)}$ are determined by mechanical boundary conditions and thermal coupling, jointly constituting the $[XH_{mn}^{(i)}]$ term in Fig. 3. $[XH_{mn}^{(i)}]$ characterizes the coupling between temperature and stress fields. The relationship between the displacement and stress on the upper and lower surfaces of the *i*-th layer can be expressed as:

$$\boldsymbol{Y}_{mn}^{(i)}(h^{(i)}) = \boldsymbol{D}_{mn}^{(i)}(h^{(i)})\left\{\boldsymbol{D}_{mn}^{(i)}(0)^{-1}\left[\boldsymbol{Y}_{mn}^{(i)}(0) - \boldsymbol{B}_{mn}^{(i)}(0)\right]\right\} + \boldsymbol{B}_{mn}^{(i)}(h^{(i)}) \tag{6}$$

Based on the continuity conditions between the laminated plates and using the matrix transmission method, the relationship between the displacement and stress on the surface can be obtained as follows:

$$\boldsymbol{Y}_{mn}^{(i)}(h^{(i)}) = \prod_{i=p}^{1}\boldsymbol{D}_{mn}^{(i)}(h^{(i)})\boldsymbol{D}_{mn}^{(i)}(0)^{-1} + [\boldsymbol{S}_{mn}]_{6\times 1} \tag{7}$$

$$\begin{aligned}
\boldsymbol{S}_{mn} = &-\sum_{j=1}^{p}\left\{\prod_{i=p}^{j}\left[\boldsymbol{D}_{mn}^{(i)}(h^{(i)})\boldsymbol{D}_{mn}^{(i)}(0)^{-1}\right]\right\}\boldsymbol{B}_{mn}^{(j)}(0) +\\
&\sum_{j=2}^{p}\left\{\prod_{i=p}^{j}\left[\boldsymbol{D}_{mn}^{(i)}(h^{(i)})\boldsymbol{D}_{mn}^{(i)}(0)^{-1}\right]\right\}\boldsymbol{B}_{mn}^{(j-1)}(h^{(j-1)}) + \boldsymbol{B}_{mn}^{(p)}(h^{(p)})
\end{aligned} \tag{8}$$

The above workflow demonstrates the integrated analysis from heat transfer modeling to thermal stress computation. These equations are compiled in MATLAB, allowing for specific and visualized deformation distribution results. The proposed model demonstrates less than 1 % deviation from FEM simulation when solving thermal-stress problems in a three-layer 3D structure (50 mm × 50 mm), achieving this accuracy with only 4,000 mesh elements – one-tenth the mesh density of FEM. The computation completes within 60 s, which is three times faster than the conventional FEM simulation. This framework significantly enhances warpage analysis efficiency for simple structures, offering rapid validation for structural configurations and material selections. This proposed method is applicable to electronics thermal management and mechanical thermal deformation analysis. Additionally, the model emphasizes cross-disciplinary coupling computation from temperature prediction to mechanical response.

2.2. Solder's thermal-mechanical parameter calibration with in-situ temperature-variable confocal micro-Raman test

Accurate material parameters are critical for reliable warpage predictions in thermomechanical simulations. In this study, the comprehensive mechanical parameters for the FR4 substrate were obtained from the manufacturer. A standard single-crystal silicon wafer (thinned and metallized to achieve the appropriate thickness) was used to simulate the MEMS chips. However, the solder layer introduces considerable uncertainty due to its dynamic phase change behavior during the die attach process. As temperature increases, the solder undergoes organic solvent volatilization (120–180 °C), flows in the molten state (above 183 °C), and subsequently solidifies upon cooling. The solder paste is described in Fig. 4(b) and (c). This nonlinear evolution results in markedly different thermomechanical responses before and after reflow, leading to variations in chip warpage under identical thermal conditions. Therefore, it is necessary to determine the thermomechanical parameters of solder in both its pre-reflow and post-reflow states.

To accurately calibrate the solder's thermal–mechanical parameters [25,26], three samples were selected for testing. The sample size was 15 mm × 15 mm, and the chip thickness was 475 μm. The thickness of the FR4 substrate was 800 μm [27,28]. The control group was a single-layer chip sample. The second sample was the chip interconnected with the substrate through solder paste before reflow. The third sample was the sandwich structure after reflow. In-situ calibration was performed using confocal micro-Raman spectroscopy, a non-contact, non-destructive technique that rapidly detects stress and strain via inelastic photon-phonon scattering. By correlating shifts in the Raman peaks of the single-crystal silicon lattice with local stress and strain, submicron spatial resolution was achieved in mapping chip surface deformation, as shown in Fig. 4(a).

To minimize potential damage to the Raman equipment from organic volatilization, experimental temperatures were limited to 100 °C. Initially, a thermal expansion calibration (25–100 °C) on the control group was conducted to isolate its intrinsic thermal expansion effect on the Raman spectrum. Subsequently, a sandwich structure preloaded with solder paste was subjected to a gradient temperature test, with Raman measurements performed at 50 °C and 100 °C. The wavelength of the Raman laser was selected as to be 532 nm. The results indicated that the pre-reflow warpage of the silicon wafer was −9.4 μm at (50 °C) and −13.1 μm (100 °C), while post-reflow curing yielded warpage values of −11.5 μm (50 °C) and −13.6 μm (100 °C). Although previous studies have shown that solder properties such as Young's modulus and CTE can vary with temperature, the variation range is typically within a 20 % range under consistent morphology. Therefore, the calibration here focuses solely on pre- and post-reflow conditions to ensure consistency between theoretical predictions and experimental measurements.

By fine-tuning the solder parameters within our thermoelastic model, the simulation results closely matched the experimental data. Further validation was achieved using a 3D thermoelastic FEM

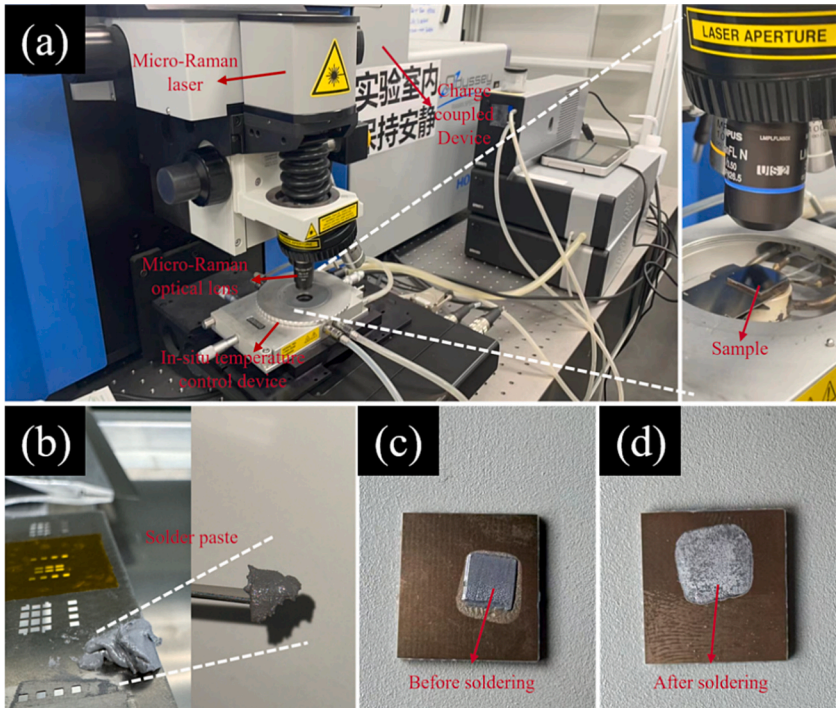

Fig. 4. In-situ temperature-variable confocal micro-Raman test and the state of solder paste before and after curing: (a) Schematic diagram of in-situ temperature-variable Raman test; (b) solder paste; the state of solder paste (c) before and (d) after soldering.

implemented in ANSYS with the same sandwich structure and material parameters (Table 1). As shown in Fig. 5, the FEM outcomes nearly coincided with those predicted by the analytical model, demonstrating engineering-level accuracy while requiring only one-third of the computational time compared to conventional FEM simulations. The positive warpage value indicates convex deformation (chip edges curl downward), while the negative warpage denotes concave deformation (chip center sinks downward). Both the Raman experimental results and the model predictions consistently exhibited concave warpage morphology, and the observed differences across temperatures and solder states confirm that the proposed model reliably captures both the form and the evolving trend of warpage. Minor discrepancies are attributed to measurement uncertainties and challenges in precisely characterizing the evolving state of the solder paste.

3. Warpage mapping and mitigation

To validate the accuracy of the proposed model and identify critical parameters affecting warpage, we conducted a series of experiments using bare silicon dies and PCB substrates.

3.1. DIC warpage measuring during the die-attach process

To further assess the model's ability to characterize warpage during reflow soldering, we employed DIC for real-time monitoring. DIC technology combines digital speckle projection and stereoscopic vision techniques to measure the 3D coordinates, displacement, and strain of an object's surface. Binocular cameras captured speckle patterns on the device surface, enabling deformation profiling via analysis of inter-camera image disparities (schematically shown in Fig. 6). Since the testing environment was open and the distance between the cameras and the sample was relatively large (>500 mm), the system was not affected by volatile organic compounds. This setup enabled warpage measurement of the chip throughout the reflow soldering process at temperatures up to 250 °C. The test sample had dimensions of 15 mm × 15 mm, with a chip thickness of 475 μm and a PCB substrate thickness of 800 μm.

In the experiment, the pre-reflow sample was placed on a

Table 1
Materials properties of MEMS die attach structure.

Materials	Properties				FEM model geometry	
	E (GPa)	Poisson's ratio	CTE (ppm/℃)	Thermal conductivity (W/m·K)	Thickness (μm)	Size (mm × mm)
Die:						
Si	190	0.28	4.1	124	475	15*15
Adhesive:						
Solder (before)	11.5	0.45	25	5	100	15*15
Solder (after)	40	0.3	15	70	100	15*15
Substrate:						
Al	60	0.34	23	8		
Fr4	16	0.13	13	0.3	800	15*15
Cu	110	0.34	18	401		

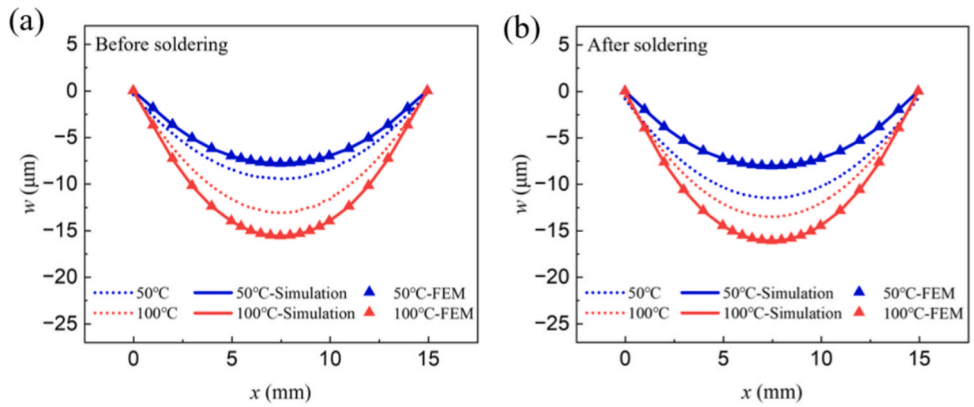

Fig. 5. The warpage state (diagonal direction) of the chip before and after soldering and the model prediction: (a) before soldering; (b) after soldering.

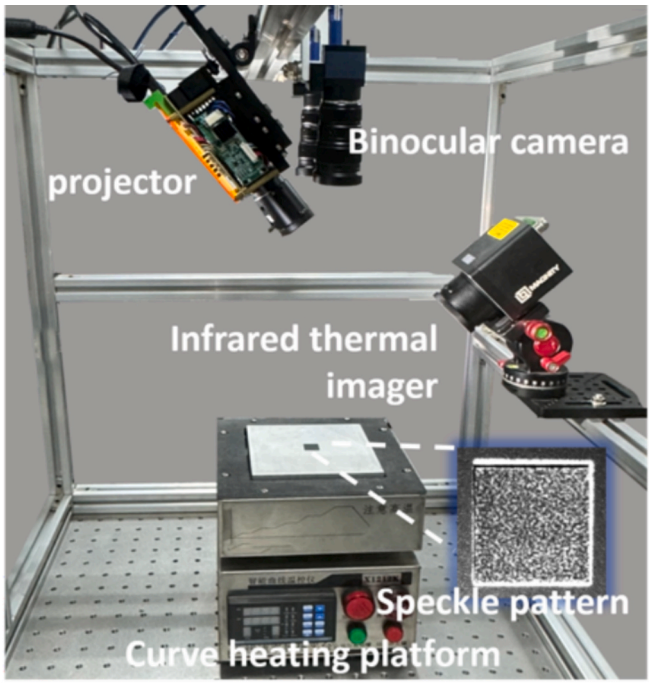

Fig. 6. Schematic diagram of the in-situ DIC monitoring equipment structure and reflow temperature curve settings.

temperature-controlled heating platform programmed with the heating profile illustrated in Fig. 2(b) to simulate the actual die-attach reflow soldering process. Surface warpage was recorded at various temperatures as shown in Fig. 7. It was observed that the warpage performed differently at the same temperature during the heating and cooling process. Additionally, the samples during the cooling process were more convex compared to when they were being heated. During the heating phase (25–160 °C), the larger CTE of the PCB substrate caused significant expansion, leading to concave deformation. Conversely, during the cooling phase following solder solidification, differential shrinkage between the silicon wafer and the substrate resulted in a gradual transition to convex warpage. Notably, the phase transition of the solder contributed to greater warpage during cooling compared to heating at equivalent temperatures. While the DIC system captured the surface morphology changes of the chip, dynamic variations of the side-view were also observed and recorded throughout the reflow process. Transient chip floating was detected during the brief solder-melting period, which may explain some discrepancies between the simulation and experimental results. Ultimately, the final chip warpage at room temperature was measured at 22 μm.

The solder layer data, calibrated via in-situ Raman measurements, was incorporated into the thermoelastic model. Using the same temperature profile and taking the initial room-temperature chip warpage as a baseline, the displacement in the Z-direction at the chip center was tracked. As shown in Fig. 8, the chip exhibited concave warpage, reaching –36.018 μm at 250 °C (without considering the effect of solder melting). And the warpage data at the same temperature also shows the differences between the cooling process and the heating process. Warpage during the cooling stage is more sensitive to temperature compared to the heating process. Upon cooling back to room temperature, the warpage transitioned from concave to convex, with a final value of 11.749 μm. This comparison further validates the predictive capability of the thermoelastic model in describing the dynamic warpage evolution of the chip during the reflow soldering process.

3.2. Structural factors affecting warpage

The thickness and material properties of each layer in the sandwich structure critically influence warpage. The chip material is single-crystal silicon. The solder layer thickness is determined by the stencil, and the parameters follow the calibrated values mentioned above, making the solder layer parameters fixed. This study systematically investigates the effects of die thickness, chip area, substrate thickness, and substrate material on post-die-attach chip warpage. A four-factor orthogonal experimental design (Table 2) was employed to evaluate parameter interactions, with warpage computed using the proposed thermoelastic model.

Using classical laminated plate theory, the thermal stress–induced warpage can be approximately expressed as:

$$w \propto f(\Delta T, h_{Total}, \alpha) \tag{9}$$

where, $h_{Total} = h_{Si} + h_{Solder} + h_{Substrate}$.

To simplify the analysis, the equivalent CTE difference ($\Delta\alpha^*$) could be defined as:

$$\Delta\alpha^* = \alpha_{Substrate} - \left(\frac{h_{Si}\alpha_{Si} + h_{Solder}\alpha_{Solder}}{h_{Si} + h_{Solder}}\right) \tag{10}$$

With a fixed solder thickness of 100 μm, a multivariate linear regression was established to quantify the effects of chip thickness, chip area, substrate thickness, and $\Delta\alpha^*$ on warpage:

$$w = \beta_0 + \beta_1 h_{Si} + \beta_2 S_{Die} + \beta_3 h_{Substrate} + \beta_4 \Delta\alpha^* + \varepsilon \tag{11}$$

where, S_{Die} represents the chip area. β_1, β_2, β_3 and β_4 are the regression coefficients for various influencing factors. ε is the error term.

The regression results shown in Table 3 indicate that substrate thickness (accounting for 58.3 % of the effect) and $\Delta\alpha^*$ (29.2 %) are the

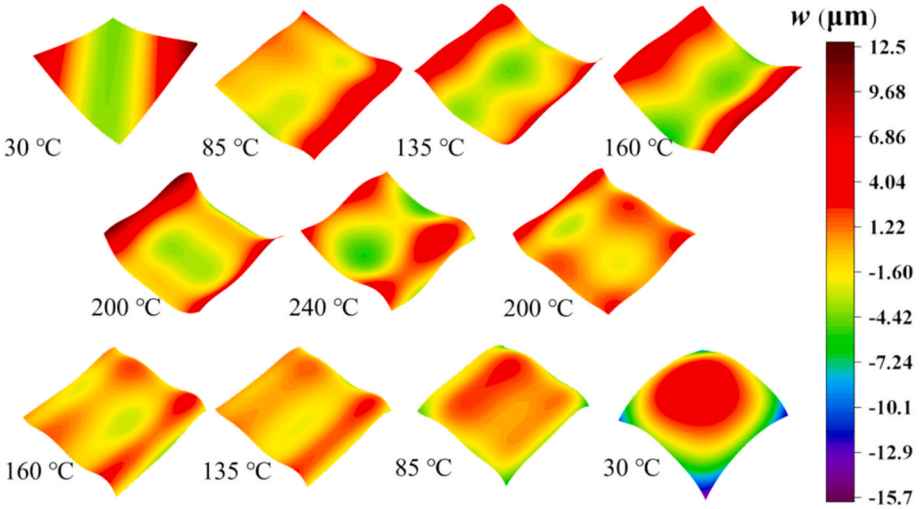

Fig. 7. In-situ DIC monitoring results of chip warpage during reflow.

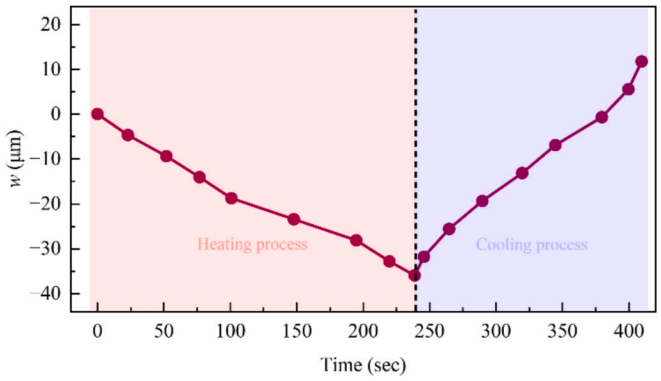

Fig. 8. Simulate the change in chip warpage during reflow.

Table 2
Four-factor orthogonal design.

Group	Die Properties		Substrate Properties		*W* (μm)	Δα* (ppm/°C)
	h (μm)	Size (mm × mm)	*h* (μm)	Material		
1	275	5*5	400	FR4	6.54	6.5
2	275	10*10	800	Al	15.81	16.5
3	275	15*15	1200	Cu	19.08	11.5
4	475	5*5	800	Cu	13.52	11.5
5	475	10*10	1200	FR4	8.08	6.5
6	475	15*15	400	Al	3.2	16.5
7	675	5*5	1200	Al	12.30	16.5
8	675	10*10	400	Cu	9.26	11.5
9	675	15*15	800	FR4	10.32	6.5

primary factors influencing warpage. Die thickness contributes 12.5 %, while chip area has a negligible impact. Moreover, the interaction between substrate thickness and $\Delta\alpha^*$ is significant: a larger $\Delta\alpha^*$ intensifies warpage, but a thinner substrate can effectively mitigate this effect (e.g. Group (6)). Conversely, even at low $\Delta\alpha^*$ values, an increase in substrate thickness may lead to higher warpage (e.g. Group (3)).

Table 3
Regression results for various influencing factors.

Factor	*β*	Standardized *β*	Weight
Substrate thickness	0.021	0.70	58.3 %
Die area	0.002	0.02	≈0 %
Die thickness	0.018	0.15	12.5 %
Δα*	0.200	0.35	29.2 %

3.3. Strategies to reduce warpage

The orthogonal experiments identified substrate thickness as the dominant factor affecting chip warpage. However, stringent packaging requirements often preclude further substrate thinning. While reducing CTE mismatch by substituting materials with similar thermal properties could alleviate warpage, such modifications are generally impractical given the fixed nature of the chip and substrate materials—any substitution may compromise device performance and reliability. To overcome these constraints, we propose a stress-balancing strategy based on the introduction of a transition layer. By adding a transition layer on the lower surface of the substrate, mechanical symmetry is achieved, generating counteracting forces that neutralize thermally induced bending moments. As shown in Fig. 9, a silicon wafer was chosen as the transition layer due to its compatibility with the chip material, thereby forming a symmetric assembly that promotes balanced stress distribution during the reflow process.

Experimental validation was performed using a chip (475 μm thickness) mounted on an 800 μm FR4 substrate. Compared to the conventional sandwich structure without the transition layer, the incorporation of the silicon wafer led to a significant reduction in warpage. Specifically, for a 10 mm × 10 mm sample, the central warpage decreased from 23.0 μm to 19.1 μm by 17.4 %, and for a 15 mm × 15 mm sample, it decreased from 20.8 μm to 18.6 μm by 10.6 %. The results are shown in Fig. 10.

The theoretical basis for this strategy lies in balancing the thermal stresses resulting from differential expansion. Although the addition of a transition layer increases overall thermal resistance (potentially impacting heat dissipation), this approach is well suited for applications with low thermal load requirements. Future work may focus on optimizing the transition layer's material properties, thickness, and placement to further refine stress distribution and reduce warpage. This strategy not only enhances the mechanical stability of die attach structure but also offers a versatile framework for addressing similar challenges in other high-precision electronic systems.

4. Conclusion

This study addresses the critical challenge of warpage in chip mounting by developing a thermoelastic-based prediction model that

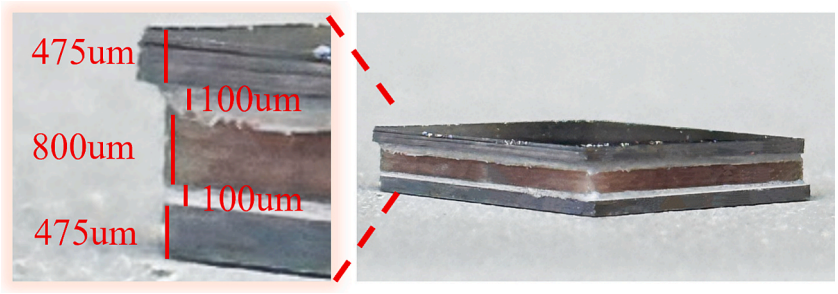

Fig. 9. Five-layer structure using transition layer.

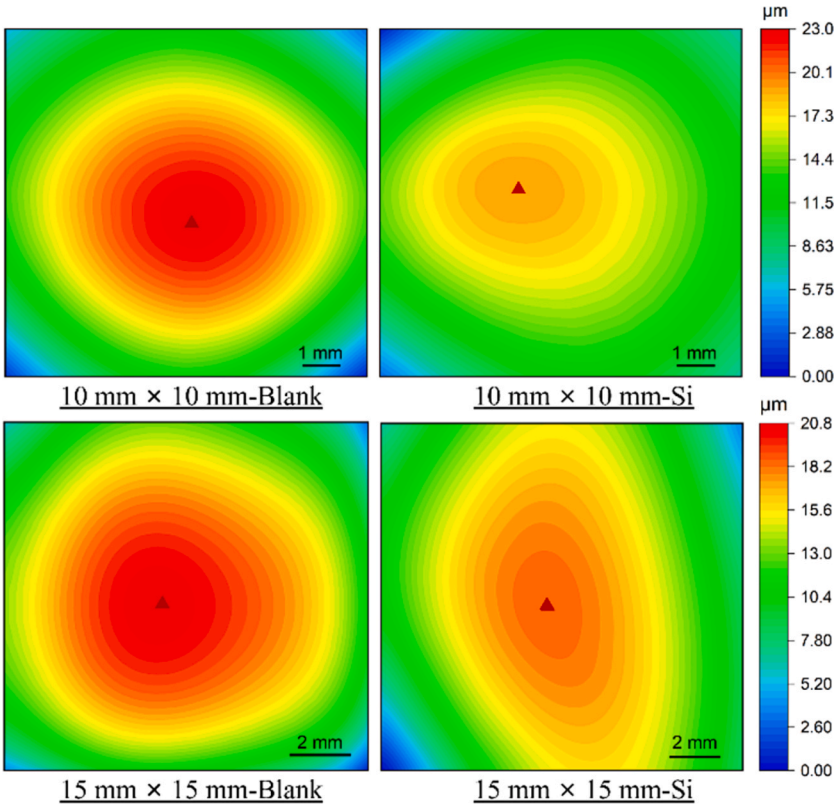

Fig. 10. Surface warpage profile test after chip mounting with three-layer structure and five-layer structure using transition layer.

accurately captures the dynamic evolution of warpage during the reflow process. This model characterizes the warpage induced by thermal expansion in laminated structures. In-situ Raman spectroscopy effectively maps the strain distribution of the chip caused by solder changes at different temperatures, providing essential material parameters for the model. Moreover, the strong agreement with error less than 1 % between FEM and predictions from our 3D thermoelastic model confirms that our approach strikes an optimal balance between computational efficiency and high-precision prediction. Continuous monitoring via DIC reveals that chip warpage undergoes a marked transformation: the chip initially exhibits a concave profile during heating, which then transitions to a convex form upon cooling after reflow curing. Comparison between these experimental observations and the model predictions further validates the model's capability to accurately describe the temperature-dependent evolution of warpage deformation.

Analysis of structural factors via orthogonal experiments further indicates that: (1) The interaction between substrate thickness and thermal expansion mismatches is the primary factor influencing warpage. In practical applications, selecting thinner substrates is advantageous. (2) Stress mitigation via the addition of a transition layer. When reducing substrate thickness is not feasible, heterogeneous integration with materials having similar CTE can effectively mitigate warpage during chip mounting by reducing $\Delta\alpha^*$. The proposed a transition layer achieves stress balance through a symmetrical structure, thereby significantly improving the chip warpage problem.

Both experimental results and simulations confirm the effectiveness of the proposed warpage reduction strategies. The insights provided by this study offer a robust framework for thermoelastic analysis, with broad applications in electronic device thermal management and structural thermal deformation analysis, ultimately contributing to enhanced reliability and performance in packaging.

CRediT authorship contribution statement

Wenyu Li: Writing – original draft, Visualization, Investigation, Formal analysis, Data curation. **Zhoudong Yang:** Writing – review & editing, Visualization, Methodology, Investigation, Formal analysis, Data curation. **Xueliang Wang:** Writing – review & editing,

Investigation, Data curation. **Yuhan Gao:** Data curation. **Jianguo Xie:** Data curation. **Fulong Zhu:** Resources. **Guoqi Zhang:** Resources. **Jiajie Fan:** Writing – review & editing, Validation, Supervision, Software, Resources, Project administration, Methodology, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.measurement.2025.118541.

Data availability

Data will be made available on request.

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