A 2.1MHz PWM Based Class D Audio Amplifier

MASTER OF SCIENCE THESIS

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A 2.1MHz PWM based Class D audio amplifier

by

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Abstract

This work presents a fully differential Class D audio amplifier using 2.1MHz pulse-width modulation (PWM) frequency and 425kHz LC filter cut-off frequency to decrease the cost of off-chip components. Moreover, feedback after LC filter structure is used to attenuate LC filter nonlinearities.
The Class D amplifier has been designed in a 140-nm bipolar CMOS DMOS SOI technology. With 14V output stage supply and 4Ω load, the Class D audio amplifier shows a dynamic range (DR) of 109dB, the maximum output power of 20W @ 0.0076%THD, and 91.2% efficiency. The Class D audio amplifier occupies an area of 5.4mm×4.0mm including seal-ring.

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Chapter 1

Introduction

This thesis describes the design of a 2.1MHz PWM Based Class D audio amplifier. The goal of this work is to determine whether it is possible to achieve a performance similar to a traditional Class D amplifier with a small inductor by increasing the switching frequency.

The basic principle of the Class D amplifier is first described in this chapter, followed by the motivation behind this work and the objectives of this design. At the end of this chapter, the organization of the thesis is given.

1-1 Basic principle

Class D modulation involves encoding information from the audio signal into a stream of pulses. The most traditional type of modulation is pulse-width modulation (PWM). An example of PWM is shown in Figure 1.1. Audio signals that are sinusoidal range in frequency from 20Hz to 20kHz. These signals, compared with high-frequency triangle carriers, generate a PWM signal. The duty of PWM is proportional to the amplitude of the audio signal. For zero input, the duty of the output pulse is 50%. For large positive input, the duty is close to 100%. For large negative input, the duty is close to 0% [1].

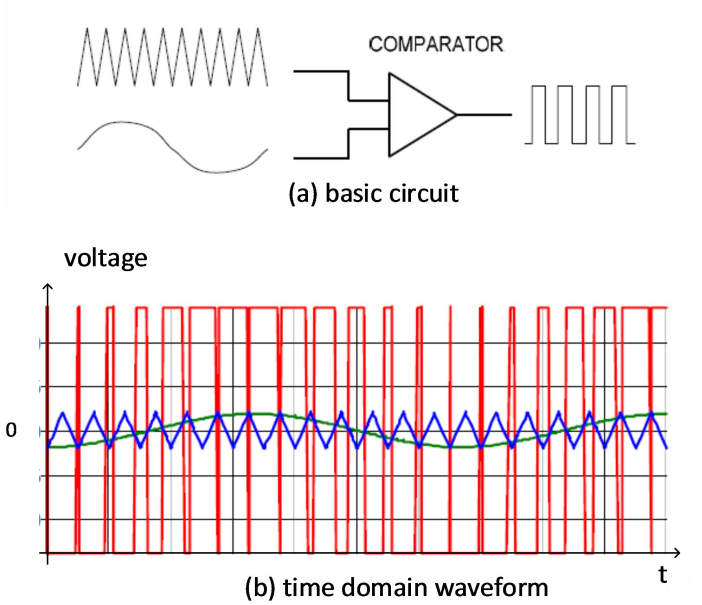


Figure 1.1: PWM concept and example [2]

A simple open-loop Class D amplifier is shown in Figure 1.2. The comparator generates a signal-relative pulse, which is then amplified at the Class D switching stage. The audio signal is then recovered after passing through an LC low pass filter [3]. Open-loop Class D amplifiers usually incur a poor power supply rejection ratio (PSRR) and are therefore very sensitive to the process voltage temperature (PVT). Consequently, closed-loop PWM Class D audio amplifiers are more popular in conventional audio applications.

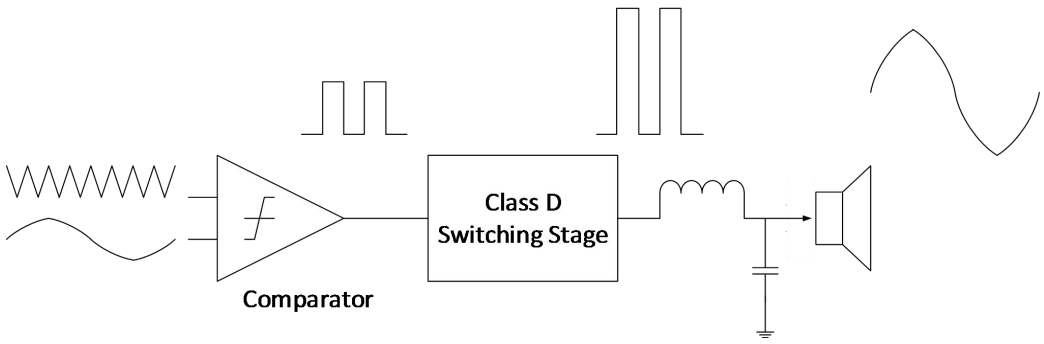


Figure 1.2: Open-loop Class D amplifier

Figure 1.3 shows the block diagram of a closed-loop Class D system. Feedback is applied to improve the PSRR and make the output less sensitive to PVT. The error amplifier is used to increase loop gain. A deadtime generator is employed to prevent the power switches of the output stage from conducting simultaneously, which will be discussed in Chapter 3.

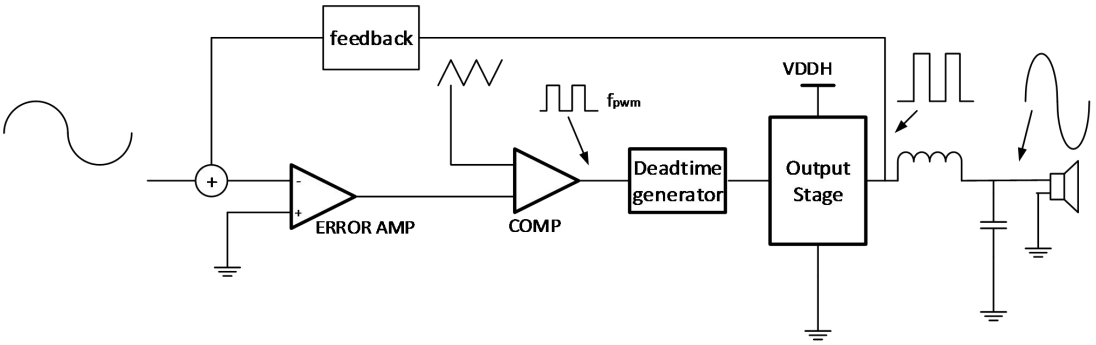


Figure 1.3: Block diagram of a traditional closed-loop Class D audio amplifier

Although Class D amplifiers have better efficiency than Class AB amplifiers, they require an output filter to prevent electromagnetic interference (EMI) and to reconstruct the output. In low-power applications, the less stringent EMI requirements make “filterless” design possible. In automotive applications, however, an output filter is still required [10].

1-2 EMI mask

The high-frequency components of the Class D amplifier may generate large amounts of electromagnetic interference (EMI) and thus disrupt the operation of other equipment. The output power of the Class D amplifier should be lower than the EMI mask to keep other equipment from being disturbed by the amplifier.

For PWM modulation Class D amplifiers, a tone emerges at the switching frequencies and the harmonics of the switching frequencies. As Figure 1.4 shows, the EMI requirement is relaxed from 300kHz to 500kHz. That is the reason why traditional Class D amplifiers switch from 300kHz to 500kHz. This design, however, tries to push the switching frequency to reach 2.1MHz, where the EMI requirement is also relaxed. At the same time, the second harmonic of the switching frequency at 4.2MHz is also located at a relatively relaxed frequency band.

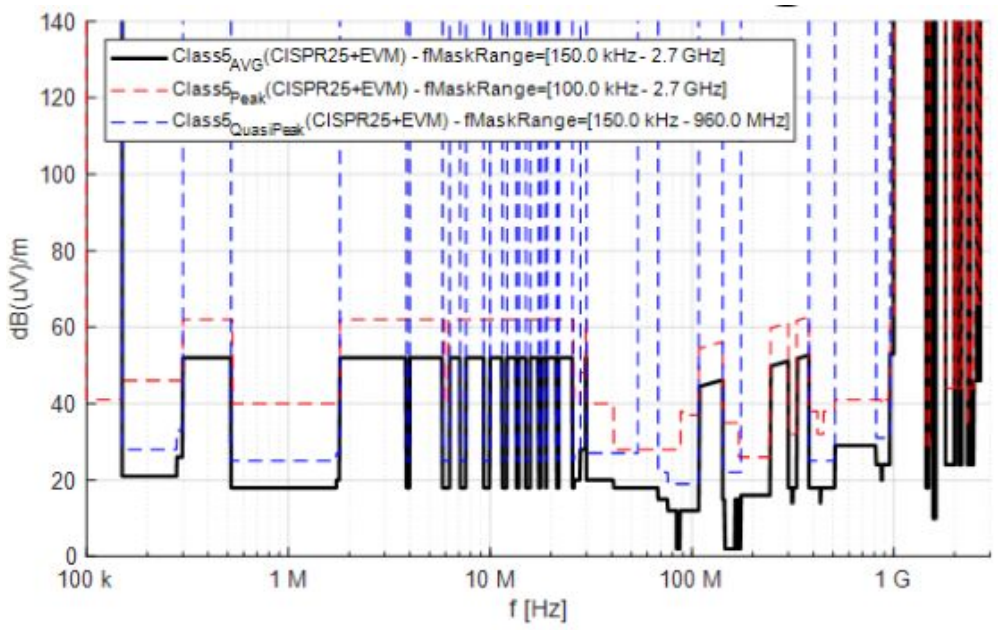


Figure 1.4: EMI mask

1-3 Motivation

The main disadvantage of Class D amplifiers in terms of cost is the LC filter. The inductors occupy space and add expense to the overall Class D audio system. In some cases, the price of the LC filter is close to that of the audio amplifier itself. In automotive applications, a bridge-tied load (BTL) is used, which doubles the component cost of the LC filter. The cut-off frequency of LC filters should be higher than the audio frequency (20Hz~20kHz) but lower than the ripple frequency. To reduce the cost of the output filter, one solution is to increase the ripple frequency. The expression of the ripple frequency is:

$$f_{ripple} = N \times f_{pwm} \tag{1.1}$$

in which, fpwm is the frequency of the high-frequency triangle, and N is the number of phases. In addition, the AD modulation has only one phase, whereas the BD modulation has two phases. Reference [4] uses multiphase operation to increase the ripple frequency. However, for four-phase modulation, four inductors are needed. Reference [5] combines the multi-phase and multi-level using two inductors. The main disadvantage is that there are four output transistors in series with the load. To maintain the same on-resistance, the size of each output transistor needs to be doubled. The output stage has eight output transistors rather than four (in traditional designs), so the area of the output transistors is four times larger.

Table 1.1: Different ways to achieve a high ripple frequency

	[4]	[5]	This design
fpwm(maximum)	1MHz	660kHz	2.1MHz
fripple(maximum)	4MHz	2.64MHz	4.2MHz
N	4	4	2
Number of inductors	4	2	2
Value of inductor	-	3.3μH	1μH
Area of output transistor	1 time	4 times	1 time

LC filter components have non-linearities which deteriorate the audio signal from the speaker. If the feedback is located after the LC filter, these non-linearities can be suppressed with a loop gain [4]. However, this approach introduces two poles into the loop, which complicates the loop stability design. Reference [4] uses digital feedback, in which an ADC is used.

By increasing the PWM frequency, a higher ripple frequency can be achieved, resulting in a higher LC cut-off frequency and smaller inductor. At the same time, two poles of the LC filter are located at a higher frequency, which means that loop stability is possible even with a simple loop design. The motivation behind this design is to design a 2.1MHz PWM frequency Class D audio amplifier with feedback after the output filter. A block diagram of this design is shown in Figure 1.5.

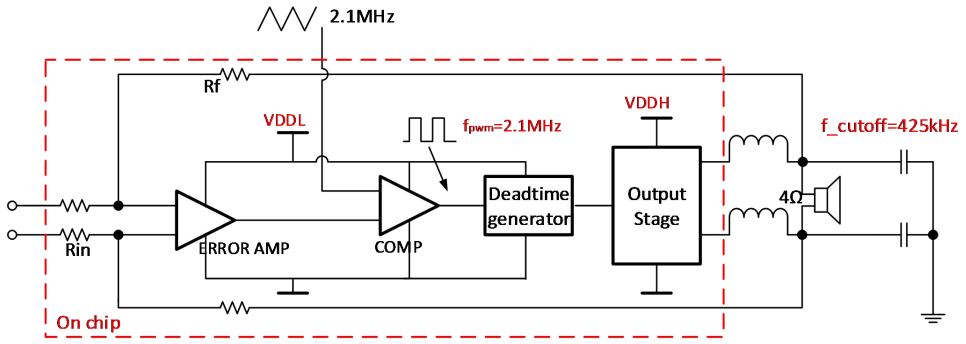


Figure 1.5: Block diagram of this Class D audio amplifier

1-4 Objectives

A good Class D audio amplifier needs to be efficient, and have low distortion and low noise. Table 1.2 shows the target specifications of this design.

Table 1.2: Target specifications

Switching frequency	2.1MHz
Supply voltage	14V
Load	BTL 4Ω
THD	<0.012%@1W
Output noise	45μVrms
Max output power@10%THD	28W
Max efficiency	>89%

The circuit has been designed in a 140-nm bipolar CMOS DMOS SOI technology.

1-5 Thesis Organization

This thesis presents circuit implementations of a PWM modulation Class D amplifier with a 2.1MHz switching frequency, which is targeted at automotive application. Apart from this introductory chapter, the rest of this thesis is divided into four chapters.

- Chapter 2 will discuss the system-level design.
- Chapter 3 will discuss the circuit implementation.
- Chapter 4 will show the simulation results of the whole design.
- Chapter 5 concludes the thesis by discussing the performance of the final design.

Chapter 2

System-level design

In this chapter, the system-level design will be discussed. The first part presents basic knowledge of the loop design. Second, the requirements of the system loop will be evaluated. Then an equivalent model of the system will be built. Lastly, the system will be design based on this equivalent model.

2-1 Basic knowledge of the loop design

For loop design, a linear model of a closed-loop Class D amplifier is needed. When the PWM switching frequency is much higher than the signal bandwidth, the Class D amplifier can be linearly modeled [6]. This closed-loop Class D amplifier acts as a simple inverting amplifier.

Figure 2.1 shows a simple inverting amplifier. Rin is the input resistor of this amplifier, Rf is the feedback resistor and A is the open-loop gain.

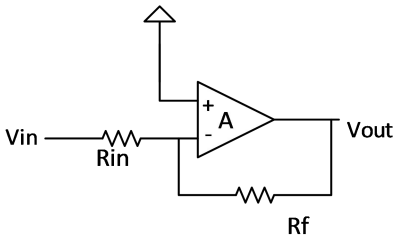


Figure 2.1: Inverting amplifier

A block diagram of this amplifier is shown in Figure 2.2.

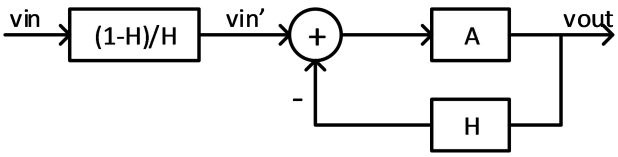


Figure 2.2: Block diagram of an inverting amplifier

for which the feedback factor is:

(2.1)

The weight of Vin is not unity. Therefore, in this design it becomes:

(2.2)

The close-loop gain of this inverting amplifier becomes:

(2.3)

In the Class D system, A is a series of blocks. For the function block of the Class D amplifier, e_n represents odd distortions or differential-mode noise.

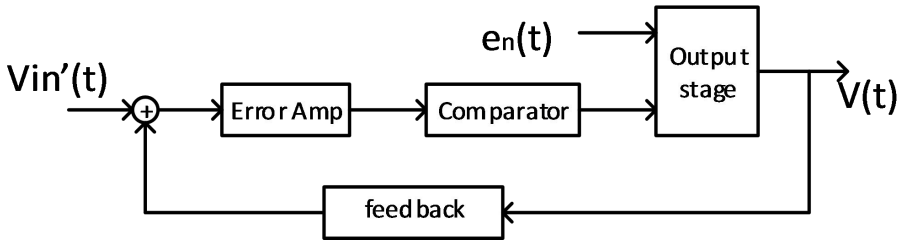


Figure 2.3: Function block of the Class D amplifier

The Class D amplifier is modeled in Figure 2.4 according to straightforward linear control theory.

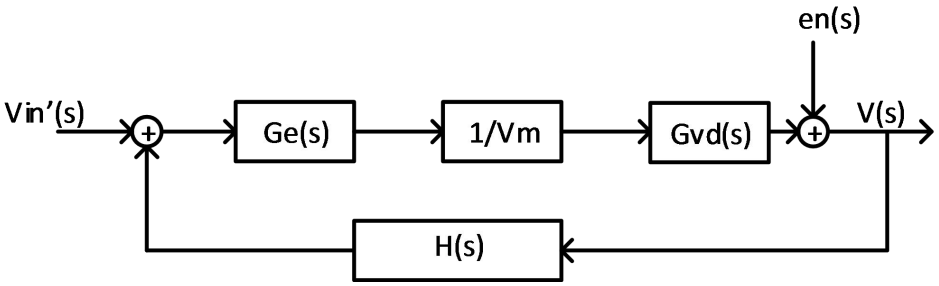


Figure 2.4: Linear model of the Class D amplifier

In Figure 2.4, Vm is the peak-to-peak voltage of the triangle.

The expression of output stage $G_{vd}(s)$ is:

(2.4)

in which Vg is the supply voltage of output stage, L is 1μH, C is 140nF, and R=2Ω. The load of the Class D amplifier is 4Ω BTL, and the equivalent single end resistor is 2Ω.

The loop gain of this feedback system is as follows:

(2.5)

The signal transfer function (STF) and noise transfer function (NTF) are derived as:

$$STF = \frac{V(s)}{Vin'(s)} = \frac{1}{H(s)} \frac{T(s)}{1 + T(s)} \tag{2.6}$$

$$NTF = \frac{V(s)}{en(s)} = \frac{1}{1 + T(s)} \tag{2.7}$$

An error amplifier is implemented to provide high differential gain to suppress odd HDs and differential noise.

2-2 Requirements

An open-loop Class D amplifier has a poor PSRR because all noise on the supply line goes directly to the output through the output stage switch. The most popular solutions focus on increasing differential loop gain to improve the PSRR. A higher loop gain directly means higher power supply noise rejection and better linearity [7].

Table 2.1: System requirements

THD	<0.012%
Loop gain @ 1kHz	>75dB
PM	>55°
L	1μH
C	140nF
LC cut-off frequency	425kHz
PWM frequency	2.1MHz

The value of the inductor and the capacitor of the LC filter have been chosen according to [4]:

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{L \times C}} \tag{2.8}$$

$$Q = R\sqrt{\frac{C}{L}} \approx 0.707 \tag{2.9}$$

The load of the Class D amplifier is 4Ω BTL; since (2.9) is meant for a single-ended load, the equivalent single end resistor is 2Ω.

2-3 Equivalent model of the system

The switching part can be represented by an equivalent gain stage in the system design. The value of this equivalent gain can be defined by the following equation:

Gain==16 (2.10)

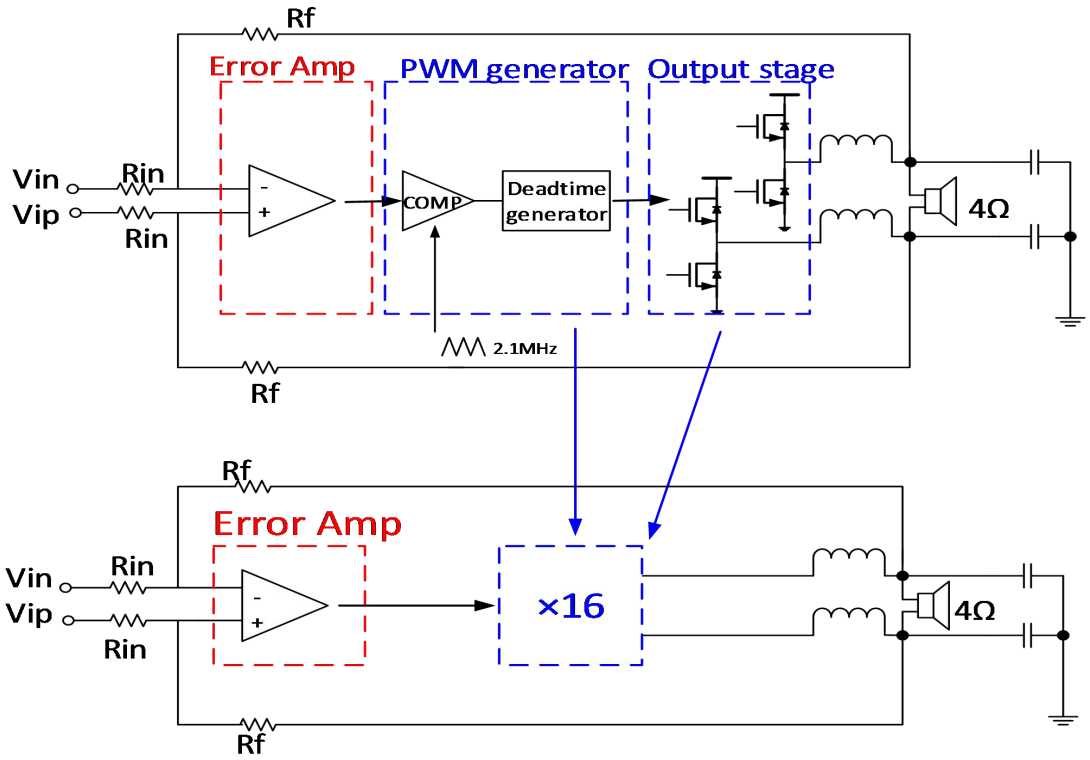


Figure 2.5: Equivalent model of the system

The peak-to-peak voltage of the triangle is limited by the input common mode range of the comparator. Since the supply of the comparator is 1.8V, this comparator is designed for a 0.8V range. Ron is the on-resistance of the output transistor. This value will be discussed further in Chapter 3.

A step input is applied to both the Class D amplifier and the equivalent model. The simulation waveform is shown in Figure 2.6. This equivalent model has a similar response with the Class D amplifier.

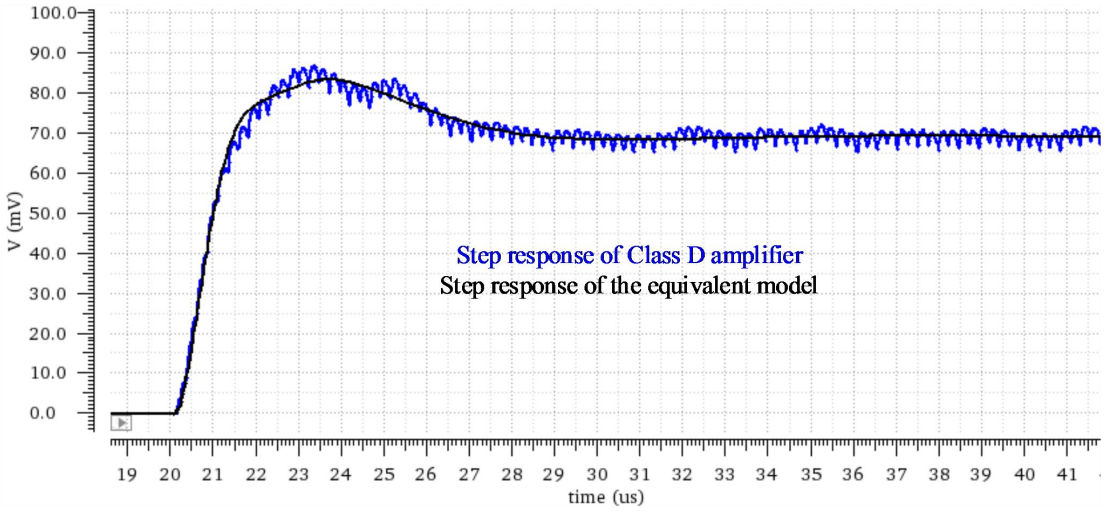


Figure 2.6: Step response of Class D amplifier and its equivalent model

2-4 Considerations

In terms of system and loop design, a higher-order system has more design dimensions and therefore needs more feedback components, hence the loop transfer function is more sensitive to those components. The main consideration of the system design is to satisfy this requirement by using a relatively low-order loop.

The goal is to calculate the loop gain at 1kHz while maintaining enough phase margin. There are three types of loops, all of which show different bode diagrams and loop gains. Also, there are two poles at the cut-off frequency of the LC filter.

Table 2.2: Calculated performance of different types of loops

	(a)	(b)	(c)
Order	first	second	second
Number of zero	0	1	2
Number of integrator	1	2	2
Loop gain @ 1kHz (PM≈50°)	44dB	53dB	82dB

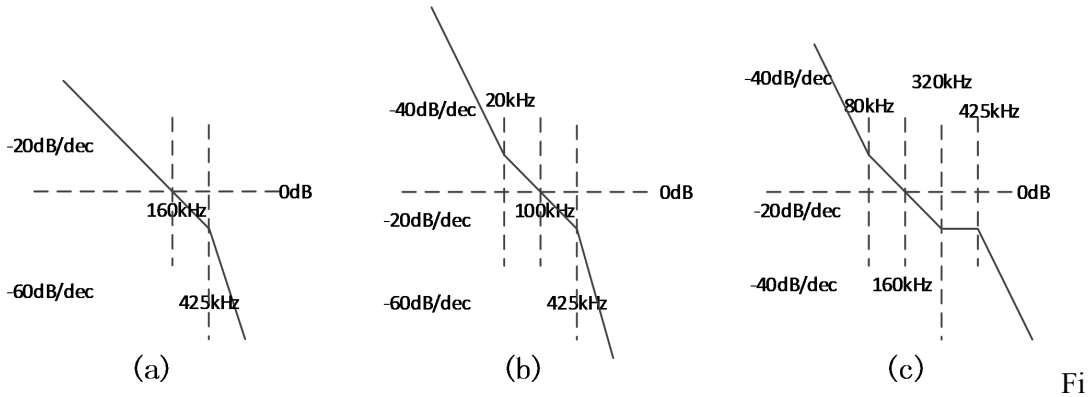


Figure 2.7: Bode diagram of different types of loops

To achieve a roughly 80dB loop gain at 1kHz, the type of loop needed is shown in the bode diagram in Figure 2.7(c). The loop structure and feedback component are built according to the specifications in that diagram.

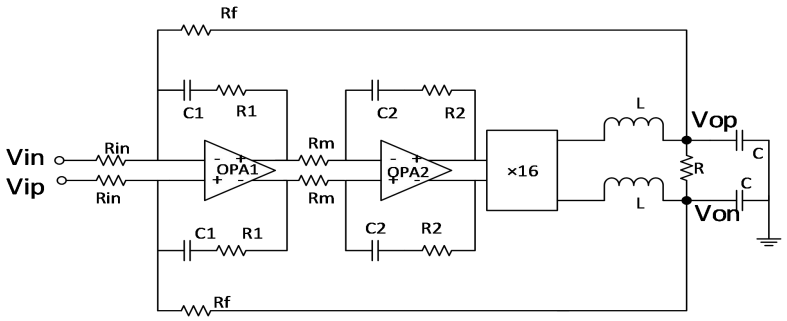


Figure 2.8: Loop structure of the (c) loop

Figure 2.8 depicts a schematic of the loop of the Class D amplifier. The error amplifier is realized by cascading INT1 and INT2. The INT1 is a proportional-plus-integral (PI) controller composed of Rin//Rf, R1, C1, and OPA1. The INT2 is another PI controller composed of Rm, R2, C2, and OPA2. The transfer function of INT1 and INT2 can be derived as:

$$H_1(s) = \frac{R_1}{R_{in} // R_f} + \frac{1}{s(R_{in} // R_f)C_1} \tag{2.10}$$

$$H_2(s) = \frac{R_2}{R_m} + \frac{1}{sR_mC_2} \tag{2.11}$$

The values of the feedback components of the error amplifier are shown in Table 2.3. Since the maximum output voltage is smaller than 14V, the gain of the system is chosen close to but smaller than the ratio of the supply voltage 14V/1.8V. The system gain, Rf/Rin, is 7 in this design.

The value of Rin was chosen to fulfill noise and area criteria, which will be presented in more detail in Chapter 3. Other component values were chosen based on Rin and loop transfer function considerations.

Table 2.3 Feedback component values of the error amplifier

Rin	Rf	R1	Rm	R2	C1	C2
30kΩ	210kΩ	6kΩ	200kΩ	200kΩ	80pF	10pF

By using this equivalent model, the loop transfer function was simulated.

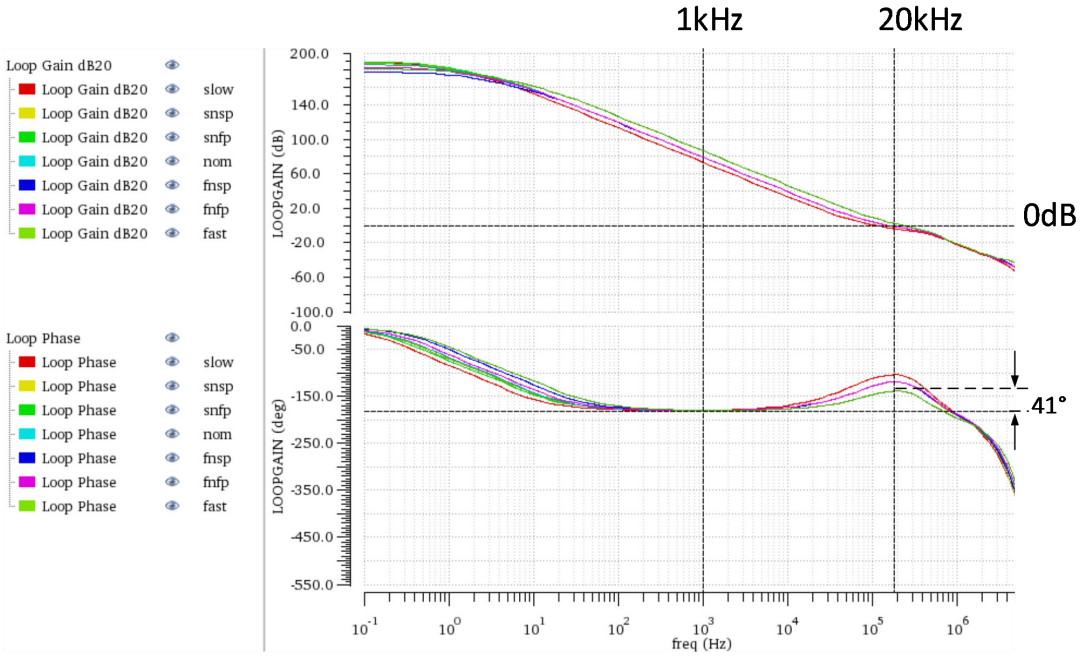


Figure 2.9: Bode diagram of the AC model

2-5 Trimming

Since feedback components may vary over the process corners, the transfer function of the loop may also vary. To ensure that the loop is stable at every corner, at least one component needs to be trimmed.

C2 (feedback capacitor of the second stage) is the best component to trim for stability purposes for the following two reasons. First, the capacitor value contributes to both zero and pole, whereas the resistor value contributes to either zero or pole, so trimming the capacitor is more efficient. Second, the capacitor of the first stage is eight times larger than that of the second stage.

Table 2.4 presents the performance achieved after trimming over corners.

Table 2.4: System performance after trimming

Loop gain @ 1kHz	>78dB
PM	>59°
L	1μH
C	140nF
LC cut-off frequency	425kHz

Chapter 3

Transistor Level Design

This chapter will discuss the circuit implementations of the function blocks needed for the Class D amplifier.

The first part of this chapter presents the requirements for each block. Then the detail of each block, such as the OPAs of the error amplifier, PWM generator and Class D output stage are discussed. The layout of the whole design is shown last.

3-1 System description

The main function blocks of this Class D amplifier are shown in Figure 3.1.

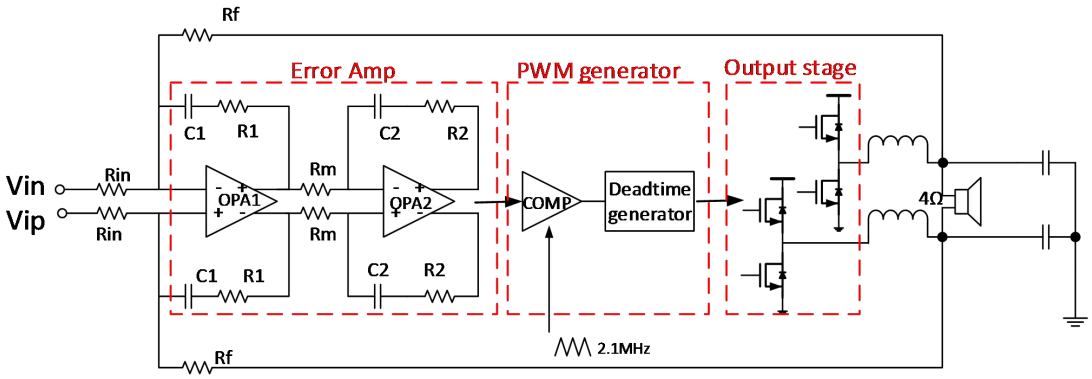


Figure 3.1: Main function blocks of this Class D amplifier

The noise requirement of the whole system is 45μVrms output noise. The gain of the Class D amplifier is 7. The input reference noise is:

(3.1)

The noise from the first stage usually contributes the most to overall system noise. In this design, noise performance depends on the error amplifier, Rin and Rf. The noise of Rin is added directly to equivalent input noise, therefore the thermal noise of Rin is the main noise source of the system. Rin value is calculated based on the noise requirement.

(3.2)

where $k=1.38\times10^{-23}$J/K is the Boltzmann constant, T is the temperature in Kelvin, and B is the signal bandwidth. In this design, T=300K, and B≈20kHz. Therefore 30kΩ is the maximum value of Rin to meet the noise requirement. Based on the frequency response in Chapter 2, when Rin is 30kΩ, C1 is 80pF. Lower noise can be achieved with a smaller Rin and larger C1. Since 80pF is already a large capacitor, Rin is 30kΩ in this design.

The feedback components of the error amp are already designed for loop consideration, as discussed in Chapter 2. Therefore, the main requirement for OPAs in the error amplifier is to provide enough bandwidth and gain so that the frequency response of the error amplifier is only determined by feedback components. For OPA1 of the error amplifier, the noise of OPA1 should be much smaller than the thermal noise of Rin.

A PWM generator is used to generate the control signal of the output stage. Comparator transfers the amplitude information to the duty information. Deadtime is used to avoid cross-conduction. If the deadtime is too short, cross-conduction may occur. If the deadtime is too long, distortion becomes an issue. Therefore, the

deadtime should be well-defined and stable over corners.

The output stage is a Class D amplifier, which amplifies the PWM signal and while driving a 4Ω BTL load. In terms of efficiency, the output stage is considered the main part of the whole system. Therefore, it should transfer the control signal from the PWM generator to the output without adding much distortion.

3-2 OPA1 of the error amplifier

3-2-1 Input common mode voltage of OPA1

Requirements

Since this design lacks a common feedback loop for the system, the input common mode voltage is set by the system. Figure 3.2 shows the common mode voltage of the system. There are two supply voltages in this system. The supply voltage of error amplifier and comparator is 1.8V. The supply voltage of the output stage is 14V. The output common mode voltage of Class D amplifier Vocm is:

$$V_{ocm} = \frac{VDDH}{2} = 7V \tag{3.3}$$

The input common mode voltage of Class D amplifier Vicm is:

$$V_{icm} = \frac{VDDL}{2} = 0.9V \tag{3.4}$$

Rin(=30kΩ) and Rf(=210kΩ) work as resistor dividers. The input common mode voltage of error amplifier Vecm is dependant on Vocm, Vicm and this resistor divider. The value is:

$$V_{ecm} = \frac{R_{in}}{R_{in} + R_f} \times V_{ocm} + \frac{R_f}{R_{in} + R_f} \times V_{icm} = 1.6625V \tag{3.5}$$

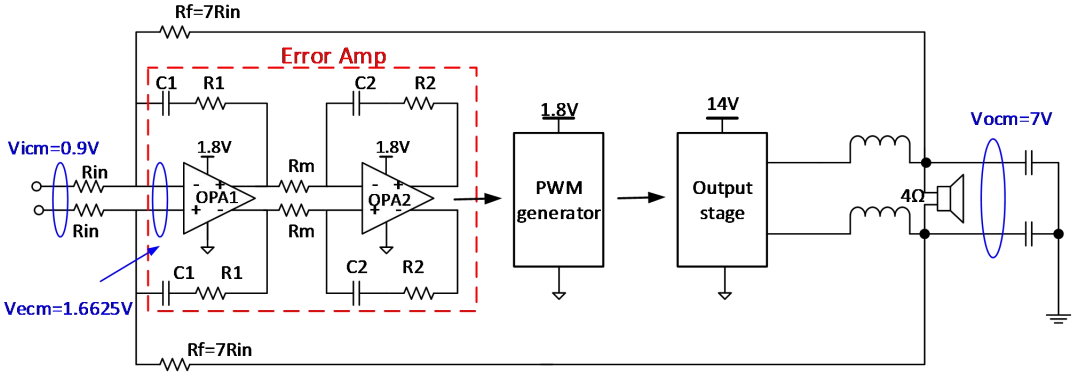


Figure 3.2: Common mode voltage of the system

Design

OPA1 is the first stage of the error amplifier. Its input common mode voltage (Vecm) is close to the supply voltage, so NMOS input transistors are needed.

3-2-2 Noise performance of OPA1

Requirements

Noise from the first stage usually contributes the most to overall system noise. The noise requirement for OPA1 is it must be much smaller than the thermal noise of Rin.

Design

The thermal noise density of Rin (30kΩ) is:

(3.6)

where $k=1.38\times10^{-23}$J/K is the Boltzmann constant and; T is the temperature.

The thermal noise of a simple common source amplifier with an active current source load is:

(3.7)

where g_{m1} is the transconductance of the input MOS, g_{mc} is the transconductance to the current source MOS, and γ is the coefficient related to the process. In this design, g_{m1} is 0.52mS and; g_{mc} is 0.18mS. The noise contribution of the channel to the overall system is less than 10%.

1/f noise can be reduced by increasing the size of the input transistors. However, larger transistors have a larger parasitic capacitor, which makes the frequency response design difficult. In this design, because the input transistors are NMOS, the relatively large size (256μm/8μm) is chosen for 2μVrms.

Simulation results

Table 3.1 shows the list of main noise sources. The main noise source is input resistor Rin.

Table 3.1: List of main noise sources

Noise source	Noise contribution
Rin=30kΩ	52.5%
Rf=210kΩ	14.6%
Input MOS of OPA1 1/f noise	10.9%
Rm=200kΩ	7.6%
Input mos of OPA1 thermal noise	5.0%
Current source of OPA1 1/f	3.6%
Others	5.8%

The noise density is shown in Figure 3.3. The white noise density is 39.4nV/sqrt(Hz).

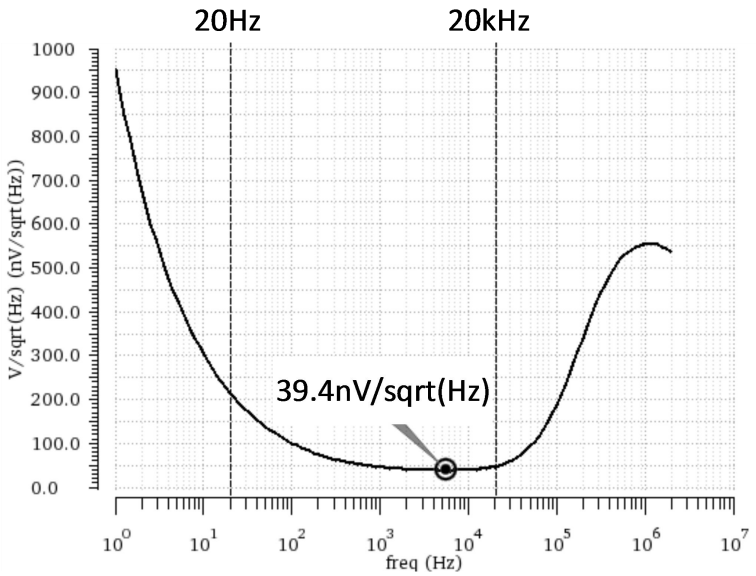


Figure 3.3: Noise density

3-2-3 Frequency response of OPA1

Requirements

The INT1 is a proportional-plus-integral (PI) controller composed of Rin//Rf, R1, C1, and OPA1. $H_1(s)$ is the ideal transfer function of INT1, which depends on the feedback components.

$$H_1(s) = \frac{1 + sR_1C_1}{s(R_{in} // R_f)C_1} = \frac{1 + j(f / f_{z1})}{j(f / f_{p1})} \tag{3.8}$$

$$f_{z1} = \frac{1}{2\pi} \cdot \frac{1}{R_1C_1} = 3.31 \times 10^5 Hz \tag{3.9}$$

$$f_{p1} = \frac{1}{2\pi} \cdot \frac{1}{(R_{in} // R_f)C_1} = 7.58 \times 10^4 Hz \tag{3.10}$$

The lowest frequency of audio frequency is 20Hz. Gain at 20Hz is:

$$\left|H_1(j \cdot 20Hz)\right| \approx \left|\frac{f_{p1}}{20Hz}\right| = 3790 = 71.6dB \tag{3.11}$$

The unity frequency of $H_1(s)$ is around 75.8kHz.

OPA1 needs sufficient DC gain and bandwidth to maintain $H_1(s)$. The frequency response requirement of OPA1 is:

$$A_{OPA1,DC} >> 71.6dB, f_{OPA1,unity} >> 75.8kHz \tag{3.12}$$

Design

DC gain of a simple common source amplifier with a current source load is:

(3.13)

where V_E is a technological parameter, the value of which is around 4V/μm. For the input transistor, the channel length L=8μm is designed for 1/f noise performance. If the input transistor is 100mV, the maximum DC gain for a one-stage common source amplifier is around 56dB, which is less than the requirement for OPA1. Therefore, a two-stage amplifier is needed for $A_{OPA1,DC}$.

As shown in Figure 3.4, OPA1 is a two-stage op-amp. M1a and M1b are input NMOSs, whereas M2a, M2b, M3a, and M3b are current sources. The common mode feedback circuit is used to control the bias of M3a and M3b.

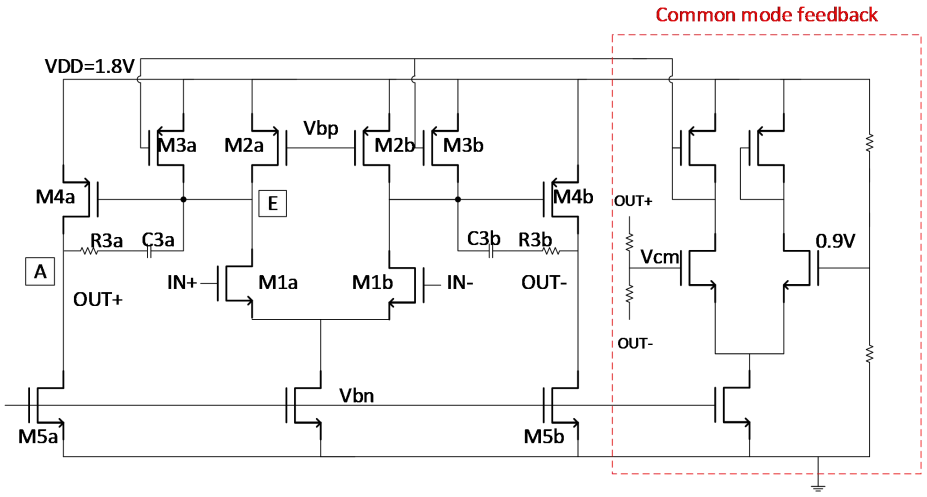


Figure 3.4: Schematic of OPA1

$A_{OPA1,v1}$ is the gain of the first stage, the expression of which is:

(3.14)

$A_{OPA1,v2}$ is the gain of the second stage. Which does not need as high of a gain as the first stage. A short channel (L=1μm) is chosen for M4a and M4b.

(3.15)

Without R3 and C3, the two-stage amplifier has two high impedance notes: note E and note A. The circuit exhibits two dominant poles. Therefore, the amplifier becomes unstable. Miller capacitor C3 is added for frequency compensation. The unity gain frequency of OPA1 is:

(3.16)

The value of C3 is set as 8pF in this design.

However, this Miller compensation introduces a right-half-plane zero. This zero will make the amplifier unstable. One approach to avoid this right-half-plane zero is

to places a resistor R3 in series with the compensation capacitor. By adding R3, the zero frequency is now:

(3.17)

Since $R3>g_{m4}^{-1}$, the zero becomes a left-half-plane zero, meaning it can be used to cancel the first non-dominant pole. In this design, gm4 is 0.24mS and R3 is 6kΩ.

Simulation results

The transfer function of INT1 with OPA1 was simulated. As Figure 3.5 shows, for the transfer function of INT1 with OPA1, $H_1(s)$' is similar to $H_1(s)$. OPA1 fulfills the requirements for this INT1 design.

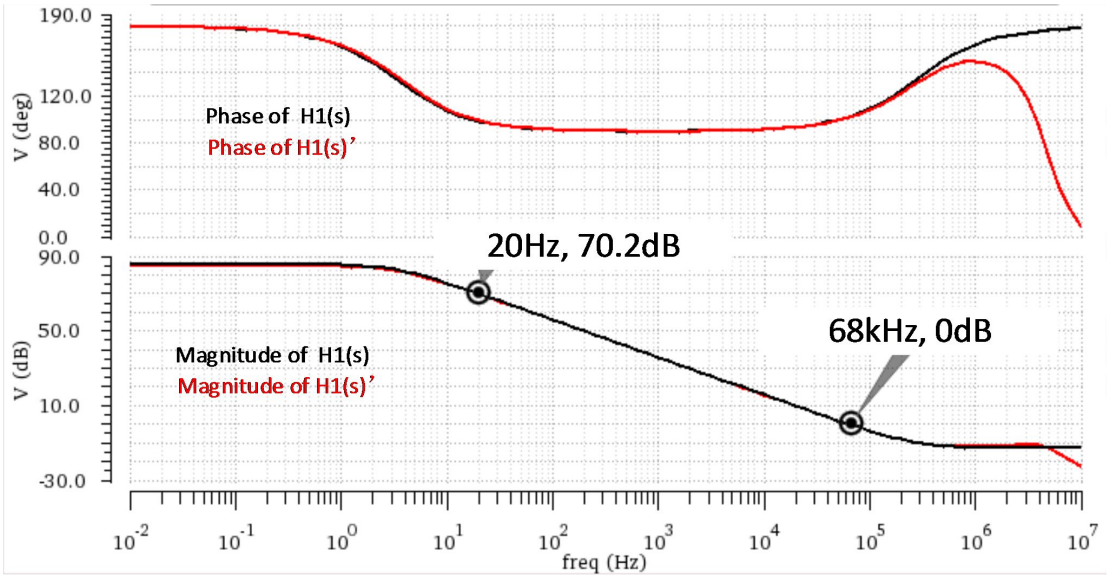


Figure 3.5: Ideal INT1 transfer function H1(s) and transfer function of INT1 with OPA1 H1(s)'

3-3 OPA2 of the error amplifier

3-3-1 Frequency response of OPA2

Since the noise of INT2 is suppressed by the gain of INT1, as long as INT1 has enough gain, the noise performance of OPA2 can be disregarded. The main consideration of OPA2 is the frequency response. INT2 is another PI controller which is composed of Rm, R2, C2, and OPA2. $H_2(s)$ is the ideal transfer function of INT2, depending on the feedback components.

(3.18)

Since

$$R_2 = R_m = 200k\Omega \tag{3.19}$$

$$f_{z2} = f_{p2} = \frac{1}{2\pi} \cdot \frac{1}{R_2 C_2} = 7.96 \times 10^4 Hz \tag{3.20}$$

the lowest of audio frequency is 20Hz. Gain at 20Hz is:

$$\left|H_2(j \cdot 20Hz)\right| \approx \left|\frac{f_{p2}}{20Hz}\right| = 3790 = 72.0dB \tag{3.21}$$

The unity frequency of $H_2(s)$ is around 79.6kHz.

OPA2 needs enough DC gain and bandwidth to maintain $H_2(s)$. The frequency response requirement of OPA2 is:

$$A_{OPA2,DC} >> 72.0dB, f_{OPA2,unity} >> 79.6kHz \tag{3.22}$$

3-3-2 Design of OPA2

OPA2 has a similar structure to OPA1. The size of the input transistors is 32μm/2μm and the compensation capacitor is 1.2pF. The resistor used to move right-half-plane zero is 10kΩ.

$A_{OPA2,v1}$ is the gain of the first stage of OPA2, and $A_{OPA2,v2}$ is the gain of the second stage of OPA2.

(3.23)

If two stages have a similar gain; L=2μm is enough DC gain for both stages. In this design, g_{m1} is 124μS. The unity gain frequency of OPA2 is:

(3.24)

The value of C3 is set as 1.28pF in this design.

In this design, g_{m4} is 0.24mS and R3 is 10kΩ. By adding R3, the zero frequency is now:

(3.25)

which can be used to cancel the first non-dominant pole.

3-3-3 Simulation results of OPA2

The transfer function of INT2 with OPA2 was simulated. As Figure 3.6 shows, the transfer function of INT2 with OPA2, $H_2(s)$' is similar to $H_2(s)$. OPA2 is good enough for this INT2 design.

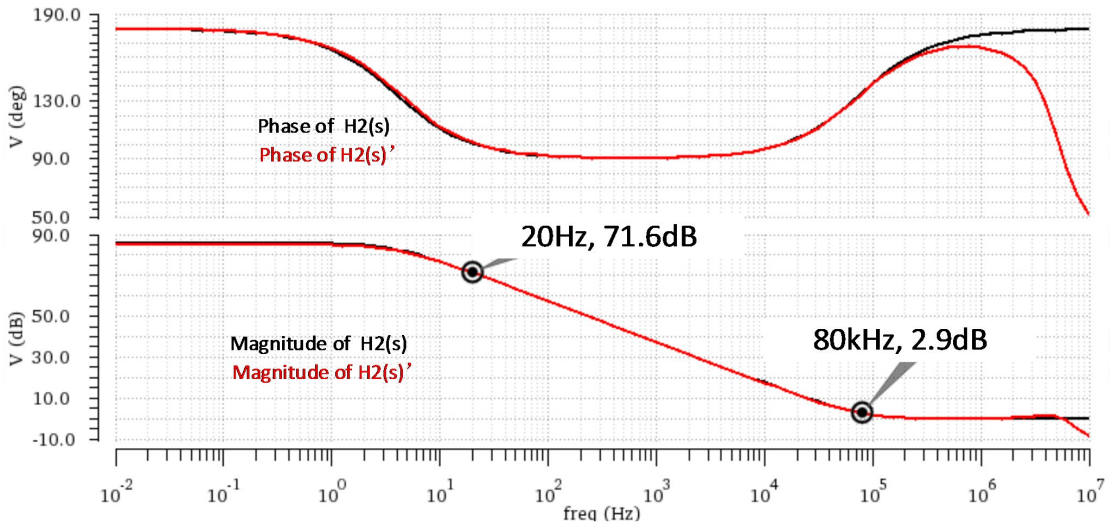


Figure 3.6: Ideal INT2 transfer function H2(s) and transfer function of INT2 with OPA2 H2(s)'

3-4 Deadtime generator

3-4-1 Deadtime definition

In the simplified model of the output stage in Figure 3.7(a), MH is the switch between Vout and VDD, and ML is the switch between Vout and GND. Because MH and ML have very low resistance, if MH and ML are on at the same time, a large current will flow through the two output transistors which will destroy the Class D amplifier. To ensure that the Class D amplifier works normally, some designs add deadtime before the two transistors switch [9] [10] [11]. As Figure 3.7(b) shows, during deadtime, both transistors are off.

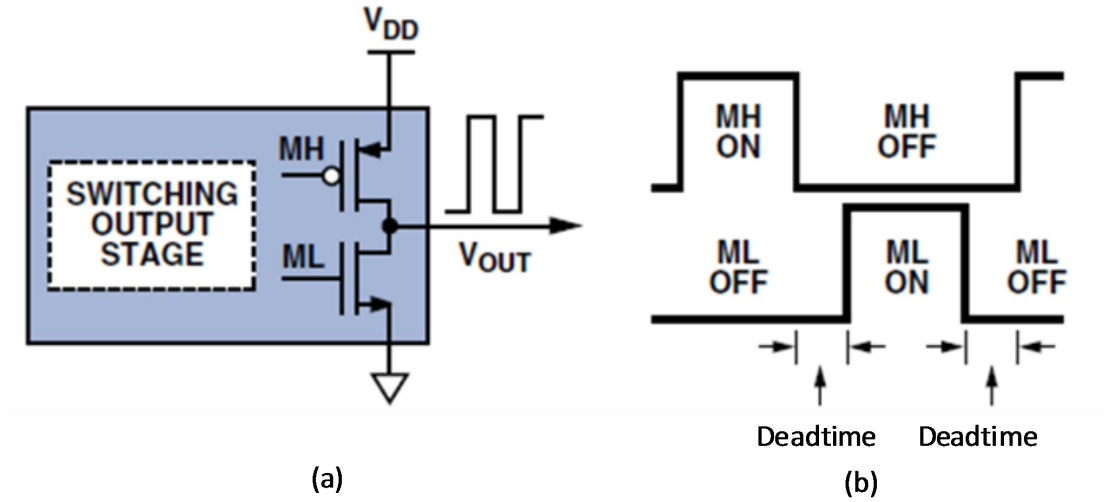


Figure 3.7: (a) Simplified model of the output stage, (b) Control signal of the output stage

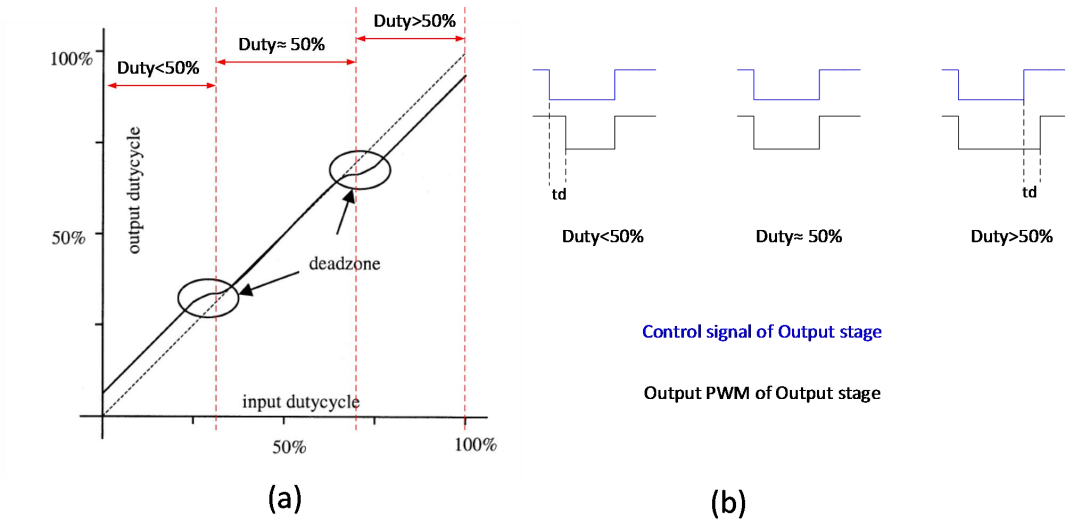


Figure 3.8: (a) Relation between input and output duty, (b) Waveform of different input duties

However, this deadtime introduces a signal-related distortion [9]. As Figure 3.8 (b) shows, when the input duty is close to 50%, the output PWM of the output stage and

control signal of the output stage has the same duty cycle. Deadtime does not cause gain loss. When the input duty is much larger than 50%, the output PWM of the output stage has less duty than the control signal of the output stage. When the input duty is much less than 100%, the output PWM of the output stage has a larger duty than the control signal of the output stage. Therefore, when input duty is far below/above 50%, deadtime causes gain loss. The duty transfer function of the output stage is plotted in Figure 3.8 (a). There are two deadzones. When the input signal is small, the signal does not cross the deadzones, causing no distortion. When the input signal is large, the signal crosses the deadzones, causing distortion. A longer deadtime means more distortion.

3-4-2 Requirements of the deadtime generator

For a BD mode Class D amplifier [8], the four output transistors of the output stage need four signals. Figure 3.9 shows the circuit of the PWM generator and how it is connected to the output stage. The signal inputs of the PWM generator, IN+ and IN-, are connected to the output of the error amplifier. The high-frequency triangle carried, Vtriangle, is a 2.1MHz input signal from the PCB. IN+ first compares with Vtriangle, then goes into the deadtime generator and generates P0 and , which are control signals for the PWM+ side. IN- goes through a similar path, then generates P180 and , which are control signals for the PWM- side. For BD modulation, the ripple frequency is two times larger than the PWM frequency.

If the deadtime is too short, cross conduction may happen. If deadtime is too long, distortion is significant. The first requirement is that the deadtime should be well defined and stable over corners. The second requirement is that the deadtime should be neither too long nor too short.

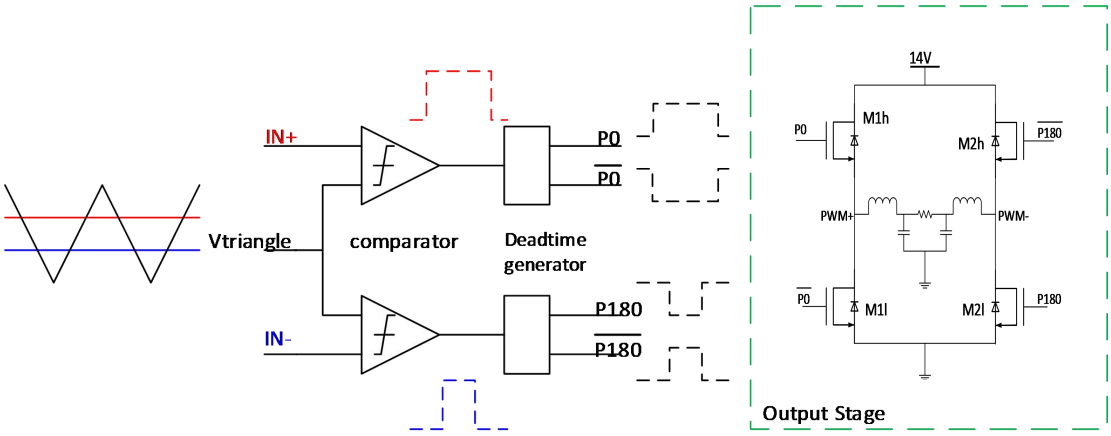


Figure 3.9: PWM generator

3-4-3 Design of the deadtime generator

The deadtime generator, as Figure 3.10 shows, is a non-overlapping cell with two

identical delay lines. The deadtime is equal to the delay time of the delay lines.

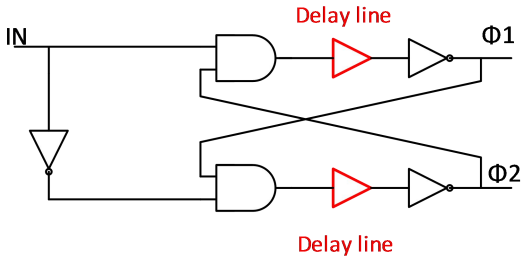


Figure 3.10: Deadtime generator

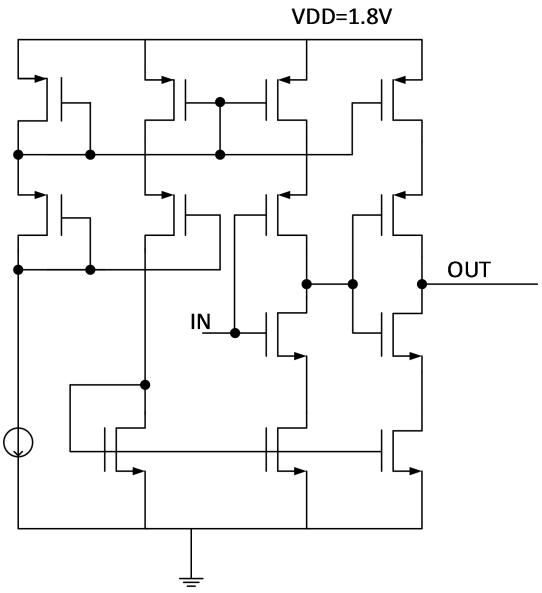


Figure 3.11: Delay lines

The simplest delay line is an inverter line. However, the delay line made by inverters has two drawbacks. First, for a unit inverter from the digital library, around 400 inverters are needed for 10ns. Second, a delay line made by the inverter changes about ±20% over corners. To decrease the number of inverters, a capacitor load can be added to the digital inverter. However, because the capacitor also changes over corners, the delay variation will be even larger. The proposed delay line, as Figure 3.11 shows, is based on a current-starving inverter. If the current is constant, the variation over corners can be less than ±7%. The current source in Figure 3.11 is an input in this design. Deadtime can be trimmed by changing the input current.

Deadtime introduces a signal-related distortion. If the gate driver is sized in a certain way, which will be discussed in Section 3-5-2, a zero deadtime Class D amplifier also works [12]. This design adds a zero deadtime mode.

3-5 Output stage

Figure 3.12 shows the output stage, the supply voltage of which is 14V. The blue components in Figure 3.12 are located on a PCB, including four bootstrap capacitors, an LC filter, and a speaker. The black components are on-chip. There are four main parts of this output stage: output transistors, gate drivers, low-dropout regulators (LDOs), and level shifters. The output transistors are M1h, M1l, M2h, and M2l. The four output transistors have the same size. The gate drivers are used to driving the output transistors. The level shifter transfers a 0V-1.8V logic control signal to a specified logic for each output transistor. The LDOs provide the floating supply for the gate drivers and level shifters. Each block design will be shown in detail separately below.

The output stage is the main block for efficiency performance. There are three types of losses:

1) Conduction loss is caused by on-resistance of the output transistor.

2) Capacitive loss is caused by charging and discharging of the parasitic capacitor. The main part of parasitic capacitor is gate capacitor of output transistor. Therefore, gate driver loss is the main part of capacitive loss.

3) Switching loss is caused by V-I overlap during the switching transitions.

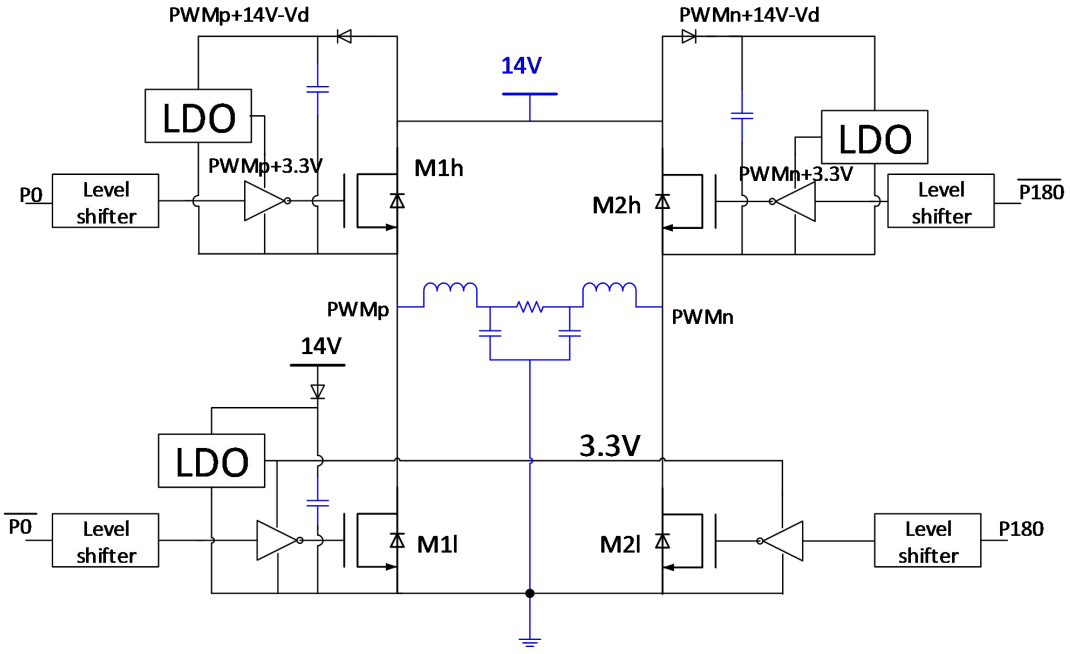


Figure 3.12: Overview of the output stage

3-5-1 Output transistor

Requirements

A larger output transistor means a smaller on-resistance and larger parasitic capacitance. Thus conduction loss decreases with size, whereas capacitive loss increase with size. As for switching loss, when switching is fast enough, the dominant current contribute is reverse-recovery current, which increases with size. The total dissipation can, therefore, be optimized by choosing the correct transistor size to balance these three power dissipation sources [6]. The maximum efficiency target is 90%, which requires choosing the output transistor size so that conduction loss is around 5%.

Design

Figure 3.13 shows the relationship between Ron and the area of the output transistor. Ron is the on-resistance of one output transistor. When choosing a W/L equal to 120000μm/0.5μm, 0.11Ω Ron can be achieved at room temperature, where the conduction loss is around 5% of the output power.

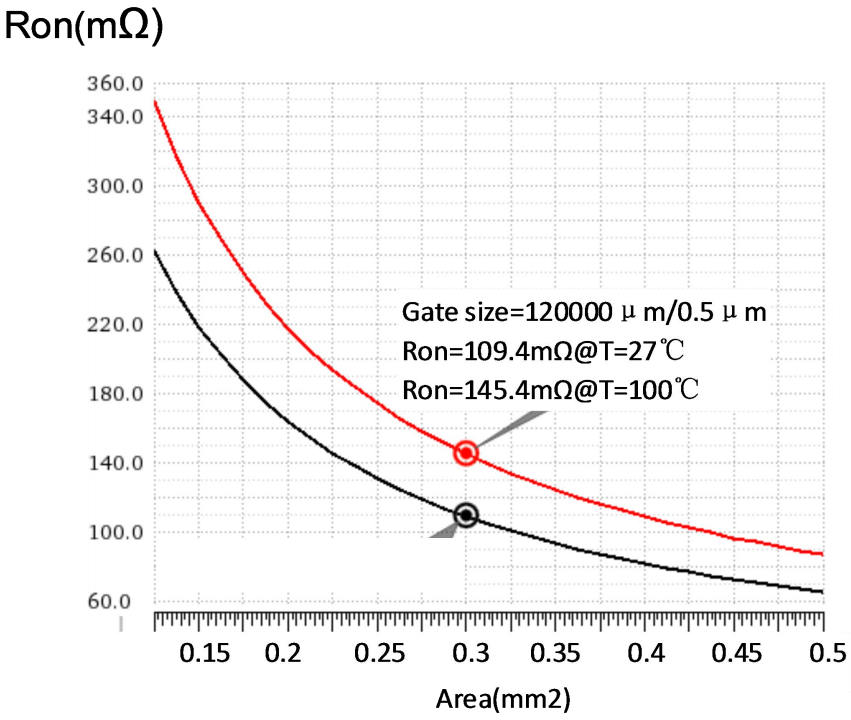


Figure 3.13: Relation between Ron and the area of the output transistor

Conduction loss can be roughly calculated as:

$$Conduction\ \ Loss = \frac{2R_{on}}{4\Omega + 2R_{on}} = \begin{cases} 5\%\ @\ T = 27°C \\ 6.8\%\ @\ T = 100°C \end{cases} \tag{3.26}$$

The loss contribution of each part will be shown in Chapter 4. The result shows that the conduction loss is around 5% in this design.

3-5-2 Gate driver

3-5-2-1 Cross-conduction

Requirements

The simplest gate driver is an inverter. The gate driver of M1h and M1l is same. The size ratio between the NMOS and PMOS of the gate driver is important to avoid cross-conduction. The PWM+ side is shown in Figure 3.14. During the deadtime, both M1h and M1l are off, as is shown in (a). When M1h is turned on, the output stage changes from (a) to (b), meaning Cgsh needs to be charged through Mph. At the same time, Cgdl needs to be discharged by Mnl, because the voltage on Cgdl changes from 0V to 14V. If the discharging of Mnl is not fast enough, the gate voltage of M1l will be higher than the threshold voltage. If M1l is on, cross-conduction will occur. To avoid cross-conduction, the NMOS of the gate driver should be much larger than the PMOS of the gate driver.

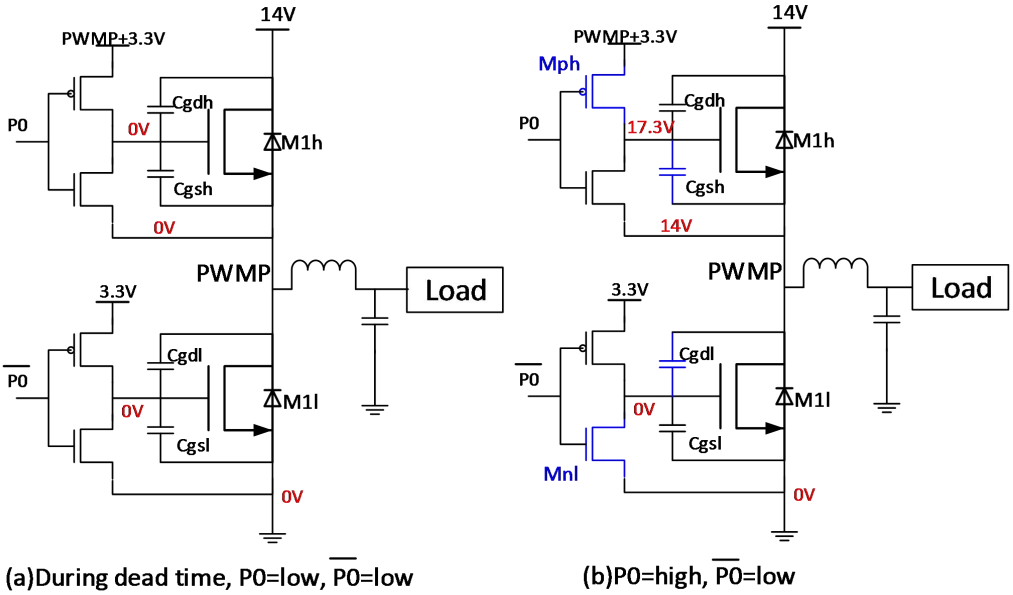


Figure 3.14: Load of gate driver

Design

Figure 3.15 shows the waveform of Figure 3.14. The threshold voltage of the output transistor is around 1.26V. When the NMOS of the gate driver is the same size as the PMOS of the gate driver, Vgs of M1l (Vgsl) goes to 1.4V, which is larger than the threshold voltage, while Ml1 and M1h are on at the same time. When the NMOS of the gate driver is six times larger than the PMOS of the gate driver, the peak value of Vgsl is 1V, which is smaller than the threshold voltage. M1l and M1h, in this case, are not on at the same time. In this design, $(W/L)_{NMOS}$ is six times the size of $(W/L)_{PMOS}$.

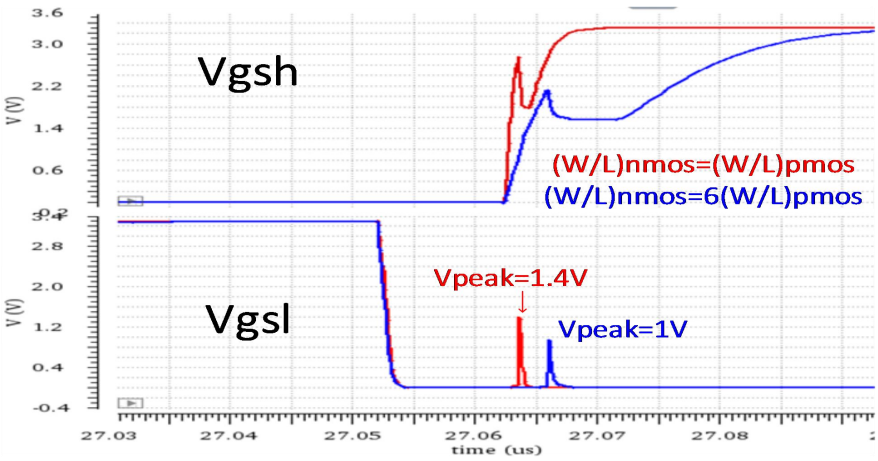


Figure 3.15: Simulation waveform of different size ratio

3-5-2-2 Efficiency

Requirements

The absolute size of the gate driver is related to power dissipation.

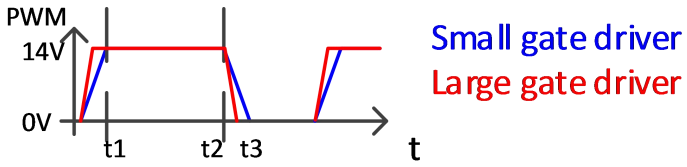


Figure 3.16: PWM waveform of different sized gate drivers

During switching transitions, the PWM voltage of the small gate driver is far from the supply voltage, and the V-I overlap of the output transistor is relatively large. As Figure 3.16 shows, when the gate driver is small, the switching transition is slow, hence a slow transition contributes additional switching loss. A large gate driver needs a larger area and therefore has a more parasitic capacitor.

Design

By taking only conduction loss and switching loss into account, the maximum efficiency is simulated with different gate drivers. As Table 3.2 shows, when the gate driver size increases from (1) to (2), efficiency increases 0.5%. However, further increases from (2) to (3) causes the efficiency improvement to become insignificant.

Table 3.2: Maximum efficiency with different gate drivers

	PMOS	NMOS	Maximum efficiency
(1)	600μm/0.32μm	3600μm/0.32μm	93.9%
(2)	900μm/0.32μm	5400μm/0.32μm	94.4%
(3)	1350μm/0.32μm	8100μm/0.32μm	94.5%

In this design, the NMOS of the gate driver is 5400μm/0.32μm, and the PMOS of the gate driver is 900μm/0.32μm.

3-5-3 LDO

Function

An external 14V supply and bootstrap capacitors are located on the PCB as shown in Figure 3.17 (a). The voltage of PWMp is either 0V or 14V. When PWMp is 0V, D1 is on, and current flows through D1 and charges Cboot1 to 14V-Vd. Vd is the diode forward voltage. When PWMp is 14V, D1 is off, and Cboot1 bootstraps Vboot,int to 28V-Vd. If Cboot1 is large enough, Vboot,int is around PWMp+14V-Vd.

The simulation model is given as Figure 3.17 (b). PCB components are connected to the chip through bond wires which have parasitic inductances. During the switching transitions, these bond wires cause ringing at the supply of the output stage. The amplitude of the ringing depends on the signal, which during simulation reached as high as 24V. Applying the noise supply directly to the gate driver (3.3V device) may cause damage to the gate driver. In this design, a low dropout regulator (LDO) is used to filter any ringing caused by the parasitic, creating a clean supply for the gate driver.

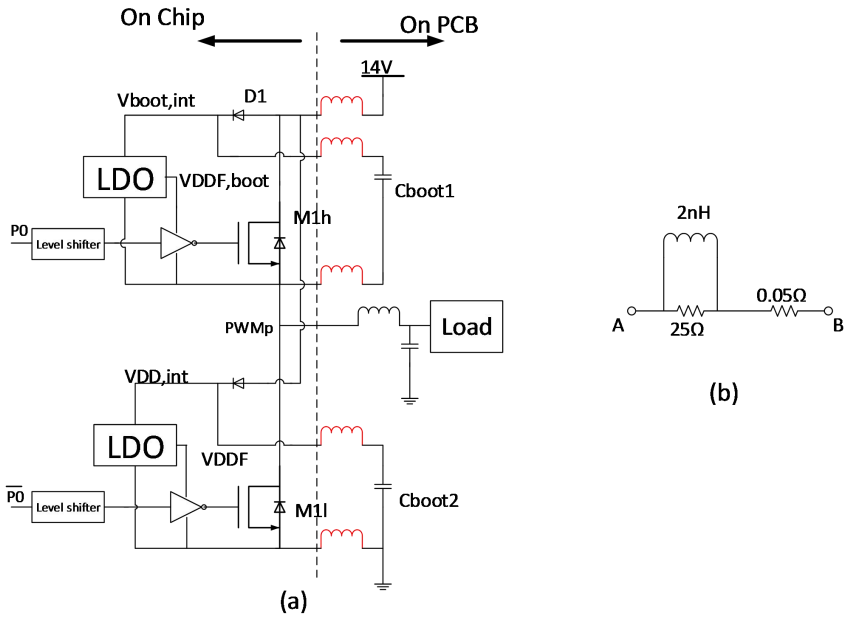


Figure 3.17: (a) Bond wire location, (b) Bond wire model

Requirements

The structure of an LDO is shown in Figure 3.18. The main output current from the LDO goes through the gate driver. When the PMOS of the gate driver is on, the source of M2 is connected to the large parasitic gate capacitance of the output transistor. When the PMOS of the gate driver is off, the source of M2 is not connected to that capacitor. Since the load of M2 changes significantly over time, it is hard to build a stable loop if the feedback is connected to the source of M2. M1 is used to

represent M2 in the feedback loop. Two high voltage cascode transistors are used to protect M1 and M2. Since M2 has a large W/L ratio, using a low voltage transistor can save area [10]. The dominant pole of this LDO loop is at the gate of M1 and M2. C1 is added to move the dominant pole to a lower frequency for loop stability. Because the reference voltage is Vpwm+1.2V, the output of the LDO is Vpwm+3.3V, and R1/R2 is 210kΩ/120kΩ. C2 is used to avoid the spike in output. A 100uA current source, Is, is used to maintain minimum current for the M2 branch. Is is achieved with a current mode level shifter; this circuit will be discussed in Section 3-5-4.

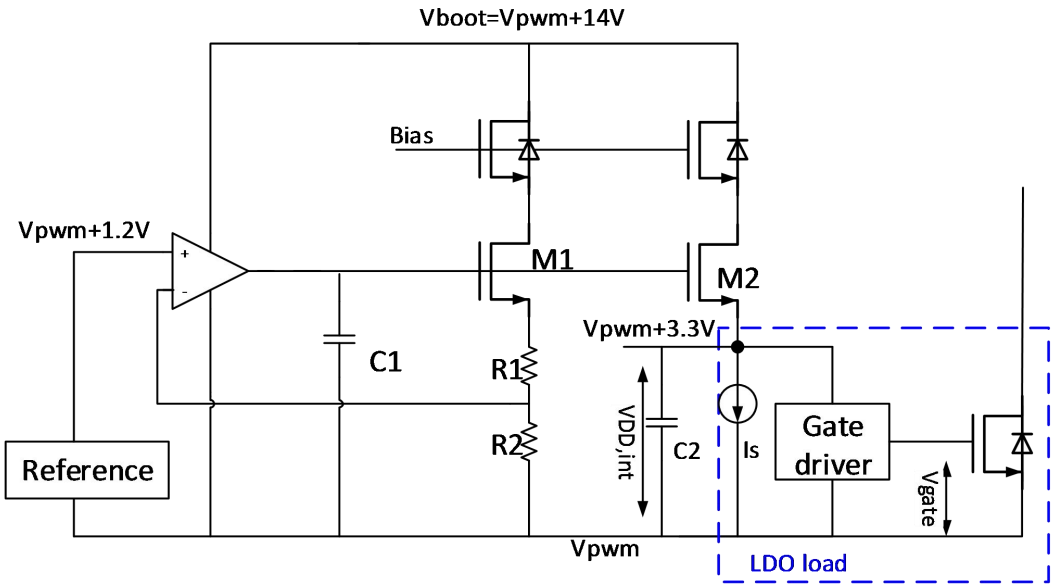


Figure 3.18: Structure of the LDO

LDO Design

M2 is the main transistor of the LDO. Since current flows through M2 to load, the size of M2 is very important in LDO design. M1 is a 1.8V device with the minimum size. The W/L is 0.768/0.16. If M2 is too small, the maximum output current is limited by the size of M2. The transition of Vgate will be slow because of the LDO, resulting in extra power loss. A large M2 needs a larger area and thus a larger parasitic capacitor. A simple LDO model with ideal OPA and ideal reference is used to estimate the power loss caused by LDO finite output current. As Table 3.3 shows, an M2 with 3000×(0.768μm/0.16μm) is a better choice for both area and efficiency.

Table 3.3: Maximum efficiency with different sized M2s

	M2	Maximum efficiency
(1)	2000×(0.768μm/0.16μm)	89.6%
(2)	3000×(0.768μm/0.16μm)	91.0%
(3)	4500×(0.768μm/0.16μm)	91.0%

Reference circuit Design

As shown in Figure 3.19, every LDO needs a reference voltage Vpwm+1.2V. There are two ways to generate that reference voltage. One is presented in [10], where the bandgap is built for each output transistor. The other involves building one bandgap in the low voltage domain, supplied by 1.8V, then referring it to the output transistor by using current. This design utilizes the latter. The reference circuit is shown in Figure 3.19. I1 is first copied to I2, then to I3 by current mirrors. M1, M2, and M3 are identical transistors, while R1 and R3 are identical resistors. PWM+1.2V can be achieved with this design.

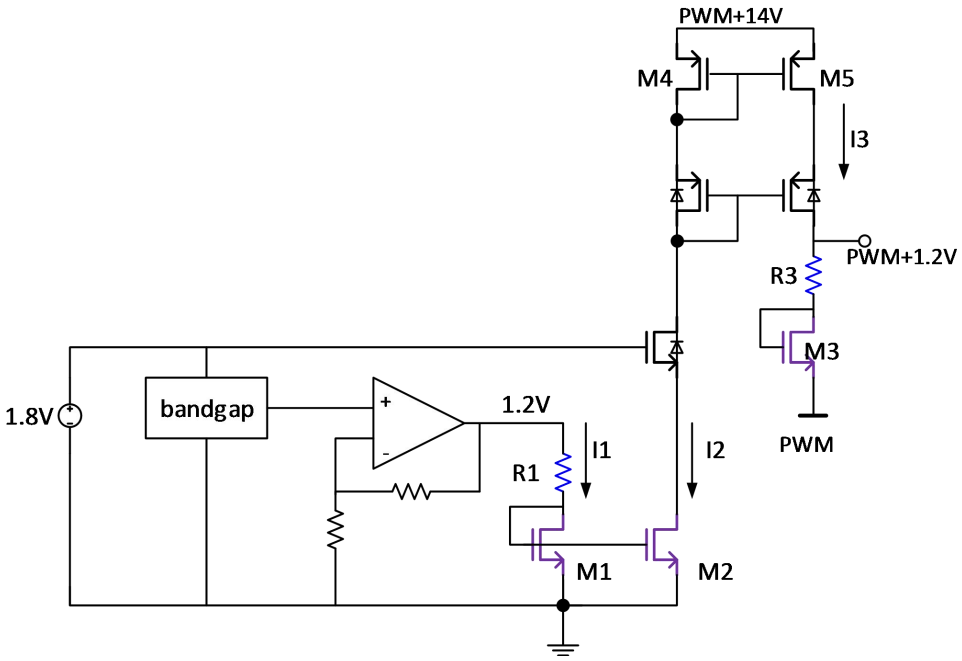


Figure 3.19: Reference circuit of the LDO

Simulation results

In order to show how the LDO filters the ringing, another structure is shown in Figure 3.20(b) without the LDO. A 3.3V supply and charge diode is used to generate 3.3V for the gate driver. As Figure 3.20 (c) shows, because of the parasitic inductor, the supply voltage is noisy. From the simulation result, the LDO helps to generate a relatively clean supply for the gate driver.

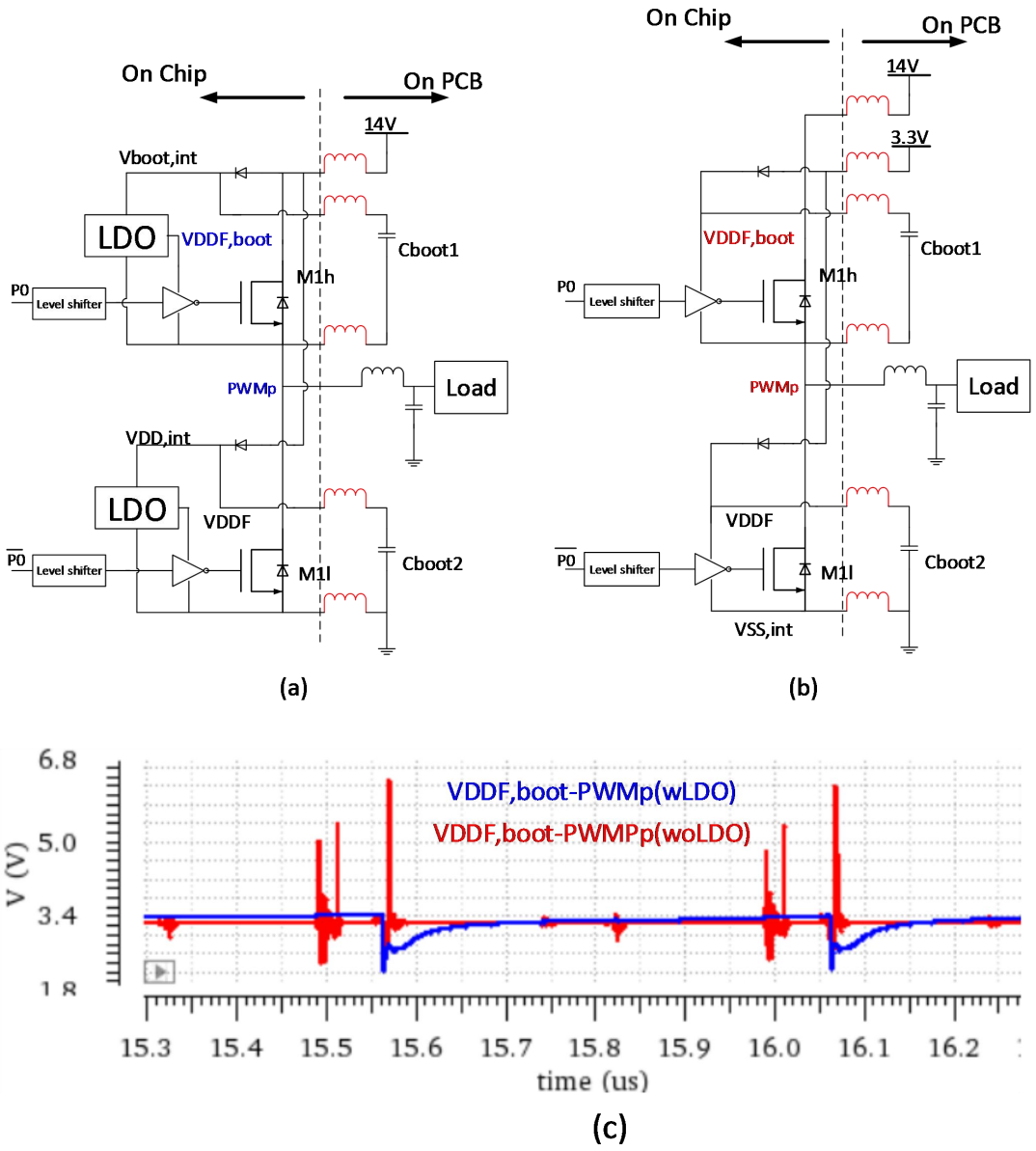


Figure 3.20: (a) Output stage with the LDO, (b) Output stage without the LDO, (c)Waveform of (a) and (b)

3-5-4 Level shifter

Requirements

As Figure 3.21 shows, the PWM signal passes through the deadtime generator and generate HS_in and LS_in. Two level shifters are used to transfer the PWM logic to the output transistors. The output of the level shifter HS cell is referenced to PWM, where the zero logic voltage is PWM, and the one logic voltage is PWM+3.3V. The output of the level shifter LS cell is referenced to ground, where the zero logic voltage is ground, and the one logic voltage is 3.3V. Therefore the level shifter HS cell has a flowing reference while the level shifter LS cell has a constant reference. Figure 3.22 shows the waveform of these two level shifters. As Figure 3.22 (a) shows, if the delay of the level shifter is not related to the reference voltage, the level shifter output

deadtime (tdo1) is equal to the input deadtime (tdi), which is set by the deadtime generator. If the delay of the level shifter is related to the reference voltage as shown Figure 3.22 (b), for example, the level shifter LS cell has a longer delay than the level shifter HS cell. The output deadtime of the level shifters tdo2 is not equal to tdi. The output deadtime of the level shifters may disappear or become negative with more delay difference between the two level shifters.

To ensure the deadtime of output is well defined by the previous deadtime generator, the delay of the level shifter should not be related to the reference.

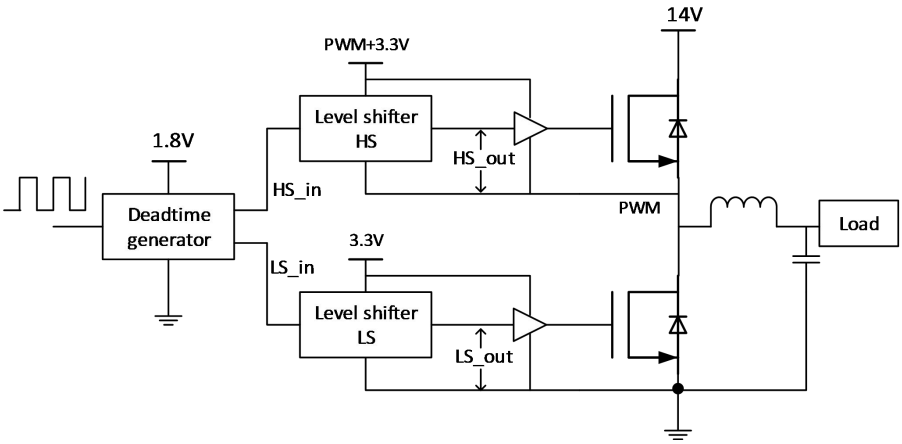
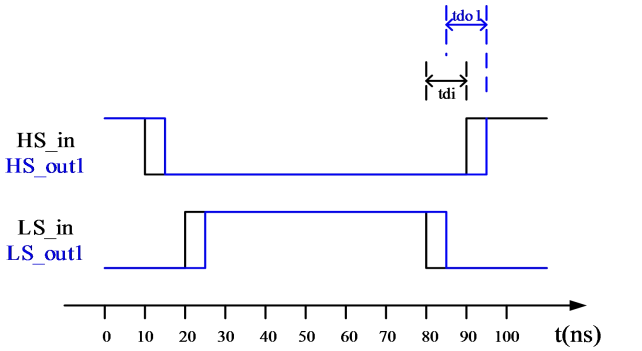
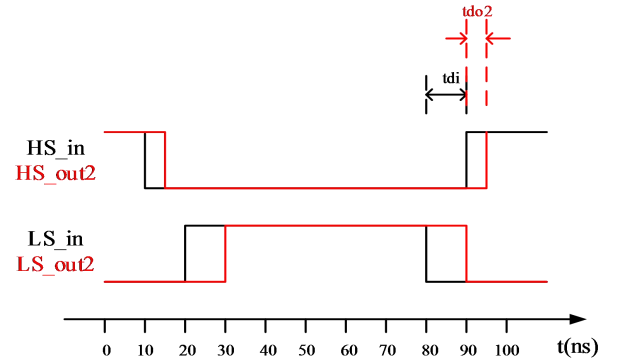


Figure 3.21: Signal transfer path



(a) if the delay of level shifter is not related to the reference voltage



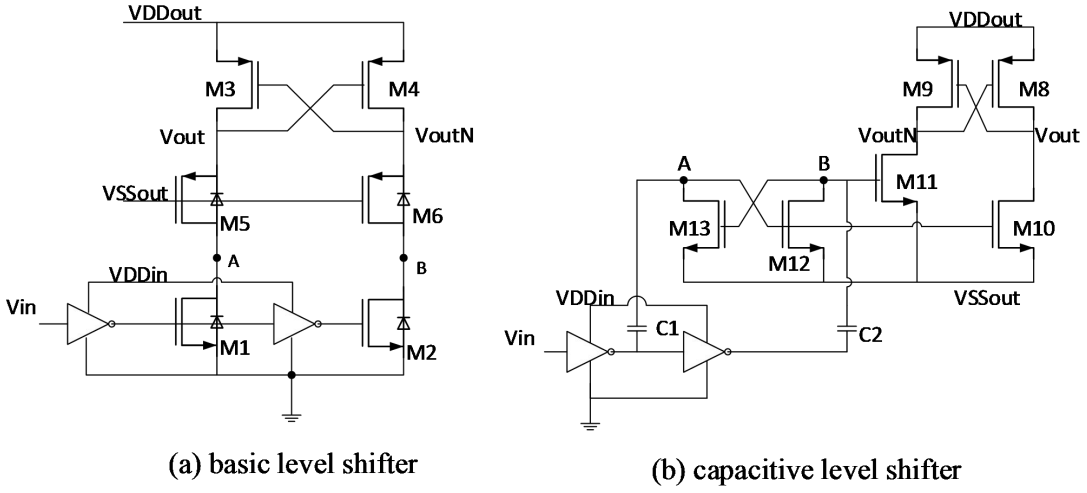
(b) if the delay of level shifter is related to the reference voltage

Figure 3.22: Waveform of the level shifter

Design

There are several types of level shifter circuit. Figure 3.23 (a) shows a basic implementation. The latch is formed by M3 and M4. Transistors M5 and M6 are used to limit the voltage on Vout and VoutN. If Vin is high, B is pulled down to ground by M2, while VoutN is pulled down to VSSout+|Vth|. On the other side, Vout is pulled up to VDDout by M3, and A is pulled up by M5 to VDDout. As Vin goes low, A and Vout are pulled down instantly. However, since M3 is still on, Vout is not pulled down completely. In this situation, there is a current path through M3, M5, and M1, from VDDout to ground. On the other side, M4 is partially on, and B and VoutN are pulled up to VDDout slowly. When VoutN is pulled up to VDDout, then M3 is off, pulling Vout down to VSSout+|Vth|. The delay occurs when M3 and M1 are conducting at the same time, causing them to counteract each other. Therefore, this level shifter is relatively slow, with a delay of around 100ns, which cannot satisfy the delay requirement. Moreover, the output signal is not a full swing [9].

A capacitive level shifter, as shown in Figure 3.23 (b), is another option. The voltage on C1 and C2 is equal to VSSout. When Vin is high, B is bootstrapped to Vssout+VDDin by C2, and A is VSSout. Additionally, M12 and M10 are off, whereas M11 and M13 are on. VoutN is pulled down by M11 to VSSout, while Vout is pulled up by M8 to VDDout. This level shifter is fast and has no static supply current. However, in the Class D amplifier, VSSout is a PWM signal. The voltage on C1 and C2 cannot change immediately, meaning the capacitive level shifter is not a good choice for Class D application.



(a) basic level shifter (b) capacitive level shifter

Figure 3.23: Level shifters

This design uses the current mode level shifter as shown in Figure 3.24. When Vin is high, M1 is on, the current from current source flows through R1, and the voltage drop on R1 is around 3.3V. When M3 is on, Vout has the same voltage with PWM. When Vin is low, current flows through R2, causing M4 to be on. Vout is PWM+3.3V. Vout is logic output referenced to PWM. A static current is needed for this current mode level shifter. The PWM+3.3V is from the LDO, so this static current

also flows through the LDO and providing minimum current to keep the LDO active. The static current is 100μA in this design.

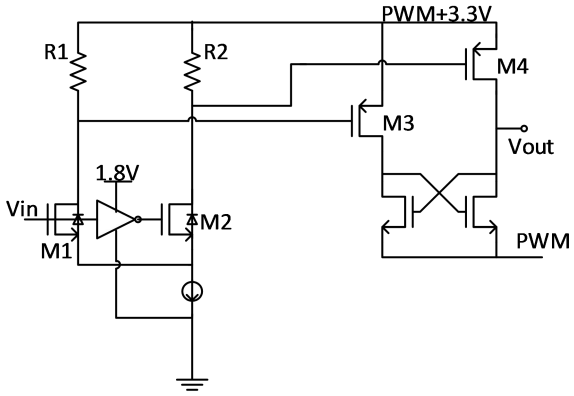


Figure 3.24: Current mode level shifter

Simulation results

Figure 3.25 shows the simulation results of the level shifters. The deadtime before the level shifter tdi is 10ns while the deadtime after level shifter is 10.3ns. This deadtime error is less than the variation (7%) of the deadtime generator itself, therefore it is acceptable for this design.

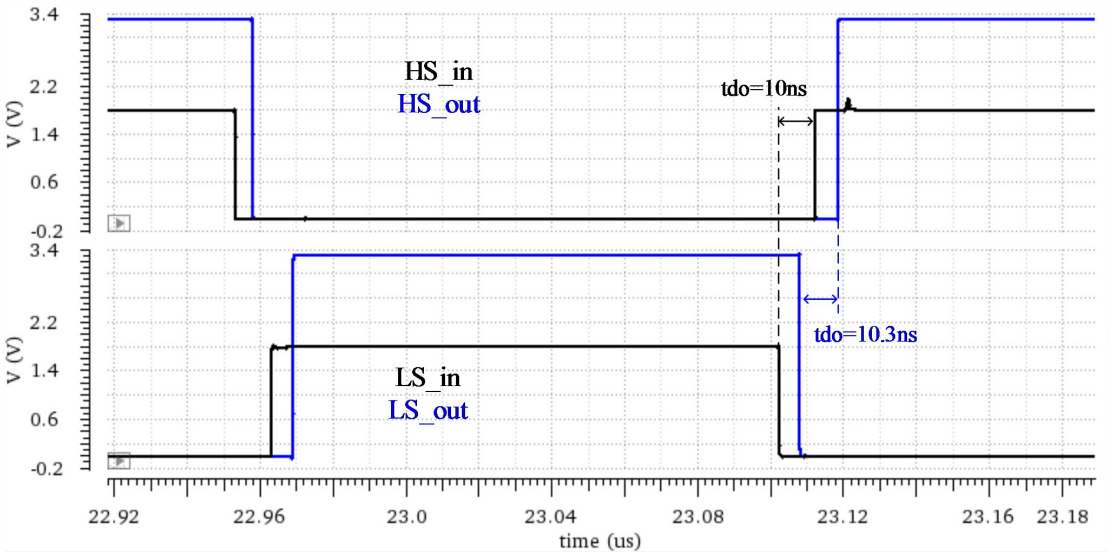


Figure 3.25: Simulation waveform of the level shifter

3-6 Layout

The layout of the design is shown in Figure 3.26. The core occupies an area of 5.2mm×3.8mm. The whole chip including the seal-ring occupies an area of 5.4mm×4.0mm.

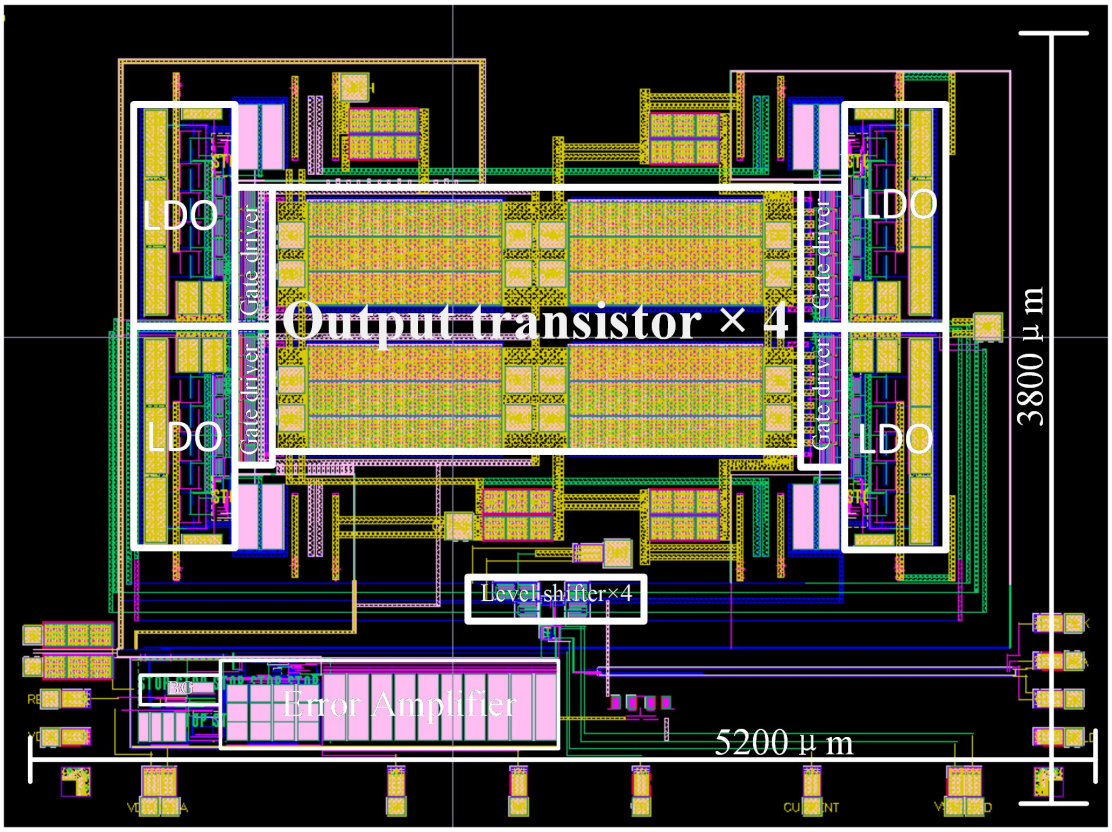


Figure 3.26: Layout of this Class D amplifier

The chip will be taped out in a 140nm bipolar CMOS DMOS SOI process and will be packaged in a 24-pin package.

Chapter 4

Simulation results

In this chapter, the simulation result of the whole system will be shown. In the first part, maximum efficiency is simulated with a large sine wave input. Next is the idle power consumption. Then linearity and noise is discussed. The last section presents a comparison with other designs.

4-1 Efficiency

Figure 4.1 shows the simulation of efficiency versus output power.

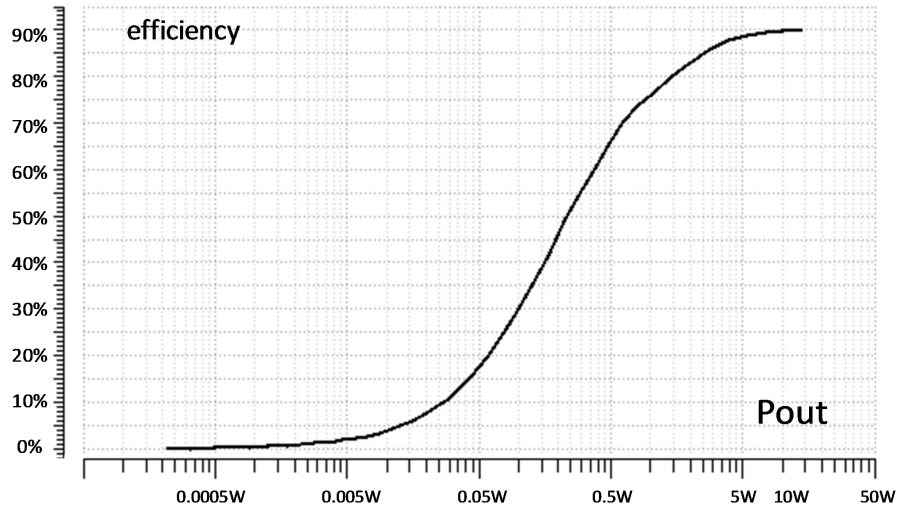


Figure 4.1: Efficiency versus output power

The maximum efficiency is simulated with a 20kHz output sine wave. The amplitude of the output is the maximum output it can achieve without visible distortion. As Table 4.1 shows, for higher temperature, Ron is higher, decreasing efficiency. The efficiency of the zero deadtime mode and efficiency of the 10ns deadtime mode are similar.

Table 4.1: Maximum efficiency of this Class D amplifier

Deadtime (ns)	T (℃)	Efficiency
0	27	91.2%
10	27	91.2%
0	100	89.6%
10	100	89.5%

The contribution ratio of different dissipation sources is shown in Table 4.2 (deadtime=0ns, T=27 ℃). Conduction loss is slightly higher than half of the dissipation.

Table 4.2: List of main dissipation sources of maximum power

Dissipation source	Value	Ratio
Conduction loss	1.09W	62.6%
Gate driver loss	0.49W	28.2%
Capacitive loss + switching loss	0.16W	9.2%
Power loss	1.74W	100%

The expression of the conduction loss is:

$$P_{conduction} = P_{out} \times \frac{2R_{on}}{4\Omega} \tag{4.1}$$

4-2 Idle power consumption

This design has a relatively high idle power consumption because of the high switching frequency. As ripple loss is related to ripple current, when input is zero, the PWM duty is 50%, resulting in ripple loss that is not negligible [11].
The expression of ripple loss is:

$$P_{ripple} = \frac{1}{3} I_{ripple}^2 \left(2R_{on}\right) \tag{4.2}$$

for which, I_{ripple} is the ripple current through the inductor, the simulation value of I_{ripple} is 0.9A, and Ron is the on-resistance of the output transistor. In this design the value of Ron at room temperature is 0.11Ω.

The contribution ratios of different dissipation sources are shown in Table 4.3. Gate driver loss is the main part of the idle power dissipation.

Table 4.3: List of the main dissipation sources of idle power

Dissipation source	Value	Ratio
Ripple loss	59mW	12.8%
Gate driver loss	344mW	74.4%
Capacitive loss + switching loss	59mW	12.8%
Idle power	462mW	100%

4-3 Linearity

4-3-1 The transfer function of the Class D stage

As stated in Section 3-4-1, the deadtime introduces a signal-related distortion. The transfer function of the Class D stage has been simulated.

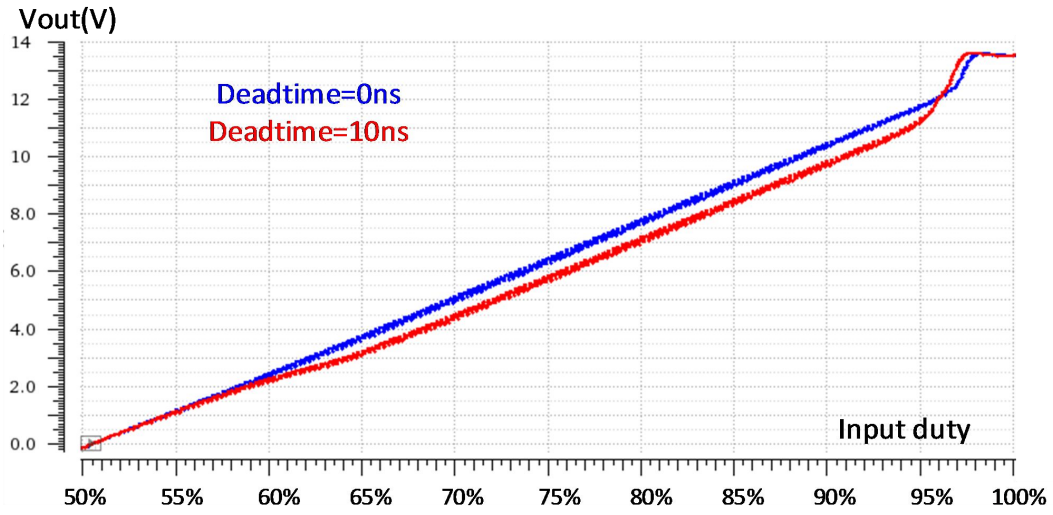


Figure 4.2: Input duty versus output voltage

As Figure 4.2 shows,

1) When the input duty is from 50% to 60%, the signal does not cross the deadzones, the deadtime does not cause distortion. An output sine wave has a power much lower than 1W cannot see the effect of deadtime.

2) When the input signal is large, the input duty is higher than 60%, the signal crosses the deadzones, the deadtime causes gain loss. An output sine wave has a power higher than 1W can see the effect of deadtime.

3) The 10ns deadtime mode clips earlier than the 0ns deadtime mode.

4-3-2 THD

THD is simulated with a 1kHz sine wave input. Different output power levels with different deadtime modes have been simulated.

As Table 4.4 and Figure 4.3 shows,

1) When output power is 0.25W, the 10ns deadtime mode and the 0ns deadtime mode show similar THD.

2) When output power is higher than 1W and sine wave is not clipping, the 0ns deadtime mode has a better THD than the 10ns deadtime mode.

3) For the 0ns deadtime mode, THD at 20W output power is better than THD at 10W output power. While for the 10ns deadtime mode, THD at 20W output power is worse than THD at 10W output power.

4) When simulated the 10%THD, the output waveform of both modes are clipped, they have the same maximum output power in such a definition.

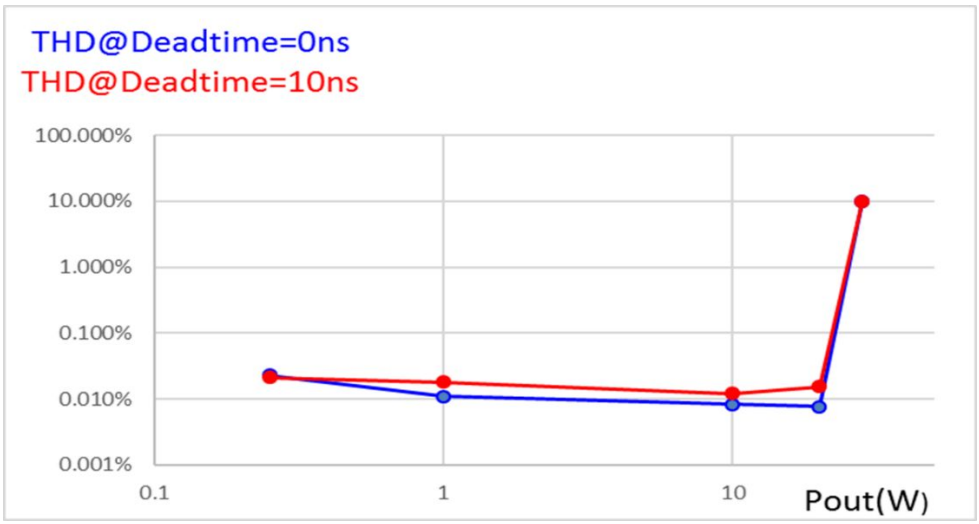


Figure 4.3: THD versus output power

Table 4.4: THD of different output power at 1kHz

Output power	0.25W	1W	10W	20W	28.1W
THD@Deadtime=0ns	0.023%	0.011%	0.0083%	0.0076%	10%
THD@Deadtime=10ns	0.021%	0.018%	0.012%	0.0153%	10%

4-4 Dynamic range

The gain of this amplifier is 7, the total input referred noise is 6.26μVrms, and the total output referred noise is 43.8μVrms. The maximum amplitude of the sine wave output is 12.6V. The Dynamic range is:

$$DR = \frac{P_{out,\max}}{P_{noise}} = \frac{12.6^2}{(4.38 \times 10^{-5})^2} = 8.28 \times 10^{10} = 109dB \qquad (4.3)$$

4-5 Performance summary

TEXAS INSTRUMENTS(TI) has produced the TAS6424-Q1 [13], which is a Class D audio amplifier which switches at 2MHz. The switching frequency of this design is similar to that amplifier. The following is a comparison between this design and the TAS6424-Q1.

Table 4.5: Comparison between the TAS6424-Q1 and this design

	TAS6424-Q1	This design
Feedback topology	Before filter	After filter
Ron of output transistor	90mΩ	109mΩ
Switching frequency	2.1MHz	2.1MHz
Supply voltage	14.4V	14V

Load	BTL 4Ω	BTL 4Ω	
Output noise	42μVrms	44μVrms	
Deadtime(ns)	-	0	10
THD@1W(1kHz)	0.02%	0.011%	0.018%
THD@10W(1kHz)	0.06%	0.0083%	0.012%
Max output power@10%THD	27W	28.1W	28.1W
Max efficiency	86%	91.2%	91.2%

This design uses the same switching frequency as the TI audio amplifier, but uses a different feedback topology. The result is a better THD and higher efficiency.

Chapter 5

Conclusion

5-1 Thesis contribution

A PWM modulation Class D audio amplifier with a 2.1MHz switching frequency has been presented in this thesis. The contributions of the thesis are summarized below:

- A small inductor is used. The simulation results show that this Class D amplifier can achieve a similar performance as other designs.
- The effect of deadtime has been simulated. The results show that, when the signal is large but not clipping yet, the linearity worsens with an increase in deadtime.
- This Class D audio amplifier achieves a better THD and efficiency than the TI amplifier counterpart, with a similar switching frequency, supply voltage and load.

5-2 Future work

On-chip measurements are required to evaluate the performance of the different mode. Since the 2.1MHz triangle signal is generated from a PCB, it can be changed.

- The relationship between EMI and the frequency of this triangle signal should be evaluated.
- Push-pull modulation performance should be investigated.

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