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A 0.25 mm^2-Resistor-Based Temperature Sensor With an Inaccuracy of 0.12 °C (3σ) From −55 °C to 125 °C

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***Abstract*— This paper describes a compact, energy efficient, resistor-based temperature sensor that can operate over a wide temperature range (−55 °C–125 °C). The sensor is based on a Wheatstone bridge (WhB) made from silicided poly-silicon and non-silicided poly-silicon resistors. To achieve both area and energy efficiencies, the current output of the WhB is digitized by a continuous-time zoom analog-to-digital converter (ADC). Implemented in a standard 180-nm CMOS technology, the sensor consumes 52 μA from a 1.8-V supply and achieves a resolution of 280 μK_{rms} in a 5-ms conversion time. This corresponds to a state-of-the-art resolution figure-of-merit (FoM) of 40 fJ · K^2. After a first-order fit, the sensor achieves an inaccuracy of ±0.12 °C (3σ) from −55 °C to 125 °C.**

***Index Terms*— Continuous-time delta–sigma modulator (CTΔΣM), energy efficiency, non-linearity correction, smart sensors, temperature sensor.**

I. Introduction

TO STABILIZE their outputs over temperature, frequency references based on MEMS or XTAL resonators usually employ temperature compensation schemes [1]–[6]. In order not to degrade the reference's jitter performance, such schemes require high-resolution temperature sensors [1]. These should also be highly energy efficient, so as not to impact the reference's overall energy consumption, and be as compact as possible.

Temperature sensors based on dual-MEMS resonators have demonstrated superb stability, resolution, and energy efficiency [1]. However, their fabrication in a non-CMOS process results in increased complexity and cost. In standard CMOS technologies, temperature sensors based on bipolar junction transistors (BJTs) [7]–[9], MOSFETs [10], [11], resistors [2]–[6], [12]–[15], and even electrothermal filters [16], [17] can be made. In terms of their resolution figure-of-merit (FoM) [18], however, the energy efficiency of resistor-based sensors is currently about two orders of magnitude greater than that of other types of CMOS temperature sensors [19]. They can also achieve high (sub-mK) resolution and areas as low as 0.1 mm^2 [14], [15].

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Depending on their choice of reference, two classes of resistor-based temperature sensors can be identified: *RC*-based sensors [2]–[4], [6], [14], which use a frequency reference to digitize a temperature-dependent *RC* time constant; and dual-resistor-based sensors [5], [12], [15], which digitize the resistance of a sensing resistor with respect to another resistor. As discussed in [20], *RC*-based sensors can achieve better stability and accuracy, because on-chip MIM capacitors are more stable and spread less than on-chip resistors. However, they require the availability of an equally accurate and stable (external) frequency reference. On the other hand, dual-resistor-based sensors can be used in a standalone manner and can be more energy efficient, as their sensitivity can be boosted by using resistors with complementary temperature coefficients (TCs.) In both cases, good accuracy (about 0.1 °C over the industrial temperature range) can be achieved after a two-point calibration [6], [12]. This paper will focus on the design of an area-efficient temperature sensor that employs silicided and non-silicided poly resistors in a Wheatstone bridge (WhB) configuration.

According to a recent survey [21], bridge-to-digital converters (BDCs) based on the combination of an instrumentation amplifier and an analog-to-digital converter (ADC) [22], [23] can achieve excellent energy efficiency, resolution, and accuracy. However, they occupy significant area (>0.7 mm^2). Voltage-controlled oscillator (VCO)-based BDCs [24] can be very compact (0.06 mm^2 in 40-nm CMOS), at the expense of energy efficiency. A compact BDC based on a hybrid flash/SAR ADC occupies only 0.044 mm^2 in 65-nm CMOS [15]. However, this was achieved at the expense of resolution (0.12 °C$_{rms}$).

Rather than reading out its open-circuit voltage, an alternative way of reading out a bridge is to measure its short-circuit output current. Current-readout WhB sensors based on continuous-time delta–sigma modulators (CTΔΣMs) are quite energy efficient, achieving resolution FoMs of 650 [5] and 49 fJ · K^2 [12], respectively. However, the latter occupies significant area: 0.72 mm^2 in a 180-nm technology, mainly due to the area of the CTΔΣM's integrating capacitors.

In this paper, a multi-bit CTΔΣM is proposed to replace the single-bit CTΔΣM used in [12]. Its multi-bit digital-to-analog converter (DAC) compensates the output current of the bridge more accurately, thus reducing the swing at the input of the modulator's loop filter. As a result, both the size of the required integration capacitors as well as the ADC's power dissipation can be significantly reduced.

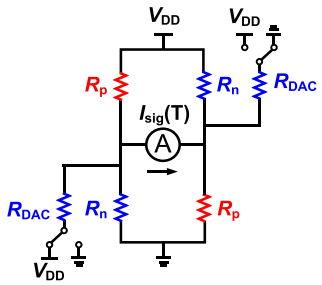

Fig. 1. WhB sensor and DAC using current readout.

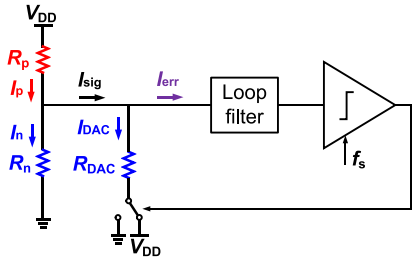

Fig. 2. CTΔΣM-based bridge readout.

The rest of this paper is organized as follows. Section II discusses the design of a zoom ADC based on a multi-bit CTΔΣM. Section III presents the circuit implementation. Measurement results and a comparison with the state-of-the-art are given in Section IV, and finally, conclusions are drawn.

II. Architecture Design

A. Wheatstone Bridge Readout and CTΔΣM

As shown in Fig. 1, the sensor consists of a WhB made from two types of resistors with positive and negative TCs: $R_p(T)$ and $R_n(T)$. For high sensitivity and stability, R_p and R_n are silicided-p-poly and non-silicided n-poly resistors, respectively [12]. A parallel resistor DAC (also made from R_n-type resistors) can then be used to cancel the bridge's temperature-dependent output current $I_{sig}(T)$. As shown in Fig. 2, the DAC forms part of a CTΔΣM, which drives the average value of $I_{err}(T)$ to zero by switching the DAC's resistors either to V_{DD} or GND and thus effectively balancing the bridge [5].

The temperature dependence of the various resistors in the WhB and in the DAC can be modeled as follows [5]:

$$\begin{aligned} R_p(T) &= R_p(T_0)\cdot(1+TC_{p1}\cdot\Delta T+TC_{p2}\cdot\Delta T^2)\\ R_n(T) &= R_n(T_0)\cdot(1+TC_{n1}\cdot\Delta T+TC_{n2}\cdot\Delta T^2)\\ R_{DAC}(T) &= R_{DAC}(T_0)\cdot(1+TC_{n1}\cdot\Delta T+TC_{n2}\cdot\Delta T^2). \end{aligned} \tag{1}$$

Here, $R_p(T_0)$, $R_n(T_0)$, and $R_{DAC}(T_0)$ are the resistances at a reference temperature T_0, while TC_{p1} and TC_{n1} are their first-order TCs, TC_{p2} and TC_{n2} are their second-order TCs, and ΔT is the temperature with respect to T_0. Noting that the active integrator virtually shorts the bridge's output terminals to $V_{DD}/2$ while the modulator ensures that the integrator's average input current I_{err} is 0, the bitstream average μ_{ADC} can be expressed as

$$\begin{aligned} \mu_{ADC} &= \frac{I_{sig}(T)}{I_{DAC}(T)} = \frac{1/R_p(T)-1/R_n(T)}{1/R_{DAC}(T)}\\ &= \frac{R_{DAC}(T_0)}{R_p(T_0)}\cdot\frac{(1+TC_{n1}\cdot\Delta T+TC_{n2}\cdot\Delta T^2)}{(1+TC_{p1}\cdot\Delta T+TC_{p2}\cdot\Delta T^2)}\\ &\quad-\frac{R_{DAC}(T_0)}{R_n(T_0)}\\ &= \frac{R_{DAC}(T_0)}{R_p(T_0)}\cdot f_{pn}(\Delta T)-\frac{R_{DAC}(T_0)}{R_n(T_0)}. \end{aligned} \tag{2}$$

Within a batch, the function f_{pn} only depends on the resistors' TCs and so will be a constant but non-linear function of temperature. The ratio R_{DAC}/R_p involves different types of resistors and so will spread significantly, while the ratio R_{DAC}/R_n involves the same type of resistors and so should spread less. As such, (2) implies that a two-point trim will be needed to fully compensate for the effects of spread.

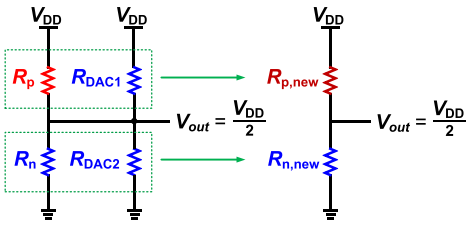

Fig. 3. Balanced WhB with R_{DAC} split and merged.

B. Temperature Sensing Resolution

With a sinc[1] filter, the temperature sensing resolution of a balanced WhB can be expressed as [20]

$$\Delta T_{WhB} = \frac{2}{V_{DD}\cdot(TC_{p1}-TC_{n1})}\cdot\sqrt{\frac{2kTR}{t_{conv}}} \tag{3}$$

where $R = R_p = R_n$ is the bridge resistance and t_{conv} is the conversion time.

Since R_{DAC} is switched between V_{DD} and GND, it can be modeled by two resistors, R_{DAC1} and R_{DAC2} as shown in Fig. 3. In order to balance the bridge, their resistances must satisfy

$$\begin{aligned} R_{DAC} &= R_{DAC1}/\!/R_{DAC2}\\ R_p/\!/R_{DAC1} &= R_{p,new} = R_{n,new} = R_n/\!/R_{DAC2}. \end{aligned} \tag{4}$$

From (4), R_{DAC1} can be expressed as

$$R_{DAC1} = \frac{2}{1/R_n-1/R_p+1/R_{DAC}} \tag{5}$$

and the first-order TC of $R_{p,new}$ can be calculated as

$$TC_{p1,new} = \frac{R_p\cdot TC_{n1}+R_{DAC1}\cdot TC_{p1}}{R_p+R_{DAC1}} \tag{6}$$

which is always less than TC_{p1}. The TC of $R_{n,new}$ is not affected since it consists of two resistors of the same type.

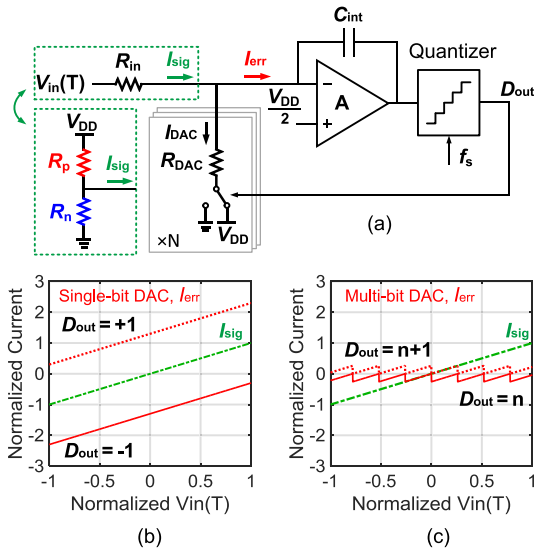

Fig. 4. (a) CT$\Delta\Sigma$M based on an active integrator. (b) Error current of a single-bit CT$\Delta\Sigma$M. (c) Error current of a multi-bit CT$\Delta\Sigma$M.

Thus, (2) can be updated as

$$\Delta T_{\mathrm{WhB}} = \frac{2}{V_{\mathrm{DD}} \cdot (TC_{\mathrm{p1,new}} - TC_{\mathrm{n1}})} \cdot \sqrt{\frac{2\,\mathrm{k}T R_{\mathrm{new}}}{t_{\mathrm{conv}}}} \quad (7)$$

where $R_{\mathrm{new}} = R_{\mathrm{p,new}} = R_{\mathrm{n,new}}$. Therefore, the presence of the resistive DAC (RDAC) decreases the bridge's sensitivity and thus its temperature sensing resolution.

C. From Single-Bit CT$\Delta\Sigma$M to Multi-Bit CT$\Delta\Sigma$M

The first stage of the CT$\Delta\Sigma$M is basically an active-*RC* integrator, as shown in Fig. 4(a), where the WhB is modeled by a source resistor driven by a temperature-dependent voltage $V_{\mathrm{in}}(T)$. In [12], the sensor's energy efficiency and chip area were limited by the large variation in I_{sig} over process, voltage, and temperature (PVT). This had to be compensated by the output current I_{DAC} of a 1-bit DAC, resulting in an even larger error current I_{err} flowing into the first integrator, as shown in Fig. 4(b). In consequence, the first integrator dissipated about half of the sensor's power, while its integration capacitors occupied 60% of the sensor's area.

A multi-bit resistor DAC ($N > 1$) can be used to reduce the magnitude of I_{err} [Fig. 4(c)]. Since most of I_{sig} will then be compensated by I_{DAC}, the first integrator's supply current, as well as the size of its integration capacitors, can be significantly reduced.

D. Integrator Nonlinearity and Noise in Multi-Bit CT$\Delta\Sigma$Ms

Nonlinearity is a key challenge in multi-bit $\Delta\Sigma$Ms. For CT$\Delta\Sigma$Ms with RDACs, the two major contributors are RDAC mismatch and the non-linearity of the first integrator. RDAC mismatch can be sufficiently suppressed by careful layout and dynamic element matching (DEM). The non-linearity of the first integrator, however, is more problematic.

In multi-bit CT$\Delta\Sigma$Ms, integrator nonlinearity increases in-band noise (IBN) [25], which, in our case, will degrade the sensor's resolution. This can be understood intuitively by considering Fig. 5(a), in which the nonlinearity of the first integrator is modeled by $f_y(x)$. This can then be shifted to the input of the modulator and to the output of the DAC, as shown in Fig. 5(b). The resulting non-linear DAC will then cause quantization noise folding and raise IBN. Being signal dependent, it cannot be mitigated by DEM. Increasing the linearity of the first stage would help, but this usually comes at the expense of higher power dissipation.

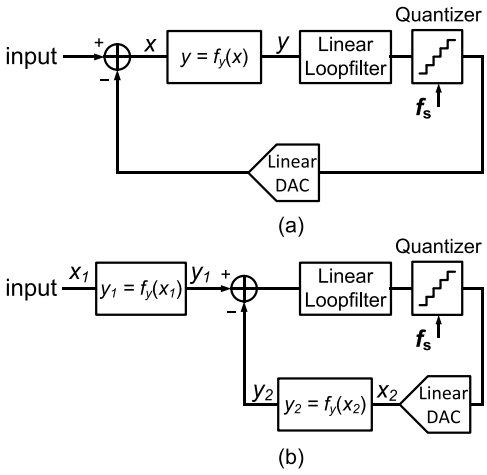

Fig. 5. (a) Nonlinearity modeling of the zoom CT$\Delta\Sigma$M. (b) Equivalent model of (a).

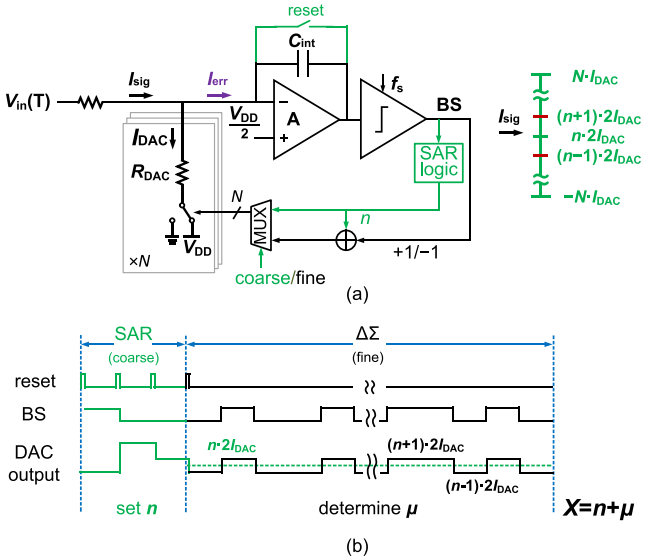

Fig. 6. (a) Schematic of a static zoom CT$\Delta\Sigma$M and (b) timing diagram example in case of a 3-bit DAC.

E. Zoom CT$\Delta\Sigma$M

During the fine conversion of a zoom $\Delta\Sigma$M, however, only two levels of its multi-bit DAC will be used [8], [26]. As a result, the DAC will still appear to be perfectly linear even in the presence of integrator non-linearity, and so, no quantization noise folding will occur [27].

The proposed zoom CT$\Delta\Sigma$M digitizes the temperature-dependent ratio $X = I_{\mathrm{sig}}/(2I_{\mathrm{DAC}})$ in two steps, as illustrated in Fig. 6, for the case of a first-order modulator. First, a coarse

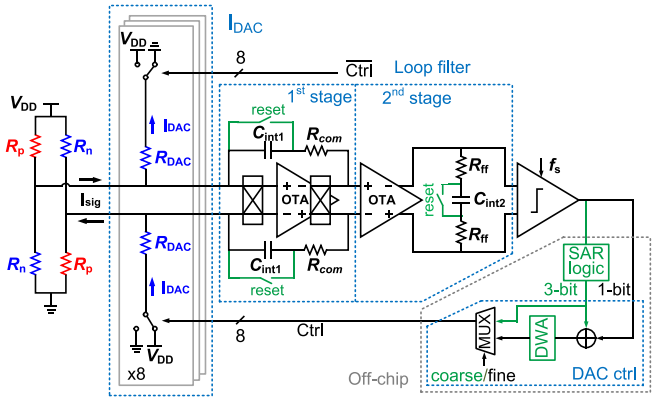

Fig. 7. Circuit diagram of the zoom CTΔΣM.

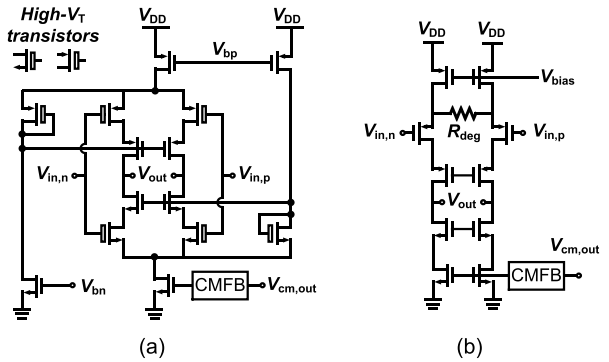

Fig. 8. Schematic of (a) current-reuse OTA in the first integrator and (b) source-degenerated OTA in the second stage.

SAR conversion determines the integer part n of X. Then, the fractional part μ is determined by a fine $\Delta\Sigma$ conversion. Compared to the complexity of conventional multi-bit $\Delta\Sigma$Ms, a zoom ADC only requires a single-bit comparator, a reset switch for the first integrator and some logic.

During the coarse conversion, the first integrator is used as a pre-amplifier for the comparator [8]. Each step of the SAR conversion then consists of choosing a DAC code, resetting the first integrator and then integrating the resulting error current for one clock cycle. The polarity of the result is detected by the comparator and used to determine the next DAC code to test. To absorb small errors from the SAR conversion and ensure that μ lies in the modulator's stable input range, over-ranging is used. This is implemented by switching the DAC between the codes $n-1$ and $n+1$ during the delta–sigma phase [Fig. 6(b)]. Since this range is significantly smaller than the full range of the DAC, the linearity and power dissipation of the first integrator can be significantly relaxed.

III. Circuit Implementation

A. Wheatstone Bridge and RDAC

In contrast to previous WhB sensors [5], [12], [15], this sensor is designed to operate over the military temperature range (−55 °C–125 °C). As a result, the bridge is unbalanced at room temperature (RT, about 25 °C), with $R_p = 100$ kΩ and $R_n = 80$ kΩ. With a 1.8-V supply, this results in $|I_{sig}| < 7$ μA over PVT, which requires a minimum DAC resistance of 120 kΩ. Given $t_{conv} = 5$ ms, $TC_{p1} = 0.29\%/°C$, $TC_{n1} = -0.15\%/°C$, and $V_{DD} = 1.8$ V, then from (5)–(7) ΔT_{WhB} is 130 μK (rms) at RT.

Since the minimum width of the process is fixed, there is a tradeoff between the number of DAC bits and the minimum possible DAC area. To ensure that the areas of the DAC and the integrating caps C_{int} are roughly equal, a 3-bit DAC was chosen, with unit elements of 960 kΩ. As in [8], an extra half-LSB unit element is used at the end of the coarse conversion to determine the optimal choice of the references used in the fine conversion [8].

B. Zoom-Based CTΔΣM

Fig. 7 shows the circuit diagram of the zoom CTΔΣM. To achieve high resolution in a reasonable conversion time, a second-order modulator was chosen with a feed-forward architecture to reduce the swing at the output of the first integrator, and thus further reduce the size of C_{int}. As in [6], the loop is stabilized by a zero realized by the inclusion of R_{ff} in the feedback path of the second integrator.

Since its non-linearity will not increase IBN, the first integrator was optimized mainly for noise. It consists of an energy-efficient current-reuse operational transconductance amplifier (OTA) rather than the two-stage opamp used in [12]. High-Vt input transistors are used to achieve a reasonable output swing (∼0.9 V at RT) [9], as shown in Fig. 8(a). To improve the modulator's stability, the pole of the OTA-based integrator is compensated by inserter $R_{com} = 1/g_m$ in series with C_{int}. To suppress its offset and $1/f$ noise while avoiding quantization-noise fold back, the OTA is chopped at the CTΔΣM's sampling frequency ($f_s = 500$ kHz) [28]. It achieves over 80-dB gain, a gain-bandwidth product (GBW) product of ∼20 MHz and consumes 22 μW at RT, which is about 60% of the power dissipated by the bridge.

As shown in Fig. 8(b), the second stage is based on a source-degenerated cascaded telescopic OTA. It has a dc gain of 80 dB and dissipates 3 μW at RT.

For flexibility, the SAR and data weighted averaging (DWA) logic are implemented off-chip. Since the SAR conversion only involves 3 bits, its duration and power overhead are negligible, and the energy efficiency of the bridge readout is basically defined by the fine conversion. Simulations show that if implemented on-chip, the SAR and DWA logic would consume less than 1 μW and less than 0.01 mm^2 area which are negligible compared to the other circuit blocks.

From simulations, the first-stage OTA's contribution to the modulator's total input-referred noise power is ∼30% of that of the WhB/DAC resistors. To decimate the bit-stream output of the second-order modulator, a sinc^2 filter is adopted, whose effective noise bandwidth is 1.33× that of the sinc filter assumed in earlier calculations. These two factors will reduce the sensor's resolution to about 170 μK (rms) with $t_{conv} = 5$ ms.

C. NonLinearity Analysis

Although the nonlinearity of the first integrator does not impact the IBN of a zoom ADC, it does impact its integral nonlinearity (INL). The main source of non-linearity is the signal dependent g_m of the current-reuse OTA, which

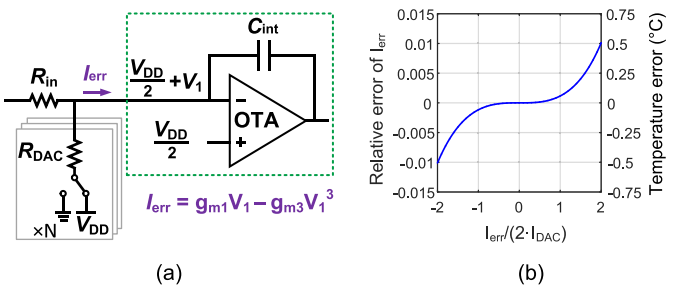

Fig. 9. (a) Nonlinearity of the input resistance of the first stage OTA. (b) Relative error giving different input signal levels.

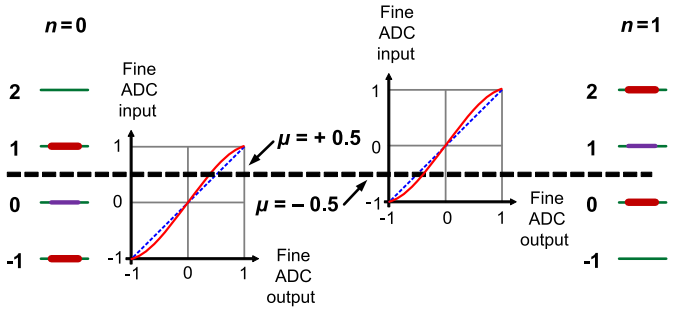

Fig. 10. Readout error of the opposite sign with two possible coarse codes.

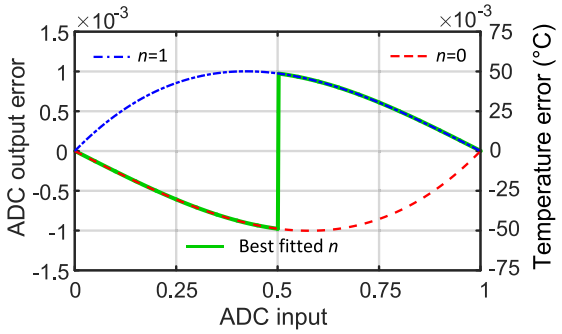

Fig. 11. Temperature error jump when changing n.

can be modeled by the addition of a third-order term g_{m3} [Fig. 9(a)]. The simulated non-linearity in I_{err} is then as shown in Fig. 9(b).

The OTA's non-linearity will cause errors in the bitstream average μ obtained after the fine conversion. These will be a weighted average of the associated errors in the two possible values of the first integrator's input current I_{err}. When $\mu = 0$, however, the bitstream output bs will toggle between $+1$ and -1 with equal probability, and since $I_{err}(\text{bs} = +1) = -I_{err}(\text{bs} = -1)$, the resulting error in μ will be 0. This will also be the case at the extremes of the modulator's input range, because the bridge's output current I_{sig} will then be exactly cancelled by I_{DAC}, and so $I_{err} = 0$. Apart from these three cases, the error of the fine ADC will be non-zero. As shown in Fig. 10, the result is a sinusoidal error curve centered on $\mu = 0$.

Choosing the range of the fine conversion to be exactly equal to two steps of the coarse conversion (two LSB over-ranging) means that there are two different ways to convert a

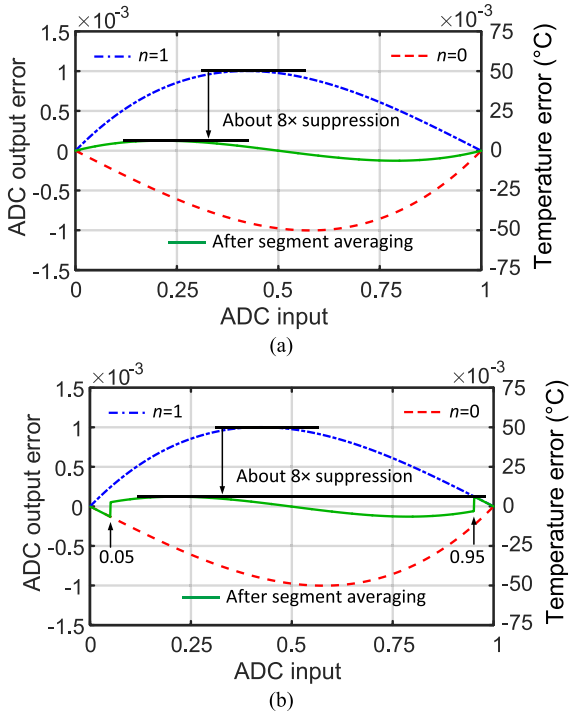

Fig. 12. Nonlinearity suppression using segment averaging (a) without a threshold (b) with a threshold of 0.05.

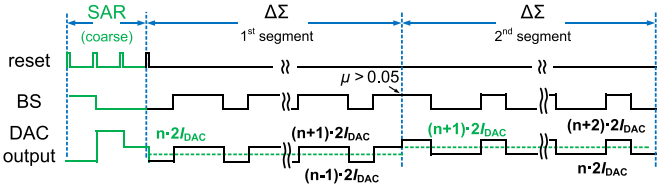

Fig. 13. Modified timing diagram of the zoom CT$\Delta\Sigma$M.

given input current, each corresponding to a different coarse code n. Ideally, the zoom ADC's output X would be the same in both cases. In the presence of OTA non-linearity, however, there will be an error in μ, which will be of opposite polarity in the two cases. As shown in Fig. 11, this means that at the coarse code transitions, i.e., when $\mu = \pm 0.5$, the error in X will abruptly change polarity. Simulations show that the jumps in X at RT can be as large as 0.1 °C, which is significantly larger than the sensor's expected resolution.

D. Segment Averaging

Noting that the errors associated with the two possible n/μ combinations are of opposite polarity, they can be mitigated by simply averaging the values of X obtained from two such conversions, as shown in Fig. 12(a). Simulations show that this approach can reduce the error by about 8×, to about ±5 mK. This approach translates to considerable power savings since without this segment averaging technique, the bias current of the first integrator's OTA would have to be increased by about 2× to obtain similar linearity.

Although the stable input range of a second-order $\Delta\Sigma$M corresponds to $-1 < \mu < 1$ for dc input signals [29], its quantization noise becomes quite large when $|\mu| \sim 1$. To avoid degrading the sensor's resolution in such cases, segment averaging is disabled when $1-|\mu| < 0.05$. As shown

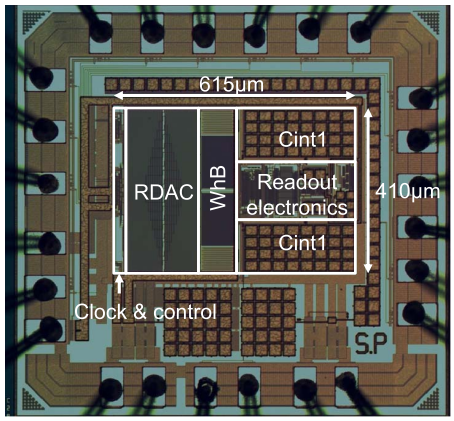

Fig. 14. Die micrograph of the prototype chip.

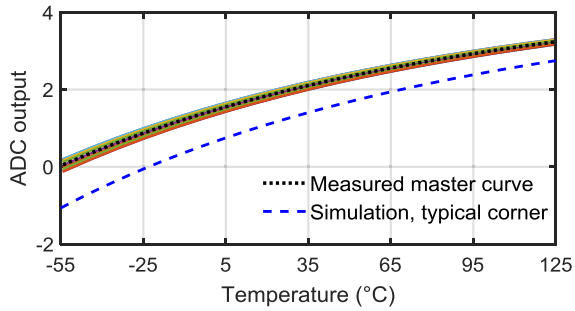

Fig. 15. Measured and simulated sensor output versus temperature.

in Fig. 12(b), this will have little effect on the sensor's linearity, since the nonlinearity is anyway quite small in these cases, and the transitions are blurred by the presence of thermal noise. The associated timing diagram is shown in Fig. 13.

IV. Measurement Results

The sensor is realized in a standard 180-nm CMOS process, with a dimension of 615 μm $\times$ 410 μ m (Fig. 14). At RT, it draws 52 μA from a 1.8-V supply, with over half of this dissipated in the WhB and the DAC. About 15% of the active area is occupied by the WhB, 30% by the DAC resistors, and another 30% by the integration capacitors of the first stage. For supply voltages varying from 1.6 to 2.0 V, the sensor's supply sensitivity is 0.02 °C/V. An off-chip sinc^2 filter is used to decimate the sensor's bitstream output.

A. Temperature Characteristic, NonLinearity Correction, and Calibration

Using a temperature-controlled oven (Vötsch VT7004), 19 chips from the same batch were characterized from −55 °C to 125 °C (in 10 °C steps) in ceramic dual in-line (DIL) packages. The reference sensor was a calibrated Pt-100 RTD. To minimize the effects of oven drift, both the Pt-100 and the chips were placed inside a cavity in a large block of aluminum.

Fig. 15 shows the sensors' output versus temperature. Due to the spread in R_p and R_n, its sensitivity is about 16% less than that in the typical–typical (TT) corner, which in turns

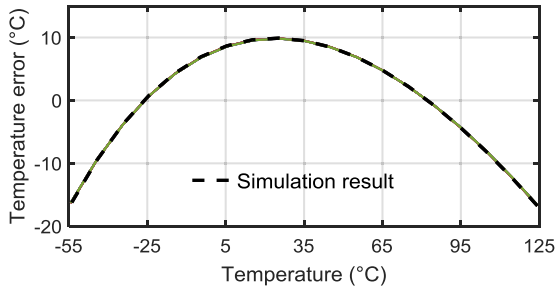

Fig. 16. Measured and simulated temperature error after an individual first-order fit.

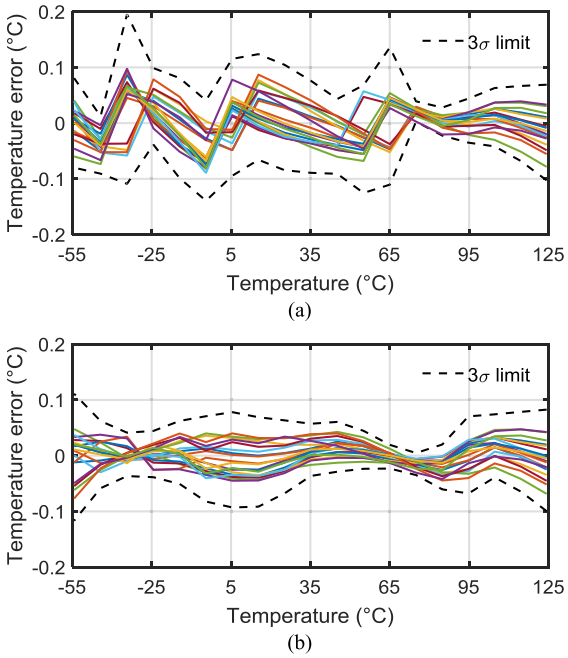

Fig. 17. Temperature error after individual first-order fit and systematic nonlinearity removal (a) without segment averaging and (b) with segment averaging.

results in less resolution: ~200 μK (rms) with $t_{conv} = 5$ ms. Over temperature, the output of the zoom ADC varies from about 0–3.2 over temperature, which is still within its designed full-scale range of −4–4. Without any calibration, the sensor has a spread of about 15 °C.

An individual first-order fit is applied to remove the process spread, i.e., the spread of $R_{DAC}(T_0)/R_p(T_0)$ and $R_{DAC}(T_0)/R_n(T_0)$ in (2). The residual error is then determined by the term $f_{pn}(T - T_0)$ in (2), which turns out to be quite systematic (Fig. 16). Despite the reduction of bridge sensitivity due to the process spread, the residual error agrees well with simulations made in the TT corner (maximum error < 0.3 °C). As in [4], [6], and [12], this error can then be removed by a fixed polynomial.

Without segment averaging, the 3σ inaccuracy is 0.2 °C after the systematic nonlinearity is removed by a fixed fifth-order polynomial [Fig. 17(a)]. As discussed in Section III-C, the jumps around −35 °C, 5 °C, and 55 °C (when the fine code $\mu = \pm 0.5$) are caused by the non-linearity of the first stage. With segment averaging enabled (Threshold = 0.05),

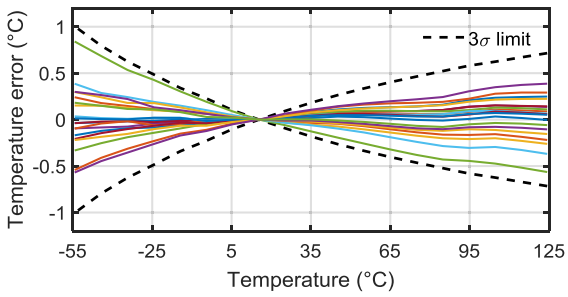

Fig. 18. Temperature error after a correlation-based one-point trim and systematic nonlinearity removal.

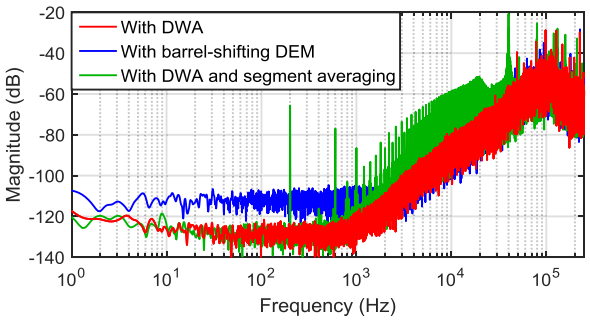

Fig. 19. Power spectral density of the bitstream output.

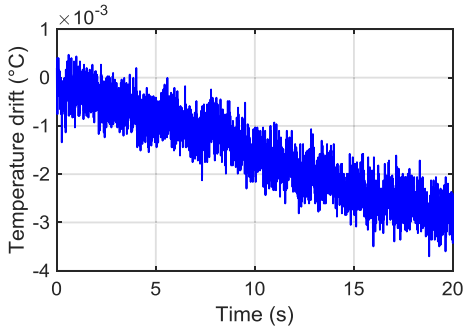

Fig. 20. Temperature drift over time.

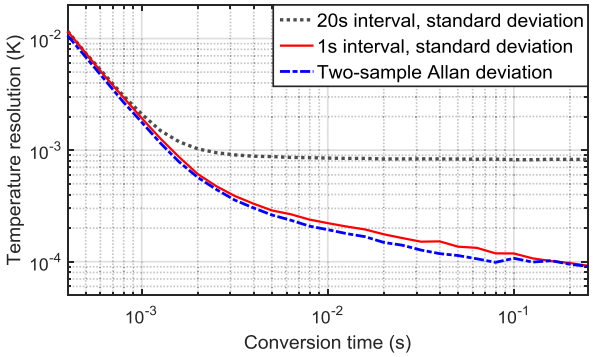

Fig. 21. Temperature resolution versus conversion time using different calculation methods.

the inaccuracy can be reduced to 0.12 °C (3σ) within the military temperature range [Fig. 17(b)]. The 1.6× improvement in accuracy is less than the 8× factor shown in Fig. 12, indicating that the majority of the error is due to the spread of the sensing resistors rather than to the nonlinearity of the ADC.

A simple offset trim results in an inaccuracy of 6.7 °C (3σ). By exploiting the correlation between the zero and first-order coefficients of the individual first-order fit [6], this can be reduced to 1 °C, as shown in Fig. 18. Compared to the 0.2 °C inaccuracy achieved by an *RC*-based sensor [6], the extra inaccuracy of this design is probably due to the fact that the non-silicided n-poly resistors in the WhB spread more than the MIM capacitors of an *RC* filter.

B. Resolution and FoM

With different DEM algorithms, the power spectral densities of the sensor's output bitstream are shown in Fig. 19. Compared to barrel-shifting DEM, DWA is more complex, but it preserves the sensor's noise floor. Applying segment averaging of 2.5-ms/segment results in tones at multiples of 200 Hz but not a raised noise floor. For a fixed conversions time of 5 ms (Nyquist frequency of 100 Hz), the tones will be located at the notches of the sinc^2 decimation filter, and thus have no effect on the sensor's resolution. The $1/f$ noise corner is at about 20 Hz, which is mainly due to the non-silicided poly resistor [6].

The sensor's noise can be converted to temperature via the RT sensitivity obtained in Section IV-B. With a 5-ms decimation filter, the sensor's output is shown in Fig. 20(a) over a 20-s period. A significant temperature drift can be seen (∼|3m °C|), which is mainly due to the temperature fluctuations in the oven.

In order to accurately estimate the sensor's resolution, this drift must be suppressed. One way of doing this is to take the difference between successive samples of the sensor's decimated output, and then compute a two-sample Allan deviation [6]. However, the differencing operation will also suppress the sensor's non-negligible $1/f$ noise (Fig. 19).

To avoid this, the standard deviation can be computed over a shorter interval (1 s), during which the temperature drift (∼140 μK, or ∼40 μK_{rms}) will be negligible compared to the sensor's noise. The 20 s of data were divided into 20 intervals of 1 s, and the average standard deviation obtained from the 20 intervals.

As shown in Fig. 21, in a 20-s interval, the standard deviation is indeed limited by drift. Computing the two-sample Allan deviation [13] suppresses this drift and results in an estimated resolution of 260 μK_{rms} with $T_{conv} = 5$ ms. Computing the standard deviation over a 1-s interval results in a more realistic estimate of 290 μK_{rms}, which corresponds to a 40-fJ · K^2 resolution FoM. Compared to the 200 μK_{rms} predicted in Section IV-A, the reduced resolution is mainly due to the sensor's $1/f$ noise.

C. Comparison to Previous Work

The performance of the sensor is summarized in Table I and compared to other high-resolution temperature sensors. It achieves a state-of-the-art resolution FoM of 40 fJ · K^2,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR ART

	This work	[12]	[5]	[4]	[6]	[14]	[1]	[9]
Sensor type	Resistor WhB	Resistor WhB	Resistor WhB	Resistor WB	Resistor WB	Resistor PPF	Dual-MEMS Resonator	BJT
Technology	180 nm	180 nm	180 nm	180 nm	180 nm	65 nm	180 nm	160 nm
Area (mm^2)	0.25	0.72	0.43	0.09	0.72	0.007	0.54	0.16
Temperature range (°C)	−55 to 125	−40 to 85	−40 to 125	−40 to 85	−40 to 85	−40 to 85	−40 to 85	−70 to 125
Trimming points	2[a]	2[a]	2[b]	3	1	2	--	1
3σ Inaccuracy (°C)	0.12	0.1	0.4[c]	0.12[c]	0.2	0.35	--	0.06
Relative inaccuracy (%)	0.13	0.16	0.48	0.19	0.32	0.56	--	0.06
Power (μW)	94	180	65	31	160	68	13000	7
Conversion time (ms)	5	10	0.1	32	5	1	5	5
Resolution (mK)	0.29	0.16	10	2.8	0.41	2.8	0.02	15
Resolution FoM ($fJ{\cdot}K^2$)[d]	40	49	650	8000	130	530	40	7300

[a] 1st order fit. [b] 1-point trim with 1st order fit. [c] min-max. [d] Energy / Conversion × Resolution^2.

which defines the state-of-the-art in CMOS temperature sensors, and is equal to that of the MEMS-based sensor in [1]. It also has a small active area of 0.25 mm^2, which is 3× smaller than [12] and is close to that of precision BJT-based sensors [9]. Packaged in ceramic, the sensor achieves a temperature sensing range from −55 °C to 125 °C, and an inaccuracy of ±0.12 °C (3σ) after a first-order fit followed by a systematic nonlinearity removal.

V. CONCLUSION

A compact, energy-efficient, resistor-based temperature sensor for the temperature compensation of MEMS/XTAL oscillators has been implemented in a standard 180-nm CMOS technology. It is based on a WhB made from silicided poly-silicon and non-silicided poly-silicon thermistors, whose output current is digitized by a continuous-time zoom ADC. Compared to a 1-bit predecessor, the sensor achieves 3× smaller area as well as higher energy efficiency. The nonlinearity of the zoom ADC is significantly mitigated by a segment averaging technique. These results demonstrate that zoom ADCs are suitable for reading WhB sensors with high energy efficiency and small chip area.

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REFERENCES

[1] M. H. Roshan *et al.*, "A MEMS-assisted temperature sensor with 20-μK resolution, conversion rate of 200 S/s, and FOM of 0.04 pJK2," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 185–197, Jan. 2017.

[2] M. H. Perrott *et al.*, "A temperature-to-digital converter for a MEMS-based programmable oscillator with <±0.5-ppm frequency stability and <1-ps integrated jitter," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 276–291, Jan. 2013.

[3] D. Ruffieux *et al.*, "A 3.2×1.5×0.8mm^3 240nA 1.25-to-5.5V 32kHz-DTCXO RTC module with an overall accuracy of μ1ppm and an all-digital 0.1ppm compensation-resolution scheme at 1Hz," in *IEEE ISSCC Dig. Tech. Papers.*, Jan./Feb. 2016, pp. 208–209.

[4] P. Park, D. Ruffieux, and K. A. A. Makinwa, "A thermistor-based temperature sensor for a real-time clock with ±2 ppm frequency stability," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1571–1580, Jul. 2015.

[5] C.-H. Weng, C.-K. Wu, and T.-H. Lin, "A CMOS thermistor-embedded continuous-time delta-sigma temperature sensor with a resolution FoM of 0.65 $pJ{\cdot}°C^2$," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2491–2500, Nov. 2015.

[6] S. Pan, Y. Luo, S. H. Shalmany, and K. A. A. Makinwa, "A resistor-based temperature sensor with a 0.13 pJ · K2 resolution FoM," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 164–173, Jan. 2018.

[7] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.1°C from 55°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005.

[8] K. Souri and K. A. A. Makinwa, "A 0.12 mm^2 7.4μW micropower temperature sensor with an inaccuracy of ±0.2°C (3σ) from −30°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1693–1700, Jul. 2011.

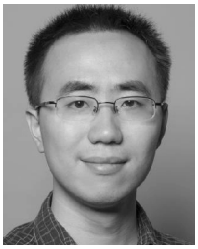
[9] B. Yousefzadeh, S. H. Shalmany, and K. A. A. Makinwa, "A BJT-based temperature-to-digital converter with ±60 mK (3σ) inaccuracy from −55 °C to +125 °C in 0.16-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1044–1052, Apr. 2017.

[10] K. Souri, Y. Chae, F. Thus, and K. Makinwa, "A 0.85 V 600 nW all-CMOS temperature sensor with an inaccuracy of ±0.4°C (3σ) from −40 °C to 125°C," in *IEEE ISSCC Dig. Tech. Papers.*, Feb. 2014, pp. 222–223.

[11] K. Yang *et al.*, "A 0.6nJ -0.22/+0.19°C inaccuracy temperature sensor using exponential subthreshold oscillation dependence," in *IEEE ISSCC Dig. Tech. Papers.*, Feb. 2017, pp. 160–161.

[12] S. Pan, H. Jiang, and K. A. A. Makinwa, "A CMOS temperature sensor with a 49fJK^2 resolution FoM," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C82–C83.

[13] S. Pan and K. A. A. Makinwa, "A 0.25mm^2 resistor-based temperature sensor with an inaccuracy of 0.12°C (3σ) from −55°C to 125°C and a resolution FOM of 32fJ·K^2," in *IEEE ISSCC Dig. Tech. Papers.*, Feb. 2018, pp. 320–322.
[14] W. Choi *et al.*, "A 0.53pJ K^2 7000μm^2 resistor-based temperature sensor with an inaccuracy of ±0.35°C (3σ) in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers.*, Feb. 2018, pp. 322–324.
[15] H. Park and J. Kim, "A 0.8-V resistor-based temperature sensor in 65-nm CMOS with supply sensitivity of 0.28°C/V," *IEEE J. Solid-State Circuits*, vol. 53, no. 3, pp. 906–912, Mar. 2018.
[16] C. P. L. van Vroonhoven, D. d'Aquino, and K. A. A. Makinwa, "A thermal-diffusivity-based temperature sensor with an untrimmed inaccuracy of ±0.2°c (3s) from −55°C to 125°C," in *IEEE ISSCC Dig. Tech. Papers.*, Feb. 2010, pp. 314–315.
[17] U. Sönmez, F. Sebastiano, and K. A. A. Makinwa, "Compact thermal-diffusivity-based temperature sensors in 40-nm CMOS for SoC thermal monitoring," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 834–843, Mar. 2017.
[18] K. A. A. Makinwa, "Smart temperature sensors in standard CMOS," *Procedia Eng.*, vol. 5, pp. 930–939, Sep. 2010.
[19] K. A. A. Makinwa. *Smart Temperature Sensor Survey*. Accessed: Mar. 2018. [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls
[20] S. Pan and K. A. A. Makinwa, "Energy-efficient high-resolution resistor-based temperature sensors," in *Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design*. Cham, Switzerland: Springer Int. Pub., 2018, pp. 183–200.
[21] H. Jiang and K. A. A. Makinwa, "Energy-efficient bridge-to-digital converters," in *Proc. IEEE CICC*, Apr. 2018, pp. 1–7.
[22] R. Wu, J. H. Huijsing, and K. A. A. Makinwa, "A 21b ±40mV range read-out IC for bridge transducers," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2152–2163, Sep. 2012.
[23] H. Jiang, K. A. A. Makinwa, and S. Nihtianov, "An energy-efficient 3.7nV/$\sqrt{\text{Hz}}$ bridge-readout IC with a stable bridge offset compensation scheme," in *IEEE ISSCC Dig. Tech. Papers.*, Feb. 2017, pp. 172–173.
[24] C.-C. Tu, Y.-K. Wang, and T.-H. Lin, "A 0.06mm^2 ±50mV range −82dB THD chopper VCO-based sensor readout circuit in 40 nm CMOS," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C84–C85.
[25] P. Sankar and S. Pavan, "Analysis of integrator nonlinearity in a class of continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 54, no. 12, pp. 661–676, Dec. 2007.
[26] Y. Chae, K. Souri, and K. A. A. Makinwa, "A 6.3 μW 20 bit incremental zoom-ADC with 6 ppm INL and 1 μV offset," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3019–3027, Dec. 2013.
[27] S. Pavan, "Efficient simulation of weak nonlinearities in continuous-time oversampling converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1925–1934, Aug. 2010.
[28] F. Sebastiano, R. H. M. Van Veldhoven, and S. Ersoy, "Modulator with high signal to noise ratio," Eur. Patent EP 2 919 388 A1, Sep. 16, 2015.
[29] S. Pavan, R. Schreier, and G. C. Temes, "Second-order delta-sigma modulation," in *Understanding Delta-Sigma Data Converters*, 2nd ed. Hoboken, NJ, USA: Wiley, 2017, pp. 63–82.



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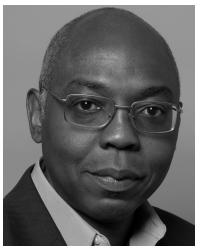

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