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Enhancing Efficiency in Piezoelectric Energy Harvesting

Collaborative-Flip Synchronized Switch Harvesting on Capacitors Rectifier and Multioutput DC-DC Converters Utilizing Shared Capacitors

Wang, Jing; Yang, Yi; Li, Zhen; Du, Sijun; Yue, Xinling; Liu, Xun; Han, Jun; Zeng, Xiaoyang; Chen, Zhiyuan

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Enhancing Efficiency in Piezoelectric Energy Harvesting: Collaborative-Flip Synchronized Switch Harvesting on Capacitors Rectifier and Multioutput DC–DC Converters Utilizing Shared Capacitors

Jing Wang, Yi Yang, Zhen Li, Sijun Du, *Senior Member, IEEE*, Xinling Yue, *Graduate Student Member, IEEE*, Xun Liu, *Member, IEEE*, Jun Han, *Member, IEEE*, Xiaoyang Zeng, *Senior Member, IEEE*, and Zhiyuan Chen, *Member, IEEE*

***Abstract*— This article proposes a novel collaborative-flip synchronized switch harvesting on capacitors (CF-SSHCs) rectifier and multioutput synchronous dc–dc converters with shared capacitors. Compared to the traditional SSHC, our CF-SSHC rectifier can increase the number of flipping phases, potentially enhancing the flipping efficiency and output power under specific conditions where C_{FLY} is close to C_P. The synchronous dc–dc converters reuse the flying capacitors to achieve a high maximum output power improving rate (MOPIR) over a limited input power range and provide multiple outputs. This work achieves an advanced number of flipping phases in capacitor-based rectifier interface technology and explores multiple-input multiple-output configurations, evaluating the system's performance under periodic and shock conditions for the first time. The system's adaptability to various piezoelectric transducer (PT) array configurations is validated, highlighting its potential for Internet of Things (IoT) networks. The design is fabricated in standard 0.18-μm CMOS. Measurement results demonstrate that the voltage flipping efficiency of up to 83% is achieved. Compared with full-bridge rectifier (FBR), the MOPIR can be increased to 5.06× and 4.78× under off-resonance and on-resonance excitation, respectively. It can also achieve a 2.14× power enhancement under shock excitation. Additionally, when the input power $P_{\mathrm{IN\_FBR}}$ is in the range of 1.42–28.4 μW, the MOPIR of the proposed system is always greater than 4.**

***Index Terms*— Maximum power point tracking (MPPT), multi-input, multioutput, piezoelectric, piezoelectric energy harvesting (PEH), rectifiers, shared capacitors, shock excitation, synchronized switch harvesting on capacitors (SSHCs).**

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Jing Wang, Yi Yang, Zhen Li, Jun Han, Xiaoyang Zeng, and Zhiyuan Chen are with the State-Key Laboratory of ASIC and System, Fudan University, Shanghai 201203, China (e-mail: chen_zy@fudan.edu.cn).

Sijun Du and Xinling Yue are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands.

Xun Liu is with the School of Science and Engineering (SSE), Chinese University of Hong Kong, Shenzhen 518172, China.

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I. Introduction

With the flourishing development of the Internet of Things (IoT), supplying power to a large number of miniature wireless sensor nodes has become an urgent challenge. Piezoelectric energy harvesting (PEH), which extracts energy from ambient vibration sources, has gained wide attention [1], [2], [3], [4]. Fig. 1(a) illustrates a conventional PEH system based on full bridge rectifier (FBR) [5]. The system is designed for a single piezoelectric transducer (PT). A FBR is used to convert the ac voltage V_{ab} into the dc voltage V_{rect}. Subsequently, a dc–dc converter regulates V_{rect} based on the input excitation to achieve maximum power point tracking (MPPT). It has advantages such as simplicity, stability, and high integration. However, due to the inherent capacitance C_P, the system can only harvest output power when $|V_{ab}| \geq V_{\mathrm{rect}} + 2V_D$. During the remaining time, the diodes are nonconductive. The shaded region in Fig. 1(a) represents the charge wasted in the periodic charging and discharging of C_P. Consequently, the energy conversion efficiency of the FBR-based PEH system is relatively low. Additionally, single PT has limited energy harvesting capacity, risks single-point failure, and lacks flexibility. In contrast, using multiple PT units enhances energy conversion efficiency and allows for customized layouts to suit specific applications. When multiple elements operate in parallel, the system can maintain energy harvesting through the remaining elements even if some degrade or are damaged, ensuring overall stability and reliability.

In recent years, various flipping techniques based on inductor and switched capacitor have emerged [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16]. For the synchronous switch harvesting on the inductor (SSHI), voltage flipping on C_P is achieved through an LC loop. To achieve higher flipping efficiency, inductors with high Q values are necessary, which

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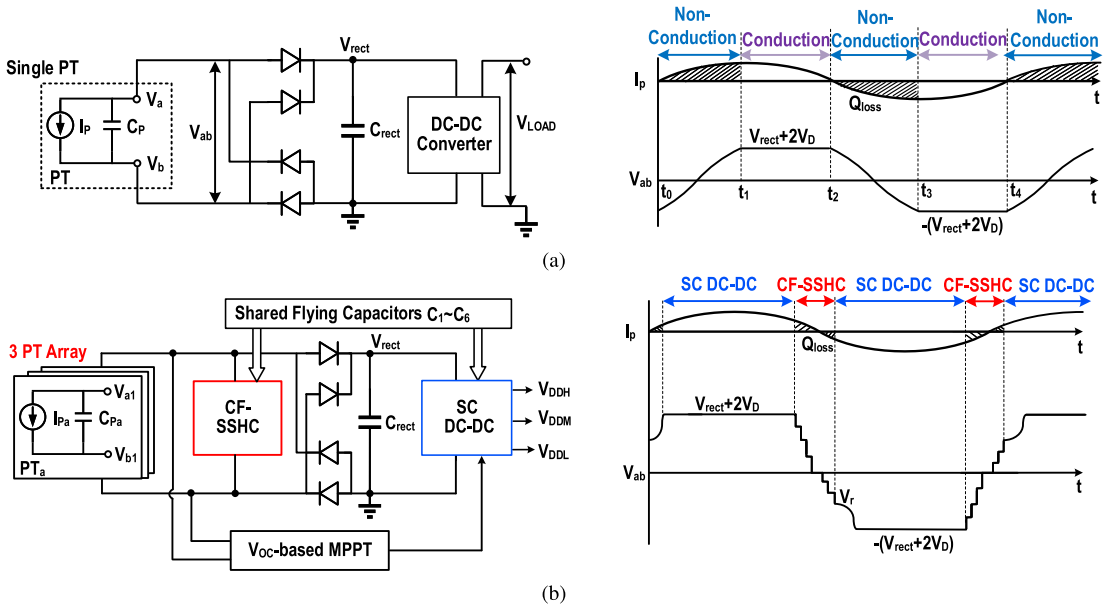

Fig. 1. (a) Conventional PEH system based on FBR. (b) Proposed PEH system based on CF-SSHC.

inevitably occupy large volumes. In contrast, the synchronized switch harvesting on capacitors (SSHC) technique relies on charge sharing to flip the charge on C_P. Multiple-phase and large flipping capacitors are utilized to enhance the output power. Complete PEH systems based on these flipping techniques have been widely implemented [17], [18], [19], [20], [21], [22], [23], [24]. Chen et al. [23] implemented a complete PEH system that includes a split-phase flipping-capacitor rectifier (SPFCR), MPPT, and dc–dc converters. However, this system is designed for a single PT, which not only reduces system reliability but also limits the number of flipping phases. Despite employing the split-phase method, the number of flipping phases is still limited to 21. Du and Seshia [22] presents a split-electrode synchronized switch harvesting on capacitors (SE-SSHCs) rectifier. By splitting the PT electrodes into four regions and temporarily connecting them in series during voltage flipping, the effective intrinsic capacitance of the PT is reduced, thereby significantly increasing the output power. However, due to the series-connecting PT units, this method not only requires high-voltage (HV) CMOS transistors but also results in high switching losses and leakage current, thereby reducing the energy harvesting efficiency. HV transistors also reduce system integration density, increase circuit complexity, and cause greater power consumption.

This article introduces a PEH system based on collaborative-flip synchronized switch harvesting on capacitors (CF-SSHCs) rectifier and multioutput dc–dc converters utilizing shared capacitors, as depicted in Fig. 1(b). By connecting three PT units in parallel, the proposed CF-SSHC rectifier can increase the number of flipping phases, thereby significantly improving the flipping efficiency and output power. For instance, in this article, 37 flipping phases were achieved using three PT units and six flying capacitors, tripling the number of flipping phases compared to traditional SSHC. This represents the highest number of flip phases currently achieved in capacitor-based flipping technologies. Due to the excellent scalability of CF-SSHC technology, this article also analyzes the performance of CF-SSHC with different numbers of stages and PT units. Furthermore, the proposed CF-SSHC utilizes flying capacitors only during brief flipping periods, allocating the remaining time for constructing the multioutput SC dc–dc converters with the flying capacitors, enhancing overall capacitor efficiency and system compactness.

II. Proposed System

A. Traditional SSHC Interface Circuit

Fig. 2 depicts a traditional N-stage SSHC rectifier circuit and the associated flipping phases [10]. The SSHC interface circuit, consisting of N flying capacitors and $2N+1$ switches, has garnered widespread attention due to its simple structure and scalability. The operational principles of the N-stage SSHC are delineated as follows: At the zero-crossing of I_P, the initial voltage across C_P is V_{rect}. The flipping phases can be classified into three periods: 1) charging period: flying capacitors $C_1 - C_N$ sequentially share with the charge on C_P; 2) clearing period: shorting C_P to clear residual charge; and 3) recharging period: connecting the flying capacitors $C_N - C_1$ in reverse polarity to recharge C_P, thereby establishing the rebuild voltage $-V_r$. It effectively reduces the charge wastage caused by the periodic charging and discharging of C_P. To quantify the enhancement in the performance of different types of synchronous switch harvesting (SSH) interface circuits, we typically employ the flipping efficiency η and its maximum output power improving rate (MOPIR). The expressions for flipping efficiency η and MOPIR are provided by [11]

$$\eta = \frac{V_{\text{rect}} + V_r}{2V_{\text{rect}}} \tag{1}$$

$$\text{MOPIR} = \frac{P_{\text{rect,SSH,MAX}}}{P_{\text{rect,FBR,MAX}}}. \tag{2}$$

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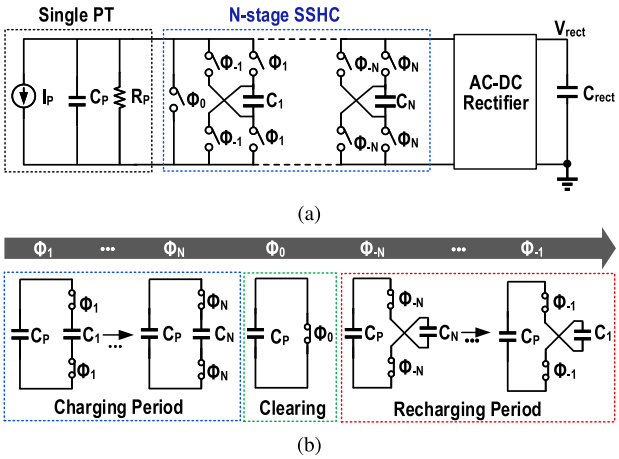

Fig. 2. (a) Traditional N-stage SSHC circuit. (b) Associated flipping phases [10].

For the traditional SSHC interface circuits, the MOPIR is typically determined by the number of stages and the ratio of flying capacitors to an inherent capacitor, denoted as C_{FLY}/C_P [12]. For instance, in the case of the single-stage SSHC, if the flipping capacitor C_{FLY} equals C_P, the MOPIR is 3. However, if $C_{\mathrm{FLY}} \gg C_P$, its MOPIR can be elevated to 4. Furthermore, increasing the number of SSHC stages can also enhance the performance of the SSHC interface circuits. If C_{FLY} equals C_P, the three-stage SSHC compared to the single-stage SSHC can increase the MOPIR from 3 to 5. If $C_{\mathrm{FLY}} \gg C_P$, it can increase the MOPIR from 4 to 8. Therefore, for traditional SSHC interface circuits, to achieve higher output power, one must either increase the number of flipping stages or the capacitance value of the flying capacitors. However, both remedies would increase the overall system volume, deviating from the trend toward miniaturization and integration of PEH. Therefore, we propose a novel CF-SSHC technique to address this challenge.

B. Proposed CF-SSHC

As illustrated in Fig. 3(a), three units are clamped in parallel, ensuring the vibration amplitude and phase between them are consistent. The electrical model of three PT units in parallel can be equivalently represented by a parallel combination of a sinusoidal current source I_P, inherent capacitor C_P, and resistance R_P. For each PT unit, the equivalent current source and capacitance become one-third of their original values, while the open-circuit voltage remains unchanged. It is worth mentioning that the area before and after the PTs are paralleled does not change. Fig. 3(b) depicts the circuit diagram of the proposed six-stage CF-SSHC rectifier. The essential components of the circuit include three PT units and six flying capacitors. We denote the three PT units as PT_a, PT_b, and PT_c. Each PT unit is equipped with individual switches (S_{ab1}, S_{ab2}, S_{ab3}), controlling its connection with the subsequent six flipping capacitors.

Fig. 4 depicts the operating phase of the proposed 37-phase six-stage CF-SSHC rectifier. Here, we denote the periods where I_P transitions from positive to negative and from negative to positive as PTC and NTC, respectively. For clarity, we divide the operating states of the CF-SSHC into (a)–(g).

1) *Forward Harvesting State:* As shown in Fig. 4(a), during the nonflipping moment, the three PT units are connected in parallel and collectively harvest energy from external excitation sources.
2) *Charging State (18 Phases):* As shown in Fig. 4(b) and (c), at the zero crossing of I_P, the flying capacitor C_1 sequentially flips C_{Pa}, C_{Pb}, and C_{Pc} of the PT units, gradually increasing the voltage on C_1. Then, C_2–C_6 are used sequentially to flip C_{Pa}, C_{Pb}, and C_{Pc}. After 18 flipping phases, the remaining charge on the inherent capacitors of the three PT units gradually decreases.
3) *Clearing State:* As shown in Fig. 4(d), the three PT units are directly shorted to clear residual charges.
4) *Recharging State (18 Phases):* Fig. 4(e) and (f) demonstrates the recharging states, which are opposite to the charging state. The flying capacitors C_6 to C_1 are sequentially used in reverse polarity to recharge C_{Pc}, C_{Pb}, and C_{Pa}, establishing the rebuild voltage.
5) *Backward Harvesting State:* After 37 flipping phases, the voltage across the three PT units changes from positive to negative, and then the three PT units are reconnected in parallel to harvest energy, as illustrated in Fig. 4(g).

Symmetrically, the operation phases for NTC and PTC are completely reversed, i.e., from Fig. 4(a)–(g).

Fig. 5 illustrates the corresponding waveforms of the proposed CF-SSHC. When the circuit is stable, the voltages across the six flying capacitors are $0.62V_{\mathrm{rect}}$, $0.5V_{\mathrm{rect}}$, $0.37V_{\mathrm{rect}}$, $0.25V_{\mathrm{rect}}$, $0.13V_{\mathrm{rect}}$, and $0.05V_{\mathrm{rect}}$, respectively. It is worth noting that for a specific rectification topology, the ratio between the voltage across the flying capacitor ($V_{C1} - V_{C6}$) and the rectified voltage (V_{rect}) remains constant, regardless of variations in the input excitation [25]. Due to the very brief duration for which the flying capacitors are used for flipping, we will reuse them to construct the reconfigurable dc–dc converters. Considering the accumulated charge on the flying capacitors at the flipping moments, special attention must be paid when constructing the dc–dc converters to prevent mutual interference between the flipping operation and the dc–dc operation. The detailed structure of dc–dc converters will be presented in Section III.

C. Performance Analysis of the Proposed CF-SSHC

The proposed CF-SSHC has the advantage of scalability, allowing it to be extended to any number of PT units and flying capacitors. We refer to the CF-SSHC with N flying capacitors and M PT units as N-stage CF-SSHC$_M$. In particular, when $M = 1$, the proposed CF-SSHC is the traditional SSHC. Fig. 6(a) illustrates the relationship between the MOPIR of the proposed CF-SSHC and traditional SSHC with the number of stages and C_{FLY}/C_P. Under the same number of stages and C_{FLY}/C_P, the proposed CF-SSHC significantly enhances the MOPIR compared to SSHC. For instance, when $C_{\mathrm{FLY}}/C_P = 1/3$, the proposed six-stage CF-SSHC increases the MOPIR from 5 to 7.3 compared to the traditional six-stage SSHC. Similarly, when $C_{\mathrm{FLY}}/C_P = 1$, the six-stage

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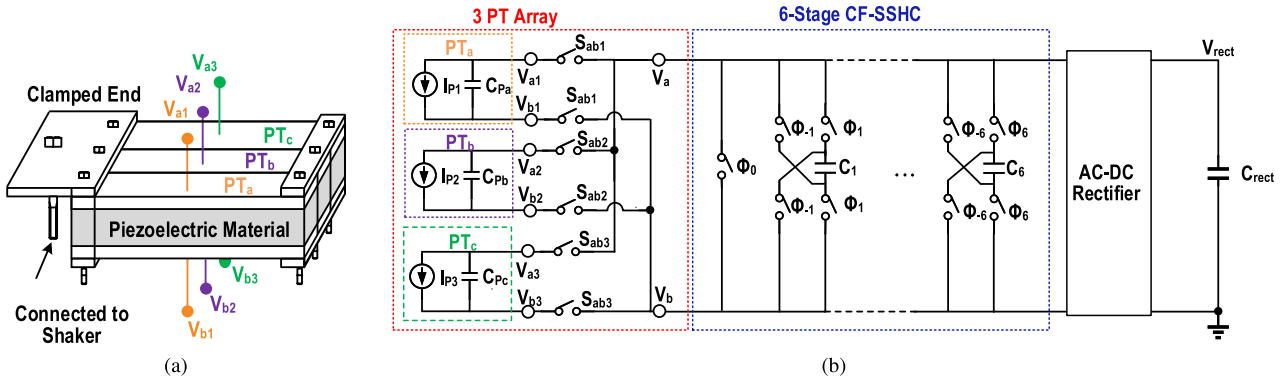

Fig. 3. (a) Schematic of three PT units in parallel. (b) Proposed six-stage CF-SSHC interface circuit.

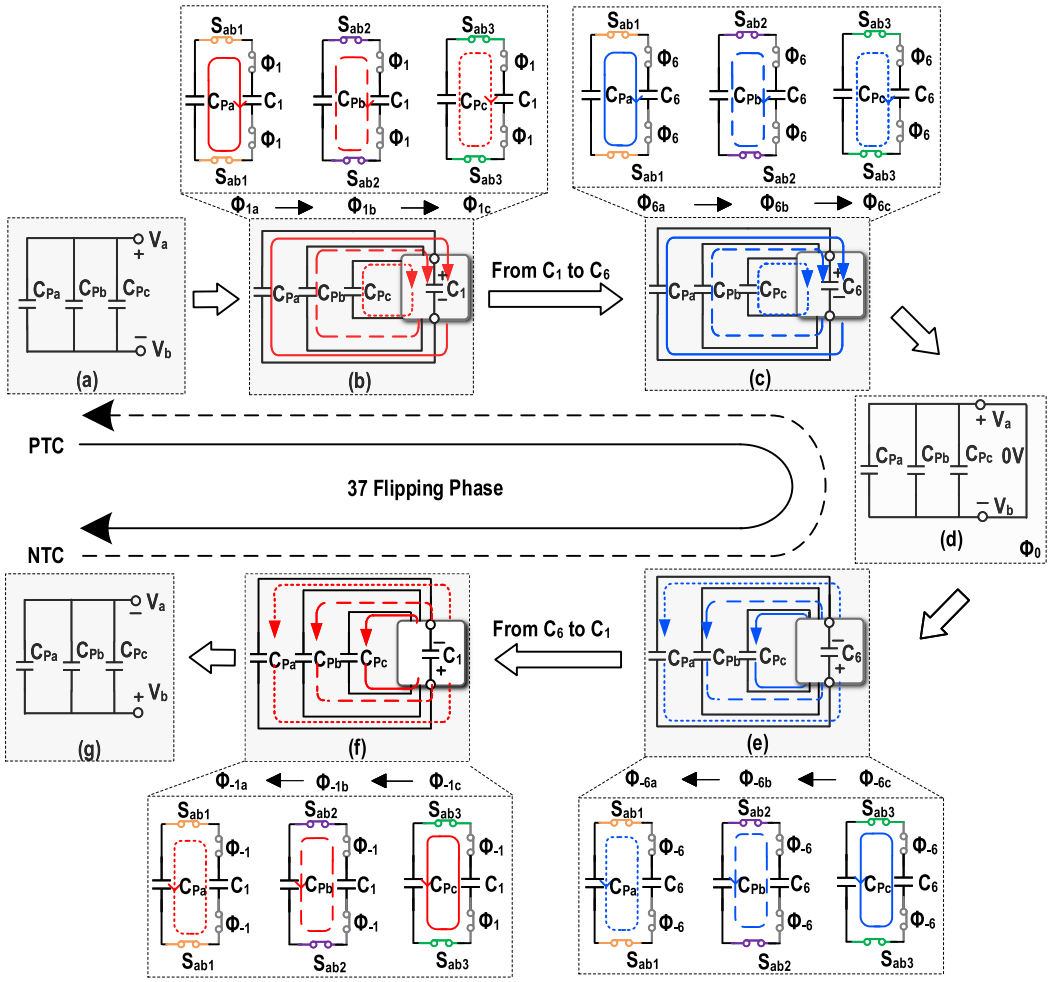

Fig. 4. Operating phase of the proposed 37-phase six-stage CF-SSHC. (a) Forward Harvesting State. (b) Charging current flows from C_{pa}, C_{pb} and C_{pc} to C_1. (c) Charging current flows from C_{pa}, C_{pb} and C_{pc} to C_6. (d) Clearing State. (e) Recharging current flows from C_6 to C_{pa}, C_{pb} and C_{pc}. (f) Recharging current flows from C_1 to C_{pa}, C_{pb} and C_{pc}. (g) Backward Harvesting State.

CF-SSHC boosts the MOPIR from 8 to 10.7. Additionally, we simultaneously compare the three-stage CF-SSHC rectifier with the three-stage SSHC rectifier, further demonstrating the superiority of the proposed CF-SSHC. Only when $C_{\mathrm{FLY}} \gg C_P$, CF-SSHC and SSHC reach the same maximum MOPIR limit. However, typical PTs have C_P in the nF range, and achieving this limit requires very large flying capacitors, which does not align with the current trend of miniaturizing PEH systems. Compared to the traditional SSHC interface, the proposed CF-SSHC interface offers the following advantages: First, the proposed CF-SSHC reduces the inherent capacitance during flipping moments. At flipping moments, as each PT unit sequentially flips the flying capacitors, the inherent capacitance C_P of each PT unit is only one-third of its original value. This effectively increases the output power and MOPIR. Additionally, while the traditional six-stage SSHC provides 13 flipping phases, the proposed CF-SSHC rectifier can extend the flipping phases to 37, thus improving the flipping efficiency. Compared

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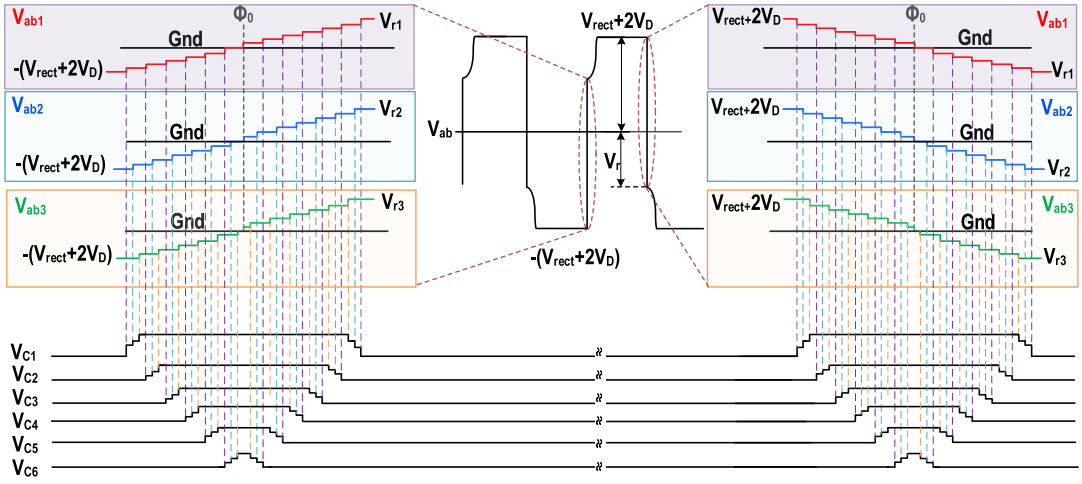
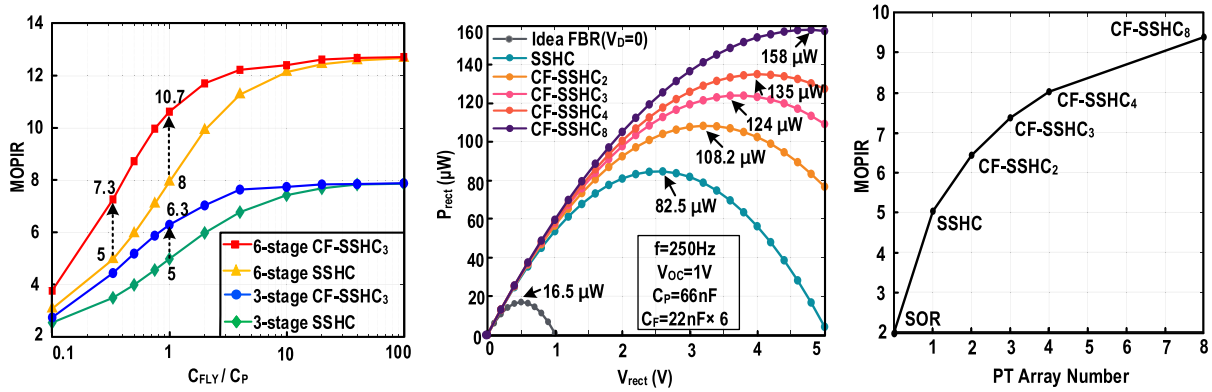


Fig. 5. Waveforms of the proposed CF-SSHC.



(a) (b) (c)

Fig. 6. (a) Relationship between the MOPIR of the proposed CF-SSHC and traditional SSHC with the number of stages and C_{FLY}/C_P. (b) Simulation results of P_{rect} versus V_{rect} for FBR and the proposed six-stage CF-SSHC with different numbers of PT units. (c) Relationship between the MOPIR with the number of PT units.

to the SE-SSHC proposed in [22], the proposed CF-SSHC connects each PT unit and flipping capacitor in parallel, thereby avoiding high voltage stress and leakage current on the switches.

Fig. 6(b) shows the simulation results of P_{rect} versus V_{rect} for the FBR, SSHC, and six-stage CF-SSHC under different numbers of PT units. For a fair comparison, although the number of PT units varies, their total capacitance C_P and open-circuit voltage V_{OC} remain constant. Simulation results show that as the number of PT units increases, the maximum output power of CF-SSHC also increases. Under the same flying capacitance, the proposed CF-SSHC$_3$ increases the maximum output power by nearly 50% compared to SSHC. To better illustrate the relationship between the number of PT units and MOPIR in CF-SSHC, we plotted Fig. 6(c) based on Fig. 6(b). It can be seen that although the maximum output power of CF-SSHC increases with the number of PT units, the marginal returns of this increase diminish. Considering the tradeoff between performance and power consumption, the six-stage CF-SSHC with three PT units prototype circuit is implemented in this article.

III. Implementation

Fig. 7 illustrates the block diagram of the proposed system, which comprises two stages: the first stage is the proposed 37-phase CF-SSHC rectifier, and the second stage consists of reconfigurable multiout SC dc–dc converters. To minimize power consumption, the control circuit operates across both high- and low-voltage domains. Specifically, the pulse generation, pulse sequence, pulse combine modules, and flipping time module are powered by the low-voltage domain V_{DDL}, while the CF-SSHC power switch, dc–dc switch, lever shifters, MPPT, and active rectifier are powered by the HV domain V_{DDH}. Next, we will provide a detailed description of the key modules.

A. Active Rectifier

Fig. 8 shows the circuit diagram of the active rectifier. During MPPT, the four multiplexers temporarily disconnect the PT from the active rectifier to perform open-circuit voltage sampling. The active rectifier is composed of two cross-coupled PMOS transistors and two amplifier-based active diodes. The

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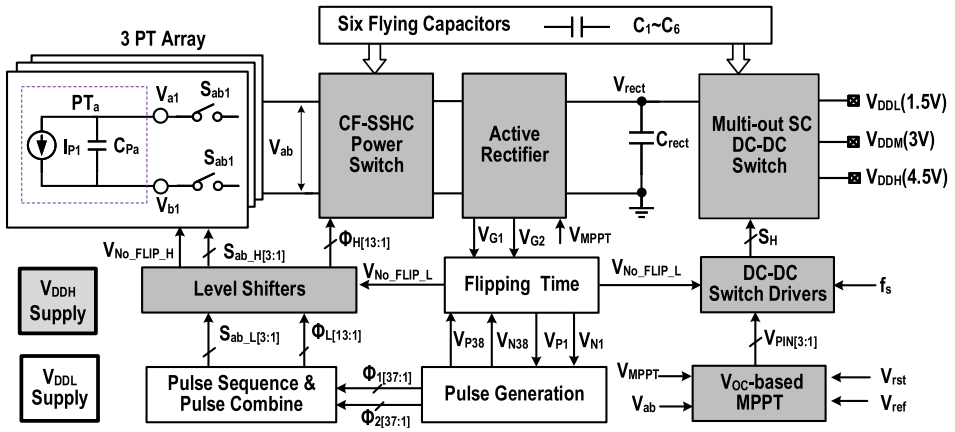

Fig. 7. Diagram of system block.

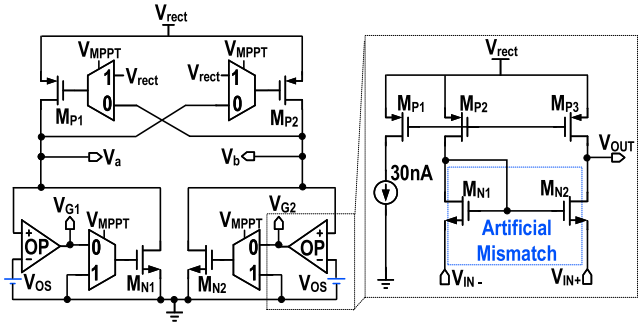

Fig. 8. Active rectifier.

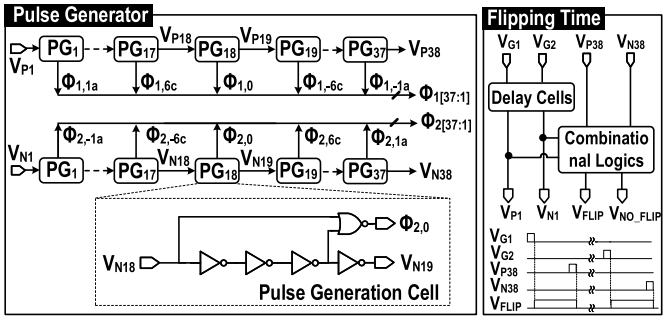

Fig. 9. Pulse generation and flipping time module.

falling edges of the amplifier outputs, V_{G1} and V_{G2}, indicate the positive and negative zero-crossing of I_P, respectively. In the ground-input-compatible amplifier, the transistors operate in the subthreshold region. The 30 nA bias current ensures reliable operation under various input conditions [26], [27]. Additionally, we introduce an artificial mismatch by setting the sizes of the input transistors of the operational amplifier to different values, thereby introducing a consistent and predictable positive offset voltage. This improves the accuracy and reliability of the rectifier. Furthermore, this method avoids the complexity associated with implementing a closed-loop control system, thereby simplifying the overall design.

B. Pulse Generation and Flipping Time Module

To ensure design margins and prevent phase overlap, the output signals V_{G1} and V_{G2} from the active rectifier undergo delay operations in the flipping timing module, resulting in the delayed signals V_{P1} and V_{P2}, respectively. Subsequently, V_{P1} and V_{P2} are fed into the pulse generation module to produce continuous pulses that drive the power switch array of the proposed CF-SSHC rectifier. Fig. 9 illustrates the pulse generation and flipping time module. The pulse generator cell consists of a chain of inverters, where the delay of this inverter chain determines the pulsewidth. To ensure complete charge sharing and prevent overlap between adjacent pulses, the width-to-length ratio of the transistors in this inverter chain should be set very small, i.e., $W \ll L$. V_{P1} and V_{P2} pass through 37 pulse generation cells, generating two sets of continuous pulse signals $\Phi_{1[37:1]}$ and $\Phi_{2[37:1]}$. Additionally, pulse signals V_{P38} and V_{N38} represent the timing of the last pulse generation. Together with V_{G1} and V_{G2}, they are fed into the flipping time module, where simple combinatorial logic generates the signal V_{FLIP} representing the flipping time and the signal $V_{\mathrm{NO\_FLIP}}$ representing the nonflipping time.

C. Pulse Sequence and Combine

Fig. 10 shows the diagram of the pulse sequence and pulse combine. Due to the pulse sequence being completely opposite during PTC and NTC, the pulse sequence module needs to merge the head and tail of $\Phi_{1[37:1]}$ and $\Phi_{2[37:1]}$ to obtain the signal $\Phi_{[37:1]}$. Additionally, considering the reuse of switches in different phases, the pulse combination module will further combine the generated pulse signals. There are mainly two methods for pulse combination. The first method is to directly use three-input OR gates to generate the control signals S_{ab1}, S_{ab2}, and S_{ab3} for the three PT units. The second method involves combining adjacent groups of three pulse signals (e.g.,Φ_{1a}, Φ_{2a}, Φ_{3a}) to generate the switch control signals for the six flying capacitors, from Φ_1 to Φ_6 and Φ_{-1} to Φ_{-6}. Specifically, we use JK flip-flops to prevent glitches that may arise from directly combining three signals. After passing through the pulse sequence and combine modules, the power switch signals are reduced from 37 bits to 16 bits. To minimize overall power consumption, the pulse generation, sequencing, and combination modules operate in the low-voltage domain.

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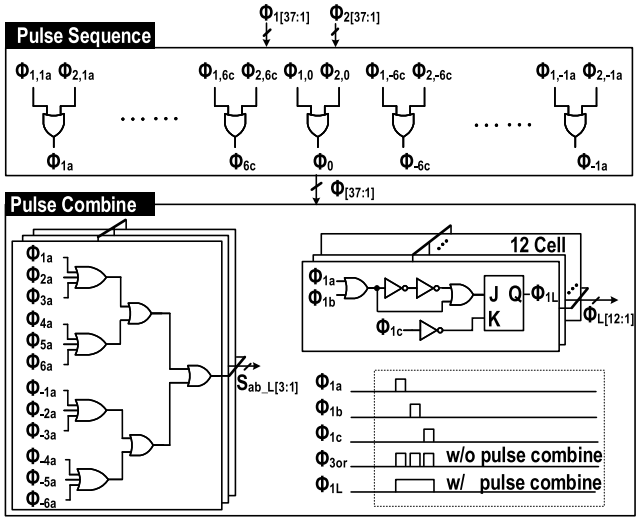

Fig. 10. Pulse sequence and pulse combine.

However, the power switch arrays must operate in the HV domain, requiring low-power level shifters to convert the pulse signals. Due to the floating voltages at both ends of the power switches, this article employs switches composed of transfer gates with dynamic body bias [11].

D. Reconfigurable Multioutput DC–DC Converters

Traditional dc–dc converters typically use a two-phase clock, with the number of flying capacitors limiting the number of conversion ratios. To minimize external capacitance, we will adopt the three-phase clock, effectively utilizing flying capacitors to enhance the compactness of the system [28], [29]. Fig. 11 illustrates the proposed multioutput SC dc–dc converters using the flipping capacitors. Based on the input power, the proposed SC dc–dc converter selects the appropriate structure according to the preset conversion ratios. On one hand, it ensures that the conversion ratios among the three output terminals remain constant, i.e., $V_{\mathrm{DDH}} = 3V_{\mathrm{DDL}}$ and $V_{\mathrm{DDM}} = 2V_{\mathrm{DDL}}$. On the other hand, it directly connects V_{rect} to one of the three output terminals to achieve MPPT. Based on the residual voltage levels of the flying capacitors after flipping, we connect C_1 and C_3 in series, as well as C_5 and C_6 to construct the SC dc–dc converters. This configuration minimizes the charge redistribution losses in the SC dc–dc converter while not affecting the flipping of the CF-SSHC stage. At low input power, the rectifier voltage V_{rect} will be directly connected to the low output voltage V_{DDL}. In the Φ_1 period, C_1 and C_3 are connected in series and charged to V_{rect}. In the Φ_2 period, C_1 and C_3 are stacked on the top of V_{rect}, pumping V_{DDM} to twice V_{DDL}. In the Φ_3 period, C_1 and C_3 are stacked on the top of V_{DDM}, pumping V_{DDH} voltage to three times that of V_{DDL}. It is worth noting that the voltage across the series connection of C_1 and C_3 is approximately V_{rect}, resulting in near-zero charge redistribution losses. At medium and high input power, the operations are similar to the process described above, and detailed elaborations are omitted here.

E. MPPT and DC–DC Switch Drivers

Fig. 12(a) and (b) illustrates the MPPT module and the dc–dc switch drivers, respectively. The MPPT is based on the fractional open-circuit voltage (FOCV) method [23]. During MPPT, V_{MPPT} is high and the PT will disconnect from the CF-SSHC rectifier. The MPPT circuit will sample the peak–peak voltage of the PT, denoted as V_{peak}. Subsequently, two identical capacitors divide V_{peak}. When V_{peak} and $1/2V_{\mathrm{peak}}$ are compared with V_{ref}, there are three possible scenarios. When the input power is low, i.e., $V_{\mathrm{peak}} < V_{\mathrm{ref}}$, both comparators output 0, causing the signal $V_{PIN<3:1>}$, which indicates the input power level, to output 001. The operating principle is similar for medium and high input power levels. The reference voltage V_{ref} affects the system's assessment of input power levels, thereby influencing the switching points of the subsequent SC dc–dc converters. $V_{PIN<3:1>}$, along with $V_{\mathrm{NO\_FLIP}}$ and the three-phase clock signal, are fed into the combinational logic circuit and control the reconfigurable dc–dc switch through the level shifters.

IV. Measurement Results

The chip prototype was designed and fabricated using 0.18 μm CMOS technology. The microscopic view of the chip is depicted in Fig. 13(a), with an active area of 0.42 mm^2. By clamping three independent PPA-1021 units together using thick insulating plates, they effectively function as three parallel PT units. When subjected to the same input excitation, their phase and amplitude are identical. Fig. 13(b) illustrates the measurement setup. The functional generator outputs sine wave and pulse wave, which are amplified by the power amplifier and drive the shaker for the periodic sine and shock vibration. Additionally, the oscilloscope monitors the output waveform, and the power supply provides the external reference voltage and the power supply. The intrinsic capacitance C_P of a single PT is 22 nF, resulting in a total intrinsic capacitance $C_{P,\mathrm{total}}$ of 66 nF. Each flying capacitor has a capacitance of 22 nF, giving a total of 132 nF for six flying capacitors. The rectifier capacitor C_{rect} and the output capacitors $C_{\mathrm{DDL}}, C_{\mathrm{DDM}}, C_{\mathrm{DDH}}$ are all 100 nF. Fig. 14 illustrates the start-up of the proposed system. Initially, the system operates in the FBR state. When V_{rect} reaches 0.8 V, the CF-SSHC rectifier begins operating, gradually increasing the voltage across the PT to 6 V. This indicates that the proposed CF-SSHC significantly enhances the voltage across the PT, thereby efficiently improving the output power. When the circuit stabilizes, the system provides three output levels, namely V_{DDL}(1.5 V), V_{DDM}(3 V), and V_{DDH}(4.5 V). Additionally, when the input power changes, each output voltage is set to 1.5, 3, and 4.5 V, respectively, by manually tuning the load current.

Fig. 15 depicts the measured waveform of the voltage at both ends of the three PT units under the sinusoidal excitation. At the nonflipping moment, the three PTs harvest energy in parallel, so the voltages at both ends of the three PTs are the same. When I_P crosses zero, the flying capacitors C_1–C_6 successively flip the voltages across the three PTs, for a total of 37 flip phases. The pulsewidth for each phase is

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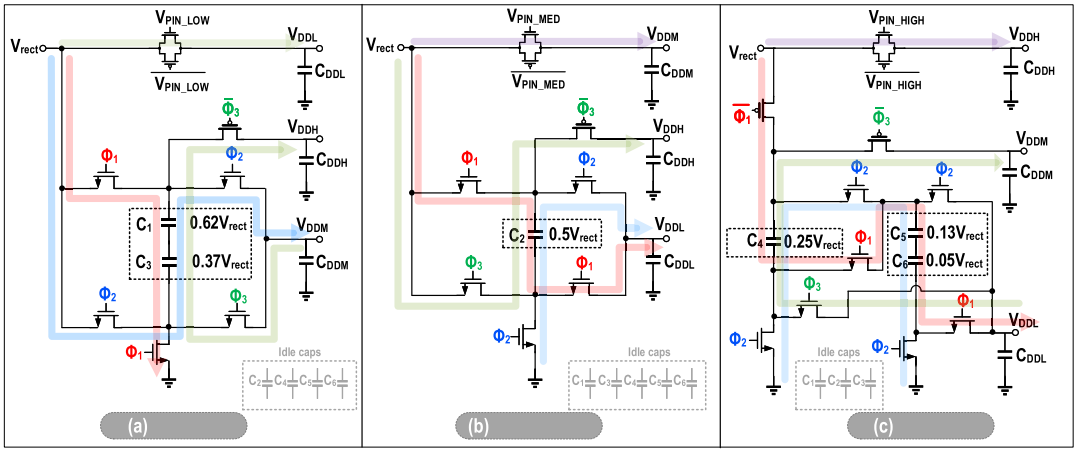
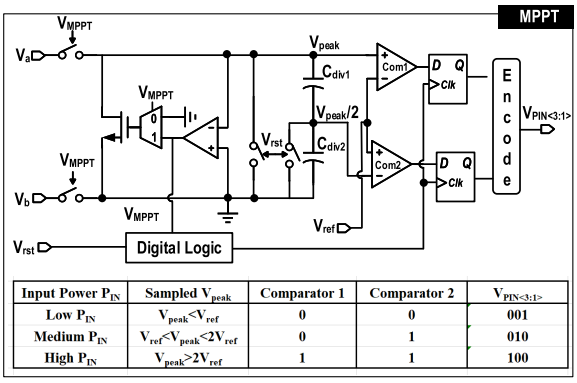
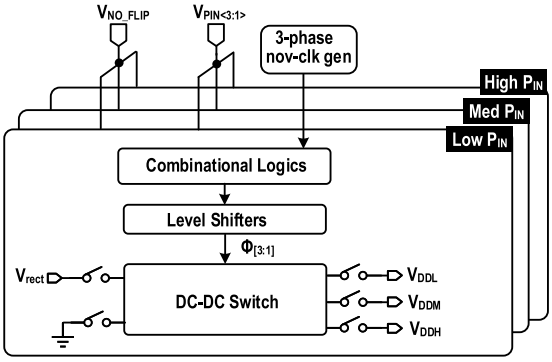


Fig. 11. Proposed multioutput SC dc–dc converters using the flipping capacitors. (a) Low P_{IN}. (b) Medium P_{IN}. (c) High P_{IN}.



(a)



(b)

Fig. 12. (a) MPPT and (b) dc–dc switch drivers.

approximately 2.7 μs, resulting in a total flip time of about 100 μs, representing a mere 0.6% of the vibration cycle. According to the flipping sequence, the rebuilt voltages across the three PTs are approximately $V_{ab3} > V_{ab2} > V_{ab1}$. The flipping efficiency is about 0.83. Fig. 16 shows the waveforms of PT under the shock excitation. In the case of shock vibration, our excitation source is a square wave with a period of 1 s, and its falling edge is only 10 ns, to simulate the case of gradual disappearance of excitation. Under the shock excitation, it first operated in the CF-SSHC mode, and its conduction time gradually decreased until the minimum open circuit voltage could not maintain the flipping operation.

Fig. 17 illustrates the MPPT process. Initially, due to low external vibration, the reconfigurable dc–dc converter operates in the low P_{IN} mode, where V_{rect} is 1.5 V. Then, we increase the input excitation and the system enters the MPPT state. Temporarily disconnecting the PT array from the CF-SSHC rectifier, the peak-to-peak voltage of the PT is sampled, which is approximately 2.5 V, indicating that the open-circuit voltage of the PT is around 1.25 V. The corresponding optimal V_{rect} is approximately 3 V. Consequently, the dc–dc converter enters the medium P_{IN} mode, and V_{rect} is connected to V_{DDM}, achieving MPPT.

Fig. 18 shows the measured output power of the CF-SSHC rectifier under various excitations. To visually demonstrate the improvements of the proposed CF-SSHC compared to FBR, the corresponding output power of the FBR under the same excitation conditions is also plotted in the figure. Fig. 18(a) presents the output power under the off-resonance frequency of 60 Hz, with $V_{OC} = 1$ V. When V_{rect} is below 0.8 V, the system operates in the FBR state, resulting in lower output power. The FBR provides 3.4 μW at an optimal V_{rect} of 0.6 V, which closely matches the theoretical calculation. The proposed CF-SSHC provides 17.2 μW at an optimal V_{rect} of 2.2 V, representing an improvement of about 5.06 times compared with the FBR. Fig. 18(b) illustrates the output power of the proposed CF-SSHC rectifier as V_{rect} varies under shock excitation. The shaker was driven with a shock impulse every 1 s. The PT generated a V_{OC} of 1.3 V. The on-chip FBR standalone was able to harvest 3.2 μW at an optimal V_{rect} of 0.6 V. The proposed CF-SSHC interface harvested 6.85 μW at an optimal V_{rect} of 1.3 V, representing an improvement of about 2.14 times compared with the FBR. Fig. 18(c) shows the harvested power under the mechanical resonance frequency of 87 Hz, with $V_{OC} = 1.3$ V. The FBR provides 9.4 μW at an optimal V_{rect} of 0.6 V, which closely matches the theoretical calculation. The proposed CF-SSHC provides 45 μW at an optimal V_{rect} of 2.8 V, representing an improvement of about 4.78 times compared with the FBR. Fig. 18(d) shows the extracted power for different open-circuit voltages together with MOPIR. It can be seen that as the excitation level increases, the harvested output power also increases. The MOPIR reaches its peak of 5.06 at $V_{OC} = 1$ V. The MOPIR

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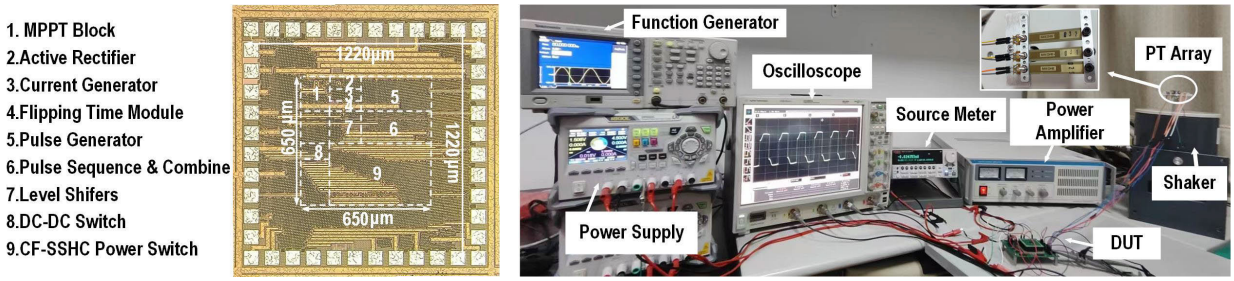

(a) (b)

Fig. 13. (a) Chip micrograph. (b) Picture of measurement setup.

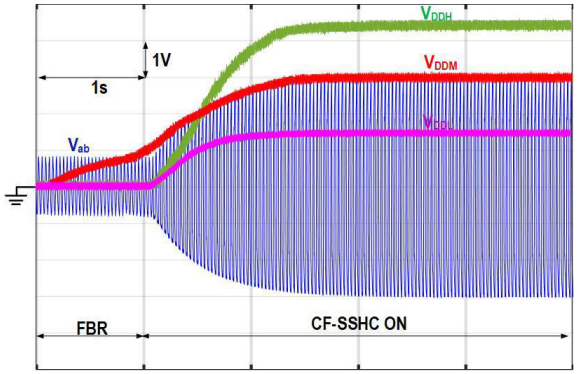

Fig. 14. Start-up of the proposed CF-SSHC.

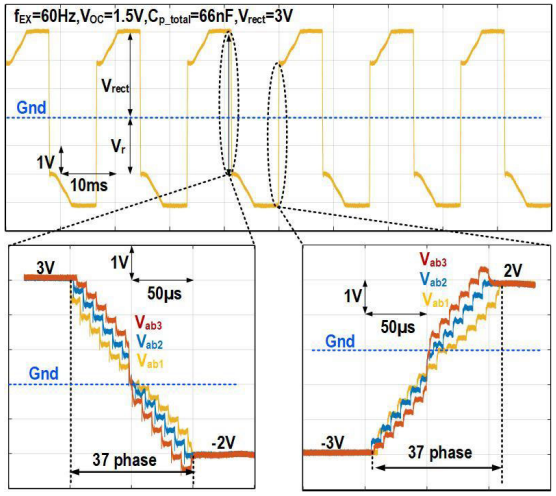

Fig. 15. Measured waveforms under the sine excitation.

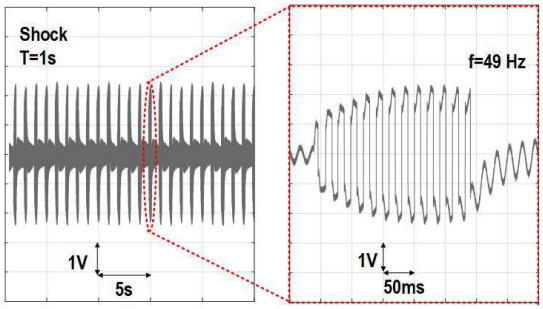

Fig. 16. Measured waveforms under the shock excitation.

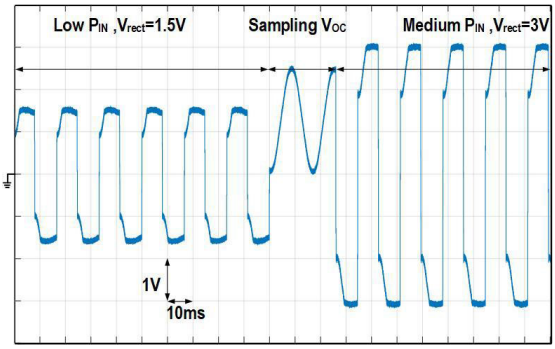

Fig. 17. Measured waveforms during the MPPT operation.

remains above 4 between an open-circuit voltage range of 0.8–2.8 V, demonstrating the effectiveness of the proposed CF-SSHC. Under higher vibration excitation, the MOPIR of the system slightly decreases due to a significant increase in the power extraction from the FBR and limitations imposed by the process voltage.

Subsequently, the relationship between P_{rect} and V_{rect} was measured at various open-circuit voltage (V_{OC}) levels. The results demonstrate that the ratio of the maximum power point voltage ($V_{\text{MPP,CF-SSHC}}$) to V_{OC} approximates a constant value, which fluctuates between 2.2 and 2.3. The measured P_{OUT} versus V_{OC} under different outputs is depicted in Fig. 19.

As illustrated in Fig. 19(a), the V_{DDL} terminal outputs the highest power when V_{OC} is below 0.9 V. For V_{OC} values ranging from 0.9 to 1.8 V, the highest output power shifts to the V_{DDM} terminal. Above 1.8 V, the V_{DDH} terminal delivers the maximum output power. Therefore, the crossover points of these three output terminals are the points at which the system switches the dc–dc structure. Based on the above test results, we set the reference voltage V_{ref} to 1.8 V during our tests. Additionally, the minimum start-up voltage of the proposed system is 0.4 V. The maximum output power of the system reaches 160 μW at $V_{\text{OC}} = 3.5$ V. Fig. 19(b) shows the measured relationship between MOPIR versus $P_{\text{IN\_FBR}}$ at different output voltages. When the input power $P_{\text{IN\_FBR}}$ is in the range of 1.42–28.4 μW, the MOPIR of the proposed system is always greater than 4. Fig. 20 provides the measured power breakdown of the proposed system.

Table I shows the comparison of the proposed work with the state of the art. This work demonstrates power enhancement

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TABLE I
PERFORMANCE COMPARISON WITH PREVIOUS WORKS

	JSSC'17[10]	ISSCC'19[23]	ISSCC'19[22]	ISSCC'22[24]	JSSC'23[14]	**This work**
Technology	0.35 μm	0.18 μm	0.18 μm HV	0.65 μm	0.18 μm	**0.18 μm**
Piezoelectric harvester	MIDE V21BL	MIDE PPA1021	Custom MEMS	N/A	Piezo-1803YB	**MIDE PPA1021**
Inherent capacitor C_P	45 nF	22 nF	1.94 nF	N/A	22 nF	**66 nF**
No. of PT	1 PT	1 PT	4 PT units	3 (TEG/PT/PV)	1 PT	**3 PT units**
Energy Extraction Technique	SSHC	SPFCR	SE-SSHC	MSVR SECE[2]	SSHSC	**CF-SSHC**
Excitation type	Periodic	Periodic	Periodic	Periodic	Periodic	**Periodic & shock**
Operating Freq.	92 Hz	200 Hz	219 Hz	N/A	130 Hz	**49Hz-87Hz**
Key Component	8 caps, 17 phase	4 caps, 21 phase	8 caps, 17 phase	1 ind, 22μH	3 caps, 8 phase	**6 caps, 37 phase**
Flipping Capacitors C_{total}	360 nF	272 nF	4 nF	N/A	233 μF	**132 nF**
C_{total} / C_P	8	12.36	2.06	N/A	10600	**2**
Converter Topology	N/A	SC DC-DC	N/A	Buck-boost	N/A	**SC DC-DC**
No. of Outputs	1	1	1	4	1	**3 (1.5V/ 3V/ 4.5V)**
Max Flipping Voltage	Below 5V	Below 6V	10.2V	Below 5V	Below 5V	**Below 5V**
Flipping Efficiency	0.8	0.84	0.85	0.5	0.78	**0.83**
MOPIR	270% - 970%	370% - 626%	257% - 589%	320%	758%	**506% (off-resonance) 478% (on-resonance) 214% (shock)**
FoM[1]	0.34 - 1.21	0.3 - 0.5	1.24 - 2.85	N/A	0.0007	**1.07 - 2.53**
Input power	N/A	0.1 μW - 9 μW	N/A	0.6 μW - 300 μW	N/A	**1.42 μW - 28.4 μW**
Max Output power	161.8 μW	64 μW	186 μW	1.2 mW	289.5 μW	**193.3 μW**
Chip Size	2.9 mm^2	0.2 mm^2	5.4 mm^2	3.11 mm^2	0.18 mm^2	**0.42 mm^2**

[1] FoM = MOPIR / (C_{total}/C_P).
[2] [24] is based on SECE, which has different performance metrics from those of SSHI/SSHC interfaces.

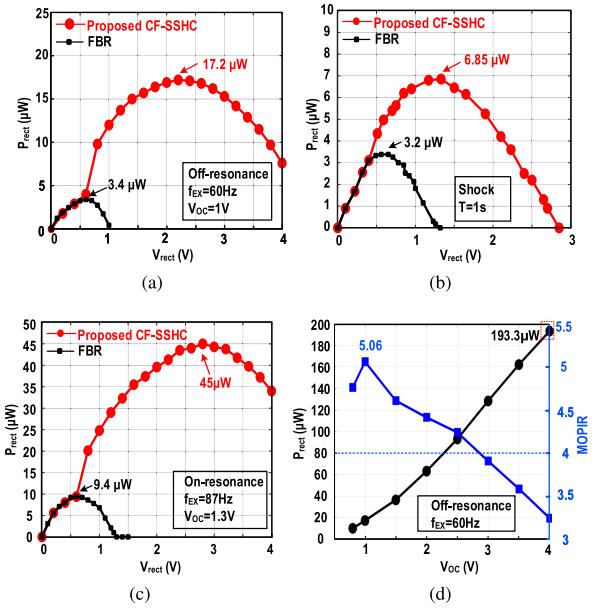

Fig. 18. Measured output power of the CF-SSHC rectifier under various excitations. (a) P_{rect} versus V_{rect} under off-resonance conditions. (b) P_{rect} versus V_{rect} under shock excitation. (c) P_{rect} versus V_{rect} under on-resonance conditions. (d) P_{rect} and MOPIR versus V_{OC}.

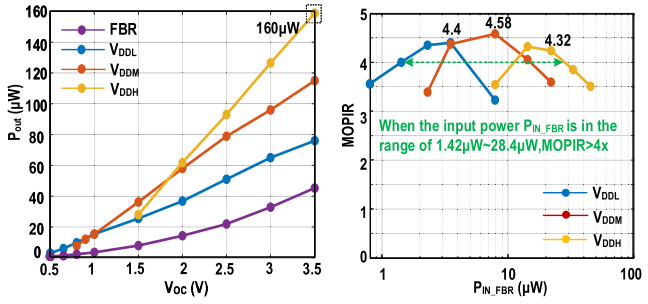

Fig. 19. Measured output power under different outputs. (a) P_{OUT} versus V_{OC}. (b) MOPIR versus $P_{\text{IN\_FBR}}$.

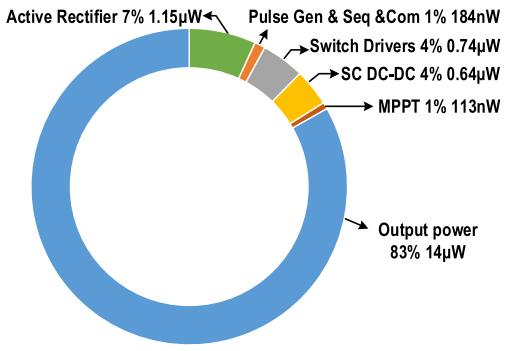

Fig. 20. Power breakdown of the proposed system.

without increasing the number or size of flipping capacitors compared to [10] and [14]. The proposed CF-SSHC uses only standard transistors, thereby avoiding the high switching losses and leakage current associated with series-connected PT units, as demonstrated in [22] and [15] employed the multistage soft-charging (MSC) technique to reduce the normalized capacitance (C_{fly}/C_p), achieving a higher FoM. However, our work offers multioutput capability and system

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adaptability, validated through comprehensive testing under both periodic and shock conditions.

V. Conclusion

This article introduces a novel CF-SSHC rectifier and the SC dc–dc converters employing the shared flipping capacitor. The proposed CF-SSHC technology can effectively increase the flipping phase and output power without increasing the flipping capacitance. Its scalability and adaptability to various PT unit configurations make it a promising solution for the evolving needs of IoT networks. By efficiently allocating flying capacitors, it optimizes resource usage and offers a compact design suitable for the multiinput multioutput PEH system.

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Jing Wang received the B.S. degree in microelectronics from Xidian University, Xi'an, China, in 2020. She is currently pursuing the Ph.D. degree with Fudan University, Fudan, China.

Her research interests include ultralow power management systems and piezoelectric energy harvesting systems.

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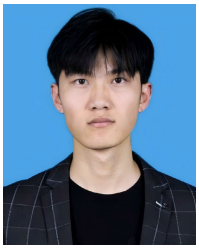


Yi Yang received the B.E. degree in microelectronics from Xidian University, Xi'an, China, in 2020. He is currently pursuing the Ph.D. degree with the School of Microelectronics, Fudan University, Shanghai, China.

His current research interests include power management and energy harvesting.

Zhen Li received the B.S. degree from Anhui University, Hefei, China, in 2016, the M.E. degree from Ningbo University, Ningbo, China, in 2019, and the Ph.D. degree from Fudan University, Shanghai, China, in 2024.

He is currently a Post-Doctoral Researcher at Zhangjiang Laboratory, Shanghai. His research interests encompass piezoelectric energy harvesting systems and power management integrated circuits.

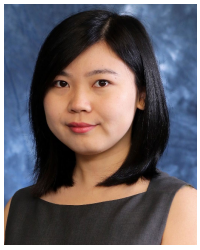
Sijun Du (Senior Member, IEEE) received the B.Eng. degree in electrical engineering from Sorbonne University, Paris, France, in 2011, the M.Sc. degree in electrical and electronics engineering from Imperial College, London, U.K., in 2012, and the Ph.D. degree in engineering from the University of Cambridge, Cambridge, U.K., in 2018.

He was with the Laboratory LIP6, Sorbonne University, and then he was a Digital IC Engineer in Shanghai, China, from 2012 to 2014. He was a Post-Doctoral Researcher at Berkeley Wireless Research Center (BWRC), Department of Electrical Engineering and Computer Sciences (EECS), University of California at Berkeley, Berkeley, CA, USA, from 2018 to 2020. Since 2020, he joined the Department of Microelectronics, Delft University of Technology (TU Delft), Delft, The Netherlands, where he is currently an Assistant Professor. His current research is focused on power management integrated circuit designs.

Xinling Yue (Graduate Student Member, IEEE) is currently pursuing the Ph.D. degree in microelectronics with the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands.

She joined the Electronic Instrumentation Laboratory, Delft University of Technology, in December 2020. Her current research interests are energy-efficient power management integrated circuits and systems, which include energy harvesting, ac/dc rectifiers, dc/dc converters, and MPPT techniques.

Ms. Yue received the Best Student Paper Award at the 2022 IEEE International Conference on Electronics Circuits and Systems (ICECS), the Student Travel Grant Awards at the 2022 IEEE International Symposium on Circuits and Systems (ISCAS), the 2023 International Solid-State Circuits Conference (ISSCC), and the 2023–2024 Solid-State Circuits Society (SSCS) Predoctoral Achievement Award.



Xun Liu (Member, IEEE) received the B.Eng. degree in electronic and information engineering from Zhejiang University, Hangzhou, China, in 2011, and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2017.

In 2017, she was a Post-Doctoral Fellow with HKUST and an Engineering Intern with the Department of Power Management IC, Qualcomm Technologies, Inc., San Diego, CA, USA. She was a Senior Analog Designer with Qualcomm, Santa Clara, CA, USA, from 2018 to 2021. In 2021, she joined Chinese University of Hong Kong (CUHK), Shenzhen, China, as an Assistant Professor. Her research interests include power management integrated circuit (IC) and analog IC design, especially in high-frequency dc–dc converters, hybrid power converters, and power amplifier supply modulator design.

Dr. Liu has been a member of the International Technical Program Committees of the IEEE International Solid-State Circuits Conference (ISSCC) since 2021 and the Eighth International Workshop on Power Supply on Chip (PwrSoC) since 2022. She was a recipient of the President Young Scholar Award from CUHK and the Qualcomm Patent Award in 2020. She was a co-recipient of the ASP-DAC University LSI Design Contest Special Feature Award in 2018. She served as the Session Chair for ISSCC 2022–2024. She also served on the review committee of APCCAS 2022.

Jun Han (Member, IEEE) received the B.S. degree from Xidian University, Xi'an, Shanxi, China, in 2000, and the Ph.D. degree in microelectronics from Fudan University, Shanghai, China, in 2006.

He joined Fudan University as an Assistant Professor in July 2006, where he is currently a Full Professor with the State Key Laboratory of Integrated Chips and Systems. His current research interests include domain-specific processors and systems for digital signal processing, machine learning, and human–computer interaction.

Xiaoyang Zeng (Senior Member, IEEE) received the B.S. degree from Xiangtan University, Xiangtan, China, in 1992, and the Ph.D. degree from Changchun Institute of Optics, Fine Mechanics and Physics, Chinese Academy of Sciences, Changchun, China, in 2001.

From 2001 to 2003, he was a Post-Doctoral Researcher at Fudan University, Shanghai, China. Then, he joined the State Key Laboratory of Integrated Chips and Systems, Fudan University, as an Associate Professor, where he is currently a Full Professor and the Director. His research interests include high-performance-energy efficient SoC for information security and artificial intelligence applications, and VLSI implementation of digital signal processing and communication systems.

Zhiyuan Chen (Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees from the University of Macau (UM), Macau, China, in 2011, 2013, and 2018, respectively.

Since 2018, he has been with the School of Microelectronics, Fudan University, Shanghai, China, as a Post-Doctoral Researcher, where he is currently an Associate Professor. His research interests include ac–dc rectifiers, dc–dc converters, and energy harvesting systems.

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