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DOI
10.1109/ESSERC62670.2024.10719584

Publication date
2024

Document Version
Final published version

Published in
ESSERC 2024 - Proceedings

An MPPT-Integrated Bias-Flip Rectifier for Piezoelectric Energy Harvesting

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2024 IEEE European Solid-State Electronics Research Conference (ESSERC) | 979-8-3503-8813-8/24/$31.00 ©2024 IEEE | DOI: 10.1109/ESSERC62670.2024.10719584

***Abstract*—Piezoelectric energy harvesting (PEH) is a promising approach to collecting ambient kinetic energy as the power supply for electronic devices. In many PEH designs, the maximum power point tracking (MPPT) technique is exploited to enhance the output power of the system. However, a typical PEH system requires a separate power stage for MPPT, which requires a large external rectified capacitor for MPPT operation and suffers from cascaded power efficiency loss. This paper presents an MPPT-integrated bias-flip rectifier where the MPPT and AC-DC rectifier are merged into one stage, resulting in fewer off-chip capacitors, faster MPPT, and less cascaded energy loss. The proposed circuit was fabricated in a 0.18μm CMOS process, and the measurement results show a 7.7$\times$ energy extraction enhancement.**

***Index Terms*—Energy harvesting, rectifiers, piezoelectric transducer, maximum power point tracking (MPPT), duty-cycled-based (DCB).**

I. Introduction

To render low-power wireless sensors self-autonomous, there is a growing interest in energy harvesting (EH). Piezoelectric energy harvesting (PEH) is a promising approach to collecting ambient kinetic energy to power wireless devices, such as health monitors and wearable devices, where the batteries cannot be charged or replaced easily. Compared with other EH schemes, PEH is preferred due to its high power density and scalability. A piezoelectric transducer (PT) can be modeled as an AC current source I_P in parallel with a capacitor C_P. A full-bridge rectifier (FBR) is commonly used with PTs; however, it suffers from significant energy loss despite its simplicity. To increase the output power of a PEH system, many active rectification approaches have been proposed [1]–[7], among which the synchronized switch harvesting on inductor (SSHI) rectifier show high energy extraction abilities. It works by synchronously flipping the voltage across the PT, V_{PT}, with a switched inductor to reduce the energy loss due to discharging and charging V_{PT}.

Fig. 1(a) shows the block diagram of a typical PEH system. The extracted power by the rectifier depends on the output voltage of the rectifier, V_R. To enhance the energy-extraction performance, the maximum power point tracking (MPPT) is required to regulate V_R at its optimal level. To achieve this, typical PEH systems employ a separate MPPT stage to regulate V_R, hence, to track the maximum power point (MPP). Conventional MPPT control techniques include perturb-and-observe (P&O) [2], [5] and fractional open circuit voltage (FOCV) [8]. A simpler duty-cycle-based MPPT technique

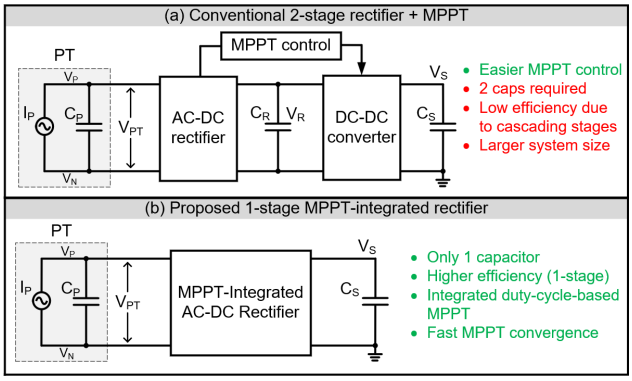


Fig. 1: Piezoelectric energy harvesting with (a) conventional and (b) proposed architectures.

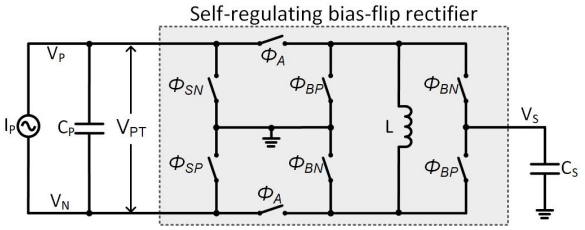
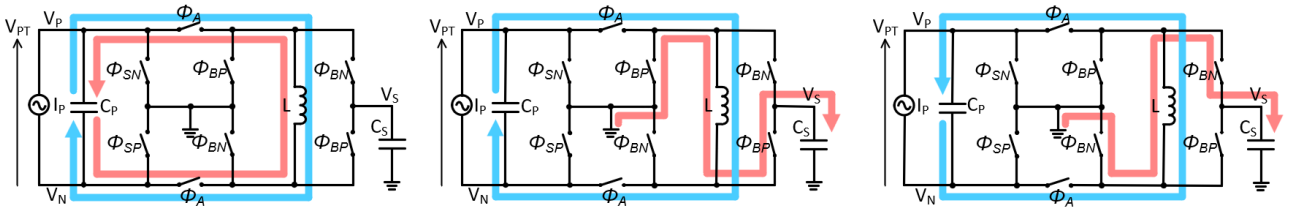


Fig. 2: The proposed MPPT-integrated bias-flip interface.

was proposed in [9] by setting the conducting duty of the rectifier at 50% to achieve the MPPT. Despite efficient MPPT performance, the two-cascading-stage architecture shown in Fig. 1(a) necessitates an external capacitor, C_R, resulting in a larger system size and a longer time to track a new MPP. Additionally, the two-stage architecture incurs cascaded efficiency losses.

In this paper, to address the drawbacks of a 2-stage PEH system, a single-stage MPPT-integrated bias-flip rectifier is proposed, as illustrated in Fig. 1(b). The MPPT operation is performed inside the rectifier, based on a DCB MPPT algorithm, by controlling the build-up time of the PT voltage in every half-vibration period. Thanks to the single-stage architecture and the DCB MPPT, only 1 off-chip capacitor, C_S, is needed. The DCB MPPT allows the PT voltage (V_{PT}) to directly climb to the MPP (V_{MPP}) without charging or discharging an intermediate capacitor. When V_{PT} arrives at the MPP, the rectifier starts to extract energy while regulating V_{PT}. Compared to conventional 2-stage architectures, the proposed



(a) PT voltage flipping (b) Multi-shot when V_{PT}>0 (c) Multi-shot when V_{PT}<0

Fig. 3: Switch configuration and current flow of each phase in the proposed rectifier.

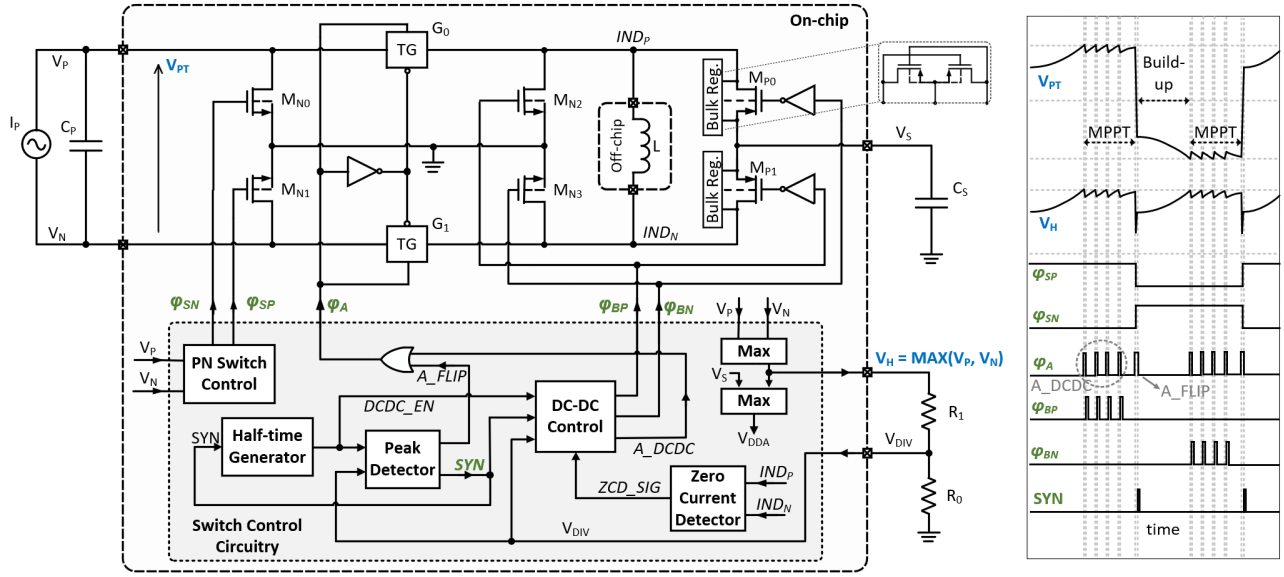


Fig. 4: Top-level architecture of the proposed rectifier with waveform of key signals.

architecture has only 1 off-chip capacitor and it eliminates cascaded energy loss.

II. Proposed MPPT-integrated Bias-Flip Rectifier

A. Operations and Analysis

Fig. 2 shows the proposed MPPT-integrated bias-flip rectifier, which consists of an inductor and 8 switches. The operation phases are shown in Fig. 3. By configuring the switch phases, the interface circuit is able to flip the voltage across C_P in phase (a), and be configured as a DC-DC converter to regulate V_{PT} in (b) and (c), according to the polarity of V_{PT}. Combined with the DCB MPPT, the proposed rectifier can achieve MPPT by simply setting the duty cycle of phase (b), or (c), at 50%. A simplified output power analysis of the proposed DCB-MPPT-integrated rectifier is given below.

The current source (I_P) can be expressed as $I_P = I_0 \sin \omega t$, and the open-circuit voltage amplitude from the PT can be derived to $V_{OC} = I_0/\omega C_P$. Assuming the V_{PT} build-up time after voltage flipping is t, and, after that, V_{PT} is regulated at V_R. The output power in C_S becomes:

$$P_S = 2fV_R V_{OC} C_P (1 + \cos \omega t) \times \eta_{dcdc}. \quad (1)$$

where f is the vibration frequency and η_{dcdc} is the DC-DC conversion efficiency of the multi-shot MPPT phases. By setting the derivative to V_R at 0, we can derive the MPPT condition, which is $t = \frac{T}{4}$. This result shows that the voltage build-up time and Multi-shot MPPT time should be equal to obtain maximum power, which can be expressed as:

$$P_{MPP} = \frac{2fV_{OC}^2 C_P}{1 - \eta_F} \times \eta_{dcdc}. \quad (2)$$

B. Top-level Architecture

Fig. 4 shows the top-level system architecture of the proposed rectifier (left) and associated waveform of key signals (right). The system includes a power stage and a switch control circuitry. The power stage contains 8 switches. Switches M_{N0-N3} are implemented with NMOS devices because they have their sources connected to the ground. Switches $M_{P0,\ P1}$ are implemented with PMOS. Bulk regulation circuits are added to the PMOS transistors to prevent the body diodes from conducting. Switches $G_{0,\ 1}$ are implemented with transmission gates since they need to transfer both low and high voltage levels during different phases. The switches are driven by 5 level-shifting drivers, which consist of level shifters to shift the control signal to a higher voltage level V_{DDA}, and chains of switch drivers. The waveform on the right shows V_{PT} being synchronously flipped with the signal SYN, and being regulated to the MPP with the signals φ_{BF} (or φ_{BF}) when V_{PT} is positive (or negative). The target voltage of V_{PT} to be

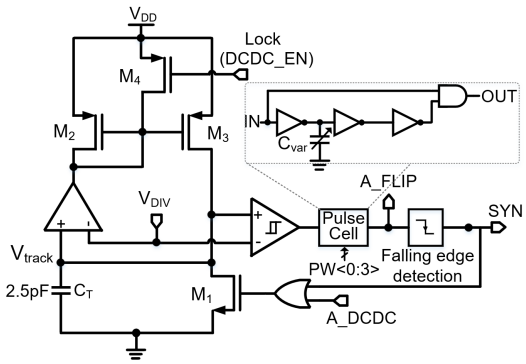


Fig. 5: Circuit diagram of the peak detector.

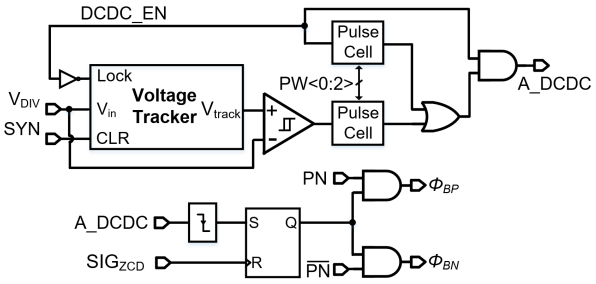


Fig. 6: Diagram of the DC-DC control block.

regulated is determined by keeping the build-up time equal to the MPPT time. In the following, the peak detector and DC-DC control blocks will be detailed, which are responsible for flipping and regulating V_{PT}, respectively.

C. Peak Detector

Fig. 5 shows the circuit diagram of the peak detector for detecting the zero-crossing moment of I_P. It is composed of a voltage tracker, a hysteresis comparator, and signal generation cells. When V_{DIV} is rising, M_2 and M_3 are turned on and will charge a C_T so that the voltage V_{track} can follow the ascent of V_{DIV}. When V_{IN} just begins to decrease, V_{track} will be held on C_T, and the output of the hysteresis comparator will go from low to high, which indicates the peak of V_{DIV}. Since V_{DIV} is a divided version of V_H, which is the max between V_P and V_N, the flipping moment can be determined. The MOSFET M_1 is used to clear the charge on C_T to reset the state of the voltage tracker, while M_4 is used to disable and lock the voltage tracker during off-state. When a peak voltage is detected, the pulse cell will generate a *A_FLIP* pulse to turn on the two switches, G_1 and G_2, to flip V_{PT}. When the *A_FLIP* pulse is over, a SYN signal will be produced by a falling edge detection circuit.

D. DC-DC Control

Fig. 6 shows the circuit diagram of the DC-DC control block. The DC-DC converter employs a constant-on-time and hysteresis regulation scheme. After V_{PT} is built up for a quarter of a vibration period (T/4), the voltage tracker will

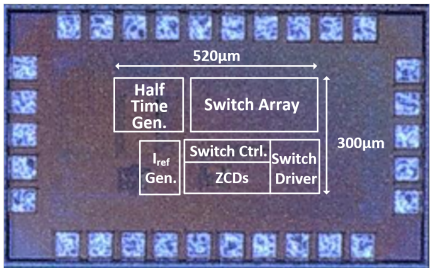


Fig. 7: Chip micrograph.

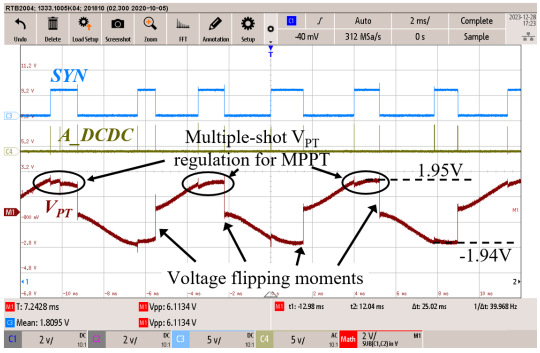


Fig. 8: Measured waveforms showing the V_{PT} voltage flipping and regulation.

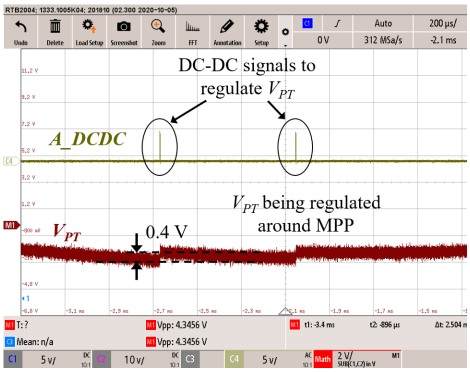
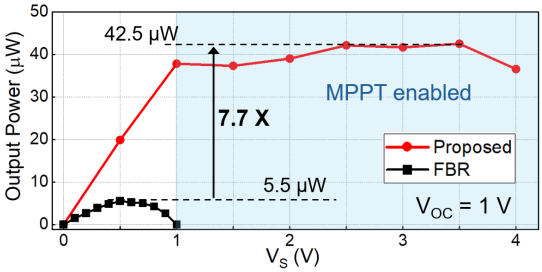


Fig. 9: Measured waveforms showing the multi-shot energy transfer for V_{PT} regulation.

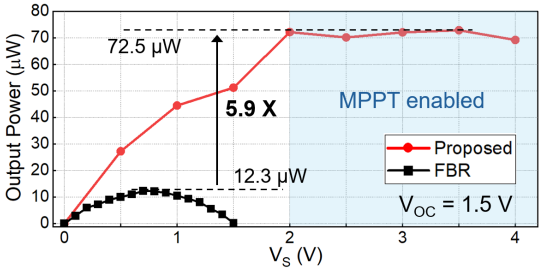
sample the V_{DIV} on the capacitor and use it as the reference for voltage regulation, using the same voltage tracker circuit as in Fig. 5. When input voltage V_{DIV} goes higher than the reference, a pulse signal *A_DCDC*, with programmable pulse width, is generated to energize the inductor with PT. After *A_DCDC*, the inductor charges the output by turning on φ_{BP} (or φ_{BN} if $V_{PT} < 0$) controlled by the zero current detector. Multiple DC-DC conversions will be performed until the peak detector detects the zero-crossing of I_P, which will clear the sampling capacitor and start flipping V_{PT}.

III. Measurement Results

The proposed rectifier was fabricated in a 180-nm BCD process with an active chip area of $0.156\,\mathrm{mm}^2$. The die microphoto is shown in Fig. 7. Fig. 8 shows the measured



(a) Output power versus V_S when $V_{OC} = 1V$.



(b) Output power versus V_S when $V_{OC} = 1.5V$

Fig. 10: Output power versus V_S voltage at different V_{OC}.

waveform of V_{PT}, which is synchronously flipped and regulated at the maximum power point (around 1.95 V) with the DCB MPPT technique. Fig. 9 shows the zoomed-in waveform when V_{PT} is regulated around the MPP with a voltage ripple of 0.4 V. The driving signal, *A_DCDC*, is generated to perform the DC-DC energy conversion.

Fig. 10 shows the output power at different V_S values. When V_{OC} equals to 1 V and 1.5 V, the proposed rectifier achieves 7.7× and 5.9× output power enhancement, respectively, compared to a passive full-bridge rectifier with near-zero-voltage-drop diodes. It can also be observed that the proposed rectifier outputs near-constant power when $V_S > 1$ V and $V_S > 2$ V for the two V_{OC} conditions, respectively, thanks to the integrated MPPT allowing the rectifier operating at the MPP constantly. The reason for lower power at low V_S levels is due to the large voltage step-down ratio between C_P and C_S when DC-DC conversion is operating, which lowers the DC-DC efficiency (η_{dcdc}) for the phases in Fig. 3 (b) and (c).

The average power consumption of the whole chip is around 1.17 μW, with the breakdown for different blocks illustrated in Fig. 11. The proposed MPPT-integrated bias-flip rectifier is compared with the prior works, and the comparison is shown in Tab. I. Among all the prior arts with MPPT enabled, the proposed rectifier achieves MPPT and bias-flipping in a single stage, with an output power enhancement of up to 7.7× compared to a full-bridge rectifier.

IV. Conclusion

An MPPT-integrated bias-flip rectifier is proposed in this paper, which integrates the MPPT and bias-flip rectifier in a single stage, to achieve optimal performance of the whole system. It eliminates an output capacitor for MPPT operations,

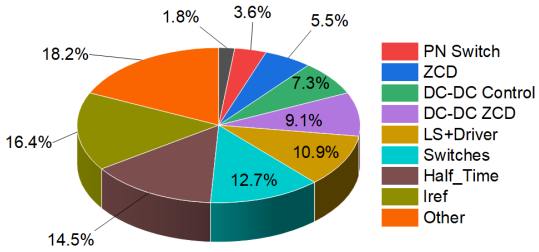


Fig. 11: Power consumption breakdown by different circuit blocks (total consumption: 1.17 μW).

TABLE I: Comparison table with prior arts.

	ESSCIRC 2018[6]	ISSCC 2020[5]	JSSC 2022[1]	ISSCC 2023[4]	ISSCC 2023[9]	JSSC 2023[2]	**This work**
Tech. (μm)	0.13	0.6	0.18	0.18	0.18	0.18	**0.18**
Area (mm^2)	0.53	14	1	1.2	0.47	0.85	**0.156**
f_P (Hz)	430	56	146	130	230	57	**110**
C_P (nF)	14	24	19	100	42	28.8	**22**
Rectifier Type	SSHI	SECE	SSHI	ES-SSHI	SSHI	Cap-SECE	**SSHI**
MPPT?	No	Yes	No	No	Yes	Yes	**Yes**
MPPT Type	–	P&O	–	–	DCB	P&O	**DCB**
Cascaded stages	1*	2	1*	1*	2	2	**1**
P_{IC}/P_{FBR}	3.85	3.28	3.68	6.4–11.7	7.38	5.75	**7.7**

* No MPPT stage

and it achieves up to 7.7× energy extraction enhancement compared to a passive full-bridge rectifier.

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