A SiGe BiCMOS amplifier for spin-qubits low-frequency readout

Towards a scalable quantum computer

Master's thesis

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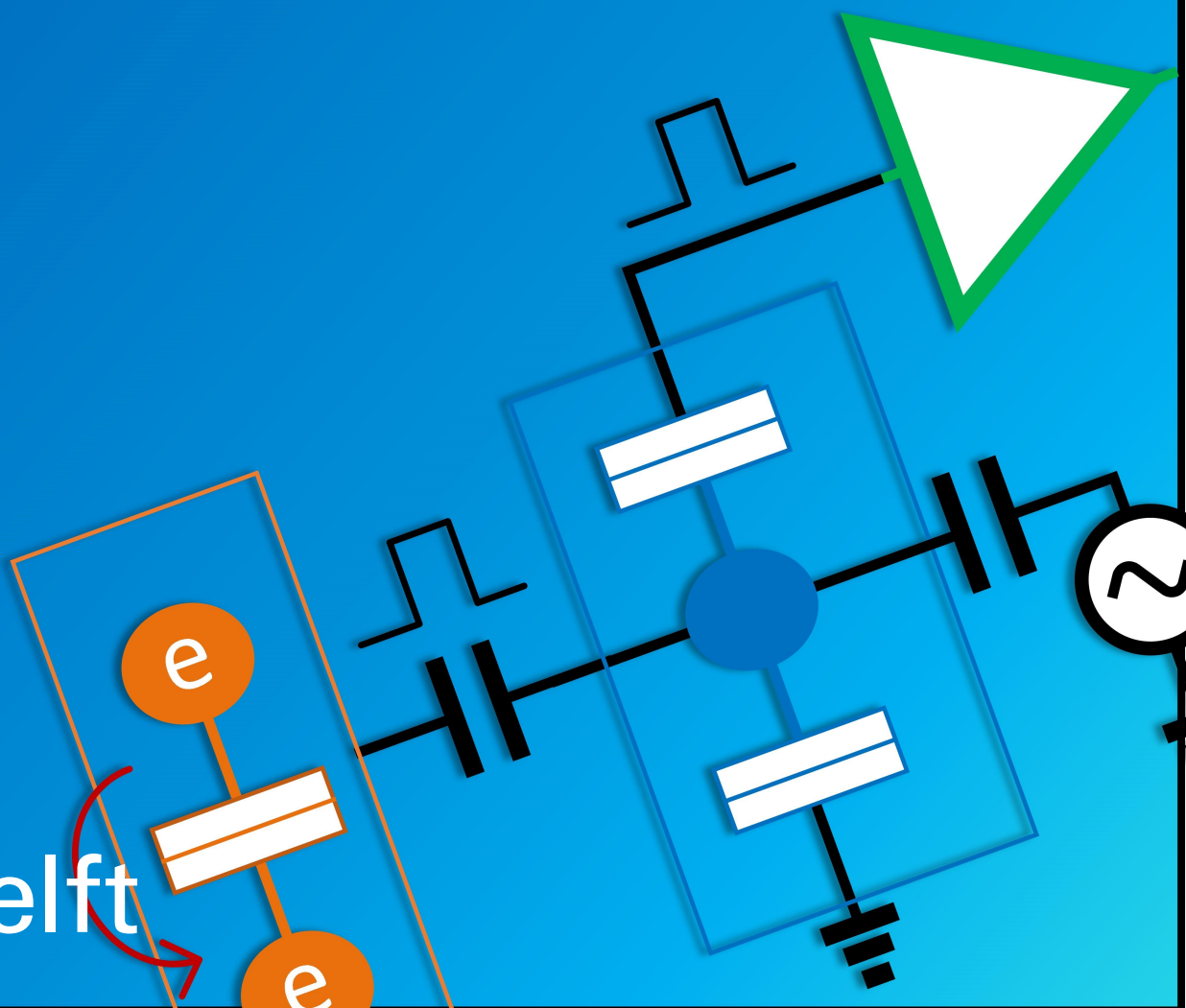
Delft University of Technology



TU Delft

A SiGe BiCMOS amplifier for spin-qubits low-frequency readout

Towards a scalable quantum computer

by

Andrea Costantini

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TU Delft

Acknowledgements

I think it was around March 2021 when Jacopo randomly brought up the idea to send a cover letter to apply for a Master's study in TUDelft. I remember laughing at the idea while we would already dream about the scenario of us studying (but also having a good time, ngl) in The Netherlands, in one of the most prestigious engineering schools in the world. The deadline for applying was already very close when we started preparing the documentation for being admitted, so the joke rapidly transitioned to a serious urge. It didn't matter that at the time there was also an exam session in PoliTo approaching and demanding our full commitment, because our heads were already travelling kilometers.

Here I am, two years and a half later, writing pages full of pride for what that funny idea turned into.

It is never easy to fit into a country which is not the one where you grew up. Putting myself through the initial discomfort and loneliness of living abroad for the first time enriched me immensely, I will never regret this choice. It felt challenging but fulfilling at the same time to embrace a new lifestyle, I am pretty sure I want to experience this again and again throughout the duration of my life. These two years gifted me with memories (my memory is embarrassing, but fortunately someone invented photographs and video-recording); it gifted me with friendships; it gifted me with mentors to look up to; most importantly, it seduced me with questions.

Dealing with the state-of-the-art technologies makes you really wonder if we as human beings are going towards the right direction, and also makes you proud about what we are able to accomplish.
I have always liked philosophy, and I have always believed that there is more philosophy in engineering and physics than there is in philosophy as a subject. The way we get to know the universe it is really the way we get to know our true selves. Quantum computing is the perfect example of technology where engineering and philosophy cross paths. We are trying to simulate the universe using properties of the universe we barely understand, and I think this is crazy enough to be worth pursuing.

My professor and mentor Fabio Sebastiano provided me with the fantastic opportunity to dive into the world of quantum computers. Thank you for all the knowledge you shared with me and for all the help with this project.
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be interpreted as a sad thing but hey, struggle is due for achieving great results!).

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Andrea Costantini
Delft, August 2023

Perfer et obdura: multo graviora tulisti. Non bene, si tollas proelia, durat amor.

Publius Ovidius Naso

Per Daniele, la persona che mi manca di più quando sono via dall'Italia.

Abstract

The concept of quantum computing is gaining increasing popularity in the last years due to its potential for running certain classes of algorithms much more efficiently than classical computation. These algorithms span from simulation of quantum mechanical effects to factorization of large number, from simulation of molecules for drug discovery to encryption of data.

One of the challenges of the current state-of-the-art of quantum computing is related to the scalability of this technology since, in order to solve the aforementioned problems, the required number of logical qubits in a quantum processor is in the order of millions. Qubits are very fragile systems and, to maintain their encoded information intact over time, it is necessary to keep them (most of the existent qubit classes) at very low temperature in dedicated dilution fridges; spin qubits in particular (the type of qubits that this work will focus on) need to be kept at around 2-300mK in most of the technologies available nowadays. Since having millions of big wires coming out of a fridge to control the qubits is nor feasible nor reasonable, it has been proposed that a big part of the interface electronics is moved from room temperature to cryogenic temperature, close to the qubits.

The readout of a qubit consists in translating its state into a piece of information that can be used for computation in quantum algorithms. In the specific case of spin qubits, the information is encoded in the spin of electrons or quantum states of multiple electrons, when those are subjected to a magnetic field. The weak magnitude of the signal encoding this type of information, together with the temperature at which the system operates result in very strict requirements for power and noise of the integrated circuit.

This work presents a review of the readout process together with the design and simulation of a low frequency readout circuit. Many readout techniques are addressed and pros and cons of each one are discussed before diving into the actual circuit design. The SiGe BiCMOS technology from IHP is analyzed due to its potential for realizing low noise readout circuit. This technology is used in Cadence for simulating and assessing the performance of some proposed readout circuit architectures, namely the Current amplifier, the Voltage amplifier, the Transimpedance amplifier and the Charge amplifier. Eventually, the Voltage amplifier, which shows the more promising results in preliminary simulations, is designed at transistor level and combined with other blocks to realize the whole front-end readout circuit. From the simulation results, it is believed that the circuit can meet the target specification of $10dB$ SNR and achieve a functional reading at cryogenic temperature with a power consumption lower than $10\,\mu\mathrm{W}$ at a speed of $1\,\mathrm{Ms/s}$.

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1 Introduction

1.1 Quantum computing

It was 1982 when Feynman theorized the possibility of simulating quantum mechanics using quantum systems instead of classical computers [1]. From that moment on, many ideas came out about how quantum systems properties could be exploited to solve hard simulation problems: from simulating quantum mechanics itself to running search algorithms [2], from advancing drug discovery [3] to factoring large numbers [4] and many more [5].
Quantum processors exploit quantum properties in order to parallelize a huge number of operations. This is possible because, contrarily to classical computers that encode information in bits with only two possible states (0, 1), quantum computers employ the so-called qubits, elements that encode information in a probabilistic form. When observing (measuring) a qubit, there is no deterministic function that can predict exactly the outcome of the observation, because the qubit is in a state of "superposition". However, after observing a system in superposition, it "collapses" in a classical state and the result of a measurement will be either a 0 or a 1.
The superposition state of a qubit is described in the quantum information theory as $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$, where α^2 is the probability of observing the qubit as a 0 and β^2 is the probability of observing the qubit as a 1. A qubit can be visualized on the so called Block Sphere in figure 1.1.

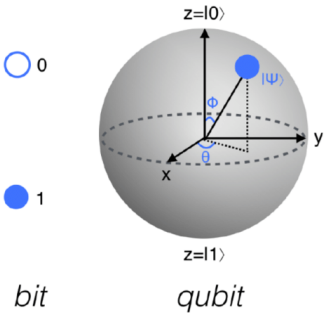


Figure 1.1: Classical bits vs quantum bits, visualized on the Block Sphere

A quantum processor is a bank of many interconnected qubits physically close to each other. The quantum processor, combined with other physical layers (interface electronics) and non-physical layers (software) forms the quantum computer.

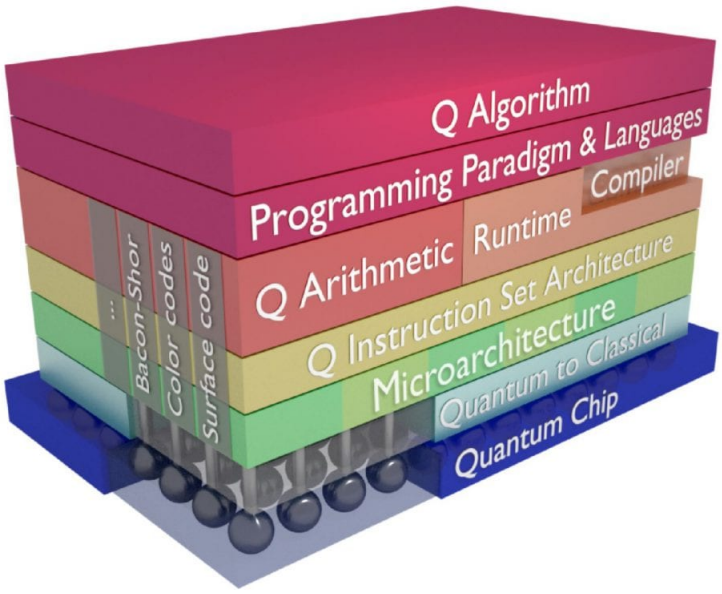


Figure 1.2: Schematic of the various parts of a quantum computer. Image from the QuTech website (https://qutech.nl/research-engineering/quantum-computing/)

The number of qubits necessary for a single quantum computer to solve efficiently the problems mentioned previously is in the order of millions.

1.2 Cryogenic electronics

At the current state-of-the-art, one of the main bottlenecks for the scalability and reliability of quantum computers is the number of interconnects that is necessary to control the quantum processor.

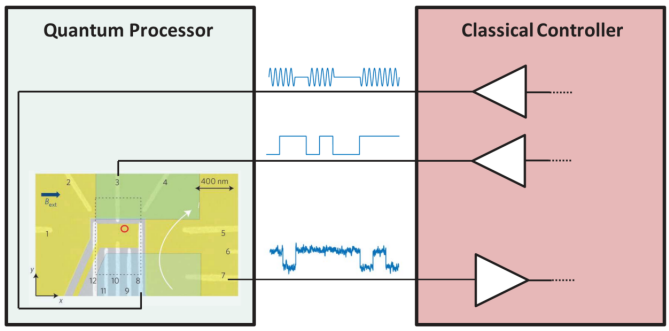


Figure 1.3: Canonical structure of quantum computers from [6]: control and readout electronics and quantum processor are separated by long interconnects

Initially, control and readout electronics were placed at Room Temperature (RT) while the quantum processor was mounted inside a dilution refrigerator and kept at Cryogenic Temperature (CT), between $100\,\mathrm{mK}$ and $300\,\mathrm{mK}$. Such configuration involves having numerous bulky wires coming out of the refrigerator, with unwanted consequences for reliability, scalability and bandwidth of signals.
In the recent years, more and more effort is being put in developing functional and high performance integrated circuits that can work at CT [7] [8] [9]. Voltage references, ADCs and other fundamental digital and analog blocks have been developed and the functionality of these circuits has been proved [10] [11] [12]. For doing so, characterization of well-known technologies like CMOS and emerging technologies like SiGe BiCMOS has been carried out to correctly foresee and simulate the behaviour of devices at low temperatures [13] [14] [15].
This growing research is driven by the goal of co-integrating interface electronics with quantum processor, eventually favouring and accelerating the scaling up of quantum computers. While the electronics blocks are being moved at lower temperatures, research is also being done for realizing functional semiconductor (or spin) qubits at relatively high temperatures, as shown in figure 1.4.

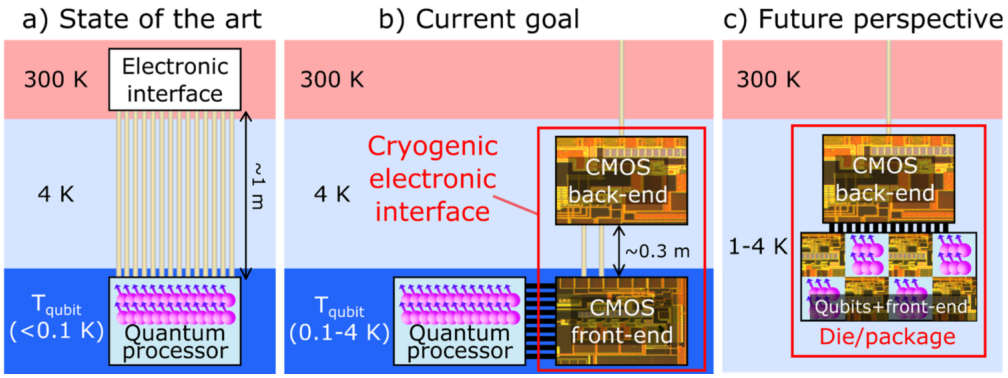


Figure 1.4: Road-map for integration of quantum processors and interface electronics proposed in [8]

1.3 Low frequency readout of spin qubits

Spin qubits are a specific type of qubits that encode information in quantum states (or more simply the spin) of single or multiple electrons; they show good potential for reliability, manufacturing and scalability to realize quantum processors employing a high number of qubits. One important step in running quantum algorithm consists in reading (or measuring) the state of a qubit, also called readout process. In the case of spin qubits, the most popular ways that are being utilized to carry out the readout are the so called RF and DC readout methods. The name DC readout is due to the fact that base-band circuit are utilised, as opposed to RF readout relying on transmission lines and reflectometry. RF readout, despite performing better at the current state than DC readout, relies on bulky and off-chip components. DC readout (or low frequency readout) instead, is of particular interest due to its potential for future integration of the readout circuit together with the qubits.
As this is the desired path for meeting the aforementioned reliability and scalability goals, DC readout is gaining increasing popularity in the field. At the current state-of-the-art however, the proposed DC readout circuits either lack the required fidelity, do not have enough reading speed or demand too high power consumption.
For this reason, this work will attempt to propose a design that improves previous DC readout works on aspects like power, Signal-to-Noise Ratio (SNR, directly related to fidelity) and reading speed, exploiting the low noise and high-efficiency features of SiGe BiCMOS technology.

1.4 Thesis motivation and objectives

A quantum processor that can really impact the world can be realized only if millions of qubits are employed and enabled to communicate with each other on a complex system architecture. For this reason, enhancing the performance of cryogenic circuits for co-integration of qubits and interface electronics is one of the keys to accomplish the main task on the long run; this work is just a small step towards this goal.
The primary target of this thesis project is to design an Integrated Circuit to perform a functional DC readout of spin qubits, exploiting the potential of the low noise Silicon-Germanium (SiGe) Heterojunction-Bipolar-Transistor (HBT). In a more broad scope, the secondary purpose of this work is to clearly define what are the specifications for DC readout, describe what is the environment in which the circuit operates and to assess the main aspects to be considered for the design of a DC readout circuit in future works.

1.5 Thesis outline

The thesis is structured as follows:

Chapter 2:
The background theory of spin qubits is presented. Quantum dots structure and functioning are explained and different readout techniques are discussed. In the end, the characteristics of transistor technologies useful for readout circuits are assessed.

Chapter 3:
The DC readout process is analyzed in detail on the frontend side and all the specifications for the frontend readout circuit are enumerated. Subsequently, different architectures to realize the frontend amplifier, core of the readout circuit, are presented; strengths and limitations are listed for each architecture.

Chapter 4:
The simulation setup and the methods for addressing the circuit performance are summarized; the chosen architecture is designed at transistor level and each block of the system is detailed. After the design, the simulation results are shown and discussed. Eventually, an overview about a possible layout implementation of the circuit is given along with an estimation of the total area.

Chapter 5:
The work is summarized in a conclusion. In the end, some considerations are made about possible improvement on the work and the next steps to take in order to push further the performance of spin qubits low-frequency readout.

2

Readout of spin qubits

In this chapter, basic knowledge about spin qubits and readout methods is presented. Moreover, the technologies for the integrated circuits used in readout circuits are shown.

2.1 Spin qubits

Due to their promising potential for scalability and the possibility of being integrated with well-established Silicon technologies, spin qubits are among the main candidates for realizing the perfect quantum computer [16]. Spin qubits encode data in the spin of a single electron confined in a hole of electrical potential subjected to a magnetic field; a system of this sort contains two possible quantum states (spin up or spin down) and displays all the quantum features described in [17].

2.1.1 Quantum dots

How to isolate a single electron in order to encode information in its spin? An effective approach is to confine the electron mechanically using electrostatic potential as repulsive force. If the size of the area in which the electron is confined is in the same order of magnitude of its wavelength (1×10^{-9} m), then the system exhibits a discrete energy behaviour and it is possible to control the (almost) exact number of electrons inside of it.
The realization of this concept, illustrated in figure 2.1, is called Quantum Dot (QD). The region where a discrete number of electrons (one in this case) can be confined is called "dot" or "island" and it is separated from electrons reservoirs (conductive regions with free carriers) by means of tunnel barriers, very thin regions of insulating material.
The transport of electrons in and out from the dot is regulated by the energy of the dot with

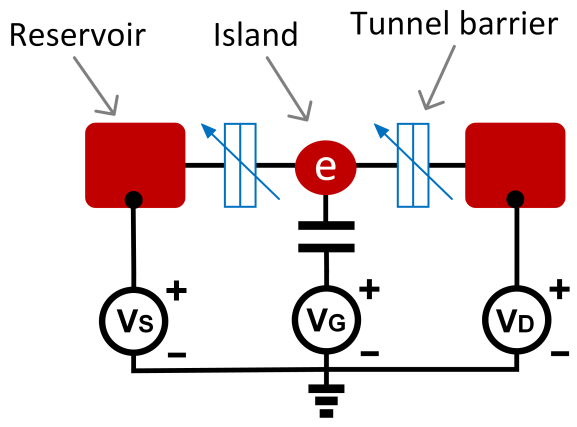


Figure 2.1: Simplistic representation of a Quantum Dot

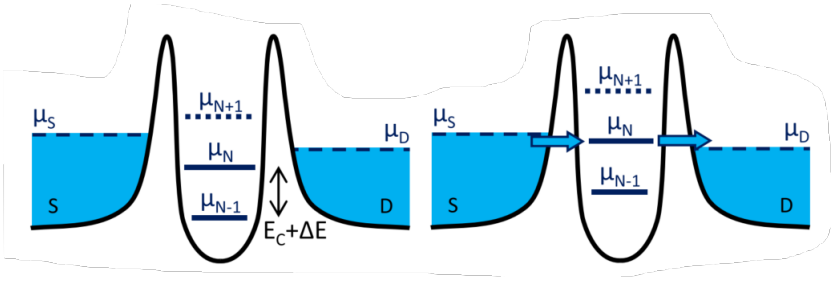


Figure 2.2: Electrochemical potential diagrams explain the charge displacement in quantum dots

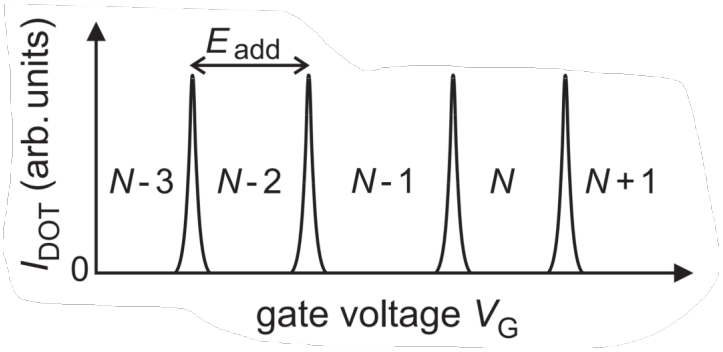


Figure 2.3: General quantum dot characteristics from [19]

respect to the energy of the tunneling barriers and the reservoirs. In figure 2.2 the white barriers represent the tunnel junctions, while the blue areas represent the reservoirs filled with electrons. Based on the voltage that is applied to the reservoirs and the dot, their electrochemical potential (μ_S, μ_D and μ_N) can be manipulated. N is a function of the energy of the dot and indicates the number of electrons trapped in the island. If the condition $\mu_S > \mu_N > \mu_D$ is satisfied, a favoured potential path is present and electrons can flow from the Source (S) to the dot and from the dot to the Drain (D) [18]. Every time that the voltage crosses the next threshold, a new electron is allowed to tunnel and therefore a spike in current is observed. Away from these values of voltage instead, the aforementioned condition is not satisfied and no current is allowed to flow: the system is said to be in a state of Coulomb Blockade (CB) [19].
As a result, the $V-I$ characteristics of this system looks like what is shown in figure 2.3. In order to ensure a regime where single-electron-tunneling is the only transport mechanism happening in the dot, it must be $K_B T << E_C$ [18] (where E_C is the Charging Energy of the dot). If this is not the case, multi-electron transport and other phenomena like co-tunneling take place, and there is only little control over N. For this reason, quantum processors based on spin qubits that are read using PSB need temperatures in the order of $100\,\mathrm{mK}$ to be read correctly, even though engineering materials is leading to qubits working at higher temperatures (still cryogenic temperature, but in the order of few K [20] [21]).
A spin qubit should be maintained in its state for a time window long enough to read and process the information that it contains. Two main phenomena limit the time that a physical qubit can preserve its information: relaxation and dephasing. Relaxation time T_1 is the time it takes for a qubit in an excited state to decay to the ground state ($\langle 1| \longrightarrow \langle 1|$); T_1 is usually larger than few ms in Silicon quantum dots. Dephasing time T_2 is instead the amount of time it takes to the phase of the qubits to lose coherence with the phase of other qubits; it reaches up to $100\,\mu s$ in purified ^{28}Si [16] but only about $10\,\mu s$ in modern manufacturing processes [22].
Up to now, a simple structure of a single QD was discussed to introduce the concept. However, for the goal of integrating millions of qubits, such structure needs to be replicated in arrays or even matrices. Examples of this are shown in figures 2.4 and 2.5 from [23] and [16]. The approach is simply to place QDs one next to each other in arrays. With such disposition, the dots are coupled to each other and there are no reservoirs near each of them: this poses numerous challenges on the control and readout of these qubits. These structure are now being investigated further and

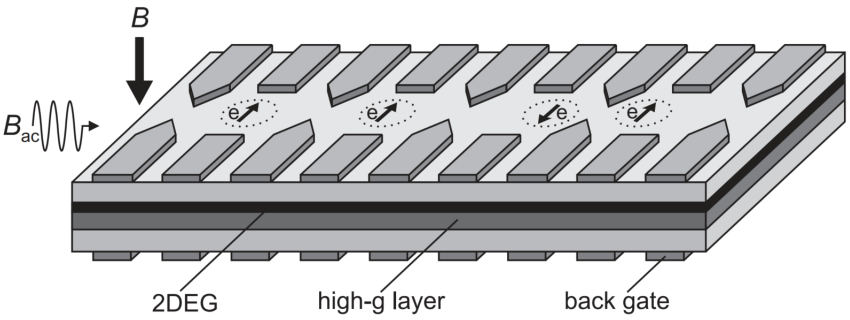


Figure 2.4: Array of quantum dots described in [23]

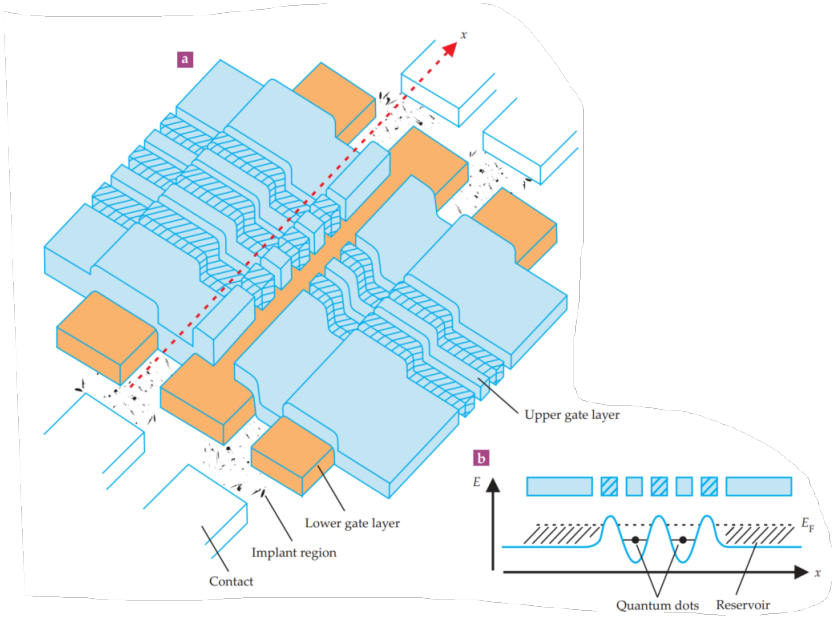


Figure 2.5: 2-D Array of quantum dots using gates on top of the Si substrate from [16]

their manufacturing is becoming more and more reliable [22]; moreover, new methods to tune and control these so-called "qubyte registers" have been developed [24]. It is hypothesized in [25] that due to the limitation of controlling too many qubits in a matrix, a structure with sparse qubit arrays each one with local electronics chip could be the solution for a scalable quantum processor.

2.2 Readout methods of spin qubits

From the algorithm point of view, the readout process of a qubit consists of measuring its state. The only kind of information that can be extracted from a qubit is a well-defined classical bit, meaning that a measurement transports the qubit out of its superposition state ($\alpha|0\rangle + \beta|1\rangle$) and makes it collapse into a classical state (0 with probability α^2 and 1 with probability β^2). Since no copy of the qubit can be available [26] and its superposition state is lost after observing it, the measurement must be a "single-shot" readout.
From a physical perspective, reading a qubit consists in mapping the resulting collapsed classical information in a measurable quantity such as charge, voltage or current. In spin qubits, the physical property that encodes the information is the spin of an electron subjected to a magnetic field. Complex experiments were carried out in history to observe the spin of an electron [27]. Although, for the application of the quantum computer, new methods have been developed to complete this task using compact circuits that operate in short time and allow the integration of reading operation with running quantum algorithms. These methods all rely on the Spin-To-Charge Conversion (STCC).
STCC results in an electrical quantity (charge, easily measurable with ICs) being correlated to the spin, the target of the measurement. In particular, the readout of spin qubits counts three steps [16] [20] [23]:

- States preparation:
  all the barriers and gates are tuned finely in order to initialize the states of the QDs as desired for the measurement.
- Spin-To-Charge conversion
- Analog-To-Digital conversion of the charge information:
  is the main task that the system developed in this work must accomplish. The charge information needs to be converted in a digital format to be used in computation by classical systems, and in some cases fed back to the quantum processor as part of an algorithm.

The passage from STCC to Analog-To-Digital conversion is possible through the use of an electrometer placed near the dots which reacts to a tunneling event by emitting a current/voltage signal. This device was initially a Quantum Point Contact (QPC) [28], recently replaced by the Single Electron Transistor (SET) for larger sensitivity [29] [30].
In the readout process, the SET is placed in close proximity with the target. Any charge displacement close enough to the gate of the SET will modulate its gate voltage, acting as an input signal on top of its biasing V_G. This ΔV_G is translated into a ΔI_{DS} through its transconductance and a ΔV_{DS} through its output impedance as in canonical transistors. The concept is displayed in figure 2.6. The result is eventually an electrical signal which is fed to a 1-bit ADC.
Based on the type of circuit used to perform the analog to digital conversion, the readout is referred to as "RF" or "DC", as it will discussed in sections 2.2.3 and 2.2.4. The first one implements the reading of the charge by means of transmission lines and matching networks operating at high frequencies; the second one, focus of this work, utilises an electrometer and analog circuitry operating in the base-band.

2.2.1 Spin-to-charge conversion techniques

As mentioned previously, STCC involves correlating the spin state of an electron with charge. There are three main ways that have been proposed to accomplish this task in the existing literature:

- Energy-Selective Readout (E-RO)
  This is the most "naive" implementation of STCC in that relies on the Zeeman splitting of

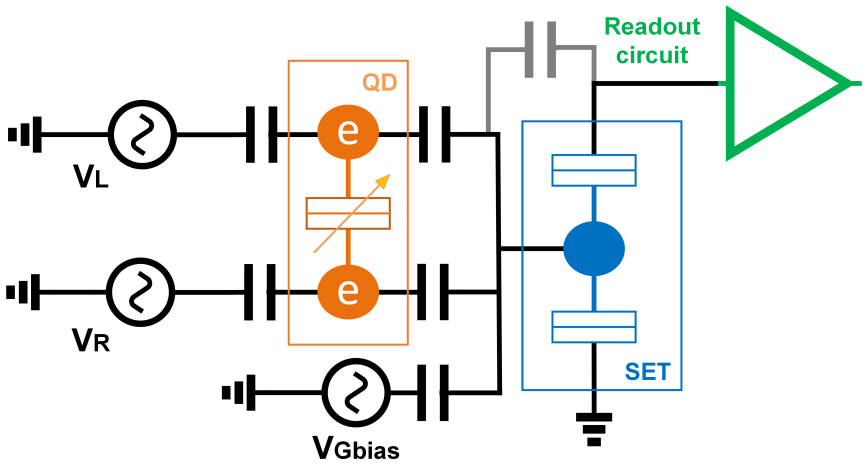


Figure 2.6: Readout configuration employing an SET coupled to a double quantum dot. PSB readout is employed as discussed in 2.2.1. V_R and V_L are respectively the gate voltages of the right and left dot, used to control the number of electrons in the islands. The bias voltage V_{Gbias} of the SET instead is used to place it in the condition of highest sensitivity

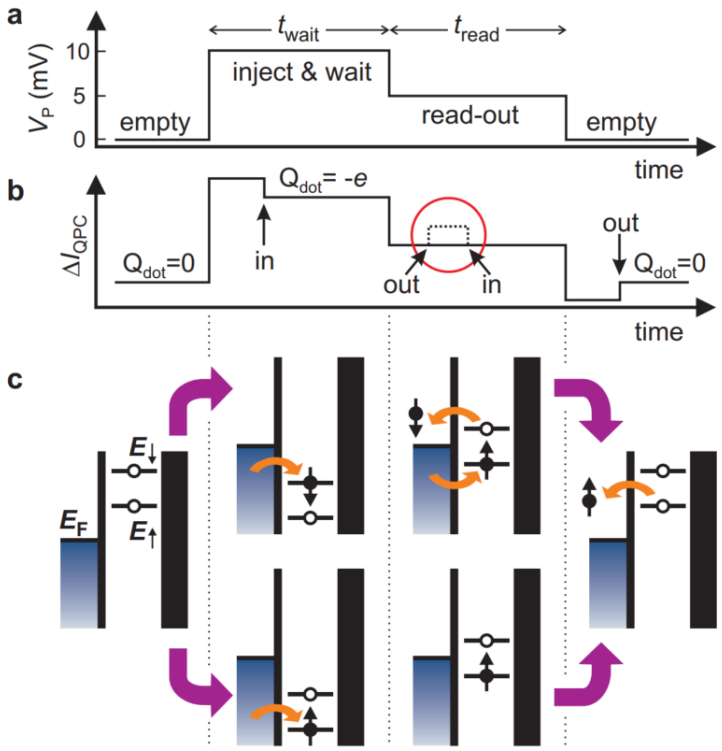


Figure 2.7: Two-level pulse technique exploiting Zeeman splitting to perform STCC [31]

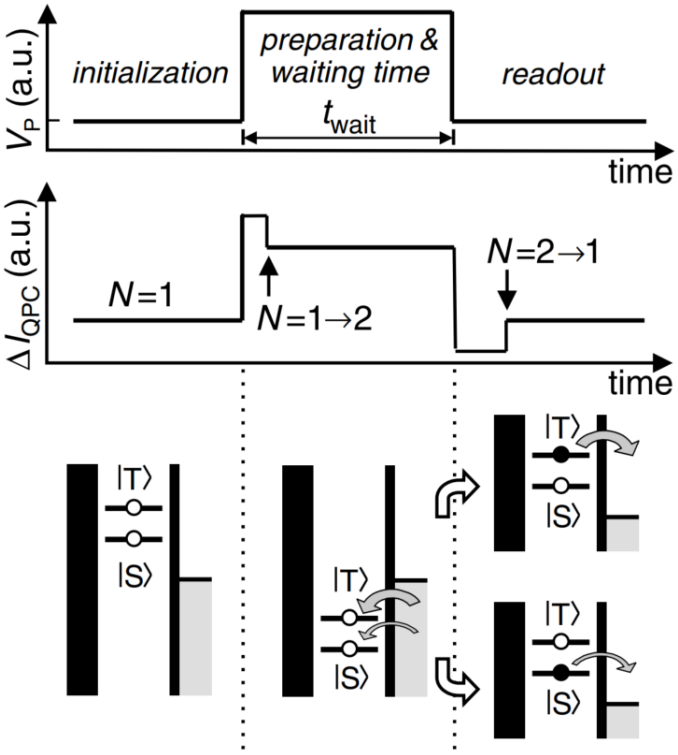


Figure 2.8: Two-level pulse technique using TR-RO to perform STCC [32]

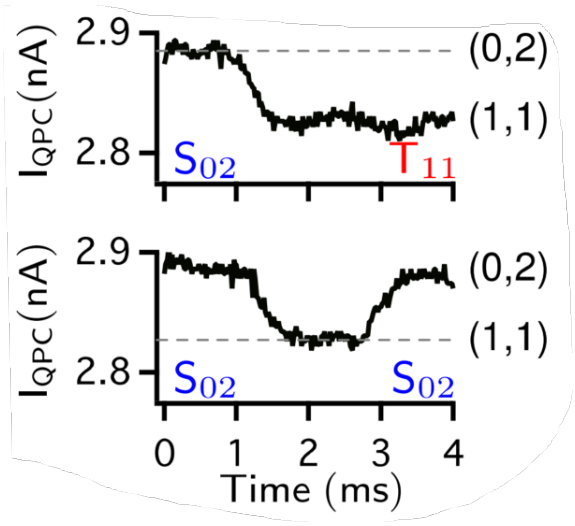


Figure 2.9: Current read from a double QD configuration is shown as function of time, for the two possible initial conditions. Tunneling is allowed (or not) based on the state of the electron already occupying the target dot [28]. In this case the STCC utilises the Pauli-exclusion principle and if the tunneling is allowed, it happens almost instantly after the tuning of the gates

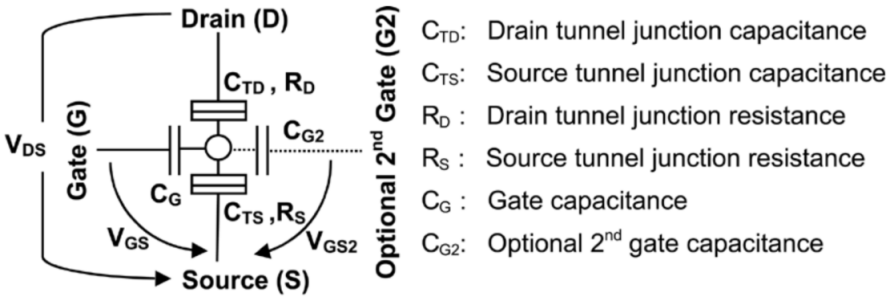


Figure 2.10: SET schematic

energy levels of an electron subjected to a magnetic field. If the field is strong enough, the electron will possess different energy levels based on its spin (for example $E_\uparrow > E_\downarrow$). As described in [31], the potential of the dot can be tuned such that tunneling is energetically favoured only for one of the two spin states. This principle is applied in [31] in the two-level pulse technique shown in figure 2.7. The main drawback of this method is that the difference between the two spin energy levels is small and very subject to high frequency noise and charge fluctuation. This makes challenging to align perfectly the Fermi level of the reservoir E_F inside the splitting range.

- Tunnel-Rate-Selective Readout (TR-RO)
  TR-RO is conceptually very similar to E-RO, although it bypasses the problem of fine tuning of the energy levels [32]. The encoding is not done in this case in the spin of a single electron, but in the quantum state of two or more electrons. This type of qubit is still referred to as spin qubit. The two states carrying the quantum information (Singlet S and Triplet T for example) are placed above the Energy level of the reservoir, hence tunneling is allowed for both cases. The property exploited here is the difference in tunnel rates $\Gamma_T >> \Gamma_S$. If the waiting time before the reading τ is chosen such that $\Gamma_T >> \tau >> \Gamma_S$, then the tunneling event can be correlated to the state and the spin: if tunneling happens after $t = \tau$, the state is declared to be $|T\rangle$, otherwise it is declared $|S\rangle$. The process can be visualized in figure 2.8.

- Pauli Spin Blockade Readout (PSB-RO)
  PSB-RO is the only readout method that can guarantee a (quasi-)deterministic tunneling event, which is very desirable for relaxed readout circuit specifications. Initially proposed in vertical devices [33], it has also been proved in lateral QDs formed in Si/SiGe structures with large coherence times [34] [28]. In this scenario, one dot contains an electron of known spin (ground state $|S\rangle$, as eventually every qubit decays to the ground state), while the other one is the target of the measurement. The two dots can have different effective electron occupancies (m, n), where the two numbers represents the effective number of electrons in the left and right dots. In presence of a magnetic field, the possible states are $|S\rangle = \frac{1}{\sqrt{2}}(|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle)$, $|T_-\rangle = |\downarrow\downarrow\rangle$, $|T_0\rangle = \frac{1}{\sqrt{2}}(|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle)$ and $|T_+\rangle = |\uparrow\uparrow\rangle$. Due to the Pauli exclusion principle, current is only allowed to flow with a transition from $S(1,1)$ to $S(0,2)$, while if the initial state is one of the triplets $T(1,1)$, blockade will occur and this state will be maintained for its lifetime (until natural decaying of T to S).

2.2.2 The Single Electron Transistor

The Single Electron Transistor, as introduced in the previous section, is a nano-scale device useful as electrometer in the readout process due to its high sensitivity [29] [35]. Morphologically, this device is very similar to a quantum dot, although the requirements on the material are less strict and the island can simply be a metallic region. It consists in an island coupled capacitively to a gate and connected to a drain and a source through tunnel junctions, as shown in figure 2.10.

The SET is used though more like a transistor, in that its purpose is to effectively amplify a signal at its gate. Its characteristics also follow the same behaviour of a quantum dot, alternating

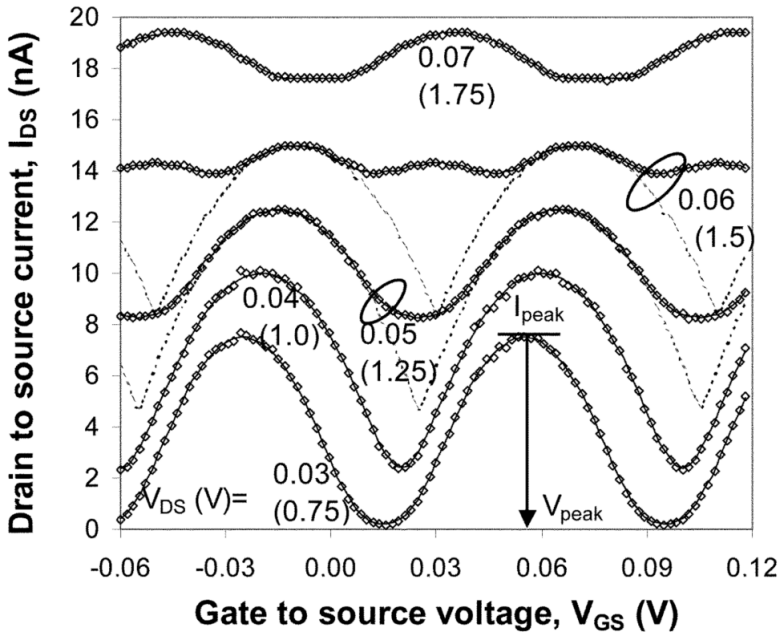


Figure 2.11: SET current characteristics measured in [36]

Coulomb Blockades (CB) states and conducting regimes based on the voltages applied at gate, source and drain 2.11. The bias point in which the derivative of the current is maximal (steepest slope) is the maximum sensitivity point for the device, because a weak voltage signal will result in a relatively large step in current in the channel. If the drain to source current magnitude is visualized as function of both V_{DS} and V_G, the so-called Coulomb diamonds are visible 2.12 if the device is operated at cryogenic temperature, highlighting the discrete nature of the transport mechanism.
Due to its strong non-linearity, it is very hard to predict how the SET interacts with the frontend circuitry and usually a lot of post-realization tuning is required. For the design of large numbers of readout circuits coupled to quantum dots, currently a lot of effort is being put into developing compact models in order to simulate SET and ICs in Circuit design environments like Cadence [36] [37].
For the scope of this work, a handy curve fitting verilog-A model is developed modifying the one realized in [38]; more details about this model will be discussed in chapter 3.1.

2.2.3 RF readout

In the RF-readout, the change in conductance of the SET is measured indirectly from the reflected wave coming back after sending a known high frequency signal towards the SET. The reflected wave can be calculated as in [39]:

$$\Gamma = \frac{Z_{load}(\omega) - Z_0}{Z_{load}(\omega) + Z_0} \tag{2.1}$$

where Z_0 is the characteristic impedance of the Transmission Line (TL) and Z_{load} is the target (SET) impedance. Since $R_{set} >> Z_0 = 50\,\Omega$, the SET resistance has little to no effect on the reflected wave, unless a resonator is added as in figure 2.13. With this configuration the load impedance becomes

$$Z_{load}(\omega) = j\omega L_c + \frac{R_{set}}{1 + j\omega R_{set} C_p} \tag{2.2}$$

At the resonance frequency, such impedance becomes strong function of R_{set}, or in other words the load is now matched to the TL and the outcome of the STCC is effectively correlated with Γ.
This readout method is at the moment the best readout method for fidelity and measurement time, reaching 97% fidelity in $1.5\,\mu$s [40], over 99% fidelity in $300\,$ns [41] and over 99% fidelity in

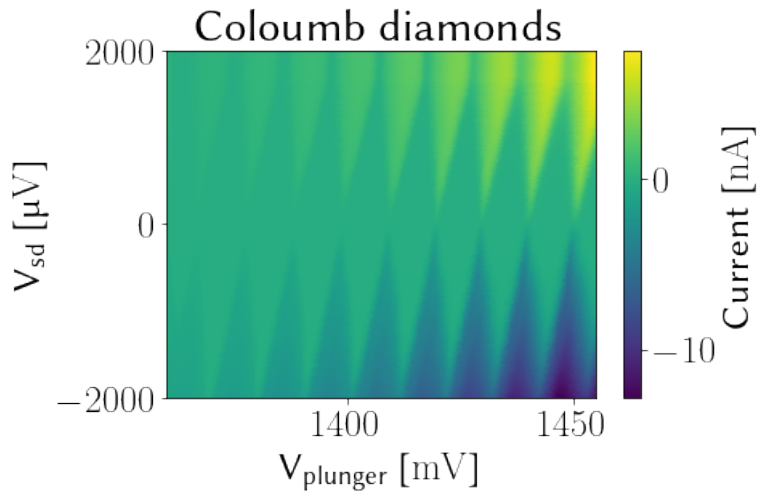


Figure 2.12: SET characteristics measured by Oriol Pietx in Vandersypen Lab, QuTech

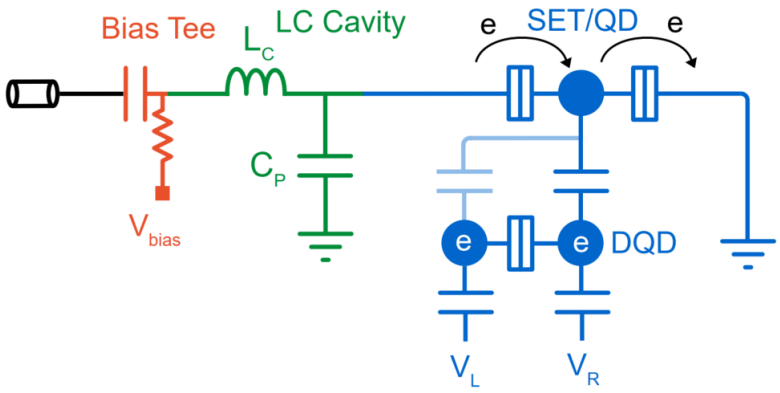


Figure 2.13: RF readout concept: the target device is connected to a matching network and probed with a signal. the reflected wave determines the result of the measurement

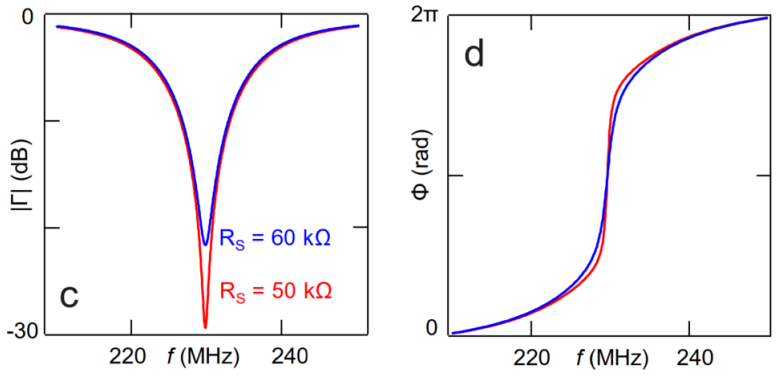


Figure 2.14: When measuring the reflected wave of a LC network, the resonance magnitude can be related to the resistance seen by the resonator [39]. the change in conductance of the SET in particular produces different reflected waves magnitudes for the two states.

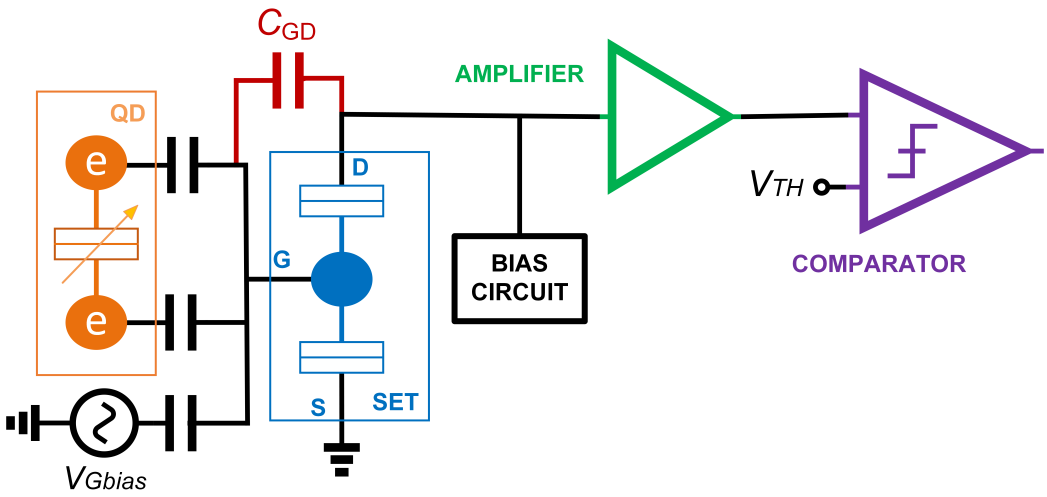


Figure 2.15: DC readout schematic: the change in conductance of the set is directly correlated with a current signal. Due to the input referred noise of comparators, this signal needs to be enhanced in magnitude first using a low noise amplifier; at a certain sample moment, the output signal is compared to a threshold to complete the digitization

[42]. Despite these being exceptional results, this technique has the important limitation of not being scalable, due to the big size of the passives required for the resonator/matching networks (inductors and capacitors). While current experiments regarding spin qubits are all performed using this type of readout, the quantum computer of the future needs an alternative that is able to scale on a large number of qubits. DC readout proposes a more scalable alternative to RF readout, although struggling more with reaching good SNR and BW.

2.2.4 DC readout

DC readout implements base-band analog to digital conversion to translate the charge information into digital information. The quantity observed in DC readout is still the change in conductance of the SET in response to a tunneling event, but the measurement is more direct in that the resulting current signal is directly amplified and then digitized. The schematic of a generic DC readout configuration following a PSB spin-to-charge conversion is shown in figure 2.15. This readout configuration shows more potential for scalability in that it does not require large passives to be realized and could potentially be integrated directly with the qubits. At the current state-of-the-art, this type of readout chain can barely go as fast as $10\mu s$ per reading while achieving the putative Bit-Error-Rate threshold for running quantum error correction algorithms $BER \leq 1 \times 10^{-3}$ [43] [15] [44] [45] [46] (or in other words, fidelity larger than $99.9\,\%$).
Most of the previous works on the topic implement a dual-chip solution where the qubits and the charge sensor are placed at $\approx 300\,\mathrm{mK}$ temperature and the frontend circuit (amplifier + comparator) are placed at $4\,\mathrm{K}$, if not at Room Temperature (RT). This configuration limits the bandwidth of the system due to interconnect parasitics between the chips [38] [15] [43]. The interconnect parasitic, estimated to be about $C_p \approx 2\,\mathrm{pF}$ [38] [15], limits the SNR of the reading because the signal is attenuated before the most significant noise sources are introduced. Reducing the interconnect parasitic capacitance could improve heavily the performance of these circuits, in fact a same chip solution has been proposed [38] and it will probably be realized in the future, given that nowadays it is possible to realize semiconductor qubits with more and more high yield in Si/SiGe and Si/SiO_2 technologies. Two possible architectures proposed in [38] for same and dual-chip solutions are displayed in 2.16.
For the design of the frontend circuit of this work, the worst case of dual-chip solution will be taken as reference when assuming the size of parasitic capacitances not to lose generality; the goal on the other hand is to realize a circuit that can be functional in both environments, so while discussing the power budget in 3.2.3 co-integration with the qubits will be assumed.

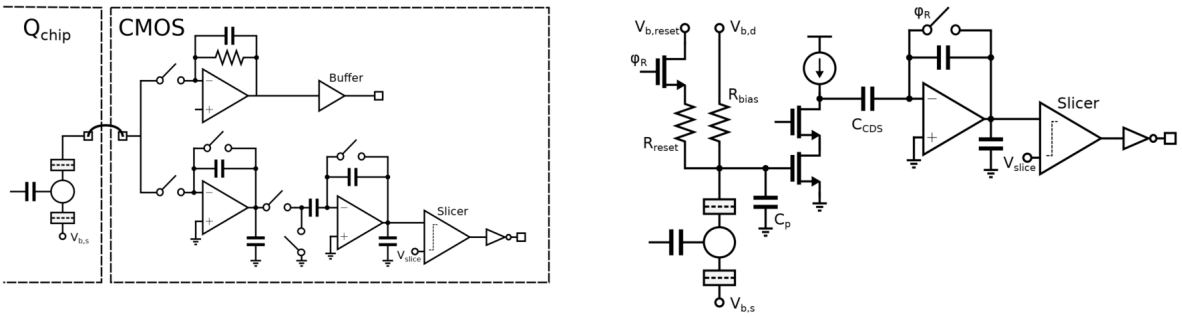


Figure 2.16: Proposed architectures for same-chip and dual-chip DC readout [38]. The same-chip solution shows more potential for large bandwidth and high frequency operation.

The current state-of-the-art DC readout still presents some limitations. Although a single-shot readout has already been performed using DC readout circuits, improvement on the readout time, reliability for continuous operation and fidelity is still needed to sustain the growing number of qubits in quantum processors. One of the best SNRs achieved up to now found in literature has been accomplished from Curry [43]. He achieves $SNR = 7.5$ with a readout time of $9\,\mu s$ using a HBT in voltage amplifier configuration. This result is very promising and it is one of the reason why it is worth examining in depth HBT-based DC readout.
The transimpedance amplifier realized in [45] effectively measures the diamonds of a quantum dot, but the SNR is not addressed. This TIA is realized in 28-nm FDSOI technology and it is used at $T = 4.2K$, achieving a bandwidth of $2.6\,\mathrm{kHz}$. This system can effectively measure the characteristics of QDs or SETs, but it is not reactive enough to sense tunneling events at high rate. Despite being low power ($1\,\mu\mathrm{W}$) it can achieve a high SNR of 60, but with a reading time of $10\,\mathrm{ms}$, too large for running QEC algorithms.
Another work worth mentioning was carried out by Fuketa and others [44]. Using a current comparator, this work claims a fidelity of 99.9% (equivalent to the target SNR) with a reading time above $10\,\mu s$. The power consumption is not mentioned in this work. This structure is very similar to a charge amplifier as it will be presented in the next chapter, although it is realized in CMOS.
The last work in terms of time and first in term of performance is the one carried out by Castriotta and others [47]. This work achieves compact integrated readout using an integrator (or charge amplifier as described in this work) in $1\,\mu s$ but with fidelity not reported and a power consumption of $1\,\mathrm{mW}$. This work has been also improved as this thesis project is already finished and this document is being written. The improved circuit [48] achieves readout in half the time with respect to the initial design, with just a bit too low fidelity of $99.86\,\%$. The interesting aspect of this work is the programmable comparator which does not need manual calibration for its threshold. The aim of this project is to propose a circuit that can improve on SNR (fidelity), reading time and power, in order to achieve a very reliable readout with an integrated and scalable solution, as discussed in section 3.2.

2.3 CMOS cryogenic operation

The effectiveness of CMOS technology to realize integrated circuit for the electrical interface of quantum processors at cryogenic temperature has already been proven [7] [8]. For this reason, it comes natural to think about the possibility of realizing the readout circuit in CMOS as well. In this section, the features of CMOS devices at cryogenic temperature is briefly explained and the main differences with the SiGe BiCMOS technology are discussed. Eventually, the choice to use the SiGe BiCMOS technology is motivated for the purpose of this work.
MOSFETs react to a decrease in the temperature with a shift in the $I - V$ characteristics. This is mostly a consequence of a modification in the electron mobility and threshold voltage, as measured in [49], [15] and [50]. The dependence of the threshold voltage respect to temperature is reported in figure 2.17. Positive side effects of operating at few K temperature include an increase in the Sub-threshold slope (SS), an increase in electron mobility and a low thermal noise.

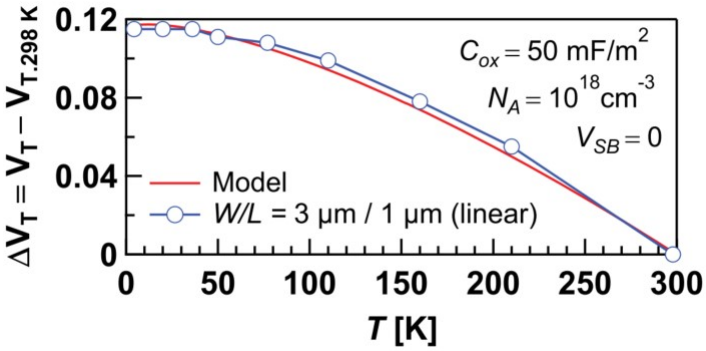


Figure 2.17: Threshold voltage variation as function of temperature in NMOS from [50]

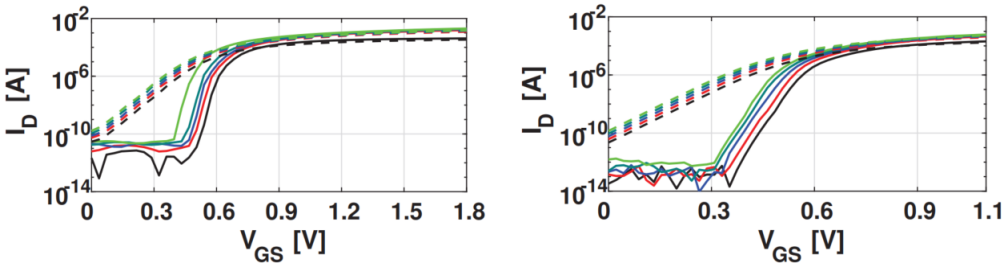


Figure 2.18: NMOS characteristics from [49]
Left: $W/L = 2.32/0.16\mu m$
Right: $W/L = 1.2/0.04\mu m$

However, also some negative effects like the kink-effect [49] can affect in a less predictable way the characteristics (even though this effect is not present in new technology nodes), due to the freeze-out and incomplete ionization of dopants in the bulk of devices.
The characteristics of NMOS is reported in figure 2.18 for comparison. As it was mentioned before, the main parameters to look at in this application are noise and power, due to the weak magnitude of the signal containing the information and the cooling power of the refrigerator in which the circuit is supposed to operate. Regarding the noise of CMOS devices, it has been demonstrated that at high frequency the channel noise of MOS transistors is dominated by shot noise, expressed as $2qI_DF$ [51]. The Noise suppression factor F shows values around 0.45 [51]. At CT, $F = 0.25$ fits better experimental data [52]. On the other hand, these transistors also display a huge low frequency noise contribution if compared to the HBT's flicker noise; this means that in order to decrease the flicker noise of an NMOS its size should be scaled up considerably, limiting the achievable bandwidth for the amplification of the signal coming from the SET. An alternative could be to use low-frequency noise cancellation techniques, but this is not always possible depending on the nature of the input signal. Even though the measurements are performed for higher current magnitudes with respect to what is used in this work, from [51] and [53] it can be seen that the minimum Noise Factor achievable for the two devices are comparable.
The feature that makes the SiGe HBT much more promising for readout with respect to MOSFETs is the transconductance efficiency (g_m/I). For bipolars in general and for HBTs in this case, the transconductance efficiency from [54] is

$$g_m/I_C = \frac{1}{U_T} \tag{2.3}$$

with U_T thermal voltage. This parameters scales with temperature (linearly for a certain range, it saturates below 70K), enhancing the efficiency of HBTs considerably at cryogenic temperatures [15]. In MOSFETs on the other hand, in the best case (weak inversion) the transconductance efficiency is

$$g_m/I_D = \frac{1}{nU_T} \tag{2.4}$$

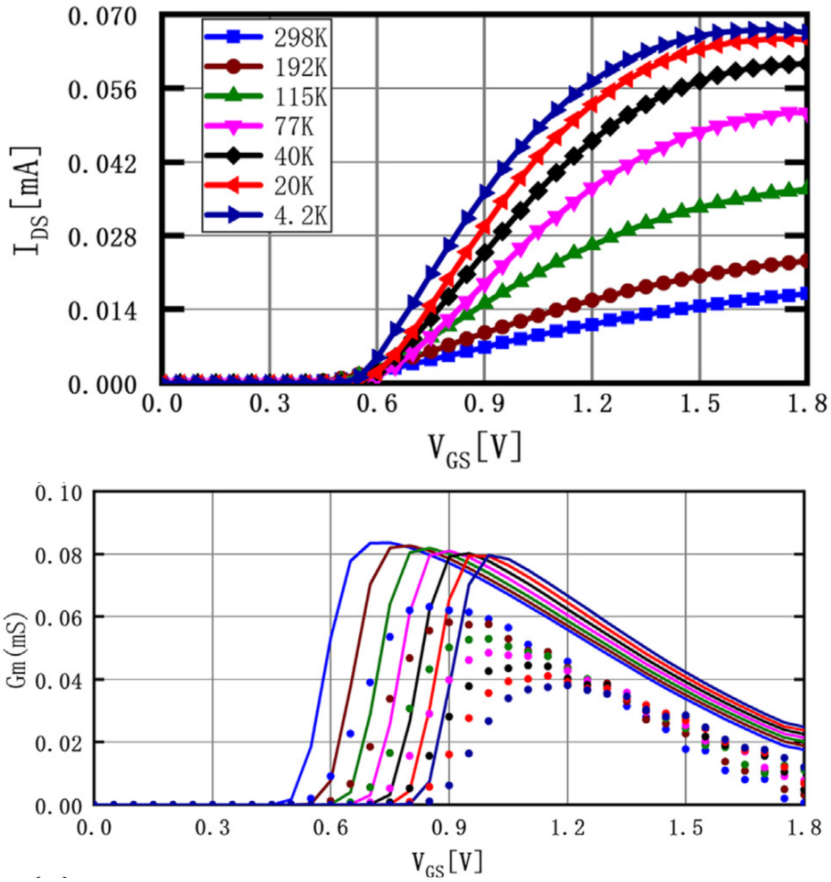


Figure 2.19: $I_{ds} - V_{gs}$ and $g_m - V_{gs}$ NMOS curves from [55]. Dashed lines indicate measured curves, while continuous lines indicate BSIM simulations. The transconductance follows the shift in the characteristics, but the peak show barely a $\approx \times 1.6$ increase from RT to LHT (Liquid Helium Temperature, 4.2K)

but in this case the factor n is equal to 1.5, resulting in an efficiency that is 67% of the Bipolars' efficiency [54]. Moreover, as visible in figure 2.19 the g_m of NMOS and PMOS at cryogenic temperature does not increase much from its RT value for same values of currents [55] [13]; the efficiency slightly increase at cryo, following the trend measured in [15] and in [56] and shown in figure 2.20 and table 2.21 Summarizing, due to their promising efficiency and noise features, the SiGe HBTs are believed to be suitable for the DC readout of spin qubits and have already been used for this purpose with encouraging results [43]. The purpose of this work is to push further those results to try and achieve a scalable DC readout of spin qubits making the best out of this technology.

2.4 SiGe HBTs for low noise cryogenic operation

To ensure the functionality of the readout circuit, first of all the information needs to be read with a certain fidelity that allows quantum error correction algorithms. For this reason, the choice of the technology takes into account primarily the noise behaviour and also of course the effectiveness of the transistors at cryogenic temperature.
This section goes through the technology of interest for this work, proven to have the potential for realizing an effective DC readout: the low noise SiGe HBT. Furthermore, the recent improvements in realizing semiconductor qubits in SiGe technology encourage the study of these devices to realize co-integrated circuits for interface with quantum processors. The characteristics of this device will be presented together with the more well-known and documented CMOS technology, to highlight their behaviour at cryo and their differences, and to motivate the choice of using SiGe HBT to perform amplification.

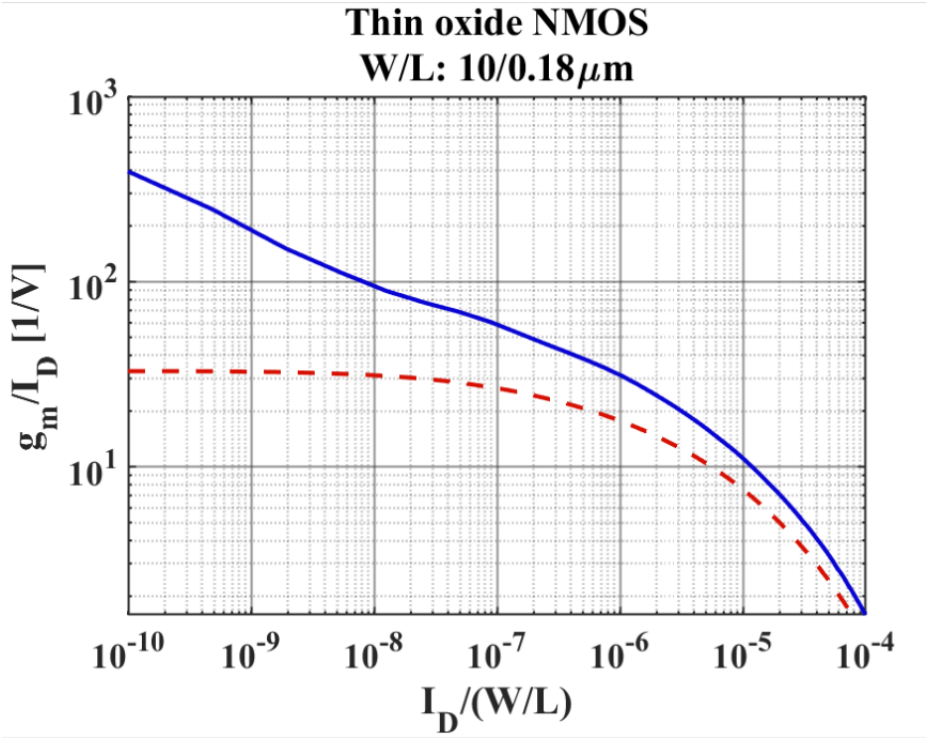


Figure 2.20: Transconductance efficiency of the NMOS in IHP SG13G2 process. Dashed lines represents RT behaviour, while continuous lines display CT behaviour

Technology		**0.16 μm**		**40 nm**	
Temperature		**4 K**	**300 K**	**4 K**	**300 K**
Device W/L	$[\mu m/\mu m]$	2.32 / 0.16		1.2 / 0.04	
V_T	[V]	0.55	0.40	0.50	0.38
SS	[mV/dec]	22.8	87.0	27.7	88.2
n	[-]	28.7	1.5	34.9	1.5
I_{on}	[A]	$2 \cdot 10^{-3}$	$1.5 \cdot 10^{-3}$	$6 \cdot 10^{-4}$	$5.3 \cdot 10^{-4}$
I_{off}†	[A]	$< 3 \cdot 10^{-11}$	$< 1.6 \cdot 10^{-10}$	$< 1.5 \cdot 10^{-12}$	$< 1.4 \cdot 10^{-10}$
I_{on}/I_{off}	[A/A]	$> 6.7 \cdot 10^{7}$	$> 9.4 \cdot 10^{6}$	$> 4.0 \cdot 10^{8}$	$> 3.8 \cdot 10^{6}$
Gate delay‡	[ps]	30.60	38.30	-	-
λ§	[V^{-1}]	3.3	0.6	4.0	1.3
		Weak Inversion			
g_m/I_D¶	[V^{-1}]	70	27	92	27
Intrinsic gain = $g_m/(\lambda I_D)$	[V/V]	21.2	45.0	23.0	20.8
		Strong Inversion (at $V_{ov} = 0.2$ V)			
g_m/I_D	[V^{-1}]	6	9	9	10
Intrinsic gain = $g_m/(\lambda I_D)$	[V/V]	1.8	15.0	2.2	7.7

Figure 2.21: Comparison between RT and CT operation for two CMOS nodes from [56]. What is shown is that the maximum transconductance efficiency increases approximately by 3 in CMOS

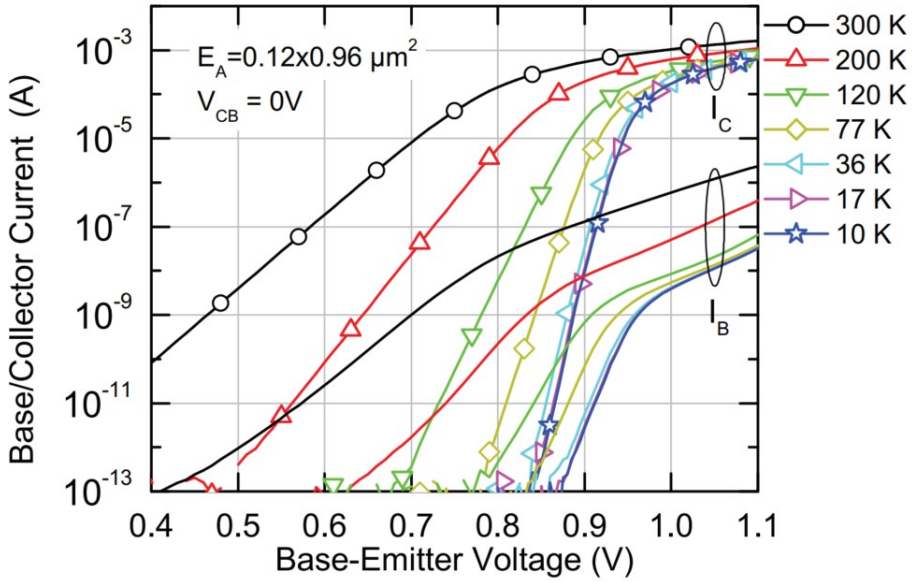


Figure 2.22: Gummel characteristics of the SiGe HBT from [59]

2.4.1 Device characteristics

The functionality of Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBTs) has been proven (contrarily to Si BJTs) at temperatures as low as $70mK$ [57] in the presence of strong magnetic fields; this is proof that HBTs are suitable for readout, in that spin qubits are operated in magnetic fields at cryogenic temperatures.
The process utilised in this work is the SG2G13 of IHP, because it can provide low noise and high efficiency operation at CT, as it will be discussed in this section. IHP provides the characteristics of the transistor shown in figure 2.22; the characteristics was also measured in independent research in [15] and [58]. The results of these measurements and simulations agree with the behaviour and characteristics of the SiGe HBT reported here.
It appears clearly that the temperature widely affects the $I-V$ characteristics, in that there is a substantial shift in the bias voltage required to obtain the same amount of current at RT and CT. Not limited to this, also the slope of the current is very different, becoming steeper the lower the temperature is. This feature is appreciated in the readout context, in that as it will be explained in chapter 3 a large g_m/I_C mitigates the input-referred noise of the transistor. The transconductance is plot against the collector current in 2.23 and against both collector current and base-emitter voltage in 2.25.

2.4.2 Small signal model

An accurate analysis of the pi-model of HBTs is depicted in [60], reported here in 2.26. For the scope of this project, there is no need to refer to this complex model when performing circuit calculations, in that some parameters can be neglected:

- The voltage variations in the contact resistances (all the resistances outside the intrinsic transistor) are negligible due to the low magnitude of the currents in the circuit.
- Given the relatively low operating frequency (which does not go near the transit frequency of the device of hundreds of GHz) most of the parasitic capacitances can be neglected. Only C_{be} (or C_π) and C_{bc} (or C_μ) may affect the circuit if the amplification requires scaling up of the size of the HBT.

Eventually a more simplistic model will be used if needed for calculations, which is displayed in figure 2.27.

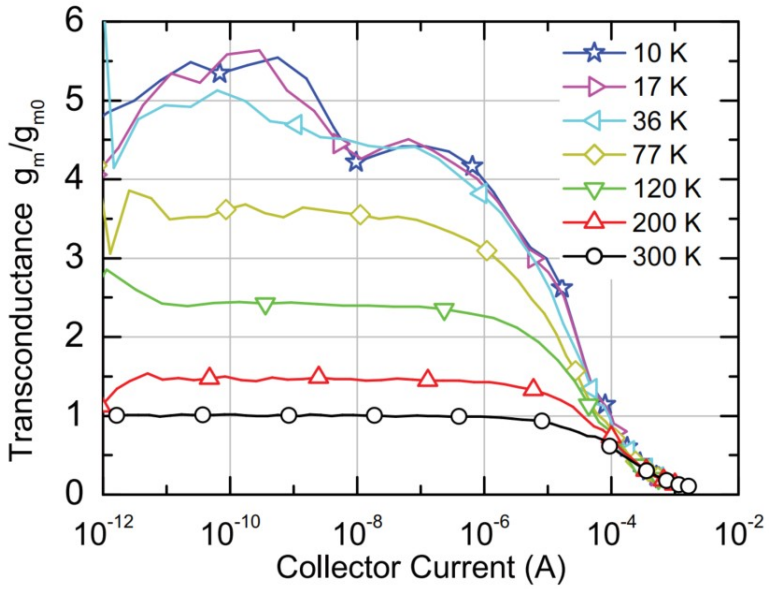


Figure 2.23: gm of the SiGe HBT for different temperatures from [59]. $gm0$ is the transconductance value at RT

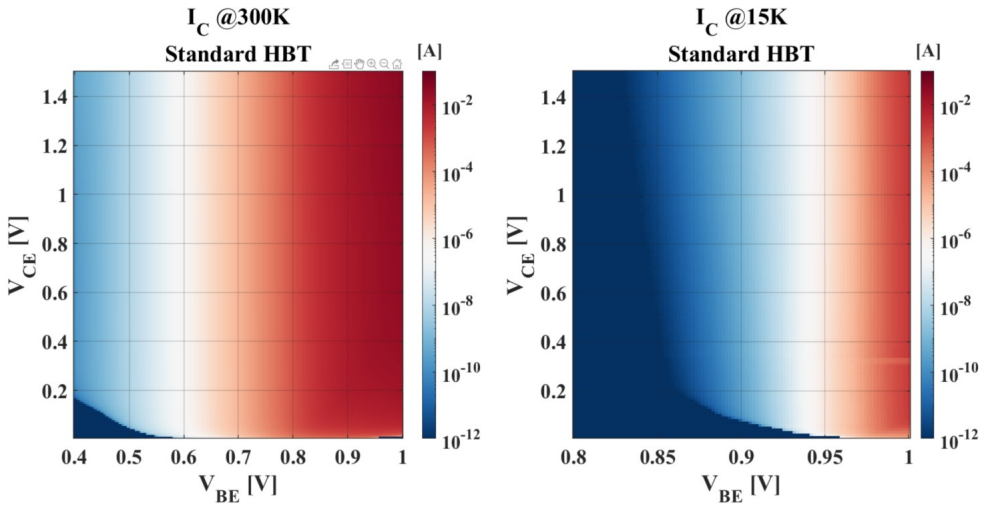


Figure 2.24: gm of the SiGe HBT for different temperatures from [15]

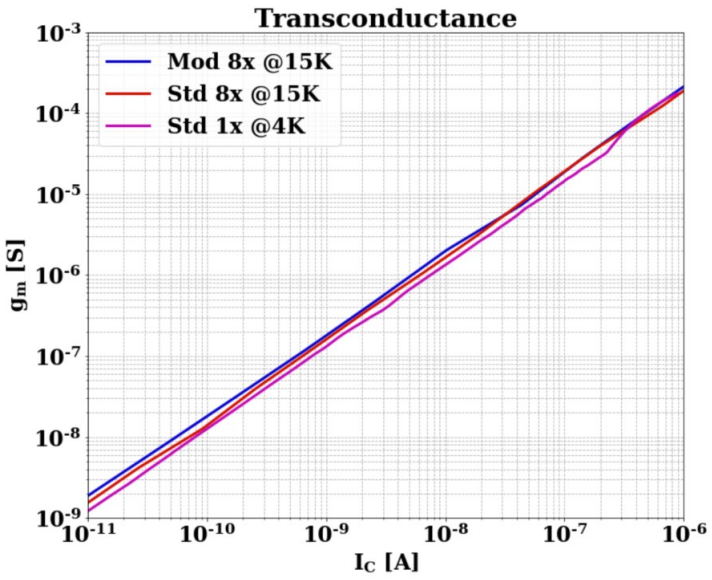


Figure 2.25: gm of the SiGe HBT for different temperatures from [15]

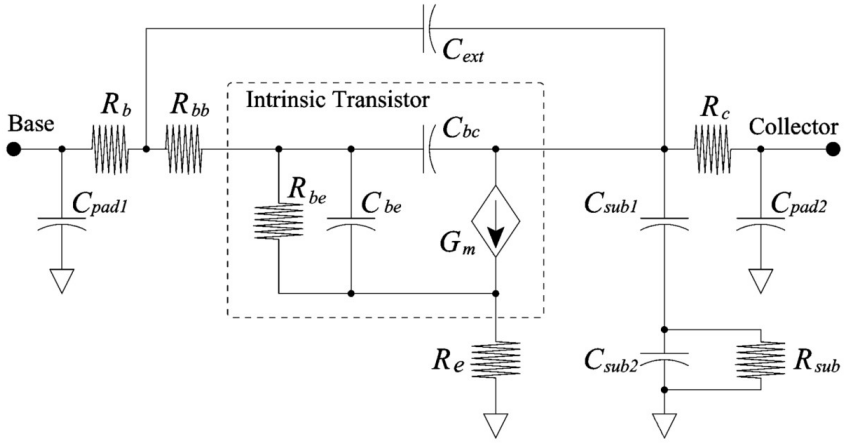


Figure 2.26: Complete small signal model for the SiGe HBT from [60]

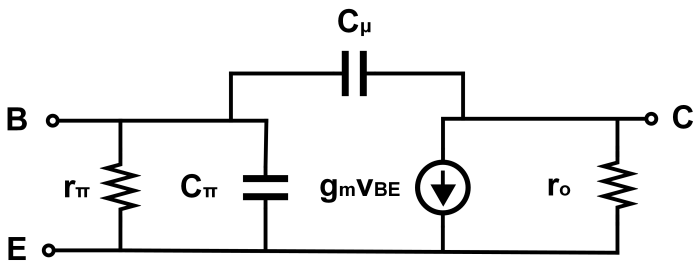


Figure 2.27: Simplified small signal model for the SiGe HBT

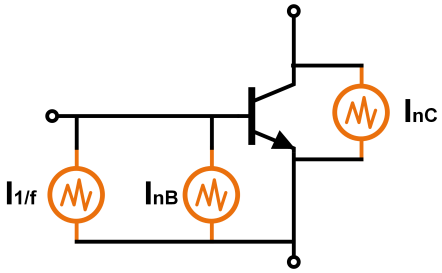


Figure 2.28: HBT noise sources representation in schematic

2.4.3 Device noise

As mentioned previously, noise is one of the main criteria for the choice of the technology to realize the frontend amplifier.An overview of the noise behaviour of the SiGe HBT is provided in [61] and [62].
The article presents the physics and modelling of white and low frequency noise sources, namely Shot Noise and $1/f$ noise. The former is caused by two independent sources:

- Collector shot noise, expressed as $I_{n,c}^2 = 2qI_C$, which arises from random injection of electrons into the base.
- Base shot noise, expressed as $I_{n,b}^2 = 2qI_B$, which arises from random injection of holes into the emitter.

The latter, also called "flicker noise", is believed to be caused by charge traps at the surface of p-n junctions [63]. This noise source is inversely proportional to frequency because the lower the current frequency the more likely charges are to get trapped in defects in the semiconductor. This noise sources can be expressed as noise current:

$$I_{1/f} = K_F \frac{I_B^\alpha}{f} \tag{2.5}$$

In this expression, K_F depends on the model and the size of the transistor and α is an experimental constant; for the SiGe HBT, it is usually $\alpha \simeq 2$ [61].
These noise sources are modelled as in figure 2.28 for practical circuit analysis.

2.4.4 Comparison: CMOS vs SiGe HBT

The choice of attempting to the design the front-end readout circuit using SiGe BiCMOS technology over CMOS is motivated in three main reasons:

- HBTs show larger transconductance efficiency, allowing for more amplification at very low power. Bipolars in CMOS have limited usability at temperatures below $70\,\mathrm{K}$ [64].
- HBTs show incredibly smaller flicker noise respect to MOSFETS
- SiGe technology shows promising results for the realization of quantum dots structures with long decoherence times. Realizing also interface integrated circuit in the same process allows for co-integration of qubits and electronics.

After the promising work by Curry [43] in realizing one-shot readout of spin qubits, the aim of this work is to continue exploring the potential of SiGe HBT devices for low noise and low frequency readout.

2.4.5 Resistors at cryogenic temperature

Resistances are heavily affected by temperature. For this reason, when drawing the layout of a circuit, adjustments need to be made to the resistance values used in simulation.
Ragnarsson measures some samples of resistances in his work [15] for the technology of interest, and the results are shown in figure 2.29. It follows from these measurements that an increase in resistance is expected at CT respect to RT.

Sheet resistance	**Uncilisided P+Poly (Rppd)**		
W/L [μm]	PDK $\Omega/sq.$	300K $\Omega/sq.$	4K $\Omega/sq.$
0.5/1	330	584	617
1/2	295	311	314
1/8	269	272	265
4/8	269	213	219

Sheet resistance	**Unsilicided N+Poly (Rhigh)**		
W/L [μm]	PDK $\Omega/sq.$	300K $\Omega/sq.$	4K $\Omega/sq.$
0.5/1	1.64 k	NA	NA
1/2	1.49 k	1.30 k	2.23 k
1/8	1.44 k	1.44 k	2.76 k
4/8	1.39 k	1.41 k	2.65 k

Sheet resistance	**Silicided N+Poly (Rsil)**		
W/L [μm]	PDK $\Omega/sq.$	300K $\Omega/sq.$	4K $\Omega/sq.$
0.5/1	15.78	74.65	75.45
1/2	11.39	17.32	5.14
1/8	8.01	8.87	1.40
4/8	8.10	12.55	1.85

Figure 2.29: Measured sheet resistance for three different types of resistors: R_{ppd}, R_{high}, R_{sil} from [15]

2.4.6 PDK IHP SG13G2 devices simulations

In this section, HBT, NMOS and PMOS transconductance efficiency and transit frequency are simulated for the pdk SG13G2 from IHP against bias current at $T_{sim} = -40\,^{\circ}\mathrm{C}$, the minimum temperature available for simulation. These data will be useful for hand calculations and qualitative considerations in chapter 3.

Figures 2.30 and 2.31 show the I-V curves of a SG13G2L NPN (used for amplification purpose in the circuit) and of a PMOS (used as active load or in current mirrors). The NPN is simulated at minimum size, while the PMOS needs a larger area due to its inherent large flicker noise.

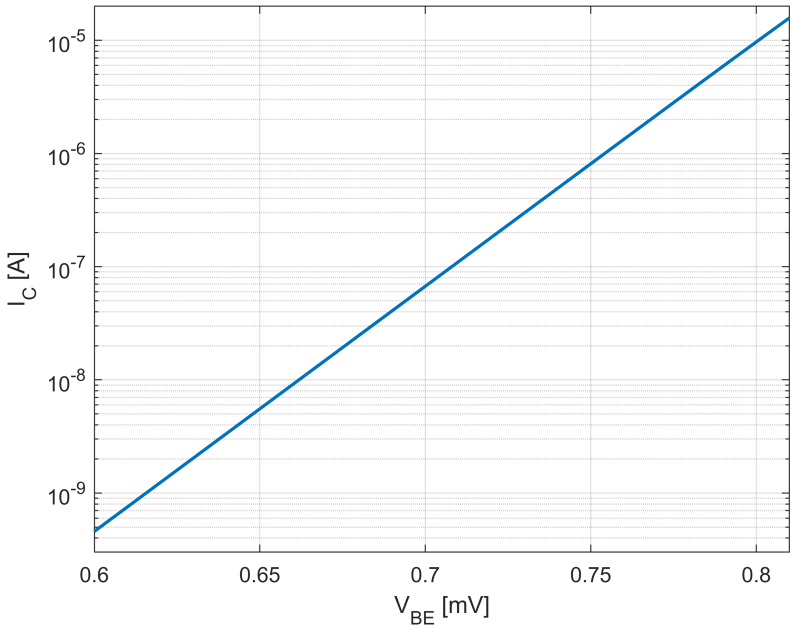


Figure 2.30: Simulated I-V characteristics of NPN model SG13G2L at T_{sim}, minimum size $E_A = 1 \times 0.07\,\mu$m, $V_{CE} = 200\,$mV

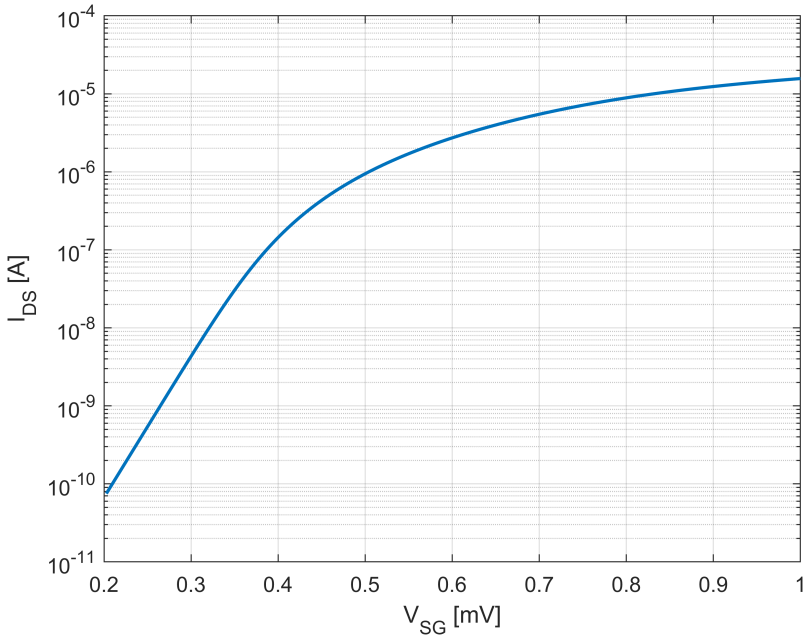


Figure 2.31: Simulated I-V characteristics of PMOS at T_{sim}, $W = L = 5\,\mu$m, $V_{DS} = 300\,$mV

The transconductance efficiency did not display dependency on W/L for MOSFETs and on EA (Emitter area) for the HBT. In the same way, very little variability was observed against V_{DS} and V_{CE} when these values are larger than the minimum $V_{DS} = 300\,$mV (minimum for saturation region) and the minimum $V_{CE} = 200\,$mV (minimum for forward active region). The sizes for the transistors are:

- $(W/L)_{PMOS} = (W/L)_{NMOS} = 1\,\mu$m$/1\,\mu$m
- $E_L/E_W = 1\,\mu$m$/0.07\,\mu$m

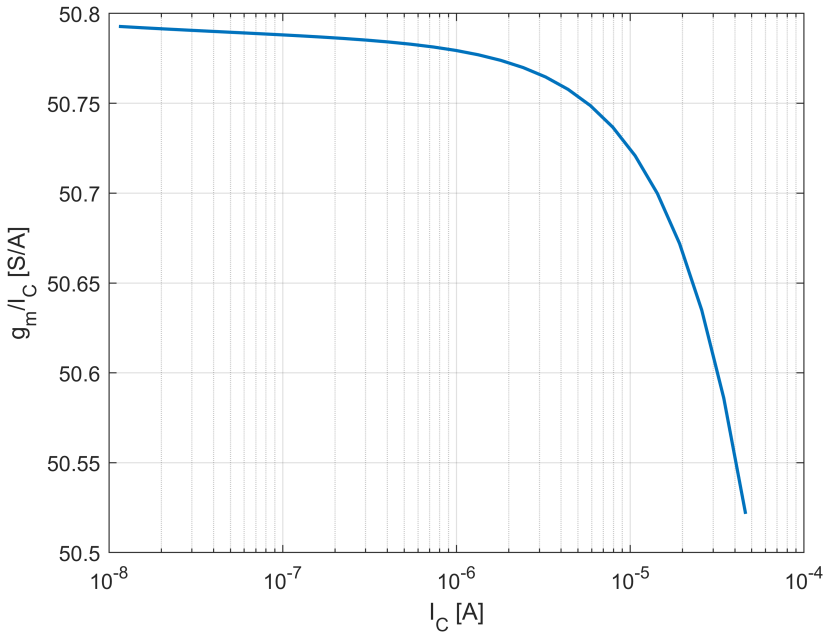


Figure 2.32: Transconductance efficiency of the HBT vs Collector current. The efficiency is constant for all bias points.

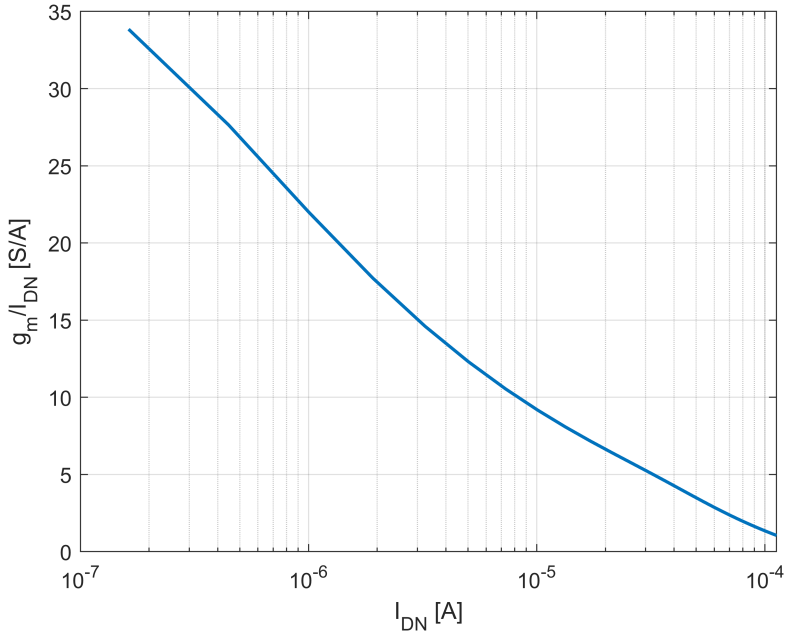


Figure 2.33: Transconductance efficiency of the NMOS vs drain-to-source current. The maximum efficiency is reached in the sub-threshold region

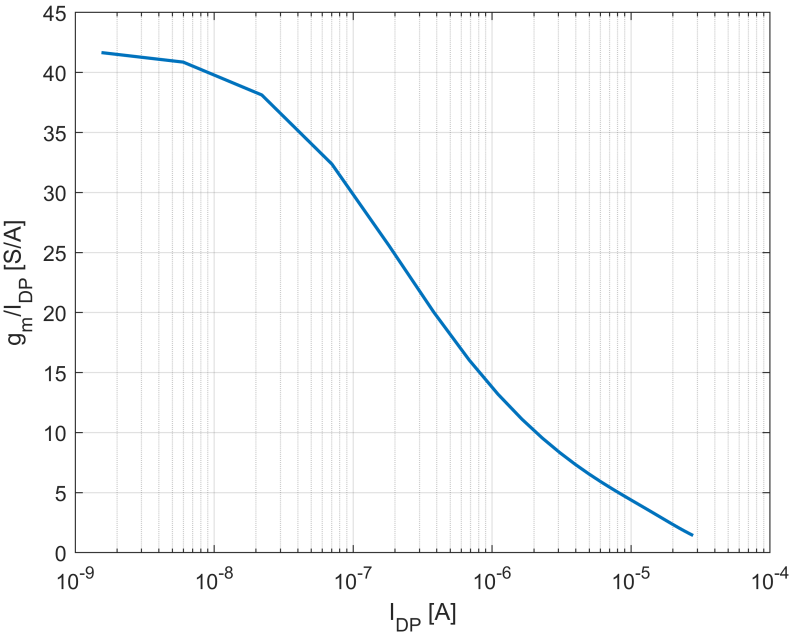


Figure 2.34: Transconductance efficiency of the PMOS vs drain-to-source current. The maximum efficiency is reached in the sub-threshold region

The f_t (transit frequency) plots are produced running AC analysis and calculating the $0dB$ crossing for the current gain (I_D/I_G and I_C/I_B) curves.

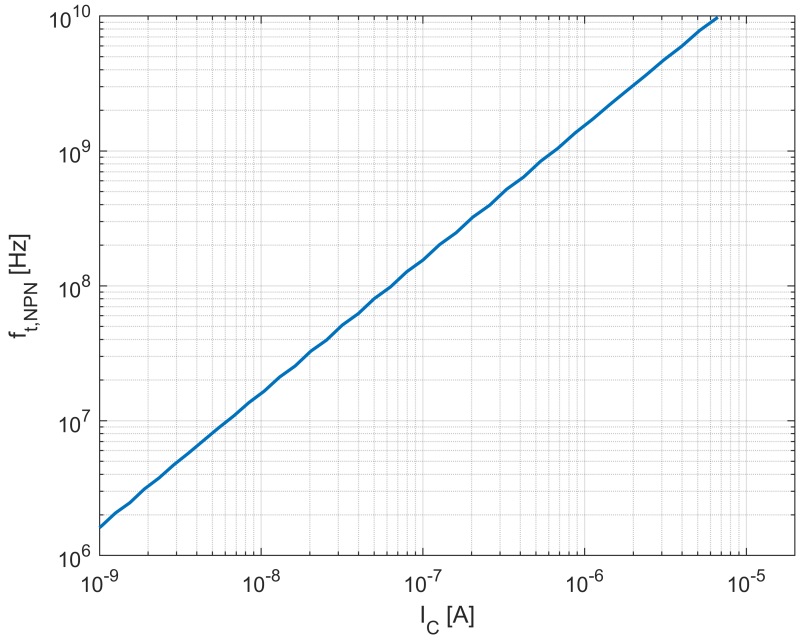


Figure 2.35: Transit frequency of NPN

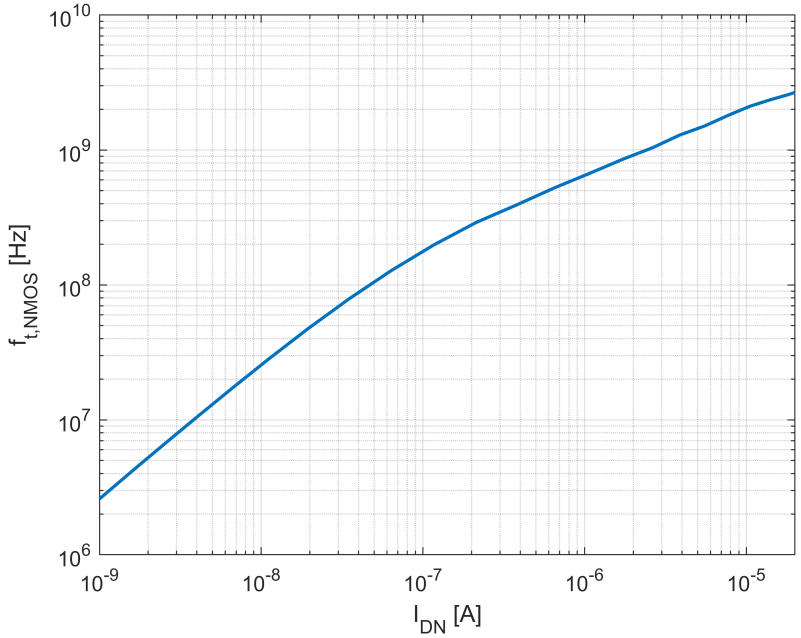


Figure 2.36: Transit frequency of NMOS

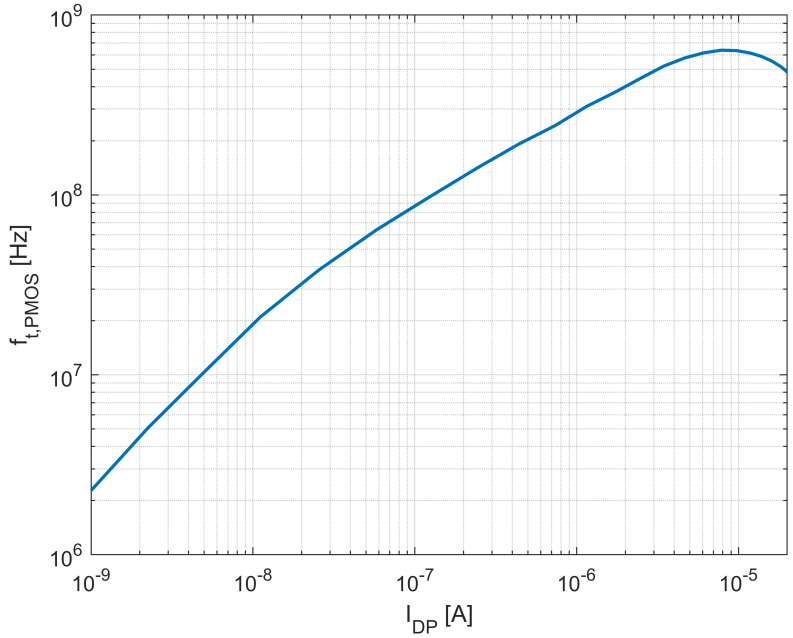


Figure 2.37: Transit frequency of PMOS

The plots in this section will be used as references for calculations in the next chapters, in order to run simulations in Cadence using the pdk SG13G2 from IHP.

In this chapter, the background knowledge on spin qubits architectures and readout has been presented. The technologies of interest for design have been compared and their main features have been shown. in the following chapter, the focus will move from the general readout process to the actual front-end circuit that is connected to the quantum dots and realizes the 1-bit ADC.

3

DC readout circuits

Having presented the background knowledge of Spin qubits readout, this chapter will dive into the set of specifications for a front-end circuit that should realize a DC readout. These specifications will be then used as metrics to compare possible architectures for the core of the readout circuit: the first amplification stage.

3.1 SET model for circuit design

As discussed previously, the SET is a strongly non-linear device. To be able to perform hand calculations, a simplified small signal (SS) model is often used, linearized around the operating point. However, it is also necessary to run simulation that include large signal behaviour of the SET; for this reason, a VerilogA model that mimics the characteristics of the SET with measured-curve-fitting method is introduced for Cadence simulations.
There is a large variability when it comes to the realization of SETs, due to their nano-scale nature. Furthermore, many different types of SETs have been realized in the past years using different techniques, as presented in 2.2.2. As a consequence, it is obvious that any model based on curve fitting fails if a different SET from the one used to derive the model is employed; however, it is very handy to have a reference to address the overall behaviour of the device and to observe what can be the interaction between this particular device and the rest of the circuit.
In the case of this work, the reference SET is one measured in Vandersypen Lab in Delft University of Technology by Oriol Pietx, as done in [38]. The device presents a characteristics that highlights the behaviour explained in 2.2.2 and it displayed in figure 3.1.

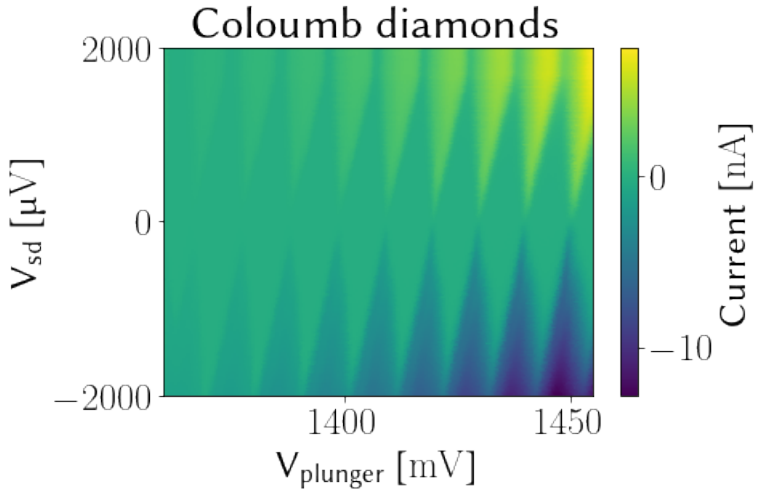


Figure 3.1: Measured characteristic of a SET

Analytical models have already been proposed for hybrid MOS-SET co-design [36] [37], but here another simpler approach is used. As proposed in [38], the curve of an SET can be expressed as the sum of hyperbolic tangent functions that recreate the rhomboidal regions. The final expression for the mathematical model, with some modifications becomes:

$$I_{SET} = \sum_{k=1}^{\#diamonds} V_{ps}^{x} \times i_{step} \Big[\frac{1}{\pi} \tanh \frac{ld \times V_{ds}(1+cd) - lp \times V_{ps} + 2k \times V_{charge}}{pw} + \frac{1}{\pi} \tanh \frac{ld \times V_{ds}(1-cd) + lp \times V_{ps} - 2k \times V_{charge}}{pw} \Big] \quad (3.1)$$

Even though the curve is not physics-based, there is an attempt in mapping the expressions' parameters into real characteristics of the device, such that the curves approximately overlap; apart from the voltages (representing the real voltages applied to the device), an example is the parameter cd, which describes the capacitive divider between plunger-drain and plunger-source capacitances (this makes the rhomboidal regions tilted). Other interesting parameters are:

- ld: represents the lever arm of the drain
- lp: represents the lever arm of the plunger gate
- Vcharge: represents the charging energy of the conductive island

Such expression results in the characteristics shown in figure 3.2

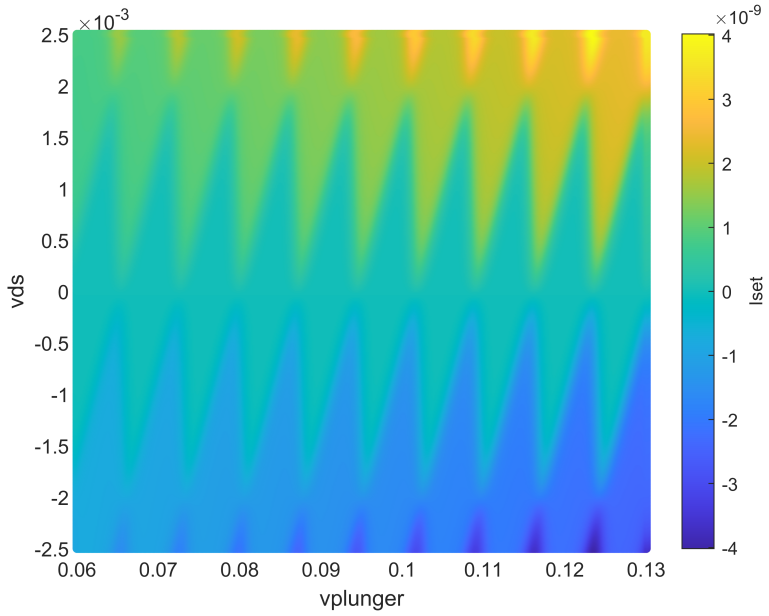


Figure 3.2: Plot of the SET verilogA model characteristics. The exact overlapping of simulated characteristics and measured curve is not guaranteed, because the exact data measured are not available. Only a fitting "by look" is possible, but it is enough in that the aim of this model is only to catch the overall behaviour of the SET. The verilogA block is excited in simulation with voltage sources such that the output signal is in the order of 300 pA, the typical value shown in table 3.4

3.1.1 Design flow for interfacing SET and frontend

The process followed for the design of the readout circuit can be visualized in figure 3.3. The characteristics of the SET available for measurements and/or the SET whom the readout circuit will have to work with should be known. Based on the characteristics, the desired operating point (OP) is identified in order to obtain the best sensitivity to input signals at the gate of the SET.

Parameter	Typical	Range
I_s	300 pA	100 pA to 500 pA
R_p	133 kΩ	30 kΩ to 1000 kΩ
C_p	2 pF	10 fF to 10 pF
F	1	0.5 to 1
$I_{LFN,f=1\,\mathrm{Hz}}$	-	10^{-23} A^2 Hz^{-1} to 10^{-24} A^2 Hz^{-1}

Figure 3.4: Typical values for SET small signal parameters from [38]. R_p is also referred to as R_{set} in this work. Noise parameters are assessed in the next section

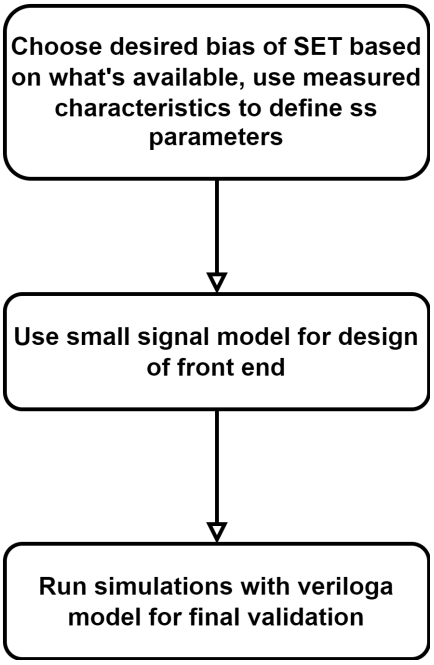


Figure 3.3: Overview of the design flow

At this point, the small signal model of the SET can be defined by linearizing the characteristics around the OP and plugged into the schematic. This method speeds up the design of the frontend circuit, since the biasing of SET and the first stage of the amplifier are codependent. In other words, tuning the bias of the amplifier would result in a shift of the bias point of the SET at each simulation run, which is not desirable to carry out a fair comparison of different amplification stages.
When a final choice has been made about the amplifier, the VerilogA model of the SET is finally used to draw a better picture of the circuit behaviour. At this final tuning stage, considerations can be done about how the swing at the drain of the SET can affect the operation of the system. Referring to the Verilog model of the SET presented in section 3.1, a bias point such that parameters of the small signal model are in the order of the "typical case" is chosen. As a consequence:

- the current step, namely the difference in current for the two possible outcomes $(0,1)$ is $I_S = 300pA$.
- the equivalent resistance from drain to source is $R_{set} = 133k\Omega$
- the input equivalent parasitic capacitance is $C_p = 2pF$. This element includes the output capacitance of the SET and all the interconnect parasitics for a two-chips solution.

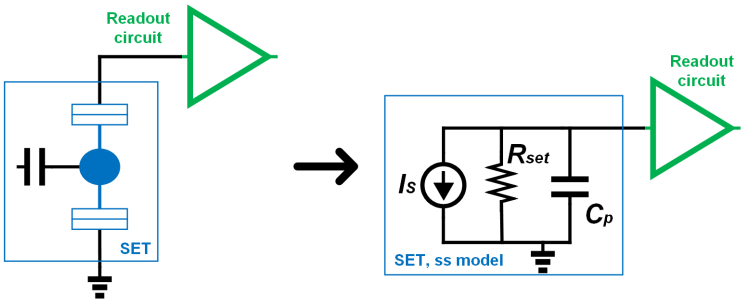


Figure 3.5: Small signal model of SET

3.1.2 Noise in Single Electron Transistors

As presented in [65] and measured in [66], the SET produces shot noise, which does not depend on temperature and behaves as white noise below $\approx 20\,\mathrm{GHz}$ [38]. This noise source introduces a fundamental limitation to the performance of the frontend, as it will be discussed in 3.2.2. The shot noise can be expressed as $I^2_{n,shot} = 2qFI_{set}$, where I_{set} is the drain to source current of the SET, q the elementary charge, and F the Fano factor, measured to be between 0.5 and 1 [65]. The shot noise is observed when the charging energy is larger than the thermal voltage, which is the case for this work.
In addition, SETs also show the presence of low-frequency noise [67]. This is referred as charge low-frequency noise, and it behaves similarly to flicker noise in conventional MOS transistors. A factor that comes into play for this noise source though, is the temperature dependency: in fact, a higher temperature corresponds to larger charge noise [68].
Overall, the expression of the noise for the SET (which does not include all the noise sources, but only the ones that are more relevant) is:

$$I_n^2 = 2qFI_{set} + K_1 \frac{I_{LFN,f=1Hz}}{f^\alpha} \tag{3.2}$$

Here, $\alpha \simeq 1$ is the noise slope, and the parameter $I_{LFN,f=1Hz}$ is typically measured at the maximum conductance point; it can be scaled (committing an approximation error) to other operating points with $I_{LFN,f=1Hz}(V) = I_{LFN,f=1Hz,max}\frac{g_m(V)}{g_{m,max}}$ [38].

3.2 Front-end specifications

This section enumerates what are the targets and specifications that the system should meet to implement effectively the desired functionality. In order to do so, firstly the exact nature of the inputs and outputs of the system are defined, and secondly the desired relation between inputs and outputs is translated into specifications.
The information of interest in the readout process is the quantum state of a target electron with two possible outcomes (spin up or down for simplicity, but also more complex quantum states can be used as shown in section 2.2.1). The result of the STCC appears at the input of the SET as a voltage pulse: the result is a current/voltage signal at its drain which is dependent on the spin. By employing a fine tuning of gates and tunnel junctions [69], it is possible to trigger (or not) a tunneling and start a "spin reading". In the PSB method, after triggering the tunneling, the reading can start immediately because the tunnel rate is so high that can be treated as deterministic. The resulting analog quantity is sampled at a certain moment and the outcome is compared to a threshold and converted in a digital value thanks to a 1-bit ADC (comparator). The threshold should be placed in such a way that if the input corresponds to a spin up, then the signal is larger than the threshold and if the input corresponds to a spin down the signal is lower than the threshold (or vice-versa). Due to the noise introduced by the comparator, the signal needs to be amplified before making the conversion, in order to avoid bit errors.
Assuming the information is contained in a current or a voltage as described in 2.2.1, the input signal in case of many consecutive readings can be modeled as a train of impulses coming from the Quantum Dots, as proposed in [38]:

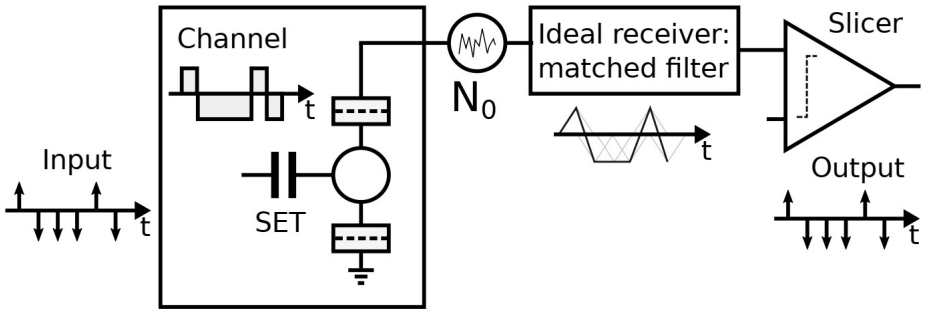


Figure 3.6: visual representation of the information being processed in the ideal readout chain, as presented in [38]

The series of impulses can be mathematically expressed as

$$I(t) = \sum_{i=0}^{\infty} b_i \delta(t - iT_b) \tag{3.3}$$

where b_i contains the information about the spin ($b_i \in \{0,1\}$) and T_b is the time between two readings (equivalently "bit time" or "symbol time" in this case). The sensor reacts to this signal producing a train of current pulses, described by an impulse response

$$s(t) = I_s\,(u(t) - u(t - T_b)) \tag{3.4}$$

where I_s is the distance in current between the two symbols $I_s = \left|I_{set,|0\rangle} - I_{set,|1\rangle}\right|$, also referred to as "current step".
If the flicker noise is neglected, then the white noise assumption is valid and the ideal receiver for this channel is the matched filter [70], whose impulse response is obtained as $h(t) = s(T_b - t)$. The final expression for the desired response after some manipulation is just

$$h(t) = I_s\,(u(T_b - t) - u(-t)) = I_s\,(u(t) - u(t - T_b)) \tag{3.5}$$

This matched filter's step response represents the one of an ideal integrator. Let's assume that there is no amplification of this signal, and the integration is performed by the current on a simple capacitor (C_p in this case), then the resulting voltage that is presented at the input of the comparator is:

$$V_{out}(T_n) = \int_{T_n}^{T_n + T_b} \frac{I_s}{C_p}\, dt = \frac{I_s T_b}{C_p} \tag{3.6}$$

Integration means by definition that the time constant of the node that it is being read is shorter than the reading duration:

$$\tau \geq R_{eq} C_{eq} \geq T_b \tag{3.7}$$

Here, C_{eq} and R_{eq} are the equivalent capacitance and resistance seen by the node on which the integration is happening (for the input node $\tau_i = (R_{set} // R_{in,amp}) C_p$). Since the signal is not settled at the sampling moment, if reset is not employed then every reading is function of the previous readings. Moreover, since the integrated current has the same polarity for the two symbols, eventually the voltage would saturates and hit the rails, instead of remaining around the threshold voltage as depicted in figure 3.7.
Resetting the input node carries also an unwanted side effect. During the reset time window, the quantum dot is ideally in preparation for the reading, meaning that its gates voltages are being set at specific levels for tunneling. As shown in figure 3.8 however, the parasitic capacitance between the drain and the gate of the SET can result in the reset signal leaking to the gates or barriers of the QDs ("kickback"). C_{GD} is usually very small for SETs (around aF [36]), although if the reset swing is large enough it could still affect the state of the qubits. The exact magnitude of the kickback that the QDs can sustain without losing fidelity is not clear from the literature and it is very dependent of the geometry of the dots. Therefore, the only guideline followed in this work will be to minimize the reset swing as much as possible.

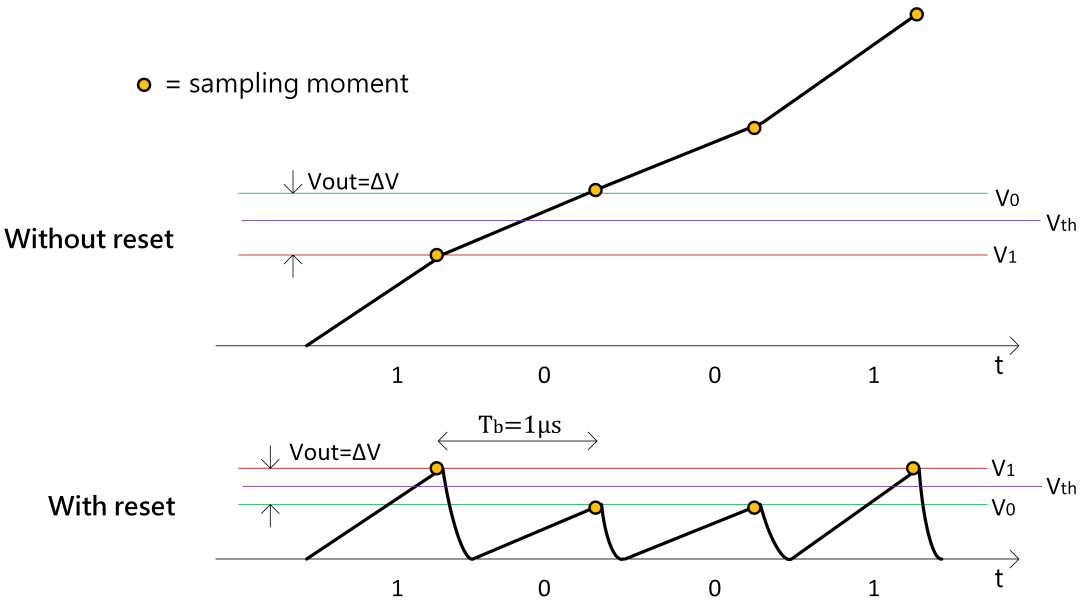


Figure 3.7: Waveforms for the integration of currents corresponding to 0 and 1 with and without reset. The signal is compared to the threshold at time instants (sampling moments) with fixed spacing of $\frac{1}{f_{symbol}}$

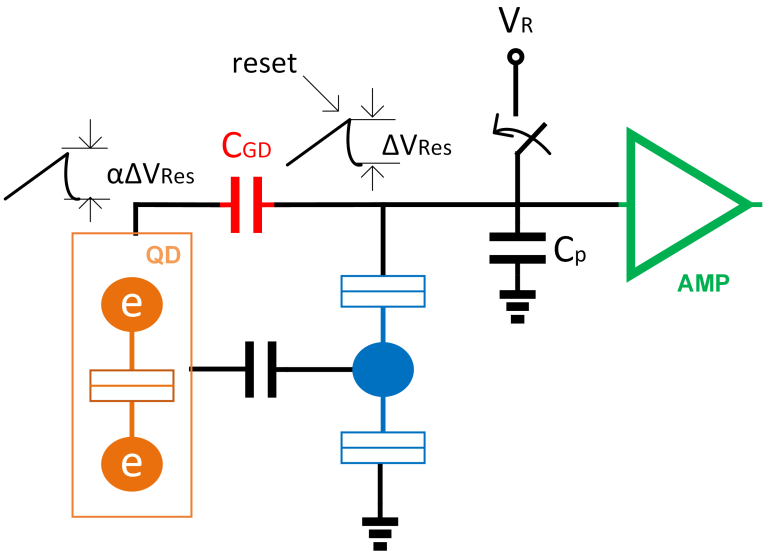


Figure 3.8: Schematic of integration at the output of the SET employing reset. The reset swing couples to the quantum dots with capacitive dividers that depends on the geometry of the QD-SET system

3.2.1 From BER to SNR requirement

For their results to be trustworthy, quantum computers require quantum error correction algorithms [71]. A common error threshold for error correction is $BER = 0.001$. In order to understand if the readout circuit is functional or not, the BER should be related to the Signal-to-Noise-Ratio (SNR), a quantity that can be defined and used in simulation of electrical circuits.
The two possible outcomes of a reading event are voltage noisy signals by definition, and their values can be described by Gaussian curves with mean μ_0 and μ_1 and same standard deviation $\sqrt{\sigma}$.

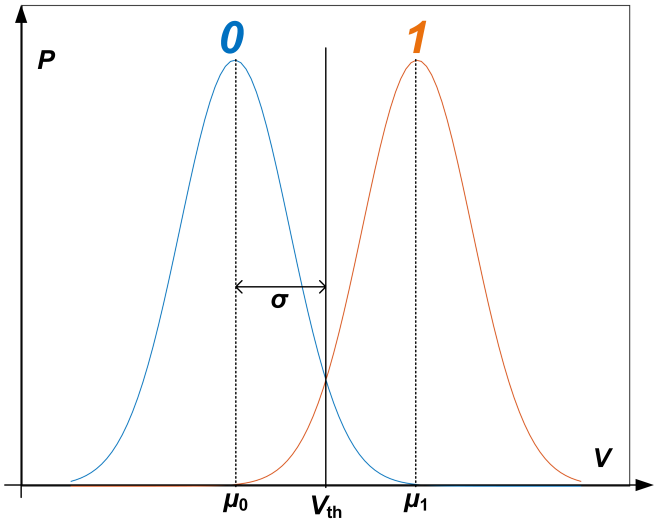


Figure 3.9: Representation of the two Gaussian curves, describing the two possible outcomes of the readout

The error in the decision corresponds to the area under the curve which exceeds the threshold and, if $V_{th} = \frac{\mu_0+\mu_1}{2}$, it can be calculated as:

$$P_{error} = \frac{1}{2} - \frac{1}{2} erf\left(\frac{\mu_1 - \mu_0}{\sqrt{2}\sigma}\right) \tag{3.8}$$

The power of the signal where the information is contained, on the other hand, is given by:

$$P_s = \frac{(\mu_0 - \mu_1)^2}{4} \tag{3.9}$$

which is the same for both symbols, assuming symmetry. Being the Q-function

$$Q(x) = \frac{1}{2} - \frac{1}{2} erf\left(\frac{x}{\sqrt{2}}\right) \tag{3.10}$$

and the signal to noise ratio

$$SNR = \frac{P_s}{\sigma} \tag{3.11}$$

then the BER is just

$$BER = Q(\sqrt{SNR}) \tag{3.12}$$

This curve is plot in figure 3.10 and it shows what is the correspondence between BER and SNR; to achieve the desired BER of 0.001, it must be $SNR > 9.5 = 9.8dB$. The target of $10\,\mathrm{dB}$ will be used in this work for practicality and to leave some margin for non-idealities in the readout chain.

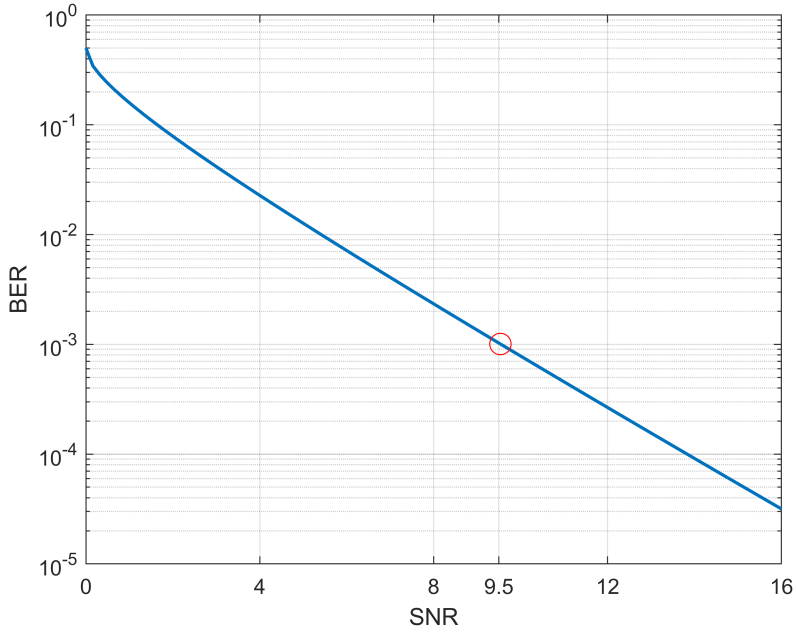


Figure 3.10: SNR required for the target BER

3.2.2 Fundamental shot noise limit

It is not possible to reach an arbitrarily high SNR for the readout, because the input SET poses a fundamental limit based on the noise it produces together with the signal. Referring to the signal assumed at the beginning of this section, the initial SNR budget can be calculated based on the SET characteristics. If a single-sided noise spectral density I_n^2 is assumed at the input of the chain, Sepke Todd and others [72] suggest that the variance of the voltage noise at the output can be calculated as:

$$V_n^2(T_b) = \frac{I_n^2}{2}\int_0^{+\infty}\left(\frac{|h(t)|}{C_p}\right)^2 dt = \frac{I_n^2}{2C_p^2}\int_0^{+\infty}|u(t)-u(t-T_b)|^2\,dt = \\ = \frac{I_n^2}{2C_p^2}\int_0^{T_b} dt = \frac{I_n^2 T_b}{2C_p^2} \tag{3.13}$$

The Signal-to-Noise-Ratio is by definition:

$$SNR = \frac{V_s^2}{V_n^2} = \frac{\frac{I_s^2 T_b^2}{C_p^2}}{\frac{I_n^2 T_b}{2C_p^2}} = \frac{2I_s^2 T_b}{I_n^2} \tag{3.14}$$

In this best case the noise is only produced by the set. If a '0' corresponds to $I_{<0>} = I_{s,bias} - I_s/2$ and a '1' corresponds to $I_{<1>} = I_{s,bias} + I_s/2$. If we assume I_s small compared to $I_{s,bias}$, then the SNR for the two symbols is approximately the same. In a scenario where $I_{s,bias} = I_s/2$, then the SET does not produce any noise for the symbol '0', and results in the worst-case SNR for the symbol '1'. The noise produced by the set for the more noisy symbol between 0 and 1 considering only SET shot noise is:

$$I_n^2 = 2q(I_{s,bias} + \frac{I_s}{2}) \tag{3.15}$$

Overall, the best SNR that can be reached with a noiseless frontend circuit:

$$SNR_{max} = \frac{I_s^2 T_b}{q\left(I_{s,bias} + \frac{1}{2}I_s\right)} \tag{3.16}$$

This expression is function of bias current and current step, two parameters that are correlated and depend on the SET model that is used and on the coupling between the SET and the QD.

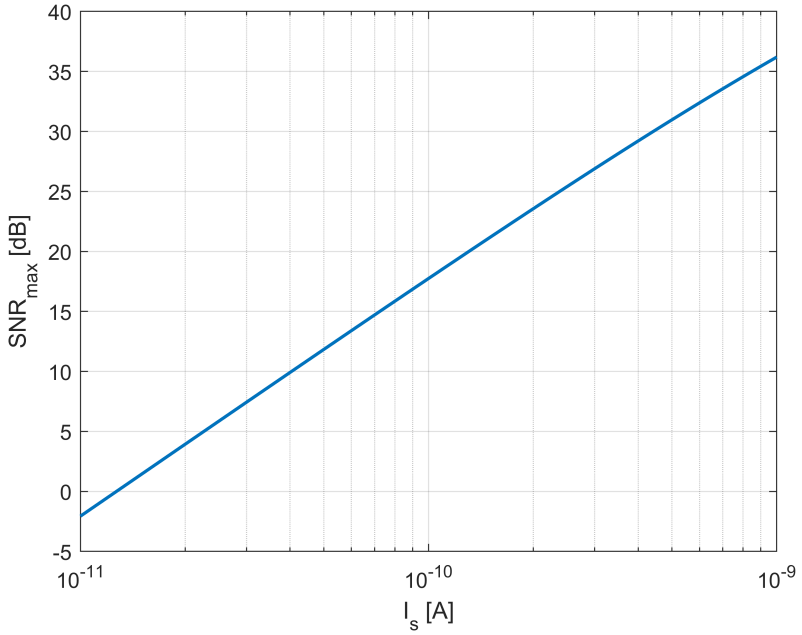


Figure 3.11: SNR initial budget vs SET current for $T_b = 1\,\mu$s and a bias current of 1 nA. Here the assumption is that with the same bias current the current step can increase due to a better coupling with the QD. If the different diamonds are available for biasing the SET, then the SNR scales differently and an optimum should be found for the OP($I_{s,bias}$,I_s)

More coupling means more current and a higher initial SNR. The maximum SNR as function of the input current is visible in figure 3.11
In this work, the set of value that is used for reference is

- $I_{s,bias} = 1nA$;
- $I_s = 300pA$;

With this assumption and the goal to read every $1\mu s$ (as it will be discussed in section 3.2.4), the theoretical SNR initial budget is $489 (= 27dB)$.
This is a fundamental limit on the SNR that assumes only SET shot noise and a noiseless frontend circuit. Not only the frontend will introduce noise in the circuit, but the first amplification stage is also expected to be the main noise contributor. If the noise contribution of the front-end circuit is added to I_n^2 in equation 3.14, an approximation of the noise budget for the amplifier can be calculated as:

$$I_S^2 = (300\,\mathrm{p}A)^2 = SNR_{max} \times I_n^2 = SNR_{target} \times \left(I_n^2 + I_{n,amp}^2\right) \tag{3.17}$$

where $SNR_{target} = 10\,\mathrm{dB}$ and the noise sources are all referred to the drain of the set/input of the readout circuit. This expression is equivalent to

$$I_{n,in,amp}^2 = I_{n,set}^2 \left(\frac{SNR_{max} - 1}{10}\right) = 48.8 \times I_{n,set}^2 \tag{3.18}$$

In the previous expression, the noise of the amplifier is assumed to be white noise with a flat spectrum. This result shows that if the amplifier's power spectral density (PSD) is more than 49 times the noise of the SET, then the SNR requirement is not satisfied. Looking at the same equation from another angle, a first order approximation for the actual SNR of the readout based on the input referred noise of the amplifier can be written as

$$SNR = SNR_{max} \frac{I_{n,set}^2}{I_{n,set}^2 + I_{n,amp}^2} = SNR_{max} \frac{1}{1 + \frac{I_{n,amp}^2}{I_{n,set}^2}} \tag{3.19}$$

This calculation gives an idea about the noise that the amplifier is allowed to produce, based on the "starting point" SNR that the specific SET used provides; it is an optimistic estimation, meaning that in presence of other (non-white) noise sources, some headroom on the noise budget is

still required. This assumption allows for a fair comparison between the proposed architectures in section 3.3, where the ratio $\frac{I^2_{n,amp}}{I^2_{n,set}}$ will be used as metric for evaluation of each amplifier configuration. The lower this ratio, the better the noise performance.

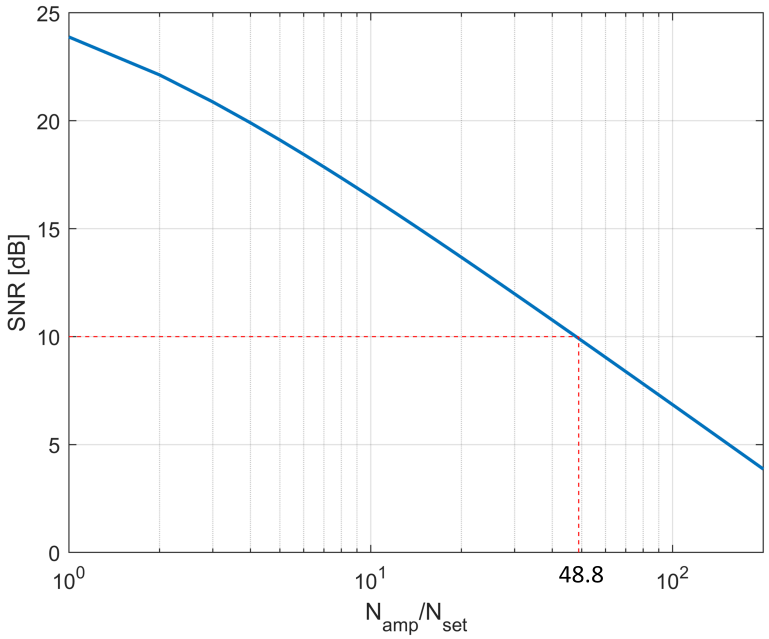


Figure 3.12: SNR vs $\frac{I^2_{n,amp}}{I^2_{n,set}}$ for an input current of $I_s = 300\,\text{pA}$ and a reading time of $T_b = 1\,\mu\text{s}$

3.2.3 Power budget

Recently, more and more effort is being spent in trying to operate spin qubits at relatively high temperature [73]. However, at the current state, most of these kind of systems are operated between $100 - 300mK$ [7]. The fridge in which the qubits and also the readout circuit operate has limited cooling power. For it to be able to maintain a stable temperature, the circuitry inside of it cannot burn more than $1mW$ at $100mK$. Assuming this as the worst case, the entire system including control electronics, readout electronics and qubits must stay within this power budget. Moreover, the main goal of DC readout and more in general of integrating electronics with qubits is the potential for scalability: the power budget for each block of the system shrinks proportionally to the number of qubits, and the 'dream goal' sits at thousands, if not millions, physical qubits.
For this work, the goal is therefore in general to minimize the power consumption, targeting $10\mu W$ for the frontend readout circuit.

3.2.4 Bandwidth requirement

Future complex quantum processors will need to process a high number of readings in short time in order to avoid decoherence of qubits [74]. Even though recent improvements on semiconductor spin technologies extended the maximum decoherence times [75] [22], the readout only consists of one step part of a more complex QEC which consists of many operations [76]. Moreover, given the huge number of physical qubits required to perform QEC algorithms (in the order of 1×10^8), introducing the possibility for time or frequency multiplexing is desirable so that not every physical qubit requires its specific readout circuit. These premises highlight that the frequency at which the readout circuit can operate should be maximized, thus this will be one of the goals of this work.
At the current state, DC readout has been successfully accomplished at a maximum frequency of about $\simeq 130kHz$ with $SNR > 7$ [43], while RF readout can already achieve one order of magnitude lower reading times, but with less scalability potential due to the size of matching networks. This being said, this project will attempt to achieve a functional ($SNR > 10$) single-shot DC read-

out operation in $1\,\mu s$, showing the capability to operate at a frequency of $1\,MSa/s$.

3.2.5 Specifications summary

Metric	Target	Functionality
BER	$\leq 1 \times 10^{-3}$	1×10^{-3}
SNR	$\geq 10\,dB$	$9.8\,dB$
T_b	$1\,\mu s$	depends on qubits lifetime
Power	$\leq 10\,\mu W$	$1\,mV$
Reset swing	$\leq 1\,mV$	depends on coupling capacitances

Table 3.1: Summary of specifications and comparison metrics for front-end evaluation. The functionality column specify what is the minimum value of the metric for functionality, while the target column includes the value that is targeted in this work

3.3 Front-end architectures

Having fixed what the expectation are for the frontend circuit, the architecture has to be established. How to perform amplification of the signal such that it can be translated into digital information and at the same time keep the noise below the target? Since also the bandwidth and power come into play, it is necessary to compare the alternatives in order to make a decision. The SET reacts to the charge at its gate by changing its conductance; the current and the voltage at its nodes are directly affected by this change in channel conductance, therefore these can be used equivalently for the readout process. The architectures that can amplify this type of information are shown in :

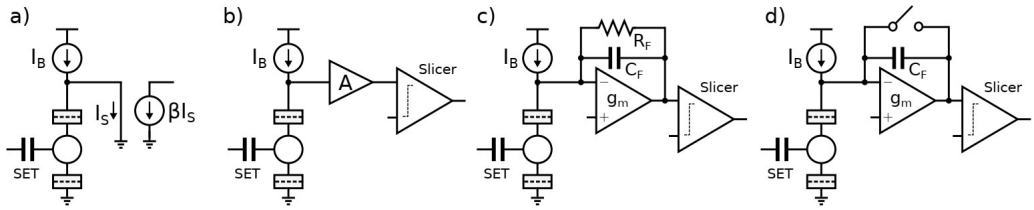


Figure 3.13: Possible architecture solutions from [38]

- a) Current amplifier: amplifies the current signal, regardless of what happens to the drain voltage of the SET. The available gain for this configuration is low (depends on ratio of transistors' areas), hence this is also referred to as 'pre-amplifier' for the need of a second stage.
- b) Voltage amplifier: due to the finite input impedance, a change in current results in a drain voltage signal for the SET. This is sensed and amplified.
- c) Transimpedance amplifier: the current signal is amplified and translated into a voltage through the feedback resistor R_F.
- d) Charge amplifier: the input current is integrated in the feedback capacitor, causing a voltage signal at the output node. This is can be seen as the high-frequency limit of the TIA solution.

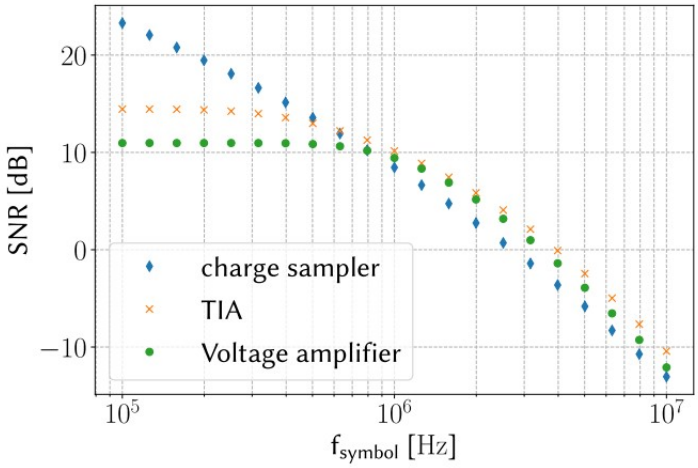


Figure 3.14: Comparison of possible architecture solutions (ideal circuits simulations from [38])

Simulations of ideal schematics and a mathematical analysis of these architectures are unfolded in [38]: from this comparison it is still unclear which solution is the best for the desired frequency of operation, as it is seen in figure 3.14. Since a purely mathematical analysis cannot exactly tell which solution is the best for the trade-off bw-power-noise, in this section of the work the four architectures are simulated to specifically address their potential for the technology of interest, SG13G2 from IHP. Using real components in simulation, including reset and actual bias voltages and currents can help in making a decision that takes into account the environment in which those amplifiers work.

The metrics that will be addressed are in first place related to the functionality (SNR, noise, output swing) and in second place to the potential for scalability (area, power, bandwidth). Only the architecture yielding the most promising results will be then designed in depth, including other real blocks of the system and performing noise periodic noise analysis including the effect of sampling.

3.3.1 Simulations setup

In the following analysis, an input parasitic capacitance of value

$$C_p = 2\,\mathrm{pF} \tag{3.20}$$

is included in simulation because a two-chip solution is assumed [15] [38]. This choice is motivated from the fact that if the same circuit is used in a same-chip solution, the performance can only improve; it is then preferred to design for the worst case.
The simulations are performed in the Cadence Virtuoso environment using Spectre and SpectreRF simulators at the minimum simulating temperature available of

$$T_{sim} = -40\,^{\circ}\mathrm{C} \tag{3.21}$$

unless differently specified.
In order to include the expected noise sources at CT, thermal noise is manually excluded in simulations, in that it is expected to be negligible. For completeness, current noise sources are added manually in parallel with resistive devices with noise magnitude of

$$I_{n,R}^2 = 4k_B T/R \tag{3.22}$$

where $T = 4K$.
Furthermore, since channel shot noise is not already accounted for in the noise model of PMOS and NMOS transistor, it is added manually using a current source in parallel with their channel, with magnitude

$$I_{n,ch}^2 = 2qFI_{DS} \tag{3.23}$$

assuming the worst case $F = 1$.
The supply used in simulation is $V_{DD} = 1.2V$ (nominal supply of the process), unless mentioned otherwise. For some configurations it will be indeed possible to lower the supply to save power.

3.3.2 Current pre-amplifier

A primitive implementation of a current amplifier is shown in figure 3.15. The circuit is a canonical current mirror, and the amplification resides in the ratio of the W/L of the two PMOS; assuming low input resistance of the amplifier ($R_{i,amp} << R_{set}, R_b$), the gain is just

$$\frac{I_{out}}{I_S} = M = \frac{W_{p2}/L_{p2}}{W_{p1}/L_{p1}} \tag{3.24}$$

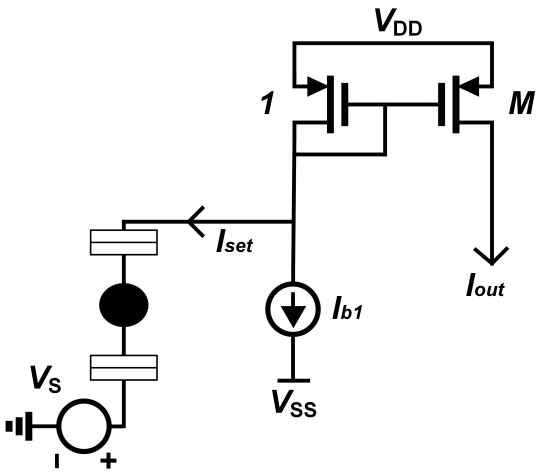


Figure 3.15: Current pre-amplifier

The best feature of the current pre-amplifier is the "safety" for the operation of QDs and SET: on one hand, any kickback from the amplifier is attenuated by the gain M and on the other hand input reset can be avoided. Resetting a node is only required if integration is happening at that node, or in other words if the node's time constant is not fast enough that the voltage can settle before the next reading ($\tau = R_{eq}C_{eq} \geq T_b$). In the case of the CA, low input resistance allows to avoid this scenario. Integration is supposed to happen in the following stages if a CA is employed.
The input resistance of the current pre-amplifier should be kept low to favour the flow of the SET current into the amplifier; if the resistance of the amplifier is too large then current is simply lost in the resistive divider. Since the desired operating frequency is $f_{symbol} = 1\text{MHz}$ and the input capacitance is assumed to be $2pF$, then it must be

$$R_i = R_{i,amp} // R_{set} = \frac{1}{2\pi f_{p,i} C_p} \simeq 80k\Omega \tag{3.25}$$

If $R_{set} \simeq 133k\Omega$, then it must be $R_{i,amp} // 133k\Omega = 80k\Omega \longrightarrow R_{i,amp} \leq 200k\Omega$. The constraint about pole frequency is obviously extended to the other nodes of the circuit, namely the gate of the current mirror and the output node (unless integration is meant to happen at the output of the CA/input of the next stage). Regarding the gate of the mirror, the bandwidth poses a strict constraint on the size of the PMOS, resulting in a trade-off between BW, gain and flicker noise.
In an ideal current amplifier, the current should flow all into the input node; this does not happen if $R_{set} > R_{i,amp}$, in that a considerable share of the signal current will be lost in the SET. An additional condition is then derived on the input resistance, which makes the previous condition redundant. Assuming a loss of 20% of the signal is accepted, it should be

$$R_{i,amp} \leq 0.2 R_{set} \simeq 27k\Omega \tag{3.26}$$

resulting an equivalent gain of

$$\frac{I_{out}}{I_S} = M\frac{R_{set}//R_b}{R_{set}//R_b + R_{set}//R_b//R_{i,amp}} = M \times 0.8 \tag{3.27}$$

However, the main downside of this architecture is the channel shot noise of the transistors. The channel noise of the input PMOS appears directly input-referred, in that its current enters the same node of the SET drain, as visible in figure 3.16;

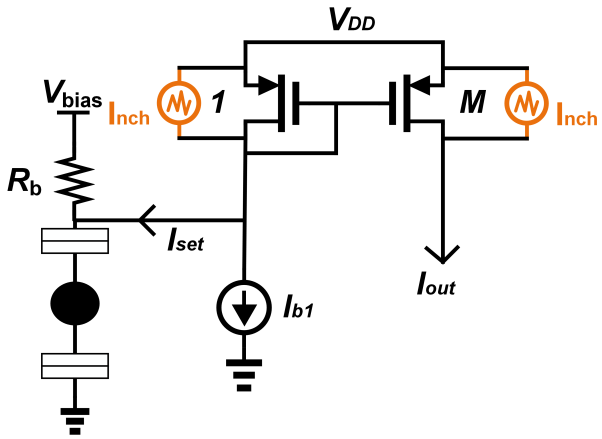


Figure 3.16: Shot noise in the channel of PMOS in the CA; for the input transistor, the shot noise enters the same node of the input current

it is recalled from section 3.2.2 that the input referred noise can be at most about 48 times the noise of the SET taken as reference. The input referred noise of the amplifier considering only shot noise is

$$I^2_{n,in,amp} = 2qI_{b1}\left(1+\frac{1}{M}\right)\left(\frac{R_b//R_{i,amp}}{R_b//R_{i,amp}//R_{set}}\right)^2 \tag{3.28}$$

With the condition that $I^2_{n,in,amp} \leq 49 \times I^2_{n,set}$, solving for I_{b1} is not trivial in that the input resistance is not a linear function of the bias current

$$R_{i,amp} = \frac{1}{g_{m,pMOS}} = \frac{1}{I_b1 \times (g_m/I_D)_{PMOS}(I_b1)} \tag{3.29}$$

The circuit is simulated in Cadence and the ratio between the input referred noise at 10 Hz (flicker and thermal noise are manually excluded in the simulation) of the amplifier and the SET shot noise is plot as function of the bias current in plot 3.17.

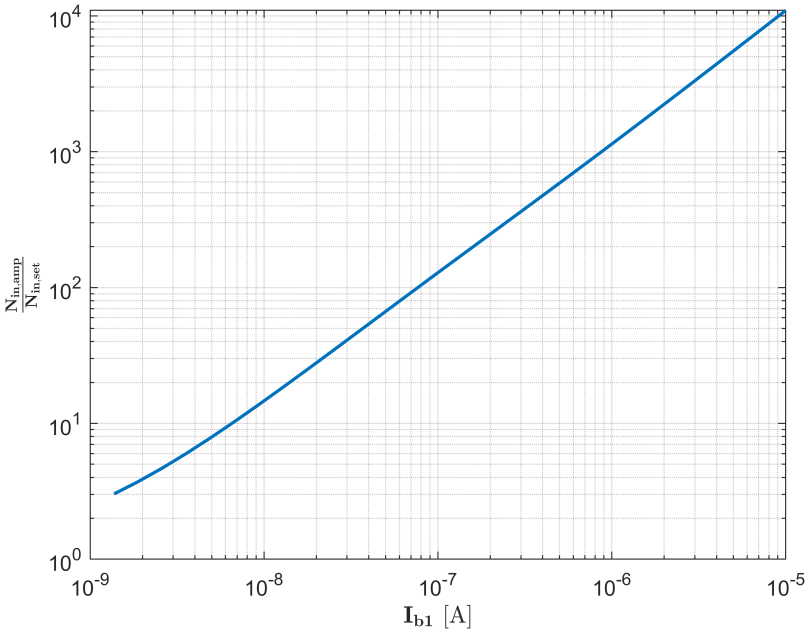


Figure 3.17: shot noise of amplifier compared to SET shot noise for different bias currents for the CA in figure 3.15

From the plot it can be seen that the circuit respects the desired condition for noise from 3.2.2 ($\frac{N_{amp}}{N_{set}} \leq 49$) only if $I_{b1} \leq 37nA$ for a gain of $M = 5$. Furthermore, in order to ensure the condition in equation 3.26 then it must be, for the input PMOS:

$$g_{m,PMOS} \geq 77\mu S \tag{3.30}$$

The gm efficiency of the pMOS from section 2.4.6 suggests a required bias current much larger than than $37\,\mathrm{nA}$ (about $5\,\mu\mathrm{A}$) at $-40\,^{\circ}\mathrm{C}$ to satisfy this condition; even considering the measured cryo-efficiency in 2.4, the noise produced is too high at the desired current level for low input resistance. The estimation is confirmed in Cadence: in figure 3.18 the input resistance of amplifier versus bias current is displayed.

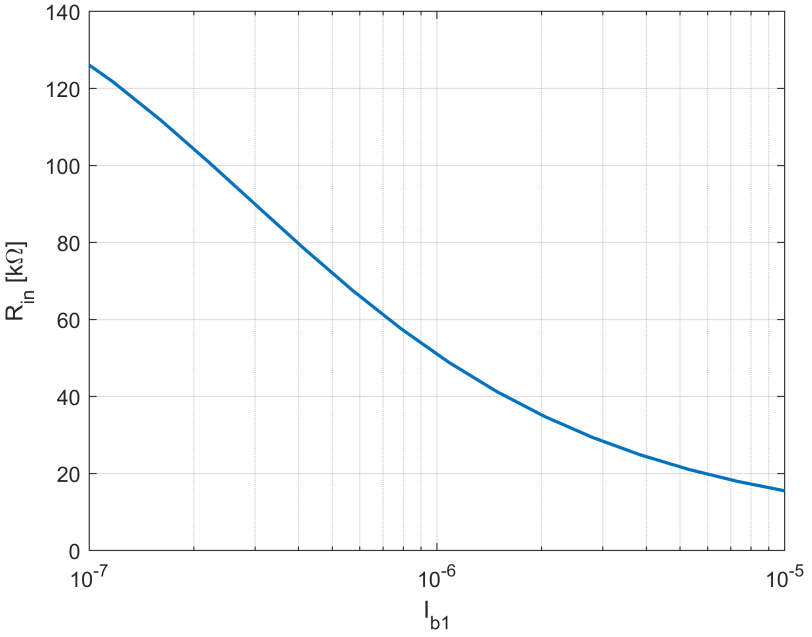


Figure 3.18: Input resistance of the amplifier vs bias current of input branch

Summarizing, this configuration cannot satisfy both the input resistance and the noise requirements, even with best case assumptions and ideal bias current. The gm efficiency can be larger if a NPN is employed at the input, as depicted in figure 3.19.

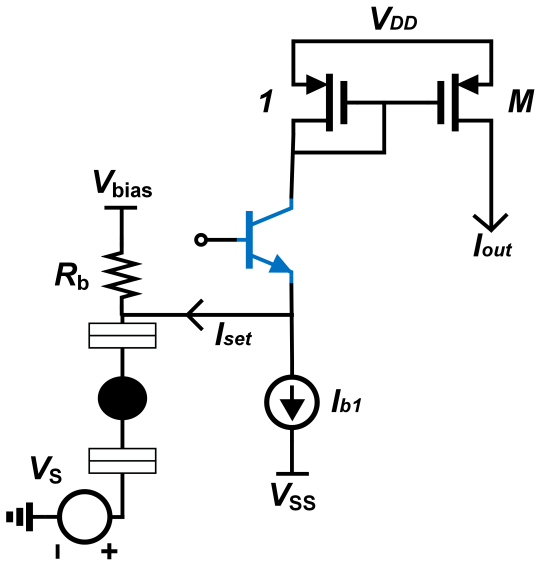


Figure 3.19: Current pre-amplifier, second version

In this case $g_{m,NPN}/I_c = 50$ at $-40°C$ and even about 200 at cryo, based on the measured data [15]. The input resistance is again too high, in that the current needed with this configuration to meet the impedance requirement is $2.5\,\mu$A, a value not compatible with the noise budget.

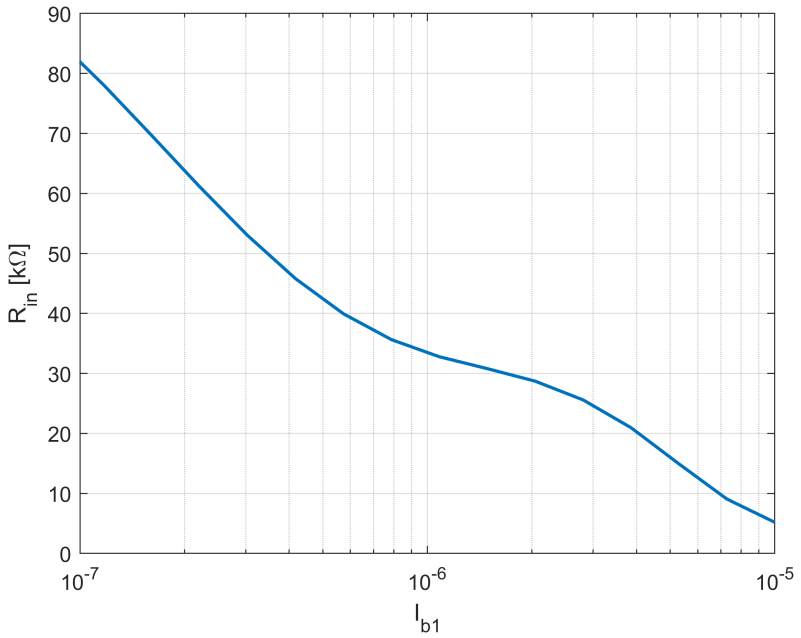
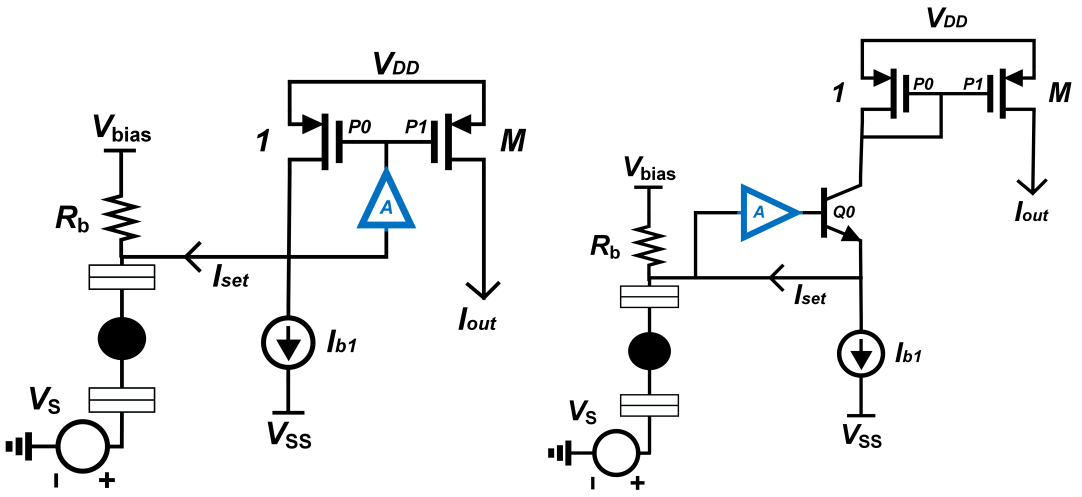


Figure 3.20: Input resistance of the amplifier vs bias current of input branch; 2nd version

Two possible solutions to decrease the current and the input resistance at the same time are shown in figures 3.21a and 3.21b Both the techniques lower the input impedance by the gain of the amplifier A implemented in the following way:

$$R_{in,amp} = \frac{1}{g_{mP0} \times A} \tag{3.31}$$



(a) Gain at the gate of the mirror (config CA3) **(b)** Gain boosting at the gate of input transistor (config CA4)

Figure 3.21: Possible solutions to reduce the impedance at critical nodes; these would allow for relaxed conditions for the current

Lowering the current further however, poses the pole at the gate of the mirror at low frequency because of their big size (necessary for flicker noise to be below shot noise level at $1\,\mathrm{MHz}$), causing integration, as seen in figure 3.22. CA3 effectively solves this if the output resistance of A is sized accordingly such that $f_{p,gate} \leq \frac{1}{2\pi C_{gate} R_{out,A}}$, hence it is investigated further. CA3 is simulated in Cadence with an ideal amplifier (whose model is depicted in figure 3.23) to test the concept. An AC simulation is performed on the CA3 configuration, using $R_{o,Af} = 100\,\mathrm{k\Omega}$ and $g_{m,Af} = 100\,\mu\mathrm{S}$, resulting in $A = 10$. As visible in figures 3.24 and 3.25, now a very low current that respects the noise budget can be used while keeping the input resistance low and avoiding integration.
Theoretically, $I_{ds,P0} = I_{s,bias}$ can be used, achieving very low noise. However, this analysis does not take into account the contribution of flicker noise and of the noise of the feedback amplifier and current source. In order to obtain a negative feedback, the amplifier should be non-inverting, hence the gain must be realized with either a CB stage, CG stage, or a two stages amplifier. The current flowing into this amplifier should be relatively high (in the order of μA depending on the efficiency), if $g_m = 100\,\mu\mathrm{S}$ is needed. Using an NPN is preferred for the high efficiency and low flicker noise, thus the real circuit is realized as depicted in figure 3.26.
In this case, V_{B0} is such that the desired I_{b1} is obtained, while V_{BA} should be such that $V_{BA} - V_{in}$ results in the required g_m. Assuming $g_m / I_C = 50$ at T_{sim} it means that it should be $I_{CA} = 2\,\mu\mathrm{A}$. Since it is desired that $I_{P0} < 37\,\mathrm{nA} << I_{CA}$, also $I_{b1} \approx 2\,\mu\mathrm{A}$. The resistance seen at the input of the feedback amplifier is

$$R_{in,A} \approx \frac{1}{g_{mQA}} \tag{3.32}$$

while the resistance at the drain of P0 is

$$R_{in,P0} \approx \frac{1}{g_{mP0} g_{mQA} R_{oA}} \tag{3.33}$$

For the input current to enter the PMOS, it is desired that $R_{in,A} >> R_{in,P0}$. It is not granted that this condition is satisfied, in that there is a difference in current between QA and P0 of around two orders of magnitude, while the gain simulated previously is only 10. If for noise specification the current in P0 must be below $37\,\mathrm{nA}$ (optimistic estimation), then from figure 2.34 the efficiency is about 35 and $g_{mP0} \approx 1.3\,\mu\mathrm{S}$. On the other hand, $g_{mA} \approx 100\,\mu\mathrm{S}$ by design. In this scenario, even if the input resistance of the PMOS is lowered by A, the preferred path for the input current will be the emitter of QA, because $R_{in,A} < R_{in,P0}$. As a result, most of the current signal would be lost.

A CG stage would suffer from the same low input resistance of the CB stage, hence the only

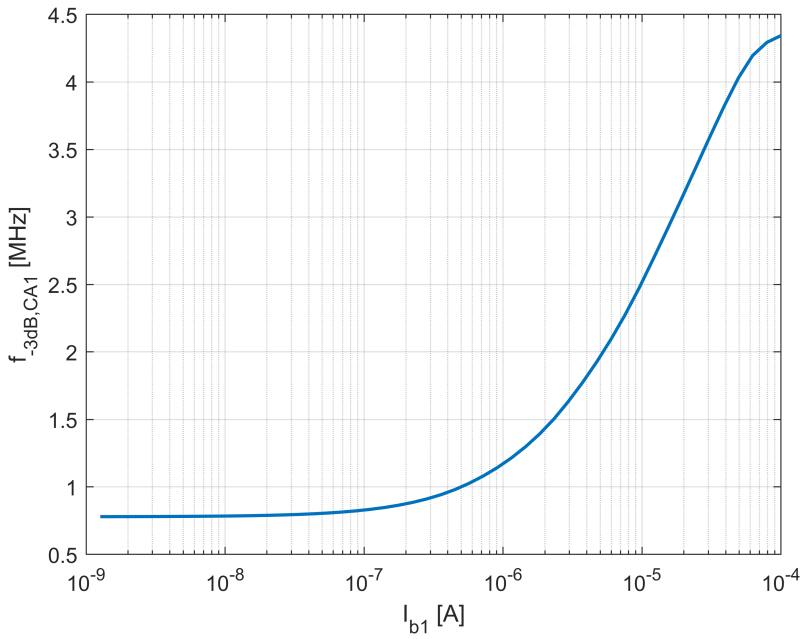


Figure 3.22: Dominant pole goes below 1 MHz for low values of bias current in the CA1 and CA2 configurations, if the PMOS is sized large for flicker noise

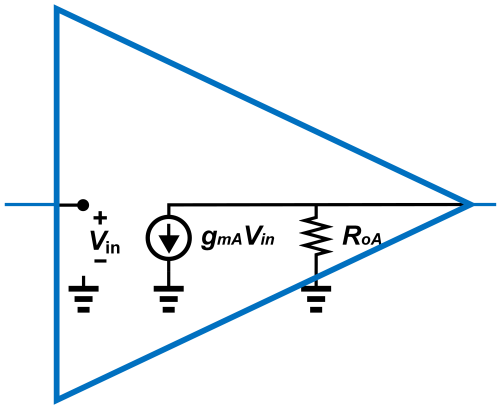


Figure 3.23: Simplified ideal model for feedback amplifier used in CA3

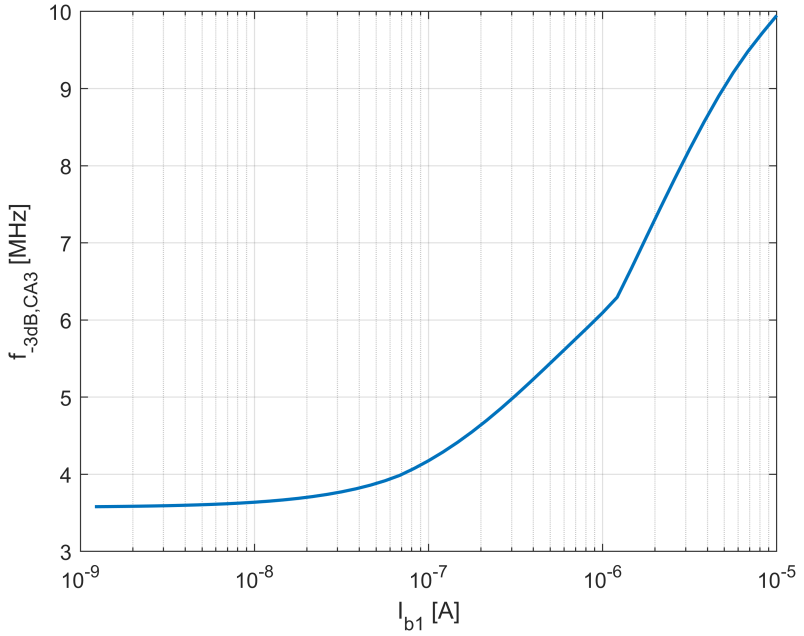


Figure 3.24: Dominant pole of CA3 for different bias current with an ideal gain of $A = 10$. Using big size PMOS now does not result in low frequency cut-off

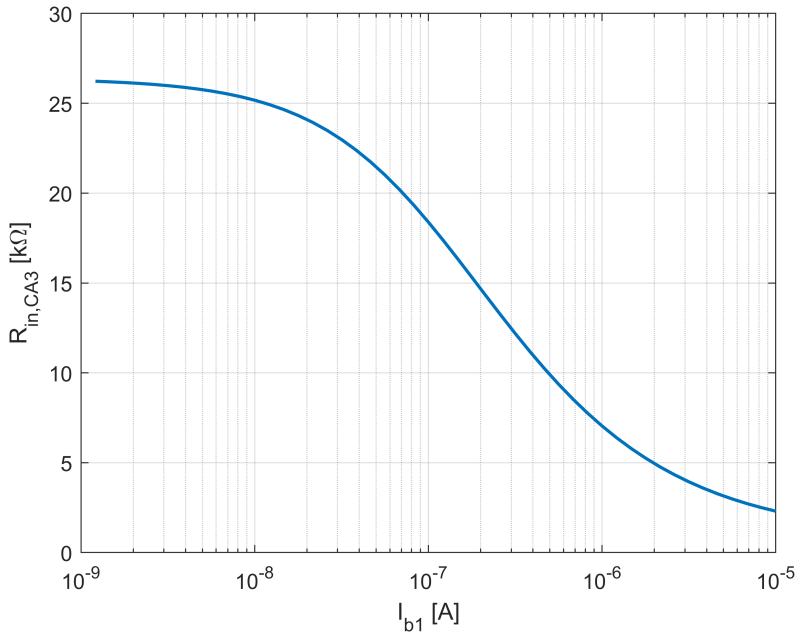


Figure 3.25: Input resistance in CA3 with an ideal gain of $A = 10$

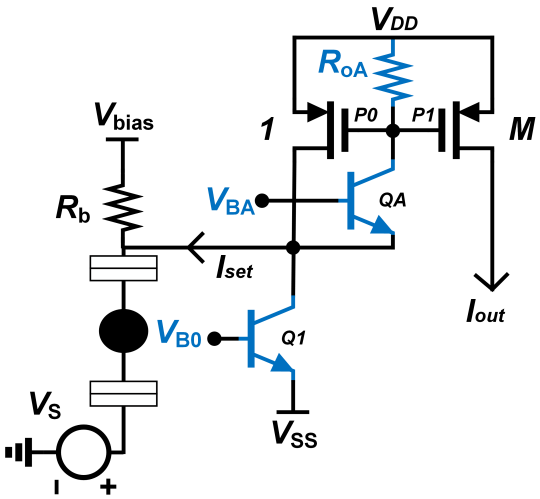


Figure 3.26: CA3 with practical implementation of current source and feedback amplifier

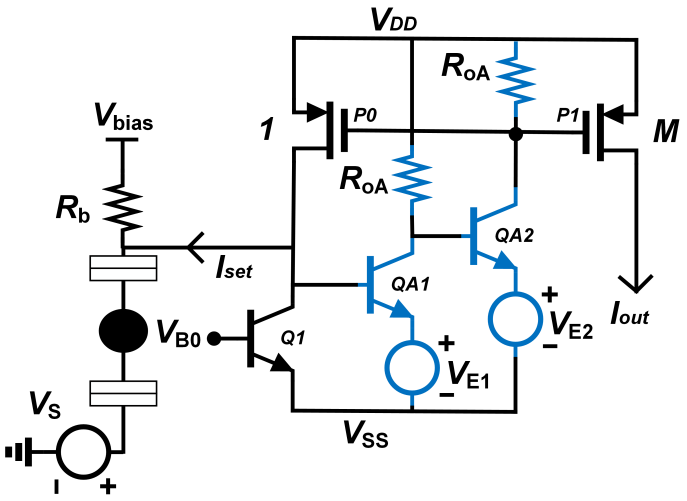


Figure 3.27: CA3 with practical implementation of current source and feedback amplifier using a 2-stage amplifier

option that remains is a two stage CE or a two stage CS, in order to ensure high input resistance for the feedback amplifier.
Figure 3.27 shows a possible implementation of the amplifier with two CE stages. In this way, the input resistance of the amplifier is $r_{\pi QA1}$, which is in the order of $M\Omega$. The required minimum gain of 10 can be divided between $A_1 \geq 5$ and $A_2 \geq 2$; with $R_{oA} = 100\,\text{k}\Omega$ then it should be $g_{mQA1} = 50\,\mu\text{S}$ and $g_{mQA2} = 20\,\mu\text{S}$. Consequently, the required currents with a transconductance efficiency of 50 are respectively $1\,\mu\text{A}$ and $400\,\text{nA}$.
It is not trivial, with this configuration, to establish the correct bias point for the devices. The emitter voltage should be chosen taking into account the supply and the required currents $I_{C,QA1}$ and $I_{C,QA2}$, such that the following conditions are met:

$$V_{DD} = V_{E1} + V_{BE,QA1} + V_{DS,P0} \tag{3.34}$$

$$V_{DD} = V_{E2} + V_{BE,QA2} + I_{C,QA1} R_{oA} \tag{3.35}$$

$$V_{GS,P0} = V_{GS,P1} = I_{C,QA2} R_{oA} \text{ based on wanted input branch current} \tag{3.36}$$

From the NPN characteristics in section 2.4.6, the wanted currents are sustained if $V_{BE1} = 755\,\text{mV}$ and $V_{BE2} = 736\,\text{mV}$. If it is acceptable that $V_{DS,P0} \approx 450\,\text{mV}$, then V_{E1} can be connected to GND (V_{SS} in this case). Substituting in the second equation instead, it is obtained $V_{E2} \approx 360 mV$. From the

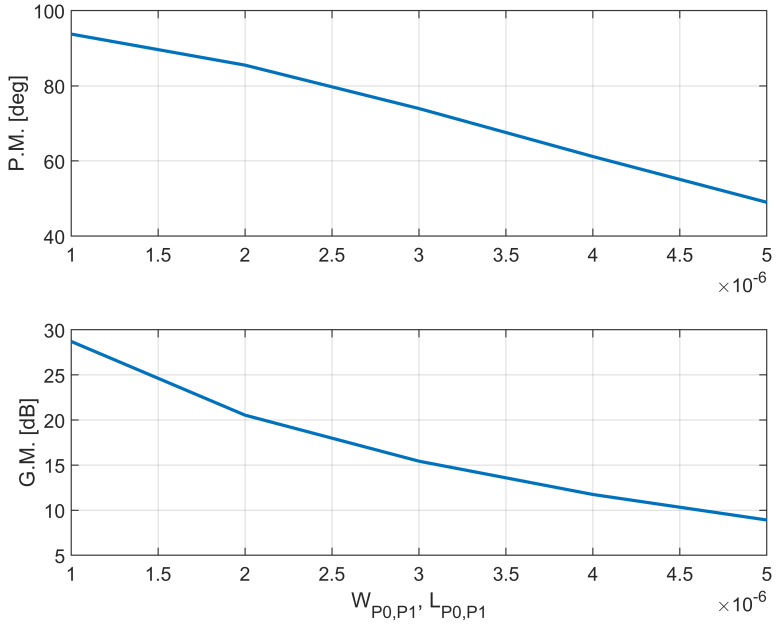


Figure 3.28: Phase and gain margins of the system loop formed by P0 and QA1,QA2. Bigger PMOS reduce the margins. In this analysis, $W_{P0,P1} = L_{P0,P1}$

third equation however, it is apparent that V_{E2} is a non-linear function of I_{b1}, because this depends on $V_{GS,P0|P1}$. Because of this non-linearity, an initial assumption is made for the design a starting point; $I_{b1} = 10\,\text{nA}$ ensures low noise, it is larger than the expected base current of QA1 and it can theoretically respect all the R_{in} and bandwidth constrictions.
From the characteristics of the PMOS in 2.4.6, it is required $V_{GS} \approx 323\,\text{mV}$ to obtain such current. As a consequence, it must be $I_{C,QA2} \approx 3.2\,\mu\text{A} \longrightarrow V_{BE,QA2} = 778\,\text{mV}$ and as a result $V_{E2} = 322\,\text{mV}$.

Simulating this configuration, it is noticed that the loop formed by the amplifier and the mirror is unstable; this because it contains two poles close to each other, namely $f_{p,in}$ and $f_{p,gate}$, both a bit above $1\,\text{MHz}$. In order to achieve stability either one of the two poles needs to be moved at very high frequency, or one of the two poles needs to be at lower frequency such that the open-loop TF crosses the $0dB$ point with enough phase margin. The first option is desirable, but not easily achievable in that the input pole is function of the loop itself: without the loop and with a bias current as low as $10\,\text{nA}$, this pole is at low frequency due to high input resistance. Trying to place at higher frequency the gate pole solves the stability issue as visible in figures 3.28 and 3.29. Due to low gain margins, the output current shows ringing for $W \geq 2\,\mu\text{m}$. This value is therefore chosen as size of the PMOS and noise analysis is performed including flicker noise and shot noise from the NPNs. The result, visible in table 3.2, shows that now the dominant noise source is the amplifier used to reduce the input impedance, as its noise appears directly at the input node. The spot noise at $1\,\text{MHz}$ is 91 times the white noise level of the SET for a bias current as low as $10\,\text{nA}$, showing that this circuit is too noisy for achieving the target SNR.
The second option to stabilize the loop (decrease one of the two f_p) would mean implementing integration at one of the two nodes under consideration. In the scenario where integration happens, the current enters parasitic capacitances instead of the mirror, meaning that the system is behaving like a VA/CHA more than a current amplifier.

During the duration of this work, it was not possible to find a way to effectively perform current pre-amplification before the readout circuit without integration of the signal or achieving low noise operation. For this reason, the CA is set aside and more effort is put in other architectures.

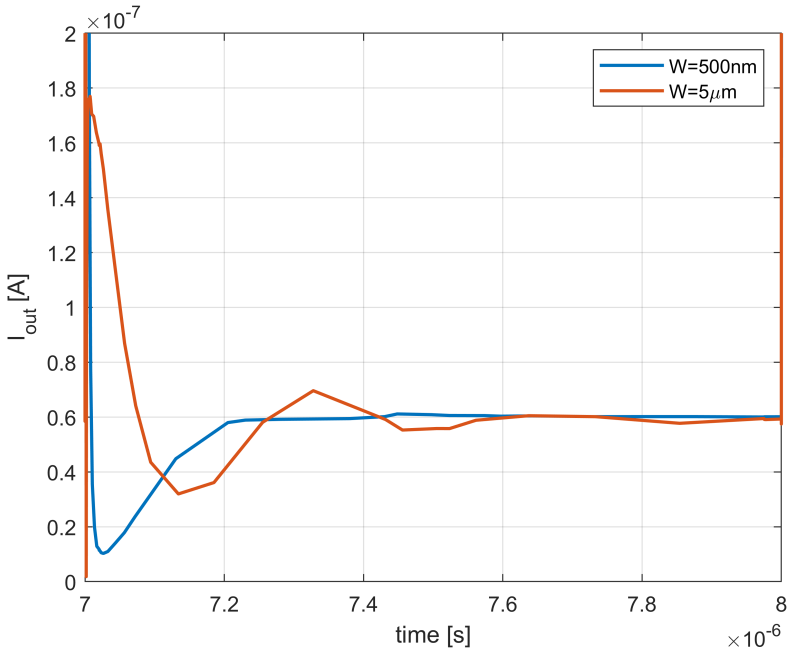


Figure 3.29: Step response of the CA3 for different sizes for P0 and P1. For smaller size, the oscillations are removed

Noise source	Contribution percentage [%]	Integrated output noise [A^2]
$I_{n,C,QA1}$	84.5	4.8×10^{-25}
$I_{n,CH,P0}$	9.6	5.4×10^{-26}
$I_{n,CH,P1}$	2.8	1.6×10^{-26}
$I_{n,SET}$	1.1	6.2×10^{-27}

Table 3.2: Simulated noise contributions for CA3 (spot noise at 1 MHz); the feedback amplifier helps satisfying the bw and input resistance constrictions, but introduces too much noise

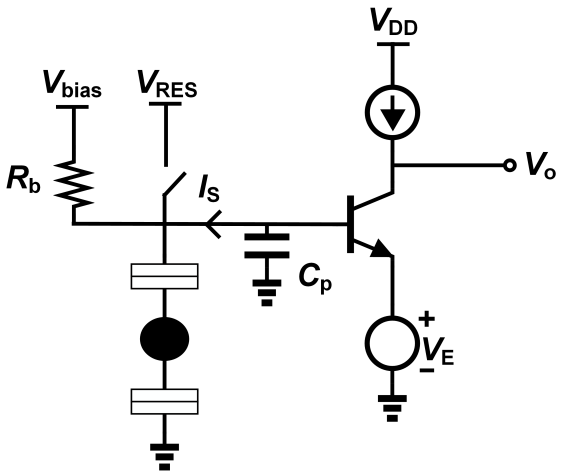


Figure 3.30: Voltage amplifier

3.3.3 Voltage amplifier

A simple voltage amplifier is depicted in figure 3.30. The DC gain of such configuration is:

$$\frac{V_{out}}{I_S} = \frac{V_{in}}{I_S} \times \frac{V_{out}}{V_{in}} = \frac{V_{in}}{I_S} \times A_V = R_{in} \times g_m R_{out} \tag{3.37}$$

where R_{out} is the equivalent resistance at the output node. This is r_o of the NPN in case of an ideal current source as a load, and it is $r_o//R_L$ in case of a resistive load. An NPN is used as amplification transistor due to its very high transconductance efficiency and low flicker noise, as discussed in section 2.4. The lowest voltage in the circuit is the emitter of the bipolar $V_E = V_{SS}$. If the source of the SET is assumed to be ground, then V_E must be negative in that the NPN needs $\approx 750\,\mathrm{mV}$ for amplifying while the SET is biased with very low drain-source voltage $V_{DS} \approx 1\,\mathrm{mV}$. Integration should be performed somewhere, as it represents the best receiver for the input: the input node seems the most reasonable choice because a big parasitic capacitance (C_p) is already present. The bandwidth constraint is here less strict compared to the current amplifier, because integration implies that the input pole is lower than $1\,\mathrm{MHz}$, and the lower bound for the bandwidth is given only by the wanted output swing at $1\,\mathrm{MHz}$.
Without considering the load capacitor, which depends also on the following stage, the frequency response depends on the input time constant $\tau_{in} = R_{in}C_p$ where $R_{in} = R_b//R_{set}$ and $R_b = 1\,\mathrm{M\Omega}$ is the bias resistance connected to the input node. The frequency of the pole for the typical set resistance of $133k\Omega$ and $C_p = 2pF$ is

$$f_{p,in} \simeq 600\,\mathrm{kHz} \tag{3.38}$$

Considering the input pole, the frequency dependent transfer function is

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m R_{out}}{1 + sC_p R_{in}} \tag{3.39}$$

It is not crucial to consider the output pole yet, in that it will cause filtering of all the noise sources and the signal equally, not impacting the SNR.
The limitation of this architecture is that, contrarily to what happens in the other amplifier configurations, the information is contained in the voltage, meaning a big voltage swing is desired at the drain of the SET. As it has been clarified in section 2.2, the signal swing is not detrimental for the readout operation; on the other hand, the reset after every incoming symbol can affect the stability of the qubits.
For the voltage amplifier (and in general when there is integration at any node) reset is needed to avoid Inter-Symbol-Interference (ISI) as mentioned in section 3.2.
The voltage amplifier has two main noise sources, one being the collector shot noise and the other one being the base shot noise. The first one, usually dominant, appears at the output and

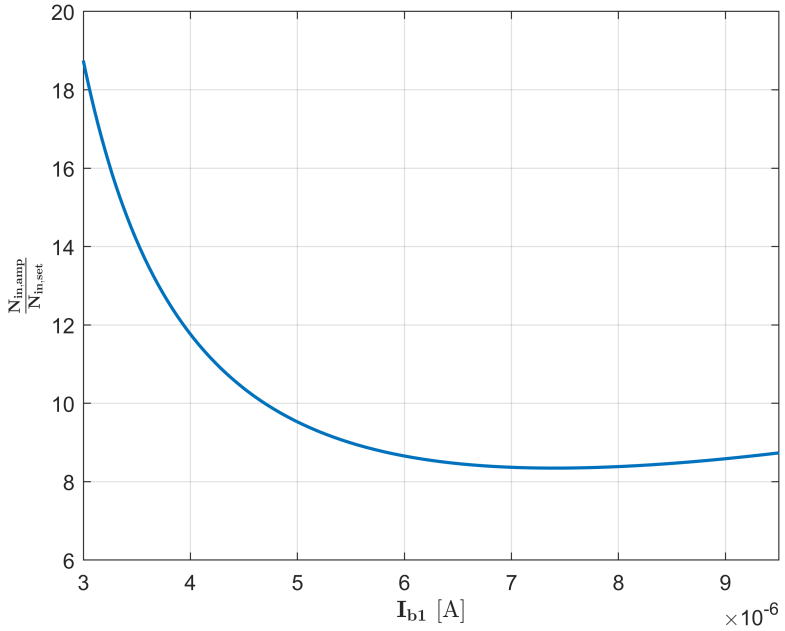


Figure 3.32: Noise performance from the analysis in 3.2.2 for the VA (resistive load). The noise is referred at the input as current source entering the input node

it is divided by the gain when referred to the input; the choice of the g_m and hence of the current impacts considerably the contribution of this noise source. The second one, appears already at the input so the choice of the gain does not have any effect on its contribution to the total noise.

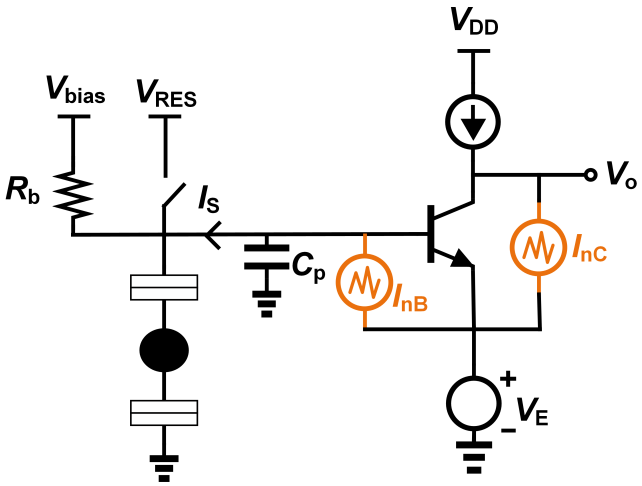


Figure 3.31: Main noise sources of the voltage amplifier

As done for the current amplifier, the input referred noise is compared to the SET noise for the VA in figure 3.32. The VA yields very good result in that for many bias current values the noise is comparable to the SET noise, with a best bias point where the amplifier produces only 8 times the noise of the SET. The noise does not get better and better by simply spending more power, in that after some value of current, the base shot noise (already input referred) of the NPN starts dominating the overall noise. Increasing the gain at this point does not improve further the ratio between amplifier noise and SET noise. In addition to this, increasing the current too much causes the OP of the output node to go too low for the NPN to amplify, resulting in a decrease in gain and higher input referred noise.
The voltage swing given by the maximum supply for the technology ($1.2V$) reduces the design space. Using a resistive load, $R_L = 100k\Omega$ is chosen because a higher resistance would imply very

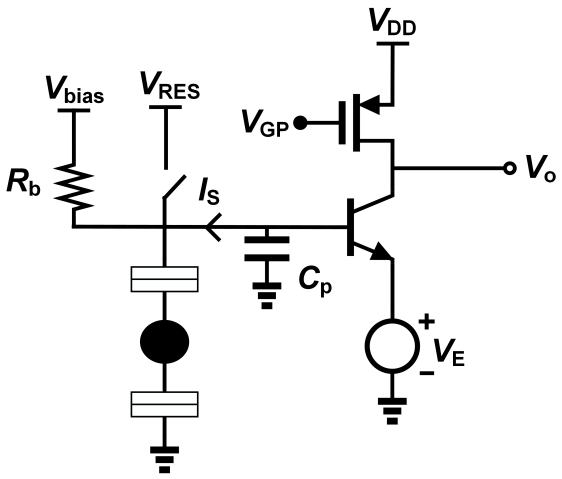


Figure 3.33: VA with active load

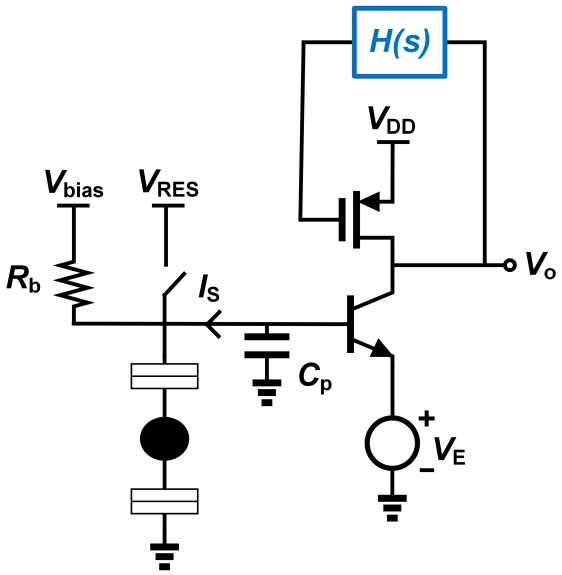


Figure 3.34: Additional feedback network for a well defined OP of the output node

low operating point for the output node, while the NPN needs at least $V_{CE} = 200mV$ to amplify correctly. Assuming an operating current of around $7.5\,\mu$A, it needs to be $V_{DD} - V_E = R_L \times 7\,\mu\text{A} + V_{CE,min}$. The supply of this configuration can be lowered to $1\,\text{V}$ without losing performance.

A possible option could be to implement the load with a PMOS. Even though the shot and flicker noise introduced would affect negatively the SNR, a positive aspect of the active load would be the possibility to reduce a lot the supply voltage, because in this case the minimum supply becomes $(V_{DD} - V_E)_{min} = V_{DS,min} + V_{CE,min} \approx 300\,\text{mV} + 200\,\text{mV} = 500\,\text{mV}$. However, since the noise shows an optimum respect to the current, it is not possible to trade the decrease in power with a decrease in noise, hence the active load in this case worsens the noise irreversibly. Assuming that there is enough SNR to sustain a bit more noise, the active load option could still result in the best option for the lower power. One problem with this configuration is that the operating point of the output node is not well defined, and any small shift in the input voltage will cause a large shift in the OP. This can be apparently solved by the use of a feedback network that adjusts the gate voltage of the PMOS and keeps the OP constant, as in figure 3.34. Implementing a feedback results however in killing most of the gain, in that the output signal becomes an input at the gate of the PMOS with opposite sign. The only way around this it is to implement $H(s)$ as a low

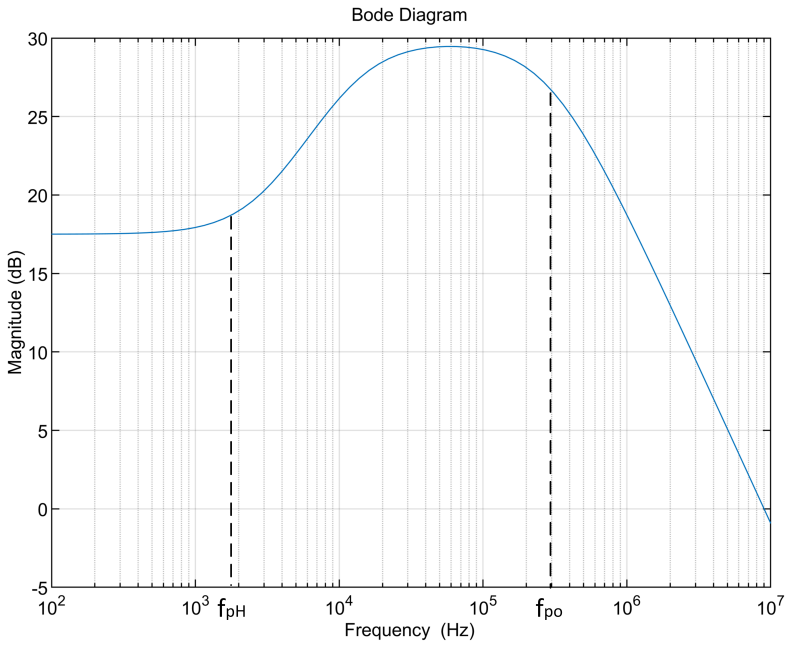


Figure 3.35: Transfer Function of Closed-Loop configuration; equivalent to band-pass filter with gain for a selected frequency range

pass filter with very low cut-off frequency, such that only the DC OP is fed back at the gate of the PMOS, while the rest of the frequencies is amplified in the open loop path. With $A(s) = g_{m,NPN} Z_{out}$ gain of the OL amplifier, $H(s) = \frac{A_H}{1+\frac{s}{2\pi f_{p,H}}}$ TF of the feedback low pass block and $A_f(s) = g_{m,MOS} Z_{out}$ then the CL TF is:

$$\frac{V_{out}}{V_{in}} = -\frac{A(s)}{1 + H(s)A_f(s)} \tag{3.40}$$

This TF shows a band-pass shape as in figure 3.35.
This type of transfer function is incompatible with the band of the input signal: assuming that the input is steady for long enough (same symbol repeated for many cycles), the information can effectively be located in the spectrum at $f_{in} \leq f_{pH}$. If this is the case, the high frequency noise is amplified more than the signal: as a consequence, the information drowns in the noise and it is lost. This being said, the VA will be further studied only in the resistive load Open-Loop configuration. For this same reason, it is not possible to implement AC-coupling at the input of the amplifier as done in [43].

From the characteristics in section 2.4.1 it can be seen that for the chosen bias current for optimal noise ($7.5\,\mu$A) the transconductance is $g_m \simeq 375\,\mu$S, given that the efficiency of the NPN is $50\,$S/A at the simulation temperature of $-40\,^\circ$C. Therefore, the gain is about $A_{DC} = g_m R_L = 37.5$ and with an expected input swing of around $I_S \times R_{in} \approx 35\,\mu$V, the output swing results in the order of $1\,$mV. The circuit behaviour for an input 0 and input 1 is visible in figure 3.36.
The finite resistance at the input node, mainly determined by the SET resistance, makes the integrator of the voltage amplifier a leaky integrator. The lower the input resistance, the smaller the time constant; this means ultimately less voltage swing at the input when the signal is sampled before reset for a given SET current. On the other hand, the opposite also holds, and the main goal should be to manufacture/use an SET with high output resistance so that the voltage swing increases.
This increase cannot go on indefinitely, in that when the input resistance grows so much that the integration becomes basically ideal, the input swing saturates; moreover, the upper bound can be given by other bias resistances that appear in parallel with the SET resistance as shown in figure 3.37.

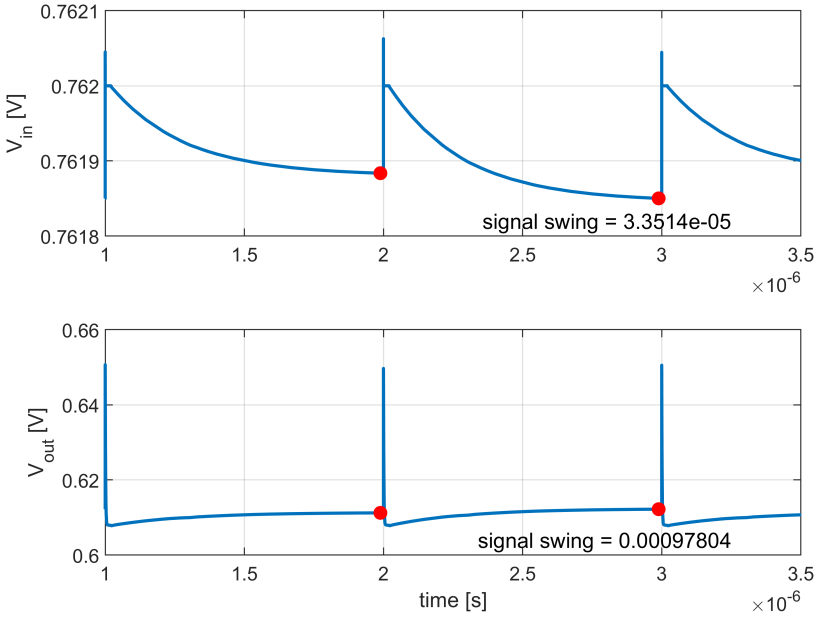


Figure 3.36: input and output signals for a 0 and a 1 in the voltage amplifier

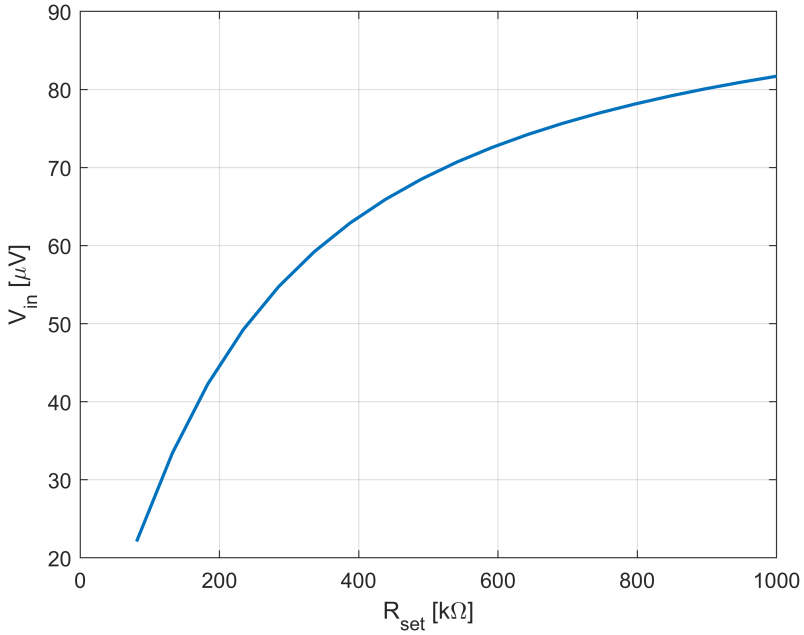


Figure 3.37: Simulated input swing vs SET resistance with a bias resistance $R_b = 1\,\mathrm{M\Omega}$ and a parasitic capacitance $C_p = 2\,\mathrm{pF}$

Considered this, an increased input swing from the SET can affect positively the SNR if the collector shot noise is dominant, in that:

$$\frac{V_{out}^2}{V_{n,out}^2}(s) = \frac{I_s^2 A^2 Z_{in}^2}{(I_{n,in,set}^2 + I_{n,in,B}^2) A^2 Z_{in}^2 + I_{n,C}^2 R_{out}^2} \tag{3.41}$$

with $Z_{in} = \frac{R_{set}//R_b}{1+s(R_{set}//R_b)C_p}$ and $A = g_m R_{out}$ (output capacitance not considered). If the system has one dominant pole, an equivalent noise bandwidth can be derived as

$$ENBW = \frac{\pi}{2} f_{p,in} = \frac{\pi}{2} \frac{1}{2\pi C_p R_{in}} \tag{3.42}$$

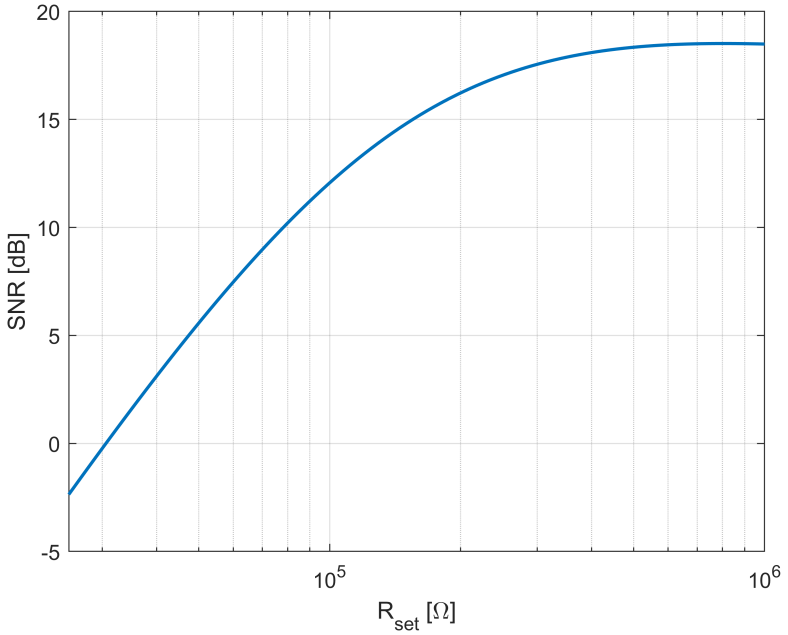


Figure 3.38: Approximated SNR vs SET resistance

A first order approximation for the SNR without considering sampling and non-white noise sources can be written as:

$$SNR = \frac{I_s^2 g_m^2 R_{in}^2 \left(1 - e^{-\frac{T_b}{\tau_{in}}}\right)^2}{\left((I_{n,in,set}^2 + I_{n,B}^2) g_m^2 R_{in}^2 + I_{n,C}^2\right) \times ENBW} \tag{3.43}$$

This equation is shown in the plot 3.38 for variable SET resistance, highlighting how a larger R_{set} results in larger V_{in} (plot 3.37) and therefore better SNR. An enhanced SET resistance is always desirable also for the CA, TIA and CHA but for a different reason; being the signal of interest in these amplifiers is the current, a low SET resistance causes a share of the signal not to flow into the amplification stage and to circulate instead in the SET.
The estimated power consumption of this stage is

$$P_{va} = V_{dd} \times I_{c,rms} \approx 1.2\,\mathrm{V} \times 7.5\,\mu\mathrm{A} = 9\,\mu\mathrm{W} \tag{3.44}$$

Overall, the VA seems to be a very good candidate as final amplifier for the frontend and deserves going through more thorough study and optimization. A more comprehensive simulation of this configuration in the complete system environment is detailed in chapter 4.

3.3.4 TIA

The TIA is just a VA with resistive feedback, as can be seen in figure 3.30. The gain of this configuration can be approximated as:

$$\frac{V_{out}}{I_S} \simeq R_F \tag{3.45}$$

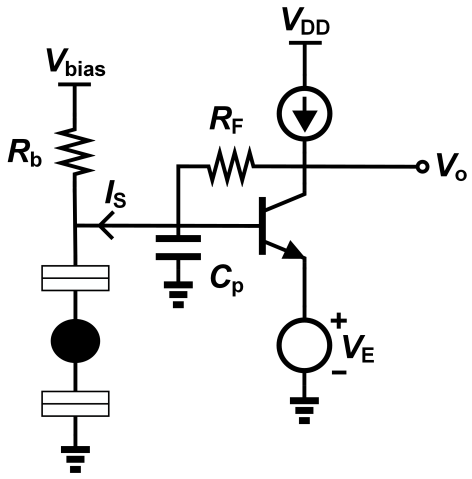


Figure 3.39: Transimpedance amplifier

The TIA can provide an alternative to the VA for one main reason: the integration can be moved from the input node to the output node, relieving the swing that the SET has to sustain during the preparation of the quantum dots states. As can be observed in figure 3.43 the input swing is only $7\,\mu\text{V}$ and depends exclusively on the signal. It is possible to avoid integration at the input despite the large parasitic due to the low input resistance; in this case integration can be performed at the output by adding a capacitance, to be sized based on the needed output swing. The feedback lowers the input resistance by the DC gain of the amplifier due to the Miller effect:

$$R_{in,amp} \simeq \frac{R_F}{g_m R_o} \tag{3.46}$$

Assuming the amplifier can provide a gain of about 30, using $R_F = 2M\Omega$ with $C_p = 2\,\text{pF}$ ensures that $f_{p,in} > f_{symbol}$ and thus integration doesn't happen at the input. The current coming from the SET will however split with the current divider:

$$I_{in} \simeq I_F \simeq I_s \times \frac{R_{set}//R_b}{R_{set}//R_b + \frac{R_F}{1+g_m R_{out}}} \tag{3.47}$$

meaning that some current does not enter the TIA and it is lost. In equation 3.47 the input resistance of the NPN is neglected because $r_\pi >> R_{set}$. Plugging the values in shows that about 64% of the SET current flows into the feedback of the TIA for the chosen R_F and the typical SET resistance value. Less signal could be lost if the gain of the amplifier is increased, however this would also mean that the OP is moved away from the noise optimum. As discussed in for the VA, a larger SET resistance increases the input signal; however this time the upper bound is set by I_s, hence the potential for increasing the SNR is lower. As it can be observed in plot 3.41, going from a $100\,\text{k}\Omega$ to a $1\,\text{M}\Omega$ SET resistance increases the SNR by $3\,\text{dB}$.
The noise simulation yields the result visible in figure 3.40. The TIA noise behaviour is just slightly worse than the VA. As done for the VA, a first approximation of the SNR can be derived as

$$SNR = \frac{V_{out}^2}{V_{n,int}^2} = \frac{I_s^2 R_F^2 \left(\frac{R_{set}//R_b}{R_{set}//R_b + R_{in,amp}}\right)^2}{\left((I_{n,set}^2 + I_{n,B}^2) R_F^2 \left(\frac{R_{set}//R_b}{R_{set}//R_b + R_{in,amp}}\right)^2 + I_{n,C}^2 R_{out}^2\right) \times ENBW} \tag{3.48}$$

The gain of the TIA is lowered if compared with the one of the VA; the gain of the VA is the limit case for the TIA with $R_F \longrightarrow \infty$. The output swing (the distance between a 1 and a 0) is $V_{out} = 225\,\mu\text{V}$. The equivalent gain is definitely lower compared to the VA, while the current used for optimum noise is slightly higher ($8\,\mu\text{A}$), resulting in an estimated power consumption of

$$P_{tia} \approx 1.2\,\text{V} \times 8\,\mu\text{A} = 9.6\,\mu\text{W} \tag{3.49}$$

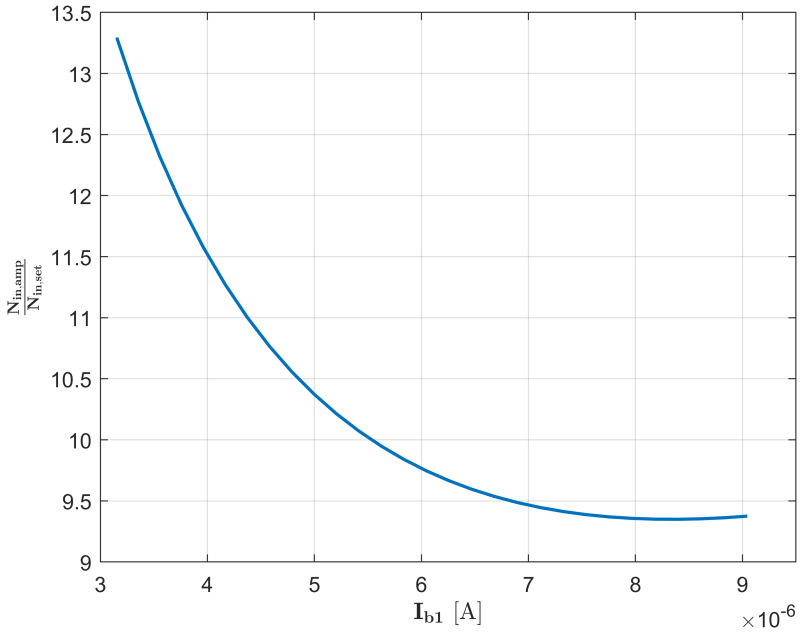


Figure 3.40: Noise performance from the analysis in 3.2.2 for the TIA

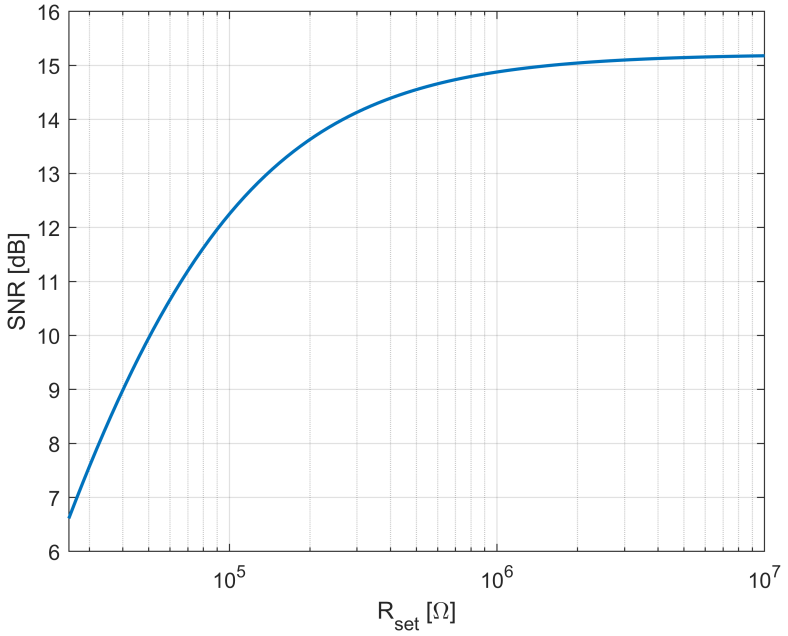


Figure 3.41: First order approximation SNR vs SET resistance for the TIA

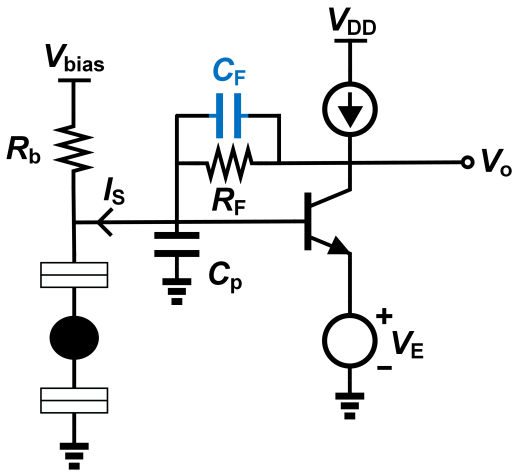


Figure 3.42: TIA: stable version with feedback capacitor

One problem associated with the TIA is that if the feedback is only resistive, then the amplifier is unstable. A capacitor in parallel as in figure 3.42 solves the issue and removes the oscillations. The value of C_F for stability depends on the input capacitor but also on the load capacitor, neglected in this analysis. For this analysis, the value used is such that for the TIA itself (not considering the input pole) the low frequency gain and the high frequency gain are equal, in other words $\frac{C_p}{C_F} \approx \frac{R_F}{R_{in}} \longrightarrow C_F = 250\,\text{fF}$. This value can only be an approximation, because the exact value of the parasitic C_p is not known a priori.
A downside of the TIA is the presence of the feedback resistor, a big passive that increase considerably the area of the circuit. Being the potential for scalability the main goal, total area is an aspect to consider. On the other hand, the smaller sensitivity of the bias current to noise and the absence of input reset are factors that keep the TIA a viable option as frontend amplifier.

3.3.5 Charge amplifier

The charge amplifier under study is the VA with capacitive feedback shown in figure 3.30. The charge amplifier can be seen as a TIA where the feedback resistor is very high; the gain of this configuration in the high frequency limit (dominant pole frequency lower than operating frequency):

$$\frac{V_{out}}{I_{in}}(t) \simeq \frac{T_b}{C_F} \tag{3.50}$$

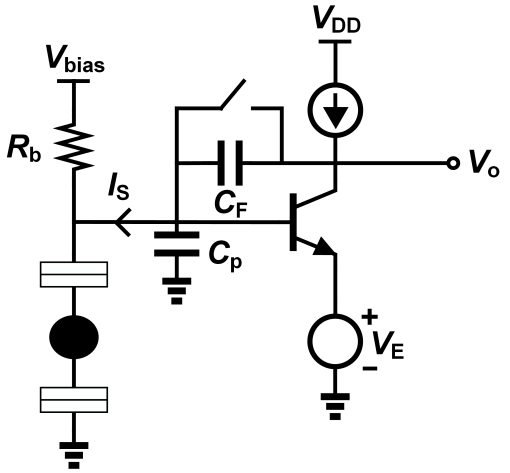


Figure 3.44: Charge amplifier

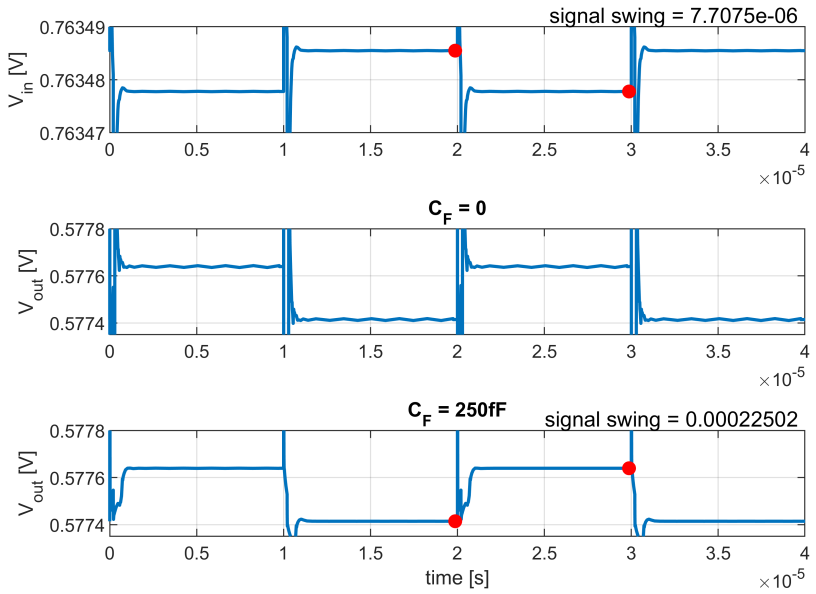


Figure 3.43: input and output signals for a 0 and a 1 in the TIA; the output node oscillates if the value of the feedback capacitor is too low. On the other hand, if C_F is too large the signal is attenuated due to integration. The plot shows operation at 100 kHz so that the oscillations are visible (at $f_{symbol} = 1$ MHz the reset happens too early for them to show up).

In this case, the integration is performed on the feedback capacitor, thus it needs to be reset after each reading at a rate of f_{symbol}. The need for reset on this capacitor poses again the problem of excess swing on the SET during the preparation of the states: during the reset the input node and the output node are brought to the same potential, however the output node is biased at a very different voltage compared to the drain of the SET for best noise result.
The input referred noise is in the best case the same of the VA, around eight times the noise of the SET. However, the noise is very sensitive to the bias current, as is shown in figure 3.45.

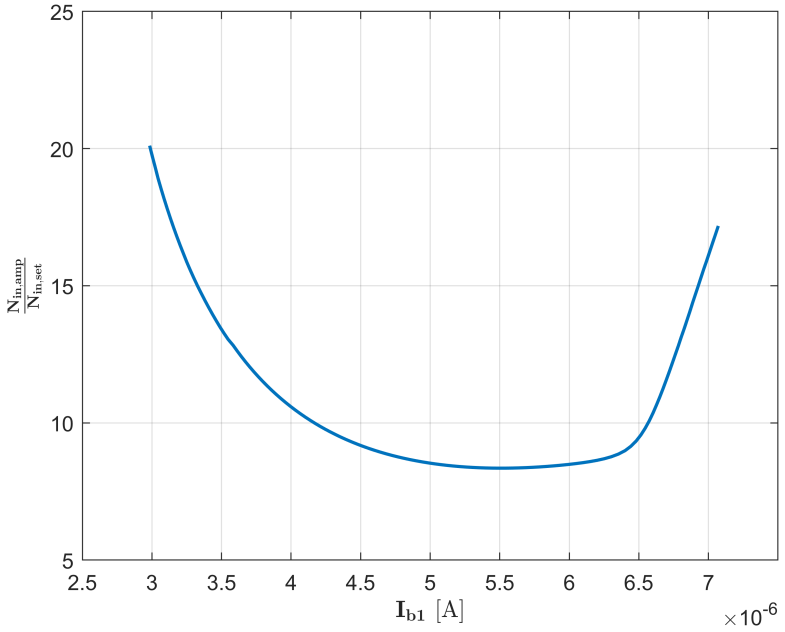


Figure 3.45: Noise performance from the analysis in 3.2.2 for the CHA

As for the VA and TIA, increasing the current after the optimum results in ultimately reducing the V_{CE} of the NPN causing reduction in gain and increment in input referred noise.

The waveforms plot in figure 3.46 show that the charge amplifier displays a perfect integrating behaviour of the output voltage if C_F is large enough. The integrating capacitor C_F should be sized such that the sampling/reset moments happen before the output node reaches a voltage too low (or too high, depending on the polarity) to avoid clipping. It should always be $200mV \leq V_{out} \leq V_{dd}$, otherwise the amplifier will start saturating, killing the output signal. With these premises, the capacitor is chosen to be small enough not to reduce the gain too much, but big such that perfect integration takes place and no current leaks into the input resistance: $C_F = 1pF$. It can seem that being $C_p > C_F$, then most of the current will flow into C_p. Due to Miller effect, the feedback capacitor appears at the input node larger, amplified by the gain such that $C_{in,eq} = C_F \times g_m R_{out}$; the current entering the amplifier is eventually (high frequency limit, neglect resistances R_{set} and r_π):

$$I_{in} = I_s \frac{C_F g_m R_{out}}{C_F g_m R_{out} + C_p} \approx I_s \tag{3.51}$$

If C_F is large such that $\tau_{in} = R_{in} C_{in,eq} >> T_b$, then increasing R_{set} has limited to no effect on the SNR; on the other hand, a lower SET resistance decreases the SNR as a consequence of less input swing when τ_{in} starts being comparable or lower than T_b (non-perfect integration). This scenario is equivalent to the case where C_F is seen by the signal as an open circuit, hence the circuit is equivalent to a VA. As for the TIA, the finite gain of the amplifier attenuates the actual gain of the CHA:

$$\frac{V_{out}}{I_{in}}(s) = Z_F \frac{A}{A+1} = \frac{1}{sC_F} \frac{g_m R_{out}}{g_m R_{Rout} + 1} \tag{3.52}$$

If the time constant is high compared to T_b, in the time domain it can also be said that

$$\frac{V_{out}}{I_{in}} = \frac{T_b}{C_F} \frac{g_m R_{out}}{g_m R_{out} + 1} \tag{3.53}$$

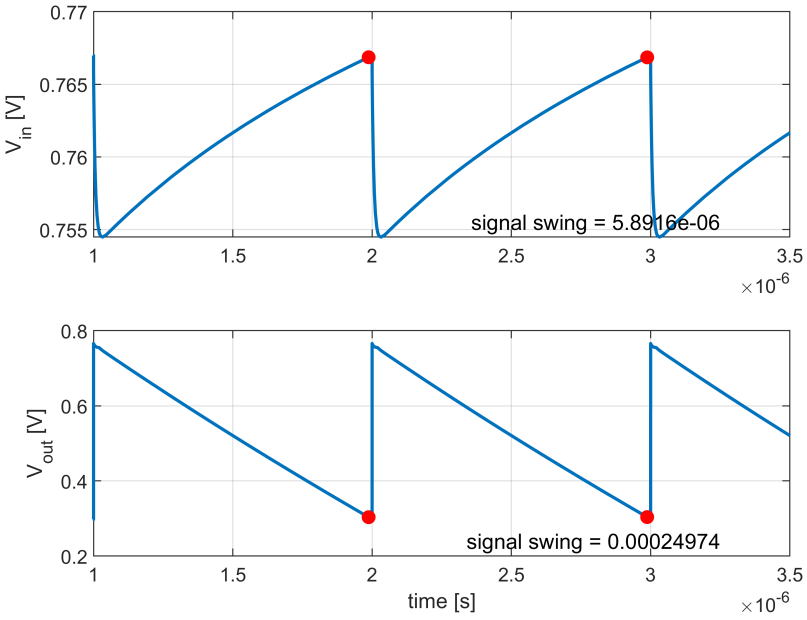


Figure 3.46: input and output signals for a 0 and a 1 in the CHA ($C_F = 1pF$)

The output swing of the charge amplifier is $V_{out} = 250\mu V$, similar to that of the TIA. While for this metric the VA tends to be the best option, from the noise point of view the charge amplifier is comparable to the VA. The reset swing is better for the VA, which also has margins for improvement if the reset voltage is accurate enough. In the CHA case, increasing R_{set} does not have any effect if there is already perfect integration.
On the power side, this configuration shows quite some potential given that the optimum noise

power is reached for $I_c = 5.5\,\mu\text{A}$ resulting in a required transconductance of $g_m = 275\,\mu\text{S}$ at $-40\,^\circ\text{C}$ and a total power consumption of

$$P_{cha} \approx 1.2\,\text{V} \times 5.5\,\mu\text{A} = 6.6\,\mu\text{W} \tag{3.54}$$

3.3.6 Comparison and conclusion

The simulation results from the four amplifiers are summarized in table 3.3. The four configurations were compared based on noise, swing, power and area at T_{sim}. At this point, the true SNR of these architectures is not simulated yet, in that without sampling, only a very coarse approximation is possible for the SNR; a specific setup to simulate the SNR will be introduced in the next chapter and it will be applied to the design of the VA. It is recalled that the parameter K is equal to $N_{i,amp}/N_{i,set}$. For a fair comparison, the noise ratio K is reported at its minimum for each configuration but also at the same minimum power level for all the architectures. The minimum current level of $3\,\mu\text{A}$ (which result in minimum power $3.6\,\mu\text{W}$) is given by practical limits regarding operating point and biasing of the devices.

	K@3.6 μW	**K$_{\text{min}}$**	**P@K_{min}** μW	**Gain@** 1 MHZ	**Reset swing** mV	V_O	Area
CA	≈ 100	91	5	5 A/A	0	1.3 nA	medium
VA	19	8.3	9	3.26 MV/A	1.1	1 mV	small
TIA	13.5	9.2	9.6	750 kV/A	0	230 μV	large
CHA	20	8.5	6.6	833 kV/A	10	250 μV	small

Table 3.3: Comparison of the four architectures for the frontend amplifier. Noise of each configuration is listed at the same power level and at the minimum possible.

VA, TIA and CHA all yield comparable results. While the TIA can reach lower noise at the minimum power level, VA and CHA have lower minimum noise levels, which can be very useful in case the target SNR is difficult to reach. While CHA reaches the same noise minimum of the VA at a lower power level, it has the drawback of presenting larger reset swing at the drain of the SET.
Due to time constraint of this work, only one configuration can be designed and layout including the whole system with bias networks and comparator. Since it is clear that the three more promising architectures have a VA as core of the block, the last and main chapter of this work will present the design of a complete frontend readout circuit employing a Voltage Amplifier. TIA and CHA are options that can be explored in future works starting from the base of the VA designed in this project.

4

Circuit design for the proposed spin-qubit readout

This chapter of the thesis covers the transistor-level design of the final circuit. The system is described block-by-block and the behaviour of the circuit is explained in details. At the end, the schematic-level performance is evaluated in simulations.

4.0.1 Setup for addressing performance in simulation

The most important metric for judging the functionality of the readout circuit is the Signal to Noise Ratio (SNR). The SNR should be $10dB$ at the input of the comparator, when the information is converted from the analog to the digital domain.
The setup depicted in figure 4.1 shows the "Ideal sampler", a block that is attached at the output of the analog block of the circuit to address the SNR at the moment of the decision made by the comparator. When V_{sample} is high, the switch is closed and the voltage is stored immediately on C_S, because the switch is ideal and possesses no resistance; this voltage is effectively the piece of information that should be extracted, and should be compared with the noise power to evaluate the SNR.

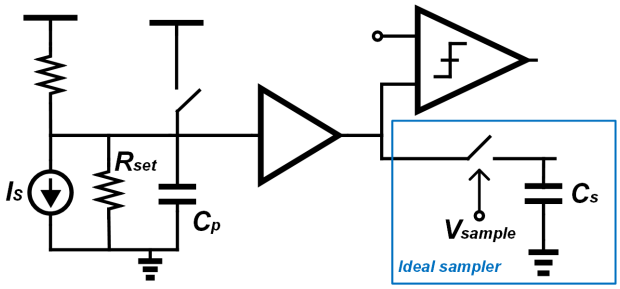


Figure 4.1: Setup for simulating the output SNR

The noise is referred at the same node using the PSS and PNoise analysis in Cadence Virtuoso using the simulators Spectre and SpectreRF, since the circuit is ideally imagined to be working at a regime of one spin reading per μs. This type of analysis comes handy because it also takes into account the noise folding of the intrinsic sampling nature of the comparator action.
The noise calculated is integrated all over the bandwidth and the SNR is calculated as

$$SNR = \frac{|V_{sampled} - V_{threshold}|^2}{\int_{1Hz}^{\infty} N_{out}^2 df} \tag{4.1}$$

It is currently not allowed to run any simulation in Cadence Virtuoso at a temperature below $-40°C$, this temperature is therefore used throughout the design process while qualitatively taking into account the CT side-effects.

4.1 Transistor-level design

In this section, the transistor-level design of the single blocks composing the readout chain is discussed. An overview of the system architecture can be seen below:

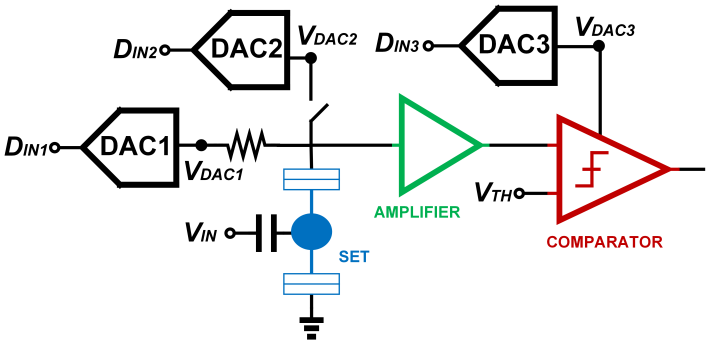


Figure 4.2: High-level view of the frontend

The circuit behaves as follows: the spin information, encoded in a voltage pulse at the gate of the SET, is first amplified and then compared to a threshold to decide whether the outcome is spin up or spin down; after each decision, all the capacitors that experience integration are reset to a constant potential using transmission gates as switches. The DACs serve to select the bias currents and voltages throughout the circuit.

4.1.1 Amplifier

The most critical block of the system is the frontend amplifier, whose purpose is to enhance the signal swing enough for the comparator to make the correct decision. In particular, the swing should be maximized to avoid two scenarios:

- the threshold voltage cannot be tuned finely enough to have equal SNR for the two symbols.
- the input referred noise of the comparator limits the performance.

As discussed in chapter 3, using a Voltage Amplifier as frontend amplification stage is the most promising way of achieving a readout with the target BER.
Considering that the signal at the drain of the SET is expected to be $\simeq 30\,\mu$V, a gain of approximately 100 would be sufficient to satisfy the aforementioned requirements. To achieve this gain, two amplification stages are employed: the first, more critical for noise, consists of an NPN-based Common Emitter stage, while the second one is a source degenerated pMOS-based Common Source stage. The amplifier is shown in figure 4.3.

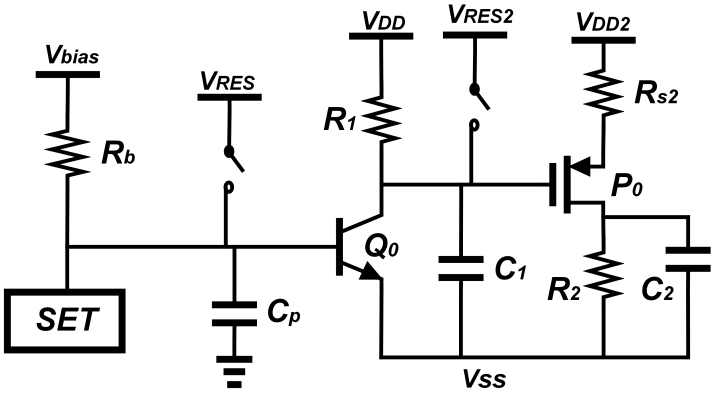


Figure 4.3: Amplifier schematic

A noise analysis is carried out for the first stage in order to identify the best operating region

Passive	Value	Passive	Value
R_b	1 MΩ	R_{s2}	100 kΩ
R_1	100 kΩ	R_2	1 MΩ
C_1	3 pF	C_2	100 fF

Table 4.1: Values of passives in the amplifier schematic of figure 4.3

for the NPN to produce the least noise possible compared to the signal swing. The main noise sources are listed below and shown in figure 4.4

- $I_{ns} = 2qFI_s$: SET shot noise
- $V_{nf,npn} \simeq K_1 \frac{I_b^\alpha}{f}$: NPN flicker noise
- $I_{nb} = 2qFI_b$: NPN base shot noise
- $I_{nc} = 2qFI_c$: NPN collector noise
- $V_{nf,mos} = K_2 \frac{I_{ds}^\theta}{f}$: pMOS flicker noise
- $V_{nch} = 2qFI_{ds}$: pMOS channel shot noise

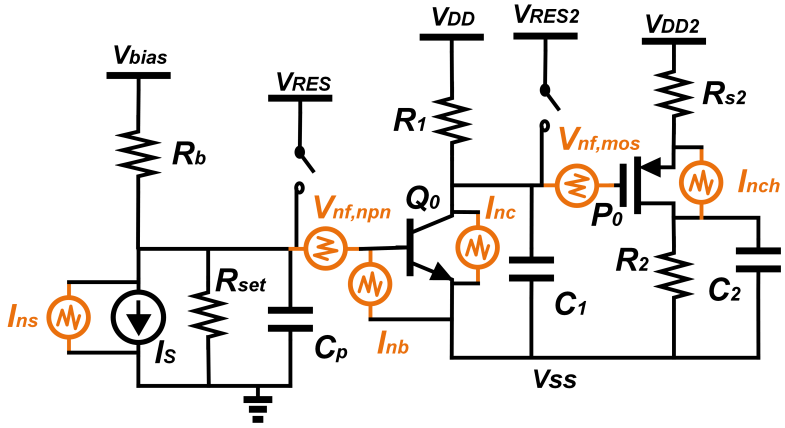


Figure 4.4: Amplifier noise sources

The total output-referred noise can be calculated using the specific transfer functions from each source to the output node. A simplified small signal model is used to perform this kind of analysis; here the noise of the second stage is also neglected, because it is divided by the gain of the first stage and doesn't impact much the final result. Therefore, in the following analysis the output of the first node will be treated as the output of the circuit.
In this model, the small signal parameter g_m is substituted with $g_m/I_c \times I_c$ in order to address the inter-dependency of the noise sources and the gain of the circuit.

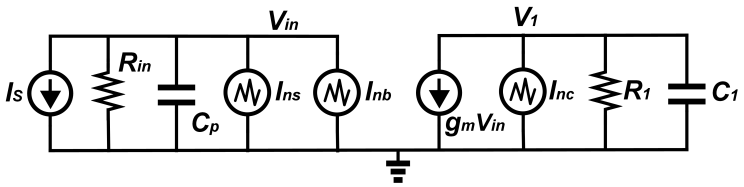


Figure 4.5: ss model of first amplification stage with noise sources

The flicker noise of transistors is neglected for simplicity. In any case, their magnitude is not significant compared to the other sources if the transistors are sized properly, being K_1 and K_2 inversely proportional to their size.
The shot noise from the SET and the base of the bipolar can be first converted in voltage and then referred to the output with the total gain of the amplifier. Considering R_{set} SET equivalent resistance, r_π small signal input NPN resistance, R_b bias resistance and $R_{in} = R_{set}//R_b//r_\pi$:

$$Z_{in}(s) = \frac{R_{in}}{1 + sC_pR_{in}} \tag{4.2}$$

The NTF for these sources is equal to the STF:

$$NTF_1(s) = STF(s) = \frac{V_{out}}{I_{in}}(s) = Z_{in}g_{m1}Z_1 \tag{4.3}$$

where $Z_1(s) = \frac{R_1}{1+sC_1R_1}$ is the output impedance of the first stage and g_{m1} is the NPN small signal transconductances.
The collector shot noise can be referred to the input as well if divided by g_{m1}, and therefore its NTF is just $\frac{NTF_1(s)}{g_{m1}Z_{in}}$. The total output noise PSD can be approximated as:

$$V^2_{n,out}(s) = \left[(I^2_{nb} + I^2_{ns}) \left(\frac{R_{in}}{1 + sC_pR_{in}} \right)^2 + \frac{I^2_{nc}}{g^2_{m1}} \right] \left(\frac{g_{m1}R_1}{1 + sR_1C_1} \right)^2 \tag{4.4}$$

With the (reasonable) assumption that $C_pR_{in} \approx C_1R_1 = \tau$, the noise PSD becomes

$$V^2_{n,out}(s) = \left(I^2_{nb} + I^2_{ns}\right) \left(\frac{R_{in}g_{m1}R_1}{(1 + sC_pR_{in})^2} \right)^2 + I^2_{nc} \left(\frac{R_1}{1 + sR_1C_1} \right)^2 \tag{4.5}$$

It is clear that base and SET shot noise experience the same TF of the signal, therefore no optimization on the SNR can be done by taking action on these sources except changing the OP of the SET and the base current of the NPN. The g_m of the transistors is proportional to the bias current but so are the noise sources, therefore it is not immediately clear what is the best current choice for the SNR.
In order to find the integrated noise, equivalent noise bandwidths (ENBW) should be used. For a generic filter TF the ENBW is by definition [77]:

$$\omega_{ENBW} = \int_0^\infty \left| \frac{H(j\omega)}{H_{max}} \right|^2 d\omega \tag{4.6}$$

For a $H_1 = \frac{R_1}{1+j\omega\tau}$, this is equal to $\omega_{ENBW1} = \frac{\pi}{2\tau}$. For a second order low pass filter $H_2 = \frac{R_{in}g_{m1}R_1}{(1+sC_pR_{in})^2}$ it is

$$\omega_{ENBW2} = \int_0^\infty \left| \frac{1}{(1 + j\omega\tau)^2} \right|^2 d\omega = \frac{\pi}{4\tau} \tag{4.7}$$

On the other hand, the signal at the output (time domain), is approximately

$$V_{out} = I_sR_{in} \left(1 - e^{-\frac{T_b}{R_{in}C_p}} \right) \times g_{m1}R_1 \tag{4.8}$$

As a consequence, the SNR can be written as

$$SNR = \frac{V^2_{out}}{V^2_{n,out,int}} = \frac{\left(I_sR_{in}(1 - e^{-\frac{T_b}{R_{in}C_p}}) \times g_{m1}R_1 \right)^2}{\left(I^2_{nb} + I^2_{ns}\right)\omega_{ENBW2}(R_{in}g_{m1}R_1)^2 + I^2_{nc}R^2_1\omega_{ENBW1}} = \tag{4.9}$$

$$= \frac{\left(I_sR_{in}(1 - e^{-\frac{T_b}{R_{in}C_p}}) \times g_{m1} \right)^2}{\left(\left(\frac{I^2_{nb}+I^2_{ns}}{2} \right)(R_{in}g_{m1})^2 + I^2_{nc} \right) \frac{\pi}{2R_{in}C_p}} = \tag{4.10}$$

$$= \frac{2I^2_sC_pR_{in}(1 - e^{-\frac{T_b}{R_{in}C_p}})^2 g^2_{m1}}{\pi \left(\left(\frac{I^2_{nb}+I^2_{ns}}{2} \right)(R_{in}g_{m1})^2 + I^2_{nc} \right)} \tag{4.11}$$

From this expression it can be seen that, if the collector current dominates the overall noise, increasing the input resistance and the input current directly causes the SNR to rise. In order to find the optimum bias current, the noise sources are rewritten as function of I_C.

$$SNR = \frac{2I_s^2 C_p R_{in}(1-e^{-\frac{T_b}{R_{in}C_p}})^2 g_{m1}^2}{2q\pi\left(\left(\frac{I_B+I_{s,bias}+I_s/2}{2}\right)(R_{in}g_{m1})^2 + I_C\right)} \tag{4.12}$$

Considering that the transconductance and the base current are also functions of the collector current as per $\gamma = \frac{I_B}{I_C}$ and $\alpha = g_{m1}/I_C$:

$$SNR = \frac{I_s^2 C_p R_{in}(1-e^{-\frac{T_b}{R_{in}C_p}})^2 \alpha^2 I_C^2}{q\pi\left(\left(\frac{\gamma I_C+I_{s,bias}+I_s/2}{2}\right)(R_{in}\alpha I_C)^2 + I_C\right)} \tag{4.13}$$

Looking for the maximum SNR with respect to the collector current means solving $\frac{\partial SNR}{\partial I_C} = 0$, or equivalently

$$\frac{\partial\left(\frac{I_C^2}{\left(\left(\frac{\gamma I_C+I_{s,bias}+I_s/2}{2}\right)(R_{in}\alpha I_C)^2+I_C\right)}\right)}{\partial I_C} = 0 \tag{4.14}$$

The solution of this equality is given by

$$2I_C\left[I_C + I_C^2(R_{in}^2\alpha^2(I_{s,bias}/2 + I_s/4))\right] + I_C^3\left[R_{in}^2\alpha^2\gamma/2\right] - \tag{4.15}$$

$$+I_C^2\left[1 + I_C(2R_{in}^2\alpha^2(I_{s,bias}/2 + I_s/4)) + I_C^2(\frac{3}{2}R_{in}^2\alpha^2\gamma/2)\right] = 0 \tag{4.16}$$

which solving for I_C gives as a result

$$I_{C,opt} = \frac{2\sqrt{2}}{R_{in}\alpha\sqrt{|\gamma|}}\,,\ \gamma < 0 \tag{4.17}$$

The first order approximation of the SNR shows that there is an optimum bias collector current, dependent mostly on the device transconductance efficiency and the input resistance. Substituting $R_{in} \approx 133\,\text{k}\Omega$, $\alpha = 50$ at T_{sim} (will change at cryo, as discussed in the next section) and $\gamma \approx 1\times10^{-3}$, then $I_{C,opt} = 13.45\,\mu\text{A}$.
After simulating this configuration, the optimum bias current is found to be around $10\,\mu\text{A}$, a value that does not deviate too much from the calculated one. Since the power budget is limited and the SNR is almost unaffected also for lower current, the bias current is chosen to be $7.5\,\mu\text{A}$.

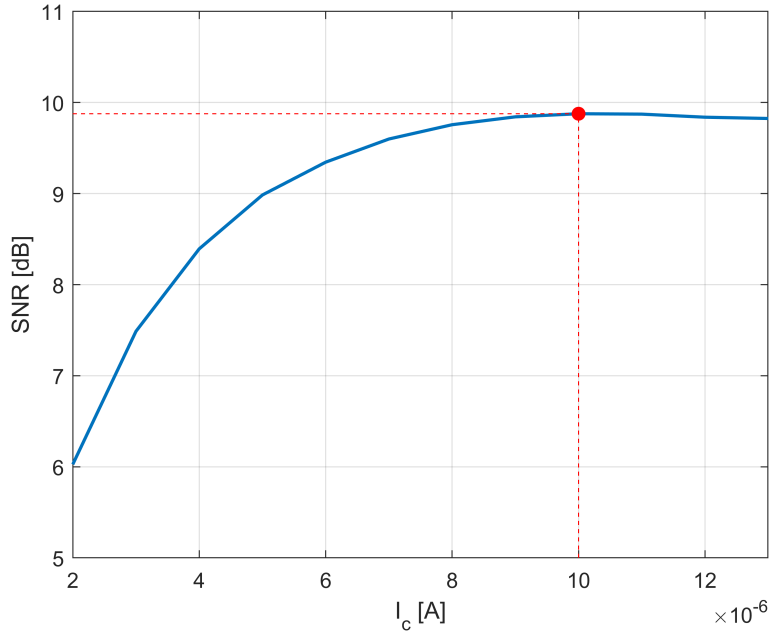


Figure 4.6: Approximation of the optimum current for SNR

The size of Q0 can be the minimum of $E_A = 0.07 \times 1\,\mu\text{m}$ because of its low flicker noise. However, in order to decrease the sensitivity of the OP with respect to the bias DAC1 (whose output is also an NPN minimum size) and its noise contribution, Q0 is realized with $M_{Q0} = 10$ transistors in parallel. To ensure the wanted current, Q0 is then biased with $V_{BE} = 745\,\text{mV}$. With this given value of current and a load resistance R_1 of $100\,\text{k}\Omega$, the supply of the first stage can be a bit lower of what discussed in the previous chapter, in that $V_{DD1} = 1\,\text{V}$ is possible and still $V_{CE,Q0} > 200\,\text{mV}$. The required $V_{BE,Q0}$ dictates the V_{SS}. Considered that $V_{DS,SET} \approx 1\,\text{mV}$, the V_{SS} needs to be shifted about $750\,\text{mV}$ lower than the source of the SET if the source is considered to be the reference of the circuit (this is arbitrary, could be the opposite as well). The same supply is shared with the current DACs and the comparator. To ensure the desired $V_{BQ0} = V_{D,SET}$, the DAC1 provides a bias current through R_b which can be adjusted using a digital code. R_b serves as current path for the excess base current of Q0; without R_b the bias point of the amplifier cannot be adjusted separately from the SET because the condition $I_{B,Q0} = I_{SET}$ would be imposed.

Regarding the second stage, it is much less important which bias current is selected in that the noise of P0 will be divided by the gain of the first stage. The transistor is sized just such that its flicker noise is below an appreciable level, leading to the choice of $W/L = 7\,\mu\text{m} \times 3.5\,\mu\text{m}$. Moreover, the integration will result in a large excursion at the output node, making a small signal model analysis useless for this stage.
The source voltage V_{DD2} is chosen such that at the reset time P0 is off, while at the sampling moment it just started conducting. This is done to limit the power consumption; if the integration makes the V_{GS} grow too much, several μA may start flowing into P0. This much current is not desired for P0 because only a small gain is required at this stage.
The resistive source degeneration R_{s2} is added in order to mitigate the effects of PVT variation and the PSRR, in that if the DC voltage at the sampling moment ($\frac{|V_{out[0]}+V_{out[1]}}{2}$) changes, then the threshold needs also to be calibrated accordingly. Despite this precaution, shift of DC sampling voltage is still a real risk, as it will be addressed in section 4.1.7.

In order to filter as much collector shot noise as possible, the pole of the output of the first stage is also kept around the same value of the input pole adding $C_1 = 3\,\text{pF}$, meaning that also this node experience integration. For this reason reset is also implemented here, with a reset voltage such that at the reset moment $V_{CE,Q0} = 200\,\text{mV}$. For the same reason of filtering channel noise of P0, $C_2 = 100\,\text{fF}$ is employed at the output of the second stage; to make the noise from P0 negligible it is just enough to keep this pole near $1\,\text{MHz}$, hence this node tracks perfectly the output

of the first stage at f_{symbol} and no reset is needed here. Overall, the system presents 3 poles: $f_{pin} \approx f_{p1} = 600\,\text{kHz}$ and $f_{p2} \approx 1.5\,\text{MHz}$.

4.1.2 Cryo-RT considerations

As discussed in section 2.4, a shift in the characteristics and some additional effects have to be considered when the system operates at cryogenic temperatures. The most important aspects that will affect the performance of the circuits are the (almost) complete absence of thermal noise and increased g_m/I of the transistors. The thermal noise of resistor is therefore manually removed in simulation, being considered negligible in the practical application. The total noise produced by the circuit is strongly dependent on the bias current of the first amplification stage, therefore it is necessary to know how the modified gm efficiency impacts the choice of the bias current.

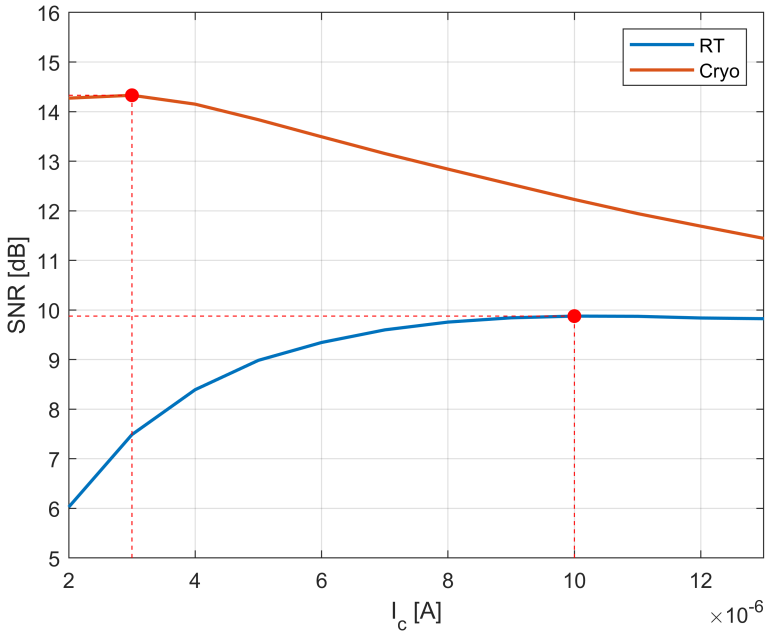


Figure 4.7: Optimum current at CT vs RT. This simulation mimics the CT condition by means of the different transconductance efficiency, taken from plot 2.23

From measured g_m of the SiGe HBT [15], the expected efficiency at $T = 4K$ is $g_m/I_c \approx 200$, four times larger compared to the value of 50 provided in simulations at $T = -40°C$. As can be seen from equation 4.17, this should result in an optimum current which is much smaller and should be taken into account when deciding on the range of the bias DACs. The same small signal model introduced in the previous section is simulated with the different value of g_m: the result of this simulation is shown in figure 4.7 and confirms that at CT $I_{C,opt} = 2.5\,\mu\text{W}$, meaning a more low power design is possible.

4.1.3 Comparator

The comparator is designed as the cascade of a pre-amplification stage and a latch. The more canonical Strong-ARM configuration is avoided due to the kickback voltage that would otherwise compromise the decision.

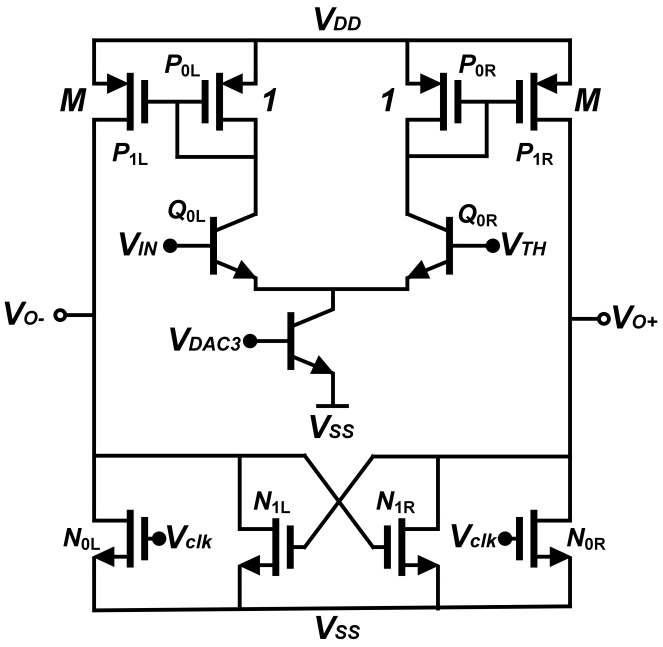


Figure 4.8: Comparator circuit. The transistors are all minimum size, in that the previous amplification is enough to suppress all flicker noise

The bias current is controlled with a DAC: as a result, the same current source of the other two DACs can be used while maintaining full control over the current in the comparator. In particular, $I_{COMP,tail} = 100nA$ is enough to guarantee the functionality of the block while minimizing the power consumption. The upper supply can be shared with the DACs and the first stage amplifier, hence $V_{DD,COMP} = V_{DD1} = V_{DD} = 253\,\text{mV}$, while $V_{SS,COMP} = -1\,\text{V}$. The difference between the supplies is $\approx 1.25\,\text{V}$.
The input referred noise of the comparator should be calculated in order to gain insight about the needed signal swing at the moment of the decision, although it is not trivial to evaluate the noise and the gain of a highly non-linear block. It is possible to simulate the outcome probability curve for different input voltages, as described in [78] and by the ADC verification manual (Rapid-Adoption-Kit, RAK) from Cadence, by running a transient noise analysis.
An input DC voltage source is attached at the input of the comparator, and its voltage is swept between $V_{TH}-2\,\text{mV}$ and $V_{TH}+2\,\text{mV}$ with a step of $100\,\mu\text{V}$ (in that the standard deviation of the noise is expected to be about this value). For each voltage, the comparator is left making decisions for 100 periods. Each decision has weight $\pm 1.25\,\text{V}$ based on the decision. The outcome of the 100 runs is averaged and this is done for each input voltage. The result is visible in figure 4.9. For the input approaching the threshold, the probability of error is higher and therefore the average of the outcomes is not close to the supplies anymore. This curve can be used to evaluate the input-referred noise (IRN) of the comparator. Before doing that, it is noted that the error probability curve is not centered around the threshold ($v_{in} = 0$ in the plot), so there is an offset (vertical dashed red line) that has to be compensated for the calculations: as per figure 4.10, this offset is about $V_{in,off} = -39.5\,\mu\text{V}$. The curve in figure 4.9 is normalized between 0 and 1 in order to be compared to a normal distribution, using the transformation

$$Ao(i) = (Ao(i) + 1.2)/2.4 \tag{4.18}$$

where each i correspond to an input voltage. Eventually, the curve Ao(i) (Average outcomes) is now a probability function with mean equal to 0 and standard deviation ($\sqrt{\sigma} = IRN$) that can be obtained as:

$$IRN(i) = \sqrt{2} \times \frac{(V_{in}(i) + V_{in,off})}{NORM_{INV}(Ao(i))} \tag{4.19}$$

and plot in figure 4.11 The average of these values shows that the standard deviation of the input-referred noise of the comparator is $IRN = 280.5\,\mu\text{V}$.

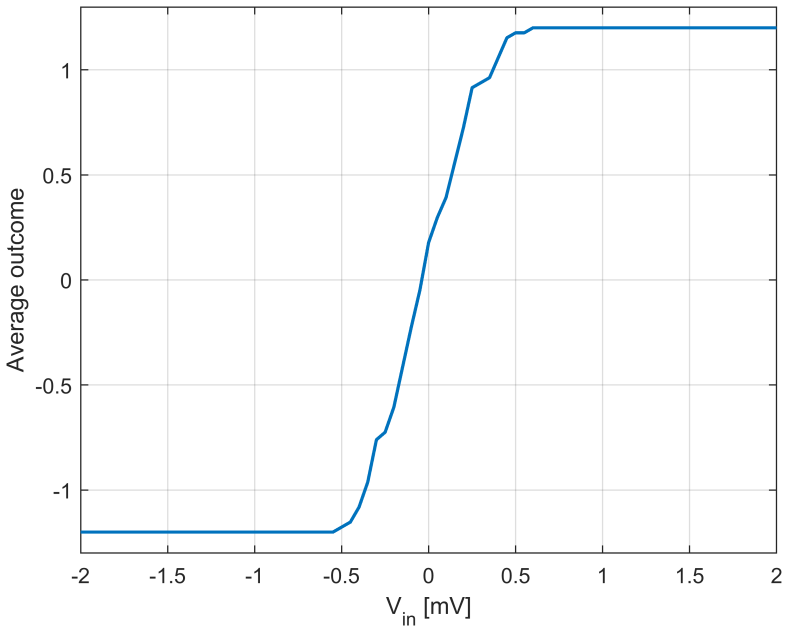


Figure 4.9: Average outcome for different voltages at the input of the comparator. Each outcome is the result of averaging 100 measurements (each measurement can be either $1.2\,\mathrm{V}$ or $-1.2\,\mathrm{V}$)

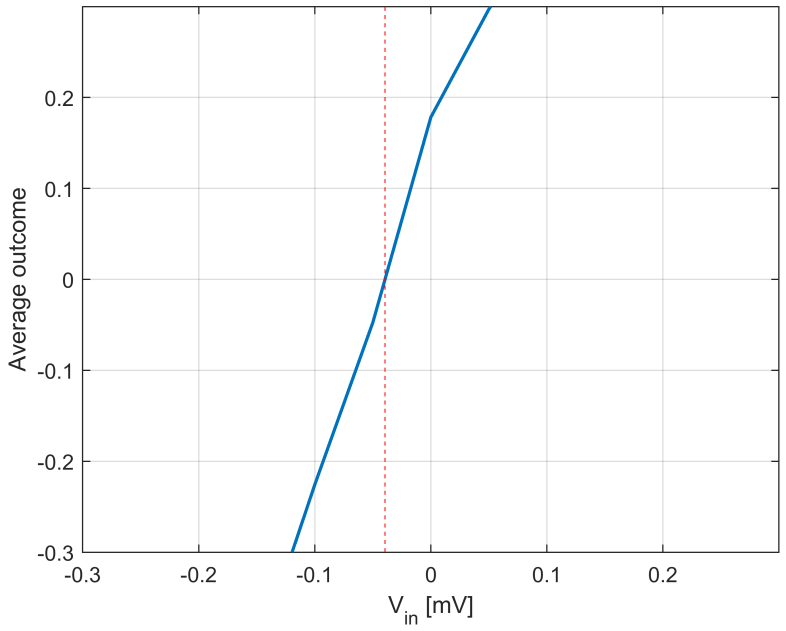


Figure 4.10: In the ideal case, the average outcome is 0 for $V_{in} = V_{TH}$; this result on the other hand shows that the comparator has an offset of is $-39.5\,\mu\mathrm{V}$

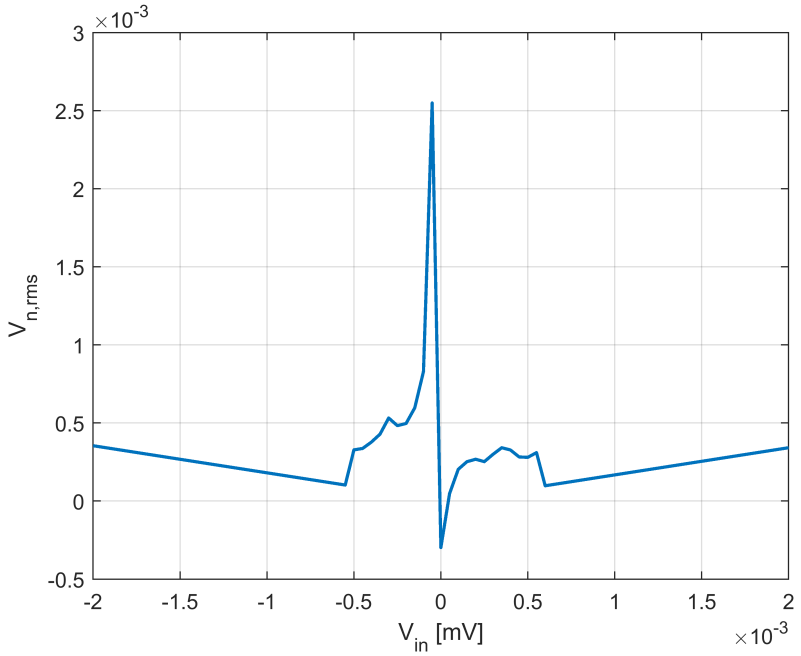


Figure 4.11: From the inverse of the NORM function, the $\sqrt{\sigma}$ can be retrieved for each input voltage. It is equivalent in this case to talk about IRN, $\sqrt{\sigma}$ and $V_{n,in,rms}$. The IRN is estimated as the average value of the measured $IRN(i)$

As it will be shown in section 4.1.5, the total integrated noise at the input of the comparator produced by the rest of the circuit is $V^2_{n,int} = 414 \times 10^{-9}\,\mathrm{V}^2$, with an output signal of $V_{o,rms} = 1.936\,\mathrm{mV}$. Since $V^2_{n,in,rms,comp} = IRN^2 = 78.7 \times 10^{-9}\,\mathrm{V}^2$ and $V^2_{n,int} >> V^2_{n,in,rms,comp}$, it can be concluded that the comparator affects only slightly the SNR ($\sim 0.4\,\mathrm{dB}$) at T_{sim}. However, considering that the output swing is expected to increase at CT, then also the noise introduced by the comparator becomes totally negligible. If for some reason the measured output swing will be lower than what expected in simulations, another amplification stage (or increasing the current in the second stage) will be required to remove any appreciable noise from the comparator.

4.1.4 Current DACs

Three current Digital-to-Analog Converters are implemented in the frontend: two of them provide the bias voltages for the amplifier's input stage, while the third one, smaller, controls the bias current of the comparator.
The structure of the first current DAC can be observed in figure 4.12. It implements an 8-bit binary structure with 255 PMOS in parallel. The flow of current is controlled through a digital code that turns on or off the designated switches. All the current branches are summed into the output branch, where the current is translated into voltage through a diode-connected NPN. The NPN is preferred over a NMOS due to its low flicker noise. The DAC2 is realized in the same way, and its output voltage is used as reset voltage for the input node.

Current Programming Accuracy[4]

Range	Programming resolution	Accuracy (1 year) 23°C ± 5°C ± (% rdg.+amps)	Typical noise (peak-peak) 0.1Hz-10Hz
100.000nA	2pA	0.06% + 100pA	5pA
1.00000µA	20pA	0.03% + 800pA	25pA
10.0000µA	200pA	0.03% + 5nA	60pA
100.000µA	2nA	0.03% + 60nA	3nA
1.00000mA	20nA	0.03% + 300nA	6nA
10.0000mA	200nA	0.03% + 6µA	200nA
100.000mA	2µA	0.03% + 30µA	600nA
1.00000A[2]	20µA	0.05% + 1.8mA	70µA
1.50000A[2]	50µA	0.06% + 4mA	150µA
10.0000A[2,5]	200µA	0.5% + 40mA	

Temperature coefficient (0°C–18°C and 28°C–50°C): ±(0.15 × accuracy specification)/°C.

Maximum output power and source/sink limits:[2] 30.603W per channel maximum. ±1.515A at ±20.2V, ±101mA at ±202V, four-quadrant source or sink operation.

Current regulation: Line: 0.01% of range. **Load:** ±(0.01% of range + 100pA).

Voltage limit/compliance:[6] Bipolar voltage limit (compliance) set with a single value. Minimum value is 10mV. Accuracy same as voltage source.

Figure 4.13: System SourceMetre series 2600 specifications as current source

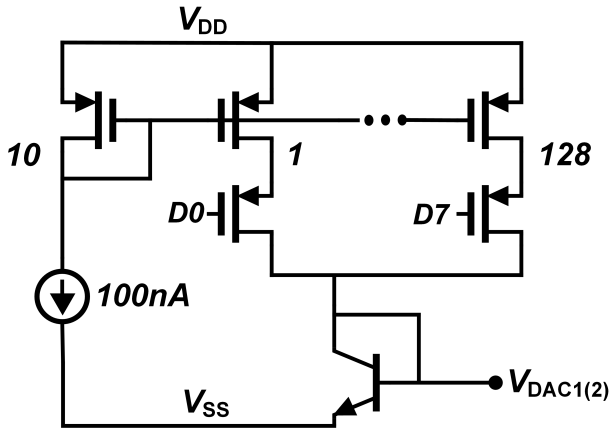


Figure 4.12: Schematic of DAC1 and DAC2

The current is sourced from outside the chip using a Keithley System SourceMetre series 2600, able to provide $(100 \pm 0.002)nA$.
The required minimum step is calculated considering two important factors: shift of bias voltages at cryogenic temperature and PVT variations. As it was already shown, the expected optimum bias current to maximize the SNR shifts down from $7.5\mu A$ to approximately $2.5\mu A$. While the current should be adjusted at cryo (as shown in table 4.2), the voltages must remain the same not to hinder the operation of the SET, which is directly coupled to the amplifier. For this reason, three knobs should be tuned together: V_{DAC1}, V_{DAC2} and V_{SS}.

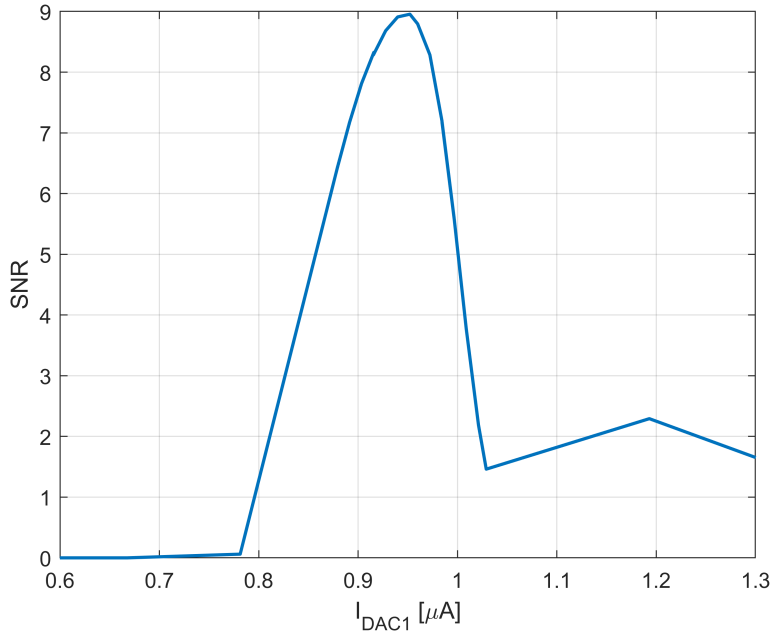


Figure 4.14: SNR vs bias current from DAC1

	$V_{SS,amp}$ $[V]$	I_{dac1} $[nA]$	I_{dac2} $[nA]$	$I_{C,bias}$ $[\mu A]$
T_{sim} Design	-0.747	1200	750	7.5
CT Design	-0.722	250	200	2.2

Table 4.2: tuning knobs to fix the bias current in the amplification stage; values to switch from the $-40\,^{\circ}\mathrm{C}$ optimum I_C to the CT optimum I_C

The SNR of the readout with respect to the two DAC's currents is simulated and shown in 4.14 and 4.15: a minimum step of $10nA$ is a safe choice to be sure that the amplifier can be biased in the optimum OP for SNR while maintaining the SET in the same state of operation. $I_{DAC1,2}$ directly set $V_{DAC1,2}$ through the I-V characteristics of the NPN. V_{DAC2} sets the reset voltage at the input, hence I_{DAC2} affects a lot the reset swing that the drain of the SET has to sustain, as shown in figure 4.16. On the other side, a large number of bit is needed because the system is quite sensitive to Montecarlo variation; as it will be explained further in section 4.1.7, to restore the desired bias point from the worst-cases montecarlo simulations, a shift in current of approximately $1.5\mu A$ might be needed. The result is a current DAC with the following characteristics:

- 8-bits resolution
- 10 nA minimum step, obtained with a factor 10 step-down from the outside current source $I_0 = 100\,\mathrm{nA}$
- range from 0 to $2.55\,\mu\mathrm{A}$

The second and third DACs make use of the same structure; DAC2 in particular is the same as DAC1, while DAC3 is smaller and counts only 3-bits and a range of currents from 0 to $3I_0$ with a step of $I_0/5$.
Flicker noise of the input PMOS can start dominating the total output noise, therefore all the PMOS are sized minimum width ($150nm$, because this scales exponentially for more significant bits) but maximum length ($10\mu m$).

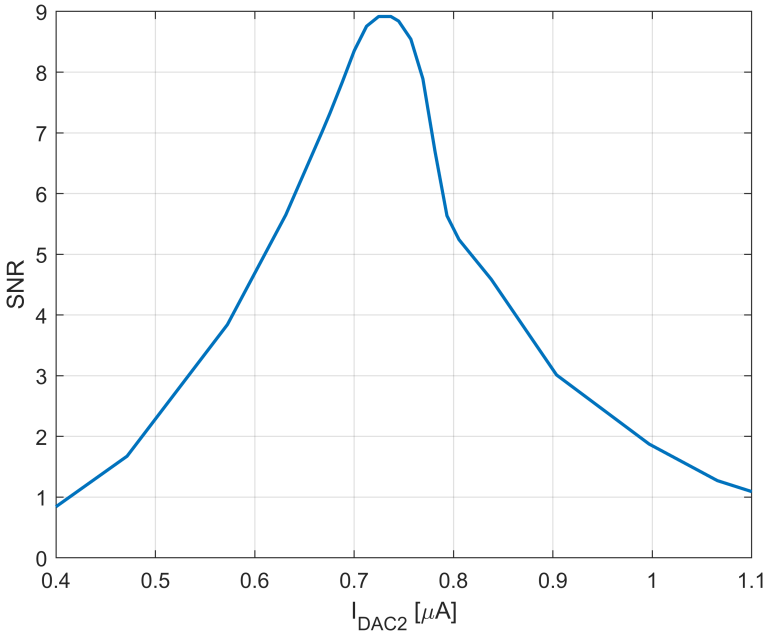


Figure 4.15: SNR vs bias current from DAC2

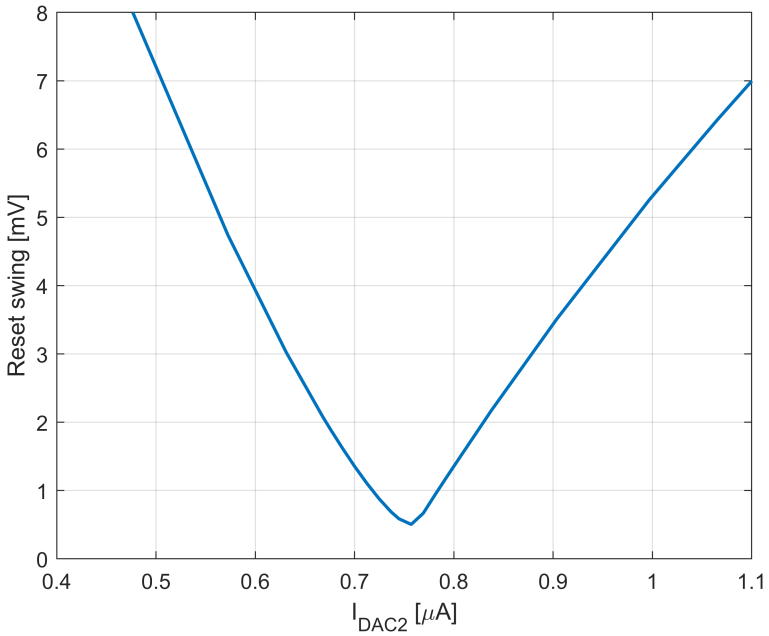


Figure 4.16: Reset swing vs bias current from DAC2

Noise source	Contribution percentage [%]	Integrated output noise [V^2]
$I_{n,C,Q0}$	41.95	1.20×10^{-7}
$I_{n,B,Q0}$	25.64	7.32×10^{-8}
$I_{1/f,Pdac1}$	7.30	2.08×10^{-8}
$I_{n,CH,P0}$	7.09	2.02×10^{-8}
$I_{n,set}$	6.16	1.76×10^{-8}
$I_{n,C,Qdac1}$	2.49	7.10×10^{-9}
$I_{n,C,Qdac2}$	2.30	6.56×10^{-9}

Table 4.3: Simulated noise contributions

4.1.5 Schematic simulations results

Once the schematic level design is completed, the performance is addressed in simulations. The SNR, the operating frequency and the power consumption are the main results of interest.
In figure 4.17 is possible to observe the evolution in time of the voltages at the main nodes of the amplifier. In these waveforms, the information is located only in the voltages at the time instant when the comparator performs sampling at its input. For this reason, the actual useful amplitude (referred here as "signal swing") which is compared to the noise power is just the difference between a '1' and a '0', in figure 4.17 denoted by two consecutive dots. The output RMS value is then half of this swing, $V_{out,rms} = 1.936\,\text{mV}$. The swing that the input node experience due to reset is about $500\,\mu\text{V}$, while the rest is due to the input signal.
In case of a random symbol sequence, the same symbol can be repeated many times in a row, effectively causing the input frequency to be lower than $1\,\text{MHz}$. As mentioned in section 3.3.3, this means that any bandpass TF would cut part of the possible signal, making the SNR function of the input code. The system is tested for a random sequence and for repeated code, as shown in figure 4.18. The worst case SNR (less output swing) holds for the case where a transition between a 0 and 1 is experienced at the input; therefore, the SNR can only improve respect to what has already been calculated for $f_{symbol} = 1\,\text{MHz}$.
The actual signal swing at each node allows to evaluate what is the actual gain of the two stages:

- $A_1 = 32.8$
- $A_2 = 3.9$
- total gain $A = 130$

The output voltage V_2 is compared to a threshold at the sampling moment; the output of the comparator (and of the overall readout) for different input symbols is shown in figure 4.19. The main noise sources are listed in table 4.3 ranked from the highest to the lowest: as expected, the collector and base shot noise of the input bipolar dominate the overall output noise. The total integrated noise output-referred of the entire circuit is $V^2_{n,out,int} = 414 \times 10^{-9}\,\text{V}^2$.
The SNR, that in this simulation is really just an estimation and depends strongly on the real SET available at the input, is simulated to be $9.3dB$ at room temperature, with the potential to increase by three to five dB below 4K. It is calculated using

$$SNR = 10log_{10}\frac{V^2_{out,rms}}{V^2_{n,out,int}} = 10log_{10}\frac{(V_{out}/2)^2}{V^2_{n,out,int}} \tag{4.20}$$

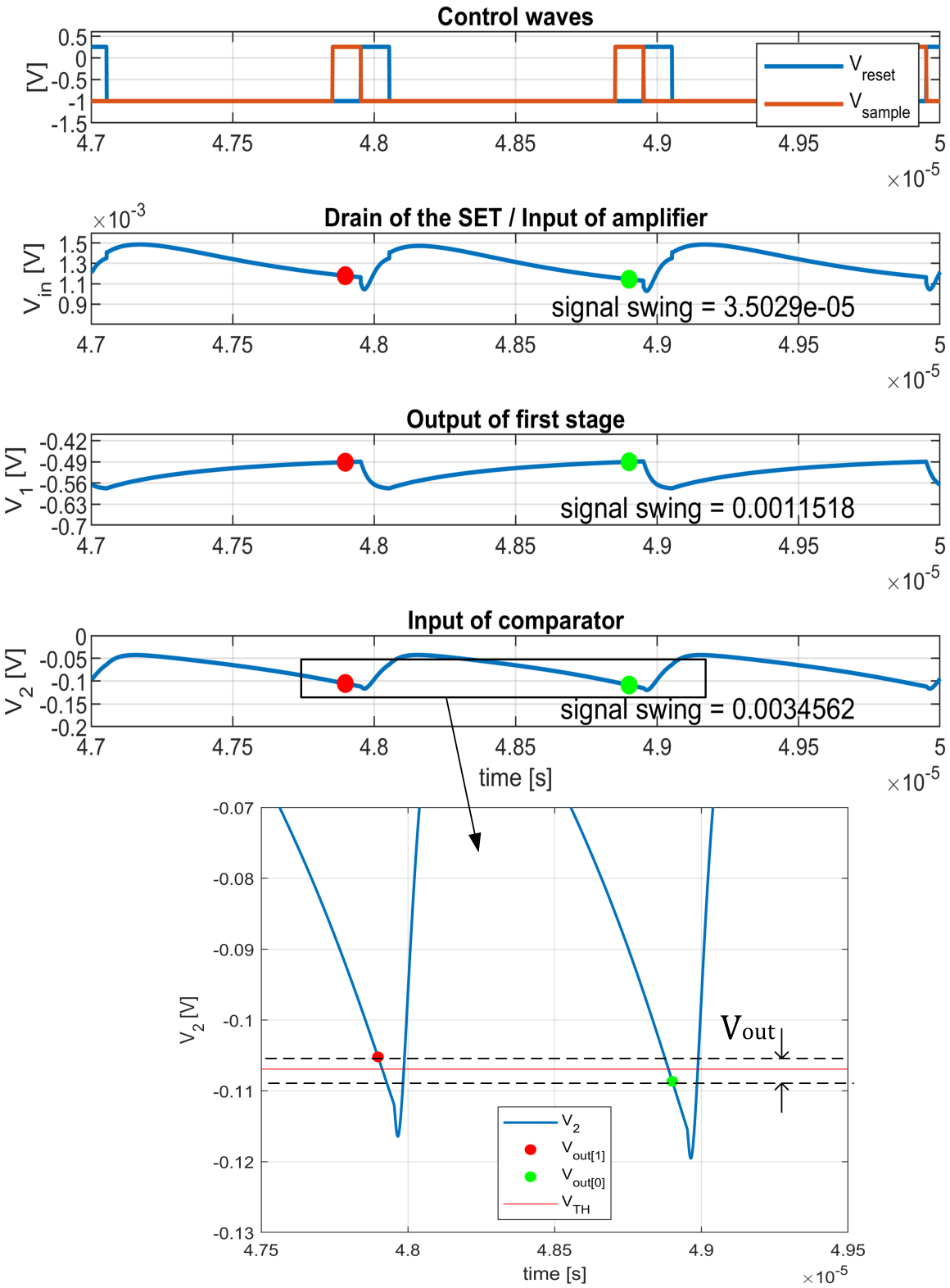


Figure 4.17: Control signals for the readout sequence and waveforms for the two symbols. When V_{reset} is high, the capacitors at every node are reset, and the SET is initialized at its maximum sensitivity point. When V_{reset} goes low, tunneling is favoured and happens almost instantaneously, as discussed in section 2.2.1, and the integration of the input current starts. When V_{sample} goes high the comparator discerns between a 0 and a 1 and the digital value is available at the output until the next reading. The dots indicate the sampling moments, when the comparator is turned on and the decision is made

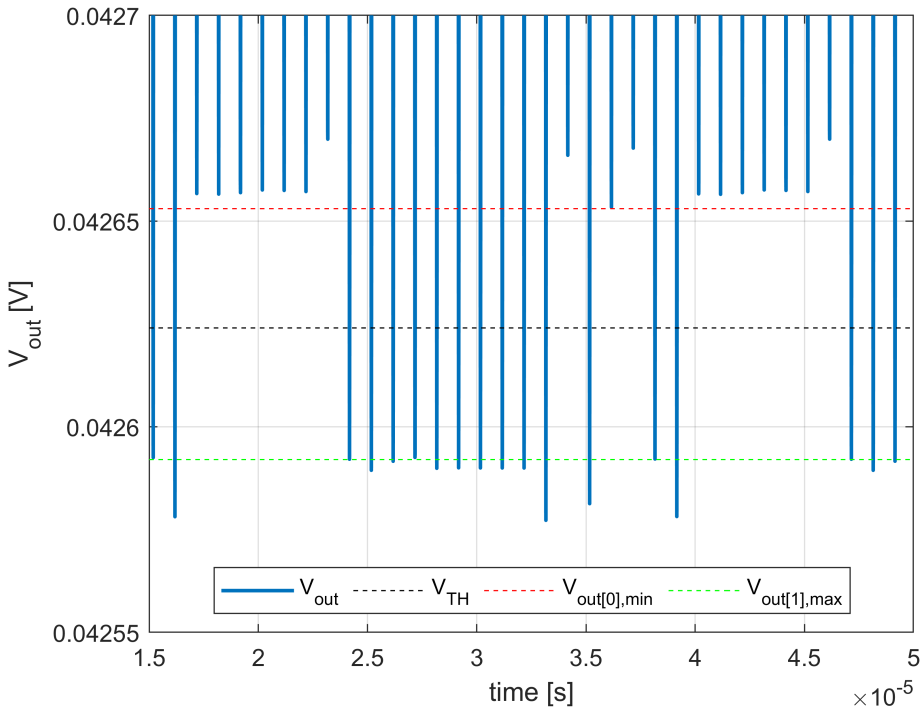


Figure 4.18: Output of the amplifier (V_2) for a possible example input sequence of bits. Note that the output signal lines look vertical because the time axis is stretched for many reading time windows

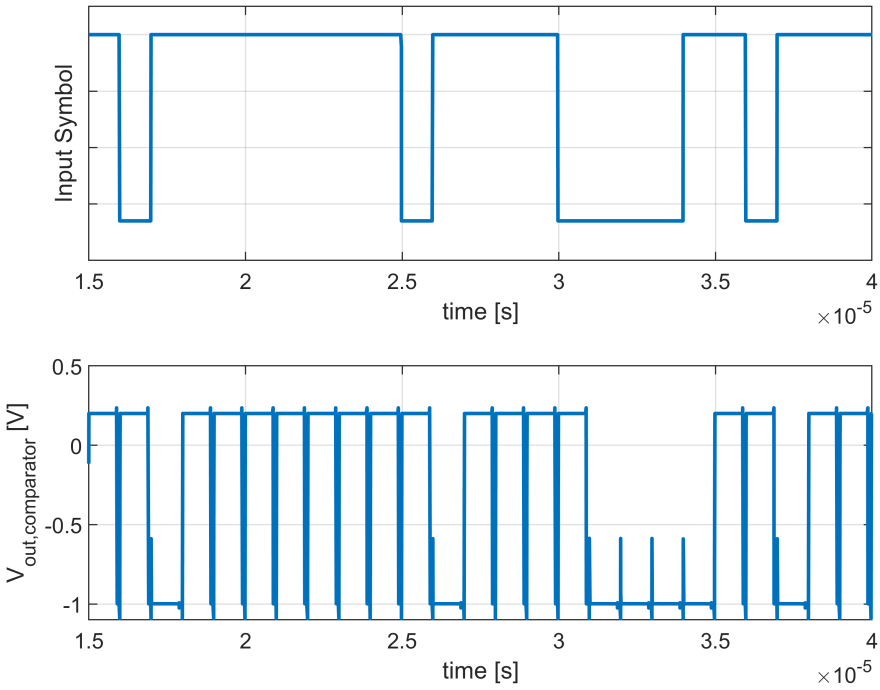


Figure 4.19: Output of comparator for a random input symbol sequence

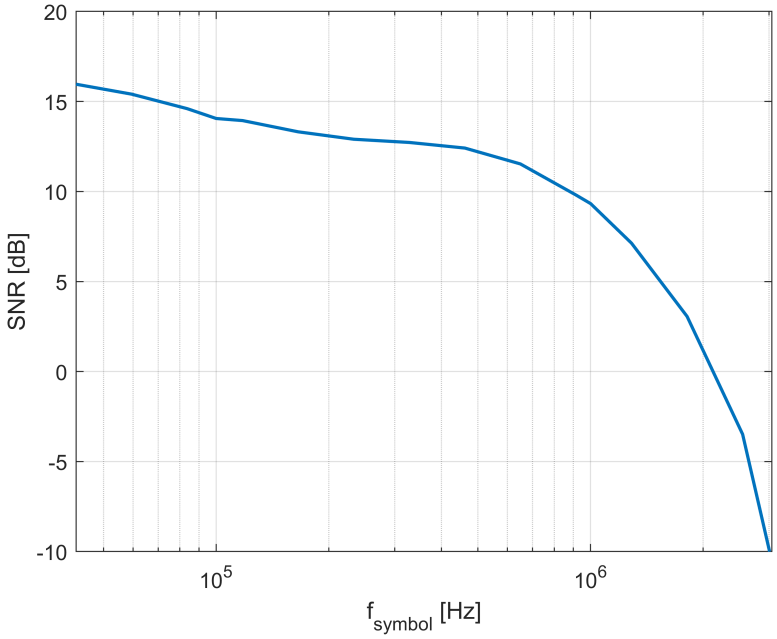


Figure 4.20: SNR vs operating frequency

The SNR is plot against the operating frequency in 4.20.
The estimated power consumption at T_{sim} is calculated as

$$\begin{aligned} P_{tot} &= P_{DACs} + P_{AMP} + P_{COMP} \simeq \\ &= (I_{DAC1} + I_{DAC2}) \times (V_{DD} - V_{SS}) + I_{C,Q0,rms} \times (V_{DD} - V_{SS}) + \\ &+ I_{DS,P0,rms} \times (V_{DD2} - V_{SS}) + 4 I_{COMP,BIAS} \times (V_{DD} - V_{SS,COMP}) = \\ &= (950\,\text{nA} + 750\,\text{nA}) \times 1\,\text{V} + 7.5\,\mu\text{A} \times 1\,\text{V} + 680\,\text{nA} \times 0.8\,\text{V} + 400\,\text{nA} \times 1.25\,\text{V} = \\ &= 10\,\mu\text{W} \end{aligned} \tag{4.21}$$

If the CT design is considered, the currents can be lowered as in table 4.2. Assuming that the second stage and the comparator dissipate the same amount of power, the power consumption at CT is potentially lower than:

$$\begin{aligned} P_{tot} &= P_{DACs} + P_{AMP} + P_{COMP} \simeq \\ &= (I_{DAC1} + I_{DAC2}) \times (V_{DD} - V_{SS}) + I_{C,Q0,rms} \times (V_{DD} - V_{SS}) + \\ &+ I_{DS,P0,rms} \times (V_{DD2} - V_{SS}) + 4 I_{COMP,BIAS} \times (V_{DD} - V_{SS,COMP}) = \\ &= (250\,\text{nA} + 200\,\text{nA}) \times 1\,\text{V} + 2.2\,\mu\text{A} \times 1\,\text{V} + 680\,\text{nA} \times 0.8\,\text{V} + 400\,\text{nA} \times 1.25\,\text{V} = \\ &= 3.6\,\mu\text{W} \end{aligned} \tag{4.22}$$

4.1.6 Programming the operating frequency

Adding only some passives and switches, it is possible for the system to have more (in this case two) operating frequencies to choose from. While the circuit was designed with the intent to work at $1\,\text{MHz}$, the possibility to instead read at $100\,\text{kHz}$ can be extremely useful for testing purposes or if the system requires to slow down operations.
Theoretically, the circuit can already work at lower frequencies as it is by looking at figure 4.20. However, a lower f_{symbol} can be taken advantage of for reducing the power consumption. The load capacitance of the output of the second stage can be in fact increase, in that now no information is present above $100\,\text{kHz}$ and in this way more noise is filtered. The result is an increased SNR compared to the previous case for $f_{symbol} = 100\,\text{kHz}$, meaning a lower current can be used and the output will still provide more than $10\,\text{dB}$ SNR. Adding capacitance on the output node of the first stage is simply done with a switch, which is controlled from outside the analog circuit. When the additional capacitance is switched on, the SNR is way above what is needed. As a

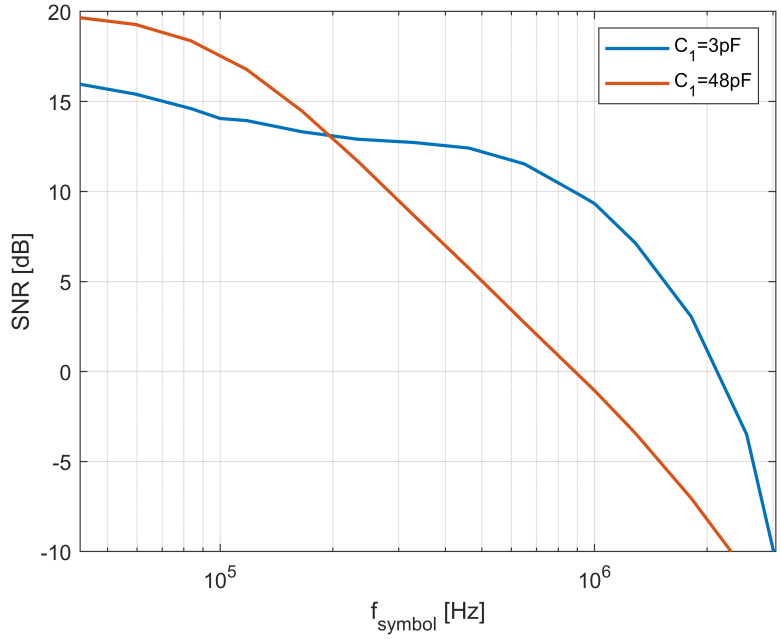


Figure 4.21: SNR vs operating frequency with additional capacitance on C_1 switched on

consequence, it is possible to change the bias voltages/currents such that the currents in the amplifier are lower, saving a lot of power.

4.1.7 Montecarlo variations

The objective of this work is to design an integrated circuit that can work in a complex system like a quantum computer. This means that the circuit should be reproducible and be functional despite the presence of PVT deviations from the nominal values of circuit parameters.
From 150 runs of Montecarlo simulations, it is observed that in most cases the circuit becomes non-functional for variations on device parameters.

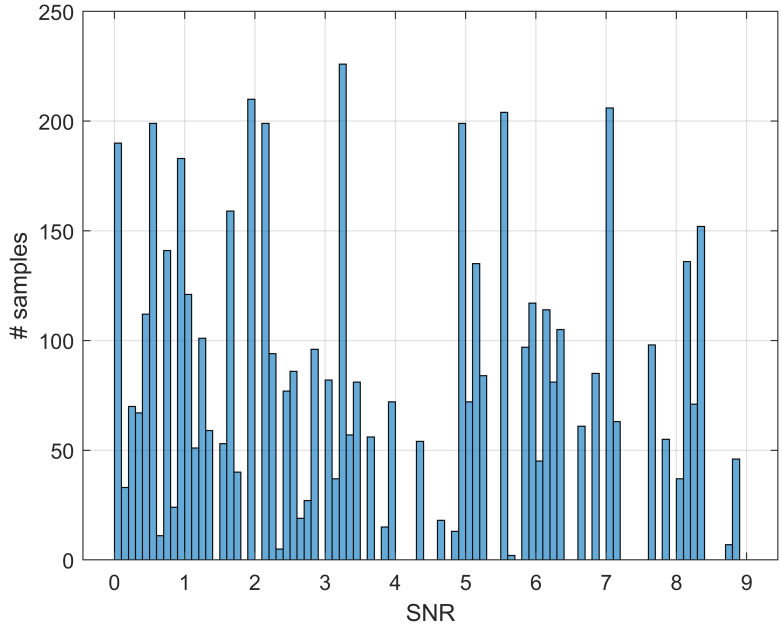


Figure 4.22: SNR (linear unit) vs different runs of Montecarlo simulation

This unfortunate outcome is mainly due to the high sensitivity of the circuit with respect to

Corner	Nominal	sample 140
SNR_{max} $[dB]$	9.3	9.6
$D_{in,1}$ [decimal]	108	103
I_{DAC1} $[nA]$	960	920
$D_{in,2}$ [decimal]	84	86
I_{DAC2} $[nA]$	745	775
V_{SS} $[V]$	-0.747	-0.744

Table 4.4: Restoring SNR for worst case corner simulation

the bias and supply voltages. Effectively, the Power supply Rejection Ratio (PSRR) is very poor, as any disturbance on the supply is just seen as an input signal applied at the input of the second stage. It is an expected limitation, originating from the choice of a single-ended configuration in which the amplification stages rely on a resistive load.
It is fortunately always possible to restore the optimum OP through calibration; this is done by adjusting the DAC's codes and the emitter voltage of the first amplification stage, as shown in table 4.4 for an example worst case (sample 140 of the Montecarlo run) where the starting SNR was $-59\,\mathrm{dB}$ with the nominal set of bias voltages/currents.

4.2 Layout

The last step for the design of the readout circuit is the realization of the layout view. In this section, the layout of each block is shown.

4.2.1 SiGe HBT NPN layout view

The model of transistor used for amplification purpose is the npn13G2L, shown in figure 4.23. Contrarily to the npn13G2, this model can be realized with different emitter widths, allowing for a bigger design space. The main difference from the layout point of view is the presence of two points of contact for the base and the collector.

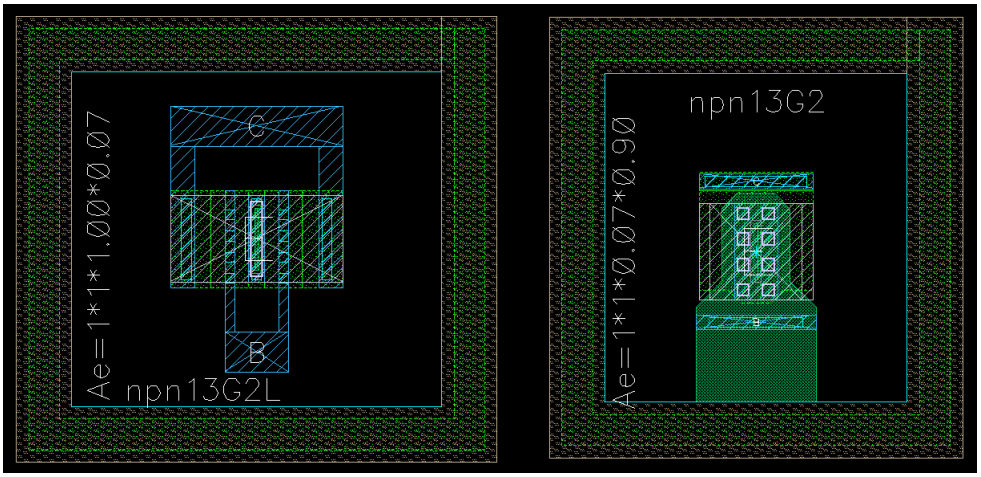


Figure 4.23: Layout view of HBTs from the SG13G2 IHP process.
On the left: npn13G2L
On the right: npn13G2

4.2.2 Contacting the substrate

In order to ensure that the bulk of transistors is at the intended potential, designated instances both in schematic and layout view are implemented to contact directly the substrate and bias it. PMOS of a certain block are placed in the same n-well together with one or more NTAP1 instances; NMOS instead are placed inside a guard ring connected to a PTAP1 instance. In particular, buffers and switches that are supposed to drive digital signals are placed in different wells/rings, separated from the analog ones. A clear division between a NMOS guard ring and two different n-wells for PMOS is visible in the comparator layout view, in figure 4.26.

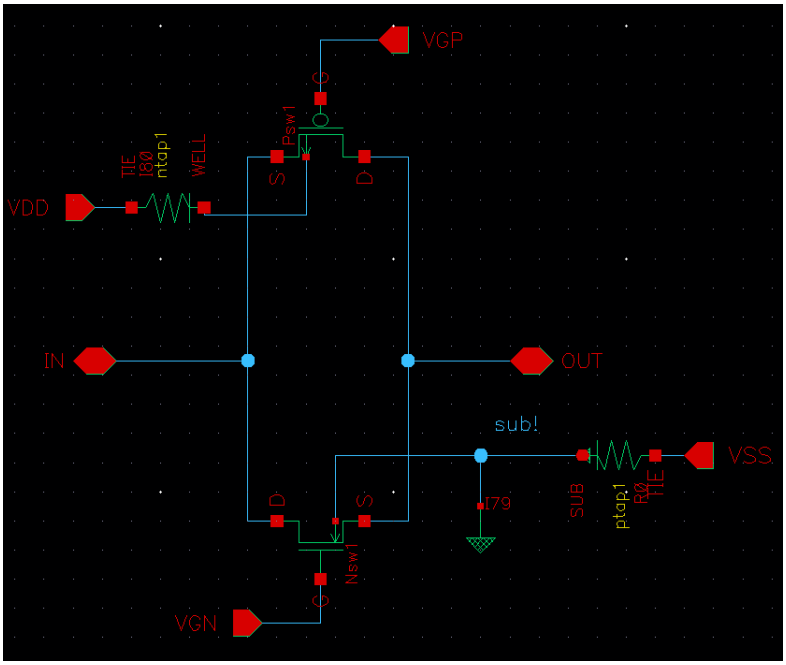


Figure 4.24: Example of substrate contacts in schematic (Transmission Gate)

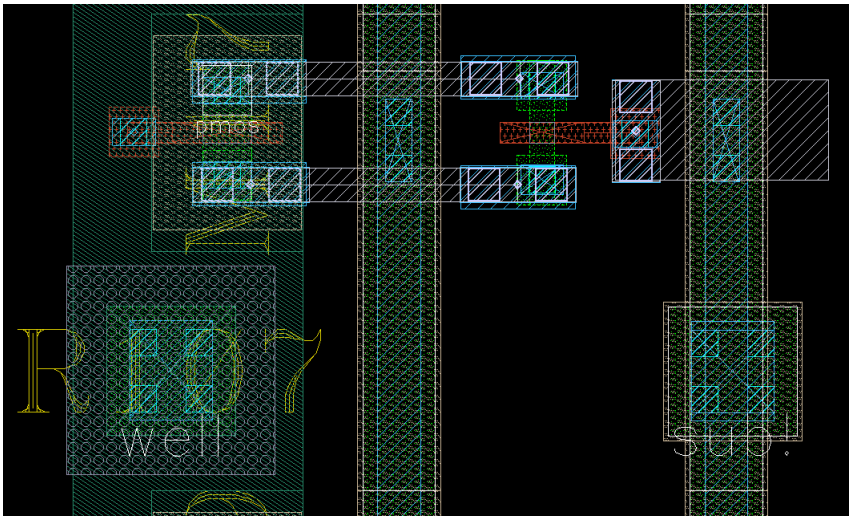


Figure 4.25: Layout detail that show how pmos and nmos are placed respect to the substrate contacts

4.2.3 Layout of the Comparator

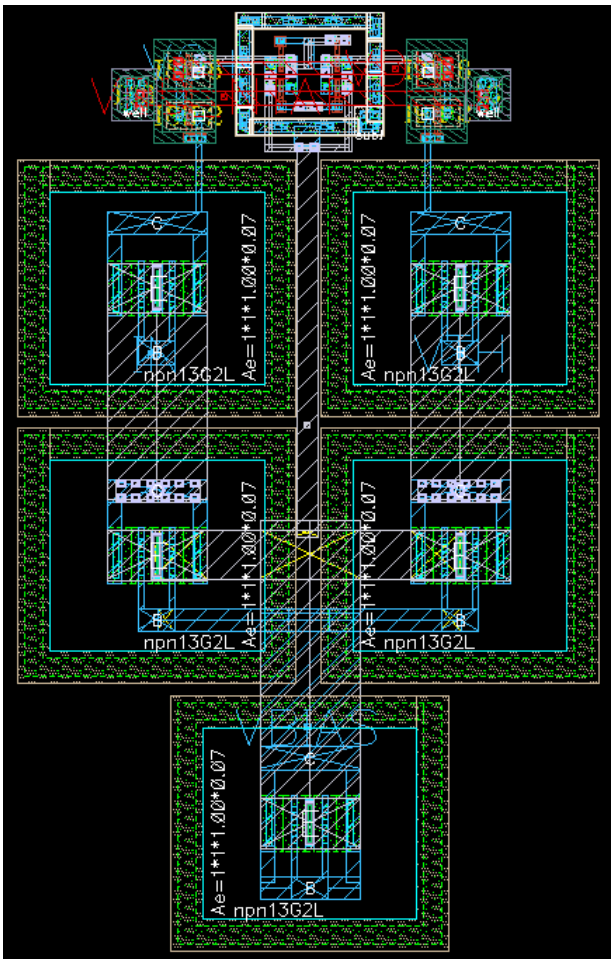


Figure 4.26: Layout view of the comparator

4.2.4 Layout of the DAC

Even though linearity is not of primary concern in this work, the currents in the DAC are balanced as much as possible by alternating fingers of transistors of the same bit with other fingers from different bits; the placement is done such that every finger corresponding to the K_{th} bit is spaced from the following finger of the same bit by $2^{N-K}\times$ fingers.

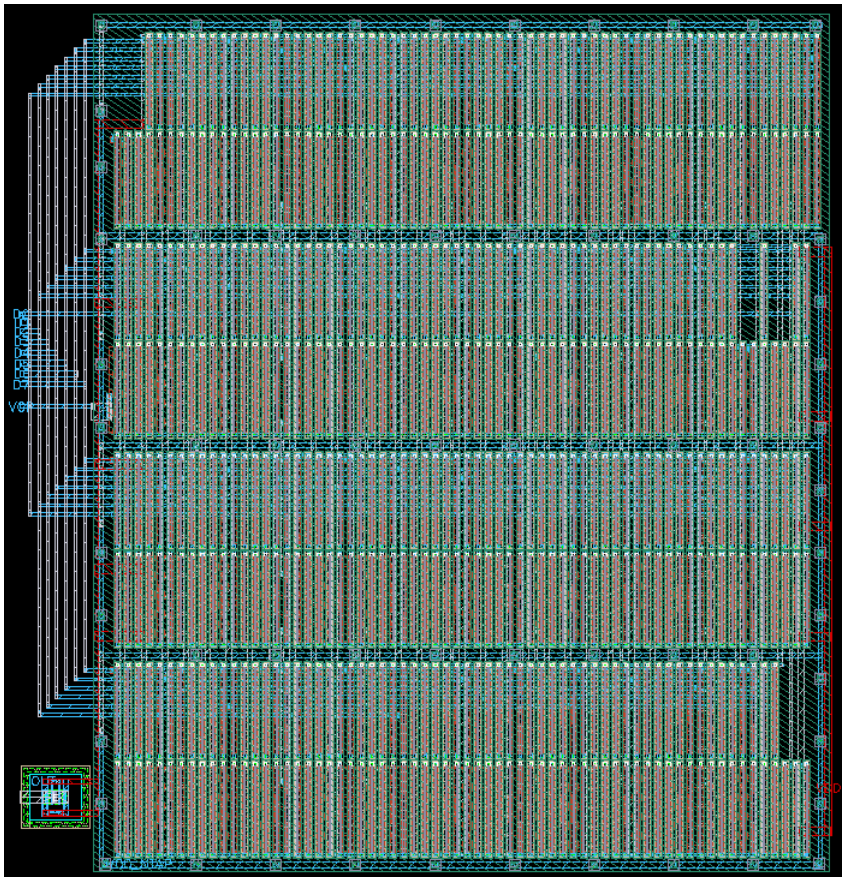


Figure 4.27: Layout view of the current DAC

4.2.5 Layout of the Amplifier

The amplifying NPN counts ten fingers in parallel. The resistors are divided in smaller resistors banks and connected with metal in series, due to their extremely big length.

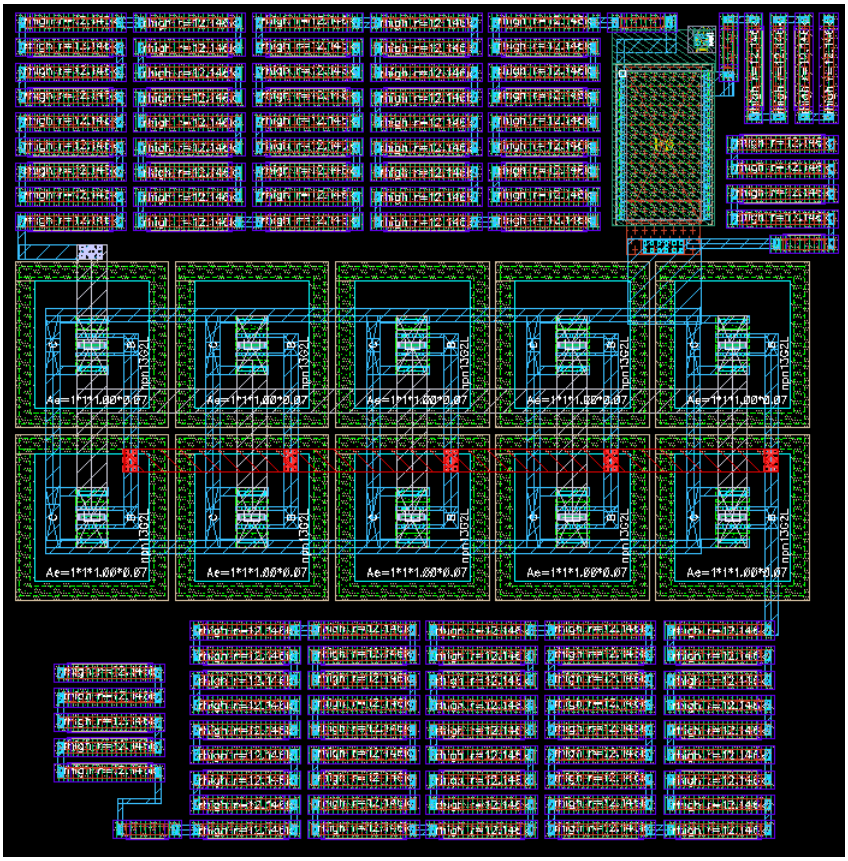


Figure 4.28: Layout view of the amplifier's core, including Q_0, P_0, R_b, R_1, R_2, R_{s2}

4.2.6 Capacitors size

The low-pass filter capacitors are the largest elements in the system. In SG13G2 technology pdk only MIM capacitor elements ("cmim") are available and each one has an occupancy of $1.5\,\mathrm{mF/m^2}$. The most bulky ones are used for filtering noise from the reset DAC, being $C_{dac2} = 8\,\mathrm{pF} \times 6 = 48\,\mathrm{pF} \longrightarrow 5329\,(\mu\mathrm{m})^2 \times 6$ and for improving the SNR when switching a $100\,\mathrm{kHz}$ operation, being $C_{added,100kHz} = 5\,\mathrm{pF} \times 9 = 45\,\mathrm{pF} \longrightarrow 3364\,(\mu\mathrm{m})^2 \times 9$.

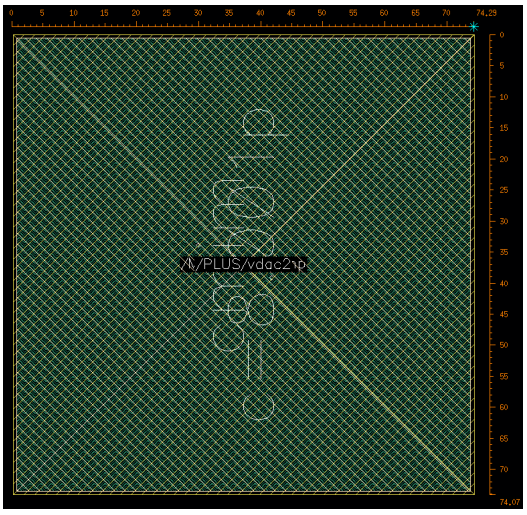


Figure 4.29: Unit capacitor cell for C_{dac2}

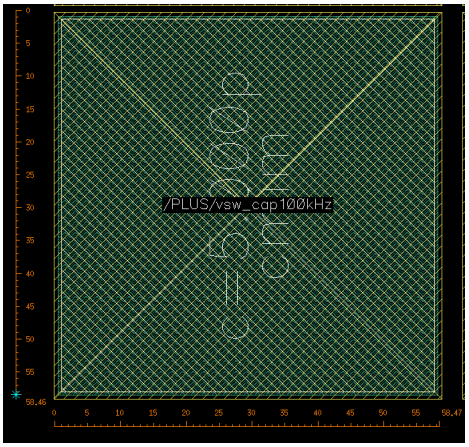


Figure 4.30: Unit capacitor cell for $C_{added,100kHz}$

4.2.7 High-level layout view and estimated area

After floor-planning of the various blocks, the overall system appears as in figure 4.31, and it occupies a total area of approximately

$$A \approx 459\,\mu\text{m} \times 252\,\mu\text{m} = 115\,908\,(\mu\text{m})^2 = 0.115\,908\,(\text{mm})^2 \tag{4.23}$$

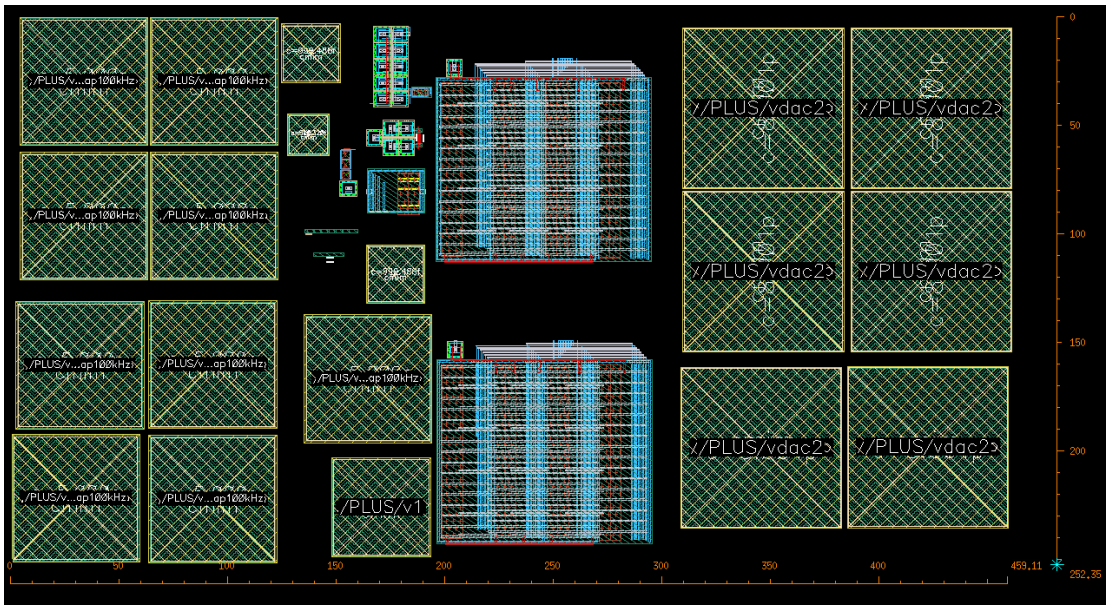


Figure 4.31: Final layout view of the circuit

The expected are occupancy of this circuit shows encouraging results for co-integration of readout front-end and qubits. If the possibility to operate at lower power and lower frequency is removed, the area is be much lower in that the bulkiest cap would is not needed.

4.3 Comparison with state-of-the-art

As conclusion of the chapter, the expected (simulated) performance is assessed and compared to other previous works in tables 4.5 and 4.6. The expected result of this system compares well with previous works, with an expected increase in operating frequency and less power consumption with respect to other DC readout works, despite occupying a bit more area (still much less than RF systems).

System	This work (expected results at T_{sim}, $f_{symbol} = 1\,\text{MHz}$)	This work (expected results at CT, $f_{symbol} = 1\,\text{MHz}$)	This work (expected results at T_{sim}, $f_{symbol} = 100\,\text{kHz}$)	This work (expected results at CT, $f_{symbol} = 100\,\text{kHz}$)
SNR $[dB]$	9.3	$\in [10,\ 14]$	17.5	$\in [18.5,\ 22.5]$
Power $[\mu W]$	10	3.6	10	3.6
Reading time $[\mu s]$	1	1	10	10
Area $[(mm)^2]$	0.116	0.116	0.116	0.116
Sensing current $[pA]$	300	300	300	300

Table 4.5: Comparison table with state-of-the-art spin qubits readout #1

System	RF [42]	DC [43]	DC [44]	DC [45]	DC [47]
SNR $[dB]$	50	8.75	10	/	9
Power $[\mu W]$	> 6000	1	64	1	1200
Reading time $[\mu s]$	6	9	10	384	0.5
Area $[(mm)^2]$	1.8	/	0.08	/	0.04
Sensing current $[pA]$	/	/	54	/	250

Table 4.6: Comparison table with state-of-the-art spin qubits readout #2

5

Conclusion and future work

5.1 Conclusion

This thesis project has achieved two main results:

- A comprehensive literature review about the state-of-the-art DC readout of spin qubits has been reported. The specifications for the readout circuits were discussed and four possible architectures for the front-end amplification were compared.
- The entire design process of a functional front-end readout circuit was carried out up to the layout stage.

5.1.1 DC readout specifications

In chapter 3, the specifications for the front-end circuit were derived, starting from assumptions on a readout process based on Pauli Spin Blockade spin-to-charge conversion. In second place, four architectures for the realization of the front-end amplifier were analyzed and compared based on these metrics.
The system needs to carry out the readout achieving $SNR \geq 10\,\mathrm{dB}$ in order to ensure a Bit-Error-Rate of $BER \leq 1 \times 10^{-3}$ (or Fidelity $F \geq 99.9\,\%$) and allow the execution of reliable quantum error correction algorithms. To enhance the scalability of the system, the number of readings that the circuit can sustain per amount of time should be maximized while the reading time must be kept well below the decoherence times; in particular, this work targeted $f_{symbol} = 1\,\mathrm{MHz}$.
The environment in which the qubits operate, combined with the final goal of co-integrating readout circuits and qubits leads to strict power consumption constraint in order to avoid overheating inside dilution refrigerators. This work attempts to minimize power with a goal of $P \leq 10\,\mu\mathrm{W}$.
The four amplifiers analyzed are the CA, the VA, the TIA and the CHA. After comparing their noise performance, it is concluded that the most promising structures are the ones based on the VA, namely VA, TIA and CHA. For all these three amplifiers, the input-referred white noise is comparable with the SET white noise; it is therefore believed that they can achieve the target SNR even if taking into account low-frequency noise and sampling. Eventually, since the three configurations all implement a VA with slight modifications, designing a VA is a reasonable choice.

5.1.2 Design of a SiGe HBT-based readout circuit

In chapter 4, the transistor level design of the front-end readout circuit was presented along with the methods of simulation. These were carried out at a simulating temperature of $-40\,^{\circ}\mathrm{C}$ and the SNR was estimated using an ideal sampler at the output node. The chosen amplifier configuration is a common emitter stage voltage amplifier followed by a common source stage with source resistive degeneration. With a bias current of $7.5\,\mu\mathrm{A}$ for the first stage and a bias current of $680\,\mathrm{nA}$ for the second stage, the two stages offer a voltage gain of about 33 and 4 respectively. If a generic SET is considered as the input of the front-end, the DC current to voltage gain is simply $A_{IV} = R_{set} // R_{in,amp} \times A_1 \times A_2$. For the sample SET used in simulations, providing an input signal

of $\left|I_{set,|0\rangle} - I_{set,|1\rangle}\right| = I_S \simeq 300pA$, the output swing is $\left|V_{|0\rangle} - V_{|1\rangle}\right| \simeq 3.5\,\text{mV}$ at $1\,\text{MHz}$.

The output noise is mainly due to the first amplification stage, and referred at the output after sampling and compared to the signal level it results in a signal-to-noise ratio of $SNR = 9.3\,\text{dB}$ at an operating frequency of $f_{symbol} = 1\,\text{MHz}$. This number is expected to grow from $2dB$ to $5dB$ at CT because of the increased transconductance of the first stage NPN. Moreover, the operating frequency can be shifted at $100\,\text{kHz}$ with a large increase in SNR, reaching a value around $17.5\,\text{dB}$ and again an expected increase at CT. The overhead in SNR for the lower frequency can be exploited for lowering a lot the power consumption.

The expected power consumption of the system, including the bias networks and the comparator is $P = 10\,\mu\text{W}$ at T_{sim} and potentially $P = 3.6\,\mu\text{W}$ at CT.

5.2 Future work

Due to time constraints, the tape-out of this circuit will occur after the realization of this thesis. For this reason, the first step to continue on the track of this work will be to measure the chip and observe if the SNR increases as expected at CT, and more importantly if the circuit is functional after calibration. Some limitations of the readout circuits which could be improved in the future are the following:

- Having a single-ended circuit results in very weak PSRR and low resilience to PVT variations, in that a change in circuit parameters causes a shift in DC voltages at the sampling moment at the output node. Even though calibration can solve this for a single-shot readout, in the perspective of producing many of these structures working at full-regime integrated with qubits, this aspect becomes fundamental. An alternative could be to enhance the design with feedbacks that can provide automatic calibration schemes.
- The effect of reset and in general of large swings at the drain of the SET that are not due to the signal itself is not well determined in terms of qubit fidelity. Accomplishing this requires a characterizations of all the parasitics of SETs and QDs and an estimation of the magnitude of the voltages that the QD can sustain without affecting the state of the qubits.
- An alternative amplifier architecture can decrease significantly the noise produced by the front-end circuit. As discussed in section 3.3.3, a bandpass transfer function could cut out all the low frequency noise improving the SNR and leaving room for decreasing the power consumption. However, this solution also results in losing the low-frequency information of the input signal, which is significant in case of repeated symbols. This problem can be worked around by forcing the input frequency at the operating frequency by applying a feedback from the output of the comparator to the input of the amplifier. In this case half period is used for the integration of the input symbol, while the other half is used for the processing of a "fake bit", being the opposite of the previous measured bit.

While working on this thesis project, some ideas came up about how the DC readout can be improved in the future so that realizing systems with many more qubits than today becomes possible.

- Now that $1\,\text{MHz}$ operation seems possible for DC readout, a time-multiplexing structure can be tested to measure more qubits with the same readout circuit, enhancing the scalability of the system. Since in previous works DC readout was carried out with reading times of about $10\,\mu\text{s}$, it is reasonable to think that this circuit could switch between 10 different SETs using a multiplexer and read each qubit for $1\,\mu\text{s}$. The challenge here is ensuring that all the SETs sit at similar bias points to preserve the functionality of the circuit.
- Going to a one-chip solution is the natural follow up of this work, in that the low power consumption of this circuit now allows for integration of amplifier, SET and QDs on the same chip. The chip could be realized in Si/SiGe technology so that QDs can possess high decoherence times and the low noise of HBTs can be exploited.
- More engineering could be done on the SET side rather than on the front-end circuit side. Since SETs are very low noise, one could employ proper amplifiers only based on SETs

(for instance cascade two SETs), so that the magnitude of the signal is enhanced before encountering more noisy devices on its path. This kind of design however is possible only as long as more compact models are realized as in [37] such that effective simulations in Cadence or other tools can be carried out. As it was observed, the main bottleneck for the SNR is the input swing, so any improvement on the input swing is desirable in future SETs (for example higher output resistance).

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