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Degradation Mechanism Analysis and Modeling of SiC MOSFETs Under 60Co Gamma Ray Total Ionizing Dose Irradiation

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***Abstract*— The degradation mechanisms of silicon carbide (SiC) VDMOSFET and trench metal oxide semiconductor field effect transistor (MOSFET) in a 60Co gamma irradiation environment were investigated. The degradation of electrical characteristics of SiC MOSFET in different working states after irradiation with different total ionizing doses (TIDs) was explored. The defects induced during the irradiation process were studied in annealing experiments conducted after irradiation. The reasons for the degradation of SiC MOSFET caused by TID were revealed, and a prediction model of threshold voltage (V_{th}) shift was proposed and verified through TCAD simulation. The V_{th}, breakdown voltage (BV), ON-resistance (R_{on}), input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse transfer capacitance (C_{rss}) were measured at different irradiation doses and annealing conditions. Experimental results indicated that the degradation of both R_{on} and C_{iss} was primarily caused by the V_{th} shift. As the doses increased, the shift in V_{th} gradually reached saturation. Similar trends to VDMOSFET were observed in trench MOSFET but with greater sensitivity to TID. In addition, MOSFETs biased at zero voltage exhibited lower shifts in V_{th} compared with those under high gate bias conditions. Furthermore, the increase in defects in the gate oxide during irradiation and annealing processes were calculated. Finally, a model predicting V_{th} shift path was established, and its accuracy and limitations were determined. This study provides valuable insights into the effect of TID on SiC MOSFETs.**

***Index Terms*— Irradiation, oxide trap, silicon carbide (SiC) metal oxide semiconductor field effect transistor (MOSFET), threshold voltage shift path model, total ionizing dose (TID).**

I. Introduction

BECAUSE of its wide bandgap, high breakdown electric field, and excellent thermal conductivity, silicon carbide (SiC) is considered one of the most suitable semiconductors for high-temperature and high-power-density devices [1], [2], [3], [4]. SiC metal oxide semiconductor field effect transistors (MOSFETs) exhibit higher switch frequency, lower energy loss, and lower temperature resistance than those of Si-based MOSFETs [5], [6], and are gradually being commercialized in applications such as dc–ac inverters and on board chargers (OBCs) for electric vehicles [7], [8]. Power devices operating in space or nuclear power plants must be able to withstand electrical stress and space radiation during long-term operation. With a bandgap of 3.2 eV, about three times that of silicon (Si), 4H-SiC exhibits a lower density of radiation-induced defects under similar irradiation conditions compared with Si. The crystal displacement energy of 4H-SiC is as high as 22 eV, whereas that of Si is only 15 eV. The higher displacement energy of 4H-SiC increases its hardness against neutron radiation. Therefore, SiC MOSFETs are deemed to have significant potential for applications in nuclear reactors and spacecraft, where robust radiation hardness is essential [9], [10], [11], [12].

However, high-energy particles and radiation in the space environment can still induce degradation, such as total ionizing dose (TID) effects, leading to the deterioration or even failure of devices. The dose rate corresponds to the altitude of the spacecraft. Generally, for spacecraft with a five-year operating cycle, the radiation dose to the components can reach 1 krad(Si) to 5 Mrad(Si). The interface barrier of SiC/SiO_2, 2.7 eV, is lower than the interface barrier of Si/SiO_2, 3.1 eV [13], which causes electrons to exhibit more violent Fowler–Nordheim tunneling into the oxide, resulting in an

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increase in gate leakage current. In addition, the defect types and density of the SiC/SiO_2 structure limit the suitability of SiC MOSFETs for space operations. Usually, two of the reasons for the degradation of SiC MOSFETs are the fixed charge in the gate oxide during irradiation and the increase in interface state density at the interface between the gate oxide and the semiconductor as the irradiation dose accumulates [14], [15]. Therefore, the irradiation resistance of MOS structures with fewer interface states, created by annealing in a nitrogen oxide atmosphere, has been studied. Although annealing in nitrogen monoxide or nitrogen dioxide atmospheres can significantly improve mobility, the severe TID caused by the introduction of additional hole traps near the interface leads to more severe degradation of the threshold voltage. [16], [17]. In addition, the degradation of SiC MOSFET after irradiation can be partially recovered, which may be related to the elimination of defects caused by thermal neutralization of trapped charges and passivation of defects [18]. Moreover, the radiation hardnesses of power devices with different structures, represented by double-diffused MOSFETs (DMOSFETs) and DMOS integrated with junction barrier Schottky (JMOS), were compared [19]. To meet the high-reliability requirements of SiC devices in power applications, it is necessary to measure and evaluate the failure rate. The atmospheric neutron-induced degradations in SiC power MOSFETs are investigated by spallation neutron irradiation Deki et al. [20] and Akturk et al. [21]. The SEB failure rate of SiC MOSFET was measured and calculated [22]. The measurement and modeling of system reliability in radiation environments have also been reported [23]. There are reports that improving the TID tolerance of MOSFETs through layout styles, the hexagonal cell has better tolerance than rectangular under the same conditions [24]. The long-term reliability of devices under the TID effect has also been studied [25]. However, there is still a lack of prediction models for the degradation of different structural devices in irradiation environments.

This study compared both the radiation tolerance and the recovery effects after annealing of VDMOSFET and trench MOSFET. The reasons for the degradation of SiC MOSFETs caused by TID effects were explained. According to the TID test standard MIL-STD-883, Si unipolar power devices are required to undergo high-temperature annealing (HTA) to accelerate the release of interface states after high-dose irradiation [26]. This process is done to prevent the contribution of interface states to irradiation degradation from being underestimated. Therefore, HTA and high-temperature gate bias annealing (HTGBA) were performed after irradiation in this study to evaluate the effects of interface states and interface traps on SiC MOSFET. Analyzed the reasons why trench MOSFETs are more sensitive to TID effects, including gate oxide thickness, gate oxide control ability over the channel, and gate oxide reliability. The sensitivity of parasitic parameters of trench MOSFET and VDMOSFET to the TID effect has also been compared and explained. This study also calculated the defects generated by irradiation, predicted the degradation of devices with different structures under different irradiation doses, and verified the accuracy of the proposed model through both TCAD simulation and experiments. This study can provide helpful guidance to evaluate the service lifetime and reliability of SiC MOSFETs used in space operations.

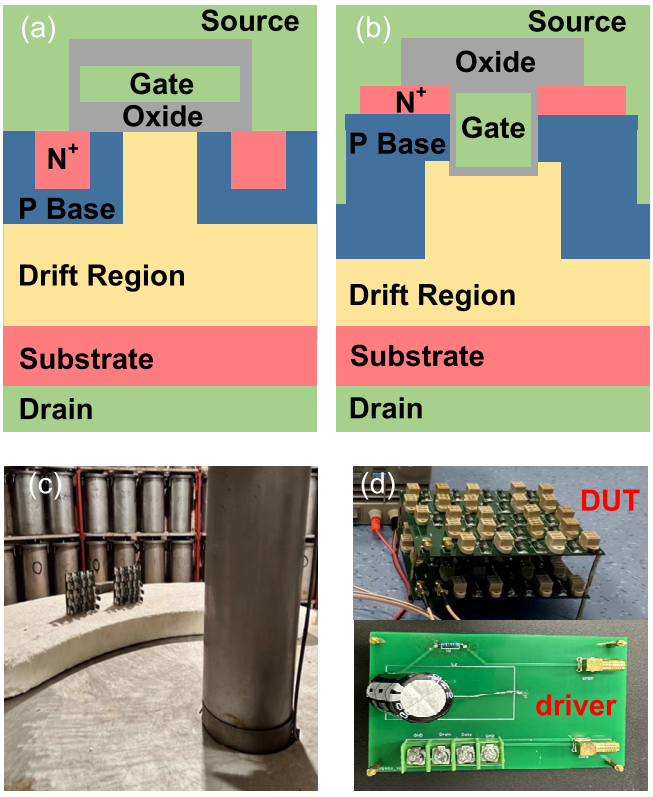

Fig. 1. Cross section of (a) VDMOSFET and (b) trench MOSFET. (c) Irradiation chamber. (d) Devices under test and the driver circuit are used to power the tested devices in the irradiation environment.

II. Tested Devices and Experimental Methods

This section overviews the structures and characteristics of the SiC MOSFET devices tested in irradiation experiments and provides a detailed description of the experimental conditions during irradiation and annealing.

A. Tested Devices and Test Setup

Representative VDMOSFETs and trench MOSFETs were selected as the tested devices commercially available 1200 V SiC MOSFETs from two manufacturers. Fig. 1(a) shows the cross-sectional views of SiC MOSFET power devices with different structures used in the TID experiments, where Fig. 1(a) and (b) represent VDMOSFET and trench MOSFET, respectively. The gate oxide thickness of the VDMOSFET is 37 nm, while that of the Trench MOSFET is 54 nm.

All samples were stored in dry ice and returned to room temperature (25 °C) for irradiation and testing. To demonstrate that the increased interface state caused by the 168 h high-temperature gate bias (HTGB) is not the reason for the recovery of V_{th}, a set of MOSFETs underwent 168 h of HTGB aging before irradiation (gate voltage bias: 18 V, ambient temperature: 150 °C). The electrical characteristics of the samples are listed in Table I. The testing conditions for C_{iss}, C_{oss}, and C_{rss} were $V_{DS} = 1000$ V, $V_{gs} = 0$ V, and $f = 100$ kHz.

TABLE I
ELECTRICAL PARAMETERS OF TESTED DEVICES

Device	VDMOSFET	Trench MOSFET	HTGB VDMOSFET	HTGB Trench MOSFET
V_{th} (V)	2.77	4.14	2.60	4.02
BV (V)	1634.69	1867.63	1632.85	1881.30
R_{on} (mΩ)	65.10	78.56	62.87	79.48
C_{iss} (nF)	1.04	0.89	1.05	0.88
C_{oss} (pF)	57.92	49.80	59.41	50.00
C_{rss} (pF)	3.37	20.10	3.43	23.66

B. Irradiation Source and Irradiation Bias

The radiation tests were carried out using gamma rays provided by a cylindrical cobalt-60 (60Co) radiation source at a dose rate of 50 rad(Si)/s. Three groups of MOSFETs were exposed to total doses of 300, 600, and 1000 krad(Si), respectively. Fig. 1(d) shows the experimental setup during irradiation.

The temperature in the irradiation chamber was always set as 25 °C. The VDMOSFETs and trench MOSFETs were divided into two groups: one group was irradiated with a gate voltage bias $V_{gs} = 18$ V, while the other group was irradiated with the gate voltage bias set to 0 V. In addition, the drain–source voltage for both groups was maintained at zero.

C. Annealing Experiments

Three annealing experiments, each including 12, 24, 48, and 168 h of annealing, were carried out. Experiment (1) room temperature annealing (RTA): The MOSFETs were placed in a constant temperature box with a temperature of 25 °C and a humidity of 50%. Experiment (2) high-temperature annealing (HTA): Annealing was carried out at 175 °C. The high temperature accelerated annealing to evaluate the temperature effect. The electrodes of the DUTs in experiments 1 and 2 were grounded. Experiment (3) HTGBA: Annealing was completed at 175 °C and $V_{gs} = 18$ V. All irradiated VDMOSFETs and trench MOSFETs had undergone annealing. In addition, a group of samples without irradiation was designed in an HTGB experiment with $V_{gs} = 18$ V and 175 °C. All measurements of the DUTs are taken after the samples have returned to room temperature.

III. ANALYSIS, MODELING, AND VALIDATION OF EXPERIMENTAL RESULTS

This section presents the experimental results and analyzes the reasons behind the results. The degradation of various electrical characteristics under irradiation is induced by a decrease in V_{th}, which is mainly due to the additional fixed charge in the gate oxide. Furthermore, by modeling the relationship between the increased fixed charges and the irradiation doses, the degree of V_{th} shift at different doses is predicted, and the feasibility of the degradation model and conclusions are finally verified through TCAD simulation.

A. Degradation Mechanism Analysis and Comparison

After short-circuiting the gate and drain, the voltage is scanned until the drain current reaches 5 mA, and this voltage is extracted as the threshold voltage. Fig. 2(a) and (b) shows that positive gate bias voltage results in a larger V_{th} shift in VDMOSFET, and the shift increases with the increasing radiation dose until it approaches saturation, reflecting the cumulative effect of radiation dose. Even if it continues to accumulate to ultrahigh doses, the V_{th} shift still shows a saturated state [27]. At low doses, there are traps for captured carriers in the gate oxide, and as time progresses, some traps are filled by charge carriers. The rate of trap capture of carriers slows down. With increasing dose, the speed of V_{th} shift slows down. Similar results are obtained with the trench MOSFET. When $V_{gs} = 18$ V, the probability of recombination of electrons and holes excited by the TID effect decreases, and more holes in the gate oxide are accelerated toward the SiC/SiO_2 interface, causing a higher trap charge generation rate. If the voltage continues to increase, the hole-trapping cross section will decrease, and a sufficiently high electric field will lead to a reduction in the V_{th} shift [28]. VDMOSFET benefits from a smaller gate oxide thickness compared with trench MOSFET, resulting in less fixed charge accumulating in the gate oxide due to radiation. These characteristics make it easier to excite defects in the oxide of trench MOSFETs and weaken the control ability of the gate over the channel subsequent to the TID effect. This makes the V_{th} degradation of VDMOSFET less sensitive to ionizing radiation effects compared with trench MOSFET. When $V_{gs} = 18$ V, the V_{th} of the trench MOSFET decreased by 13.42 V and the VDMOSFET decreased by 3.05 V after irradiation. In addition, as the annealing time increases, the V_{th} of VDMOSFET and trench MOSFET show a weak recovery trend. The hole trap at the SiO_2/SiC interface and oxide traps in the oxide layer accumulate energy over time until the energy is sufficient for the transition. As shown in Fig. 2(c) and (d), the recovery phenomena of HTA and HTGBA are more obvious. The V_{th} curve of VDMOSFET is drawn with a dashed line, while the trench MOSFET is drawn with a solid line. This phenomenon is caused by both large electrical stress and high temperatures, with electrons entering the oxide through more intense thermionic emission tunneling to eliminate trap charges.

Normally, the V_{th} shift is considered to be associated with changes in interface state density, interface trap charge, and the addition of fixed charges. The variation in interface state density before and after irradiation and annealing was calculated by extracting the slope of the sub-threshold current [29], [30]. This method is commonly used for evaluating the interface state density of SiC/SiO_2. The midgap voltage shift is used to calculate the change in fixed charge [31]. Fig. 3 shows the sub-threshold current before and after different doses of irradiation and annealing.

When $V_d = 10$ V, V_g is scanned with a scan interval of 0.14 V. The scanning range of V_g is shown in Fig. 3. The red boxes in the figure indicate the part of the current that is sub-threshold current. The curve outside the red box indicates that the device is not conducting and will enter saturation. The slope of the sub-threshold portion of the device with the largest V_{th} shift was fit and the interface state density change was calculated. To eliminate the interference of HTGB on the

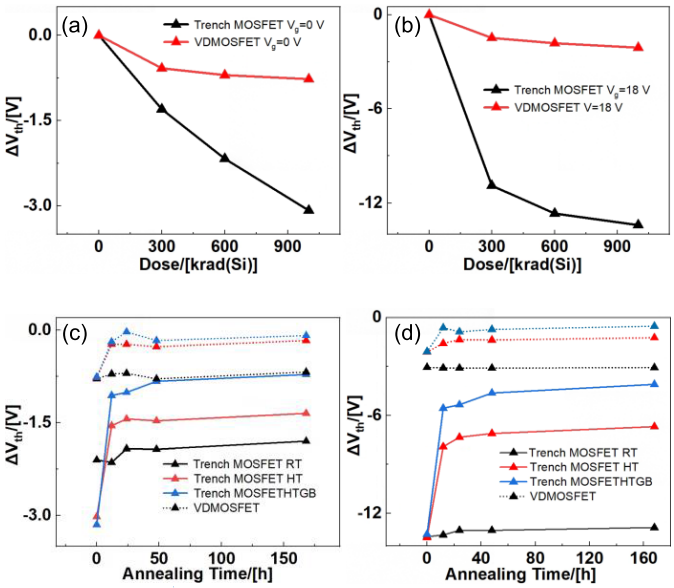

Fig. 2. When (a) V_{gs} = 0 V and (b) V_{gs} = 18 V, the shift of V_{th} for VDMOSFET and trench MOSFET during the irradiation, when (c) V_{gs} = 0 V and (d) V_{gs} = 18 V, the shift of V_{th} for MOSFET during the annealing processes.

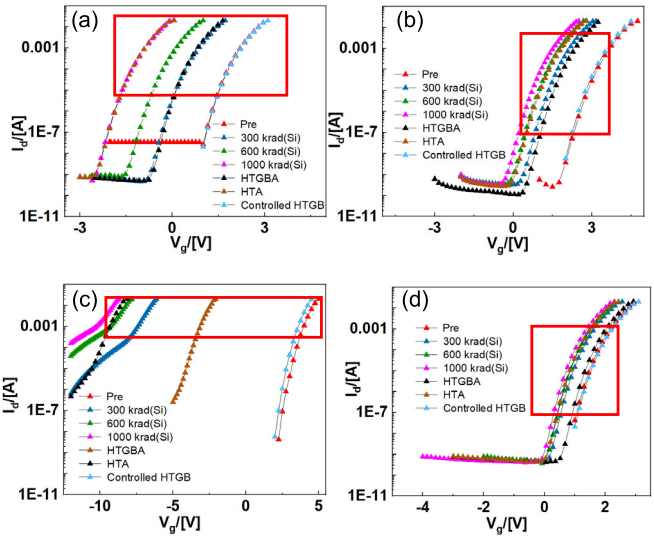

Fig. 3. Sub-threshold current of (a) VDMOSFET with V_{gs} = 18 V. (b) VDMOSFET with V_{gs} = 0 V. (c) Trench MOSFET with V_{gs} = 18 V and (d) trench MOSFET with V_{gs} = 0 V.

interface density of states, the slight interference of HTGB on the interface state with a duration of 168 h was verified by the HTGB control experiment.

In Table II, D_{it} is the interface state density, N_{it} is the interface trap, and N_{ox} is the fixed charge. The interface state density and interface traps after irradiation are represented by D'_{it} and N'_{it}, respectively. The interface states follow an exponential distribution for $E_c - E_t < 0.4$ eV and a nearly uniform distribution from 0.4 to 1.0 eV. The interface traps are uniformly distributed between 0.4 and 1.0 eV. The defect concentration and V_{th} changes listed in the table are compared with those of unannealed devices after irradiation. The changes in interface state density of the devices listed in Table II reveal

TABLE II
DEGRADATION OF ELECTRICAL PARAMETERS AND CHANGES IN DEFECTS AFTER ANNEALING

Device	VDMOS FET	Trench MOSFET	HTGB VDMOSFET	HTGB Trench MOSFET
ΔV_{th} (V)	-3.1	-13.4	-0.5	-4.1
D_{it} ($eV^{-1}*cm^{-2}$)	$3.2e^{11}$	$2.4e^{11}$	$3.2e^{11}$	$2.4e^{11}$
D_{it}' ($eV^{-1}*cm^{-2}$)	$3.3e^{11}$	$2.6e^{11}$	$3.3e^{11}$	$2.4e^{11}$
N_{it} (cm^{-2})	$9.0e^{8}$	$9.7e^{9}$	$7.1e^{9}$	$8.6e^{9}$
N_{it}' (cm^{-2})	$9.3e^{8}$	$1.1e^{10}$	$7.9e^{9}$	$9.3e^{9}$
ΔN_{ox} (cm^{-2})	$5.4e^{11}$	$2.2e^{12}$	$1.2e^{11}$	$6.8e^{11}$

a weak influence of TID effects on the SiC/SiO_2 interface state density when V_{gs} = 18 V, Dose = 1000 krad(Si), and annealing time = 168 h. In the VDMOSFET, when the N_{ox} decreases by $5.4e^{11}$ cm^{-2}, the D_{it} only decreases by $1.0e^{10}$ $eV^{-1}*cm^{-2}$. The V_{th} recovery attributable to the decrease in D_{it} is roughly 2% of the recovery caused by the reduction in N_{ox}. This corresponds to a slight degradation in the time-dependent dielectric breakdown (TDDB) characteristics of SiC MOSFETs undergone TID effects, which is in agreement with the findings of a previous study [25].

Fig. 4 illustrates the capacitor–voltage (CV) shift corresponding to different doses of irradiation and annealing processes. To measure the gate capacitance (C_g), $V_d = V_s = 0$ V, an ac small signal (V_{ac} = 0.02 V) with a frequency of 1 MHz was given to the gate. V_g was scanned from −20 to 20 V at intervals of 0.1 V. During irradiation, the CV characteristics shifted toward the negative direction of the X-axis, indicating the increase in positive fixed charges in the gate oxide. This is associated with the capture of holes by traps in the gate oxide. The specific impact of the increase in fixed charges on the V_{th} during irradiation and annealing processes was calculated through the amount of CV characteristic shift, as listed in Table II. The increase in fixed charges during irradiation leads to a V_{th} decrease, which is almost equal to the measured decrease in V_{th}. Therefore, under experimental conditions, the shift in interface state density and interface trap charge on the V_{th} during irradiation and annealing processes is minimal. The interface state density and interface trap charge can be ignored, and the degradation of the V_{th} is solely determined by the increase and decrease in fixed charges. There are two reasons for this. First, most of the holes excited by the TID effect are captured by oxide traps during the transition to the SiC/SiO_2 interface, resulting in fewer holes reaching the interface. Second, Si-H dangling bonds have a probability of reacting with particles to produce interfacial states.

Fig. 5(a) reveals the slight degradation of breakdown voltage (BV) due to ionizing radiation effects and the weak recovery of BV during the annealing process. Since the V_{th} of some MOSFETs has shifted to negative values, the devices have become depletion MOSFETs. To ensure the channel turn off, a gate voltage of −12 V is applied during BV measurement. Fig. 5(b)–(e) shows the degradation of ON-state characteristics in the two MOSFETs after different

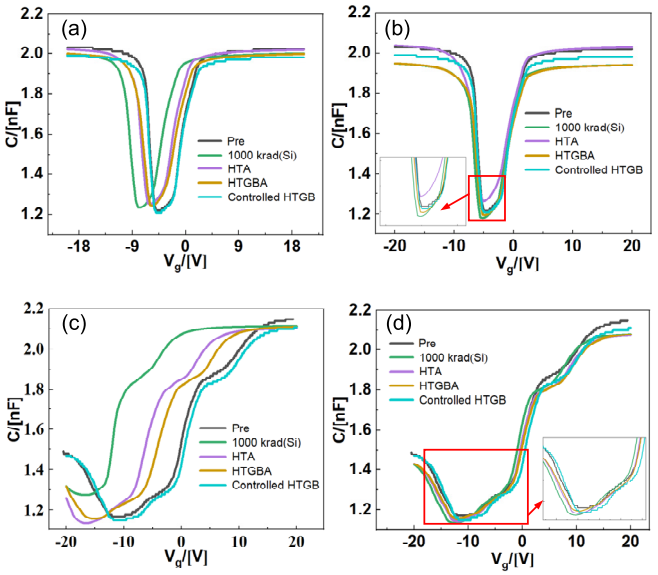

Fig. 4. CV of (a) VDMOSFET with $V_{gs} = 18$ V. (b) VDMOSFET with $V_{gs} = 0$ V. (c) Trench MOSFET with $V_{gs} = 18$ V and (d) trench MOSFET with $V_{gs} = 0$ V.

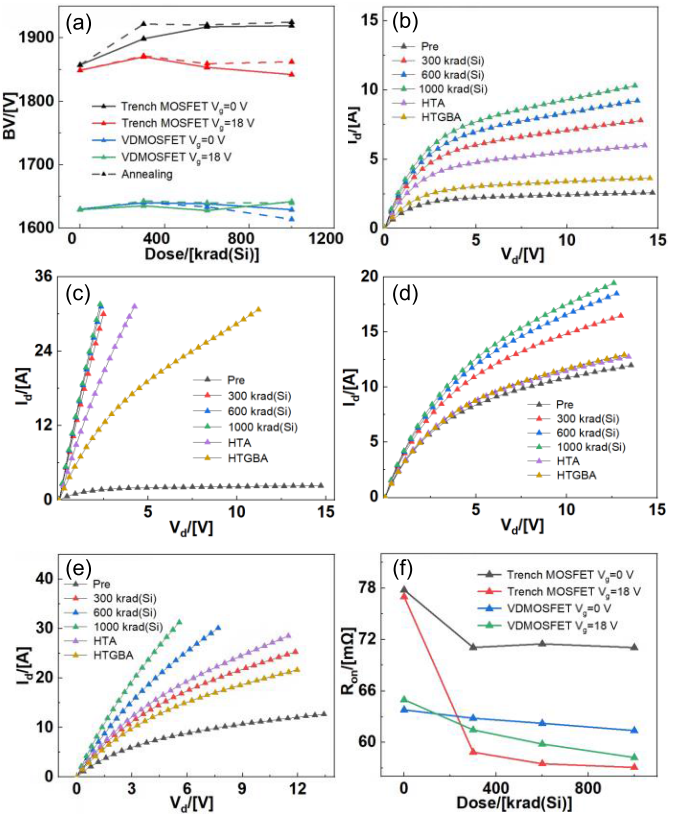

Fig. 5. (a) Shift of BV of VDMOSFET and trench MOSFET after irradiation at different doses. The ON-state characteristics of the MOSFETs recover after different doses of irradiation. (b) VDMOSFET, V_{gs} =0 V. (c) VDMOSFET, $V_{gs} = 18$ V. (d) Trench MOSFET, $V_{gs} = 0$ V, and (e) trench MOSFET, $V_{gs} = 18$ V. (f) Shift of R_{on} of VDMOSFET and trench MOSFET after irradiation at different doses.

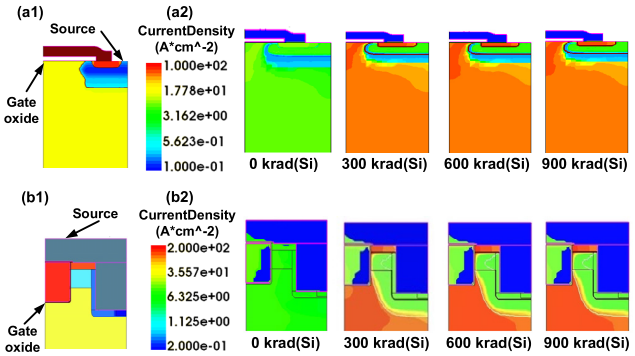

Fig. 6. When $V_{gs} = 1$ V, (a1) device structure of VDMOSFET and (a2) conductive channel area after irradiation at different doses. (b1) Device structure of trench MOSFET and (b2) Conductive channel area after irradiation at different doses.

doses of irradiation. When $V_g = 8$ V, V_d scans at intervals of 0.04 V starting from 0 V. The output characteristics exhibit an upward shift. Similar to the trend of V_{th}, the upward shift becomes more pronounced as the irradiation dose increases. The negative shift of V_{th} leads to an increase in the concentration of inversion layer charge carriers under the same gate voltage. The enlargement of the cross-sectional area of the inversion layer determines the degree of upward shift in the ON-state characteristics. Fig. 5(f) illustrates the degradation effects of R_{on} during the radiation. The degradation of R_{on} exhibit similar trends to those of V_{th}. As the dose increases, the degree of R_{on} degradation saturates. A TID simulation was conducted to consider insulator SiO_2 as a semiconductor with extremely high bandgap width. Three TID simulations were conducted at room temperature, each with a dose rate of 50 rad(Si)/s, reaching total doses of 300, 600, and 900 krad(Si), respectively.

As shown in the TCAD simulation in Fig. 6, the shift in V_{th} increases the conductive channel area and carrier concentration under the same V_{gs} when not fully conductive, thereby reducing R_{on}. The more the V_{th} shifts, the more the R_{on} decreases. The I_d versus V_d curve exhibits an upward trend with increasing doses due to the TID effect weakening the control of the gate. Annealing partially restores control, regressing the curve somewhat.

Not only the dc characteristics mentioned above, but also the ac characteristics of power devices are degraded by the TID effect. The curve of parasitic capacitance versus V_d is helpful for assessing the reliability and losses of SiC power devices. Fig. 7(a)–(c) presents C_{iss}, C_{oss}, and C_{rss} of the devices before and after irradiation and annealing processes, respectively. C_{oss} and C_{rss} are insensitive to TID, but a significant increase in input capacitance may lead to mismatches between the MOSFET and gate driver, causing systemic failures. Similar to the degradation results of V_{th} and R_{on}, gate voltage during irradiation accelerates the degradation of C_{iss}. In addition, a more pronounced degradation is observed in trench MOSFET compared with VDMOSFET.

The composition of three capacitances is jointly given by (1)–(3) [32]. Since the small changes in C_{rss}, changes in the C_{iss} are determined solely by C_{gs}. C_{gs} is given by (4), where changes in the V_{th} lead to variations in the depletion layer depth beneath the oxide under high bias conditions, affecting the depletion region capacitance. Depletion layer depth decreases, and C_{de} increases. Furthermore, the introduction of fixed charges in the oxide during the radiation process alters

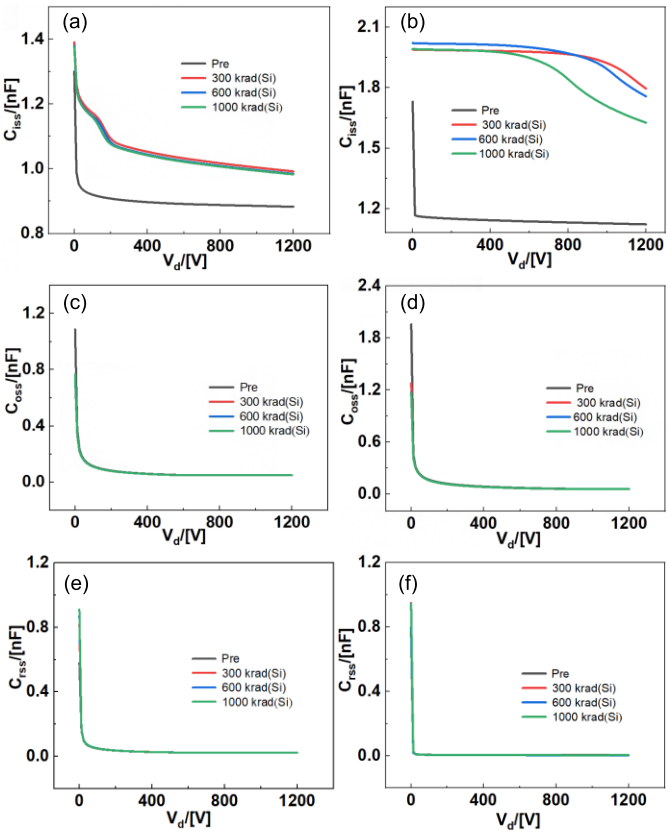

Fig. 7. C_{iss} of (a) VDMOSFET and (b) trench MOSFET during the irradiation. The C_{oss} of (c) VDMOSFET and (d) trench MOSFET during the irradiation. The C_{rss} of (e) VDMOSFET and (f) trench MOSFET during the irradiation.

the capacitance storage capability of the gate oxide, leading to an increase in C_{ox}. The combined variation of these two capacitances results in an increase in C_{gs}. The changes in C_{de} and C_{ox} are caused by the interface state and the fixed charge of the gate oxide, and an intuitive manifestation of the changes in the interface state and the fixed charge is the shift of V_{th}. In summary, all of the changed characteristic parameters are causally related to the variation in V_{th}. Therefore, predicting the degradation of V_{th} during the TID is informative

$$C_{iss} = C_{gs} + C_{gd} \tag{1}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{2}$$

$$C_{rss} = C_{gd} \tag{3}$$

$$C_{gs} = C_{\text{ox}} + \frac{C_{\text{pwell}} C_{\text{de}}}{C_{\text{pwell}} + C_{\text{de}}}. \tag{4}$$

In (1)–(4), C_{gs} is the capacitance between the gate and the source, C_{gd} is the capacitance between the gate and the drain, C_{ds} is the capacitance between the drain and the source, C_{ox} is the oxide capacitance, C_{pwell} is the P-well region capacitance, and C_{de} is the depletion region capacitance. The degradation of C_{ox} and C_{de} is related to fixed charges and interface density of states. It is effective in directing the perception of changes in fixed charges and interface density of states through the degradation of V_{th}. Therefore, predicting the degradation of V_{th} during the TID will be important and informative.

B. Threshold Voltage Degradation Modeling and Prediction

In the above section, it is demonstrated that the shift in V_{th} during the irradiation is primarily caused by the increase in positive fixed charges in the gate oxide. Therefore, accurate prediction of the fixed charges generated in the gate oxide during irradiation would enable the prediction of the V_{th} shift. The continuity equation for holes is given by the following equation:

$$\frac{\partial p}{\partial t} + \frac{\partial j_p}{\partial x} = G - R \tag{5}$$

where p is the hole concentration, j_p is the current density, $j_p = p(x)\mu_p E$, μ_p is the hole mobility, G is the hole generation rate, R is the hole recombination rate, expressed by $R = p(x)\tau_p$, τ_p is the hole lifetime, and H_{trap} represents the holes captured by the trap. During the irradiation, the hole generation rate G is related to the density of the irradiated material, the type of rays, and the dose rate, and it can be expressed by the following equation [26]:

$$G = \frac{\rho_{\text{ox}}}{1.6 \times 10^{-10} E_{\text{ergox}}} F(E) \frac{dD}{dt} \tag{6}$$

where ρ_{ox} is the density of SiO_2, E_{ergox} is the energy required to produce an electron-hole pair during ionization in SiO_2, and D is the dose during the irradiation. The yield is $g_0 = \rho_{\text{ox}}/1.6 \times 10^{-10} E_{\text{ergox}}$ $F(E)$, which is a value related to the electric field intensity in oxide. It represents the probability of carrier recombination generated during the irradiation. In the dual composite model that simultaneously considers sufficiently dense and relatively sparse situations, the approximation (7) of the $F(E)$ [33], [34] is

$$F(E) = \left(\frac{E + E_C}{E}\right)^{-m} \tag{7}$$

where E_c is the critical electric field that separates carriers, satisfying $E_c = \chi\mu$, where χ is the geometric mean of the absolute electronegativity of Si and O atoms, and m is a constant. For the 60Co used in the irradiation experiment of this study, $E_c = 0.65$MV/cm, and $m = 0.9$. At a steady state, $\partial p/\partial t = 0$ and the combination of (5)–(7) can be obtained. Under the influence of gamma irradiation, the current density j_p can be expressed by the following equation:

$$j_p = g_0 F(E) \mu_p \tau_p E \left[1 - \exp\left(-\frac{t_{\text{ox}}}{\mu_p \tau_p E}\right)\right] \frac{dD}{dt} \tag{8}$$

where E is the electric field intensity in SiO_2 and t_{ox} is the gate oxide thickness. In this study, it is considered that the electric field intensity in SiO_2 is uniformly distributed. By mathematical approximation, when the applied voltage is 0 V, $\mu_p \tau_p E/t_{\text{ox}} \to 0$ and $j_p \to g_0 F(E) \mu_p \tau_p E/t_{\text{ox}}\, dD/dt$. When the external electric field is large, because of the small thickness of the gate oxide, $\mu_p \tau_p E/t_{\text{ox}} \to \infty$, and $j_p \to g_0 F(E) t_{\text{ox}} dD/dt$. In the modeling, five following approximations are made, including.

1) Due to the fact that the neutral traps have a much smaller capture rate for charge carriers compared with hole trap charges, the capture of charge carriers by neutral traps is neglected.

2) The distribution of traps in the gate oxide is assumed to be continuous.
3) The gate oxide is treated as an infinitely large flat plate, disregarding the edge effects of the gate oxide.
4) The fixed charge value near the SiC/SiO_2 interface is considered constant and does not vary with the dose.
5) Under positive gate bias or zero gate bias, the hole density at the boundary near the SiO_2/gate metal side is assumed to be 0. These approximations are made to simplify the model and facilitate analysis, and they enable the establishment of a continuity equation for hole traps

$$\frac{\partial N_{hox}(t)}{\partial t} = \sigma_{ptox} j_{ptox} [N_{hox} - N_{hox}(t)] \tag{9}$$

where σ_{ptox} represents the trap's cross-sectional area for capturing holes in the gate oxide, expressed in terms of the cross-sectional area of the gate oxide; j_{ptox} denotes the hole current density in SiO_2; and N_{hox} is the surface density of hole traps at the SiC/SiO_2 interface. When the dose rate remains constant, substituting (8) into (9) yields as follows:

$$N_{hox}(D) = N_{hox} + N_{hox} \exp\left[-\sigma_{ptox} g_0 F(E) \mu_p \tau_p E \left[1 - \exp\left(-\frac{t_{ox}}{\mu_p \tau_p E}\right)\right] D\right]. \tag{10}$$

In summary, the V_{th} shift caused by gamma rays can be expressed as follows:

$$\Delta V_{ot} = \frac{-q t_{ox}}{\varepsilon_{ox}} \left\{ \begin{array}{l} N_{hox} + N_{hox} \exp\left[-\sigma_{ptox} g_0 F(E) \mu_p \tau_p E \\ \left[1 - \exp\left(-\frac{t_{ox}}{\mu_p \tau_p E}\right)\right] D \end{array} \right\} \tag{11}$$

where q is the electron charge and ε_{ox} is the dielectric constant of SiO_2.

Fig. 8 compares the V_{th} shift experimentally measured and the predicted results by the proposed model. When the electric field intensity is high, the results predicted by the model are in good agreement with the experiments. Since there are only three doses in the experiment of this study, to supplement the data and better verify the model, this study verified the correctness of the model through TCAD simulation. TCAD simulations rely on Mobility Models, Recombination Models, and Bandgap Narrowing Models, among others. The irradiation process also demands physical models such as Gamma Irradiation Models and Trap Distribution Models. The dose rate in the Gamma Irradiation Model is set to 50 rad(Si)/s, the source rise time (DoseTSigma) is 90 s, and the irradiation times are set from 2000 to 22 000 s with a step size of 1000 s. Fixed charges and interface traps follow an exponential distribution. It is indicated that when the dose is low and the electric field intensity is 0, the model cannot accurately predict the V_{th} shift at this time because the influence of interface trap charges is ignored. Since the trench, MOSFET reaches the saturation state later than the VDMOSFET when the gate bias is not loaded. At this time, there is a deviation between the model and the test value caused by interface trap charges.

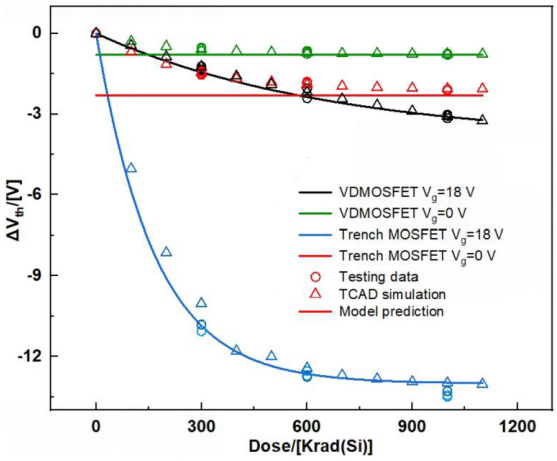

Fig. 8. V_{th} shift prediction, measured data, and simulation of SiC MOSFETs under irradiation environment.

IV. Conclusion

In this study, the TID effects on SiC VDMOSFET and trench MOSFET were investigated under the condition of gamma-ray irradiation at doses of 300, 600, and 1000 krad(Si). The reason why trench MOSFETs have poorer TID tolerance has been revealed. The results can be concluded as: first, the degradation trends of R_{on} and C_{iss} were similar to the degradation trend of V_{th}, which can be attributed to the shift in V_{th} increases the conductive widening of the channel caused by the degradation of V_{th}. The C_{ox} of the trench MOSFET is more sensitive to the TID effect. Next, HTA and HTGBA were performed to demonstrate the minimal impact of interface traps on SiC MOSFET degradation. Furthermore, interface states were found to be insensitive to TID for SiC MOSFETs. The defects affecting the TID tolerance of SiC MOSFETs were identified as fixed charges in the gate oxide. Finally, a prediction model was developed to establish the relationship between fixed charges in the gate oxide and the dose. For devices biased with gate voltage, the fixed charges in the gate oxide exhibited an exponential relationship with the dose. Generally, this study provides insights into the TID tolerance of SiC MOSFET power devices, which is helpful for the application of such devices in space operations and nuclear power plants.

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