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# Analysis of Conductance Variability in RRAM for Accurate Neuromorphic Computing

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***Abstract*—While Resistive RRAM (RRAM) offers attractive features for artificial neural networks (NN) such as low power operation and high-density, its conductance variation can pose significant challenges when the storage of synaptic weights is concerned. This paper reports an experimental evaluation of the conductance variations of manufactured RRAMs at the memory array level. Working at the memory array level allows to catch cycle-to-cycle (C2C) as well as device-to-device (D2D) variability and, hence, to propose a realistic evaluation of the conductance variation. Variability is evaluated with respect to the RRAM low resistance state (LRS) and high resistance state (HRS) conductance ratio. This ratio is selected as the parameter of interest as it guarantees the proper operation of the RRAM: the larger the ratio, the more reliable and robust the RRAM cell is in storing and retrieving data. The measurement results show that the conductance ratio is heavily affected by variability. Large spatial and temporal variations are reported, making challenging RRAM-based analog weight storage.**

***Keywords— RRAM, Variability, Neuromorphic, Computing, Synaptic weights, Reliability.***

## I. INTRODUCTION

Resistive RAM (RRAM) is a promising technology not only for large data storage but also to enable energy efficient computing solutions which could facilitate the deployment of artificial intelligence at the edge (edge-AI) [1]. However, not solving the issues related to no-idealities such as the variability in the electrical parameters of RRAMs (e.g., conductance variability) may block further development of the technology [2,3]. In RRAM-based neural networks (NN), conductance variability results in weight variability [4,5,6]. Weight variability can affect the network during training and inference, affecting the network ability to make precise predictions. The training process is particularly sensitive to the fluctuations of the synaptic weights [7]. Even slight variations can move the optimal work of the network, leading to uncontrolled accuracy loss during inference [8]. Therefore, there is an urgent need to analyze and quantify the conductance variability in RRAMs.

A solution to improve the network resilience against conductance fluctuation issues is to intentionally inject some noise into the synaptic weights during the training, exploiting a technique called variability-aware training (VAT) [9]. To obtain realistic results after the training process, such noise should be linked to the actual variability of the RRAM device, including device to device (D2D) and cycle to cycle (C2C) variabilities. However, this last point is neglected in many publications [10]. An alternative way to mitigate conductance fluctuations issues at the NN level is the mapping-aware biased training methodology [11] which consists in identifying RRAM conductance states inherently more immune to variation (favorable states). Then, a mapping-aware training technique is adopted where important weights are directly get mapped to such favorable states [12]. The mapping-aware training considers the inherent non-idealities of RRAM devices, such as variations in the conductance levels in the first place [12]. Therefore, detecting devices suffering from variability issues is a crucial step before considering a mapping-aware training methodology practical implementation. However, in this case as well, this aspect is not taken into account in many publications [13].

In this context, this paper advances the state-of the art by providing a silicon-based analysis of the conductance variability in RRAMs. Conductance variability is assessed quantitatively for each cell of a memory array test chip. Afterwards, a ranking of the cells more immune to variability is established. Finally, cells more favorable to weight mapping are derived from this ranking.

The main contributions of this study are summarized below:

- RRAM conductance variation silicon data are collected at the test chip level.
- A deep analysis of the conductance variation over multiple cycles is provided to understand the conductance stability and repeatability.
- Outcomes of this work are supported by silicon results related to an Oxide-based RAM (OxRAM) technology provided by ST-Microelectronics.

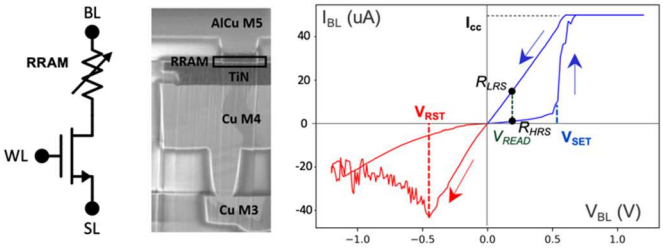
Considering that the limited precision of RRAM devices intended to map synaptic weights is addressed [14], outcomes derived from this study can be applied to any mapping technique currently used to implement RRAM-based NN accelerators, namely, (a) multilevel [15,16], (b) binary [17], (c) unary [18], (d) multilevel with redundancy [19] and (e) slicing [8]. Moreover, this study contributes to the understanding of the conductance variation in RRAMs [20] from an electrical standpoint, which is the first step before enabling accurate analogue computing with imprecise memory devices. Also, although functional silicon-based RRAM NN accelerators have been published in the literature [21,22], we cannot but notice that a demonstrator combining high recognition accuracy with analog weight storage and low-power operation is still missing.

The remainder of this paper is organized as follows. Section II introduces the specifications of the manufactured RRAM cells. Section III presents the experimental setup. Section IV reports the silicon measured data on RRAM conductance variability and analyze them. Section V shows

how the made analysis can enable accurate RRAM based neuromorphic computing. Finally, Section V concludes the paper.

## II. Specifications of the Manufactured RRAMs

RRAM devices typically operate based on the reversible change in resistance caused by the formation and rupture of conductive filaments (CFs) [15]. From a physical standpoint, when a voltage is applied across the cell (i.e., between the top and bottom electrodes), depending upon the voltage polarity, one or more CFs made out of oxygen vacancies are either formed or ruptured. Once the CFs are formed inside the metal oxide, bridging the top and bottom electrodes and leading to a low-resistance state (LRS), current can flow through the CFs. Subsequent resistance changes are achieved by rupturing the filaments. Applying a voltage with reversed polarity causes the filaments to break, leading to a high-resistance state (HRS). Fig. 1a presents the considered 1T1R RRAM device where one transistor (W = 0.8 µm and L = 0.5 µm) is connected in series with one resistive element (RRAM). The resistive element, shown in Fig. 1b, is incorporated in the Back End Of Line (BEOL) of a 130 nm technology, between metal layers [23]. The stack is deposited using Physical Vapor Deposition (PVD) where a 10 nm Hafnium dioxide ($HfO_2$) layer is placed on the top of a TiN Bottom electrode (BE). A Ti/TiN bilayer stack is then deposited as a top electrode (TE) to form a capacitor-like structure. Fig. 1c presents a classical 1T1R I-V hysteresis. Based on this characteristic, the 1T1R cell operation can be understood as follows: after an initial electro-Forming (FMG) step, the memory element can be switched reversibly between LRS and HRS. Resistive switching corresponds to an abrupt change between the HRS and the LRS. The resistance change is triggered by applying specific biases across the 1T1R cell, i.e., $V_{SET}$ to switch to LRS after a SET operation and $V_{RST}$ to switch to HRS after a RESET (RST) operation.




(a) (b) (c)

Fig. 1. (a) Symbol view of a 1T1R cell. (b) SEM cross section of the RRAM stack [23]. (c) RRAM I-V hysteresis.

TABLE I. Standard Cell Operating Voltages

| | FMG | RST | SET | READ |
|---|---|---|---|---|
| WL | 2 V | 2.5 V | 2 V | 2.5 V |
| BL | 3.3 V | 0 V | 1.2 V | 0.1 V |
| SL | 0 V | 1.2 V | 0 V | 0 V |
| Resistance | 10 kΩ | 240 kΩ | 15 kΩ | - |
| Conductance | 100 µS | 4 µS | 66,6 µS | - |

The voltage levels used during the different operating steps are presented in Table I, along with the nominal resistance and conductance values. Note that a nominal conductance ratio around 16 is obtained for the targeted technology (66,6 µS / 4 µS, see Table I). During the read operation, typically, a small read voltage (0.1 V) is chosen to not disturb the current state of the cell. In practice, at the circuit level, the read operation is performed by sensing the current associated with the cell resistance to determine whether the cell is in logic '0' (HRS) or in logic '1' (LRS). It is worth noting that in the 1T1R configuration, the transistor controls the amount of current flowing through the cell according to its gate voltage bias. This clamping current is referred to as the compliance current ($I_{CC}$).

## III. Experimental Setup

Fig. 2.a presents the test chip considered for measurements which is a classical 1T1R array. Memory cells are grouped to form eight 8-bit memory words. Word Lines ($WL_X$) are used to select the active row, Bit Lines ($BL_X$) are used to select active columns during a SET operation and Source Lines ($SL_X$) are used to RST a whole memory word or an addressed cell. To allow a full flexibility during characterization, BL, WL and SL nodes are externally available. During the RRAM cell characterization, the extraction of $R_{LRS}$ and $R_{HRS}$ is achieved using 1 ms DC voltage sweeps with a 1 mV voltage step; the applied voltage increases step by step and the current flowing through the cell is measured, allowing an extraction of the I-V characteristics of each cell. Fig. 2.b presents a view of the fabricated memory array. Due to the limited pin out of the probe card, only a 7x7 memory array is available for our experiments (i.e., a subset of the 8x8 array).

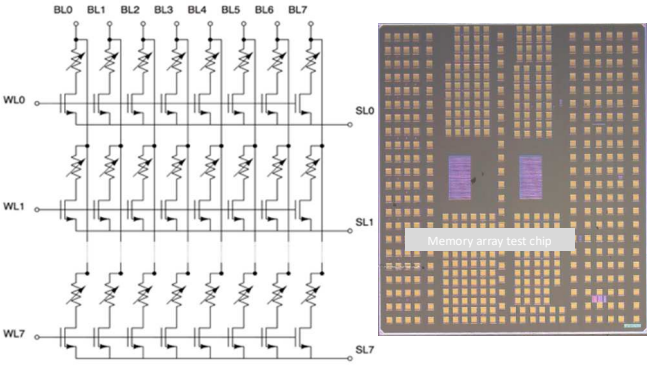



Fig. 2. (a) 8x8 RRAM memory array and (b) physical view of the fabricated memory array.

Before any operation, the memory array is first formed (FMG). Then, memory cells are RST one by one to extract the $R_{HRS}$ value at 0.1 V. After RST, cells are SET to extract the $R_{LRS}$ value, also at 0.1 V. The RST/SET process is repeated 230 times for the whole array in order to catch C2C as well as D2D variability. The measurement protocol seen by each cell of the array is presented in Fig 3.

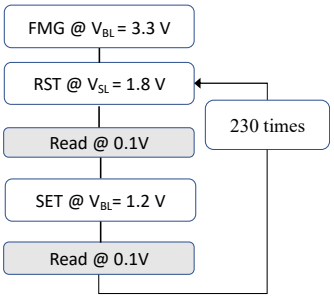
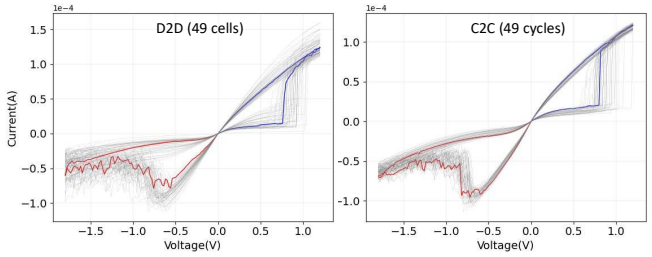



Fig. 3. Measurement protocol: after FMG, a RST/SET operation is repeated 230 times for each addressed cell. RST and SET operations are followed by a read operation to extract the cell resistances.

## IV. EXPERIMENTAL RESULTS

### A. Preliminary results

Although RRAMs have shown interesting properties, one of the most important challenges of the technology is the control of the device variability (temporal and spatial) in both LRS and HRS states [24, 25]. In fact, variations of $R_{HRS}/R_{LRS}$ are so unpredictable that they have been employed as an entropy source in True Random Number Generators (TRNG) [26, 27]. Fig. 4 shows the impact of D2D and C2C variability at the I-V characteristic level after RST/SET operations applied to each of the 49 cells of the memory array (D2D variability, Fig.4a) and after a RST/SET operation applied only 49 times (for comparison purposes) to an isolated cell of the memory array (C2C variability, Fig.4b). The nominal characteristic is highlighted in red (RST) and blue (SET) colors. Based on these preliminary measurement results, it appears clearly that HRS and LRS resistance/conductance is affected by spatial and temporal variations. Hence, this non-ideality has to be considered when designing RRAM-based NN. In this context, the next section proposes a quantitative analysis of conductance variations. A cell tracking analysis will be conducted in order to monitor the evolution of the conductance ratio of each cell of the memory array presented in Fig. 2a over 230 programming cycles. The state of individual memory cells will be tracked to detect cells that deviate from their nominal behavior (i.e., deviation from the nominal conductance ratio of 16).




(a) (b)

Fig. 4. Experimental evidence of (a) cell level D2D variability and (b) cell level C2C variability. The nominal characteristic is highlighted in color.

### A. Conductance ratio variability evaluation

In Fig. 5, the evolution of the LRS/HRS conductance ratio of three different cells (i.e., located at three different addresses) is presented in the logarithmic scale. Cell (5;0), where '5' and '0' represent the WL and BL line numbers respectively, is the most affected by variability.

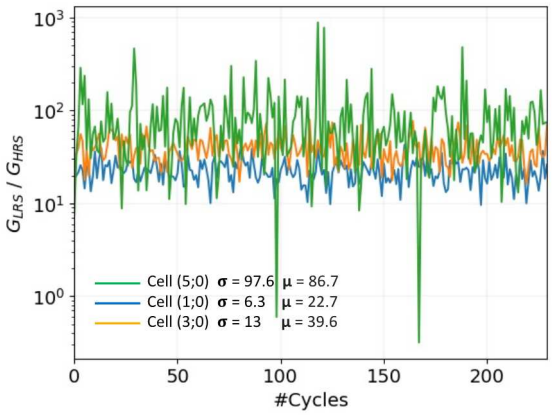



Fig. 5. Conductance ratio versus the number of RST/SET cycles for 3 different cells of the memory array presented in Fig. 2a.

Large conductance fluctuations are reported with a conductance ratio standard derivation σ = 97.6 with respect to its mean value μ = 61.5. In contrast, cell (1;0) and cell (3;0) are less impacted with standard derivation values equal to 6.3 and 13 respectively. Note that for cell (5;0), the conductance ratio falls below one in two cycles, resulting in an overlap between LRS and HRS conductance levels. Hence, this cell needs to be avoided for synaptic weight storage. The evolution of the conductance ratio standard derivation of the 49 cells of the memory array is provided in Fig.6a. The standard deviation ranges from 2.8 (min. value) to 97.6 (max. value). A 2D representation of the standard deviation values over the memory array is presented in Fig.6b. Each cell is associated with a variable degree of grey. The whiteness of a cell reflects lower standard deviations. The white color being associated with the minimal standard deviation and the black color with the maximal standard deviation. For instance, cell at location (5;0), associated with a black color, is the most affected by variability with a standard deviation of 97.6, while cell at location (4;5), associated with a white color, is the least affected by variability regarding its standard deviation of 2.8.

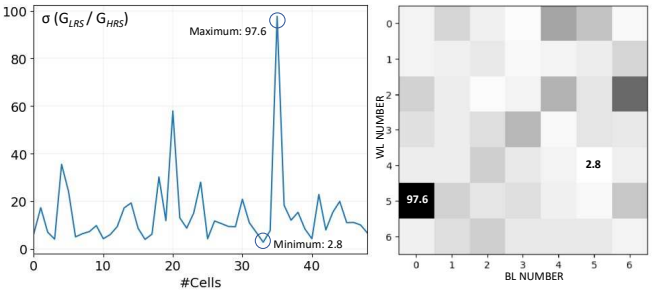



Fig. 6. (a) Evolution of the conductance ratio standard deviation of each cell of the memory array. (b) Topological representation of the standard deviation of each cell of the memory array. The values of the most impacted cell (97.6) and least impacted cell (2.8) are reported in (a) and (b).

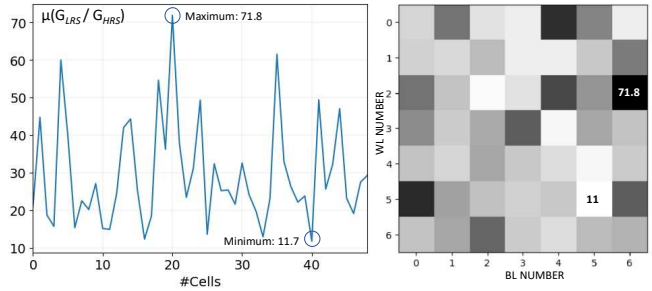



Fig. 7. (a) Evolution of the conductance ratio mean value of each cell of the memory array. (b) Topological representation of the mean value of each cell of the memory array. Largest and smallest values are reported in (a) and (b).

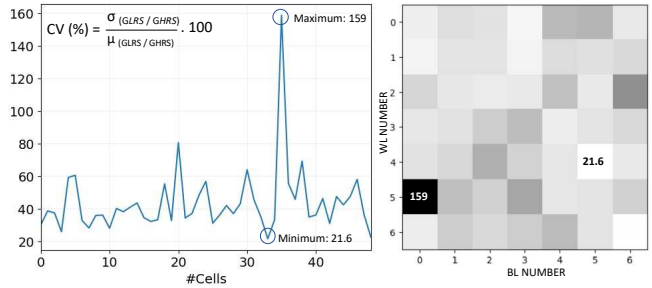



Fig. 8. (a) Evolution of the coefficient of variation CV of each cell of the memory array. (b) Topological representation of CV for each cell of the memory array.

Fig. 7 presents the evolution of the mean value of the conductance ratio for each cell of the memory array. Interestingly, this parameter is also affected by variability, demonstrating that the conduction window differs across the cell in the array. The fluctuation of the mean value of the conductance ratio is a relevant information when NN weight mapping is concerned as narrowing the conductance window results in a significant reduction in the conductance modulation capability of the cell (i.e., reduction of the number of analog conductance levels).

Fig. 8 presents the evolution of the ratio of standard deviation to the mean value (σ/μ) for each cell of the memory array. This parameter is a dimensionless quantity that is used to measure the relative variability of the conductance ratio dataset, even if the datasets have different scales (i.e., different mean values). It is referred to as the coefficient of variation CV. The formula for calculating CV is given in (1).

$$CV\ (\%) = \frac{Standard\ deviation}{Mean}.100 = \frac{\sigma}{\mu}.100 \quad (1)$$

Dividing the standard deviation by the mean value essentially standardize the measure of the variability. In Fig. 8a, the minimum CV value of 21.6% indicates that the standard deviation is relatively small compared to the mean, while the maximum CV value of 159% suggests a larger relative variability. As this parameter combine the influence of the standard deviation and the mean value, the latter will be considered in the upcoming discussion section.

## V. VARIABILITY AWARE NEUROMORPHIC COMPUTING

The proposed analysis revealed that conductance variability is a major concern in RRAM technology for computing. Hence, outcomes of this study are crucial for anticipating the functionality and reliability of NN relying on individual RRAM cells to store the synaptic weights.

The conductance ratio has been chosen as the main criterion to assess the robustness of RRAMs used in neuromorphic computing applications for two reasons: (i) a stable conductance ratio is essential for consistent learning processes, enabling the network to adapt to new information while updating the previously stored information (ii) a high conductance ratio provides a larger dynamic range for multi-level cell storage (MLC [28]) which enables better differentiation between different synaptic states, turning the NN more robust. The conductance ratio is monitored against 230 RST/SET programming cycles. A number of 230 cycles allows to assess the stability of the conductance ratio, without wearing out the memory cells. In other words, a time-zero robustness evaluation is conducted before the implementation of RRAMs as synaptic weights where reliability parameters such as endurance and retention come into place. A dataset of 230 conductance ratios is extracted for each cell of a memory array. The standard deviation, the mean value and the CV parameters have been computed to analyze the behavior of each cell. Based on the CV parameter, a ranking of the most favorable cells (i.e., cells with lower μ/σ ratio) is proposed in Table II. The CV parameter (column 2) accounts for both the stability (σ contribution, column 3) and the mean value (μ contribution, column 4) of the conductance ratio. The addresses of each cell are reported in column 5.

According to Table II and based on the NN application requirements, favorable conductance states presenting low CV values can be chosen to map significant weights [13]. Conversely, conductance states presenting high CV values (such as the worst cell in Table II last column) can be skipped during the weight mapping process due to less immunity to variations.

TABLE II. FAVORABLE CELLS RANKING

| # | CV | σ | μ (S) | (WL; BL) |
|---|---|---|---|---|
| 1 | 21.6 | 2.79 | 12.04 | (4;5) |
| 2 | 22.4 | 6.58 | 29.33 | (6;6) |
| 3 | 25.8 | 4.07 | 15.72 | (0;3) |
| 4 | 28.0 | 4.25 | 15.15 | (1;3) |
| 5 | 28.2 | 6.35 | 22.53 | (1;0) |
| 6 | 30.2 | 6.33 | 20.97 | (0;0) |
| 7 | 31.0 | 7.95 | 25.64 | (6;0) |
| 8 | 31.1 | 4.24 | 23.62 | (3;4) |
| 9 | 32.2 | 3.97 | 12.35 | (2;2) |
| 10 | 32.7 | 11.80 | 36.25 | (2;5) |
| Worst cell | 159 | 97.6 | 61.5 | (5;0) |

While the conductance ratio variability is an important criterion at time zero [29], it is worth noting that time-dependent reliability metrics [6] such as endurance, retention and read/write stress also play a critical role in determining the robustness of RRAM-based NNs. Particularly, cycling and endurance can lead to hard errors (memory cell stuck at one conductance state forever, with a conductance ratio stuck at one [30]). Also, similarly to other emerging memory technologies, RRAMs is subject to defects that directly impact the conductance ratio [31]. Therefore, appropriate test mechanisms are required to detect RRAM-related failures due to these defects [32,33]. Beyond RRAMs, the NN CMOS subsystem variability [34] (including the neurons [35], the RRAM reading [36] and programming circuitry [37,38]) can also impact the conductance ratio. Hence, a complete analysis strategy [39] has to be defined to mitigate the impact of all these non-idealities on the conductance fluctuations in RRAM-based NN accelerators.

## VI. CONCLUSION

The existing of important fluctuations in RRAM conductance has been experimentally established after applying a limited number of programming cycles to individual cells of a memory array. The electrical behavior of each cell of the array has been analyzed at the electrical level. We have reported a large range of variation of the conductance ratio standard deviation (from 2.79 to 97.6) as well as its mean value (from 12.04 to 61.5). After having computed the coefficient of variation CV of each cell of the array, a large variation of this parameter was also reported (from 21.6 to 159). In the light of these findings, and as future perspectives, this study has motivated the design of hardware and software solutions intended to mitigate the impact of the conductance variability to ensure the correct operation of RRAM-based neuromorphic systems.

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