Optimisation of LPCVD-SiN_x Membrane for Micro-hotplates/Nano-Reactors

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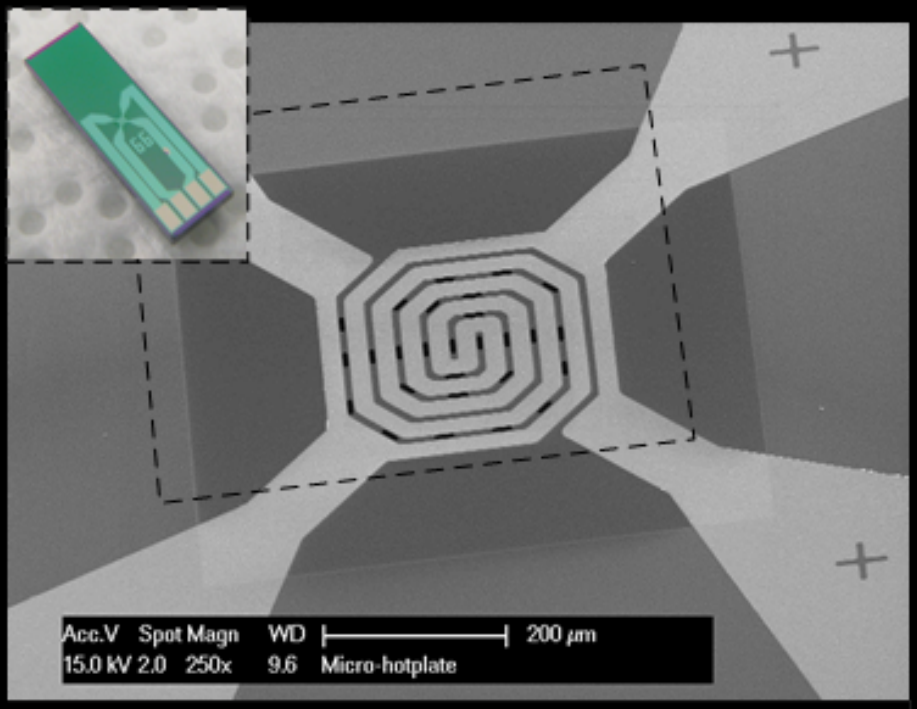

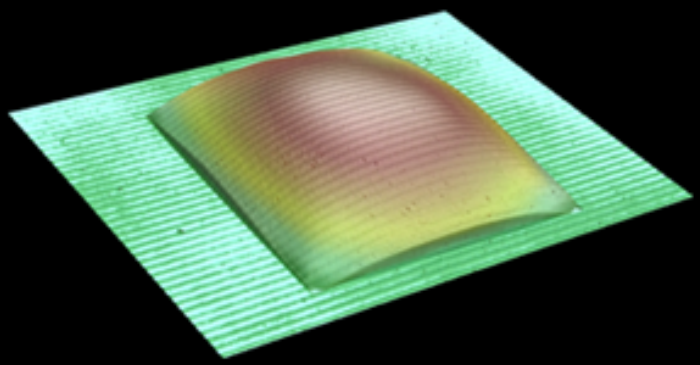

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Challenge the future

Optimisation of LPCVD-SiN_x Membrane for Micro-hotplates/Nano-Reactors

by

Sarat Shankar Sinha

in partial fulfillment of the requirements for the degree of

Master of Science
in Electrcal Engineering

at the Delft University of Technology,
to be defended publicly on Monday March 26, 2018 at 13:00 PM.

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This thesis is confidential and cannot be made public until March 26, 2019.

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Abstract

Micro-hotplate and Micro-hotplate integrated Nano-reactors are a revolution for in-situ observations in Transmission Electron Microscopy (TEM) imaging. They currently operate at about 400^0C without any problems. The SiN_x membranes of micro-hotplate and nano-reactors have integrated micro-heater along with electron transparent windows. The major problem is the shift in 'z' direction of the membranes as a function of pressure and temperature. This creates a change in focus during in-situ TEM imaging affecting the image quality. Net compressive forces can be a reason for bending of membranes, as far as temperature is concerned. Thus, introduction of residual tensile stress was considered to solve this problem. Simple COMSOL simulations were made using plate models to verify the effect of residual tensile stress in membranes as a function of temperature and pressure individually, as well as a combination of both. It was concluded that residual tensile stress does reduce thermal buckling. It also reduces the bulging due to pressure but bulging as a function of pressure can't be made zero. It also concludes thermal buckling is more dominant at lower pressure and pressure bulge is more dominant at higher pressure.

Different residual stress LPCVD-SiN_X films were deposited and material properties like Young's modulus, refractive index and density were characterized. A saturation to the deposition and residual tensile stress was found as a function of gas-ratio. Surface morphology and IR spectra were also determined using AFM and FTIR respectively. All the characterization done proves the change in material composition with fabrication parameters. The introduction of high residual stress questions the reliability of the membrane and hence, there was a need to check if high tensile residual stress doesn't break the membranes. Thus, a new device for wafer level pressure testing of membranes was designed and fabricated. The pressure bulge test was done and reflections were recorded for various pressure and stress levels. The membranes were found reliable up to a pressure of 1.5 bar. New generation of micro-hotplates were fabricated using this concept and an increment of 400^0C in the operating temperature of micro-hotplates and nano-reactors, without any-shift in 'z' direction due to temperature, was achieved.

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K	Reaction rate coefficient
A	Area
R	Resistance
T	Temperature
E_a	Activation Energy
P	Pressure
d	Deflection
ν	Poisson's ratio
σ	Stress
GA_{av}	Average grain area
GW_{av}	Average grain width
S_Q	Root mean Square Roughness
I	Moment of Inertia
ρ	Resistivity, Density
k	Thermal Conductivity

Abbrevations

AFM	Atomic Force Microscopy
CTE	Coefficient of Thermal Expansion
DSP	Double Side Polished
EBR	Edge Bead Removal
EKL	Else Kooi Laboratory
FEM	Finite Element Method
FTIR	Fourier Transform Infra Red
GR	Gas Ratio
LPCVD	Low Pressure Chemical Vapour Deposition
MEMS	Micro-Electro Mechanical Sensors
SEM	Scanning Electron Microscope
TCR	Temperature Coefficient of Resistance
TEM	Transmission Electron Microscope
VCO	Voltage Controlled Oscilloscope

CHEMICAL FORMULAE

BHF	Buffered Hydrofloric Acid
DCS	DichloroSilane
HF	Hydrofloric Acid
HNO_3	Nitric Acid
KOH	Poatassium Hydroxide
PES	Poly Ether Sulfone

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Background and Motivation

1.1. Chemical Reaction and Catalysis

Every new evolution is a result of slow, moderate or fast reactions occurring either in nature or artificially in lab. Therefore, it fascinates a huge group of people to investigate these reactions to know the fundamentals of change. With advancements in science, our capability to look at molecular and atomic level has deepened our understanding of reactions. The changes in reactions, specially the contribution of catalysts, at nano or atomic scale results in the formation of properties at macro level [1].

A catalyst is a substance that influences the rate of chemical reaction but doesn't participate in the reaction itself and catalysis is the process in which catalysts are used. Broadly, a catalyst can be classified into two types: positive catalyst and negative catalyst. A positive catalyst increases the rate of reaction and a negative decreases the rate of reaction. Positive catalyst are widely used. Negative catalyst are used when the rate of reaction is vigorously high and sometimes to slow down the high exothermic release of energy. This increase or decrease in the rate of reaction is ruled by activation energy.

Activation energy is the minimum energy required to start the chemical equation. The mathematical governance is given by the Eq. (1.1)

$$K = Ae^{-}(\frac{E_a}{RT}) \tag{1.1}$$

where K is the reaction rate coefficient, A is the frequency factor, R is the gas constant, T is the absolute temperature and E_a is the activation energy. From Eq. (1.1), it can be seen that the activation energy influences the rate of reaction.

Positive catalysts helps in lowering the activation energy barrier and thus helps in increasing the rate of reaction. Apart from this Eq. (1.1) states the dependence of temperature to the rate of reaction. Also the frequency factor A, depends on the collision between particles. The collision in turn depends on the concentration and partial pressure of gases. Thus, temperature and pressure are the two most important variable that influences the rate of reaction apart from activation energy.

It is very important to investigate both the reaction as well as catalysis at nano-level to understand its fundamental effect on the overall reaction. It has to be done at certain pressure and temperature to study the rate of reaction and its influence to the system. There are tools and techniques that are used for observing reaction between nano-particles in presence of nano-catalysts.

The best tool available for observing these reactions at atomic level is Transmission Electron Microscope (TEM) [2]. The chapter further deals with the TEM, the limitations of TEM, devices used to overcome those limitations and finally research questions and outline of the thesis.

1.2. Transmission Electron Microscope

TEM is one of the tools that can investigate nano-particles. A working diagram of TEM is shown in Fig. 1.1

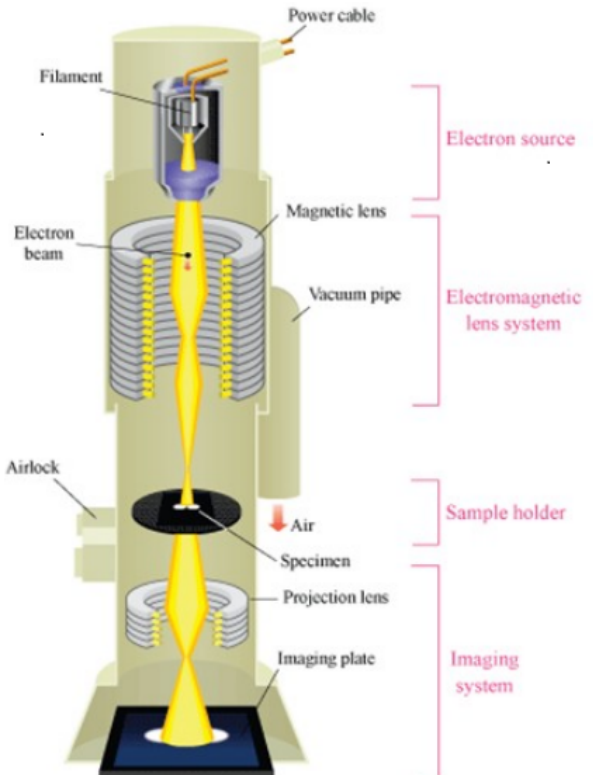

Figure 1.1: Working of Transmission Electron Microscope

The electrons are generated from electron gun and are channeled through magnetic lenses to make a concentrated beam of electrons. The sample is maintained in vacuum. TEM follows a similar steps as Rutherford's experiment. The electron beam with such high energy and intensity penetrates the sample, where the density of atoms is less. The electron rebounds where the density of atoms is high. The transmitted electron are collected and an image is formed.

The main point to be noted here is that the TEM is operated in vacuum. It can observe the materials kept in vacuum. The vacuum is important to make the mean free path of electron to be large and also to reduce the scattering of electron. More the scattering, less electrons will reach the detector and thus the quality of image will be reduced. Chemical reactions which requires ambient temperature and pressure are difficult to be studied under TEM due to the vacuum limitations, specially for in-situ observation. The problem has been solved by introduction of micro-devices. One such device is discussed in the next section. It acts as an add-on for the TEM to provide ambient temperature and pressure without disturbing the vacuum of the TEM.

1.3. Integrated micro-hotplate/nano-reactor for in-situ TEM

There are two devices under discussion:

- The Micro-hotplate: A micro-heater with integrated electron transparent windows, which serves also as the core sub-component in the nano-reactor.
- The Nano-reactor: A micro hotplate with a an additional covering on the top to form a gas-channel

The need for in-situ observation inside TEM led to the invention of a device called "Nano-reactor".The nano-reactor is an integrated device with a MEMS micro-hotplate, electron transparent window and

a gas channel packaged as a single system. This device can be used as an independent source for observation in TEM if gas flow (pressure) is not needed. It has been a revolution since then. Lots of reaction involving phase changes [3, 4], study of nano-particles under various environmental and industrial conditions [5, 6], kinetics [7], formation of dislocations [8, 9] and may more such phenomena has been observed and reported. The schematics of Nano-reactor is shown in Fig. 1.2.

Creemer[10] first time successfully fabricated windows integrated environment cell with windows using micro-fabrication techniques and ultra thin transparent windows.

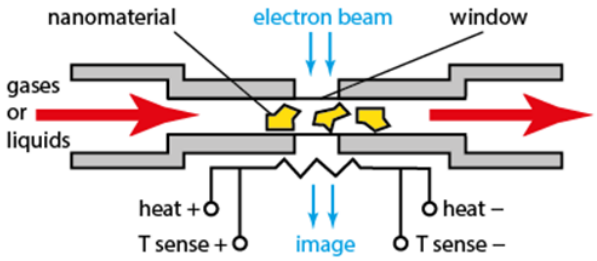

Figure 1.2: Nano-reactor Schematic

The nano-reactor can be broadly broken down into three major components:

- The micro-hotplate
- The Electron Transparent Windows
- The gas channel

The first two in the list mentioned above makes the micro-hotplate for TEM and if the third item in the list is also included it becomes a nano-reactor. The descriptions in thesis are individually applicable for both the both the device if working independently. These components are discussed in detail in the Section 1.3.1, Section 1.3.2 and Section 1.3.3

1.3.1. The micro-hotplate

The ambient temperature that is needed for the chemical reaction is provided by this micro-hotplate. The micro-hotplate consists of four-contact pads. Two are used for current injection and two are used for sensing the voltage across the membrane. So, the two contact pads on which voltage is sensed helps in finding the real time temperature inside the channel.

From, Fig. 1.3, the micro-hotplate in various capacity can be seen. Fig. 1.3(a) shows the micro-hotplate on a membrane. The interesting part is Fig. 1.3(b), where an enlarged view of the same can be seen and compared with the cross-sectional view in Fig. 1.3(c) for better understanding. It can be clearly seen from Fig. 1.3(b)-(c) about the coils of micro-hotplate and how the electron transparent window is embedded inside it. The coil is designed in such a way that it can accommodate windows in between and has access to the ambient temperature required. Thus, it is really important to know the temperature distribution across the heaters in order to know the accuracy of results. The uniformity [11], thermal stability and power consumption can be taken as choice with the selection of material used as well as the design of micro-heater.

Some of the most commonly used materials are Silicon, Platinum, Molybdenum, Titanium Nitride, Silicon Carbide and tungsten [10, 12, 13]. Some of the design considerations can be found in [14, 15].

The micro-hotplate made in this thesis uses platinum as the material with a sputtered thickness of 100 nm. The heater design is considered from [12]. It should be noted that these micro-hotplates are also used independently for TEM observations and many other sensor applications.

1.3.2. Electron Transparent Windows

In Fig. 1.2, the electron transparent windows are indicated. It is also shown in Fig. 1.3(b) and (c) as top and cross-sectional view of the placement of these windows. The main objective of these

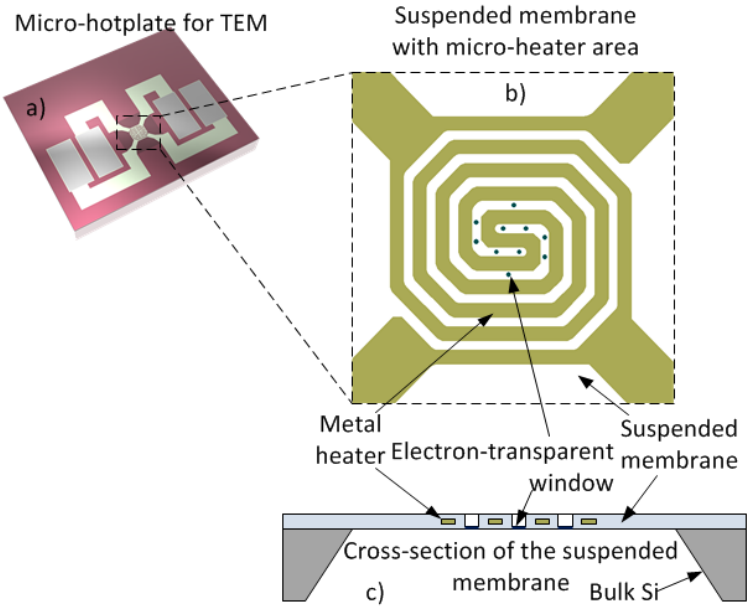

Figure 1.3: (a) Micro-hotplate with micro-heater on the suspended membrane (b) enlarged view of suspended membrane with metal heater and (c) The cross-sectional view showing the membrane,Electron transparent windows, micro-heater and the suspended membrane

windows comes from the name itself, i.e., electron transparent. Electron transparency means reducing the scattering of electron. With lower scattering of electron, more electrons will reach the detector and thus better imaging. The scattering depends on material density, atomic number and thickness [16].

Windows also avoids the leakage of gas from the reaction chamber and thus helps to maintain the vacuum of TEM. Thus mechanical reliability of the membranes are equally important along with the flatness of membrane. Any bending in the membrane will decrease the resolution of imaging. Some of the materials used to produce are silicon di-oxide [17], silicon carbide [13], silicon nitride [10] and Alumina [18]. Presently, graphene [19] is in research for the same. The integration of windows in nano-reactors can be seen in Fig. 1.2. The electron transparent windows used in this thesis are made with LPCVD SiN_X with thickness of 20nm.

1.3.3. Gas micro-channel

When the micro-hotplate gets covered by an another suspended silicon nitride layer a gas channel is formed over the micro-hotplate, making the device work as a nano-reactor. The upper membrane also acts as a passivization membrane and the lower membrane supports the micro-hotplate. These membranes have gas inlets and outlets as shown in the Fig. 1.2. The mechanical reliability of the membrane becomes important due to two reasons:

- The gas pressure may cause the stress in the membrane.
- As the micro-hotplate is sandwiched between these two membrane, it becomes really important to look into thermal conductivity and thermal stress induced in the membrane.

LPCVD SiN_X serves as a good option and has been used extensively in recent past [10, 20, 21]. This is because of its high Young's modulus, inertness and thermal stability. Silicon Carbide is also an option [13]. The membranes in this thesis are made up of SiN_x. The thickness of the upper membranes and lower membranes are approximately 200nm.

1.4. Current generation Nano-reactor

The current generation from a fabricated device to a chip as shown in Fig. 1.4 shows the current commercial micro-hotplate with Molybdenum as the heater material, manufactured at EKL, TU Delft.

Currently, the membranes are manufactured using Low Pressure Chemical Vapour Deposition (LPCVD)

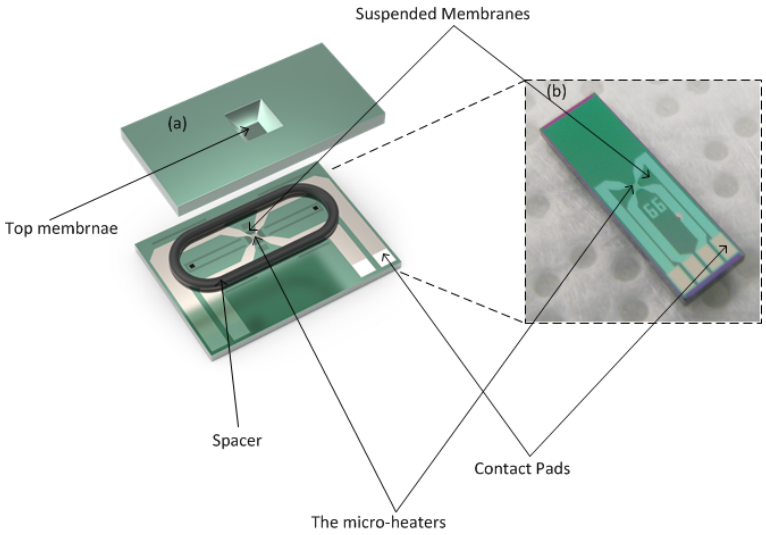

Figure 1.4: (a) Open configuration of Nano-reactor and (b) The fabricated micro-heater

SiN_x. The transparent electron windows are also made using LPCVD SiN_x. Nano-reactors can be classified into two types when it comes to placement of the two suspended membranes.

- Open membranes
- Closed membranes

Open membranes

The open membranes are shown in Fig. 1.4(a). In this configuration, the top and bottom membranes are completely separated. The samples are loaded in the lower membrane with micro-hotplate and then the structure is closed with top membranes. The distance between the two membranes is kept constant with the help of fabricated spacers (O- rings). This configuration is more popular due to ease of loading the samples. Unfortunately, it can only operate without bulging up till 1 bar and temperatures up to 400^oC. Above a temperature of 400^oC bulging can be observed as a fuction of temperature.

Closed membranes

The top and bottom are kept intact at a constant separation with the help of micro-pillars fabricated as shown in Fig. 1.5. The micro-pillars make it a very complex device with respect to loading of samples but at the same time, this configuration of devices can sustain higher pressure (up to 14 bar) and relatively higher temperature range of 660^oC, which is more closer to the industrial standards [22].

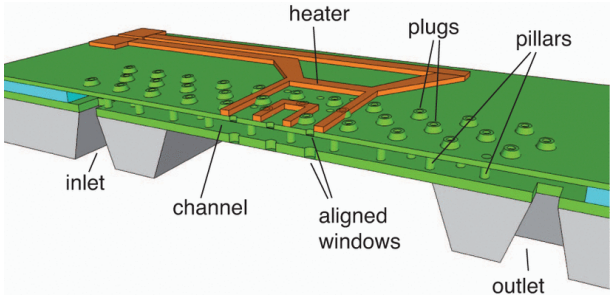

Figure 1.5: closed configuration of nano-reactor

The commercial trend of production is more tilted towards the open membrane configuration because of its ease to load samples. The rest of the thesis is based on open membrane configuration. Nano-reactor mentioned in this thesis means an open configuration until and unless stated otherwise.

Limitations of Current Generation Micro-hotplate/Nano-reactors

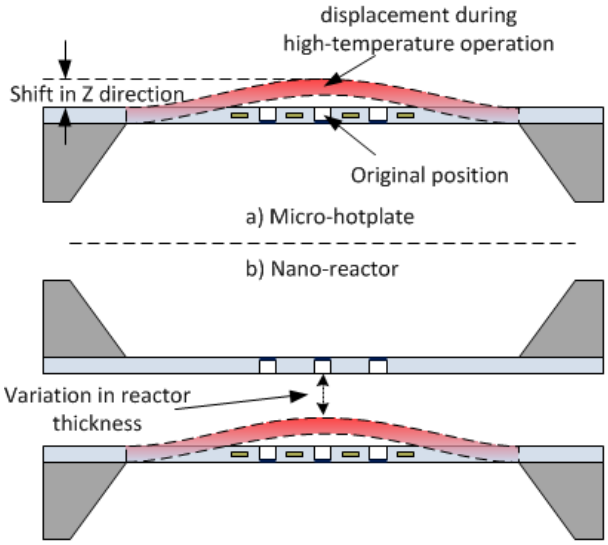

Figure 1.6: The shift in 'z' direction in case of (a)Micro-hotplate and (b) Nano-reactor

Short term limitations are important for the continuation of long-term research. Some of the major problems that the current generation Nano-reactor faces are as follows:

- The bulging in the suspended membrane for a temperature higher than 400^{o}C.
  - The bulging in the suspended membrane causes a shift in 'z' direction which changes the path length travelled by the electron to reach the detector. The change in optical path length shifts the focus of the TEM creating hindrance in the in-situ observation.
  - The bulging changes the volume of the nano-reactor channel as shown in Fig. 1.6(b). The change in volume changes the number of gas molecules inside the channel and thus the ambience of in-situ observation is disturbed. The number of molecules per unit volume inside the channel also changes, which may create scattering. The partial pressure of the channel will also change and this may affect the kinetics of the reaction.
  - This also creates mechanical reliability issues with the membranes and may affect the life time of membranes.
- The pressure in channel is presently limited to 1 bar.
  - Lots of industrial process are conducted at a pressure higher than 1.5 bar. Although closed membranes overcome this problem, the open configuration is still struggling with the problem.
  - The pressure also creates stress in the membrane and introduces a shift in 'z' direction, which leads to bulging as discussed above.
- The pressure testing of LPCVD-SiN_x membranes or in general thin films membranes
  - The pressuring testing of micro-hotplates are done after dicing all the chips from wafer and placing them in special holders to see the bulging individually.

There are also lot of other issues like transparency of electron windows, wetability of membranes, thermal inertness, uniformity in temperatures distribution and a lot more.

This thesis focuses on the bulging problem of the membranes of LPCVD SiN_x for micro-hotplate and nano-reactor and its reliability.

1.5. Formulation of research questions/goals

Taking into considerations the limitations of the system, some of the research goals have been formulated as a master thesis. The research goals are as follows:

- Understand the nature and causes of bulging in thin films due to temperature and pressure.
- Tuning the deposition process parameters of thin film SiN_x layer and study the mechanical property of the SiN_x layer.
- Improve the membranes of the micro-hot plate in order to minimize the bulging of membranes at high temperatures.
- Setting up a wafer-level pressure testing system of micro-hotplates.
- Characterize the SiN_x according to the changes in fabrication parameters.

1.6. Organization and structure of this thesis

This thesis starts with analyzing the causes for the shift in 'z' direction of the suspended membranes. To study this, it is important to discuss and understand the mechanics behind the phenomena. This has been done in Chapter 2. This chapter also gives out some basic simulations to show the effect of residual stress on SiN_x membrane on shift in 'z' direction of the membrane. It integrates the concepts of residual stress with temperature and pressure.

Once the concept was found to be beneficial for tackling the 'z' direction shift problem, it is time to study the complete theory of residual stress. This is where Chapter 3 comes into picture. This chapter studies the sources of residual stresses and how films with residual stress can be manufactured. Once the films are manufactured, it was necessary to know if the introduction of residual stress changes the basic material properties of the thin film. Various characterization concepts like stress, strain, density, Young's Modulus, optical constant, surface roughness and IR spectrum were used to highlight the changes in some of the material properties.

By knowing that the residual stress can be generated by varying LPCVD SiN_x parameters, in Chapter 4, the SiN_x layers are produced with different tensile residual stresses and membranes are made using this. A new method for wafer-level pressure testing has been developed to check the reliability of membranes with varying tensile residual stress under pressure loading. Wafer level Bulge testing setup has been done to record the deflection at various pressure. This data was further used to extract Young's modulus using COMSOL models. The data was compared with rotating pointer method in Chapter 3 and both the data are in agreement.

The next chapter, Chapter 5, the concepts to make new generation of micro-hotplates are applied. TCR and thermal buckling characterization has been done and it shows a substantial increase in the operating temperature of micro-heaters without any shift in 'z' direction. The concept of change in residual stress seems to be working and has been proved towards the end of the chapter.

Chapter 6 concludes this thesis by highlighting the important conclusions from the thesis and suggestions for future work.

2

Theory and Residual Stress Simulations

2.1. Introduction

In order to study the effect of stress, it is important to do some preliminary examination with the help of simulations as well as some available mathematical equations, to make sure that stresses can make a difference in the shift in z-direction of the membrane. It will also give an idea of the intuitive range of stress which has to be focused. With the preliminary examination it can be concluded if the change in stress affects the shift in 'z' direction, then it can be dealt in detail and fabrication can be performed.

It is known that the membrane is under the influence of both temperature and pressure. It will be interesting to see the influence of stress on a thin film as a function of temperature and pressure. This chapter deals with micro-heater simulations to find out the mechanism of working, as well as to get an idea and range of temperature distribution. This has been discussed in Section 2.3.1. The concept of bulging and buckling phenomena is shown in Section 2.2.1. The next Section 2.2.3 deals with the plate theory, which is further used to make some basic simulations.

2.2. Solid Mechanics Background

The simulations discussed in this section is based on the concepts of Solid Mechanics. Thus it is really important to discuss some concepts here.

2.2.1. Buckling vs bulging

The shift in 'z' direction of the membrane is the real problem for both the nano-reactor and micro-hotplate applications. In this chapter this has been decomposed into buckling and bulging of membranes.

Bulging

Bulging is the phenomena that occurs when a load is applied perpendicular to membrane. The membrane in this case is the silicon nitride and the perpendicular load applied is pressure. The pressure given at the bottom creates a tensile stress in the membrane and to release that stress the membrane shifts in 'z' direction as other direction have fixed boundaries. This phenomena is commonly known as bulging. It is shown in Fig. F.1.

The circular membrane bulging is known since a very long time. Eq. (2.1) gives an analytical fit for a thin square membrane [23].

$$P(d) = C_1 \frac{t\sigma_0}{a^2} d + c_2(v) \frac{tE}{a^4} d^3 \tag{2.1}$$

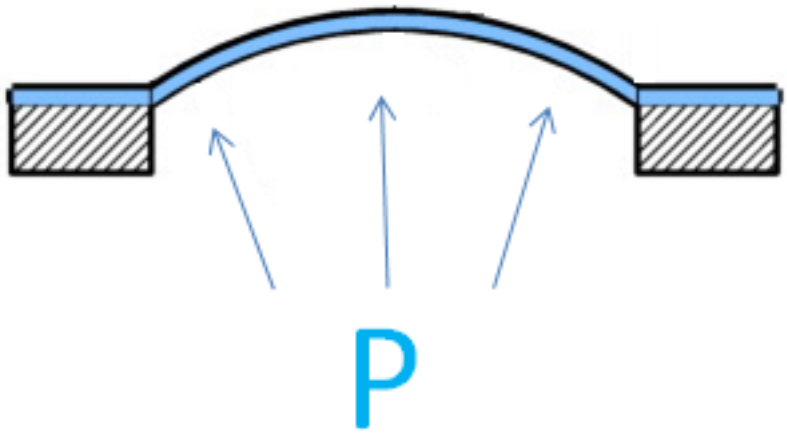

Figure 2.1: Membrane bulging under Applied pressure

where P is the applied pressure, C_1 and C_2 are curve fitting constants as shown in Table 2.1, t is the thickness of the membrane, σ_0 is the stress in the membrane, d is the deflection in the direction perpendicular to the thin film plane and ν is the Poisson's ratio.

Keeping everything constant except for the pressure, it can be seen that, an increase in pressure is directly proportional to deflection.

Table 2.1: Fitting Constant for Equation 2.3

	c1	c2(v)	c2(0.25)
Allen et al (1987)	3.04	1.473 (1-0.272 υ)/(1- υ)	1.37
Tabata et al. (1989)	3.04	1.473 (1-0.272 υ)/(1- υ)	1.37
Pan et al. (1990)	3.41	1.37(1.075-0.292 υ)/(1- υ)	1.83
Vlassak & Nix (1992)	3.393	(0.8+0.062 υ)ˆ3/(1- υ)	1.84
Maier-Schneider et al. (1995)	3.45	1.994(1-0.271 υ) /(1- υ)	1.86

Buckling

Buckling on the other hand is a sudden sideways deflection of a member structure. Buckling has different modes depending on the direction and propagation of stress. It is one of the major causes of failure in a structure. The buckling is generally caused by the compressive stresses and the critical buckling stress for a thin film can be given by Eq. (2.2) [24].

$$\sigma_{Cr} = \frac{5.33D\pi^2}{h.a^2} \tag{2.2}$$

where σ_{Cr} is the critical stress for bulging, D is given by Eq. (2.3), h is the thickness and a is the length of the square membrane.

$$D = \frac{E.h^3}{12(1-\nu^2)} \tag{2.3}$$

It is very important to note that micro-hotplate may go through buckling due to thermal stress. In case of nano-reactors, as both the gases as well as heating from micro-heaters are present both bulging and buckling phenomena can be observed. Though, at very low pressure, the thermal buckling is the dominant effect as bulging is almost negligible. Conceptual simulations are done in this chapter to find the range of stress which can affect the bulging and buckling of the membranes. The study in the next section make use of the plate theory, thus it will be interesting to know little about solid mechanics concept. This section deals with some basic concepts used in thesis for simulations and analysis.

2.2.2. Plane stress

Stress in a material is generally considered to be a 3D concept, as can be seen in Fig. 2.2. Plane stress is defined as the state of the stress in which the normal stress σ_z and the shear stress τ_{xz} and τ_{yz}, directed perpendicular to x-y plane are assumed to be zero. The assumption is valid because the dimensions in z directions is very small as opposed to other two lateral directions. It can be seen from Fig. 2.2.

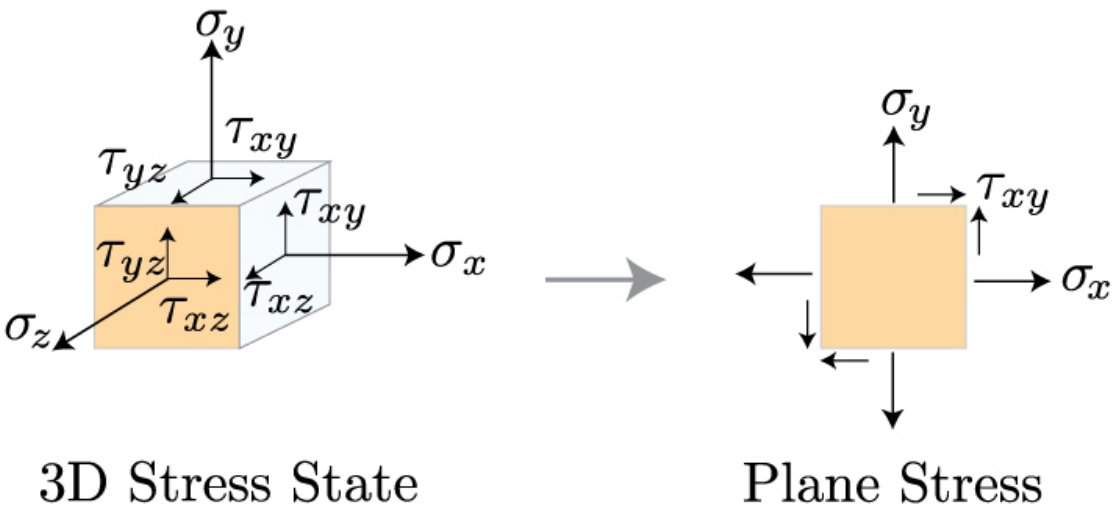

Figure 2.2: Comparison of 3D stress and Plane stress

Similar conditions are applied to plane strain as well. The Plane strain considers only strain in the x and y directions and the stains in the perpendicular z directions are ignored.

2.2.3. Plate Theory

A plate is a structural element for which thickness is small as compared with the surface dimensions. The thickness of the model is generally constant and is measured normal to the surface. The thickness can be made variable but it has to be made sure that it is still smaller than the surface dimensions. The difference between the plate theory and plane stress condition is that in plate theory, stress distribution across the thickness is allowed and there can be bending moments. Also plate can have torsion, so it can twist.

Theory

The plate theory is based on three basic assumptions.

- The mid-plane remains a neutral plane without any stress or strain. The bending in the plate is due to deformation above and below the mid-plane.
- Line elements normal to the mid-plane remains normal to the mid-plane after bending.
- Vertical strains are ignored.

As the plate theory is used as a modelling tool to simulate the SiN_x, used in this thesis, it will be useful to understand the in- and out-of- plane forces and moments acting on a system in detail. It is shown in the Fig. 2.3.

The equations used for calculations of in-plane stress, the bending moment and the out of plane stresses are provided in Appendix E. The simulation models considered in this chapter are based on the plate theory.

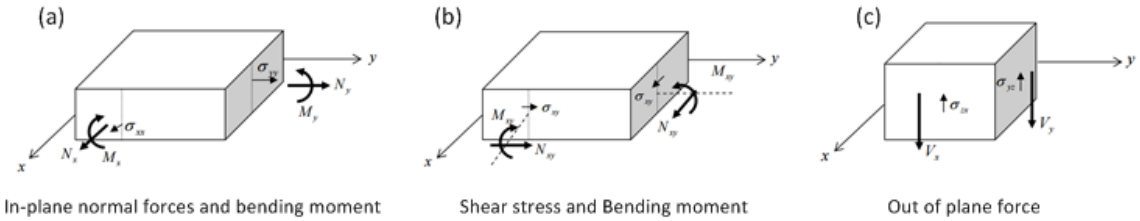

Figure 2.3: The various forces and bending moment in the plate

2.2.4. Forces and Equilibrium conditions

Before going into the equilibrium state of the elements, the type of forces present in the system are discussed. As the membrane is getting heated, thermal stress develops in the membrane. The thermal stress in a material is given by Eq. (2.4)

$$\sigma_T = E\alpha\Delta T \tag{2.4}$$

where E is the Young's modulus, σ_T is the thermal stress, α is the coefficient of thermal expansion and ΔT is the change in temperature. The thermal stress forms one of the in-plane forces developed.

The membranes are fixed at the edges, which is the case in simulations as well as the actual scenario. To understand it in a very simplified approach: other elements which are not at boundary can push the nearby elements to release the thermal stress but the boundary element does not have a choice as the other side of the boundary element is fixed. The fixed end thus produces a reaction to maintain the system in equilibrium. The condition at equilibrium is shown in Fig. 2.4

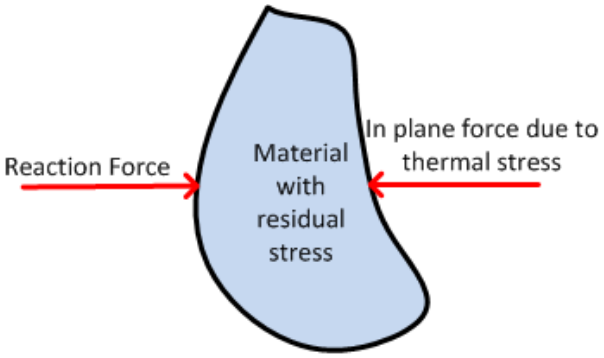

Figure 2.4: The equilibrium condition of a solid element

As the reaction force is opposite in nature it should be compressive. Thus introducing a residual stress, which is tensile in the membrane will help us to tackle the compressive loading provided by the reaction force. The reaction force is expected to increase as thermal stress increases. Thus it might create bending in the 'z' direction. Mathematically, zero bending condition is given in Eq. (2.5)

$$F_{net} = F_{Thermal} - F_{Reaction} \tag{2.5}$$

where F_{net} is the net force on the body, $F_{Thermal}$ is the in-plane force generated by the thermal stress and $F_{Reaction}$ is the in-plane force by the boundary. This is a simplified analysis to show that the introduction of residual tensile stress can help reducing the thermal buckling. In general, the systems are non-linear and one to one relation as discussed does not work, but the simplified model is good enough for understanding and developing an intuition.

2.3. Simulations

This thesis uses COMSOL for simulations. COMSOL in turn uses Finite Element Models (FEM) and numerical methods to analyze the result.

2.3.1. Micro-heater Simulation

A micro-heater is an integral part of nano-reactor as discussed in Section 1.3.1. Micro-heaters are also extremely important for other applications. It helps to maintain the nano-reactors at a particular temperature, which is one of the most important parameter for the reactions. In order to understand the temperature distribution and voltage sensing, simulations that were performed, are presented in this section.

Temperature Distribution across membrane

The micro-heater is enclosed between two thin membranes in case of nano-reactor, which otherwise is not a requirement. It is very important to know that these membranes form the channel for the gases. Thus the upper membrane is separated by spacers and is not in contact with the heater. The model takes some considerations for making a 3D model of the micro-heater to be mimicked as a 2D model. This model is equally useful for micro-heater and the assumptions considered are valid for both.

- The effective thickness of the membrane has been modulated to 400 nm silicon nitride membrane (consists of an upper and a lower portion, each with 200 nm). Although there can be a difference between the bulging at top and bottom membranes due to the temperature difference between the two, the distance between the two membranes is very small. So, convection can be neglected for simplicity. So a single membrane is assumed in place of two. This is not necessary if only micro-hotplate is considered for simulation.
- The effective thermal conductivity(k) was considered by accounting for 400 nm of silicon nitride and 100 nm of platinum heater. The formula used for effective thermal conductivity calculation is given by Eq. (2.6)

$$k_e t_e = k_{SiN_x} t_{SiN_x} + k_{Pt} t_{Pt} \tag{2.6}$$

- The platinum heater acts as a heat source for the device. More the injected current, more is the joule heating and thus higher the achieved temperature.
- The temperature profile can be seen in Fig. 2.5. The variation of temperature range with current can be verified. The current is varied from 1 mA to 10 mA. High temperatures can be reached by going to higher current values. Generally the operating temperatures are close to 1000^{o}C. The temperature profile shown in Fig. 2.5 is for reference with the current input as 10 mA.

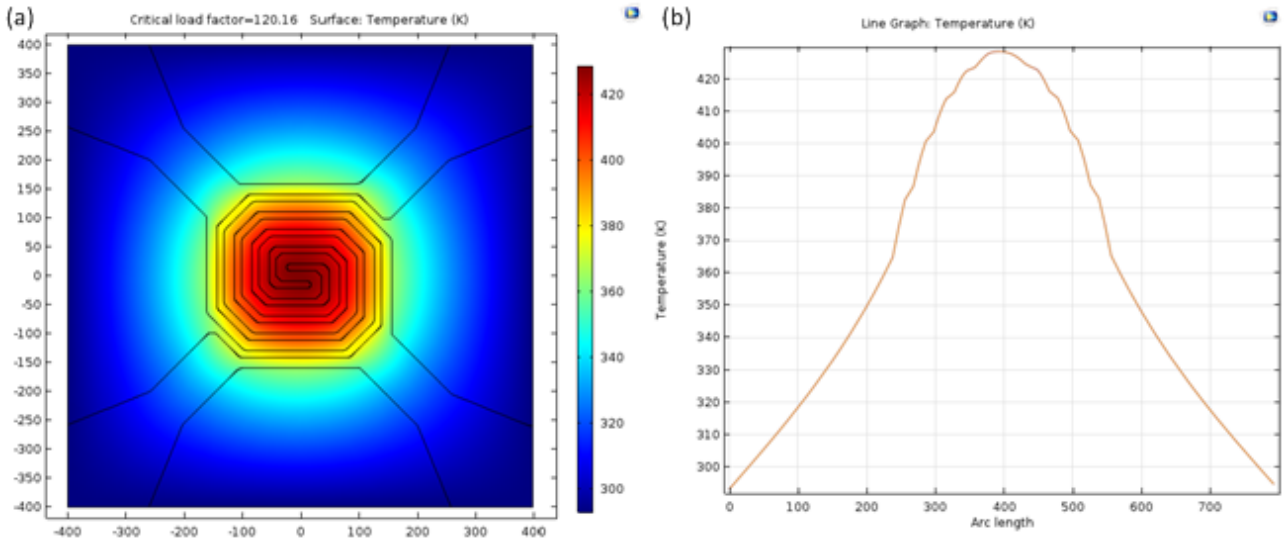

Figure 2.5: (a)Temperature distribution at I=10mA (b) Temperature distribution plot-COMSOL

- The voltage distribution can also be seen in Fig. 2.7. The change in voltage attributes considerably to the heat dissipation and the rise in temperature.

- The temperature dependence of resistance is also taken into consideration. Linearized-resistivity attribute of COMSOL was used to do this.

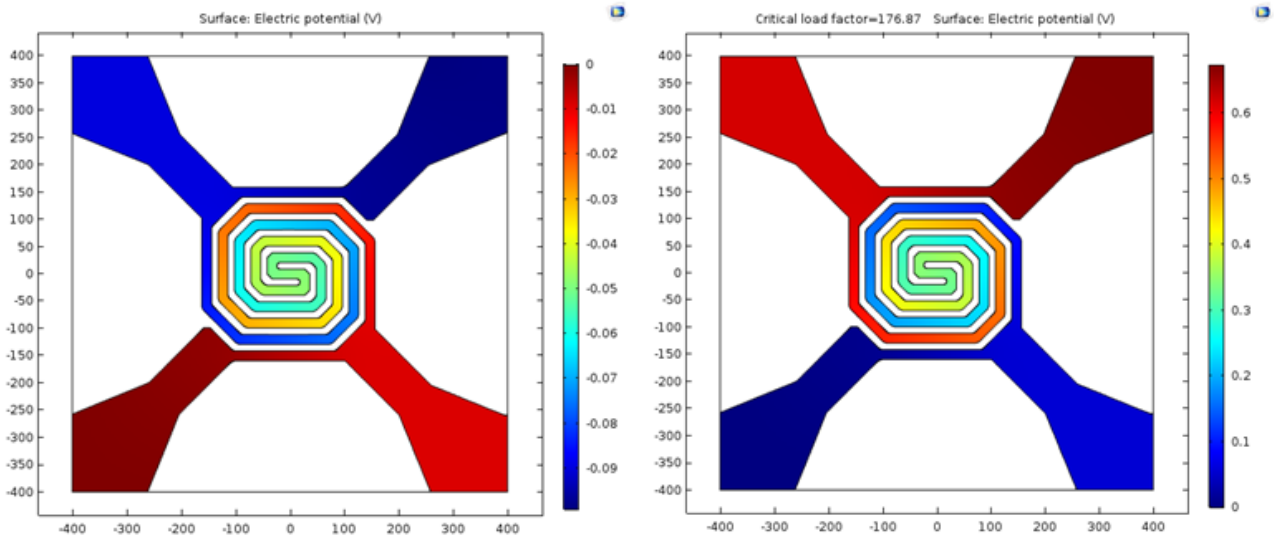

Figure 2.6: (a)Voltage distribution at I=1mA (b)Temperature distribution at I=10mA

From the above simulations the following aspects can be concluded.

- It shows the temperature range in which the device can work at a particular current.
- This non-uniform heating can cause a non-uniform stress distribution across the membrane.
- As the temperature in the central heater area is higher and has better uniformity, the transparent electron windows are mostly concentrated in a small central heater area.

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2.3.2. Buckling due to Temperature

In the previous section the non-uniform distribution of temperature across the membrane present in micro-hotplate and nano-reactors is discussed. This non-uniformity is the main cause of a non-uniform stress distribution, which may lead to buckling of the membrane. The buckling can be tackled with the help of tuning the residual stress in more tensile region. These heaters are suspended on silicon nitride membrane, which are there for insulation and support.

Insulation can be qualitatively discussed in reference with thermal conductivity. Thermal conductivity of a few heater materials and the two membrane materials that are used for production at EKL are shown in Table 2.2

Device discussed in this thesis uses platinum as the heater material and Silicon Nitride as the membrane material. From Table 2.2 it can be seen that platinum has higher CTE than Si_3N_4, which is present above and underneath platinum. It means platinum expands more than Si_3N_4 with each degree rise in temperature. This creates a thermal stress in the membrane and can be the cause of compressive stress in the Silicon Nitride membrane with fixed boundaries, which in turn leads to a shift in 'z' direction of the membrane. This phenomenon may be observed during experimentation. Some simulations supporting the same is presented here.

Simulations

The previous section describes the temperature distribution across the membrane. In this section, a simplified model is considered. Salient features of the model are discussed below.

Table 2.2: Thermal conductivity of some heater and membrane materials

Material	Thermal conductivity [W/m.K]	CTE [1/K]
Platinum	71.6	9
Molybdenum	138	5
Silicon Nitride	29	2.6
Silicon Carbide	120	2.2

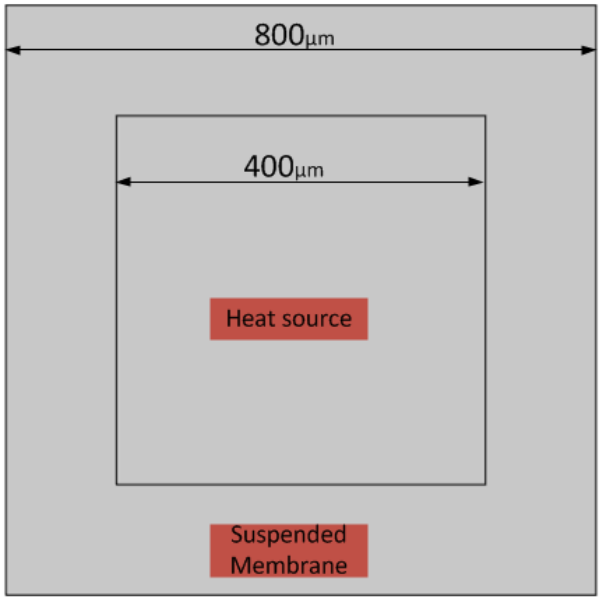

Figure 2.7: A COMSOL Plate model

- A 2D plate model is considered. One area marked is the heat source and the other beneath is the membrane.
- To simplify the model further, the heater area is simply replaced by heat source which uses power to generate the heat.
- For generating a temperature profile, power was swept across 10 mW to 200 mW. The average temperature range of heater is around 1000°C for practical purposes. Thus for all the simulations in this chapter a range of power from 10 mW to 100 mW is only considered as the average temperature of the surface reaches 1000^{o}C.(Fig. 2.9)
- The temperature profile for 10 mW and 100 mW is shown in Fig. 2.8. The max temperature reached is approximately 2500^{o}C. Although this is extremely high temperature, it has been shown here in order to show the range of in-line forces and the temperature at which it changes from tensile to compressive.
- Once the desired temperature profile was created, the in-line forces were calculated. As per the sign convention, the tensile forces are assumed to be positive and compressive forces are taken to be negative.
- The buckling is a phenomena under compressive stress. Thus the transition from net tensile force to net compressive force gives the guideline about which tensile stress has to be chosen to avoid shift in 'z' direction in a given temperature range.
- A comparative study of the temperature and in-line forces has been shown in Fig. 2.10.

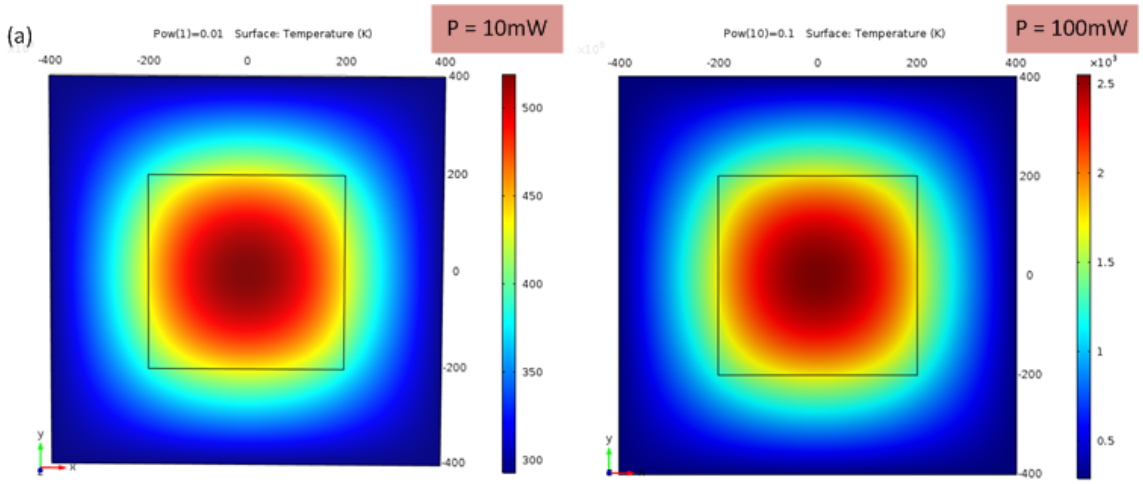

Figure 2.8: Temperature distribution for (a)min and (b)max power considered

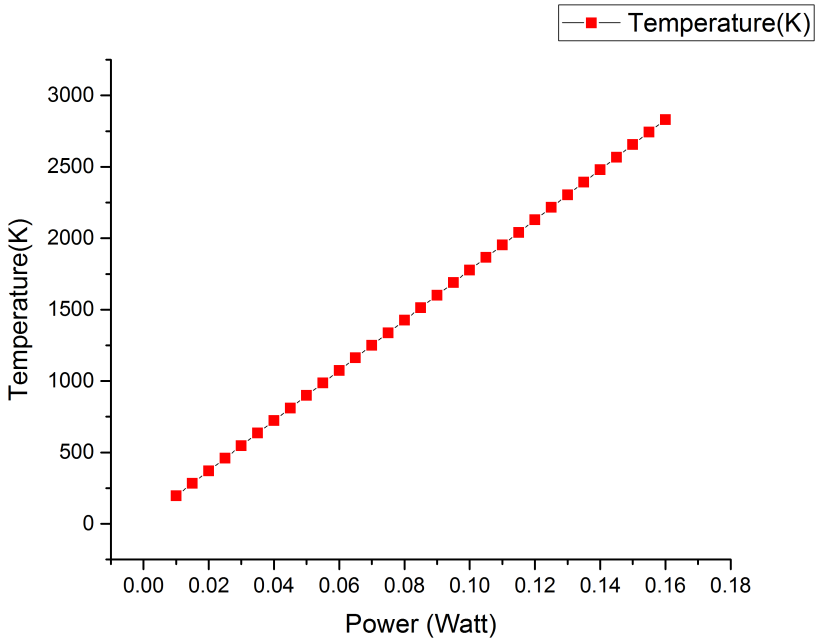

Figure 2.9: The average temperature as a function of power

Conclusions

This section, with a very basic model, concludes that increasing the residual tensile stress in the membrane can be an excellent choice to reduce the shift in 'z' direction. This idea can be further used in this thesis as it can be beneficial in increasing the operating temperature of micro-hotplate as well as nano-reactors. To make the guidelines of which stress level can go up to which temperature, Fig. 2.11 has been plotted. It clearly shows that with the increase in stress the temperature range without any buckling can also be increased.

2.4. Pressure Bulge Simulations

Micro-hotplates can be used when the reactions has to observed just in the presence of thermal stress. For example, phase change of material as a function of absolute temperature. Generally, reactions happen at a particular temperature and pressure. So, it is very important to see the effect of pressure on the membranes.

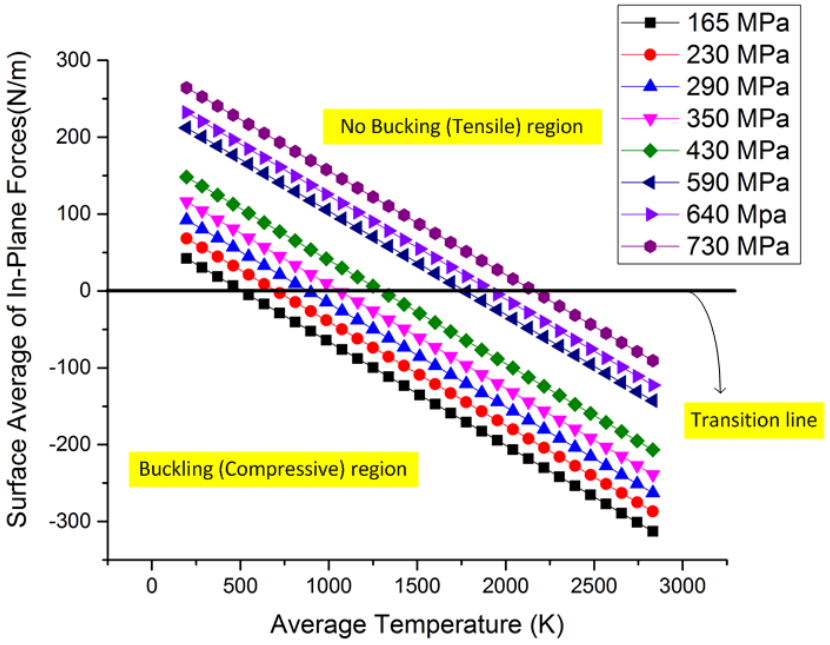

Figure 2.10: Average In-plane force vs Temperature

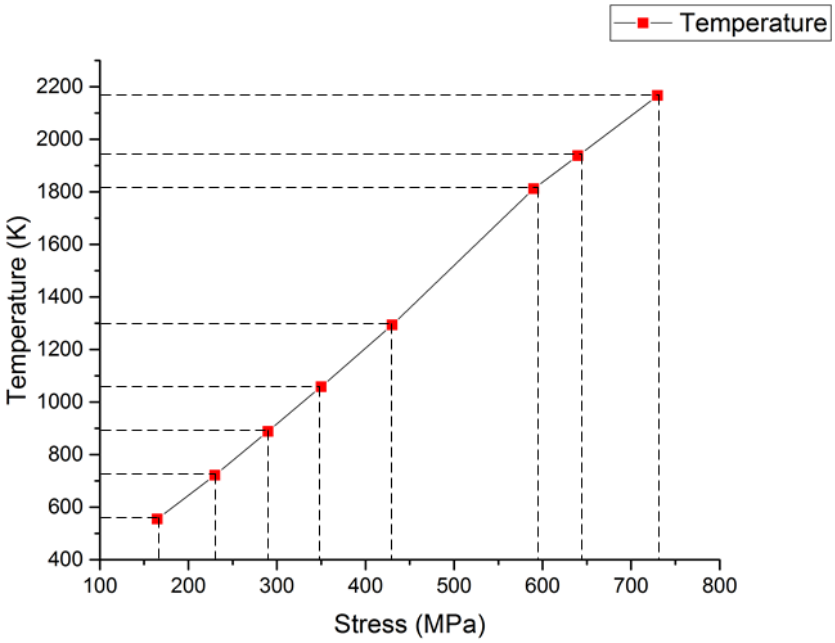

Figure 2.11: Temperature with zero shift in 'z' direction at various stress

It will be interesting to find out if the stress affects the shift in 'z' direction, popularly known as the bulging effect.

Computational Analysis

The simulations considers the following assumptions and features:

- A 2D plate model is considered. The plate model is the 2D representation of shell with limited bending stress and thus it is ideally suited for basic simulations.

- This simulation shows the effect of pressure on thin membranes. A face load was applied and the boundaries were fixed. The bulging profile is shown in Fig. 2.12
- Different pressure has been applied to demonstrate the effect at various pressure and a similar trend has been found. It is also in accordance with the considered analytical model.
- A comparative study with different stress membranes has also been presented as shown in Fig. 2.13

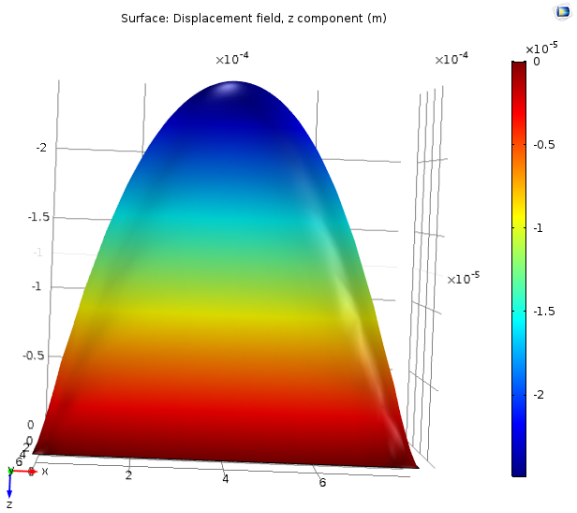

Figure 2.12: One of the bulging profile Simulated in COMSOL

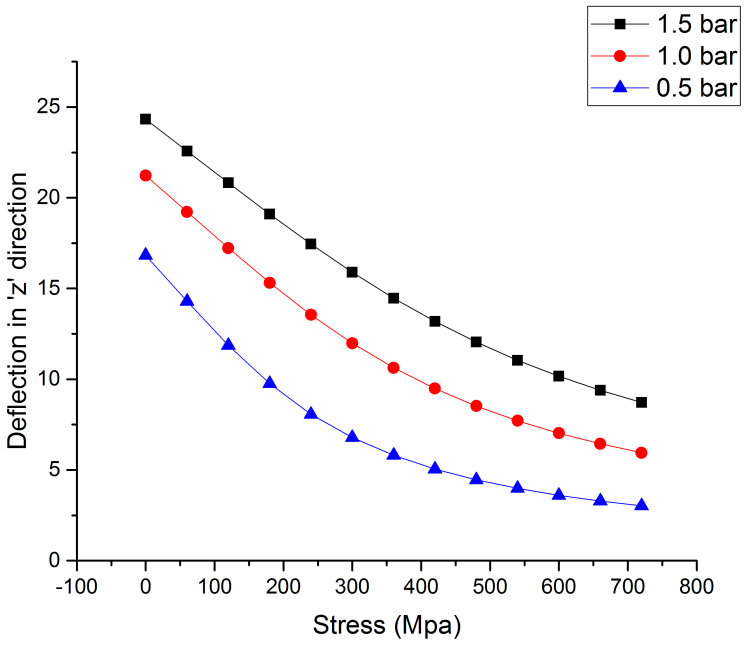

Figure 2.13: Displacement of various stress wafers at different pressure

Conclusions

The first conclusion from this simulation is that there will always be a bulge if there is pressure applied. At the same time, it can be seen that the bulging in the membrane is reduced with the increase in

residual tensile stress. It is in accordance with the intuitive thinking. This simulations also uses almost the same range of tensile stress as used in the previous section. Thus similar stress value can be used for fabrication purposes. After this section, it is known that introduction of residual tensile stress in the membrane is beneficial in both the cases of pressure and temperature. In some cases, a combined effect of these two may not be as linear as it has been thought. So, it is extremely important to simulate the conditions which includes both temperature and pressure. This has been done in next section.

2.5. Analysis with both Temperature and Pressure

Application of both temperature and pressure is the real scenario for the observation of reactions. Thus it is important to simulate under the application of both pressure and temperature. If the pressure is kept constant, the shift in 'z' direction becomes a function of residual stress in the membranes. Membranes can be chosen with a particular residual tensile stress. The choice of residual stress will be according to maximum temperature the device has to operate. An increase in residual tensile stress increases the maximum operating temperature without any shift in 'z' direction.Thus, there will not be any need to change the focus of the tool till a particular temperature.

Simulations

The simulations for this case uses the same features described in Section 2.4 for pressure bulge and Section 2.3.2 for buckling due to temperature. The same plate model is used, but this time both the temperature profile using the power source and the face load as pressure have been applied.

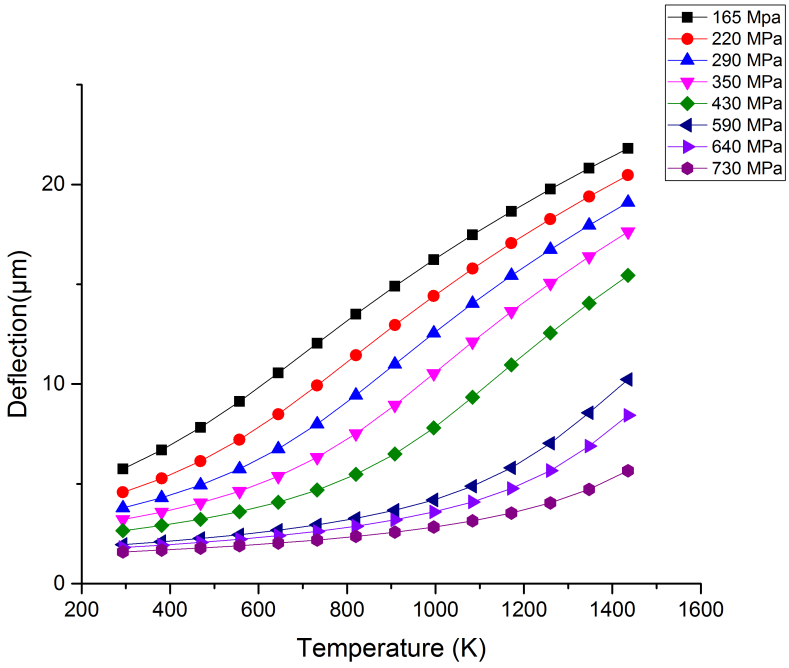

Figure 2.14: The deflection at various temperature (P = 0.1 bar)

Conclusions

It can be observed from Fig. 2.14 and Fig. 2.15 that shift in 'z' direction decreases with increase in residual tensile stress. It was expected to decrease as it was already found that it decreases with temperature and pressure individually. Thus, a combined effect should also be a decrease in 'z' direction shift.

An interesting conclusion that comes out of this analysis is that the shift in 'z' direction at lower pressure (see Fig. 2.14) is more due to thermal bulging and difference in shift is relatively high. The bulging due to pressure dominates at high pressure (Fig. 2.15) and is generally the case in nano-reactors. Although the increase in residual tensile stress, decreases bulging but the reduction is not very high.

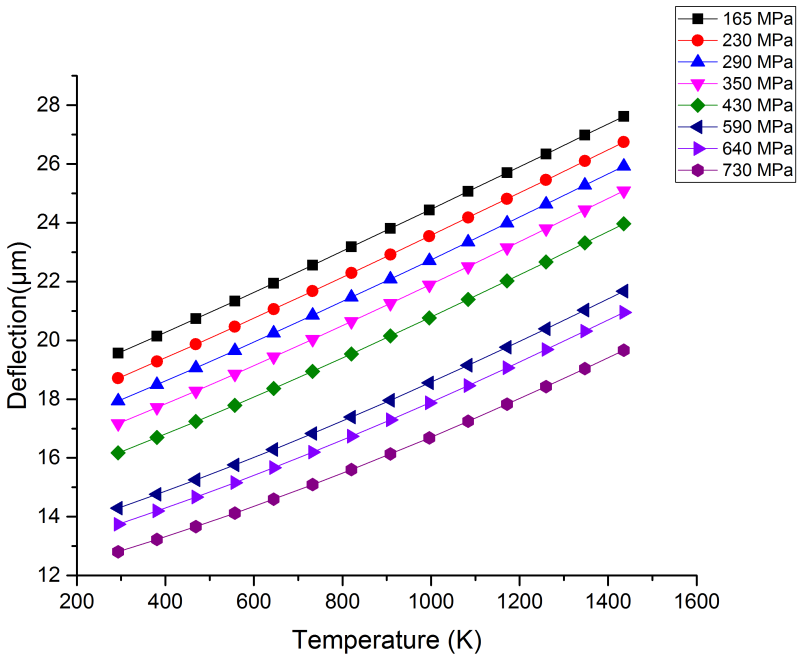

Figure 2.15: The deflection at various temperature (P = 1 bar)

2.6. Conclusion

This chapter introduced the theory behind buckling and bulging. The concept of plate theory needed for FEM simulations are explained. COMSOL simulation were done to study the effects of bulging and buckling due to Pressure applied and temperature distribution across membrane as a function of increase in residual tensile stress. Firstly, effect of temperature and pressure were individually studied and later on a combined study of both (Temperature and Pressure) was done. The temperature simulations will be important from micro-hotplate point of view and a combined effect gives an idea about the case in nano-reactor. It was concluded that an increase in residual tensile stress is highly effective to reduce thermal buckling. It is also effective in reducing the pressure bulging but not in the same order of magnitude as compared to thermal buckling. Thus, at this point in thesis it became highly important to study the process of making membranes with various residual tensile stress.

3

LPCVD- SIN_x Characterisation

3.1. Introduction

Introduction of residual tensile stress can reduce the shift in 'z' direction. Chapter 2 provided us with a lot of simulations and gave us a fairly solid background on the introduction of residual stress for increasing the operating temperature of devices which was previously limited by bulging and buckling due to applied pressure and temperature. It should be noted that compressive stress can lead to buckling. In order to avoid compressive stress, more residual tensile stress has to be introduced. Thus the further chapters in this thesis deals with only residual stress of tensile nature.

This chapter deals with the theory behind residual stress and how residual stress can be introduced during processing. The same is discussed in Section 3.2. The method of introducing the residual stress, is expected to bring changes in material properties of SiN_x. Thus, characterization of mechanical properties like Young's Modulus is done in Section 3.3. Young's modulus can be mathematically defined as the ratio of stress and strain. Thus, stress and strain characterization has been done in Section 3.3.1 and Section 3.3.2 respectively. It was also important to know the optical properties and the material composition. It was done using ellipsometry in Section 3.4.1 and FTIR in Section 3.4.2 respectively. Finally, in Section 3.5.1, the Surface roughness and grain properties has been calculated. It is very important to note that The thesis form hereon deals with only residual tensile stress.

3.2. Stress in thin films

The mechanical properties of the deposited thin film membranes depend on various factors like temperature, pressure, humidity etc. These mechanical properties play a huge role in proper working of the device and its reliability. Residual stress in the membrane is one of the major outcomes of changes in fabrication parameters.

3.2.1. Tensile vs Compressive Stress

The stress developed can be tensile or compressive.The bending of the wafer in downward or upward direction depends on the relative stress induced as shown in Fig. 3.1. In this thesis, residual stress is pushed more into tensile region. The goal is to avoid any net compressive forces in order to avoid any kind of membrane bulging. The theory and methods to fabricate membranes from low to high residual stress has been discussed in upcoming sections

3.2.2. Residual Stress

Residual stress can be defined as stress field that exist in absence of any external load and are the result of mechanical (fabrication) process which may cause deformation.The residual stress in a thin-film can be mainly due to the following reasons:

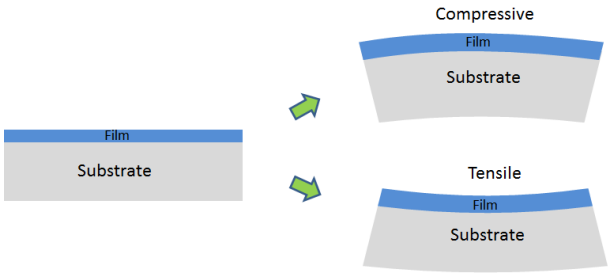

Figure 3.1: A pictorial representation of tensile and compressive stress

Table 3.1: Material and their lattice constants

Element/Compound	Lattice constant
Si	5.431
αSi_3N_4	7.766
βSi_3N_4	7.586

- Lattice Mismatch
- Mismatch in co-efficient of thermal expansion(CTE)
- Intrinsic stress

Lattice Mismatch

When a thin film is deposited on a substrate, at the interface of substrate and the thin film there is a lattice mismatch. This mismatch is one of the cause of the induced stress. In this case thin films are deposited using LPCVD. LPCVD deposits either αSi_3N_4 or βSi_3N_4. α and β are the crystallographic structures of the Si_3N_4. The films made in this thesis can be considered as αSi_3N_4 as it can be deposited at low pressure. It can be seen in Table 3.1 that there is a difference in lattice sizes of silicon and silicon nitride. This difference in sizes contribute to the misfit factor apart from stressing out the interface layer. The interfacial stress later builds on the stress in other deposited layers.

Mismatch in Coefficient of Thermal Expansion

Coefficient of thermal expansion is a material property. This number gives the quantity by which a material will expand with one unit change in temperature. The thin films are deposited at a high temperature (846°C, for LPCVD used here) and then slowly cooled down to lower temperatures and finally at room temperature. During this process, the thermal stress is induced in the membrane. The coefficient of thermal expansion of Si and standard silicon nitride are given in Table 3.2. It can be seen that silicon will expand faster than silicon nitride and thus it will create a push-pull effect, inducing stress. Thermal stress can be calculated as shown in the Eq. (2.4).

Table 3.2: Comparision of CTE for Bulk Si and Membrane Si_3N_4

Element/Compound	CTE $(10^-6°C)$
Si	3.3
Si_3N_4	2.6

Intrinsic Stress

The intrinsic stress is developed in the membrane during deposition or growth. The main cause of these kind of stresses is the non-equilibrium conditions in which the films are deposited. The causes of intrinsic effects can't be defined properly as it varies drastically from sample to sample. It causes might

include grain growth, defect annihilation, phase transition and others. In a broader sense, defects in the crystal can lead to intrinsic stress.

The thermal mismatch contributes to the residual stress here.This thesis tries to optimize this residual stress for LPCVD SiN_x for zero bulging.

3.2.3. Pre-stress

The basic structural theory suggests one of the reasons for the bulging may be that the temperature goes high and converts positive tensile stress of the membrane into the negative compressive stress as shown in Section 2.3.2. Thus, in this thesis it has been tried to optimize the tensile stress, maintaining the mechanical reliability of the membrane, in order to reduce bulging at higher temperatures. To do this, the initial stress or the pre-stress in the membrane needs to be tuned in such a way that the net stress in the membrane is either tensile or in very low compressive stress range to avoid buckling. To tune this process, we need to understand how these thin films are made and what are the fabrication parameters involved.

LPCVD

There are several ways to deposit thin films. One of the commonly used methods is Low Pressure Chemical Vapour Deposition (LPCVD). This method is used in this thesis to deposit membranes of silicon nitride. The low pressure chemical vapour deposition mechanism is displayed in the Fig. 3.2.

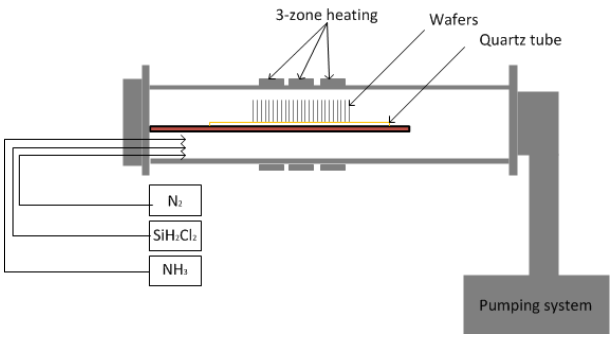

Figure 3.2: Schematics of LPCVD

The whole LPCVD is controlled by a digital controller. The machine has a paddle on which a Quartz holder is kept, where wafers can be loaded for deposition of films. The paddle comes out when a recipe is activated using digital controller and wafers are loaded facing the side from which the gas flows. It takes help of the pumping system to maintain the gas pressure of the reaction chamber. The use of gases does vary from the type of film deposition. As this thesis uses mostly silicon nitride deposition, the gases involved are ammonia(NH_3) and di-chlorosilane (SiH_2Cl_2). The reaction happens at the surface of silicon wafers, which means the reactant gases react when they come in the contact with the silicon surface. The reactor has "three-zone" heating to maintain the uniformity of deposition across the wafer. The three heaters are maintained at different temperatures so that they can compensate for the minor fluctuation in the gas flow. The surface reaction involved is given below:

$$3\,\mathrm{SiH_2Cl_2} + 4\mathrm{NH_3} \longrightarrow \mathrm{Si_3N_4} + 6\mathrm{HCl} + 6\mathrm{H_2} \tag{3.1}$$

The above equation is the reaction for a stoichiometric silicon nitride under a constant temperature and pressure. The one produced in thesis in not stoichiometric. So, it is refered as LPCVD-SiN_x

Optimization of stress using variable parameters

The deposition of a thin film depends on three basic parameters in case of LPCVD :

- Temperature
- Pressure

- Gas Ratio (GR)

In this thesis, the temperature was kept constant at 846°C during all the depositions. The pressure was also kept constant at 150 mTorr. The gas ratio was varied in order to tune the pre-stress in the nitride layer deposited. The characterization of this nitride layer has been discussed in detail. The concept of stress in the wafers were obtained from varying the gas ratio [25] and was used for preliminary analysis. The sum of the gases were converted to 400 sccm as per the limitations of the furnace.

3.3. Young's Modulus

The Young's modulus is the measure of a material's ability to resist deformation under load. It is defined as the ratio of stress acting on the material to the resulting strain induced in the material. The mathematical representation is shown in Eq. (3.2)

$$E = \frac{\sigma}{\epsilon} \tag{3.2}$$

Where σ is the stress and ϵ is the strain. As the calculation of this ratio depends on the knowledge of stress and strain induced in the membrane by the variance of process parameters. The next subsections of this section introduces the method of stress and strain characterization.

3.3.1. Stress Characterization

Stress is characterized using wafer curvature method. A beam of laser measures the radius of the curvature before and after deposition. It uses bare wafer (without any film) as a reference for radius of curvature measurement for the layers deposited on top of the substrate. As the bare silicon wafers are almost flat, the radius of curvature is very high.

The equation involved in the calculation of stress is given as:

$$\sigma = \frac{E_s}{6(1-v_s)} \frac{(h_s)^2}{h_f} \left(\frac{1}{R} - \frac{1}{R_0}\right) \tag{3.3}$$

where,
σ = Stress in the thin film
E_s = Young's modulus of the substrate
v_s = poison's ratio of the substrate
h_s = thickness of the substrate
h_f = thickness of the film
R and R_0 = radius of curvature of the surface after and before deposition

It should be noted that during LPCVD deposition, films are deposited on both side of the wafers. If stress meter is directly used in this case, the stress can't be found as the front side and back side will bend equally nullifying any change in the radius of curvature of the silicon wafer. Thus, deposition on one side of the wafer (generally the back side is the choice) is etched completely before measuring the stress.

After introducing the fundamentals of stress characterization technique, the next step was to tune the process for introducing stress in the SiN_x layer. Four test wafers were used to extract the data points and fit the points to find an equation for between gas ratio (GR) and stress. The mathematical equation will be further used to calculate the gas ratio for a particular value of residual stress desired. The data points extracted are given in Table 3.3.

After the deposition of nitride with the given gas ratios, a plot of stress with respect to gas ratio was generated. The graph is shown in Fig. 3.3. This was used as a reference for further calculation of gas ratio for fabrication of wafers with various tensile residual stress. Also the deposition rate is very important to calculate the time for required thickness. These four deposition was done for 28 mins and then the thickness was measured and deposition rate was calculated. It can be found in Table 3.4. This has also been used as a reference for the entire thesis to calculate the time of deposition.

Table 3.3: Gas ratio and corresponding measured stress level for initial stress

Sample Number	DCS	NH_3	Gas Ratio(GR)	Measured Stress (MPa)
S1	340	60	0.1764	36
S2	340	60	0.1764	62
S3	310	90	0.2903	246
S4	310	90	0.2903	247

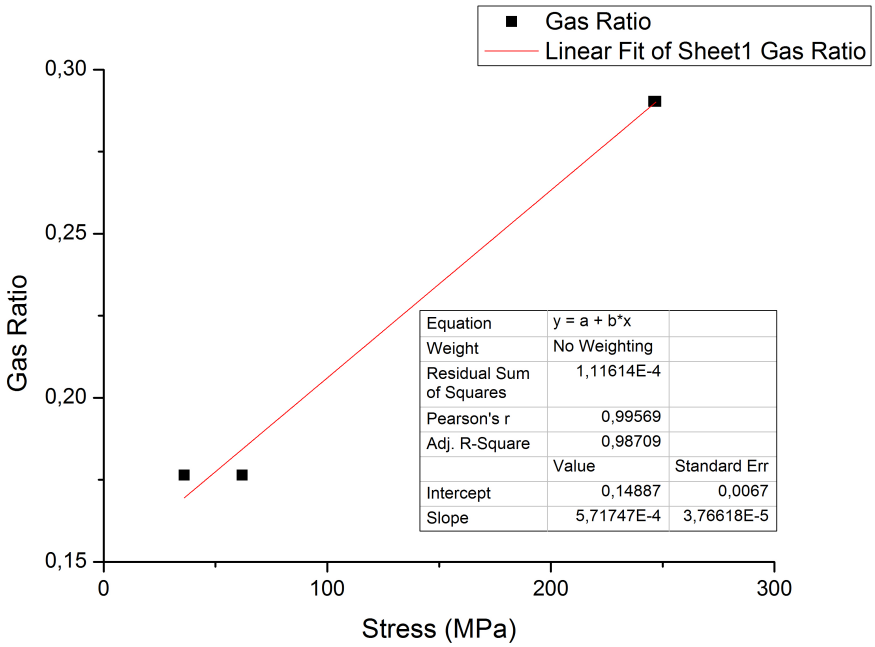

Figure 3.3: Initial Stress Characterization

Table 3.4: The thickness and deposition rate of test wafers

Sample Number	Stress	Thickness	Deposition rate
S1	36	216	7.5176
S2	62	214	7.6008
S3	246	243	8.1896
S4	247	244	8.1928

From Fig. 3.3, we can find the relation between gas ratio and stress. The approximate equation found is given in Eq. (3.4).

$$GR = 0.0006\sigma + 0.149 \tag{3.4}$$

The gas ratios were calculated using Eq. (3.4) and converted to a total of 400 sccm due to furnace limitations. The same is given in Table 3.5.

It can be observed that sample S1 and S2 were deposited with the same gas ratio but stress measurement predict different values. This is because of the fact that these wafers were not deposited simultaneously in the same batch. Considering the variance in deposition conditions and measure-

Table 3.5: The calculated stress with Gas composition and Deposition time

Stress(MPa)	DCS(sccm)	NH_3(sccm)	Deposition time(mins)
230	88	312	49'9"
290	97	303	48"1'
350	105	295	46"56'
500	120	280	44'30"
700	140	260	41'36"
900	160	240	39'18"
1200	182	218	36"06'
1500	220	180	33"26'
1900	260	140	30"36'

ments, these data points are still reliable. Deposition rate is also extremely important to know the time of deposition, as changes in deposition time can lead to various thickness. The deposition time with the initial stress is shown in Table 3.4. The same is plotted and a linear fit is found. The relation is given in Eq. (3.5)

$$DR = 0.0032\sigma + 7.4024 \tag{3.5}$$

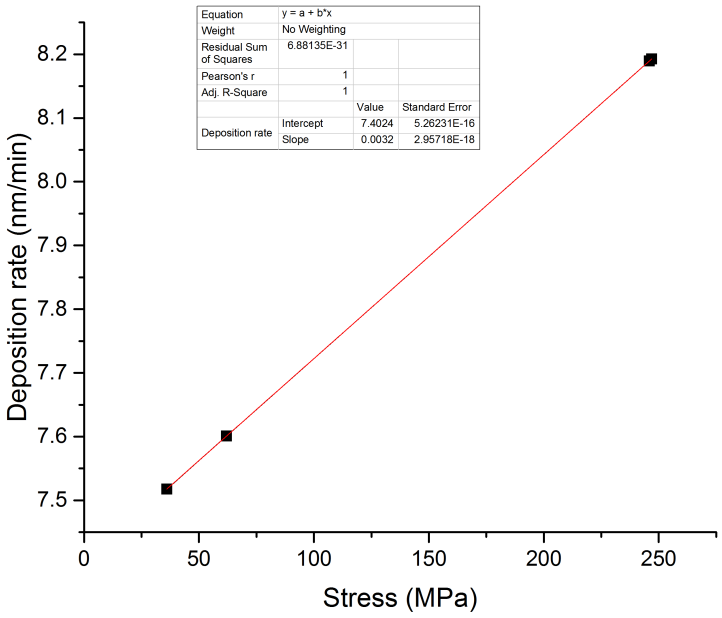

Figure 3.4: Deposition rate vs Stress

The relation found from graph is used to calculate the deposition rate and is shown in Table 3.5. The deposition rates were calculated for 400nm thickness of LPCVD-SiN_x.

Deposition of SiN_x with various stress

LPCVD deposition was done using some of the gas ratios, taken from the theory developed in previous section (See Table 3.5), and was characterized using stress meter for stress. The values obtained are

listed in Table 3.6.

Table 3.6: Stress characterization

Stress(MPa)	NH_3(sccm)	DCS(sccm)	Stress measured(MPa)
230	88	312	211-254
290	97	303	263-286
350	105	295	355-371
500	120	280	422-436
900	160	240	558-594
1500	220	180	626-648
1900	260	140	709-733

Observations and Conclusions

From Fig. 3.5, it can be seen that the difference between the expected stress and the stress characterized increases with increase in stress (as shown in Fig. 3.5) or alternately with the increase in the flow of ammonia in the reaction. It is because the reaction reaches a saturation point and the relation is no more linear [25]. At the same time it should be noted that this saturation is achieved by only varying the gas ratio. Different levels of stress can be obtained by varying the temperature and pressure.

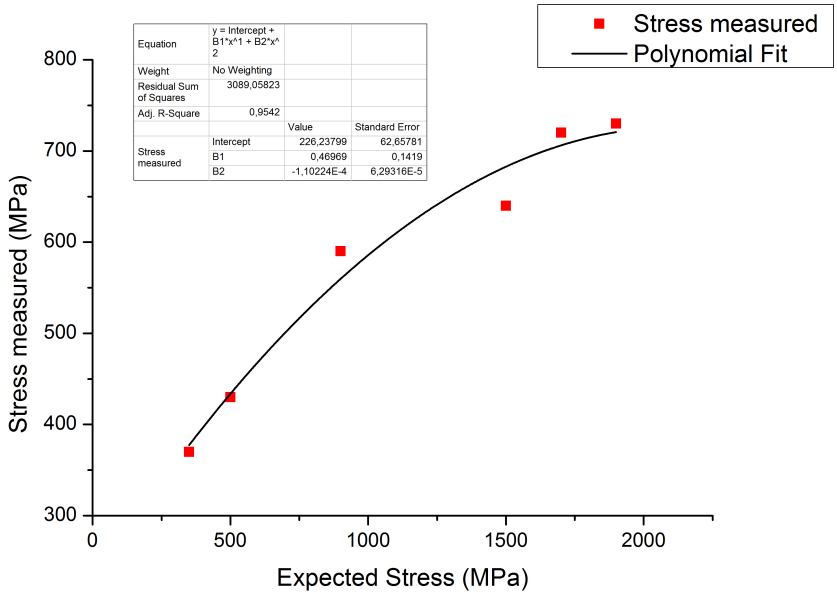

Figure 3.5: Expected stress vs Stress measured

Second interesting observation is that deposition rate increases with increase in NH_3/DCS ratio. In fact for the last residual tensile stress deposition, it decreases a bit. It confirms that the maximum point is achieved and the rate doesn't increase anymore. It also supports the previous argument of saturation.

3.3.2. Residual strain characterization

Strain in a material is defined as change in length divided by the original length. As layers are prestress, the strain has been developed in the layer. Thus, it needs to be characterized. Secondly, it will

be useful in characterization of Young's modulus.

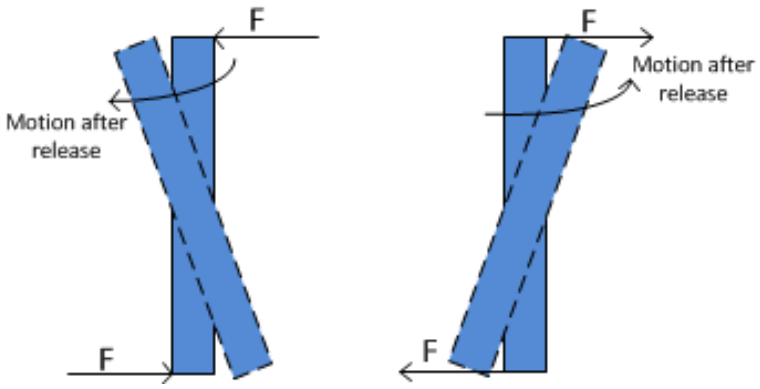

Figure 3.6: Conceptual diagram predicting direction of motion

The structures use rotation of pointers to characterize the stress. The direction of motion of pointers depends upon the type of stress induced in the layer. It is conceptually shown in Fig. 3.6. It can be seen that if stress is compressive the couple developed will rotate the pointers in anticlockwise direction and clockwise in case of tensile stress.

Rotating Pointer

The concept of rotating pointer [26] is widely used to characterize strain in MEMS devices. If the stress is characterized in parallel, it can also give us the Young's modulus. A rough schematic of the structure before and after release is given in Fig. 3.7. The value that is indicated in the pointer after deflection can help us to calculate the strain in the membrane with help of Eq. (3.6).

$$\epsilon_R = \frac{Oy}{(L_A + L_B)(L_C + O/2)} \cdot \frac{1}{C_F} \tag{3.6}$$

where ϵ_R is the strain in the layer, y is the deflection of the pointer after release, O is the perpendicular distance between the two side arms, L_A,L_B and L_C are the length of the arms and C_F is the correction factor.

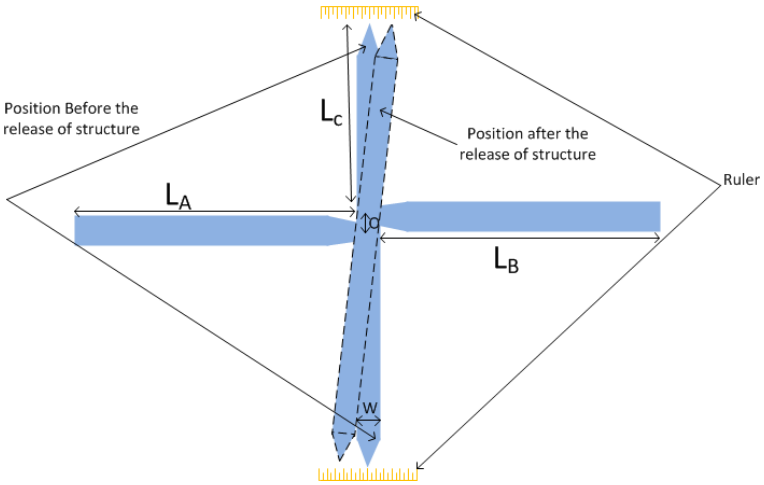

Figure 3.7: Working of rotating pointers

COMSOL simulations

Simulations were performed in COMSOL to determine the range of deflection of the pointer after the release of residual stress and also (b) to verify the direction of deflection of the pointer according to

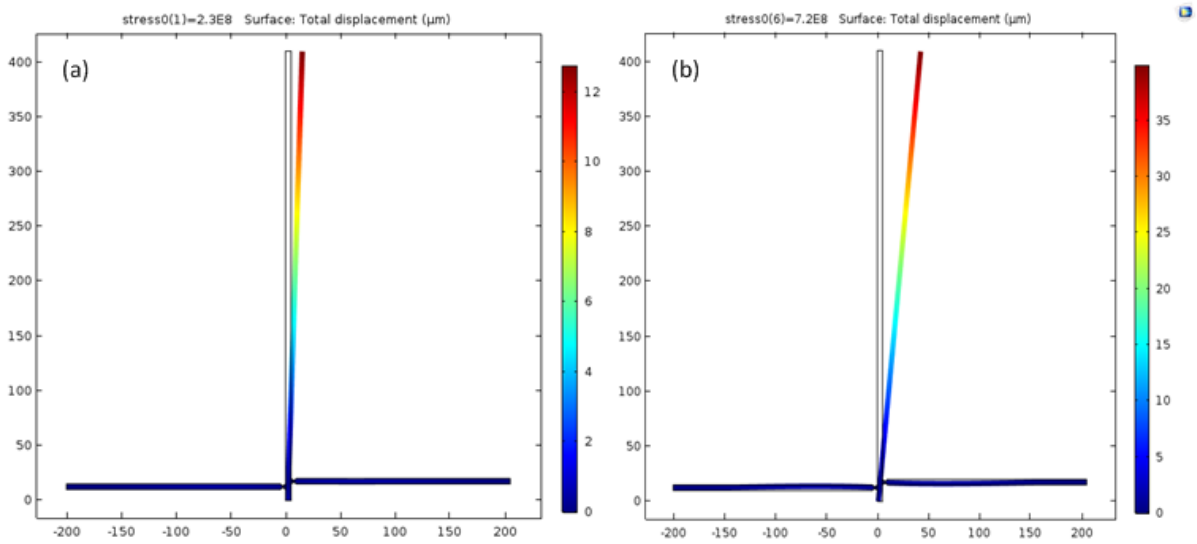

Figure 3.8: Deflection of pointers with stress (a) 230MPa and (b) 720MPa

Table 3.7: Parameters used for COMSOL modelling

Geometry	L_A (μm)	L_A (μm)	L_A (μm)	O (μm)
1	200	200	295	5
2	90	90	362.5	15
3	55	55	362.5	15

the concept discussed earlier (Fig. 3.6). The parameters for simulation of the pointers is shown in Fig. 3.8. Based on the simulation, we conclude that the design works and deflection of the pointer increases with increasing stress. Also, the linearity of the deflection with increase in stress is shown by Fig. 3.9 and also three kind of geometry has been considered. The different geometry and parameters is described in Table 3.7.

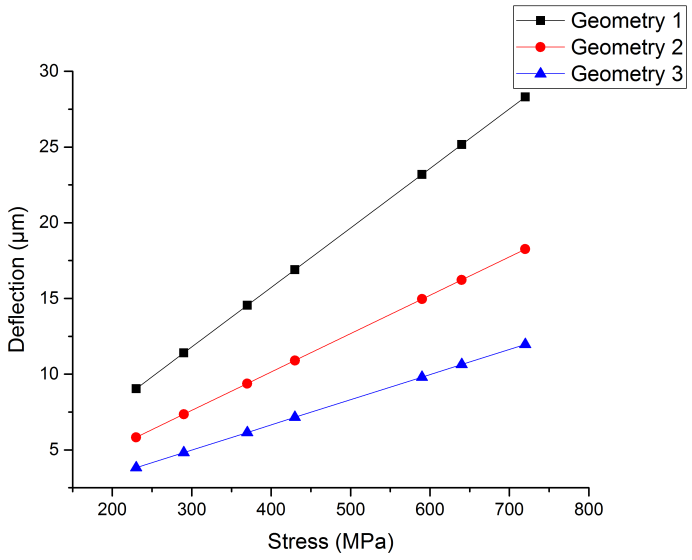

Figure 3.9: Deflection of pointers with stress

Mask design

Mask design was carried out for rotating pointers. As the wafers experience different stress levels during processing, the length and width of the membrane which would survive the process is not known. Specially, after release multiple structures could collapse due to the torque or bending moment generated by the slight non-uniformity of the structures as well as the stress distribution. So, structures having different lengths - L_A, L_B and L_C (see Fig. 3.7) - were designed. Also the distance (O) between the two supporting beams was varied.

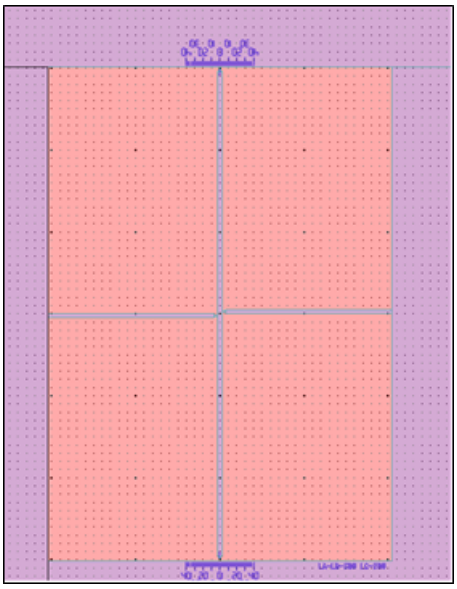

Figure 3.10: Mask design of rotating structures

The final mask design can be seen in the Fig. 3.10. The mask has a 3-layered design. The first layer is the structure (rotating pointers), the second layer is aluminum and the third layer is a meshed structure. Meshed structure hasn't been used in this thesis.

Fabrication

This is the first fabrication process of the thesis. Thus it is very important to discuss some basic rules. In this thesis, the concept of surface micro-machining [27] has been used in most cases. The process flow is shown in Fig. 3.11. A detailed flowchart is available in the Appendix A.

The first step starts with the alignment markers. Then nitride deposition was done. As the gases are present everywhere in the chamber, the deposition takes place on both sides of the wafer. It can be seen in Fig. 3.11(a). The back side nitride was removed in order to check stress on the wafer (Fig. 3.11(b)). The next step was deposition of Aluminum. The Aluminum was deposited by sputtering (Fig. 3.11(c)). The requirements of Aluminum are as follows:

- As LPCVD-SiN_x is transparent. The reflection from optical microscopy will not be problem. But observing the reflections from SEM could be an issue. Thus the rulers and the tip of pointers were covered with a little bit of Aluminum in order to observe the reflections properly.
- The aluminum sputtered should be as thin as possible. Otherwise it may affect the net residual stress, which may affect the deflection of pointers. In this case the aluminum deposited was of 50nm thickness.

Patterning of aluminum was done when it was ready to be etched (Fig. 3.11(d)(e)). This was a critical step. It wasn't recommended to use dry etching method as it might make the surface rough. Thus wet etching is the remaining option. The standard bath of aluminum uses polyethersulfone (PES) solution. The PES solution was initially tried and it was found that the resist was floating. This was due to the

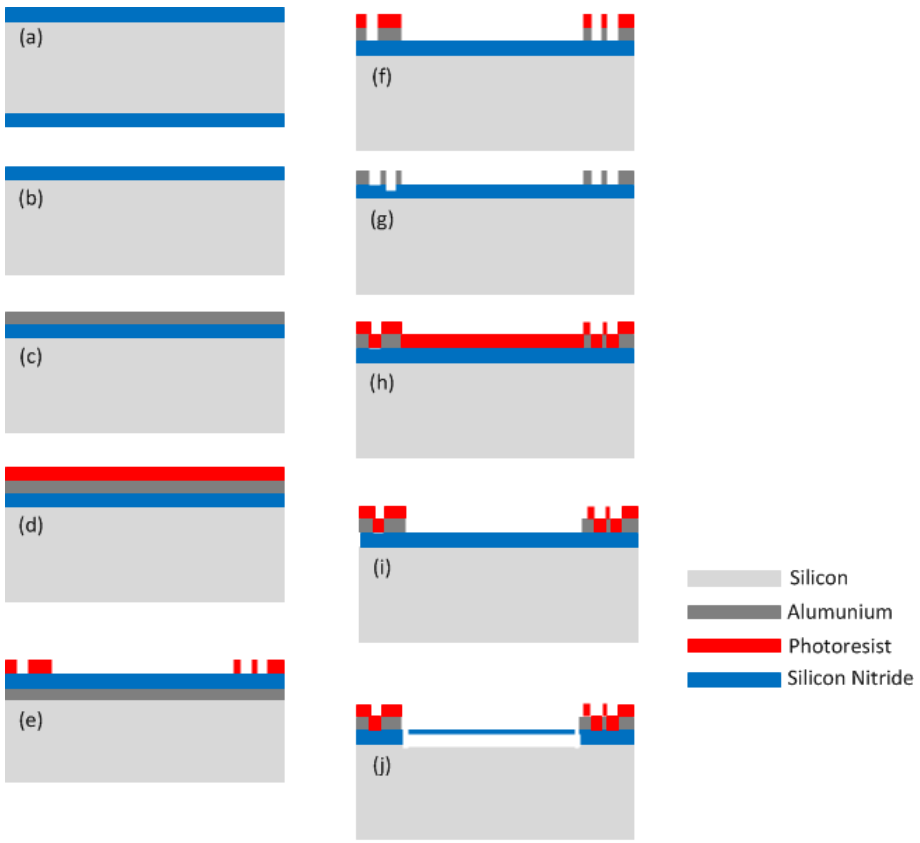

Figure 3.11: Process flowchart for rotating pointers and hinges (a)silicon nitride deposition (b) Backside removal of silicon nitride (c) Aluminum deposition (d) Photo resist on front side (e) Patterning of Aluminum (f)Aluminum etching (g)Photo resist removal (h)Photo resist on front side for hinges (i)Photo resist for hinges (j)Dry etching and release of hinge structure

poor adhesion of the resist to aluminum. So, extra bake was done in oven at 130°C for 30 mins. This increased the adhesiveness of photo resist to the aluminum surface but the end result was found to be same. The reason may be a very fast etching rate of PES (approximately 160nm/min). PES also has very high viscosity, thus it comes out of the surface very slowly, which means it continues etching till it is completely rinsed by water. It makes sense as from experimentation it has been found out that some structures are more damaged than others. So, PES was rejected as a choice. HF 0.55% was tried after hard bake in oven. HF 0.55% etch rate is 90nm/min and has relatively very less viscosity. This led to a more controllable etching and the etching was successfully done(Fig. 3.11(f)(g)).

Lithography steps for pointers were performed and silicon nitride was etched using dry etching method. This method of etching nitride is highly reliable and a thicker photo resist was used to make sure it doesn't etch in the pointer area(Fig. 3.11(h)(i)). After etching of oxide area the last and extremely critical step was the release of structures.

The structures has to be released from the Si- SiN_X interface. Wet release was not considered due to stiction problem [28]. Thus, dry etching was used to release the structure(Fig. 3.11(j)).

The time used for release of rotating pointer was 1 min 10 s. The release of the structures were inspected using microscope as well as Scanning Electron Microscope (SEM).

Fabrication results

The fabrication flow has been discussed. The rotating pointers fabricated is shown to be in shifted position towards right after the release of nitride beneath the surface of pointers. The movement is

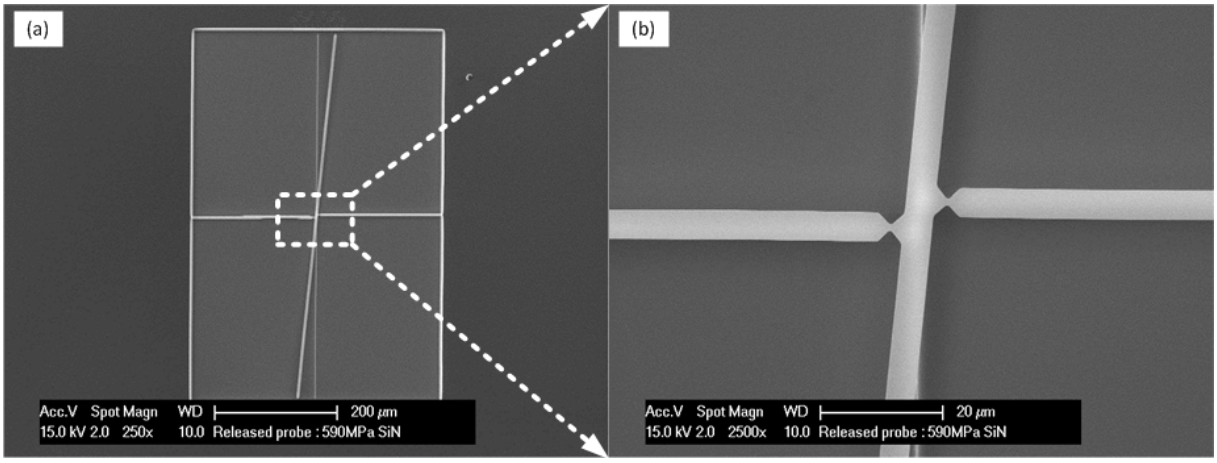

Figure 3.12: Process flowchart for rotating pointers

well followed in the direction predicted by the theory and simulations. It can be see in Fig. 3.12. The most critical point from where the device can be broken is the midpoint due to the probability of twisting moment formed at the center. Thus, Fig. 3.12(b) enlarges the midpoint and it shows it to be in good condition. Thus, this pointers can be used to calculate the deflection. Some of the pointers especially one for the large stress was found to be broken due to excessive tensile force generated in order to rotate. One such pointer is shown in Fig. 3.14. Devices with larger arms were also observed to be broken more frequently with respect respect to the devices with lower arm span. Thus at higher stress only smaller arms survived while all the larger arms were found out to be broken. This is because large arms are susceptible to large deflection and thus huge stress at the center. That's also the reason for more structures falling down for higher stress.

The deflection was calculated by taking SEM images and drawing a straight line through the pointer to check its reading on ruler (Refer Fig. 3.13). This deflection can be fitted in the Eq. (3.6) to calculate the strain. The stress in the wafer was calculated before fabrication. The values of strain and stress can be used to extract young's modulus using Eq. (3.2). The extracted young's modulus can be found in Table 3.8.

Table 3.8: Extracted Young's modulus using rotating pointers

Stress (Mpa)	Geometry	Deflection (μ m)	Extracted Young's Modulus (GPa)
430	1	23	244
590	1	30	257.5
640	3	10	243
730	2	15	160

3.4. Optical Characterization

3.4.1. Optical Constant

The layers have different stress, so does the atoms at the smallest level. As the crystal lattice goes under stress it starts interacting with different wavelength of light. Ellipsometry is one such method which utilizes this to find the optical constant of the material.

The basic structure of the ellipsometery is shown in Fig. 3.15. The electromagnetic waves from the light source gets polarized by the polariser. The compensator generally changes the phase of the light because of the anisotropy present in its structure. The light waves gets changed to elliptically polarized

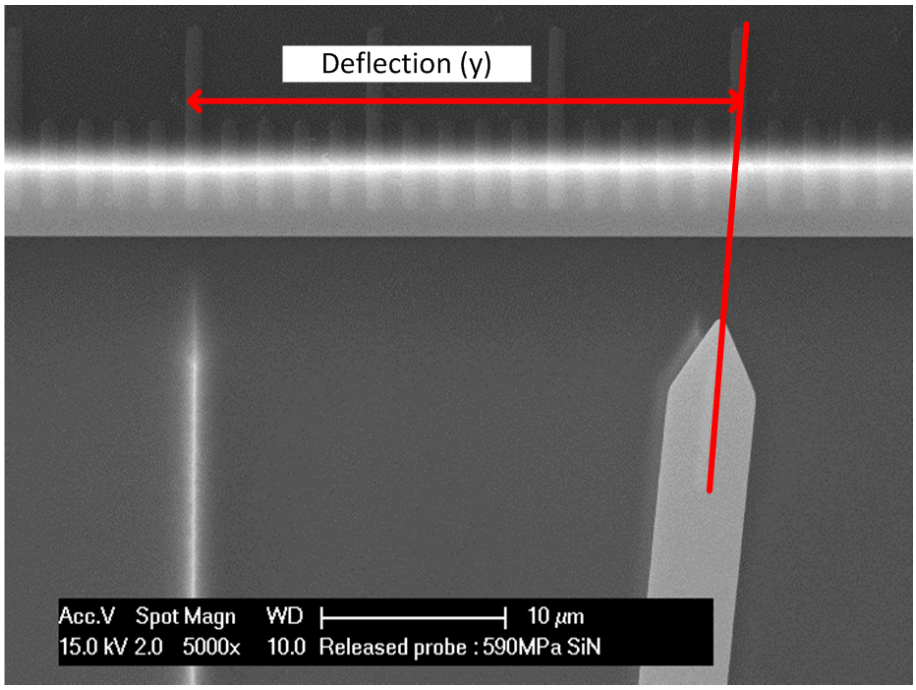

Figure 3.13: The deflection of rotating pointer using SEM

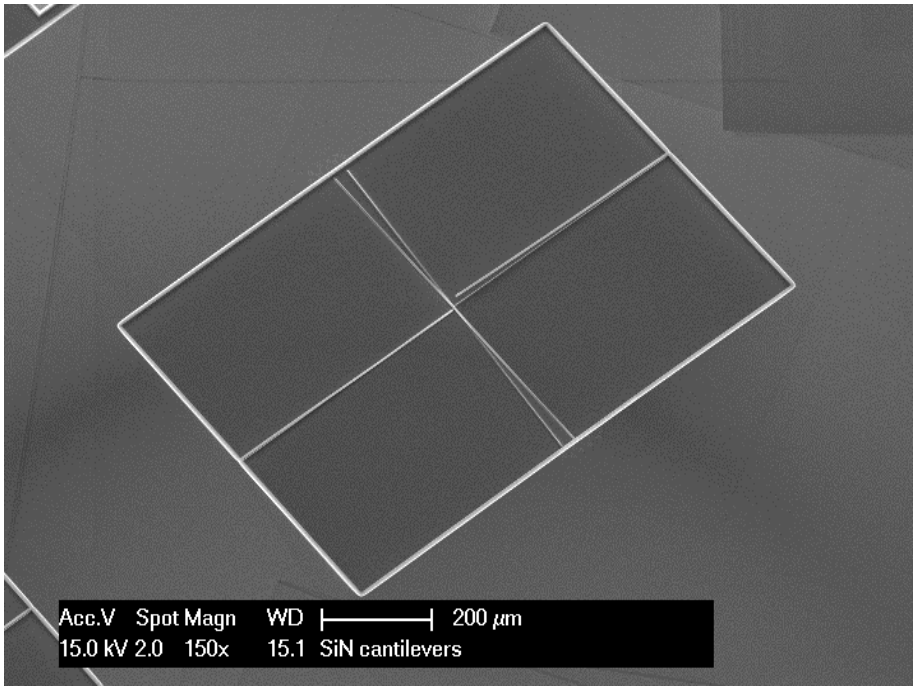

Figure 3.14: SEM images of broken pointers due to high stress

by the phase of the travelling light. It then gets reflected back and, the analyzer and detector detect the changes in the phase.

As different samples were deposited with different nitride compositions, it was important to know the uniformity of deposition. Thus, five points were taken on the wafer (refer Fig. 3.16) and each point was analyzed in order to show the uniformity. It also helped us to determine an average optical constant for the layer. The data for five point analysis as well as overall constant is shown in Table 3.9.

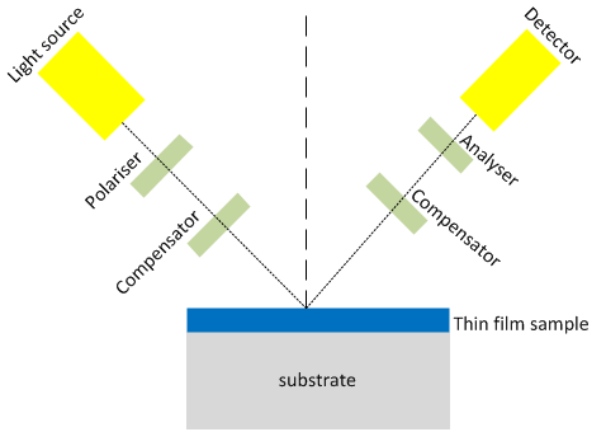

Figure 3.15: Experimental setup for Ellipsometry

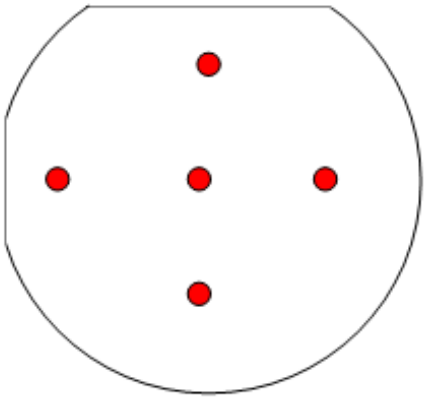

Figure 3.16: Five point measurement for optical constant

Result and Conclusions

The optical constant graph as a function of stress and a table with average optical constant at various stress levels is presented in Fig. 3.17 and Table 3.9 respectively. It shows that the optical constant increases by increasing the residual tensile stress. The measurement is done using ellipsometry and it works in the polarization mode.As the material is not under any external field which polarizes it. The main polarized factor is the residual stress in the layer itself.This change also indicates the change in the content of Si and N in the surface [25, 29]. While fitting the curve it was observed that fitting range of wavelength varies with the variation in stress, this also indicates the change in material properties.

Table 3.9: Refractive Index

Gas Ratio(DCS/NH_3)	Stress(MPa)	Refractive Index (5 point average)
312/88	370	2.125
280/120	430	2.115
240/160	590	2.078
180/220	640	2.027
140/260	720	2.041

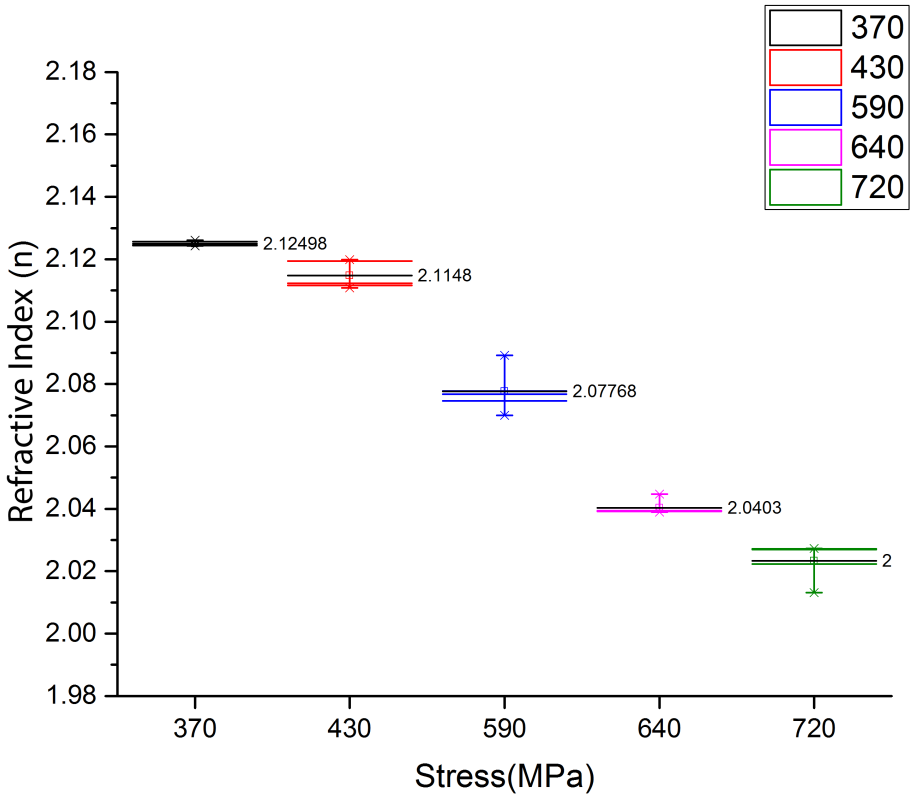

Figure 3.17: Refractive Index at different stress

The refractive index of Si and Si_3N_4 at 632.8 nm are 3.882 and 2.023 respectively. As the residual tensile stress is increased the amount of ammonia in the gas ratio is increased, the refractive index comes very close to the nitride Si_3N_4.

3.4.2. FTIR Analysis

FTIR stands for Fourier transform infrared, one of the widely used methods in present day spectroscopy. It is used to detect the molecular combinations in a material. FTIR working is similar to that of Michelson Interferometer. A basic diagram of FTIR is shown in Fig. 3.18.

The Michelson interferometer shown in Fig. 3.18 shows four major components:

- Fixed mirror
- Movable mirror
- Beam splitter
- Detector

A beam of IR light generated from the IR source strikes the beam splitter. The beam-splitter splits the beam into two equal parts and directs each part to a equally distant moving and fixed mirror, placed perpendicular to each other. Ideally, as the mirror are placed at equal distances there should be zero path difference between the two light beam after reflection from the mirror. But, there is a moving mirror which moves as the light strikes on it. This creates a path difference between two light beams which meet back to the beam splitter after getting reflected from the two mirror. This generates an interference pattern ranging between constructive and destructive interference known as interferogram. This resultant beam is then passed through the sample and gets detected at the

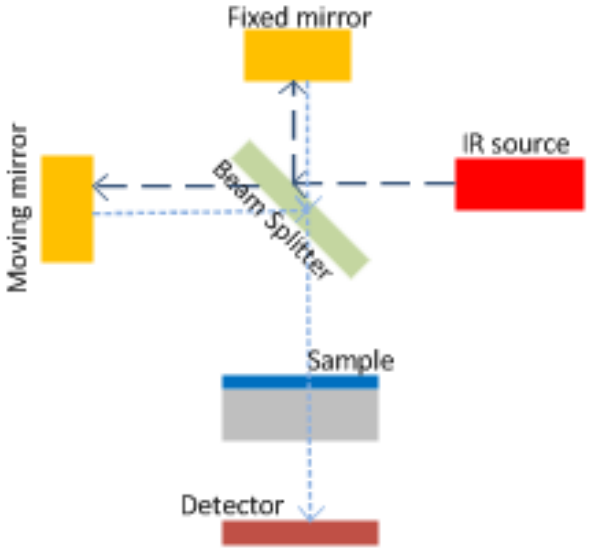

Figure 3.18: Basic working of FTIR

detector. Interferogram is a time domain graph. Fourier transform is used to convert it to frequency spectrum.

Firstly, bare silicon wafer is taken as sample to understand the reference of Si-Si bonding. Secondly, the wafer with silicon-nitride membrane is loaded and measurement is done. As the second measurement contains information about both the Si-Si bonds as well as Si-N bonds, the reference is subtracted from the second measurement to get data only about Si-N bonds. These data is then compared from the references from literature to find out the content of Si in the sample.

Results and conclusions

Table 3.10: FTIR peaks

Stress (Mpa)	Si-N peak (cm^{-1})
380	845.8
430	844.5
590	841.7
640	838.9
720	836.9

The peaks detected from FTIR measurements are shown in Table 3.10. It is not easy to observe the peaks in the figure in Appendix F. As the thickness of the wafers was constant the intensity of light abosrbed was same but peaks have some shift, whcih predicts either stretching of bonds or a slight change in composition. Thus, Table 3.10 has an updated for reference.

3.5. Surface Roughness and Density Characterization

3.5.1. Surface Morphology using AFM

Atomic force Microscopy (AFM) is one kind of scanning probe microscope (SPM). All SPM techniques uses probe to detect the surface properties like height, friction etc. AFM is now one of the most common tool for material characterization.

As shown in Fig. 3.19, the cantilever lever tip interacts with the sample either in contact, non-contact or tapping mode. The movement of the tip is controlled in both vertical and lateral direction. It is

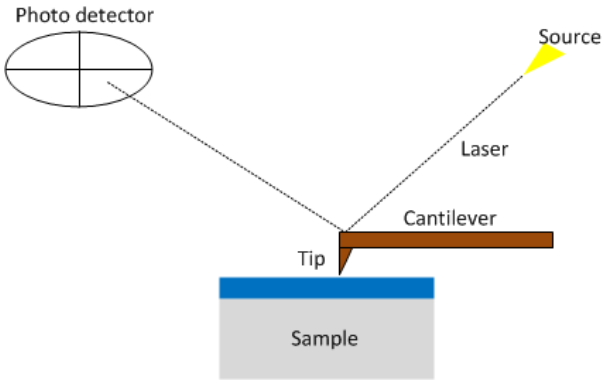

Figure 3.19: Working of AFM

controlled by Beam Deflection Method. The beam deflection method works as: a laser is deflected from behind the tip and is collected at the 4-quadrant photo detector arrangement (shown in Fig. 3.19), which gives the feedback to the positioning electronics, which in turn controls the motion of the cantilever.

Results and Conclusions

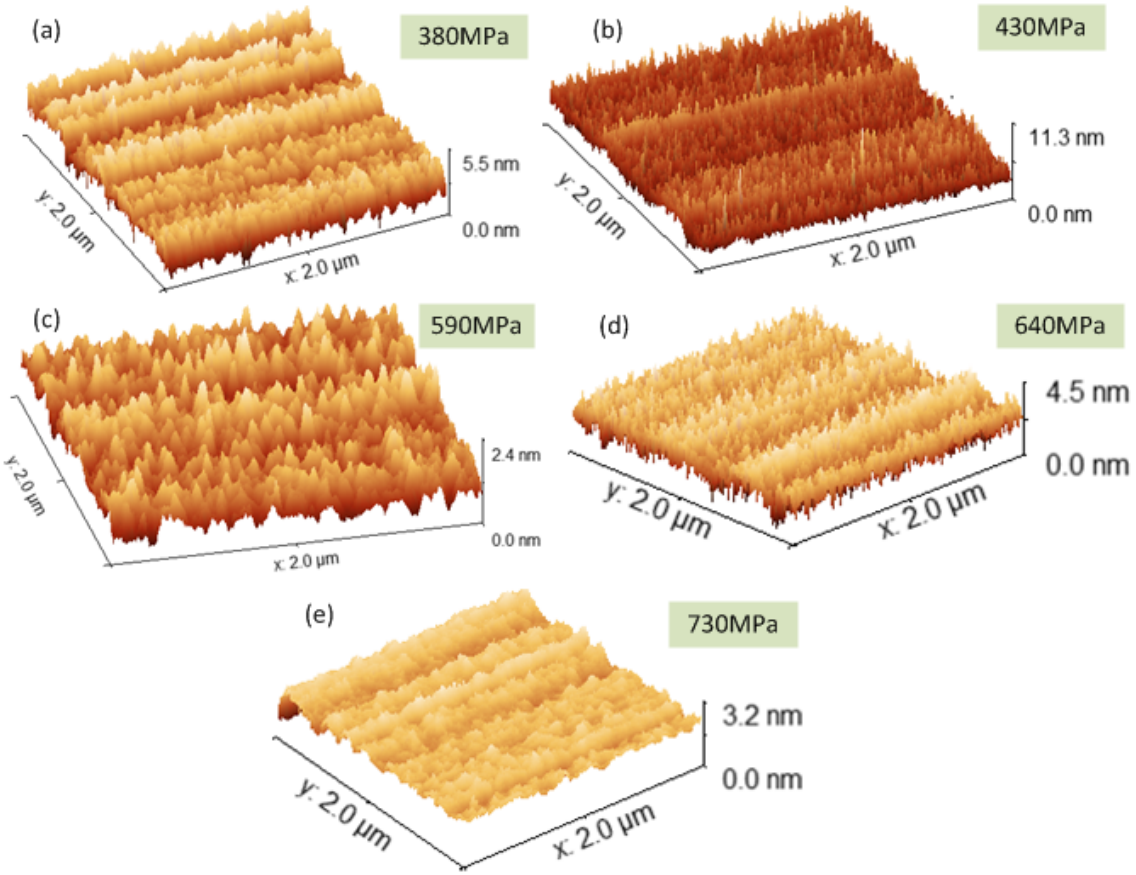

Figure 3.20: 3D images from AFM at different stress

3D profile of the LPCVD-SiN$_x$ is shown in Fig. 3.20. AFM was done in order to check the basic surface roughness. It is found the Mean Square surface roughness is less than 1nm (Refer Table 3.11), which completely lies within the range of LPCVD SiN_x [30]. A low surface roughness (~5 nm) is desirable for microelectronic applications [13]. The average grain area (GA_{av}), average grain width (GW_{av}) and RMS surface roughness (S_Q) is also presented. Although no trend could be found in this regard. Further studies are required to comment anything about the grain area and width.

Table 3.11: Surface roughness at various stress

Stress (Mpa)	GA_{av} (nm^2)	GW_{av}(nm)	S_Q(nm)
380	2424	32.43	0.560
430	6238	7.889	0.259
590	1232	10.46	0.142
640	4624	32.50	0.148
720	436.8	13.17	0.109

3.5.2. Density Characterization

As the content of silicon and nitrogen atoms vary in the thin film deposition, the density is bound to change. Thus, characterization of density was important. The density characterization was done by measuring the mass of silicon wafer before depositing the nitride and after the nitride deposition. The mass of the wafer after deposition is subtracted from the mass of the wafer before deposition. It gives the mass of the thin film deposited. As LPCVD deposits, on both sides of the wafer, the obtained mass is further divided by a factor of two. It is mathematically expressed in Eq. (3.7)

$$M_t = \frac{M_{SiN+Si} - M_{Si}}{2} \tag{3.7}$$

where, M_t = Mass of the thin film
M_{SiN+Si}= mass of the wafer after deposition
M_{Si} = mass of a bare Silicon wafer

Table 3.12: Density with various stress

Sample	Stress (MPa)	Density (g/cm^3)
S1	420	2.794
S2	590	2.713
S3	640	2.570
S4	720	2.229

Conclusions

The results of density characterization can be seen in Fig. 3.21. It can be seen that with the increase in residual tensile stress the density decreases. It is already known that increasing the content of ammonia while depositing the nitride layer increases the residual stress. The atomic mass of nitrogen is lower than silicon. Nitrogen (14u) is lighter than Silicon(28u). The increase in amount of nitrogen, increases the nitrogen content in the membrane.Thus, density of low stress films(more Si) was found to be higher compared to the density of higher stress films.

3.6. Conclusions

The study of residual stress was done in detail. Gas-ratio (DCS/NH_3) for introduction of low to high tensile stress were found and thin films were deposited. Deposition rates were calculated and a saturation in the deposition with respect to gas ratio was found. The stress was characterized. The stress was found to be saturating with increase in the ammonia content. The strain was calculated using the fabricated rotating pointers. With the available stress and strain, Young's modulus was calculated. Refractive index characterization using five-point measurement. It also indicated the uniformity of deposition. FTIR analysis was done too see the IR shift in spectra with increasing nitrogen content. Density characterization was done and a decrease in density with increase in ammonia content was

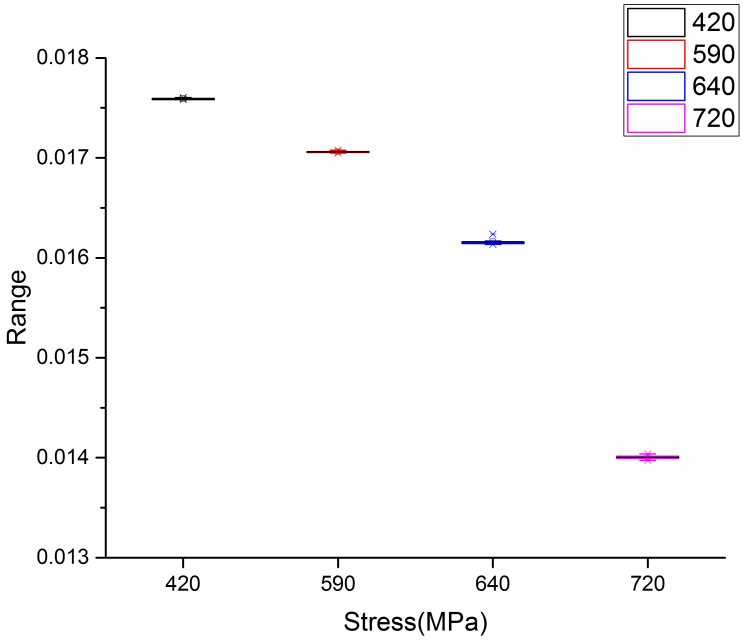

Figure 3.21: Density variation with Residual stress

found. This was probably due to a relative increase in nitrogen bonds in the material. Atomic force microscopy was done to measure the roughness of the materials. The roughness was found to be well within the limits of LPCVD silicon nitride. The characterization was important to understand the further experiments. With the knowledge of basic material properties, this thesis can move forward to manufacture membranes.

4

SiN_X Membranes

4.1. Introduction

In Chapter 3 it has been stated that this thesis tries to explore the effect of residual stress in order to reduce bulging. The variance in the observed material properties makes it interesting to observe the effect of stress in the membranes. For testing the bulging in the membranes, the devices are diced and individually placed on a test setup. This method is time consuming and requires delicate handling of the diced membranes. In order to improve the testing methodology, wafer level testing of membranes is developed in this thesis. Another goal is to investigate the mechanical reliability of the devices under pressure loading up to 1.5bar.

In this chapter, design and characterization of wafer-level pressure testing of membranes is discussed. The design requirements and concept is discussed in Section 4.2. Masks with embedded micro-channels designed for this process is described in Section 4.2.2. Moving further, the fabrication of these wafer level testing along with test structures is discussed in Section 4.2.3. The test methodology and setup is discussed in Section 4.2.4.The processing and results are tabled in Section 4.3.2. The last Section 4.3.2 tries to extract Young's Modulus using the available deflection, after measurements using the simulations.

4.2. Wafer-level pressure loading system for micro-hotplate/nano-reactor

In order to mimic the chemical reaction at atmosphere pressure, the maximum inner pressure in the nano-reactors needs to reach 1 bar. This means there is a 1 bar pressure difference across the both membranes on the top and bottom of the gas channel. Thus the reliability of the SiN_x membrane under such high pressure difference is essential.

In current products, pressure loading test is performed on each individual chips. To guarantee the stability when working at 1 bar across the membrane, a higher pressure difference up to 1.5 bar is used during the test. As the test is done in atmosphere condition, an absolute pressure of 2.5 bar is applied as schematically shown in Fig. 4.1. As the flatness of the fixture is not good enough for the pressure-tight sealing, special O-ring is often used.

4.2.1. Concept for wafer-level pressure loading system

To load pressure on wafer-level, a straight forward concept is done by mechanically clamping the wafer while applying a high pressure on the bottom side as shown in Fig. 4.2a. This approach is however limited by the following aspects,

- The force load is too high. A 1.5 pressure difference on the entire wafers bottom surface generates more than 1000 N force, which equal to 100 kg mass loaded on one side of the wafer. To compensate this amount force without bending the wafer or too much (avoiding breaking or leaking issue), the holder and the fixture (the cap on top of the wafer) will be quite bulky.

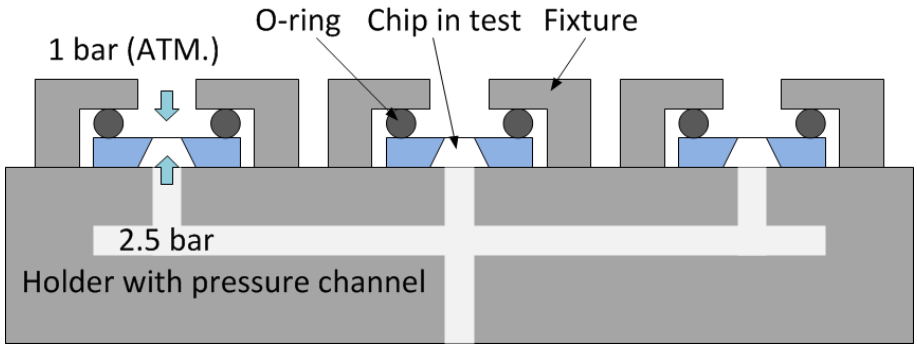

Figure 4.1: A conceptual drawing of the pressure loading system for individual chip test

- Cross-talk between broken membrane and other membranes. In case of broken membranes due to mechanical failure, the pressure in the pressure chamber will drop dramatically, leaving the test on the other membranes non-reliable.

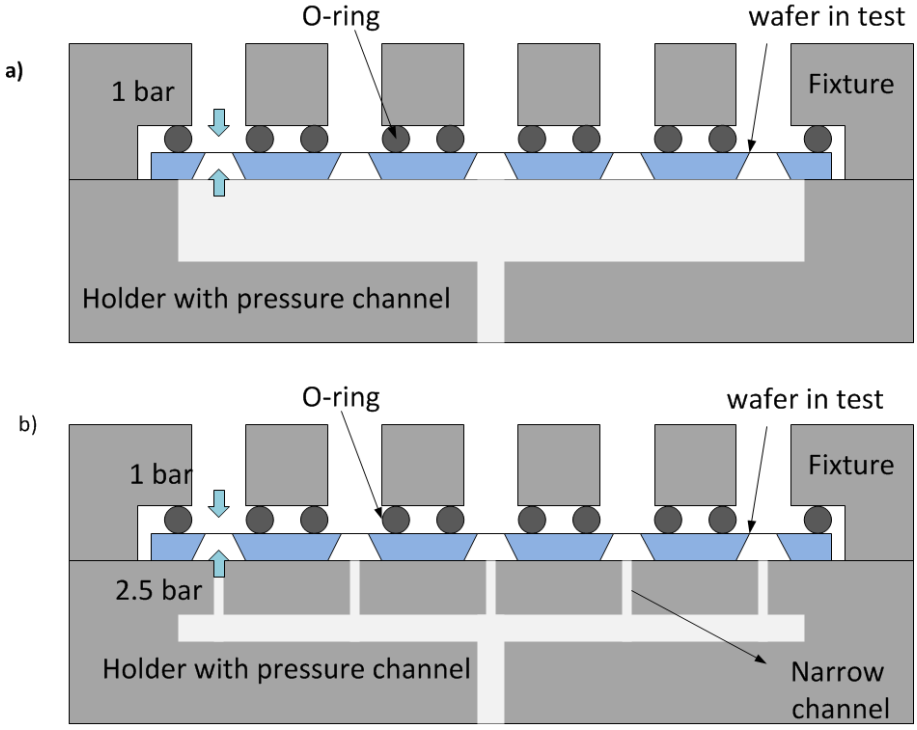

Figure 4.2: a) Conceptual drawing of the wafer-level pressure loading system with a pressure chamber, b) Wafer-level pressure loading system with narrow channel distributing the pressure.

To address the above two issues, the complex gas channels can be fabricated into the holder as shown in Fig. 4.2(b), narrow channels (or chock points) can be used to limit the gas flow (thus less pressure drop) in case of broken membrane. This however increase the complexity of the fabrication of the holder, and it also require a better precision during the fabrication. Furthermore, hundreds of O-rings are required in the assembly to seal the pressure or provide soft contacts (to avoid force concentration). The top fixture can make the top side of the wafer difficult to access, giving less flexibility to combine the pressure loading system with other measure techniques (optical, electrical, etc.).

To overcome the above mentioned issues, a pressure distributing approach with vacuum clamping on the same side is proposed Fig. 4.3. The system benefits from a hybrid holder design as per the below points,

- The main mechanical supporting and pressure/vacuum accesses are achieved with a metal holder fabricated with conventional machining, where the precision is not critical.
- On top of the metal holder, a pressure/vacuum re-distribution holder is used to precisely distribute the 2.5 bar pressure under each individual membrane with narrow channel design limiting the gas flow. As the total area of the 2.5 bar pressure is kept small, there is still enough space for the vacuum to clamp the wafer in a stable way. This re-distribution holder is fabricated with bulk micro-machining technology, so that precision of the fabrication is not a challenge. For different wafer layout, dedicated re-distribution wafer can be applied.

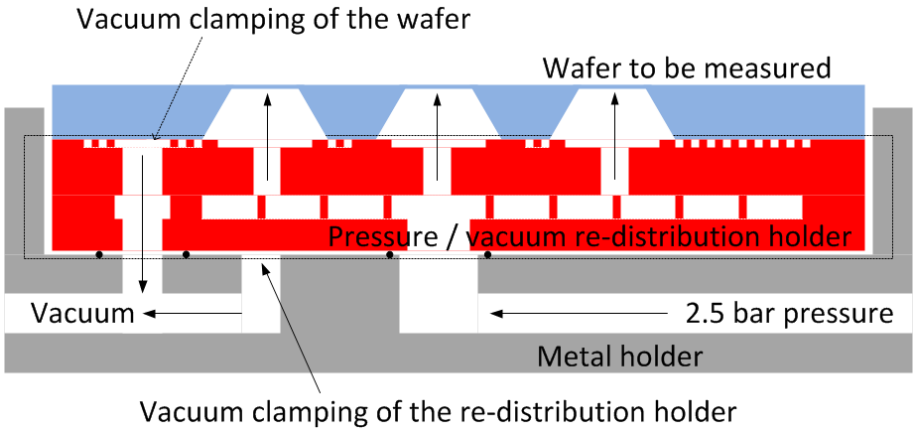

Figure 4.3: Conceptual drawing of the wafer-level pressure loading system with a hybrid holder for pressure/vacuum re-distribution.

4.2.2. Mask Design

As stated before, the fabrication and mask design depends on certain requirements. The requirements for wafer level pressure testing of device are,

- A high pressure inlet for pressure upto 1.5 bar.
- A distribution channel.
- Vacuum holes to hold wafer and device together under high pressure.
- Pressure inlets in sync with the position of hotplates on wafer.
- A way to check the the pressure under the membranes.

As there is a need for formation of a channel, it can only be formed with top and bottom surfaces. This gives the need of using two wafers, creating some spacers between them and then binding them together at the end. The spacers will decide the height of the gas distribution channel. To make vacuum holes from the bottom to top, through holes should be etched. The wafers have to be bonded eventually, the through holes have to be a part of the top as well as the bottom wafers. Hence, the wafers have to be processed at front and back sides. Thus two masks for each wafers brings us to a total count of four masks. It will be easier to visualize if we start from bottom wafer and then come to the top wafer as it is the direction of gas flow.

The mask set designed for the mechanical reliability of membrane under applied pressure at wafer level are mentioned below,

- Bottom wafer Backside mask
- Bottom wafer Top mask
- Top Wafer Backside mask
- Top Wafer Frontside mask

Bottom wafer-backside mask

As the test bed has two output holes: one for vacuum and other for high pressure, the bottom mask should contain the high pressure inlets and the vacuum as its inputs. The high pressure inlets will take the pressure from the test bed and the vacuum will start sucking through the test bed. This part of the wafer level test structure will be in contact with the designed wafer level test bed.

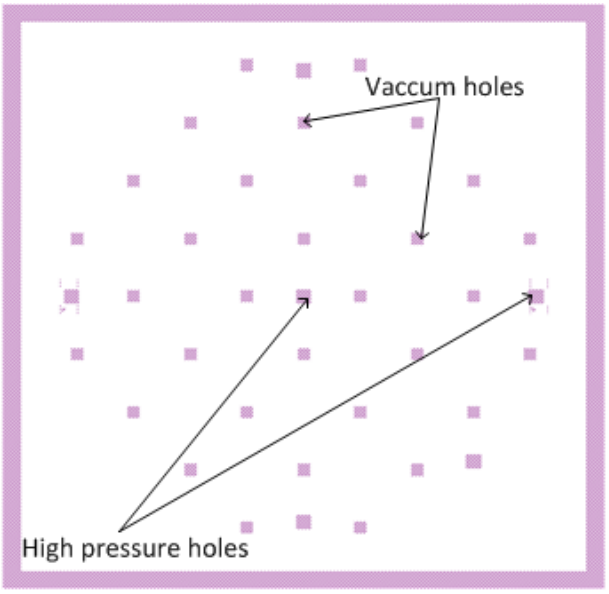

Figure 4.4: Bottom wafer-backside mask layout

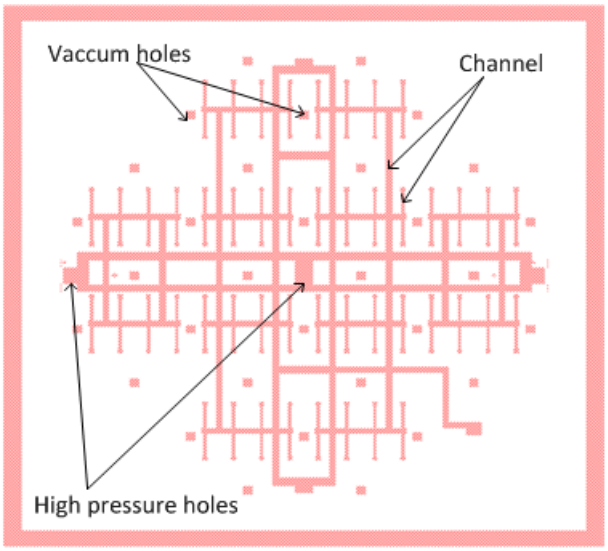

Figure 4.5: Bottom wafer-top mask layout

The bottom wafer-backside mask is shown in Fig. 4.4. It can be observed that both the vacuum holes as well as the high pressure holes in the picture are made in the form of squares. The dimensions of the vacuum holes and high pressure holes are 2mm x 2mm and 2.5mm x 2.5mm respectively.

Bottom wafer-top mask

The bottom wafer should have two major purposes: A high pressure inlet for gases to come in and a channel to distribute the gases into the nano-reactor sites. Both these can be seen in Fig. 4.5. The

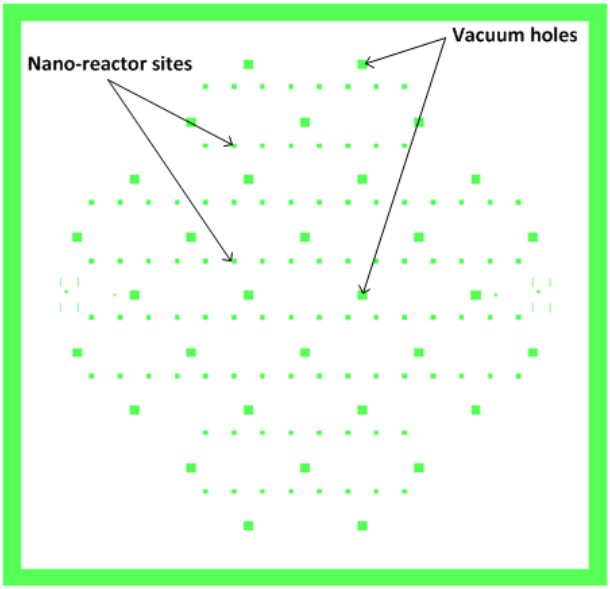

Figure 4.6: Top wafer-back side mask layout

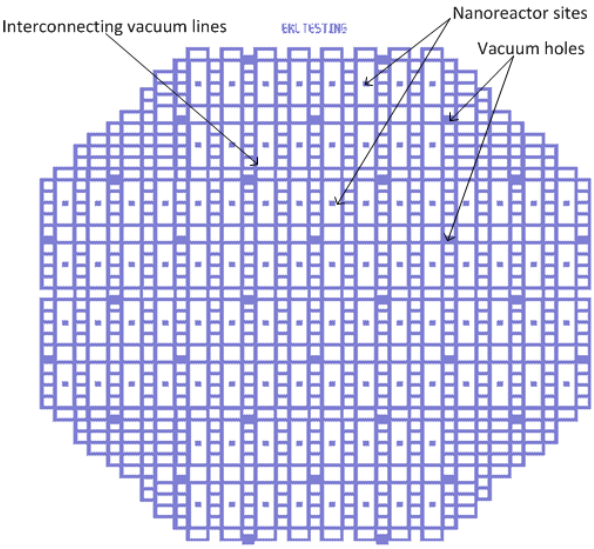

Figure 4.7: Top wafer-front mask layout

third set of structure seen is vacuum holes, which has to be etched through both the bottom and top wafers, so that vacuum reaches the wafer on the device and all the three: the test bed, the device and the wafer with micro-hotplates stick together properly and there is no leakage of gases. The critical dimensions are highest at the entrance point of high pressure gases in order to reduce damage to the pressure burst. The dimension for initial distribution has a width of 2mm and it reduces to 1.5mm in the middle as the flow propagates. It later reduces to 0.4 mm as it goes into the channel for membranes. This dimension distribution is done in accordance with the Bernoulli rule. The change in dimensions makes the flow laminar and free from any turbulent effect.

Top wafer-backside mask

The back side of the front wafer must fulfill two tasks: the back side should also have nano-reactor sites, as during fabrication it needs to be etched from the back for the pressure to reach the sites. Secondly, the vacuum holes should also be present on the back side of the wafer, as the presence of the vacuum has also been designed to hold the wafer with nano-reactors. Both the nano-reactor sites and the vacuum holes are seen in Fig. 4.6. The lateral dimension of the nano-reactor sites are kept

as 0.7mm, which is very close to the membrane dimensions of the nano-reactors. The dimension of these nano-reactor sites are made a little smaller than the membranes of nano-reactor itself to create an impact on pressure of the membrane.

Top wafer-front side mask

This mask is designed for the top wafer on the front side. It can be seen in Fig. 4.7, the mask contains small holes, which are actually the nano-reactor sites. The dimension of these holes are taken with the same configuration as that of nano-reactors, so that there is no offset between the inlets of nano-reactor and the pressure through wafer level pressure testing device.

Lot of vacuum holes are created in order to hold the wafer, the fabricated device and the test bed together. To maintain the uniformity of vacuum throughout the wafer it needs to be connected together. It can be seen in Fig. 4.7 that with the help of interconnect lines all the vacuum holes are connected.

4.2.3. Fabrication of the re-distribution holder

In this process, a double side polished(DSP) wafers were considered for fabrication. This was done as the backside of top wafer needed to be bonded with the front side of the bottom wafer as per the design. As in case of DSP wafers both sides are polished and bonding of two polished surface is stronger. In other cases roughness of backside wafers reduces the quality of bonding. The second reason was that lithography has to be done in both side of the wafer. A smooth surface will lead to better structures (due to better lithography) and probably a similar etching from both sides of the wafer.

A good bonding becomes important in this case as no leakage of air through the channels is allowed. It was observed during initial fabrication that devices with improper bonding leads to heavy leakage although it was not quantified.

A process flowchart is developed for the fabrication of the wafers. The pictorial representation of the flowchart is shown in Fig. 4.8. A detailed flowchart can be found in Appendix B. Some of the critical choices made for fabrication are discussed.

As the first step of any fabrication process is making of alignment markers. This step was performed first. The alignment markers were made by ”Double-oxidation” method (see Fig. 4.8(a)-(d)). This method was used as it is not recommended to use any dry-etching method. The dry etching method generally makes the surface a little rougher and can affect the quality of bonding. A double-oxidation uses the Fick’s law and selective oxidation is done making alignment markers. Interestingly, the oxide in this case was not etched till the last as it was used as a protective layer to keep the surfaces as smooth as possible till the end. Thus, the alignment marks on the oxide was used for all lithography steps and oxide was etched at the last just before bonding.

The next step was lithography. Lithography was required on both sides as four masks were designed in total one for each surface of both wafers. Standard recipes from EVG coater were used. The no-edge bead removal (EBR) was preferred in order to make sure oxide stays everywhere, even in the corners. recipes with EBR will remove oxide from the edges while etching and once again can be a problem during bonding. Manual exposure was done as the masks used were plastic masks and can be used only with manual exposure. The energy of exposure depends upon the thickness of the photo resist and a little extra exposure of around 2-3 seconds should be done. In this case an exposure time step of 30s was used. It should also be checked at what intensity the lamp is working as the light intensity keeps reducing during it’s life-cycle. Hard contact was used during exposure for better accuracy. The development was done in the automatic developer. This lithography step was done for both top and bottom wafer, one time for each wafer surface. Etching of photo resist was done using plasma etching. This dry-etching method was used as it only disturbed the silicon surface which needs to be etched in later steps. Secondly, etching methods are highly selective, so it doesn’t attack silicon.

Etching of the oxide in several steps (Fig. 4.8(c),(e) and (f)) was done done in Buffered Hydrofloric acid (BHF 1:7). It attacks only oxide and leaves behind a smooth silicon surface. This was used to open the windows for through etching in silicon. The opening was made from both sides of the wafer to make the etching faster and maintain the top dimensions and bottom dimensions of holes same. One

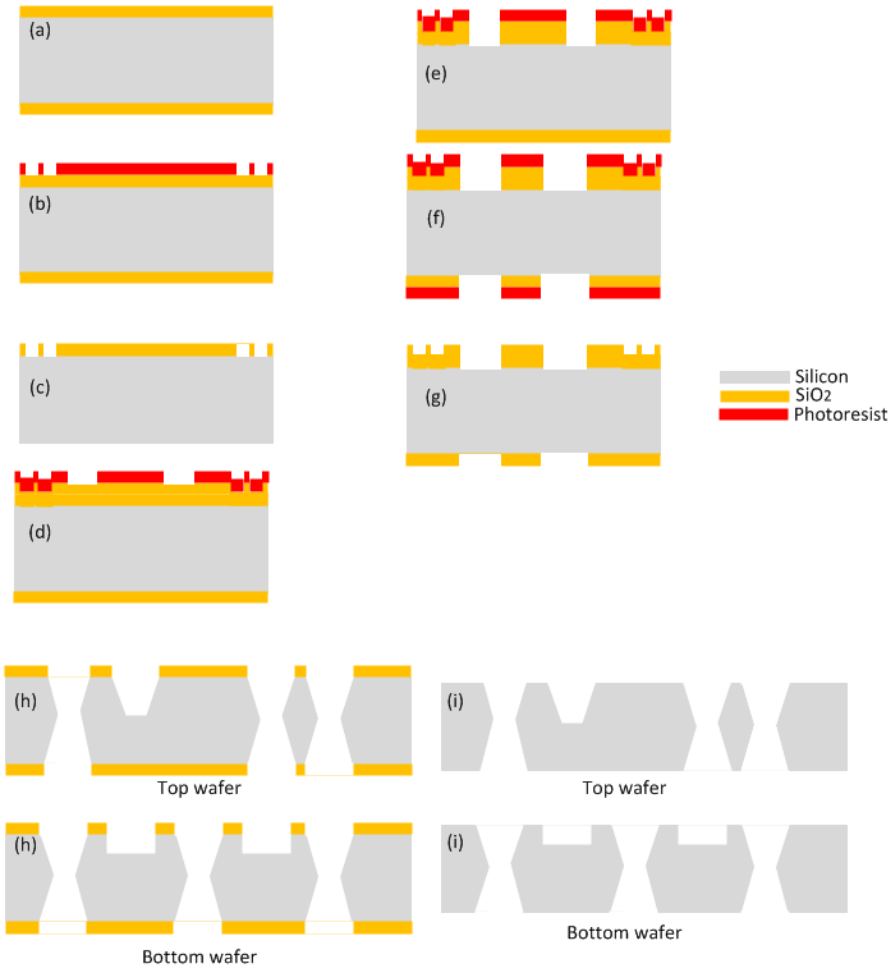

Figure 4.8: Process flowchart of redistribution holder - (a)Thermal oxidation (b) Photo resist patterning on front side (c) Etching of oxide (d) Thermal oxidation and patterning (e) Oxide etching Front side (f) Oxide etching backside (g) Removal of photo resist (h) Top Wafer and bottom wafer before removal of oxide (i) Top Wafer and bottom wafer after removal of oxide

side etching lead to smaller windows at the top. TMAOH was used for etching the Silicon. The opened windows in the front and backside can be seen in Fig. 4.8(g).The reaction between Si and TMAOH produces hydrogen bubble, which marks the beginning of the reaction. The etch rate of TMAOH (25% @85^{o}C) for Si etching is around 0.6μm/min. A visual inspection of through holes was done before taking out the wafers. After the silicon holes were through etched(see Fig. 4.8(h)) the oxide was removed by BHF (1:7) wet chemical etching, gently stopped on oxide silicon interface. (see Fig. 4.8(i)).

HF 0.55% etching and Marangoni drying was used after this in order to maintain the smoothest possible surface for bonding of wafers. HF 0.55% removes the native oxide. As silicon is highly reactive with the oxygen present in the atmosphere it always forms a native oxide. Generally, the thickness is assumed to be 25nm for the native oxide. The next is step is Marangoni cleaning. Marangoni is generally used for removing particles and getting cleanest possible surface. As the wafers has through holes it was also more beneficial. The Marangoni works on the principle of surface tension. The wafers are rinsed in demi-water and while taking it out Iso-propyl alchohal (IPA) is sprinkled which drags all the water droplets from surfaces as well as corner of the holes to the bottom and wafer is completely dried.

The last step after this is bonding with annealing. The bonding is done with the help of special alignment markers made for cameras in the bonding machine. One of the wafers is fixed and other can be adjusted to align the markers. then the distance between two wafers is decreased and a force of 1KN is applied at 500 ^{o}C. It is annealed for an hour to make the bonding stronger.

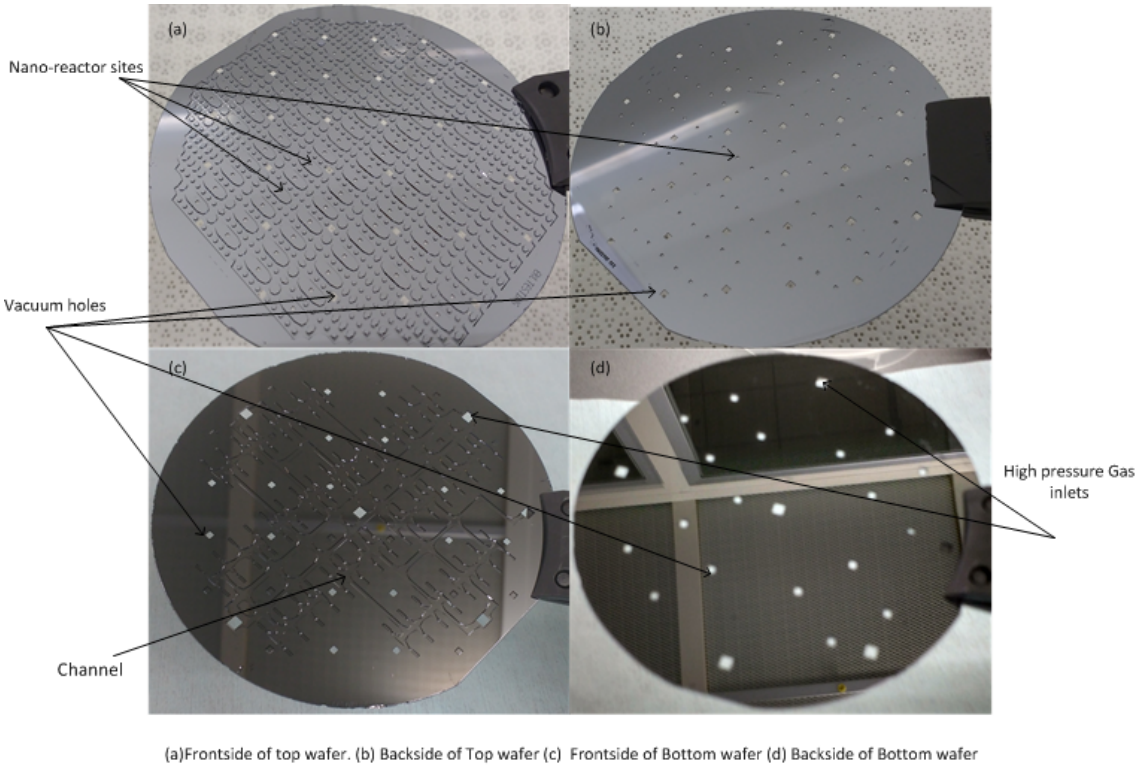

Figure 4.9: The fabricated device before bonding and Annealing

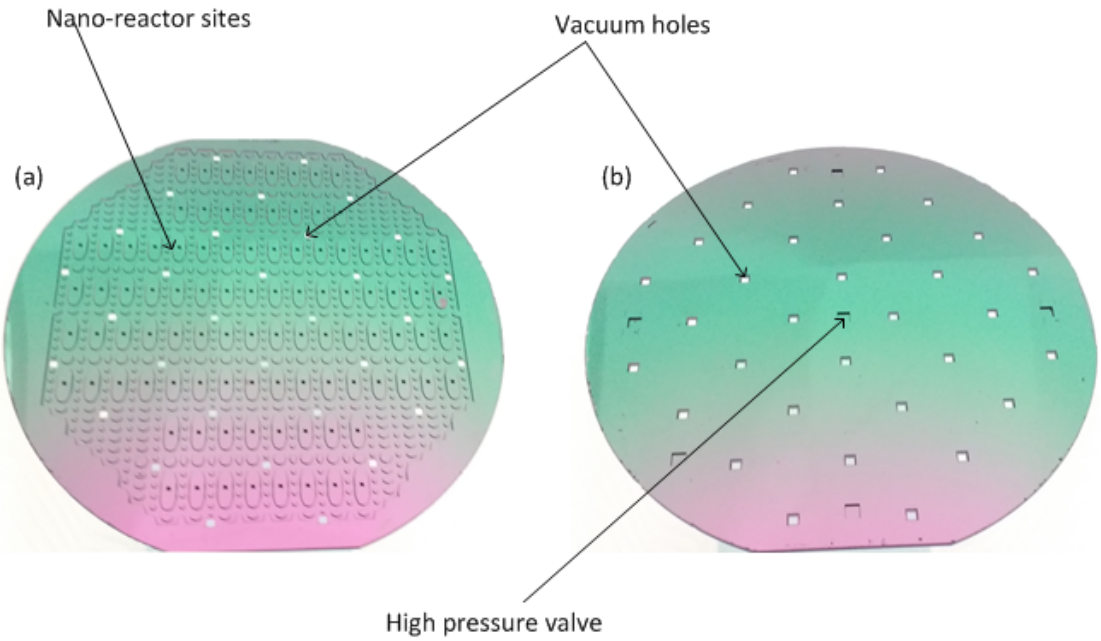

Figure 4.10: The final pressure level testing device

After this an optional oxidation step is done. It is done in order to make the bonding between the two wafer stronger.

The fabricated device before bonding and annealing is shown in Fig. 4.9. It shows that the requirements for this fabrication has been met.

- The vacuum holes are etched through both the top and bottom wafer and can be clearly seen in Fig. 4.9.
- The front wafer (refer Fig. 4.9 (a) and (b)) the nano-reactor are through etched for the pressure to come directly on the devices put on nano-reactor sites.
- The gas inlets are etched through the bottom wafers. (refer Fig. 4.9(c) and (d)).
- The channel structure can be seen in (refer Fig. 4.9(c)).

The final device after bonding, annealing and oxidation is shown in Fig. 4.10

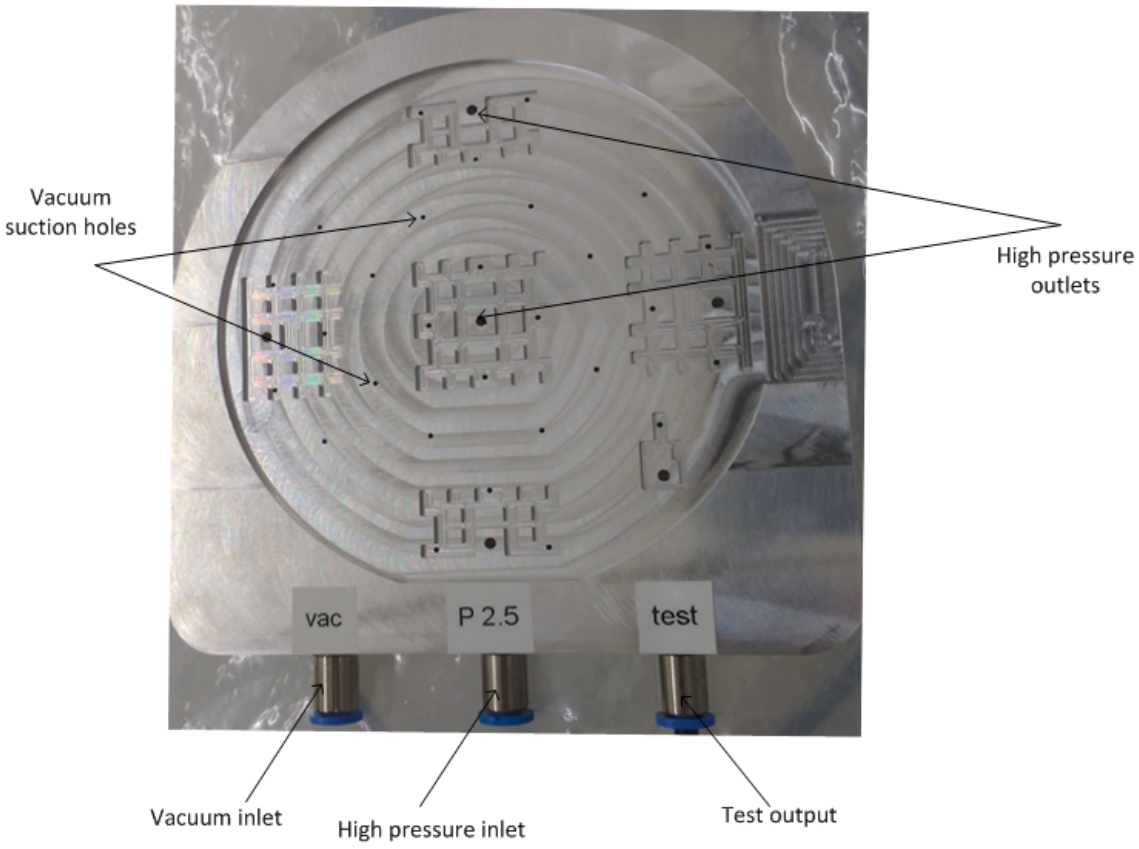

Figure 4.11: Test Bed

4.2.4. Implementation of the measurement system

To test the device fabricated in Section 4.2.3 a test bed is required where device can be kept and pressure can be applied. The test bed setup used for the experiment is described as follows:

- The test bed should have a pressure inlet for high pressure, an inlet for vacuum and a test output to check the pressure distribution. It can be seen in Fig. 4.11 that there are three ports, P2.5 is the port for high pressure, port ”vac” is inlet for vacuum line and port test is an outlet for checking the pressure distribution inside the test bed. So, a pressure meter can be connected here.
- The top of the test bed should be same as the bottom of the wafer level pressure testing device. It means it should take input from inlet P2.5 and distribute it to high pressure inlets as shown in Fig. 4.11.
- The smaller inlets shown on the top is the vacuum suction holes. This helps to hold both the devices and test wafer kept on top of the test bed.

4.3. Bulging measurement with pressure load

4.3.1. Sample preparation

Test samples with different stress in the silicon-nitride membranes were prepared. These membranes mimicked the membranes present in the commercial micro-heaters used in nano-reactors. These membranes were prepared for being tested on the wafer level testing device developed in this thesis.

As the membranes are close to the commercial one, the membranes also should follow a similar process. The process flow is shown in Fig. 4.12((a)-(g)). A complete fabrication flowchart is shown in Appendix C.

The test wafers have to be mounted on wafer level re-distribution holder testing device. So the backside must be polished. It will prevent scratches on the device and a better vacuum suction. Thus DSP wafers were used. The process is briefly discussed. First a 100nm oxide growth (wet oxidation) is done (Fig. 4.12(b)). Oxide is later etched from membrane leaving behind a smooth membrane. Then approximately 400nm of silicon-nitride is grown (Fig. 4.12(c)). Lithography is done on the back side of the wafer (Fig. 4.12(d))followed by dry etching of silicon-nitride and oxide in the back side (Fig. 4.12(e)). The etching was done for approximately 2 mins, in order to land on the silicon surface. Over etch was not a problem here as silicon has to be etched in the exposed area in the later step. The silicon surface was later etched from back side in KOH and the membranes were formed as shown in the Fig. 4.12(f). The dimensions of the membranes for various stress is shown in Table 4.1.

Membranes with high residual tensile stress were getting broken while processing. This could be due to the decrease in reliability of the membrane with increase in tensile stress. The broken membranes were covered with Kapton tape by manual pick and place. The Kapton tape was able to survive the pressure of 1.5 bar while testing the device.The kapton has also high thermal stability.

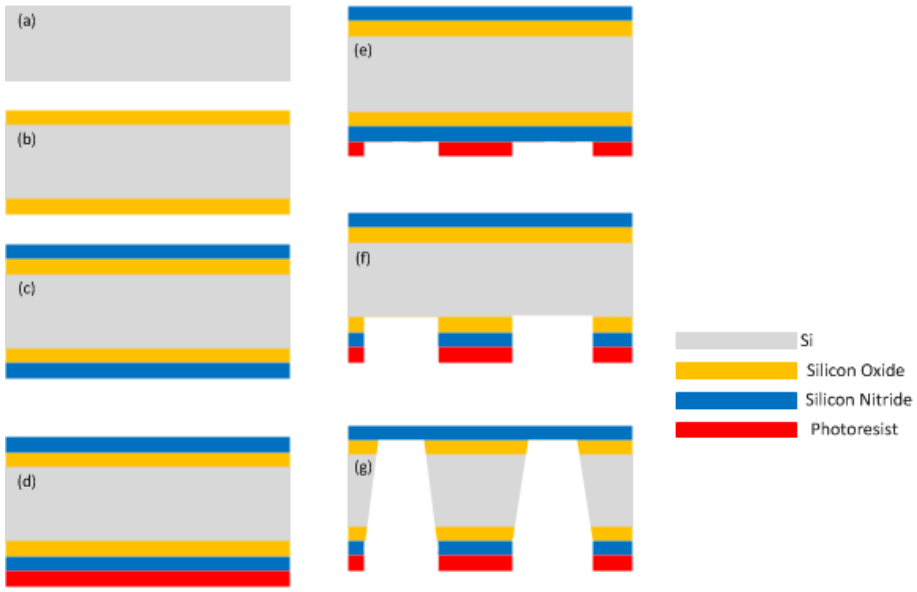

Figure 4.12: (a)Bare Silicon wafer (b) Silicon dioxide deposited (c) Silicon-Nitride Deposition (d) Photo resist on the back side (e) Photo resist patterning (f)etching back side with TMAOH

4.3.2. Bulging measurement

The bulging profiling was done under KEYENCE profilometer as shown in Fig. 4.13. It uses both optical as well as laser imaging to capture the profile. The wafer testing re-distribution device developed is kept on the test bed. The wafer with membranes are kept over it and then the vacuum is plugged in. It helps in holding all the three together.

The pressure meter was used to monitor the flow inside the test bed. The pressure meter has input from the high pressure line for nitrogen pumps inside EKL. The pressure meter controls the flow of

Table 4.1: Various membrane sizes at different stress level

Stress (Mpa)	Measured dimension of Membrane (μm)
370	806.213
430	806.364
590	806.506
640	809.272
730	805.01

pressure inside the device. The pressure was varied as 0.5 bar, 1 bar and 1.5 bar and bulging profile was registered. The EKL vacuum line was used for suction. The test was connected to a pressure meter for initial testing to check the variance in the pressure. The test was found working fine and the input pressure was in sync with the output pressure. Thus, during the actual measurements the pressure meter was not connected.

The stage of the KEYENCE and the lens had a clearance distance of 5cm in total. The test bed that we had has a height of approximately 2cm height leaving behind 3cm clearance. Thus all the profile measurement were done at the lowest resolution as the increasing the lens resolution would have almost touched the sample.

The results obtained from three sources: A mathematical formulation, simulations and the results

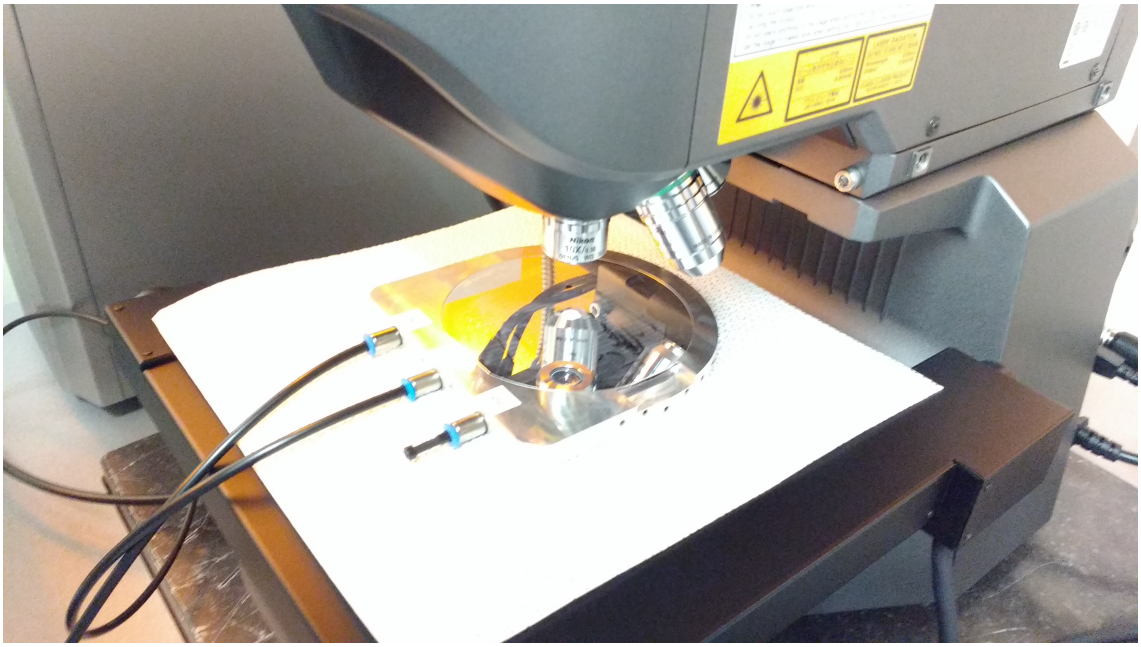

Figure 4.13: KEYENCE profilometer test setup

from fabrication. The results will be discussed in this section.

The raw data is obtained from Fig. 4.14. This data has to be processed before analyzing. Various image processing attributes like marking a reference plane. The reference plane is marked as the layer just beside the membrane. It is done using area selection. The next processing is done by correcting the tilt of the plane. Surface smoothing and height cut attributes was of the KEYENCE software was also used. After doing this the same processing was propagated to all the data to maintain the uniformity.

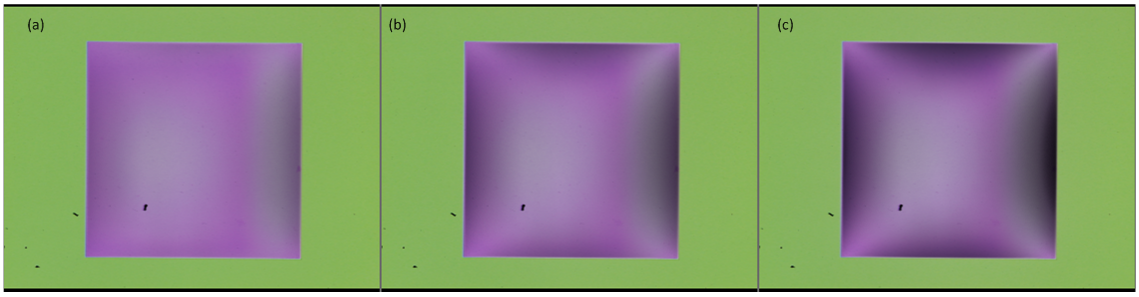

Figure 4.14: A sample laser and optical image profile from KEYENCE for (a) 0.5 bar (b) 1 bar and (c) 1.5 bar

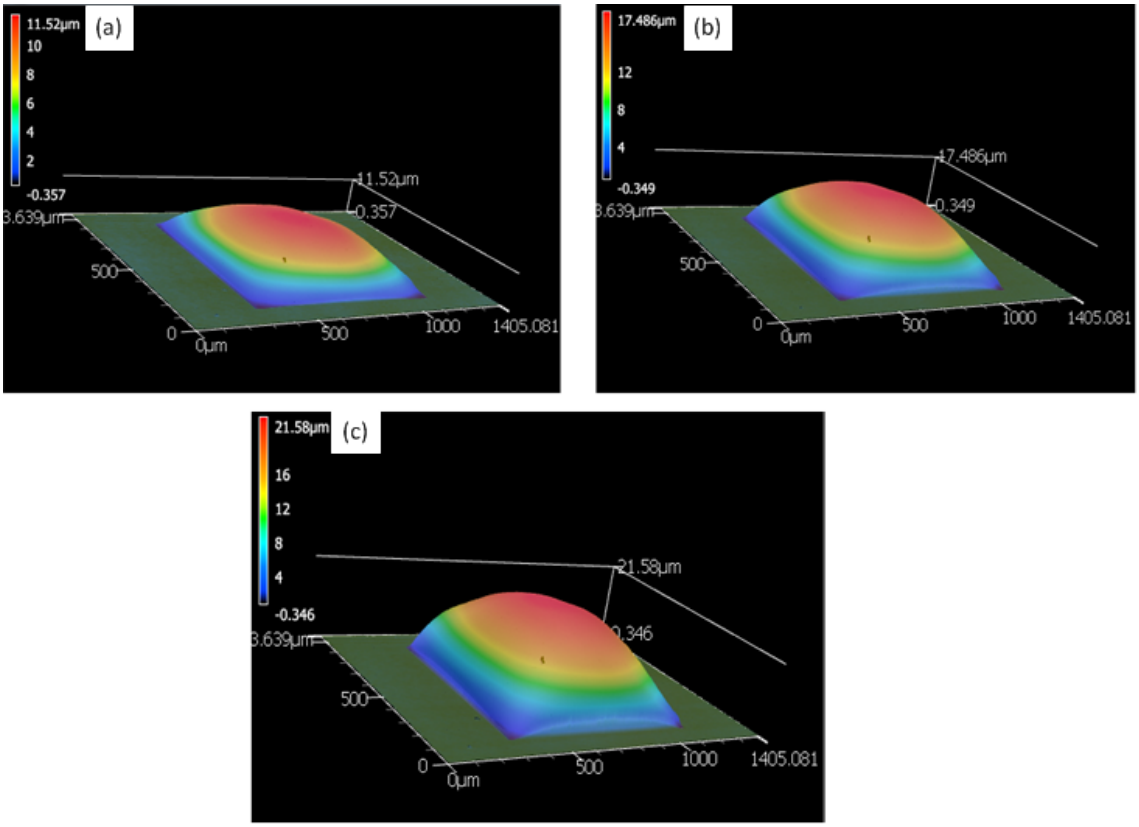

Figure 4.15: A sample bulging profile from KEYENCE for (a) 0.5 bar (b) 1 bar and (c) 1.5 bar

After the processing the 3D profile of the membranes the output images was generated. It can be seen in Fig. 4.15. The data was collected at pressure of 0.5bar, 1 bar and 1.5 bar. The data was collected for various stress levels. one of the collected data for a stress level of 370 MPa has been plotted in Fig. 4.16 for reference. The collected data was presented in Table 4.2.

Conclusion

In this section we see bulging results from simulations, processing and analytical model. All the data is present in table Table 4.2. It can be observed form the table that the introduction of the stress does make an impact but the impact is not very high. It means that the reduction can be seen in case of bulging but the the bulging still exist. The further increase of stress can help but certainly it will go into highly tensile region and it's very difficult for the membrane to operate. As we have already seen while fabrication membranes were getting broken. Any further increase in tensile stress will hugely question the reliability of the membrane. The data obtained from Keyence has a difference from simulated and mathematically calculated values. This is due to the fact that COMSOL and mathematical models used standard material data to calculate the deflections.

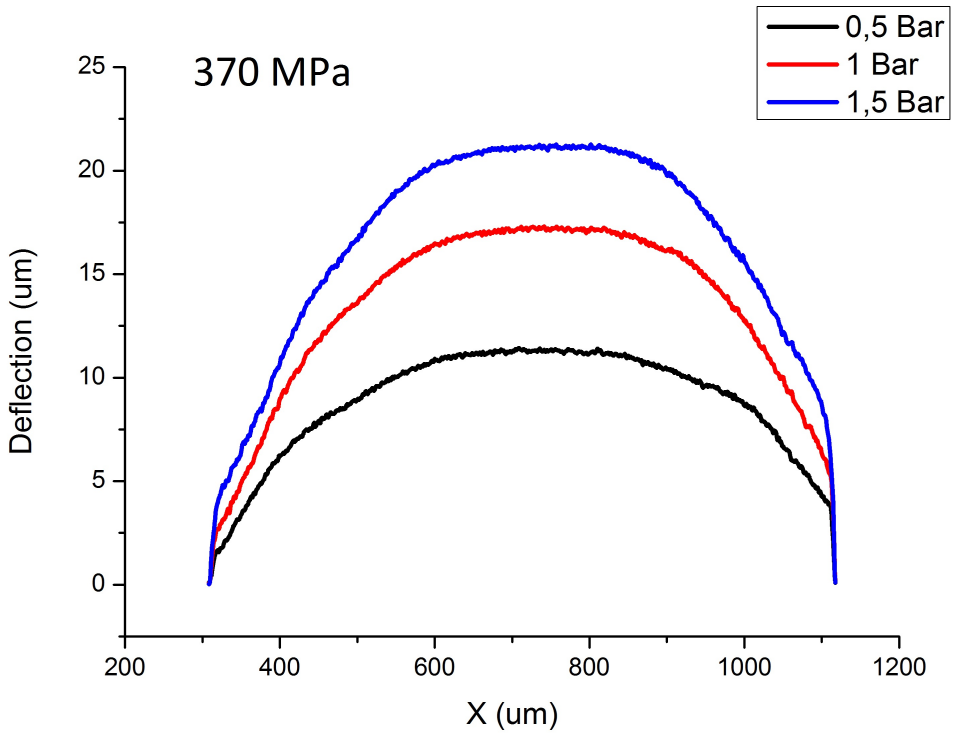

Figure 4.16: Bulging profile from Keyence for 370MPa at three different pressure

4.4. Extraction of Young's Modulus

Simulations

The simulations in this section uses the same model as shown in Section 2.3.2. As it doesn't require any power source and thermal expansion component. The thermal domain has been disabled. The simple model uses the face load to apply the pressure. The Young's modulus is scanned in the range of 100 GPa to 400 GPa. These simulations were done at a constant pressure of 1.5bar. The deflection is already known from experiments. The approximate deflection was found and the corresponding young's modulus was assumed to be the the value for that particular stress.Though, this is a method to extract the Young's modulus but as we are keeping the other material constants like Poisson's ratio, density etc. so, only an approximate range of value can be found. The thickness and dimensions of the membrane were varied with each value of stress. The values extracted is presented in Table 4.3
The young's Modulus extracted from this simulations shows a very similar trend with respect to the data extracted from rotating pointers presented in Table 3.8

4.5. Conclusions

In this chapter, a new methodology for wafer-level pressure testing of membranes was developed. The design requirements, feasibility of the process and measurement set-up were studied and process flow was developed. Bulging measurements with pressure load and KEYENCE profilometer for different stress level membranes was tested. Using the deflection results obtained from measurements, Young's modulus was extracted. The Young's modulus was found to be very close with the values calculated using rotating pointers.

Table 4.2: Measurement of bulge from various sources

Stress (Mpa)	Pressure(bar)	Deflection(μm) Surface maximum	Deflection-COMSOL(μm)	Deflection -Eq. (2.1)(μm)
370	0.5	11.637	11.2108	9.725
	1	17.628	16.788	14.003
	1.5	21.508	20.534	16.875
430	0.5	10.505	10.534	9.261
	1	14.966	16.168	13.60
	1.5	20.439	19.97	16.514
590	0.5	9.187	8.663	7.909
	1	15.073	14.288	12.352
	1.5	19.106	18.232	15.383
640	0.5	8.007	8.167	7.5324
	1	14.283	13.7398	11.979
	1.5	18.623	17.707	15.037
720	0.5	8.365	7.464	6.974
	1	14.740	12.9057	11.40
	1.5	19.289	16.889	14.493

Table 4.3: Young's Modulus Extraction using COMSOL

Stress (Mpa)	Young's Modulus-COMSOL (GPa)
370	230
430	250
590	225
640	250
730	190

5

Fabrication and characterization of micro-hotplate with desired pre-stress

5.1. Introduction

Chapter 3 has introduced the concept of reduction of shift in 'z' direction by introducing residual stress in the SiN_x membrane. Whereas, chapter 4 checks the reliability of these stressed membrane and confirmed it's operating reliability till 1.5 bar. These results have to be implemented in fabrication and characterization of micro-hotplate as well as nano-reactors. This chapter uses the concept of residual stress in fabricating the new generation micro-hotplates and nano-reactor.

In this chapter, fabrication of new generation micro-hotplate/nano-reactor device is presented in Section 5.2 , temperature coefficient of platinum heater characterization in Eq. (5.1) and finally the buckling characterization for the working temperatures upto 800^{o}C is discussed in Section 5.4.

5.2. Fabrication of new generation nano-reactors

The flowchart of new generation nano-reactor is shown in Fig. 5.1. A detailed flowchart can be found in Appendix D.

A double side polished silicon wafer is used as the starting material in this process since lithography is done on both front and back side of the wafer. In the first step alignment markers are patterned and etched on the front side of the wafer. In this process, a total of nine wafers for three different deposition parameters are processed. The wafers are numbered for easier sorting during the process.Wet oxidation was done and back side oxide was etched in BHF 1:7.(see Fig. 5.1 (b)-(d)).The initial bending of the wafer is determined using the stress meter.200nm of low stress LPCVD-SiN_x was deposited. The main deposition parameters that are varied for the three different batches are flow rates of DCS and ammonia.The variation in the gas ratio enables changes in residual stress of the deposited silicon nitride. The temperature and pressure are kept constant at 846^oC and 150mTorr. The thickness of silicon nitride is measured using WOOLAM measurement system and the average thickness was found to be 200 +/- 20nm.Silicon nitride on the back side is etched using Alcatel plasma etcher as shown in steps Fig. 5.1 (e)-(f)).

The litho steps were done to pattern with NLOF negative photo resist for platinum evaporation.A platinum layer of 160nm with 20nm of adhesion layer is deposited using CHA evaporator system. As platinum can't be etched easily, lift-off process for platinum (see Fig. 5.1 (g)-(j))has been used. In lift off, the platinum is deposited everywhere and then the resist is removed using NMP.The resists takes away the platinum deposited on top of it and platinum only remains in the place where there was no resist.

The next step was the creating space for TEM windows. Dry etching of silicon nitride using Alcatel plasma etcher is done to create space for windows (Fig. 5.1 (k)-(m)). 20 nm silicon nitride was deposited in the slots.

The KOH window is patterned on the backside of the wafer. Next, the contact pad opening was done before etching of silicon since membranes will be very fragile after the KOH step and handling can be a problem and etching can be a greater problem. Thus the formation of membranes was done at the last step in the process flow. The wafers are placed in a contaminated KOH bath. The etching rate is calculated to be 90nm/min(Fig. 5.1 (n)). This etching process takes about 5 hours. The wafers are removed from the KOH bath by checking if there is no bubbling in the KOH bath. The wafers are cleaned and later diced as individual devices.The final product can be seen in Fig. 5.3.

It can be seen that the fabrication process here shows only the micro-hotplate integrated with the TEM windows. It is because this was sufficient enough for the concept to be tested. Apart form this the complete nano-reactor system will have the upper membrane which will be separated from the bottom membrane by the spacers, which are in the form of 'O' rings.

5.3. Characterization of TCR

Three stress values were fabricated. The stress in the underneath layer (silicon nitride in this case)also affects the layer(platinum) [31].The temperature dependence of resistance is given by Eq. (5.1)

$$R = R_0(1 + \alpha\Delta T) \tag{5.1}$$

Three different samples were taken from three different stress level and was characterized for the TCR. The setup and methodology are discussed in the following Section 5.3.1

5.3.1. Setup and Methodology

The devices are characterized using Cascade Micro tech probe station connected to thermochuck temperature controller. The machine has four probes connected to the source measurement unit and oscilloscope. The full system is provided with a microscope to observe the changes in the micro heater.The complete setup is shown in Fig. 5.4 . The samples are kept on the gold plated chuck and probes were placed in contact with micro hotplate electrodes. The chuck was heated from room temperature (25^{o}C) to 200^{o}C in steps of 50^{o}C.

From the graph in Fig. 5.5 it can be seen that the resistance increases with temperature as per the relation Eq. (5.1). In the literature,The TCR value of platinum is around 0.00106 K^{-1}. The slope of the graph in 5.5, which gives the TCR, it is found out to be 0.00182K^{-1}. This value is higher than that available in the literature. This can be due to the fact that the experiments are performed under atmospheric pressure. Convection was not taken into consideration, which is a source of heat loss.

5.4. Thermal Buckling characterization

It has already been explained before that thermal buckling is due to compressive stress. So, as the temperature rises the membrane wants to expand but the ends are fixed. So, the fixed ends generates reaction forces to compensate the demand of expansion and as per newton's third law it should be opposite in nature. If the reaction forces builds up a net compressive stress in the mebrane, it can lead to buckling.

Setup and Methodology

Interferometry will be ideal for characterizing buckling. In this we try intuitively to look into the thermal buckling effect. The devices were kept in cascade micro tech wafer probe station. The device has four contact pads as shown in shown in Fig. 5.7. The contact pads were probed with the four probes available. Two probes were used to inject the current and the other two were used to sense the voltage generated across the heater. The current and the voltage were used to calculate the resistance. The resistance at various currents is shown in Fig. 5.6. The curve has been fitted and the fitting is a second order polynomial. This fitting constants have been used to formulate a relation between Pt heaters resistance and current injected as shown in Eq. (5.2)

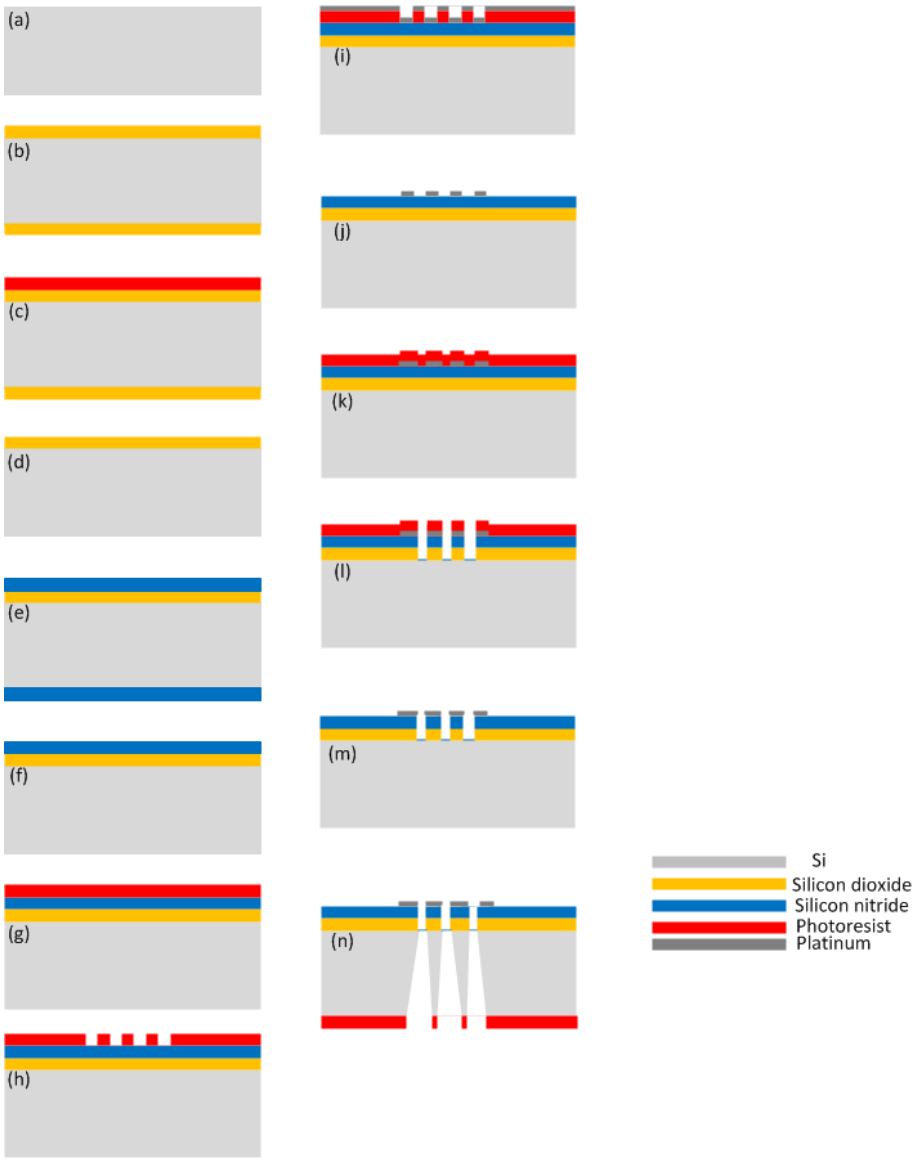

Figure 5.1: Process flow for new generation nano-reactors - a)Bare Silicon wafer (b) Thermal oxide deposition (c) Photo resist on Front side (d) Backside removal of oxide (e) silicon nitride deposition (f) Back side removal of silicon nitride (g)Photo resist front side (h)Patterning of Photo resist (i)Platinum deposition (j)Lift-off process (k)Photo resist on front side (l)Dry etching of silicon nitride (m)Removal of photo resist (n)Backside etching of silicon in KOH

$$R = 163.866 + 585.247I + 674942.706I^2 \tag{5.2}$$

As TCR has already been characterized, The value of resistance at various current was used to find the temperature of the device. The current was swept from 1mA to 20mA. The device at some of the current and temperature is shown in Fig. 5.7. It can be seen that at a current of 5mA there is no buckling at all and at 10mA although there is a little buckling but it can be hardly observed with these images provided. Fortunately, buckling can be seen with a current of 15mA very clearly. The device was burnt, probably the membrane broke at a current of 20mA. The breaking temperature was found to be 928.23^oC. The stress of the membrane used in this device was 290MPa.The experiment gave an intuitive understanding of the buckling. It can also be seen that the temperature range for buckling is improved a little.

The buckling characterization was also done at DENSolutions B.V, Delft. The graph obtained for z direction displacement with temperature is shown in Fig. 5.8

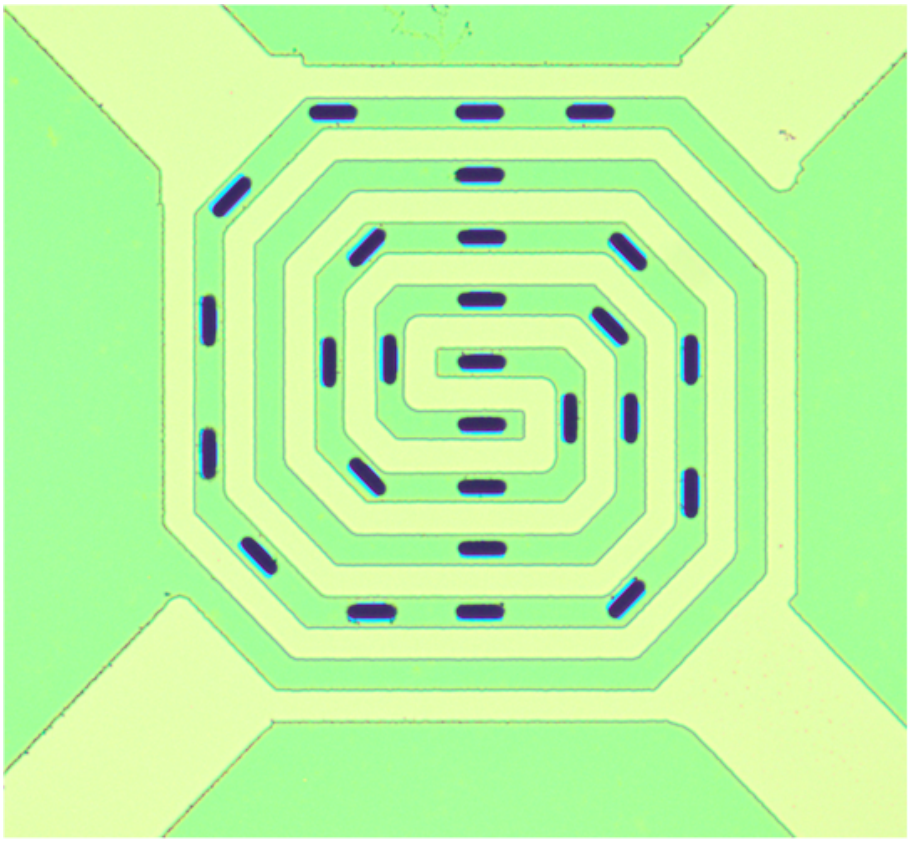

Figure 5.2: optical image of micro-heater with integrated TEM Windows

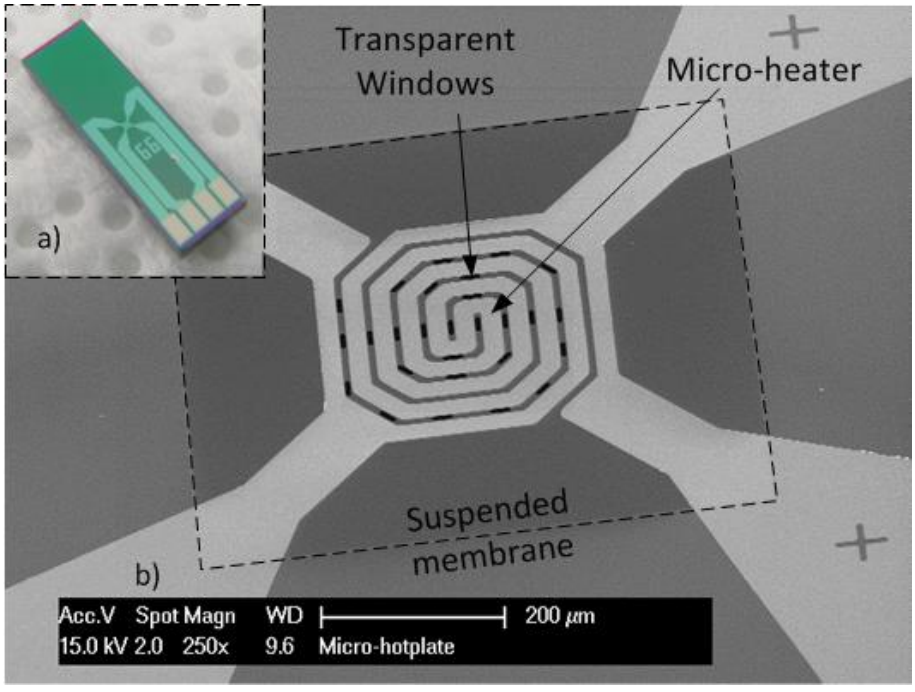

Figure 5.3: Micro-heaters with integrated TEM windows. (a) chip level (b)SEM

Conclusion

Using the test setup presented in this chapter, the thermal buckling has been characterized for the stress levels of 230 MPa and 290 MPa. The concept of thermal buckling has been introduced in Section 2.3.2.

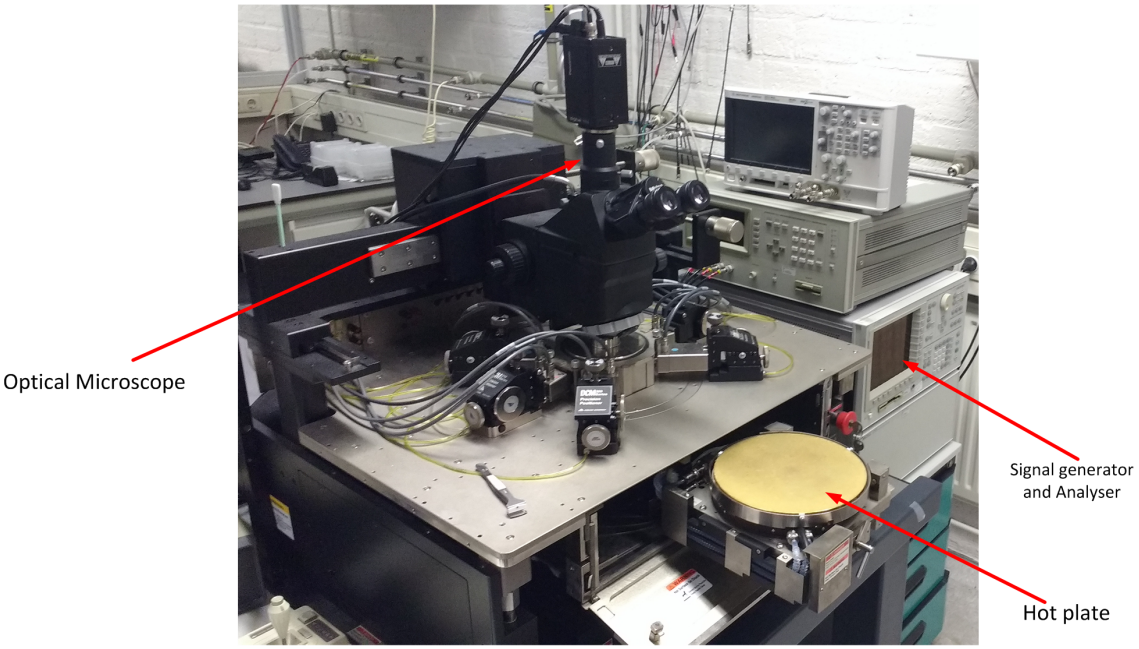

Figure 5.4: Cascade setup for TCR characterization and buckling

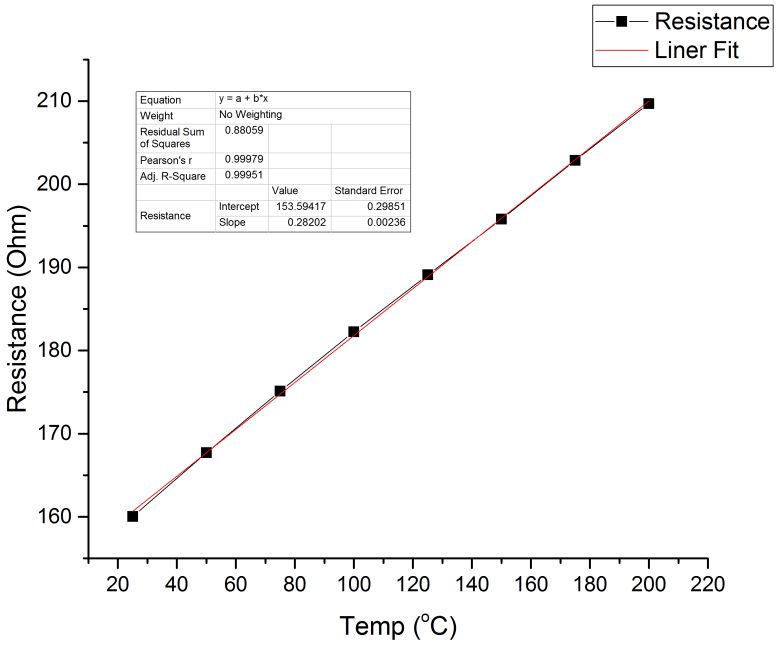

Figure 5.5: Resistance as a function of Temperature

It also showed the temperature up to which a membrane with residual stress can go up to without buckling. A comparative study is shown in Table 5.1. It is found to be in accordance with the simulation predictions made.

5.5. Conclusion

In this chapter, fabrication process flow for new generation of micro-hotplate/nano-reactor was developed. The thermal characterization of the micro-hotplate/nano-reactor was done to extract TCR of the devices. The resistance of the micro-hotplate was found to be increasing linearly with temperature.

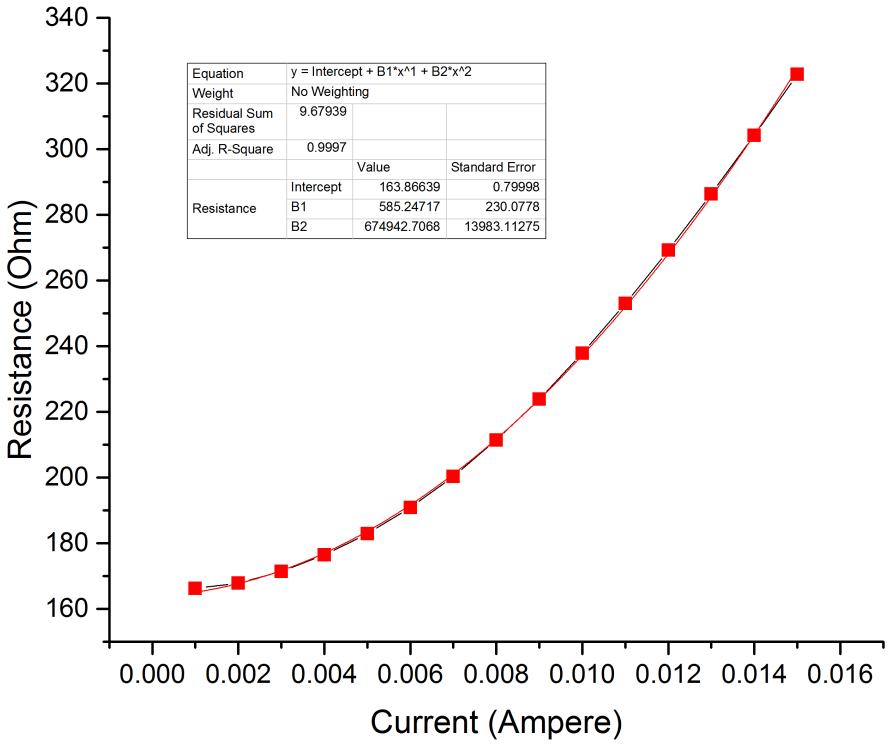

Figure 5.6: Resistance values at various temperature

Table 5.1: Comparison of buckling temperature (Simulation and Experiments)

Stress (MPa)	No buckling temperature-Simulations (^{o}C)	No buckling temperature-Experiments (^{o}C)
230	449.22	-
290	615.89	538.69

Thermal buckling characterization was done to determine the breaking temperature of the devices using optical microscope. For device with 290Mpa, buckling was observed for a current of 15mA corresponding to a temperature of 539^oC. Further experiment for buckling characterization of the devices was done and zero shift in the z-direction was observed up to a temperature of 800^oC in devices having stress values of 350 Mpa.

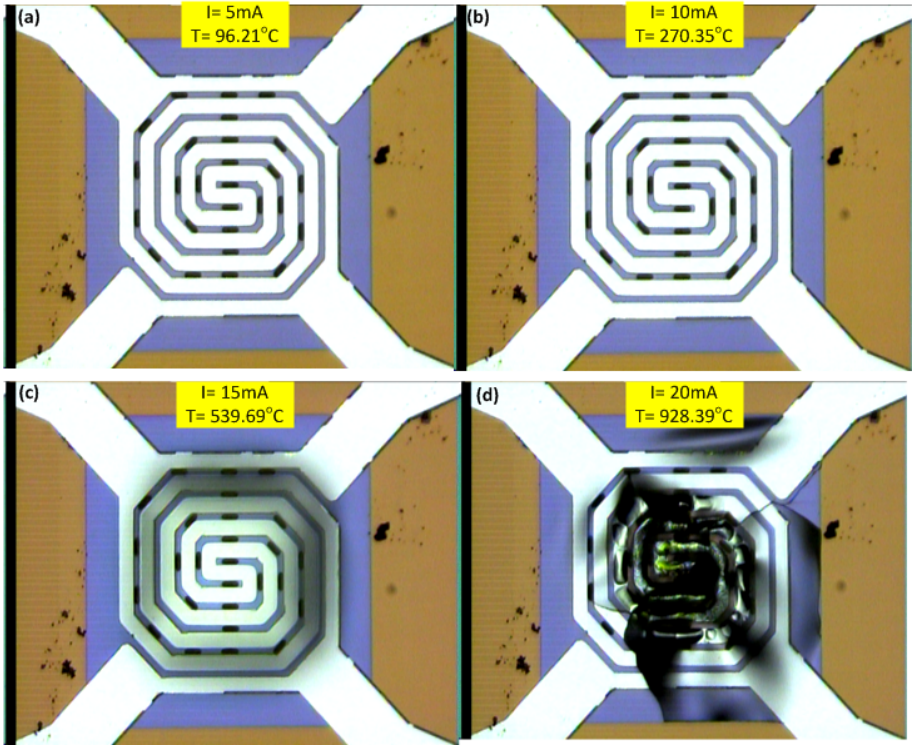

Figure 5.7: Shift in 'z' direction of membrane at (a)T=96.21^{o}C (no shift observed) (b)T=270.35^{o}C (no shift observed)(c)T=539.69^{o}C(shift can be seen in light green)and (d)T=928.39^{o}C (device broken) for stress=290MPa

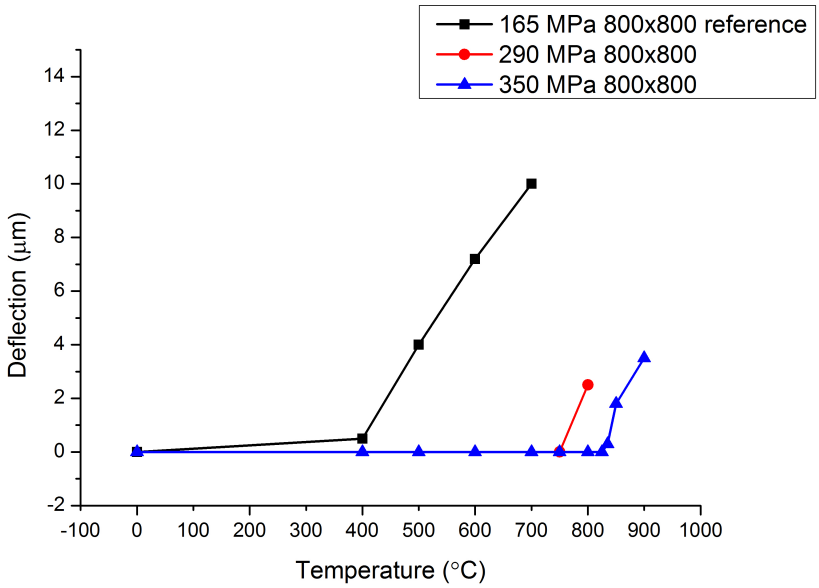

Figure 5.8: The shift in 'z' direction as a function of Temperature

6

Conclusions and Future work

6.1. Introduction

Every work starts with a goal in mind. This thesis started with a goal to reduce the bulging in the LPCVD- SiN_x membrane. Various studies and experiments were done to reach the goals of the thesis. The goals were divides into sub-gals and then the study was done. The conclusion in this chapter deals with reviewing the research goals and the directions taken and the what can be at the end concluded form the work. It is presented in Section 6.2.The research always opens the doors for new things. It will be discussed in the future work in this chapter in Section 6.3. It will be helpful in taking the research forward and providing directions.

6.2. Conclusions from the work

To discuss about the conclusions, let us first review the research objective and a set of goals at the start of the thesis. Each goal is reviewed in the further subsections and the conclusion derived from each goal is discussed. It is also interesting to know how one of these goals led to the formation of other goals and finally led to achievement of the research objective.

Study of causes of bulging and methods to improve them

From the problem definition in Section 1.4, it can be seen that the bulging happens while increasing the temperature. Thus, the obvious option was to suspect physical changes due to Temperature. Thermal stress is one of the major effect that the membrane goes through with change in temperature. It was further studied to find out that compressive stress is one of the major causes for the buckling in the membrane. Thus it became really interesting to find out whether it's the main cause of the of the bulging in our case. Thus, the next goal was to study the stress in the layers.

Stress in Thin films

To prove the hypothesis that tackling compressive stress or making the membranes more tensile can be a solution, simulations were done using COMSOL. A shift in 'z' direction both due to thermal buckling and pressure bulging was found to be reduced with an increase in residual tensile stress. The combined effect of both temperature and presssure was also studied. It gave two interesting conclusions: a) The bulge due to pressure can't be reduced to zero. If there is pressure, there will be bulging. b) At low pressure thermal buckling is the dominant phenomena and at higher pressure, the pressure bulging dominates.

It was very important to know about the layers that is getting deposited. So, the deposition method itself was studied in detail. As it was found that introduction of residual tensile stress may solve the the shift in 'z' direction problem. The fabrication parameters were analyzed to make the layer more tensile. The stress was characterized and the increase in Residual tensile stress was found. As the stress was formed by changing the gas ratio, it was expected to change the composition of Silicon Nitride and thus it became extremely important to characterize the LPCVD-SiN_x to know its basic material properties. It also helped us to check the reliability of the membrane. Structures(rotating pointers) were fabricated

to characterize the young's modulus. AFM, optical characterization and FTIR was done to analyze if the other properties like roughness, grain size, optical constants and composition in the layer. After, all this analysis it was concluded that with varying the deposition parameters the properties of the layer can be changed with varying residual stress in the membrane. It was expected to fabricate membranes and find out the real scenario and effects of increase in stress. Thus a new goal was formulated to study and fabricate the membrane of the device and develop techniques to see bulging and to check reliability of the membranes.

Bulging in thin films membranes

Bulging of LPCVD-SiN_x was important to check the reliability of the membrane in practical working condition of the device. At the same time, the another goal of the thesis was to find a way to do the wafer level bulge testing of the various devices at a time. Thus, a new device concept was needed. This was developed and fabricated. The membranes fabricated were tested using this method and the results were found good enough when compared with simulations. Some of the important conclusions here:

- The pressure bulging was reduced with increase in residual tensile stress , but the reduction is not much at higher pressure. Also the bulging is never zero.
- Only pressure bulging was tested at wafer level as heaters were not fabricated on the membrane and this is the source of heat production

So, with these conclusions, a new goal was formulated towards the research objective. The micro-heaters were integrated on top of the membrane. The micro-heaters were heated to reach various temperature values and the bulging was intuitively characterized at EKL, TU Delft as well as with the help of full characterization setup at DENSolutions B.V., Delft. The results were good and operating range for nano-reactors were increased by almost 400^{o}C and the new temperature was found to be 840^{o}C without any thermal buckling in the membrane.

Overall Conclusions

This thesis concludes three major overall conclusions from the work:

- The tensile stress can be induced in the membranes by changing the gas ratio. The change in ratio only works till a particular limit of tensile stress and then it saturates. It is expected that it changes the properties of the membrane.
- The bulging reduces with respect to pressure by the increase in residual tensile stress but at higher stress values it just saturates.
- The bulging reduces greatly with the introduction of tensile stress in the membrane. It helps to increase the operating range of nano-reactors from 400C to 840C

6.3. Future scope of work

One research always open the doors for the new ones. Thus, it is very important to improve. This thesis gives a lot of scope for the future work. Some of the future work are suggested here.

- The stress in the membranes has only been increased with the help of varying gas ratio. The effect to temperature and pressure on the stress in the layer still needs to be studied.
- The simulations used in this thesis are mostly 2D to mimic the 3D devices. It will interesting to make 3D models and compare the relative error with The 3D model.
- The wafer level pressure testing device works fine but needs a lot of improvement.
  - The uniformity of pressure distribution needs to be checked. Any method to confirm this will be a great improvement.
  - The test bed checks pressure at only one point. Multiple points checking will be better and will give a better idea of the inlet pressure at various points.

  - It can be observed that in this thesis broken membrane were blocked by using Kapton tape. The breaking of one membrane during testing can lead to failure of the testing device. Thus a method to block the membrane while testing can be really useful. Implementation of a valve, which closes on the pressure difference can be a potential solution.

- The membrane has been tested up to a stress of 720Mpa. The stress in the wafer can still be increased and reliability has to be check. The membrane works quite well this stress but the limit is still not known.
- The nano-reactors fabricated towards the end have SiN_x membrane with residual tensile stress of 230MPa , 290 Mpa and 350Mpa. The higher stress membranes should be used to fabricate the nano-reactor and find if it further improves the the shift in 'z' direction in any sense. It will be also a good check for the reliability of membrane in fabrication.
- The present test setup for characterization of bulging doesn't combine the effect of temperature and pressure together. A test setup where both can be implemented together will complete the full product cycle from manufacturing to quality check of the device.

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A

Structure of Young's Modulus Measurements Flowchart for SiN_x

Alignment Markers

1. Measure the wafer bow for the stress test.

2. Coating

   Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

   - A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
   - Spin coating of Shipley SPR3012 positive resist, dispensed by a pump. The approximate spinspeed is 3450 rpm.
   - A Soft Bake (SB) at 95 ^{o}C for 90 seconds

   Always check the relative humidity (48 $\pm$ 2 %) in the room before coating, and follow the instructions for this equipment. Use program '1-Co - 3012 – zerolayer'.

3. Alignment and exposure

   Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine. Expose mask COMURK, with job 'Litho/ZEFWAM' and the correct exposure energy (120 mJ or check the energy list).

4. Wafer numbering

   Use quartz pen to number the wafers on the photoresist layer

5. Developing

   Use the developer station of the EVG120 system to develop the wafers. The process consists of:

   - A post-exposure bake at 115 ^{o}C for 90 seconds.
   - Developing with Shipley MF322 with a single puddle process.
   - A hard bake at 100 ^{o}C for 90 seconds.
     Always follow the instructions for this equipment. Use program 'Dev - SP'.

6. Inspection: Line width and overlay

   Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

7. Plasma etching: Alignment markers

   Use the Trikon Ωmega 201 plasma etcher. Follow the operating instructions from the manual when using this machine. It is not allowed to change the process conditions and times from the etch recipe. Use sequence urk_ npd (with a platen temperature of 20^{o}C) to etch alignment markers into the Si.

8. Photoresist stripping

   Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier. Use program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

9. CLEANING: HNO3 99% and 69.5%

   - **Clean** : 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO3 99% (Si)' and the carrier with the red dot.
   - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
   - **Clean** : 10 minutes in concentrated Nitric acid at 110 ^{o}C. This will dissolve metal particles. Use wet bench 'HNO3 69,5% 110^{o}C (Si)' and the carrier with the red dot.
   - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
   - **Dry** : Use the Avenger Ultra pure-6 'rinser/dryer' with the standard program, and the white carrier with a red dot.

Sin Membrane - Process on front side

1. LPCVD DEPOSITION: 400 nm low-stress Silicon nitride

   Furnace tube : E2 **Program name** : 4INCHVAR (waits for operator)

   Follow the instructions for the LPCVD furnace when using this equipment.

Gasses & flows	Pressure	Temperature	Time
SiH_2Cl_2 / NH_3 = 280 / 120sccm	150mTorr	846^{o}C	44'30"
SiH_2Cl_2 / NH_3 = 240 / 160sccm	150mTorr	846^{o}C	39'18"
SiH_2Cl_2 / NH_3 = 180 / 220sccm	150mTorr	846^{o}C	38'30"
SiH_2Cl_2 / NH_3 = 140 / 260sccm	150mTorr	846^{o}C	39'42"

   Note:

   - The layer thickness depends on the deposition time, which can be calculated from the average deposition rate during recent furnace usage.
   - An extra test wafer (for etch deposition parameter) can be deposited for stress / thickness measurement and etch tests.

2. Measurement: Silicon nitride thickness

   Use the WOOLAM measurement system for layer thickness measurements. Follow the operating instructions from the manual when using this equipment.

   Program : Lowsteress-LPCVD

   Nitride thickness : 400 $\pm$ 40 nm on a bare silicon wafer.

3. Removal of back side Nitride (On one wafer)

   - Use Alcatel plasma etcher
   - Follow the operation instructions from the manual.
   - The etch rate is about 77 nm/min (not accurate, especially for small holes).
   - Use the SiN test wafer to test the etch rate.

4. Measurement: Stress bending of the test wafers

   Measure the final bending of the stress test wafers on the stress meter. This is the residual stress in the wafer.

Structures - Process on frontside

1. Sputter Aluminium

   Thickness : 50nm

   Tool : Sigma

   Temp : The nearest available during deposition

2. Coating

   Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

   - A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
   - Spin coating of Shipley SPR3012 positive resist, dispensed by a pump. The approximate spin speed is 3450 rpm.
   - A Soft Bake (SB) at 95 ^{o}C for 90 seconds.

   Always check the relative humidity (48 $\pm$ 2 %) in the room before coating, and follow the instructions for this equipment. Use program '1-Co – 3027- 1.4um'.

3. Alignment and exposure

   Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine. Expose mask MEMS TRAINING (DIE 8), with job die6x6\9IMG (and the correct exposure energy (150 mJ or check the energy list).

4. Developing

   Use the developer station of the EVG120 system to develop the wafers. The process consists of:

   - A post-exposure bake at 115 ^{o}C for 90 seconds.
   - Developing with Shipley MF322 with a single puddle process.
   - A hard bake at 100 ^{o}C for 90 seconds.

   Always follow the instructions for this equipment. Use program 'Dev - SP'.

5. Inspection : Linewidth and overlay

   Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

6. Extra bake

   Oven, Polymer lab. 30 mins @ 130oC

7. Aluminium Etching

   HF 0.55 % around 40 secs. Transfer it immediately to water bath.

8. Inspection : Linewidth and overlay

   Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

9. Photoresist stripping

   Strip resist Acetone 1 min @ 40^{o}C + cleaning (metal)

10. Cleaning: HNO3 99% and 69.5%

    - **Clean** : 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO3 99% (Si)' and the carrier with the red dot.
    - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
    - **Clean** : 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use wet bench 'HNO3 69,5% 110C (Si)' and the carrier with the red dot.
    - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
    - **Dry** : Use the Avenger Ultra pure-6 'rinser/dryer' with the standard program, and the white carrier with a red dot.

11. Coating Use the POLO manual coater station to coat the wafers with photoresist. The process consists of:

    - A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas, 10 min.
    - Spin coating of Shipley SPR3012 positive resist. Use program in folder 'Nlof2020' for thickness = 3.5um.
    - a Soft Bake (SB) at 95 ^{o}C for 90 seconds.

    Always check the relative humidity (48 $\pm$ 2 %) in the room before coating, and follow the instructions for this equipment. Use program '1-Co – 3027- 2.1 um'.

12. Alignment and exposure

    Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine. Expose mask 'MEMS TRAINING', with job 'DIE6X6' (ID 7) and the correct exposure energy (280 mJ or check the energy list).

13. Developing Use the developer station of the EVG120 system to develop the wafers. The process consists of:

    - A post-exposure bake at 115 ^{o}C for 90 seconds.
    - developing with Shipley MF322 with a single puddle process.
    - A hard bake at 100 ^{o}C for 90 seconds.

    Always follow the instructions for this equipment. Use program 'Dev - SP'.

14. Inspection: Linewidth and overlay

    Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

15. Etching

    In Drytek, STDSIN, land into bulk Si, over-etch is allowed.

16. Adxien

    For isotropic silicon etching to release (dry) your structure.

    time: for rotating structures 1 min. for cantilever 3 mins.

17. Photoresist stripping

    Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use program 1: 1000 watts power and automatic endpoint detection + 2 min. over etching.

B

High Pressure Channel Test Holder

1. Marker Oxidation (Wet oxidation)
   Furnace: D1 or C1
   Time: 00:08:40
   Recipe: MARKOXB

Process	Temperature [^{o}C]	Gases & Flows [Litre/min]	Time [min]	Remarks
Boat in	800	N : 3.0 O : 0.3	5	
Stabilize	800	N: 3.0 O: 0.3	10	
Heat up	+10 ^{o}C/min	N : 3.0 O: 0.3	30	
Stabilize	1100	N : 3.0 O : 0.3	10	
Oxidation	1100	N : 2.25 O : 3.85	38.5	
Cool down	-5 ^{o}C/min	N : 3.0	100	Wait for operator
Boat out	600	N : 3.0	5	

2. Measurement of oxide thickness : Use the Leitz MPV-SP measurement system to measure the oxide thickness:
   Program: Th. SiO2 on Si, >50nm auto5pts
3. Coating
   Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
   - A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas.
   - Spin coating of Shipley SPR3012 positive resist, dispensed by a pump. The approximate spin speed is 3450 rpm.
   - A Soft Bake (SB) at 95 ^{o}C for 90 seconds.

   Always check the relative humidity (48 pm 2 %) in the room before coating, and follow the instructions for this equipment. Use program '1-Co - 3012 – zero layer'.

4. Alignment and exposure

   Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine. Expose mask COMURK, with job 'Litho/FWAM' and the correct exposure energy (120 mJ or check the energy list).

5. Developing

   Use the developer station of the EVG120 system to develop the wafers. The process consists of:

   - A post-exposure bake at 115 ^{o}C for 90 seconds.
   - Developing with Shipley MF322 with a single puddle process.
   - A hard bake at 100 ^{o}C for 90 seconds.

   Always follow the instructions for this equipmentUe program 'Dev - SP'.

6. Inspection: Linewidth and overlay

   write wafer numbers on your logbook indicating DR1, DR2,DR3,DR4,DR5 and DR6. Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

7. Extra bake- 30' @130^{o}C -measurant

8. Window etching: BHF (1:7)

   - **Moisten** : Rinse for 1 minute in wet bench 'H_2O/TRITON X-100' and use the carrier with the blue dot. The bath contains 1 ml Triton X-100 per 5000 ml demi water.
   - **Etching** : Use wet bench 'SiO2-ets (1:7)' at ambient temperature, and the carrier with the blue dot. The bath contains a buffered HF solution (Merck LSI selectipur, SiO2 1:7).
   - **Etch time** : Depends on the layer thickness and composition. Etch until the backside of the wafer(s) is hydrophobic, plus an extra 30 seconds. The etch rate of thermally grown oxide is 1.3 $\pm$ 0.2 nm/s at 20 ^{o}C.
   - **QDR** : Rinse in the Quick Dump Rinser with the standard program until the resistivety is 5 MΩ.
   - **Drying** : Use the Semitool 'rinser/dryer' with the standard program, and the orange carrier with a red dot.
   - **Inspection** : Visually, through a microscope. All the windows must be open and the hydrophobic test may be applied.

9. Photoresist stripping

   Strip resist Acetone 1 min @ 40^{o}C

10. Cleaning: HNO3 99% and 69.5%

    - **Clean** : 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO3 99% (Si)' and the carrier with the red dot.
    - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
    - **Clean** : 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use wet bench 'HNO3 69,5% 110C (Si)' and the carrier with the red dot.
    - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
    - **Dry** : Use the Avenger Ultra pure-6 'rinser/dryer' with the standard program, and the white carrier with a red dot.

Process	Temperature [^{o}C]	Gases & Flows [Litre/min]	Time [min]	Remarks
Boat in	800	N : 3.0 O : 0.3	5	
Stabilize	800	N: 3.0 O: 0.3	10	
Heat up	+10 ^{o}C/min	N : 3.0 O: 0.3	30	
Stabilize	1100	N : 3.0 O : 0.3	10	
Oxidation	1100	N : 2.25 O : 3.85	38.5	
Cool down	-5 ^{o}C/min	N : 3.0	100	Wait for operator
Boat out	600	N : 3.0	5	

11. Thermal Oxidation (Wet Oxidation)

    Furnace : D1 or C1

    Time: 00:08:40

    Recipe: MARKOXB

12. Measurement : Oxide thickness

    Use the Leitz MPV-SP measurement system to measure the oxide thickness:

    Program: Th. SiO2 on Si, >50nm auto5pts

    Oxide thickness: 700-730 nm after 2 marker oxidation steps

Patterning SiO2- Process on both sides

1. Coating (front side)

   Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

   - A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas, 10 min.
   - Spin coating of Shipley SPR3012 positive resist. Use program in folder 'Nlof2020' for thickness = 3.5um.
   - a Soft Bake (SB) at 95 ^{o}C for 90 seconds.

   Always check the relative humidity (48 $\pm$ 2 %) in the room before coating, and follow the instructions for this equipment.

   Front side of wafer DR1,DR2,DR3

   Front side of wafer DR4,DR5,DR6

   Recipe: 1-co-3012-1.4um

2. Alignment and exposure Processing will be performed on the EVG420 contact aligner Follow the operating instructions from the manual when using this machine.

   Mask top wafer (DR1,DR2,DR3) front side: Top-wafer channel

   Mask bottom wafer(DR4,DR5,DR6) front side: Bottom wafer channel

   Exposure time 30 sec

3. Developing

   Front side of the first wafer

   Front side of the second wafer

   Use the developer station of the EVG120 system to develop the wafers. The process consists of:

   - A post-exposure bake at 115 ^{o}C for 90 seconds.
   - developing with Shipley MF322 with a single puddle process.
   - A hard bake at 100 ^{o}C for 90 seconds.

   Always follow the instructions for this equipment. Use program 'Dev - SP'.

4. Inspection : Line width and overlay

   Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

5. Plasma etching: (oxide – 700nm) (until si)

   Use Dry tek to etch oxide first

   Recipe : STDOXIDE

   Time : 01:30 min

6. Photoresist stripping

   Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use program 1: 1000 watts power and automatic endpoint detection + 2 min. over etching.

   Cleaning: HNO3 99% and 69.5%

   - **Clean** : 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO3 99% (Si)' and the carrier with the red dot.
   - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
   - **Clean** : 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use wet bench 'HNO3 69,5% 110C (Si)' and the carrier with the red dot.
   - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
   - **Dry** : Use the Avenger Ultra pure-6 "rinser/dryer" with the standard program, and the white carrier with a red dot.

7. Coating (back side)

   Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

   - A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas, 10 min.
   - Spin coating of Shipley SPR3012 positive resist. Use program in folder 'Nlof2020' for thickness = 3.5um.
   - a Soft Bake (SB) at 95 ^{o}C for 90 seconds.

   Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment. Back side for Wafer DR1, DR2, DR3, DR4, DR5, DR6

   Recipe: 1-co-3012-1.4um

8. Alignment and exposure

   Contact aligner front side alignment on the zero layer

   Mask top wafer (DR1,DR2,DR3) back side: Topwafer- holes

   Mask bottom wafer (DR4, DR5,DR6) back side: Bottom Wafer- holes

   Exposure time 30 sec

9. Developing

   Wafers DR1, DR2, DR3, DR4 , DR5 and DR6

   Use the developer station of the EVG120 system to develop the wafers. The process consists of:

   - A post-exposure bake at 115 ^{o}C for 90 seconds.
   - developing with Shipley MF322 with a single puddle process.
   - A hard bake at 100 ^{o}C for 90 seconds.

   Always follow the instructions for this equipment. Use program 'Dev - SP'.

10. Inspection: Linewidth and overlay

    Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

11. Plasma etching : (oxide – 500nm) (until Si)

    Use Dry tek to etch oxide first

    Recipe : STDOXIDE

    Time : 01:00 min

12. Plasma flash : Photoresist Removal

    Use Telpla system, program 1

13. Cleaning (Si)

    - **Clean** : 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO3 99% (Si)' and the carrier with the red dot.
    - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
    - **Clean** : 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use wet bench 'HNO3 69,5% 110C (Si)' and the carrier with the red dot.
    - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
    - **Dry** : Use the Avenger Ultra pure-6 'rinser/dryer' with the standard program, and the white carrier with a red dot.

14. Native oxide etch

    Dip Etch in 0.55 HF @ 4 mins.

15. TMAOH Etching : SAL

    TMAOH in SAL lab

    Rinse and Dry

16. Cleaning in SAL (silicon cleaning)

    - **Clean** : 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO3 99% (Si)' and the carrier with the red dot.
    - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

- **Clean** : 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use wet bench 'HNO3 69,5% 110C (Si)' and the carrier with the red dot.
- **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
- **Dry** : Use the Avenger Ultra pure-6 "rinser/dryer" with the standard program, and the white carrier with a red dot.

17. Etching: BHF (1:7)

- **Moisten** : Rinse for 1 minute in wet bench 'H_2O/TRITON X-100' and use the carrier with the blue dot. The bath contains 1 ml Triton X-100 per 5000 ml demi water.
- **Etching** : Use wet bench 'SiO2-ets (1:7)' at ambient temperature, and the carrier with the blue dot. The bath contains a buffered HF solution (Merck LSI selectipur, SiO2 1:7).
- **Etch time** : Depends on the layer thickness and composition. Etch until the backside of the wafer(s) is hydrophobic, plus an extra 30 seconds. The etch rate of thermally grown oxide is 1.3 $\pm$ 0.2 nm/s at 20 ^{o}C.
- **QDR** : Rinse in the Quick Dump Rinser with the standard program until the resistivety is 5 MΩ.
- **Drying** : Use the Semitool "rinser/dryer" with the standard program, and the orange carrier with a red dot.
- **Inspection** : Visually, through a microscope. All the windows must be open and the hydrophobic test may be applied.

18. Cleaning procedure : RCA 1 (H2O2:NH4OH:H2O=1:1:5 @ 75 ^{o}C) + Marangoni Drying

- **Clean** : Rinse the quartz RCA1 beaker with DI water and place it on a hot plate.
  Rinse the thermocouple connected to the temperature controller with DI water and place it in the RCA1 beaker. Slowly pour the measured amount of chemicals into the beaker:
  - 2500 ml DI water
  - 500 ml NH4OH
  - Use the 1000ml and 500ml graduated cylinders

  Make sure that the mouth of the bottle does not make contact with the graduated cylinder in order to prevent contamination. Never pour back chemicals into the bottle.
  Clean the graduated cylinder with water.
  Turn the temperature controller on the hot plate and set the temperature to 75 ^{o}C.
  When the temperature reaches 65 ^{o}C, add 500ml of H2O2.
  In the meantime put the wafers in the proper carrier (green/blue dots).
  When the temperature reaches 72 ^{o}C, dip the carrier with the wafers into the beaker, but don't start the timer yet.
  Once it reaches 75 ^{o}C, start the 10 minutes countdown. When the 10 minutes are done, turn off the hot plate and transfer the wafers to the DI water container and start rinsing.
- **Rinse** Rinse in the water bath for 5 minutes and in the meantime start the demi water for the Maragoni dryer. After 3 minutes, turn on the IPA in the Maragoni bath.
- Dry Carefully place the wafers in the maragoni wafer holders and then dip them into the solution for 40 seconds. After that, start taking them out of the bath and because of the IPA they'll come out dry.

19. Layer stripping: Native Oxide + Marangoni Drying (HF 0.5 %)

Etch + Dry Use MARANGONI wet bench located on the Cleaning line. After cleaning the bath with DI water fill the bath with "0.55% HF" (room temperature). Put your wafers in carrier slots and dip them in solution for 4min. Turn the water valve on for a 5min. At the end of the time, one minute before you lift your wafers turn the IPA valve on. Take your dried wafers and turn all valves off.

Reminder :

Read the Marangoni Manuals and follow all instructions.

Use proper Marangoni bath ("Si"- max. 6 wafers or "Metal bath"- max 4 wafers).

Do not forget to turn the 0.55% HF container valve (behind the chemical station) ON before you start filling the bath.

Do not forget to turn all valves OFF after finished the etching/drying step (DI, IPA, 0.55

20. Bonding + Annealing

    Alignment is done on the AML using the bonding holders Silicon direct bonding.

    Use a force of 3000N during 5 minutes in order to bond the wafers. WB1715

C

Testing Structures

Sin Membrane - Process on frontside

1. Measure the wafer bow for stress test
2. LPCVD deposition: 400 nm low-stress Silicon nitride

   Furnace tube : E2 **Program name** : 4INCHVAR (waits for operator)

   Follow the instructions for the LPCVD furnace when using this equipment.

Gasses & flows	Pressure	Temperature	Time
SiH_2Cl_2 / NH_3 = 280 / 120sccm	150mTorr	846^{o}C	44'30"
SiH_2Cl_2 / NH_3 = 240 / 160sccm	150mTorr	846^{o}C	39'18"
SiH_2Cl_2 / NH_3 = 180 / 220sccm	150mTorr	846^{o}C	38'30"
SiH_2Cl_2 / NH_3 = 140 / 260sccm	150mTorr	846^{o}C	39'42"

   Note:

   - The layer thickness depends on the deposition time, which can be calculated from the average deposition rate during recent furnace usage.
   - An extra test wafer (for etch deposition parameter) can be deposited for stress / thickness measurement and etch tests.

3. Measurement: Silicon nitride thickness

   UUse the WOOLAM measurement system for layer thickness measurements. Follow the operating instructions from the manual when using this equipment.

   Program : Lowstress-LPCVD

   Nitride thickness : 400 $\pm$ 40 nm on a bare silicon wafer.

4. Removal of back side Nitride (On one wafer)

   - Use Alcatel plasma etcher
   - Follow the operation instructions from the manual.
   - The etch rate is about 77 nm/min (not accurate, especially for small holes).
   - Use the SiN test wafer to test the etch rate.

5. Measurement: Stress bending of the test wafers

   Measure the final bending of the stress test wafers on the stress meter. This is the residual stress in the wafer.

Structures process on backside

1. Coating

   Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

   - A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas
   - Spin coating of Shipley SPR3012 positive resist, dispensed by a pump. The approximate spin speed is 3450 rpm.
   - A Soft Bake (SB) at 95 ^{o}C for 90 seconds.

   Always check the relative humidity (48 $\pm$ 2 %) in the room before coating, and follow the instructions for this equipment. Use program '1-Co – 3027- 1.4um'.

2. Alignment and exposure

   Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.

   Follow the operating instructions from the manual when using this machine.

   Expose mask DENS-KOH_V7, with job "SPECIAL\GREGORY\g20x21" (and the correct exposure energy (150 mJ or check the energy list).

3. DEVELOPING

   Use the developer station of the EVG120 system to develop the wafers. The process consists of:

   - A post-exposure bake at 115 ^{o}C for 90 seconds.
   - Developing with Shipley MF322 with a single puddle process.
   - A hard bake at 100 ^{o}C for 90 seconds.

   Always follow the instructions for this equipment. Use program 'Dev - SP'.

4. Inspection : Linewidth and overlay

   Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

5. Etching

   Only on process wafers

   In Drytek, STDSIN, land into bulk Si, over-etch is allowed.

6. Inspection: Linewidth and overlay

   Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

7. Photoresist stripping Strip resist Acetone 1 min @ 40^{o}C + cleaning (metal)

8. Cleaning: HNO3 99% and 69.5%

   - **Clean** : 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO3 99% (Si)' and the carrier with the red dot.
   - **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
   - **Clean** : 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use wet bench 'HNO3 69,5% 110C (Si)' and the carrier with the red dot.

- **Rinse** : Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
- **Dry** : Use the Avenger Ultra pure-6 ”rinser/dryer” with the standard program, and the white carrier with a red dot.

D

Pt Micro-Hotplate Flowchart

This flowchart can't be shown completely due to EKL confidentiality.

The main steps in this process are described below

1. Alignment markers
    - Coating of wafers
    - Exposure mask COMURK with litho job ZEFWAM.
    - Wafer numbering
    - Development of the wafers.
    - Plasma etching of Alignment markers.
    - Photo resist stripping
    - Cleaning of the wafers
2. SiN_x Membrane - Process on front side
    - Thermal oxidation
    - Measurement : Thermal oxide thickness
    - Coating and Baking
    - Oxide etch
    - Photo resist Stripping
    - Nitride deposition and thickness measurement.
    - back side etch and stress measurement
    - Measurement: Initial bending of the test wafers
    - LPCVD Deposition: 200 nm low-stress Silicon nitride (WAFERS ARE CONTANMINATED)
    - Measurement - silicon nitride thickness
    - Backside etching
    - Measurement of stress and bending of the test wafers
3. PT Heater - Process on front side
    - Coating of the wafers
    - Alignment and exposure for PT heater
    - Developing of the wafers
    - Plasma flash.

- Evaporation of Ta 20nm /Pt 160nm.
- Photo resist Lift-off
- Pt-annealing and 200nm low-stress silicon nitride deposition
- Measurement of silicon nitride thickness
- Backside etching
- Measurement of stress and bending of the test wafers

4. TEM window process on front side
   - Coating of the wafers
   - Alignment and exposure for TEM window
   - Developing of the wafers
   - Plasma etching of SiN holes.
   - Wet etching of thermal oxide.
   - Cleaning
   - LPCVD deposition of 20nm TEM window
5. KOH window- Process on backside
   - Coating of the wafers
   - Alignment and exposure for KOH window
   - Developing of the wafers
   - Plasma etching of KOH opening.
   - Cleaning
6. Pad opening on front side
   - Coating of the wafers
   - Alignment and exposure for KOH window
   - Developing of the wafers
   - Plasma etching of pad opening.
   - Photo resist stripping
   - Cleaning
7. Membrane release process on backside
   - Cover front side with photo resist
   - KOH etching using contaminated holders
   - Cleaning

E

Plate theory In-line forces and Moments

In-plane

Normal forces

$$N_x = \int_{\frac{-h}{2}}^{\frac{h}{2}} \sigma_{xx}\, dz$$
$$N_y = \int_{\frac{-h}{2}}^{\frac{h}{2}} \sigma_{yy}\, dz \tag{E.1}$$

Bending moments

$$N_x = -\int_{\frac{-h}{2}}^{\frac{h}{2}} z\sigma_{xx}\, dz$$
$$N_y = -\int_{\frac{-h}{2}}^{\frac{h}{2}} z\sigma_{yy}\, dz \tag{E.2}$$

Shear force

$$N_x y = \int_{\frac{-h}{2}}^{\frac{h}{2}} \sigma_{xy}\, dz \tag{E.3}$$

Twisting moment

$$N_x y = \int_{\frac{-h}{2}}^{\frac{h}{2}} z\sigma_{xy}\, dz \tag{E.4}$$

Out-plane

Shearing forces

$$V_x = -\int_{\frac{-h}{2}}^{\frac{h}{2}} \sigma_{zx}\, dz$$
$$V_y = -\int_{\frac{-h}{2}}^{\frac{h}{2}} \sigma_{zy}\, dz \tag{E.5}$$

F

FTIR Spectra

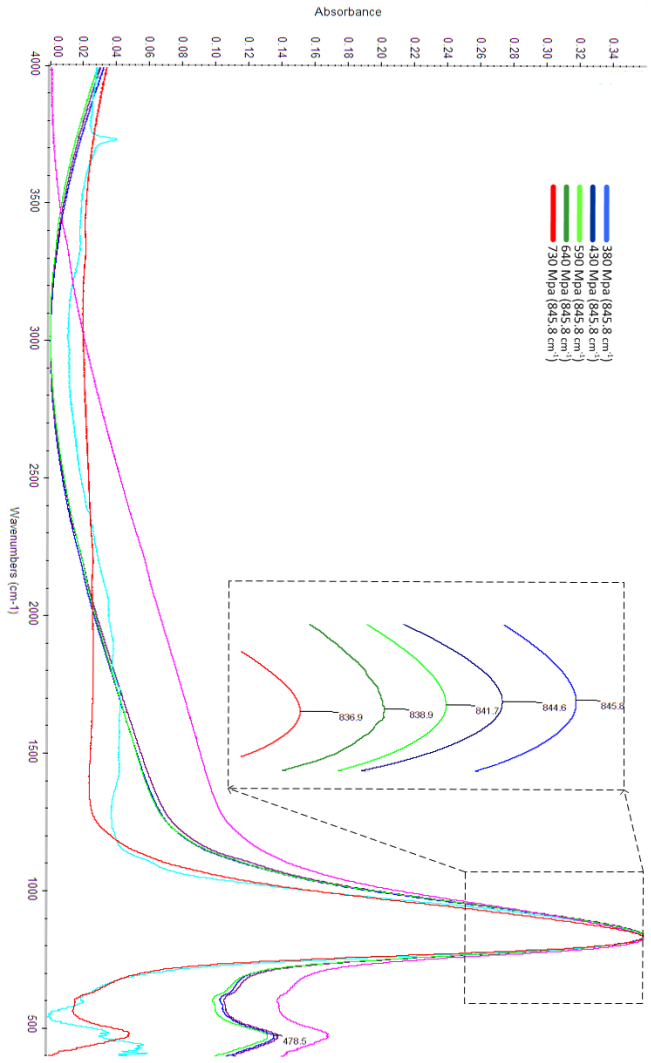

Figure F.1: The FTIR Spectra Of LPCVD SiN_x at various residual tensile stress