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Mm-wave passive components for integrated phased array antennas

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PROEFSCHRIFT

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in het openbaar te verdedigen

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A mio padre, mia madre e mio fratello
(ci sono distanze che separano, ed altre che uniscono)

Contents

List of acronyms

1D	one-dimensional
2D	two-dimensional
3D	three-dimensional
ac	alternating current
Al	aluminum
AR	aspect ratio
ADAS	advanced driver assistance system
ADS	advanced design system
AUT	Antenna Under Test
BFN	beam forming network
CMOS	complementary metal oxide semiconductor
CPW	coplanar waveguide
dc	direct current
DIMES	Delft Institute of Microsystems and nanoelectronics
DRIE	deep reactive-ion-etching
EM	electromagnetic
ERWG	equivalent rectangular waveguide
ESD	electro-static discharge
FFT	Fast Fourier Transform
FMCW	frequency-modulated continuous-wave
FWR	fast wave region
GaAs	gallium arsenide
G-S-G	ground-signal-ground
HFSS	high frequency structural simulator
HPBW	half-power beam-width

HRS	high resistivity silicon
IC	integrated circuit
IF	intermediate frequency
ISM	industrial-scientific-medical
KOH	potassium hydroxide
LNA	low noise amplifier
LPCVD	low pressure chemical vapor deposition
LPF	low pass filter
LTCC	low temperature co-fired ceramics
MEMS	micro-electro-mechanical system
MIMC	metal-insulator-metal
PCB	printed circuit board
PECVD	plasma-enhanced chemical vapor deposition
PA	power amplifier
PEC	perfect electric conductor
PMC	perfect magnetic conductor
PNA	performance network analyzer
RF	radio frequency
RFID	radio frequency identification
Rx	receiver
RWG	rectangular waveguide
SCPW	shielded coplanar waveguide
SIIG	substrate integrated image waveguide
SIW	substrate integrated waveguide
SoG	silicon-on-glass
SSL	side lobe level
TC	Technology Center
TE	transverse electric
TEM	transverse electroMagnetic
TM	Transverse Magnetic
TRL	Thru-Reflect-Line
TTDL	true time delay line
Tx	transmitter
TWG	trapezoidal waveguide

Chapter 1

Introduction

1.1 Introduction

"To sense is the ability to understand or be aware of (something)", as the Merrian-Webster dictionary [1] reports. In order to increase our capability of understanding the environment and be aware of dangers visible or not visible to human eyes, sensing devices are pervading everyday life in commercial, industrial and medical applications.

A sensor is usually defined by the object or element it is trying to sense (distance, pressure, temperature, etc.) and the physical mechanism that the device will employ (mechanical, electrical, optical, etc.) to convert the information in a signal that can be further processed and analyzed. Sensor based on electrical principles (see Fig. 1.1) can be divided by the frequency range they operate in, from (contact) low frequency (e.g., capacitive and inductive), to (remote) medium and high frequencies (e.g., ranging sensors), up to optical frequencies (e.g., passive infra-red detectors).

Electromagnetic sensors (EM) operating at microwave (0.3 to 30 GHz) and millimeter-wave (30 to 300 GHz) frequencies collect the energy transmitted by electromagnetic waves by employing antennas and electrical circuitry capable of conditioning the received signals (i.e., amplifying, filtering and shifting it to lower frequency) and digitizing them to provide as output the measured information. Such sensors provide the ability of penetrating objects which are opaque to light (clothes, cardboard boxes, etc.) when compared to their optical equivalent (imager and radiometer), and have been traditionally employed only in specialized fields such as in military (e.g., radars), space (e.g., radiometers) and life science (e.g., spectroscopes) applications due to their costs and complexity.

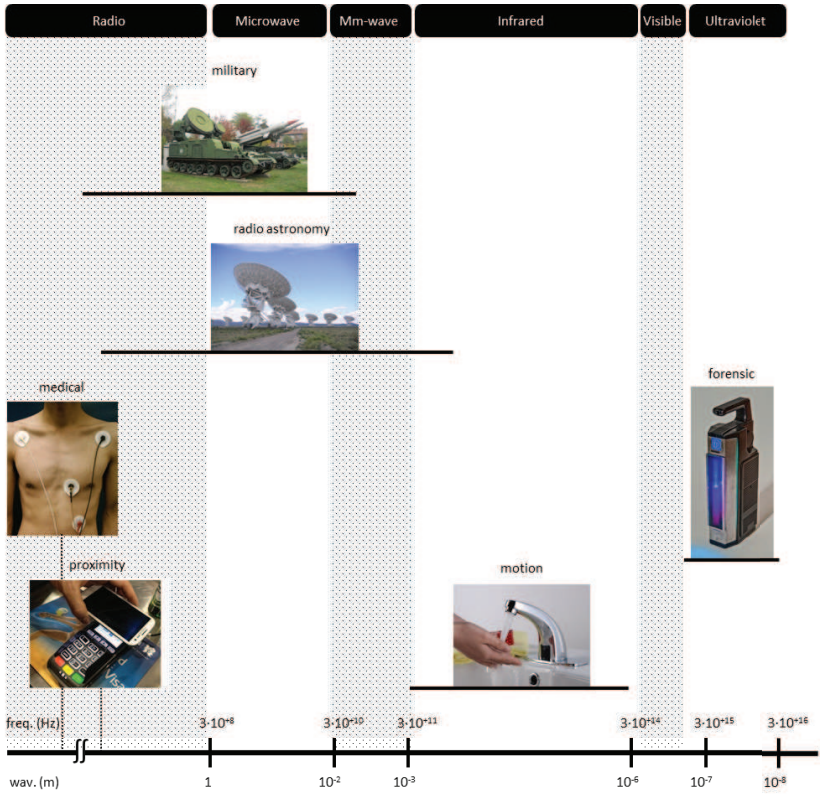


Figure 1.1: Commercial, military and astronomy sensors across the EM spectrum [2–7]; commercial sensors are mostly concentrated at RF, low microwave and infrared frequencies.

Only recently, sensor topologies operating in the mm-wave bands (see Fig. 1.2) are gathering more interest for commercial and industrial applications, as they can take advantage of the acquired maturity of lower cost technologies capable of operating at high frequencies while integrating several functionalities. Commercial examples of such sensors include imaging radars for assisted driving systems (under development), body scanners, and distance sensors for hostile environments (e.g., fog, dust, chemical vapors).

The frequency up-scaling of electromagnetic sensors is favorable for a number of reasons:

- Dimensions: the antenna dimension which is proportional to the

(a)

(b)

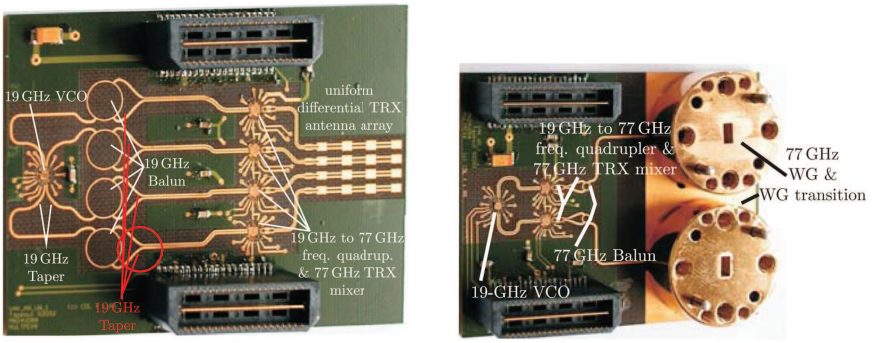
Figure 1.2: Examples of commercial mm-wave systems: (a) automotive radar [8], and (b) body scanner [9].

wavelength, decreases as the frequency increases, allowing for more compact systems.

- Performance: lateral and radial resolutions of the acquired image are in the order of half-a-wavelength (in diffraction limited scenes [10]) and therefore improve as the frequency increases.
- System complexity: simple narrow band circuit designs allow to compensate parasitic elements by using resonance techniques only in a few percent relative bandwidth. As the frequency increases however, the same relative band corresponds to larger absolute band, allowing to transmit, receive and process more information by using simple narrowband circuit design.

Automotive radar systems [12–15], capable of supporting functions such as adaptive cruise control, pre-crash protection and collision warning system, are among the most successful commercial implementation of EM mm-wave sensor. Furthermore, their recent frequency up scaling from 26 to 77 GHz [16] allowed to improve the accuracy in the identification of small radar cross-section objects like pedestrian and bicycles.

In order to operate at such high frequencies, the interfacing of the mm-wave EM sensors to the integrated circuits (i.e., generating and conditioning

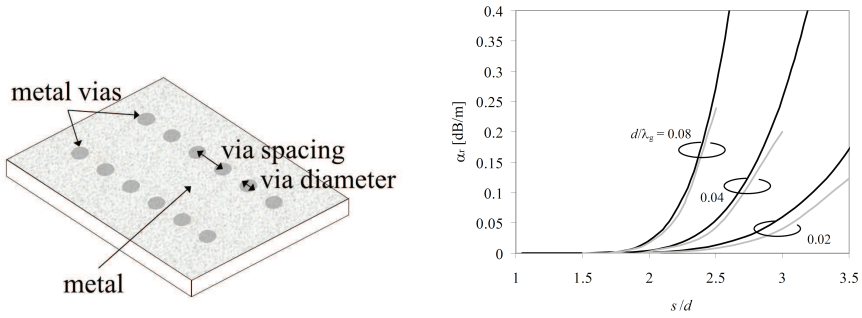


(a) (b)

Figure 1.3: A 77 GHz radar sensor for the automotive industry [11], with (a) differential-patch or (b) bulk waveguide antennas. The active circuits as voltage-controlled oscillator (VCO), frequency multipliers and mixers are connected to the PCB by means of bond wire technology.

the mm-wave signal), the signal routing and its coupling to the air (i.e., via transmitting and receiving antennas) must be optimized and miniaturized at the same time. State of the art systems (see Fig. 1.3 [11]) make use of bond-wire technology to interface with the integrated circuit (IC) environment, transmission lines on printed circuit board (PCB) to distribute the mm-wave signals, resonant planar antennas or more bulky waveguide aperture antennas (when higher gain is required) to radiate the signal. These approaches for interfacing, routing and radiating signals pose major limitations in employing relative bandwidths (i.e., frequency bandwidth divided by center frequency) required for high resolution imaging, thus leaving the bulk solutions (see Fig. 1.3b) as the only current option for broad band interfacing. From a commercial stand point, planar systems that allow compact high-performance and low volume interfaces are required in order to expand the potential of currently existing mm-wave applications as well as to open new ones.

The research presented in this thesis is focused on the realization of broadband interfaces to the IC environment, interconnections and radiating elements, based on silicon integrated waveguides and scalable in the entire mm-wave, for present and future applications. Such components are employed in this work for the design of the passive building blocks of a 3D imaging sensor operating around 94 GHz.



(a) (b)

Figure 1.4: Substrate integrated waveguide: (a) layout [17] and (b) attenuation constant [18] due to radiation leakages (dielectric and metal lossless). The top and bottom faces of a PCB are covered with a layer of metal; after that, metallic vias are punched through the PCB to form the via fenced side walls of the waveguide. In (b), s is the via spacing and d the via diameter.

1.2 Motivation

State-of-the-art EM sensors as the ones presented in the previous section require passive components that pose critical challenges in their interfacing with the IC environment, in the routing of high frequency signal, and in the realization of radiating elements when gains higher than resonant patches on electrically thin substrates are required.

1.2.1 Interface and routing

At mm-waves, on-wafer interconnections based on planar transmission lines, such as microstrip (MS) and coplanar waveguides (CPWs) exhibit poor performances due to the high metal and dielectric losses [19–21]), and achieve a low field confinement [22–24] due to substrate coupling and radiation losses.

Array of metallized vias (in PCB technologies) [25] or floating shields (in integrated technologies) [26] can be employed to improve field confinement and reduce leakage into substrate, but total losses (i.e., conductive, dielectric and radiative) remain higher than 0.5 dB/mm at 50 GHz and 0.7 dB/mm at 100 GHz for a shielded coplanar waveguide (SCPW) topology in the back-end of a CMOS (complementary metallic-oxide-semiconductor) technology, for example.

On the other hand, bulk metallic rectangular waveguides (RWG) work-

ing at 94 GHz are able to guide signals with losses lower than 0.01 dB/mm, (ideally) providing no radiation nor substrate leakage effects [27]) due to the full metal enclosure. Nevertheless, waveguides are three-dimensional components with a bulk profile, thus difficult to interface with planar IC.

In order to transfer the benefits of waveguide technology to a planar environment, several solutions have been proposed over the years for the realization of waveguides on a PCB [28–33] or directly in a wafer environment [34–37]. Among them, substrate integrated waveguides (SIW) [17], manufactured by punching metallic vias through a printed circuit board (see Fig. 1.4a [17]) have gained large popularity pushing toward a higher level of system co-integration [38, 39]. Although well demonstrated at low mm-waves, (insertion losses of 0.2 dB/mm at 30 GHz [40]), their frequency up-scaling seems to be difficult to achieve due to the (limited) resolution of the fabrication process. As an example, the minimum feature size on PCB processing is in the order of 75 μm [41], and typical values for the via spacing (see Fig. 1.4a) are in the order of 200 μm. To place these number in the component prospective, it must be mentioned that to avoid radiation leakages, the metallic vias should be spaced closer than one tenth of the guided wavelength λ_g [41, 42], resulting in a distance smaller than 150 μm for 100 GHz operation (d/λ_g=0.04 at 100 GHz, and s/d<2, see Fig. 1.4b) [18], which is not achievable with the current PCB technology. Moreover, the reduced resolution of the fabrication technology reduces the capability to design and integrate more complex structures capable of achieving broadband operation.

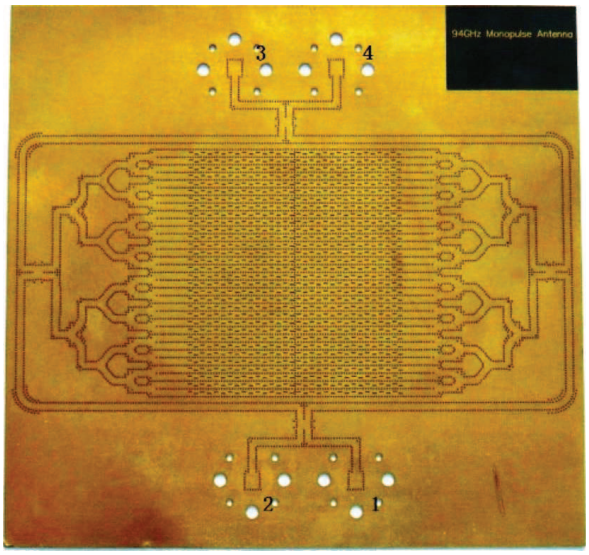
All these considerations highlight the need to investigate improvements that can be achieved at component level for transition to the IC environment (this thesis, chapter 4), waveguide section and antennas (this thesis, chapters 5 and 6)

1.2.2 Radiating elements

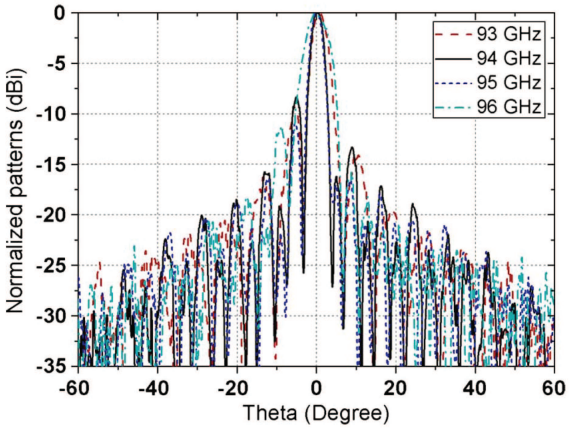
In order to increase the gain of the radiating elements in respect to that of resonant patches fabricated on electrically thin substrates, dielectric lenses [44, 45] or (planar) array configurations [46, 47] can be used.

In the first case, a dielectric lens is physically mounted on top of a planar antenna [48, 49], requiring extra assembly operations and reducing the electronically steering capability of the radiated beam. In simple antenna array topologies instead, the radiation of several (identical) antennas is combined coherently, increasing the gain of the array which is, in first approximation, increased proportionally to the number of element employed [50, 51].

At mm-wave frequencies, the use of patch antennas as radiating element



(a)



(b)

Figure 1.5: Substrate integrated waveguide bidimensional array in W band [43]: (a) layout and (b) radiation pattern in the H plane (i.e., xz cut plane). The power radiated by each waveguide slot in (a) follows a Taylor distribution; at the design center frequency (i.e., 94 GHz), the first side lobe in (b) is just -8 dB below the main lobe.

in array topologies has been successfully demonstrated at 77 GHz [52, 53], for instance in automotive applications, and is currently under investigation at 120 GHz [54,55]. The up-scaling beyond these frequencies is however hindered by the excitation of surface waves in the antenna substrate [23], which becomes electrically thick and acts as a dielectric slab, trapping and guiding rather than radiating the energy emitted by the patch. To mitigate this effect, substrates with a reduced thickness (i.e., silicon back end or air membranes [56]) and/or with a low dielectric constant [57] can be used, but such designs are expensive in area (ground plane usually at least twice the patch size) and only allow the design of narrow band antennas (the electrically thinner the substrate, the smaller the antenna matching bandwidth [51]). Dipole antennas offers a more compact topology, but achieve lower efficiencies because their omnidirectional radiation pattern causes a large fraction of power to be lost in the lossy substrate

Substrate integrated waveguide technology has been proposed as a viable option for the realization of radiating elements, providing mm-wave antennas (see Fig. 1.5a [43]) which do not suffer from surface waves nor requires air membranes and are capable of achieving a large operational bandwidth. Nevertheless, no technique to reduce the amplitude of radiation side lobes in high-gain SIW antennas has been effectively employed at mm-waves due to the previously mentioned limitation of PCB technology (see Fig. 1.5b [43]).

The possibility of employing a high resolution fabrication technology (this thesis, chapter 3) provides the platform to investigate, design and optimize antenna arrays with low side lobe generation and operating over a large relative bandwidth (this thesis, chapter 5).

1.3 Design challenges and objectives

The thesis work is focused on the realization of a technology platform for radar systems in the millimeter-wave range: as demonstrator, a 94 GHz phased array antenna for a bistatic radar system on silicon is considered. This requires the design and optimization of frequency scalable low-loss long interconnections and on-wafer passive components with reduced size, weight and cost, capable of addressing commercially viable and potentially large applications at deep mm-wave.

While relying on technologies that allow IC-compatible steps (for large volume fabrication) and standard assembly (i.e., bond-wiring and flip-chip), the targeted components need to provide high performance and low losses for the realization of:

- FMCW radar sensors in silicon technology operating at mm-waves
- Frequency scanning arrays in waveguide with high gain and beam steering capability.
- Low-loss mm-wave transmission lines and components based on silicon integrated waveguides.
- Ultra wideband transitions for interfacing with the active ICs.

Note that due to limitations in the measurement setup avaiaible at the university, frequencies higher than 130 GHz could not be targeted. Nonetheless, as the proposed platform relies on integrated waveguides, the frequency up-scaling of the passive components only requires a down-scaling of their gemoetrical dimensions, easy to realize in a manufacturing process based on photo-lithography.

1.3.1 94 GHz FMCW radar demonstrator

The hardware complexity of antenna arrays depends on the number of feed lines and variable element delays. As example, an NxN array with independent phase control at each antenna element is shown in Fig. 1.6a.

To support lower complexity/cost applications capable of realizing imaging sensor, frequency scanning arrays [58–60] are investigated and implemented in this thesis work as radiating element of a highly integrated radar sensor. To reduce the phase control elements from N^2 to N, the antenna topology of Fig. 1.6b is also considered: a linear array (along rows, N) of frequency scanning arrays (along columns, M). Beam steering in the vertical direction is achieved by means of N phase shifters, while in the horizontal direction by means of frequency scanning, as explained in section 1.3.2.

1.3.2 Frequency scanning array

The frequency scanning arrays of Fig. 1.3.2 are implemented using the silicon integrated waveguide technology, and allow to perform one-dimensional electronic beam steering [58], without the need of phase shifters (see Fig. 1.7a). For a wave travelling along the waveguide in Fig. 1.7b, the progressive phase of the signal feeding the array elements is equal to the physical distance between the radiators times the (frequency dependent) phase constant β=w/v of the wave. As the frequency changes, the electrical distance between two consecutive radiators varies, and 1D electrical scanning with frequency is achieved.

The determination of optimum element spacing and geometrical dimensions to achieve maximum beam steering within the smallest frequency

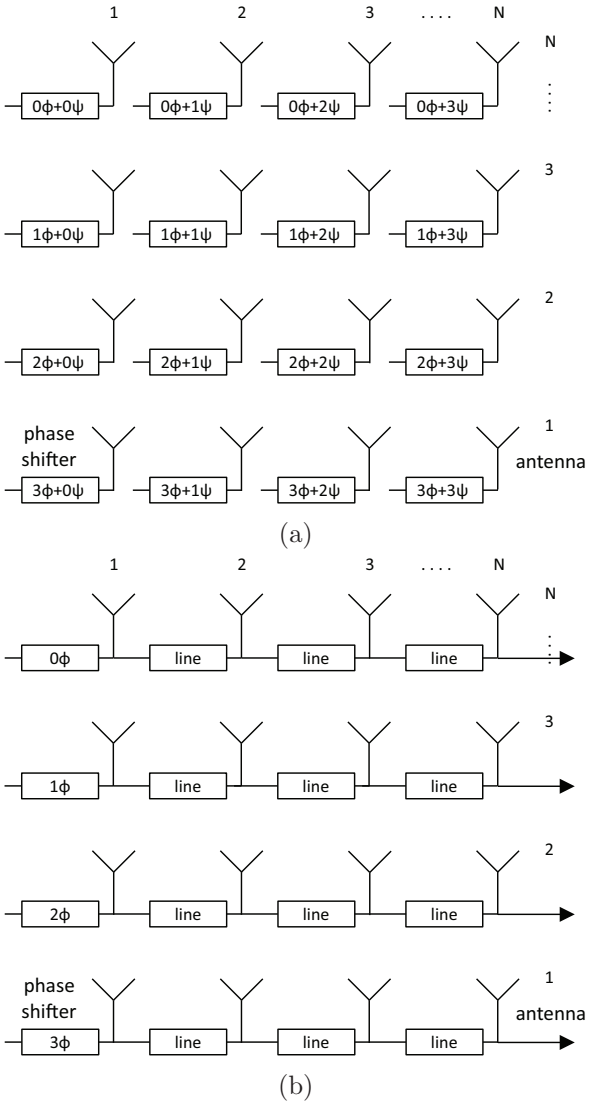


Figure 1.6: High-gain antenna based on a: (a) square (NxN) phased array antenna or (b) linear array (along columns, N) of frequency scanning arrays (along rows, M); a progressive phase excitation scheme along the columns is reported as example. In (b), beam steering is achieved with frequency control along the rows and with phase control along the columns.

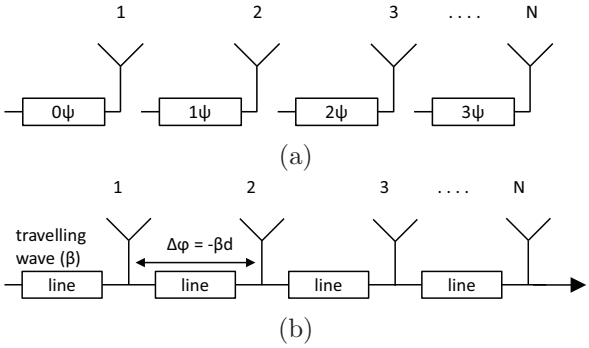


Figure 1.7: Working principle of: a (a) phased and (b) a linear frequency scanning array. In (b), a wave with phase constant β propagates along a linear array of radiators spaced at uniform distance d: each radiator is thus excited by a signal with a phase delay with respect to the previous element $\Delta\phi$=-β d=-wd/v, v being the phase velocity, which depends by the frequency.

bandwidth are set as design objectives. The excitation of higher order modes or radiation from multiple spatial harmonics [59, 60], which would spread the radiated power on secondary lobes and reduce the total gain of the array antenna, is avoided by developing a structured analytical design flow (this thesis, chapter 5).

1.3.3 Silicon integrated waveguide

The frequency scaling of SIW in the whole mm-wave band requires structures with continuous metallic side walls rather than discrete arrays of vias. This thesis work targets the realization of waveguides in the mm-wave frequency range with continuous metallic side walls, on high resistivity silicon substrates, with IC-compatible steps and with easy interface to planar circuit. As the continuous metallization walls drastically reduces radiation leakages, the design of waveguide components as interconnections, bends, Y- and T-junction, only working on their fundamental propagating mode and exhibiting a broadband impedance matching, is tackled (this thesis, chapters 3 and 5).

Furthermore, the frequency up-scaling of SIW components only requires a geometrical down-scaling of the waveguide cross-section dimensions (e.g., a sub-millimeter cross-section is required above 75 GHz). This is experimentally proved up to 120 GHz, taking advantage of the photo-lithographic

accuracy of the proposed IC process for manufacturing waveguides, which allows a minimum feature size smaller than 1 μm.

1.3.4 Wideband transition

While on-wafer integration is favorable for boosting performance and reducing complexity, mm-wave systems are in practice realized on few (typically two) substrates to compromise between performance and costs due to the large area required by the antenna elements. As example, commercial applications like automotive radars at 77 GHz [11] and their prototypes at 120 GHz use PCB for the antenna and another one (Si, SiGe, GaAs) for the active chip, which is then top mounted by means of bond-wire or flip-chip technology.

For the proposed 94 GHz radar demonstrator, the active components are integrated using CMOS/BiCMOS technologies, which require expensive IC processing techniques, while the interface/routing and antenna elements are realized in lower cost (i.e., per unit area) technologies with less masks and a poorer resolution [61–63]. When silicon substrates are employed, the manufacturing of passive components remains expensive when compared to PCB solutions due to the higher costs of silicon area (even for poorer resolution processes), but it would become a favorable choice at deep mm-wave frequencies (above 200 GHz) where the use of PCB material is hampered by substrate losses.

Conventional interfaces to the ICs involve the use of bond wires [64] or flip-chip assemblies [65]. In order to use silicon integrated waveguide environment in combination with these assemblies techniques, planar transitions to convert the classical quasi-TEM(transverse electromagnetic) mode, delivered from the active circuits, into the fundamental TE_{10} (transverse electric) mode propagating in the waveguides are required.

In literature, several vialess transitions based on electromagnetic coupling and resonating components have been developed [66–69], but they either provide a narrow impedance matching bandwidth [66], or require the use of large matching structures [67, 68] and the patterning of the back metal [67, 68]. In this work, a planar transition easy to manufacture (e.g., requiring a single metal layer and no vias), frequency scalable and exhibiting a ultra-wide impedance matching bandwidth is aimed for interfacing the waveguide environment to planar ICs.

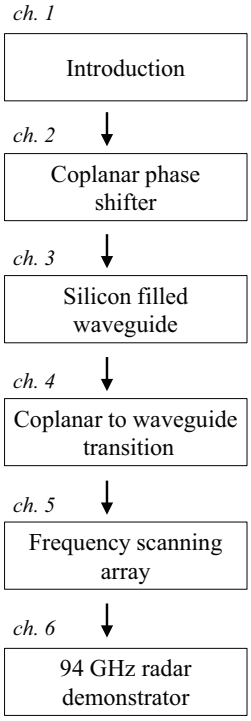


Figure 1.8: Thesis flow, from the introduction of a new integrated waveguide technology on silicon to the demonstration of a narrow-beam radar system at 94 GHz.

1.4 Organization of the thesis

The research activity carried out in the thesis time frame (from October 2006 to August 2012) explores the realization of broadband frequency-scalable passive components for on-wafer phased-array antennas in the whole mm-wave frequency band. The thesis work flow is organized as sketched in Fig. 1.8.

Chapter 2 faces the design of analog electronically tunable phase shifters working at 50 GHz using a coplanar waveguide as transmission line for the smart antenna concept of Fig. 1.6. The controllable phase delay is achieved by periodically loading the line with reverse biased silicon-on-glass (SoG) Schottky diode, whose direct current (DC) control voltage modifies the line unit length capacitance and hence phase constant and delay.

Chapter 3 introduces a novel manufacturing technology based on IC-

compatible steps enabling the realization of silicon-filled integrated waveguide interconnections with continuous metallic side walls. For practical reasons (i.e., measurement setup available in the university lab), operating bandwidths around 50 and 94 GHz are targeted. The frequency scalability of the technology is experimentally demonstrated up to 130 GHz, while no measurements could be carried out in the deep mm-wave range due to the lack of hardware instrumentation.

Chapter 4 presents a planar transition based on a U-shaped resonant slot for interfacing SIWs to planar circuits in CPWs. The ultra-wide impedance matching bandwidth achieved by the transition is explained by means of the slot dipole antenna Q-factor; furthermore, a numerical analysis is carried out to extract simple (frequency scalable) design rules for the transition.

Chapter 5 explores the realization of high-gain smart antennas. A travelling wave slotted waveguide frequency scanning array topology is analyzed by means of the Floquet theorem and the (periodic) Brillouin diagram, which allow to extract sufficient design conditions to enforce only one spatial harmonic inside the (radiating) fast wave region (FWR) of the array.

Finally, chapter 6 illustrates the potentialities of the proposed silicon SIW technology for the implementation of high-performance highly co-integrated mm-wave systems. As demonstrator, a complete frequency-modulated continuous-wave 94 GHz radar sensor on silicon for 3D imaging is presented. The high-gain antenna is implemented with a linear array of frequency scanning arrays (see Fig. 1.6b), interfaced to the active chips by means of flip-chip assembly and CPW-to-SIW transitions. In addition to this, key components as high-frequency electrically tunable distributed phase shifters and waveguide power splitters for the beam forning network of high gain antennas are presented.

Chapter 2

Integrated coplanar phase shifters

2.1 Introduction

Phased array currently used in communication and radar systems make large use of phase shifter components to control the relative phase of each radiating element and electronically steer the beam of the antenna system [70]. For broadband applications, phase shifters with a linear variation of the phase shift with respect to frequency are required in order to prevent beam squinting [71, 72] and to radiate (or receive) under the same angle all the frequency components of a broadband signal.

Phase shifter topologies that employ the physical length of a transmission line to delay a signal are called true time delay lines (TTDL). TTDLs reported in literature have been traditionally based on switched [73, 74] or (narrow band) reflected [75,76] topologies, which are area expensive as they make use of lines of different lengths and switches to select the one of desired length and time delay.

Switched and reflected lines use space (their physical length) to produce the required delay, while keeping the phase velocity of the propagating wave constant. Recently, a new concept based on periodically loaded (i.e., distributed) lines [77] has been introduced, which produces a delay by changing the phase velocity ($v=1/\sqrt{LC}$) of the signal, for instance by periodically loading the line with varactors, while keeping the length of the line constant.

Distributed TTDLs commonly employ micro-electro-mechanical systems (MEMS) [78, 79] or (GaAs and silicon Schottky) diodes [80–83] as tunable

capacitance. The diode series resistance (typically 2-5 Ω [84]) limits the quality factor of Schottky varactors on silicon; MEMS varactors on the other hand, exhibit very high quality factor and linearity, but require high control voltages, large area, and exhibit poor reliability and switching speed when compared to semiconductor based solutions [85].

In this chapter, a distributed topology of analog phase shifter at 50 GHz based on Schottky diodes is presented. The TTDL is analog in the sense that the phase shift value at the output can be continuously tuned (by choosing the proper bias voltage), as opposed to digital where the output is discretized [73]. The contributions to losses of metallization, substrate and diodes are analysed, and design equations are derived to minimize the total losses and area consumption of the structure for a given phase shift. A new process developed at the Dimes T.C. for manufacturing Schottky diodes based on silicon-on-glass substrate transfer technique [86] is briefly explained. Simulation results using Agilent ADS software are presented and compared to experimental measurements for different frequencies and diode bias voltages.

2.2 Distributed phase shifter

The distributed phase shifter is based on a coplanar waveguide line periodically loaded with reverse biased varactor diodes as reactive elements, whose (voltage) tunable capacitance allows to control the transmission line phase velocity. First, general equations that relate the phase velocity and characteristic impedance of the line to the diode capacitance (section 2.2.1) and to the line geometrical dimensions (section 2.2.2) are derived; subsequently, the phase shifter losses are analyzed (section 2.2.3) and design equations are derived in order to minimize the total losses (section 2.2.4) and area consumption (section 2.2.5) of the structure.

2.2.1 Model of the loaded line

In appendix A, the model of a generic lossless two-conductor transmission line is presented in terms of its distributed components (i.e., inductance per unit length L_t and capacitance per unit length C_t) and of its lumped circuit (i.e., inductance L_l and capacitance C_l of a small section).

When the line is periodically loaded with shunt variable capacitances C_{var} of spatial period ℓ, a unit cell can be defined as in Fig. 2.1a, where a parallel capacitance is added to the circuit of Fig. A.1b. As all periodic structures, the loaded line exhibits a resonance, which takes place at the

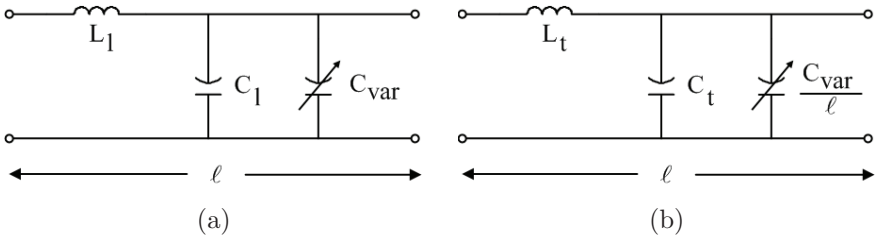


Figure 2.1: (a) lumped and (b) distributed model of a small compared to the wavelength section of a loaded lossless transmission line.

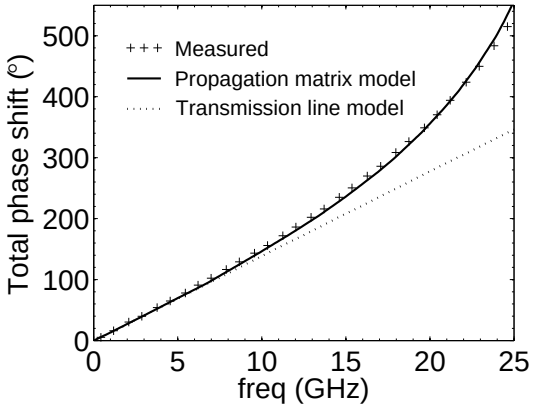


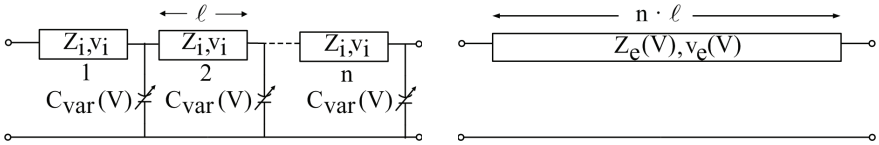
Figure 2.2: Transmission line and propagation model for a distributed phase shifter [87] with a Bragg frequency of 30 GHz. Well below this value, both models give similar results, while at higher frequencies the transmission line model cannot account for the non-linear dispersive behaviour of the structure and a propagating matrix model is needed to match the measurements.

so-called Bragg frequency f_{Bragg} [87]:

$$f_{Bragg} = \frac{1}{\pi \ell \sqrt{L_t (C_t + \frac{C_{var}}{\ell})}} \tag{2.1}$$

and which depends on the loading condition of the line.

At operating frequencies well below this value, a transmission line model for the phase shifter can be used (see Fig. 2.2 [87]). The lumped loading capacitance C_{var} can be distributed over the length of the unit cell as C_{var}/ℓ (see Fig. 2.1b), and a synthetic artificial transmission line (see Fig. 2.3)



(a) (b)

Figure 2.3: (a) a transmission line periodically loaded with voltage dependent lumped capacitances and (b) its synthetic equivalent; note that the characteristic impedance and phase velocity are voltage dependent.

with modified extrinsic impedance Z_e and phase velocity v_e can be defined [87–89]:

$$v_e = \frac{1}{\sqrt{\frac{L_l C_{l,tot}}{\ell^2}}} = \frac{1}{\sqrt{L_t(C_t + \frac{C_{var}}{\ell})}} \tag{2.2}$$

$$Z_e = \sqrt{\frac{L_l}{C_{l,tot}}} = \sqrt{\frac{L_t}{C_t + \frac{C_{var}}{\ell}}} \tag{2.3}$$

The term "extrinsic" refers to the fact that a loading element has been added to the intrinsic (i.e., unloaded) line. If C_{var} is a variable capacitance, the phase shift can be modified by an external control signal. The time delay ϕ_l experienced by a wave travelling along n sections ℓ of the line is given by $n\beta\ell$ (see eq. A.8), where the phase constant β contains the extrinsic phase velocity given by eq. 2.2. The phase delay is voltage dependent, and a controlled tunable phase shifter is obtained.

Eq. 2.2 says that the phase velocity is frequency independent and thus the phase shift is linear with frequency. In all the equations mentioned above, C_{var} is always divided by ℓ, which is small with respect to the wavelength, as if the lumped capacitance can be distributed over the length of the transmission line section in order to be added to the intrinsic line capacitance per unit length C_t (see Fig. 2.1b). At frequencies close to Bragg resonance, eq. 2.2 and the transmission line model in Fig. 2.1a become inaccurate: the discrete nature of the loading capacitances prevails and a propagation matrix model of the phase shifter needs instead to be employed [87], which leads to a non-linear phase shift with frequency (see Fig. 2.2). As rule of thumb for a good linear behaviour, the Bragg frequency of a distributed phase shifter should be at least two and a half times larger than the maximum operating frequency [79, 89].

2.2.2 Design equations

In the equations presented in section 2.2.1, the capacitance per unit length of the intrinsic line C_t is always added to the lumped capacitance C_{var} normalized to the length of the section ℓ. Those quantities can be therefore grouped in a variable called the loading factor x [87]:

$$x = \frac{C_{var}^{max}/\ell}{C_t} \tag{2.4}$$

where the maximum value of the variable capacitance has been used.

The capacitance ratio y is defined as:

$$y = \frac{C_{var}^{min}}{C_{var}^{max}} \tag{2.5}$$

and depends on the type and the manufacturing process of the capacitance, with a larger capacitance sweep from C_{var}^{min} to C_{var}^{max} corresponding to a lower y.

The impedance of the extrinsic line varies according to the loading capacitances: in the case C_{var} is made with a varactor diode, losses are higher when approaching the forward region, where the maximum value of the capacitance occurs. It is therefore preferred to impose the minimum line impedance, associated to the maximum value of C_{var}, to be 50 Ω (see eq. 2.3) in order to at least minimize reflection losses. When instead the line is loaded with a lower value of capacitance, larger reflection losses will occur since the line impedance is higher than 50 Ω; however, the diode will be working in the (deep) reverse-biased region and hence will exhibit lower insertion losses.

The minimum impedance Z_e^{min} of the loaded line is produced with the maximum value of capacitance C_{var}^{max}:

$$Z_e^{min} = \sqrt{\frac{L_t}{C_t + \frac{C_{var}^{max}}{\ell}}} = \frac{Z_i}{\sqrt{1+x}} \tag{2.6}$$

The characteristic impedance Z_i of the intrinsic (unloaded) line is given by:

$$Z_i = Z_e^{min}\sqrt{1+x} \tag{2.7}$$

and has therefore to be larger than 50 Ω. Eq. 2.7 is a fundamental design equation since it relates the impedance of the unloaded line, which only depends on the line geometrical dimensions and dielectric layers, to the lumped capacitance (contained in x) loading the line. For a CPW, the

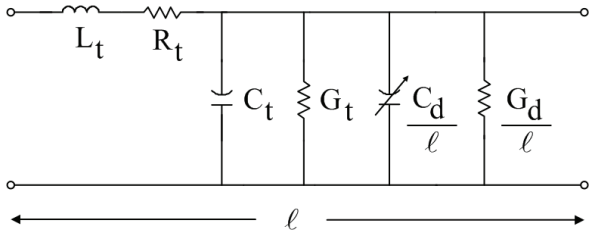


Figure 2.4: Section of a loaded lossy transmission line.

expressions of the characteristic impedance in terms of physical dimensions can be found in [90].

The minimum Bragg frequency in eq. 2.1 is given by:

$$f_{Bragg}^{min} = \frac{1}{\pi\ell\sqrt{L_t C_t(1 + C_{var}/\ell)}} = \frac{v_i}{\pi\ell\sqrt{1+x}} \tag{2.8}$$

Since f_{Bragg}^{min} is set to two and a half times the maximum working frequency (see section 2.2.1), the loading period ℓ can be determined as:

$$\ell = \frac{v_i}{\pi f_{Bragg}^{min}\sqrt{1+x}} \tag{2.9}$$

Said ϕ_l the phase shift experienced by a wave β travelling along one section ℓ of the line (see eq. A.8), the total tunable phase shift $\Delta\phi$ experienced by the wave when sweeping the loading capacitance between its minimum and maximum value is given by:

$$\Delta\phi = (\beta_{min} - \beta_{max})\ell = 2\pi f\frac{\ell}{v_i}(\sqrt{1+x} - \sqrt{1+xy}) \tag{2.10}$$

and the number of section required to achieve a given $\Delta\phi$ phase shift is given by:

$$n = \frac{\pi}{\Delta\phi} \tag{2.11}$$

2.2.3 Metallic, dielectric and diode losses

In section 2.2.2 general design equations were presented for choosing the impedance of the intrinsic line (eq. 2.7), the minimum Bragg frequency, the loading period (eq. 2.9) and the number of sections (eq. 2.11) independently from the implementation of the variable capacitance. The capacitance ratio y is fixed by the technology: from eq. 2.10 and 2.11, the maximum allowed

sweep has to be used in order to minimize the number of sections required and hence insertion losses. Similarly, also the loading factor x can be chosen to minimize losses and area consumption; however, since the phase shifter losses are affected by how the variable capacitance C_{var} is implemented, a choice has to be made and the following considerations only apply to the case of a reverse-biased diode varactor.

Fig. 2.1 reported the lossless model of a small section of extrinsic transmission line. Losses are taken into account by adding a series resistance per unit length R_t for conductive losses in the metal and a parallel conductance per unit length G_t for dielectric losses in the substrate; losses in the diodes are mainly caused by the contact series resistance. Using the parallel model of the diode described in appendix B, the extrinsic (i.e., loaded) lossy line in Fig. 2.4 is obtained, where C_d and G_d are the diode parallel capacitance and conductance given by eq. B.4 and B.5 reported in appendix B.

The propagation constant γ is expressed as:

$$\gamma = \sqrt{(R_t + j\omega L_t)(G_{t,tot} + j\omega C_{t,tot})} \tag{2.12}$$

$$G_{t,tot} = G_t + \frac{G_d}{\ell} \tag{2.13}$$

$$C_{t,tot} = C_t + \frac{C_d}{\ell} \tag{2.14}$$

where, similarly to what found in section 2.2.2 for the diode capacitance, also the diode conductance G_d is divided by the length of the section when added to the intrinsic line parallel conductance per unit length G_t. In the assumption of small losses, the propagation constant γ becomes:

$$\gamma = \alpha + j\beta = \alpha_{cond} + \alpha_{diel} + \alpha_{diode} + j\beta \tag{2.15}$$

where the phase constant β and the attenuation constant α for each loss mechanism are given by:

$$\beta = \omega\sqrt{L_t C_{tot}} \tag{2.16}$$

$$\alpha_{cond} = \frac{R_t}{2Z_i} \tag{2.17}$$

$$\alpha_{diel} = \frac{G_t Z_i}{2} \tag{2.18}$$

$$\alpha_{diode} = \frac{G_d^{parallel} Z_i}{2} = \frac{Z_i}{2R_d^{series}} \frac{1}{1+Q_d^2} \tag{2.19}$$

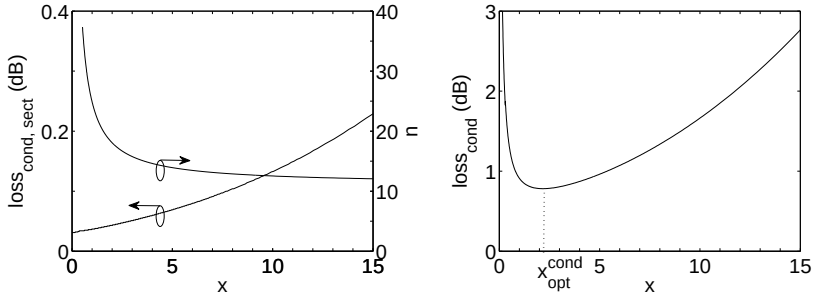


Figure 2.5: Conductor loss of a distributed phase shifter: (a) per section and (b) for a 180° differential phase shift. A CPW with a gap of 50 μm on an Eagle 2000 pyrex glass substrate ($\epsilon_r = 4.6$) is considered. Conductor losses increase for x approaching to 0 since this corresponds to a CPW with a very narrow signal line (see eq. 2.7).

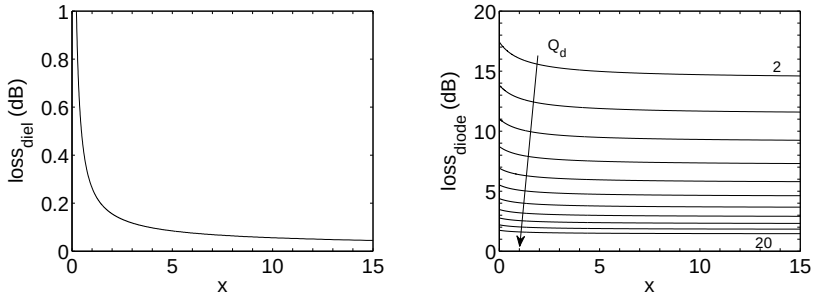
with Q_d the diode Q-factor. The expressions of the resistance per unit length R_t and parallel conductance per unit length G_t of the intrinsic line can be found in [90].

2.2.4 Loss minimization

The conductive, dielectric and diode series resistance losses of the phase shifter can be computed using the expressions of the attenuation constants found in section 2.2.3. Conductor losses per section (in decibels) are given by:

$$loss^{dB}_{cond,sect} = 8.69\,\alpha_{cond}\ell \tag{2.20}$$

where the factor $20\log_{10}e$=8.69 arises from the conversion from nepers to decibels. Fig. 2.5a reports the metallic losses of a single section of the phase shifter, and the number of sections required to obtain a total phase shift of 180°. Since the loading factor is related through eq. 2.7 to the impedance of the intrinsic line (which depends on the line geometrical dimensions [90]), it is possible to show that a large loading factor x corresponds to a line with a high intrinsic impedance Z_i, that has therefore higher conductive losses [91]. However, increasing the loading factor, the number of sections decreases since this corresponds to a larger diode (variable) capacitance with respect to the (fix) intrinsic line capacitance (see eq. 2.4). Multiplying the two curves together according to eq. 2.20, the conductor losses of the phase shifter for a 180° total phase shift are obtained. Fig. 2.5b shows the



(a) (b)

Figure 2.6: (a) dielectric and (b) diode loss for a 180° differential phase shift. A loss tangent of 0.005 for the substrate is assumed. The diode Q-factor is logarithmically sweeped from 2 to 20 at 50 GHz.

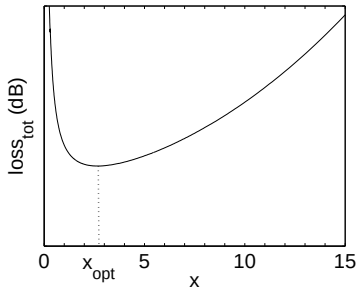


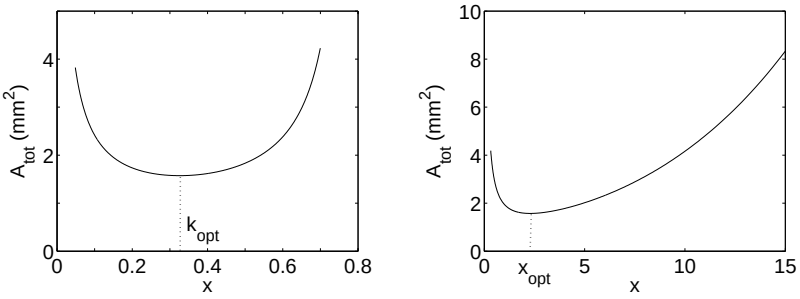
Figure 2.7: Total losses of a distributed phase shifter for a 180° differential phase shift. Only the shape of the curve is relevant; the exact values on the vertical axis depends on the diode Q-factor and is therefore omitted.

existence of an optimum value of the loading factor x_{opt}^{cond} that minimizes the losses. As example, if the CPW is realized on an Eagle 2000 pyrex glass substrate ($\epsilon_r = 4.6$) and with a gap of 50 μm, x_{opt}^{cond} corresponds to a signal line width of also 50 μm.

In a similar fashion, dielectric and diode losses are obtained. Adding up the three terms, the total losses of the phase shifter (excluding reflection losses) are computed:

$$loss_{tot}^{dB} = loss_{cond}^{dB} + loss_{diel}^{dB} + loss_{diode}^{dB} \tag{2.21}$$

Dielectric losses in the substrate are very small compared to the other two terms (see Fig. 2.6a) and can be neglected. The exact value of diode losses



(a) (b)

Figure 2.8: Phase shifter total area versus: (a) the normalized signal line width and (b) loading factor. A pyrex glass substrate with $\epsilon_r = 4.6$ is considered, with the signal line width arbitrarly fixed to 50 μm.

depends upon the diode Q-factor, but the slope in Fig. 2.6b versus the loading factor is very small and the curve is assumed to be flat. Therefore, the shape of the curve in Fig. 2.7 representing the total losses is the same as the one in Fig. 2.5a, and hence the x_{opt} that minimizes the total losses can be approximated with the x_{opt}^{cond} that minimizes conductor losses.

2.2.5 Area consumption minimization

The characteristic impedance of a coplanar waveguide is a function of the normalized signal line width k [90]:

$$k = \frac{S}{S + 2W} \tag{2.22}$$

where S is the signal line width, W the gap and hence $S + 2W$ the spacing between the two ground planes. Eq. 2.22 states that only the ratio W/S determines Z_i rather than the separate values of S and W.

The signal line width of a CPW is usually dimensioned smaller than $\lambda_g/10$ in order to maintain a good transverse confinement of the electromagnetic field. The ground plane B of the CPW has to be wide enough to allow the electric field in the gap to decay to zero in the transverse section. Based on the parametric study reported in [92], a good choice for it would be:

$$B = S + W \tag{2.23}$$

The total area A_{tot} occupied by the CPW phase shifter is then given by:

$$A_{tot} = (S + 2W + B)n_{sect}\ell \tag{2.24}$$

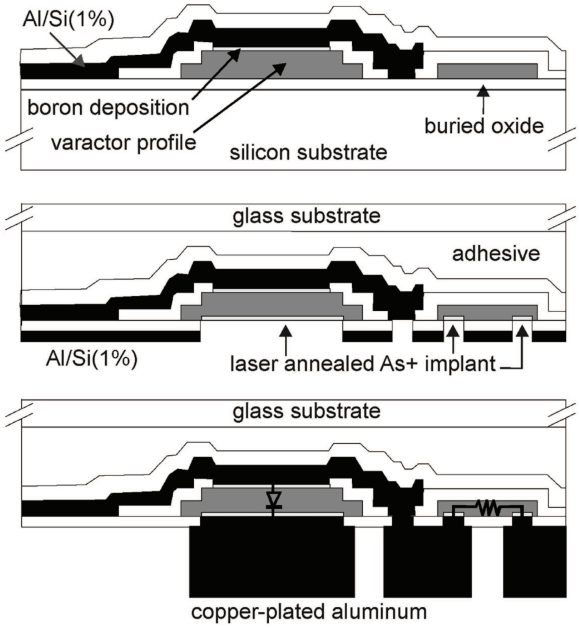


Figure 2.9: Process flow for the manufacturing of a Schottky diode and a high-ohmic resistor using the Dimes T.C. silicon-on-glass technology [85].

and can be expressed as a function of k and x:

$$A_{tot} = (1 + \frac{2}{k}) \frac{1}{\sqrt{1+x} - \sqrt{1+yx}} \frac{v_i}{2f} W \tag{2.25}$$

The area consumption depends by the ratio W/S contained in k (as for the characteristic impedance), but also from the particular value of W. Therefore, if S is fixed to an arbitrary value, A_{tot} can be plotted versus k which is only a function of W. The total area consumption in Fig. 2.8a shows a minimum for $k_{opt} = 1/3$. Since k is related to x through eq. 2.7, it can be shown (replace x given by eq. 2.7 in eq. 2.25 and express Z_i as a function of k through [90]) that the k_{opt} minimizing the area consumption corresponds exactly to the same x_{opt} in Fig. 2.8b that minimizes the phase shifter total losses in section 2.2.4.

2.3 Dimes T.C. varactor diode

The Q-factor of a varactor implemented with a reversed-biased diode is usually limited by the series resistance associated with the buried layer used for contacting the diode. To overcome this and drastically increase the Q-factor, a new generation of varactor diodes [85] was developed at the Dimes center that makes use of substrate transfer technique and allows to manufacture diodes with metal contacts on both sides.

The technology process is described in Fig. 2.9: a Schottky diode is realized on the top face of a silicon substrate, and the first metal contact is formed. The wafer is then glued upside down to a glass carrier, and the silicon wafer is removed at the bottom. After the wafer transfer, the other side of the diode can be accessed, and the second metal contact is opened.

The key feature of this process is the drastic reduction of the series resistance of the varactor by eliminating the buried layer typically used for contacting the diode. The ability of having ohmic contacts on both sides together with the usage of a glass substrate which reduces dielectric losses allows Q-factors in the order of 100 or more at 2 GHz to be achieved [85,93].

Therefore, voltage-controlled capacitances can be realized exhibiting low losses and high Q-factors in the reverse-bias region of the diode. Linearity requirements can be satisfied by the implementation of special varactor topologies and optimization of the implanted/epitaxially grown doping profile [93–96].

2.4 Phase shifter simulation

The distributed phase shifter was simulated with the aid of Agilent ADS in two steps: first, the intrinsic (i.e., without diodes) CPW is simulated with ADS Momentum [97], placing ports in correspondence to the diode locations. After that, the unloaded transmission line is imported in an ADS schematic [98], where varactor diodes are connected and the entire phase shifter can be simulated.

The design parameters are summarized in Table 2.1. The value of the diode series resistance is calculated from the Q-factor results reported in [85, 93]; Q_d was fixed to 3 at 50 GHz at -1 V biasing voltage since the electroplating of copper on the contacts, which further reduces losses, was not available for this particular process run. Note from Table 2.1 that for an optimum design (i.e., the loading factor x_{opt} is chosen) the minimum diode capacitance C_{diode}^{min} is practically equal to the capacitance of the intrinsic line C_l, as discussed in detail in section 2.4.1.

Table 2.1: Design parameters: specifications (working frequency and material properties) are on the top-left side; independent variables are chosen based on the considerations of section 2.2.

specifications		dependent var.	
freq (GHz)	50	Z_i (Ω)	91
glass ϵ_r	4.6	Z_{max} (Ω)	65
substrate loss tangent	0.005	ℓ (μm)	260
Q_d	3[1]	n_{sect}	18[2]
capacitance ratio y	0.42	$\Delta\phi_{sect}^{diff}$ (°)	10.5
independent var.		C_d^{min} (fF)	35
Z_{min} (Ω)	50	C_d^{min} (fF)	15
f_{Bragg}^{min} (GHz)	125	C_l (fF)	16
loading factor x	2.3	A_{tot} (mm × mm)	0.35 × 4.68

[1] at 50 GHz and -1 V

[2] for a 189° total phase shift

Fig. 2.10 reports a simulation of the phase shifter of Table 2.1 versus the frequency for the minimum and maximum loading condition: in both cases the structure behaves linearly with frequency, which is the result of the proper selection of the Bragg frequency (i.e., two-and-a-half times the operating frequency).

The second step was to simulate the phase shifter fixing the operating frequency (i.e., 50 GHz) and sweeping the bias voltage in order to change the diode capacitance. Fig. 2.11a shows that varying the voltage from -1 V to -10 V, a total phase shift of 197° is obtained. The minimum voltage is limited by the diode breakdown (-11 V was assumed), while the maximum dc voltage was set to -1 V. Considering in this work a maximum amplitude of the alternating current (ac) signal of 1 V, the choide avoids that the ac signal sumperimposed to the dc bias pushes the diode in the the forward region where the increase of current flowing from the CPW signal line to ground planes through the diode series resistance would drastically increase the insertion losses. This is evident in Fig. 2.11b: the phase shifter losses are minimum when the varactors work in deep reversed-biasing condition, while the S_{21} signal exponentially decreases as the dc voltage approaches zero. The input impedance matching is instead always below -10 dB for all the biasing voltages.

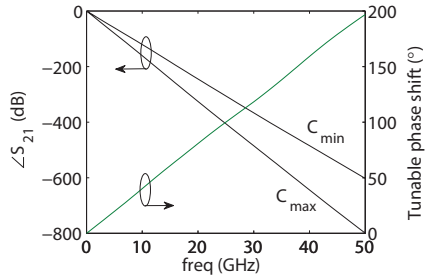
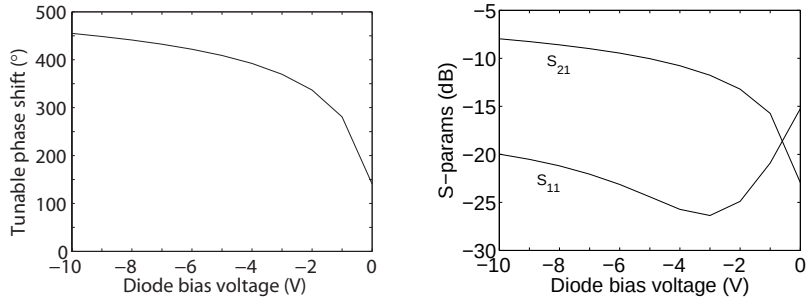


Figure 2.10: Simulations: phase shift and total phase shift; a diode breakdown voltage of -11 V is assumed. The total phase tunable shift is 197° at 50 GHz.



(a) (b)

Figure 2.11: ADS simulations: (a) total tunable phase shift and (b) losses. The diode reverse bias voltage cannot exceed the breakdown voltage.

2.4.1 Diode loading effect

The diode series resistance was added to the schematic simulations based on the results contained in [85, 93], where the diode Q-factor is reported at 2 GHz and for capacitances in the order of tens of picofarads. Since no high frequency characterization of the silicon-on-glass manufacturing process was available, a linear scaling for the diode Q-factor with frequency and with area was assumed as first order approximation. However, due to the significantly higher frequency (i.e., 50 GHz versus 2 GHz reported in [85, 93]), parasitic elements and fringing effects that do not linearly scale with frequency, this approximation can only lead to qualitative results.

In order to understand the impact of the linear scaling approximation on the phase shifter losses, a simulation was carried out sweeping the Q-

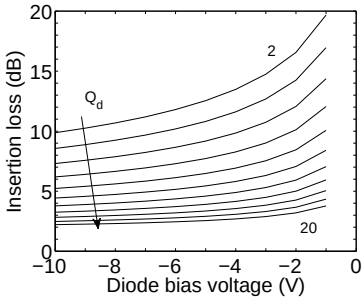
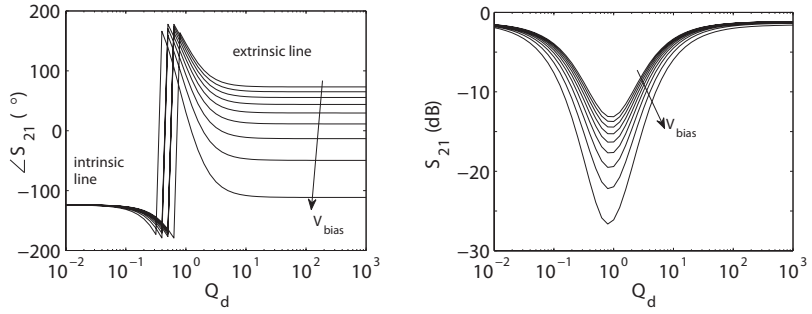


Figure 2.12: Simulations: insertion loss (i.e., $-S_{21}$) for a logarithmic sweep of the diode Q-factor from 2 to 25 at 50 GHz; the value of Q_d reported on the graphs is at -1 V.



(a) (b)

Figure 2.13: Simulations: phase shift (a) and insertion loss (b)) for a logarithmic sweep of the diode Q-factor and a linear sweep of the bias voltage from -9 V to -1 V at 50 GHz.

factor from 2 to 20 at 50 GHz. For high Q-factors, losses in Fig. 2.12 are almost dc voltage indepentent, while for low Q-factors (i.e., approaching 2) they become strongly dependent to its exact value, showing a variation of even one order of magnitude as the bias voltage is swept.

Fig. 2.13a reports the phase and the magnitude of the signal at the output of the phase shifter for a logarithmic sweep of the diode Q-factor, parameterized with respect to the bias voltage. When the Q-factor is small ($Q_d < 1$), the parallel diode capacitance is close to zero (eq. B.5) and the parallel conductance approaches $1/R_d$ (eq. B.4). The current mostly flows in the diode conductance rather than in the tunable capacitance, so that the phase of the output signal is independent from the applied bias voltage.

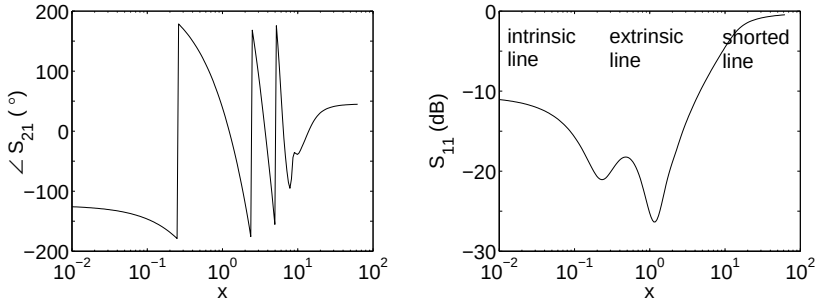


Figure 2.14: Simulations: phase shift (a) and return loss (b)) for a logarithmic sweep of the loading factor x. The diode Q-factor is set to 3 at 50 GHz and the bias voltage at -1 V.

The circuit acts as an intrinsic line, that is as if no loading elements were applied, and no phase shift can be produced. When the Q-factor increases ($0.1 < Q_d < 1$), the current starts flowing in the tunable capacitance, whose susceptance becomes comparable or bigger than the conductance associated to the diode series resistance. For $1 < Q_d < 10$ a large phase shift is achieved but insertion losses are significant (see Fig. 2.13b). Finally, for a large Q-factor ($Q_d > 10$) losses decreases for the same amount of phase shift and the structure properly behaves as a voltage-controlled extrinsic transmission line.

Extra considerations on the existence of an optimum value x_{opt} of the loading factor can be drawn in simulations by sweeping x, for instance by varying the diode maximum capacitance (i.e., at -1 V) and keeping the intrinsic line capacitance C_l fixed (see eq. 2.4). When $x < 0.1$ (see Fig. 2.14a), the diode susceptance acts like an open circuit: the loading effect of the varactors is too small compared to C_l and no phase shift can be produced. For $0.1 < x < 1$, the phase of the signal is affected by the the diode capacitance; this variation becomes extremely significant when $1 < x < 10$, as the slope of the $\angle S_{21}$ curve reveals. The result is not surprising since it was shown in section 2.4 that the optimum value of the loading factor x_{opt} which minimizes losses and area occupancy corresponds to a diode capacitance of the same order of magnitude of the intrinsic line capacitance (see Table 2.1). Last, when $x > 10$ the capacitive susceptance is so large to short the signal line to the ground plane of the coplanar waveguide. The phase of the output signal does not change with the diode capacitance since the input impedance of the line is very high: the signal

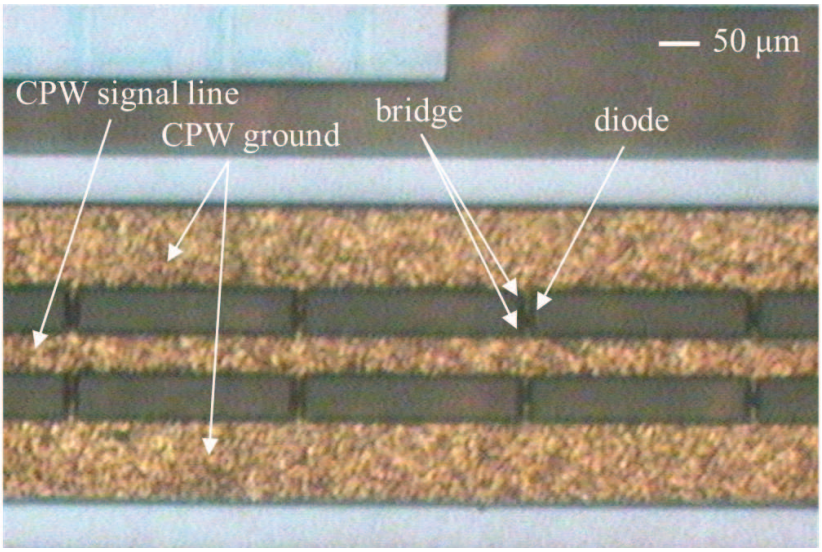


Figure 2.15: Photo of a distributed phase shifter. Metal bridges (in vertical) are used to connect the varactor diodes to the signal line and ground plane of the CPW.

hardly enters the phase shifter but is mostly reflected back, and the return loss of the structure approaches 0 dB (see Fig. 2.14b).

2.5 Phase shifter measurements

Measurements were performed with an HP8510C Vector Network Analyzer [101] on a Cascade probe station [102] using infinity ground-signal-ground probes [103] with a pitch of 100 μm. Fig. 2.15 shows a picture of the realized distributed phase shifter: the gap between the signal and ground plane of the coplanar line is periodically loaded with small diodes, which are connected to the CPW by using metal bridges and are manufactured according to the process described in section 2.3. Since two diodes per section are used in parallel on both sides of the line to maintain the symmetry of the circuit, each diode has only half of the capacitance value reported in Table 2.1; however, the total Q-factor of each section ($Q=1/wR_dC_{var}$) is unchanged because as result of the parallel conection the total capacitance is doubled but the total resistance halved.

The first set of results in Fig. 2.16 shows the phase shifter performances

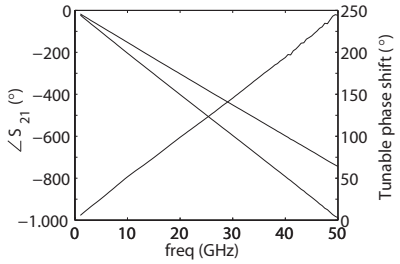
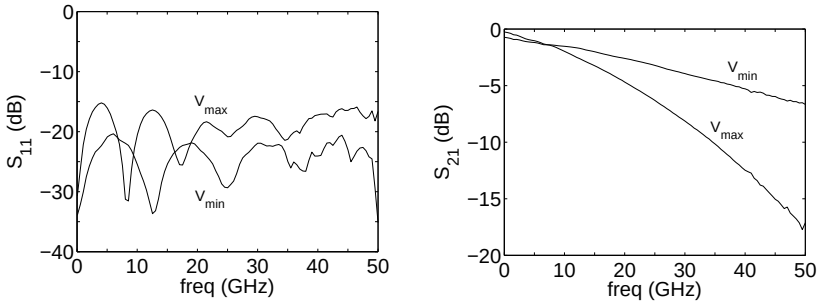


Figure 2.16: Measurements results: phase shift and total tunable phase shift versus frequency.



(a) (b)

Figure 2.17: Measurement results: (a) return and (a) insertion loss versus frequency for -15 V and -1 V bias voltage.

versus frequency for the maximum and minimum diode voltage, respectively -1 and -15 V, as the measured breakdown voltage is -16 V. The value is much lower than the -11 V used in design and simulations that was based on a worst-case scenario. In practice, the breadown voltage of Schottky diodes manufactured at the Dimes T.C. showed signifcant fluctuations per process run, and moroever no characterization of femtofarads varactors was available during the design stage. The breakdown voltage of -11 V was based on the experimental results of [85, 93], valid for diodes with a capacitance three order of magnitudes larger.

As already found in simulations, the phase shift is linear for both loading conditions of the line from low frequency up to 50 GHz; subtracting the two delays, the total phase shift on the right axis is obtained. The return loss in Fig. 2.17a is always below -15 dB for the whole frequency range. The insertion loss in Fig. 2.17b is small and comparable for both voltages

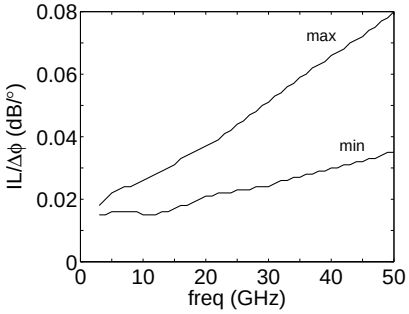
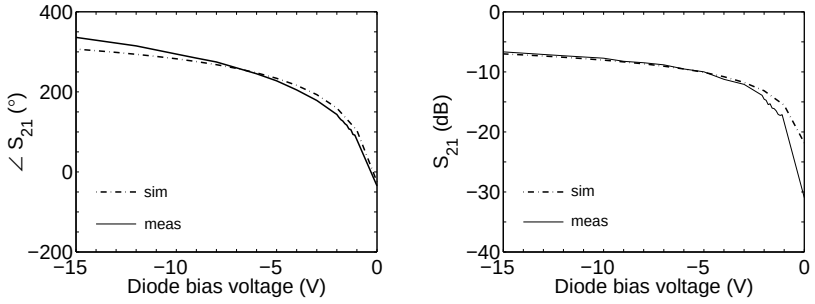


Figure 2.18: Minimum and maximum insertion loss for a total phase shift of one degree versus frequency.



(a) (b)

Figure 2.19: Measurement results: (a) return and (b) insertion loss versus the diode (reverse) bias voltage at 50 GHz.

at low frequency, where the diode Q-factor is high and the susceptance is much bigger than the conductance; as the frequency increases, the Q-factor decreases and the insertion loss strongly depends on the bias voltage, as already predicted by Fig. 2.12.

The relation between phase shift and losses is expressed in Fig. 2.18 as losses per degree of phase shift. This means for instance that at 20 GHz the phase shifter will exhibit insertion losses between 0.021 and 0.037 dB/° for the different biasing conditions, or equivalently a difference of 3 dB between maximum and minimum insertion loss (i.e., 6.7 and 3.8 dB, respectively) for a 180° total phase shift.

Fixing the operating frequency to 50 GHz, the phase shifter behaviour is then analysed for different reverse biasing conditions in Fig. 2.19. The phase

Table 2.2: Comparison of distributed phase shifter designs using different diode technologies.

design	[99]	[100]	[87]	this work
transmission line	CPW	SIW	CPW	CPW
diode technology	GaAs	discrete[1]	CMOS 130 nm	SoG
freq (GHz)	10	29	40	50
$\text{loss}_{max}/\Delta\phi$ (dB/180°)	2.2	14.7	9.8	12.5
$\text{loss}_{min}/\Delta\phi$ (dB/180°)	1.4	8.3	5.3	4.9

[1] bondable varactor chip

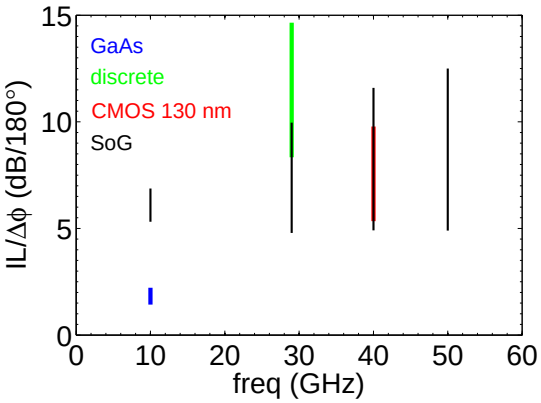


Figure 2.20: Comparison of distributed phase shifter performances using different diode technologies: the vertical lines represent the measured losses for a 180° total phase shift, considering a full sweep of the diode reverse bias voltage.

shift does not change linearly with the applied voltage since the current-voltage characteristic of the diode is non-linear, but this is not important in the implementation of a delay line as the linearity needs to be guaranteed only with respect to the frequency. Insertion loss agrees well with simulations, where a diode Q-factor of 3 at 50 GHz was used. The structure achieves a total total phase shift of 244° by sweeping the diode voltage from -15 V to -1 V with a maximum insertion loss of 17 dB. The possibility of

biasing the diodes with even lower voltages allows to increase the achievable capacitance sweep (i.e., the capacitance ratio y is lower than what reported in Table 2.1) and hence to employ a smaller number of sections. With the present design, a total phase shift of 180° can be obtained with a maximum insertion loss of 12.5 dB by reducing the number of sections in Table 2.1 from 18 to 14.

A comparison of distributed phase shifters employing different transmission lines and diode technologies is reported in Table 2.2 and Fig. 2.20; no results at 50 GHz were found in literature. The use of discrete diode chips gives much worse performances than a design where diodes and transmission lines are integrated together; SoG and CMOS 130 nm varactors exhibit similar losses, but are outperformed by GaAs diodes.

It is worth mentioning one final recommendation. In order to reduce losses, it could (incorrectly) be thought that the diodes should operate only in the deep reverse bias region where they exhibit lower losses. However, this would reduce the variable capacitance sweep and a larger number of sections should be used for achieving the same phase shift, increasing in turn losses. As example, a 180° phase shift can be achieved by using 14 sections and a maximum voltage of -1 V, leading to an insertion loss of 12.5 dB, which increases to 14 dB when 18 sections and a lower maximum voltage (in the specific case -2.1 V) are used. The equations presented in section 2.2 already guarantee minimum losses (and area occupancy) for the design. The only precaution to take consists in avoiding the diodes to work in the forward region, so that the superposition of the dc and rf signal should always be smaller than 0 V.

2.6 Conclusions

In this chapter, the possibility of integrating varactor diodes in the gap of a coplanar waveguide was explored in order to control the phase delay of the line and to produce a voltage controlled phase shifter.

A design operating at 50 GHz based on a distributed topology was presented: the structure is compact in size thanks to the low area required by the passives, and good performances in terms of phase shift and return loss are achieved. The main limitation is constituted by the insertion loss when the diodes are biased close to the forward region, but a conspicuous improvement in the Q-factor at mm-wave frequencies is expected by increasing the silicon doping level and by electroplating a layer of copper on the diode metal contacts.

Considering the high losses achieved by the proposed phase shifters however, the smart antenna design of Fig. 1.6a based on individual antennas,

each of which connected to a phase shifter, has to be discarded, and a new technology for the realization of frequency scanning arrays as in Fig. 1.6b has to be developed in the next chapters.

Chapter 3

Silicon filled waveguide

3.1 Introduction

At mm-wave frequencies, the small wavelength in the order of millimeters opens the possibility to the realization of high performance systems [104–107] with the electronics and the antennas cointegrated in single compact modules [108,109]. To achieve this, technology platforms [110,111] to interface active (integrated circuits) and passive (radiating elements) components in a low loss and broadband fashion are required.

Transmission lines such as coplanar waveguides and microstrips are commonly used to transfer or process high-frequency signals from one point to the other or to provide impedance matching and harmonic termination in integrated circuits [112, 113]. Neverheless, their high conductor losses (several decibels per centimeter [19–21]) and poor field confinement (crosstalk [22] and surface wave [23, 24] effects) above 30 GHz discard their use in applications such as imaging systems, where the mm-wave signal has to be distributed for several wavelengths from the active chip to the large (i.e., high gain) phased array antenna [114]. Shorting vias in the ground plane [25] or floating shielded CPW topologies [26] can be employed, but the achieved attenuation losses are still high, in the order of 0.75 dB/mm for a gallium arsenide (GaAs) substrate and 0.7 dB/mm for a back-end CMOS 130-nm technology at 100 GHz, respectively.

Metallic waveguides can guide microwave signals for long distances with low losses [27] providing ideally perfect field confinement, but their bulk nature hinder their use as interconnection for planar circuit. Several attempts to manufacture waveguides at mm-wave frequencies have been reported in literature based on micromachining techniques [34–37] or low temperature

co-fired ceramics (LTCC) materials [28, 115, 116], but their frequency upscaling is limited by the increasing insertion loss due to alignment accuracy and field leakage. On the other hand, manufacturing flows based on IC process techniques would allow easy scaling of the waveguide dimensions because of the higher geometrical control and minimum feature size resolution.

In this chapter, a new technology for manufacturing silicon-filled integrated waveguides based on photo-lithography is illustrated. The technology steps are explained and two different types of waveguide are considered: when a potassium hydroxide (KOH) solution is used as etchant, waveguides with a trapezoidal cross-section are obtained; when instead a deep reactive-ion-etching (DRIE) is performed, waveguides exhibit a rectangular cross-section. Design rules are presented, and a numerical modal analysis for KOH waveguides with different height over width aspect ratios (AR) is carried out. In the end, measurement results are reported and compared to Ansoft HFSS [117] simulations.

3.1.1 Mm-wave metallic waveguides

Metallic waveguides operating at millimeter waves reported in literature can be grouped into two categories: micromachined waveguides, exhibiting continous metallic side walls, and substrate integrated waveguides, whose side walls are discrete as made of periodic metallic vias.

One of the first examples of micromachined waveguide is the snap-together structure reported in [118]: two wafers are etched, metallized, and then bonded together, resulting in an air-filled waveguide with a rectangular cross-section, but the resulting structure is bulk in nature and cannot be interfaced in an easy way to planar circuits. Other attempts based on planar IC process techniques involved the use of photo-imageable thick-films [119] and photo-resist material [120]. The process in [119] starts with a thick aluminum plane for mechanical stability; on top of it, a layer of dielectric is screen printed and then removed in correspondence of the waveguide vertical walls, where conductive paste is used to fill in the trenches. These steps are repeated several times in order to increase the waveguide height, which can reach up to 60 μm by using 18 layers. In [120] instead a thick layer of photoresist is spinned and developed on a substrate to form the waveguide shape; after it, a layer of gold is evaporated and electroplated, and the photoresist is washed away. In both approaches the reduced height of the resulting waveguide, limited either by alignment accuracies for stacking more layers or by photo-resist thickness, causes higher losses when compared to ordinary rectangular waveguides.

Recently the substrate integrated waveguide concept [28] was introduced, opening the posssibility to the design of passive components using waveguides [29–33]. A substrate integrated waveguide is a synthetic waveguide realized (for instance on a printed circuit board) as in Fig. 1.4a: the top and bottom faces are formed by conventional patterning of metal layers, while the side walls are made of metallic vias punched through the dielectric substrate. The word "synthetic" refers to the fact that SIWs present the same electromagnetic behavior of waveguides with continuous metallic side walls, if the radius and the spacing of the vias are a small fraction of the wavelength: to avoid radiation leakage, the via diameter needs to be smaller than one eight of the waveguide width, and the via spacing smaller than two and a half times the via diameter.

and the via spacing need to be smaller than one eight and one third of the waveguide width, respectively [17, 41, 121, 122]. This condition limits the scalability of SIWs fabrication process as the limited geometrical control (e.g., shrinkage of the conductor and dielectric layers in LTCC) and the minimum via diameter in the order of few hundred of microns [123, 124] would cause field leakage through side walls [125, 126] at high frequencies (e.g., above 100 GHz). Moreover, the reduced fabrication resolution [127] limits the achievable performances of high gain antennas: as example, the minimum metal opening around 75 μm for an SIW on PCB [128] would reduce the gain of a Taylor array at mm-wave frequencies as the first (wide) slots of the array would already radiate most of the power.

3.1.2 Mm-wave dielectric waveguides

Another topology of waveguide that can be implemented in PCB technology is the so-called substrate integrated image guide (SIIG) [124], the PCB equivalent of a dielectric waveguide, where the signal is confined inside a dielectric by the high refraction index difference between the waveguide substrate (dielectric) and the exterior media (dielectric with rows of air vias). SIIGs require several rows of vias to achieve a high transmission line Q-factor (e.g., above 500) at 94 GHz [124], bringing the total waveguide width to several wavelengths. In this case, they exhibit low losses and has been used for the design of high gain antenna arrays up to 94 GHz [67].

Similar considerations apply to ridge gap waveguides [129], which take advantage of metamaterials to simulate a perfect magnetic conductor (PMC). The structure is formed by two parallel conducting surfaces, ideally perfect electric conductor (PEC), between which the field propagates, and two PMC side walls, which provide field confinement and are implemented by corrugating one of the two surfaces with a periodic texture outside the ridge.

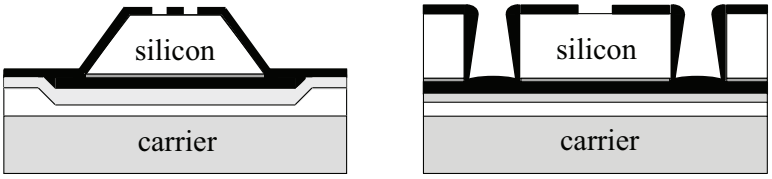
The resulting waveguide requires dedicated fabrication capabilities and is not planar in nature, as the nails that typically form the corrugation require a height comparable to the total waveguide height. Moreover, the number of nail rows in the transverse dimension determines the field confinement, which is for instance better than 50 dB at 15 GHz when the waveguide has a width of two free space wavelength [130].

As a result, antennas based on dielectric waveguides tent to have large cross-sections, and difficult to assemble in bi-dimensional configurations as the ones aimed to in Fig. 1.6b, where each antenna needs to be spaced less than $\lambda_0/2$ from the adjacent one.

3.2 Process overview

Two process technologies were developed at the Dimes T.C. in Delft and at Philips MiPlaza lab in Eindhoven for integrating metallic waveguides on high-resistivity silicon wafers [131]. Both processes are based on substrate transfer techniques [86] and silicon etching [132], allowing to realize waveguides for easy interfacing with planar ICs and with continuous metallic side walls. The manufacturing steps make use of conventional photo-lithographic techniques, with a minimum feature size of 0.5 μm and a limited number of masks (i.e., three); the high resolution of the process opens up the possibility to design a number of passive components as planar interconnections (chapter 3) and transitions (chapter 4) for flip chip assembly (chapter 6), slotted waveguide arrays (chapter 5), passive beam forming networks (chapter 6). The use of substrate transfer technology separates the role of the material where the structures are realized from the substrate that acts as a mechanical carrier [133], allowing to perform continuous thru-wafer etching (rather than only discrete vias) to define the waveguide cross-section. Waveguides can be then implemented using high resistivity silicon as dielectric in order to reduce losses, while a different substrate (e.g., glass or silicon) is employed to support the structures.

Two types of etching process were investigated, which lead to waveguides with different cross-sections. In the first approach, prof. Ronald Dekker and Pascal de Graaf employed a potassium hydroxide solution [134, 135] to etch the silicon at Philips MiPlaza lab . Since the etching is not isotropic but proceeds (faster) along preferred crystallographic planes, the resulting waveguide cross-section is trapezoidal, with the side walls tilted of 35.3° with respect to the vertical direction (see Fig. 3.1a). In the second solution, the technology was improved at the Dimes T.C. by prof. Lis K. Nanver and Vladimir Jovanović to enhance the anisotropy of the etching: the KOH etching of silicon was replaced by a deep reactive-ion-etching [136]



(a) (b)

Figure 3.1: Cross-section of a: (a) KOH and (b) DRIE etched waveguide.

(i.e., plasma etching), leading to waveguides with perfect vertical side walls and a rectangular cross-section (see Fig. 3.1b).

DRIE etching, when compared to KOH, achieves a superior control of the geometrical dimensions of the structure since sharp convex corners can be etched at a rate independent of the crystallographic orientation of the wafer and without the need of corner compensating structures [137] (see section 3.3.1). Nevertheless, the realization of perfectly vertical side walls poses a technological challenge for the waveguide metallization, mostly when high AR (height over width close to one) trenches are considered. For this reason, KOH-etched waveguides were developed first in order to prove the possibility to integrate low loss waveguides at millimeter waves.

3.2.1 MiPlaza wet (KOH) etching process

The manufacturing flow of KOH etched structures begins with a high resistivity (e.g., 0.7-1.3 kΩ·cm) <100> oriented silicon wafer which is grinded back and wet damage etched until the desired height (half of the waveguide average width). Next, 50 nm of low-stress low-pressure chemical vapor deposition (LPCVD) nitride is deposited, and 1 μm of Al is sputtered, constituting the bottom metallization of the waveguide. The aluminum is then removed from the edge of the wafer and two layers of respectively 0.5 μm plasma-enhanced chemical vapor deposition (PECVD) nitride and 0.5 μm PECVD oxide are deposited (Fig. 3.2a). The silicon wafer is glued [138], top-down, to a 525 μm thick glass carrier, which provides the required mechanical support for the following steps. The stack composed by the silicon and the glass wafers is flipped upside-down and the new front side is further processed. The nitride layer is patterned on the exposed side (Fig. 3.2b) and the silicon is wet etched using a 33% KOH solution (Fig. 3.2c); the etching angle is 35.3° with respect to the vertical direction [134]. Next a 1 μm-thick layer of Al is sputtered to implement the top horizontal and side

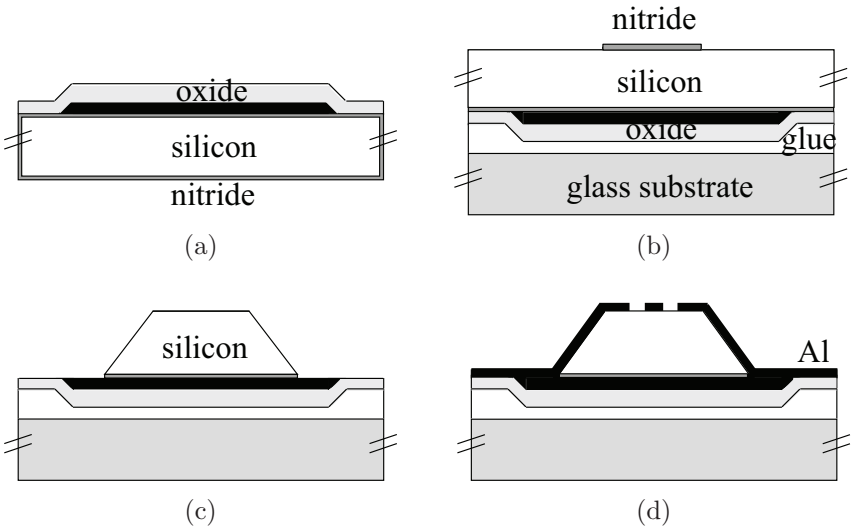


Figure 3.2: KOH waveguide, technology steps: (a) after aluminum deposition, (b) the silicon wafer is glued top-down to a glass carrier; the waveguide side walls are then (c) etched and (d) metallized.

walls of the waveguide. To complete the process, the top aluminum layer is patterned (Fig. 3.2d) by using resist spray coating, followed by contact lithography and wet chemical etching.

3.2.2 Dimes T.C. plasma (DRIE) etching process

The process flow of DRIE etched structures is sketched in Fig. 3.3. Starting from an n^- high-resistivity silicon substrate ($\rho > 1000\Omega$·cm), the first metal deposition (4 μm of Al) is sputtered on the top side of the wafer and patterned using the first mask (Fig. 3.3a). The back side of the wafer is fully metalized and bonded to a silicon carrier for mechanical support (Fig. 3.3b). The DRIE is then performed on the openings selected by the second process mask (e.g., trenches): the plasma beam etches through the whole silicon substrate and lands on the oxide (Fig. 3.3c). The oxide at the bottom of the trench is removed, and a second layer of thicker metal (4 μm of Al) is sputtered on the top face including the side walls (Fig. 3.3d) making contact to the first (top) and to the bottom metal layers. A metal coverage on the side walls of 1.9 μm near the top face and 0.5 μm near the bottom face of the trench is obtained, as shown in Fig. 3.4. A small tilt angle of the side walls of 0.36° was measured.

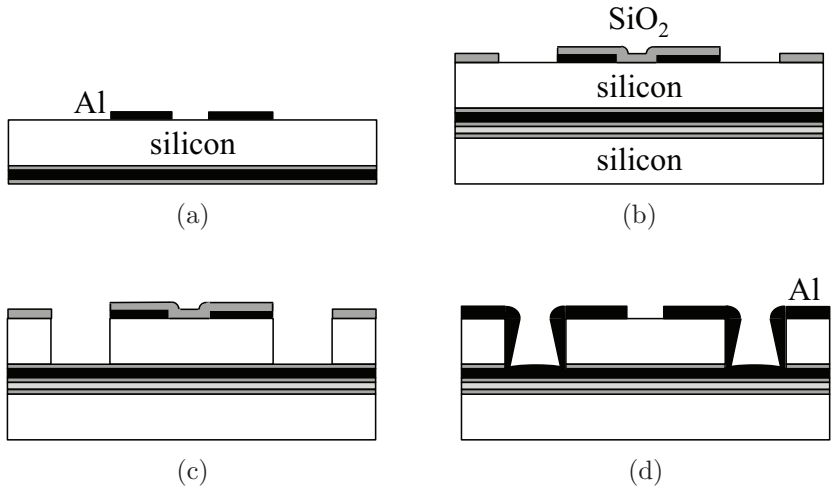
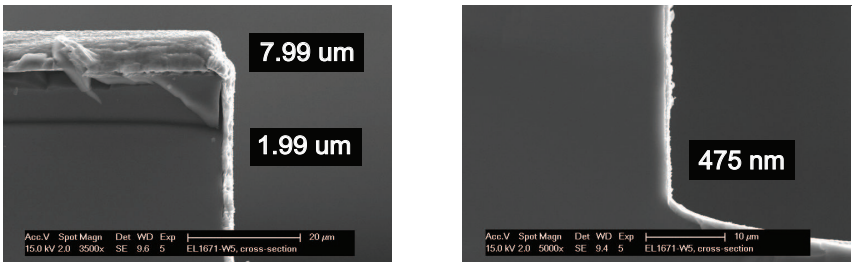


Figure 3.3: DRIE waveguide, technology steps: (a) first deposition and patterning of the thin top metal, and deposition of the back metal, (b) gluing of the wafer to a mechanical carrier (e.g., silicon dummy wafer) and patterning of the oxide, (c) silicon etching, (d) second thick metal layer deposition and patterning.

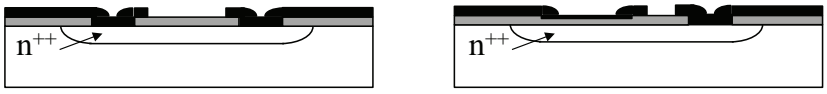
Note that the metallization is performed in two steps: a (thin) first layer, deposited before the DRIE, is used for high resolution planar structures (e.g., transitions and slot antennas), while a (thick) second layer, deposited after the DRIE, ensures metal coverage on the side and bottom of the waveguide trench. Such a two-step metallization is preferable as a one-step process would require (after metal deposition) the use of a thick photo-resist layer, which limits the patterning resolution, to protect the metal on the trench side walls while patterning the metal on the waveguide top face.

Resistors and capacitors can be integrated by adding few steps at the beginning of the process. First, a layer of thermally-grown silicon dioxide is used to preserve the interface between the Si substrate and the first Al layer clean. For a resistor (see Fig. 3.5a), a high-dose of phosphorus is implanted and annealed, which produces the n^{++} channel of the diffused resistance. To integrated the capacitor, the initial silicon dioxide is used as dielectric ($\epsilon_r = 3.9$) of a metal-oxide-semiconductor (MOS) capacitor over the n^{++} region (see Fig. 3.5b). A resistance of $6.8\Omega/\square$ and a capacitance 0.86 $\mathrm{fF}/\mu\mathrm{m}^2$ (oxide thickness 42 nm) were measured. The integration of such components is crucial when targeting the realization of complex waveguide designs to be



(a) (b)

Figure 3.4: Metal coverage (in white) of the waveguide side walls: (a) top and (b) bottom of the etched trench.



(a) (b)

Figure 3.5: Process modification for including: (a) a diffused resistor or (b) a MOS capacitor.

used in real systems: matched load resistances are required to implement travelling wave arrays, simplifying the design process and increasing the antenna operational bandwidth, while low loss capacitors are needed as by-pass capacitances, difficult to integrate on the silicon chips due to the stringent electrostatic discharge (ESD) rules and large area occupancy.

3.3 Design of integrated waveguides

Conventional rectangular waveguides employ the TE_{10} as the fundamental mode of operation, and simple design equations to dimension the structure can be found in literature [139]. The width of the waveguide w determines the cut-off frequency f_{co} of the first propagating mode:

$$f_{co} = \frac{c_0}{2w\sqrt{\epsilon_r}} \tag{3.1}$$

Depending whether the height is smaller or larger than half the waveguide width, the first higher order mode is the TE_{20} or the TM_{01}, respectively. For a height to width AR equal to 0.5 instead, the cut-off frequencies of these two modes coincide, hence maximizing the low loss frequency range where only the fundamental TE_{10} mode propagates.

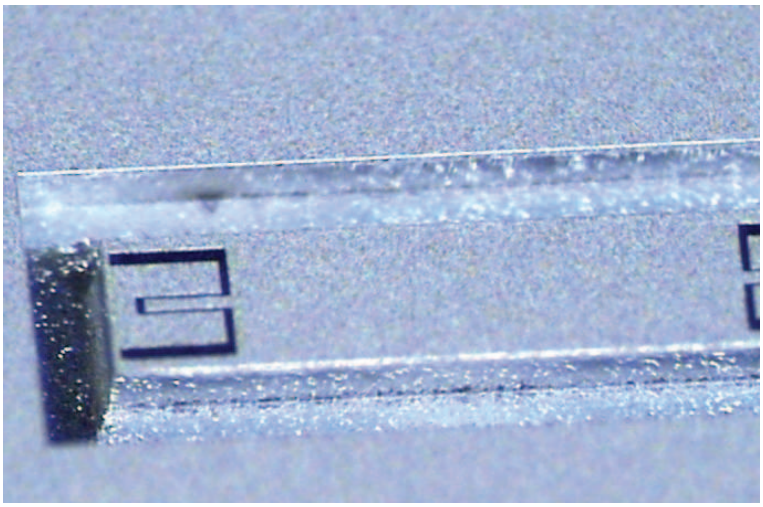


Figure 3.6: DRIE waveguide, camera picture. The silicon substrate has been removed all around the waveguide; metal is in light grey, while in black a slot transition from coplanar to waveguide (see chapter 4) is also visible.

Waveguides manufactured with the DRIE process of section 3.2.2 and operating in the W-band were realized, with a height of 280 μm and a width of 560 μm, resulting in a cut-off frequency of 77 GHz; design parameters are reported in Table 3.1). Fig. 3.6 shows a camera photo of the structure: the waveguide is filled with high-resistivity silicon (i.e., 0.7-1.3 kΩ·cm) and surrounded by a trench with an AR of 1.5 (note this is the AR of the trench, not of the waveguide cross-section). The structure is enclosed by continuous metallic walls which guarantee a high field confinement: the minimum aluminum coverage, occurring at the bottom of the trench side walls, is 0.5 μm (skin depth 0.259 μm at 100 GHz) and gives rise to a worst case power leakage through metal of $exp^{-0.5/0.259} = 2\%$ at 100 GHz (assuming the currents on the outer face of the waveguide radiate all the power they carry). Due to the relatively high dielectric constant of silicon (i.e., $\epsilon_r = 11.9$), the propagating wavelength and the geometrical dimensions are reduced by a factor larger than 2 when compared to air-filled waveguides.

When waveguides are manufactured with the KOH process described in section 3.2.1, the structures of Fig. 3.7 are obtained: the photo shows the waveguides on top of the glass wafer, where the surrounding silicon has been etched away.

Table 3.1: Design parameters of a DRIE waveguide.

width (μm)	560
height (μm)	280
cut-off frequency (GHz)	77
metal thickness: top face (μm)	8
metal thickness: top side of trench (μm)	1.99
metal thickness: bottom side of trench (μm)	0.475
skin depth (μm)	0.25[1]

[1] at 100 GHz

KOH waveguides should be designed to work with their fundamental TE_{10} mode defined by eq. 3.1. As no design equations are available in literature for waveguides with a trapezoidal cross section, a numerical study based on Ansoft HFSS software of the modes propagating in the structure was carried out. Simulation results of the electric and magnetic fields in the cross-section show that a trapezoidal waveguide (TWG) exhibits the same cut-off frequency of an equivalent rectangular waveguide (ERWG) with equal height and width w_e given by:

$$w_e \approx \frac{w_t + w_b}{2} \tag{3.2}$$

where w_t and w_b represent the width of the top and bottom face, respectively (see Fig. 3.8a). The simulated cut-off frequency of the fundamental mode for the trapezoidal waveguide is very close to the one of the ERWG (relative error smaller than 0.6 %, see Fig. 3.8b), while the mono-modal frequency bandwidth and the the first higher order mode cut-off depend on the waveguide AR, as discussed in section 3.4.

For a fixed cut-off frequency, a trapezoidal waveguide is dimensioned in the following way [140]: w_e is calculated from eq. 3.2, the substrate height H is set to half of w_e, and the widths w_t and w_b are found from geometrical considerations:

$$w_t = w_e - H\, tg\, \alpha \tag{3.3}$$

$$w_b = w_e + H\, tg\, \alpha \tag{3.4}$$

where α=35.3° is the tilt angle of the side walls.

To show the possibility of frequency scaling, three samples of waveguide with different cut-offs were realized on the same silicon wafer, with the

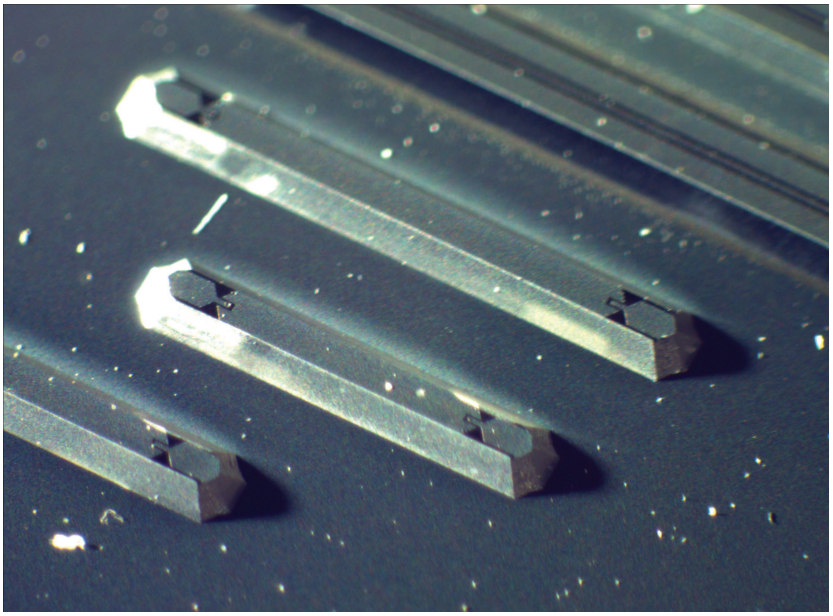
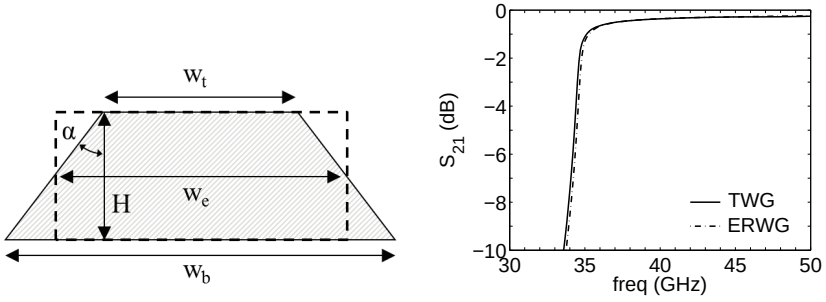


Figure 3.7: KOH waveguide, camera picture. The trapezoidal cross-section of the waveguides is clearly visible; a slot transition (in black) from coplanar to waveguide is opened in the top face metallization. Corner compensating structures were used, as explained in section 3.3.1.



(a) (b)

Figure 3.8: KOH trapezoidal waveguide and its rectangular equivalent: (a) cross-section and (b) simulation. In (a), the difference in the cut-off frequencies is 0.15 GHz.

Table 3.2: Geometrical dimensions of three KOH waveguides with different aspect ratios.

waveguide	I	II	III
cut-off frequency (GHz)	35	50	77
top width w_t (μm)	1040	670	360
bottom width w_b (μm)	1440	1070	760
rectangular equivalent width w_e (μm)	1240	870	560
substrate heigth H (μm)	290	290	290
aspect ratio (H/w_e)	0.23	0.33	0.52

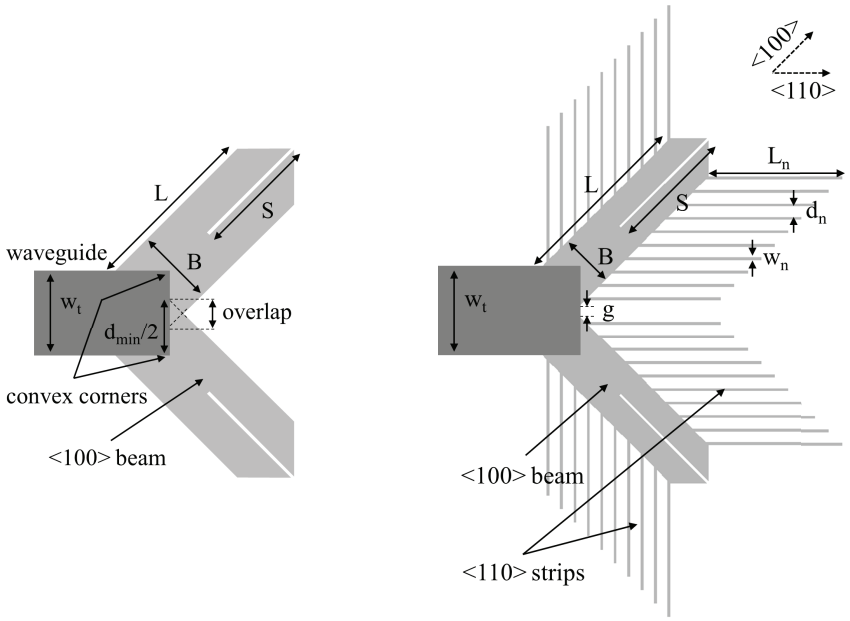
Table 3.3: Dimensions (in μm) of the corner compensating structures.

waveguide top width w_t	360
substrate thickness H	290
safety space g	20
beam length L	722
beam width B	240
slit length S	553
strip length L_n	495
strip width w_n	10
strip spacing d_n	10

dimensions reported in Table 3.2. Due to technology limitations, the height of the substrate H was kept constant to 290 μm rather then properly scaled with the waveguide width w_e (i.e., H=0.5w_e), resulting in only Waveguide III (see Table 3.2) being designed with an AR close to the optimum value of 0.5.

3.3.1 Corner compensation

To employ the KOH technology for the design of waveguide structures, the different etching rates of the silicon planes, which depend on their cristallographic orientation, needs to be accounted for. Waveguides were manufactured using <100> silicon wafers and the etching mask was aligned along



(a) (b)

Figure 3.9: Waveguide: (a) with <100> slit beam, (b) the proposed design with <100> slit beam and <110> delay strips; the <100> and <110> directions are also reported.

that direction. Starting from the top face of the wafer, the silicon crystallographic planes are removed during the KOH step with different speeds according to their orientations, and under-etching occurs at the four convex corners of the waveguide (see Fig. 3.7) due to the emergence of fast etching planes [137]. This results in poor control of the shape and size of the final structure. To improve the geometrical definition, extra features called compensating structures are usually added in the etching mask to each convex corner in order to enlarge its physical extension, thus delaying the moment the corner is exposed to the etchant.

In literature, many examples of such structures [137] are reported, all requiring a considerable amount of free space around the corner. Consider for instance the <100> oriented beam with a slit in the middle [137, 141] (see Fig. 3.9a): for a thru-wafer etching, the width of the beam has to be twice the substrate thickness. For this reason, the minimum distance d_{min} between two adjacent corners, required to avoid overlap of the compensating

structures, cannot be smaller than:

$$d_{min} = 2\sqrt{2}H \tag{3.5}$$

where H is the substrate thickness. Unfortunately such structures cannot be used on the short side of a trapezoidal waveguide since d_{min} is always bigger than the distance between the two corners w_t=H(2-tgα) (with w_e=2H in eq. 3.2) and would cause the overlap between the two beams. As example, for a 77 GHz cut-off KOH waveguide on a 280 μm silicon wafer, the top metallization is 360 μm wide while the slit beam would require a d_{min} of 425 μm. For this reason, a new design of corner compensating structure was considered.

Since the width of the <100> oriented beam is limited by the width of the waveguide top face, narrow <110> strips are added to act as delay elements. The motivation is to compensate the reduced width of the <100> beam with other elements, namely the strips, to postpone the moment at which the KOH solution starts etching it. Considering Fig. 3.9b, where w_t is the top metallization width of the waveguide and B the beam width, if defining g as a safety spacing to leave between two adjacent corner compensating structures, then the following equations apply:

$$B = \frac{w_t - g}{2} \cdot \sqrt{2} = \frac{w_t - g}{\sqrt{2}} \tag{3.6}$$

$$S = 2H \tag{3.7}$$

$$L_n = \frac{2H - B}{2} \cdot V \cdot 1.03 \cdot 1.94 = (H - \frac{B}{2}) \cdot V \cdot 1.03 \cdot 1.94 \tag{3.8}$$

$$L = 2H + (V - 1) \cdot H = (V + 1) \cdot H \tag{3.9}$$

where S is the slit length, L_n the strip length, V the etching ratio of the <411> to the <100> direction, L the <100> oriented beam length. The factor 1.03 takes into account the inclination of the {411} with the vertical planes, and the factor 1.94 the angle between the {411} and the {010} planes [137]. The strip width and spacing are not mentioned in the above equations and need to be optimized with a numerical simulator. The strips have to be dense enough to protect the <100> beam for a sufficient time in order to compensate for its reduced width, but also very thin to avoid the formation of a residue at the bottom of the substrate.

Table 3.3 shows all the dimensions of the proposed structure for a KOH waveguide with cut-off at 77 GHz. In Fig. 3.10 the results of a process simulation carried out with ACES software [142] are reported, where the waveguide corner is showed at different instants of the etching process. Starting

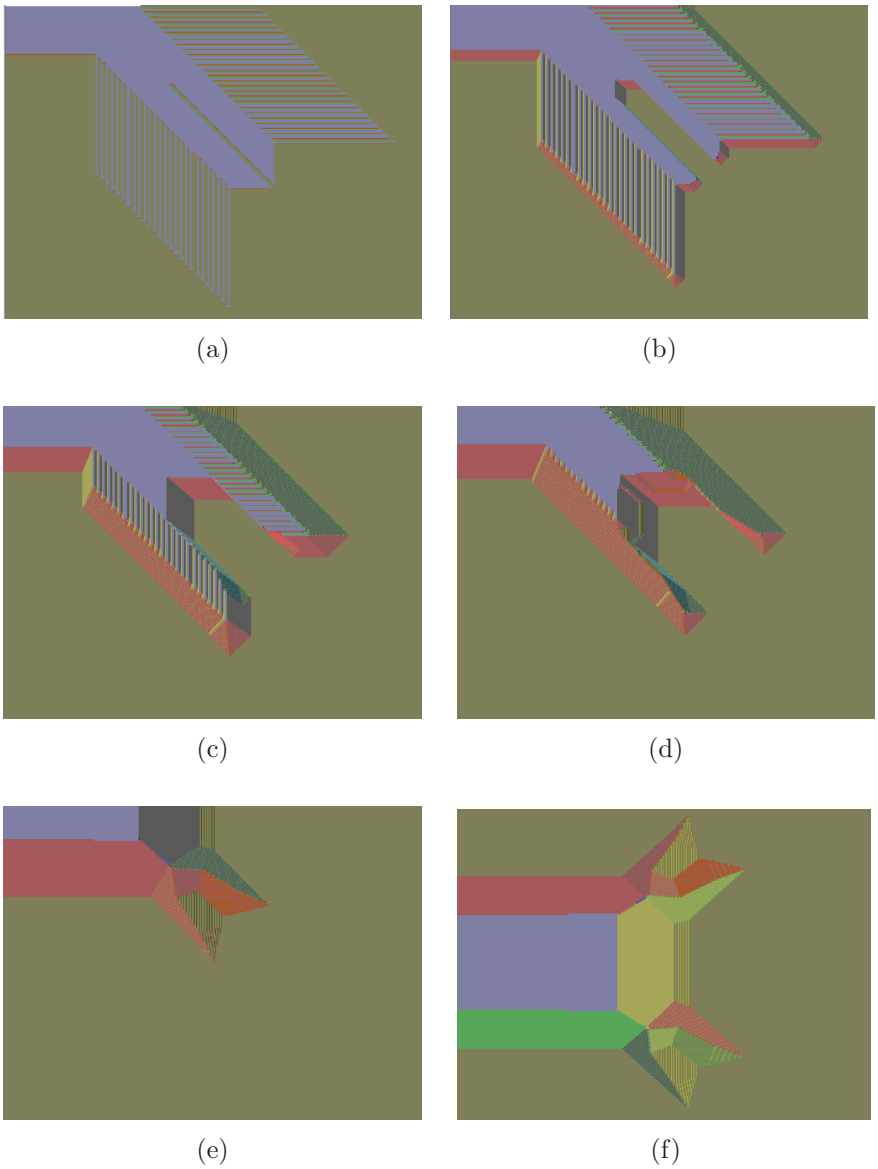
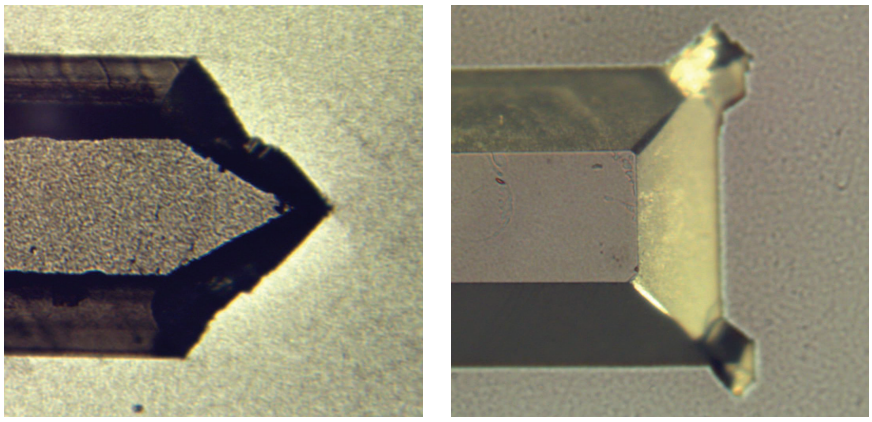


Figure 3.10: ACES simulation of the proposed corner compensating structure as the etching proceeds: (a) the initial structure with the corner compensating mask, (b) the etching starts along the slit and the strips, (c) the slit is completely opened, (d) the strips are consumed, (e) the etching is completed and a small residue is visible at the bottom of the substrate. A top view of the final waveguide corners is given in (f).

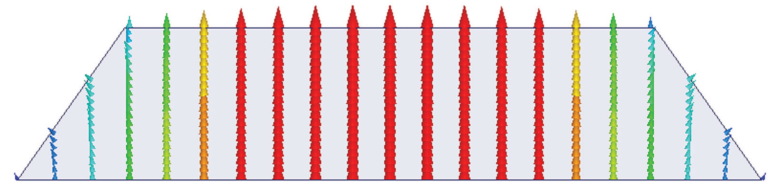


(a) (b)

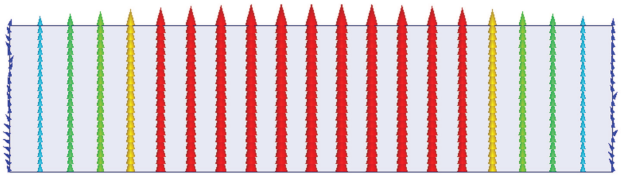
Figure 3.11: Comparion of a waveguide: (a) without and (b) with the proposed corner compensating structure.

from the protected corner (Fig. 3.10a), the etching first takes place in the slit along the <100> direction and in the delay strips along the fast-etching <411> direction (Fig. 3.10b); when the slit (Fig. 3.10c) and the strips (Fig. 3.10d) are completely consumed, the etching proceeds along the <100> oriented beams until it reaches the convex corner (Fig. 3.10e). The advantage of using narrow (rather than large) delay strips is that they are etched along the <411> direction at their convex corners, leaving a <100> oriented residue in Fig. 3.10d at the bottom of the substrate (large strips would leave a <110> oriented residue) that is effectvely removed during the etching of the <100> oriented beam.

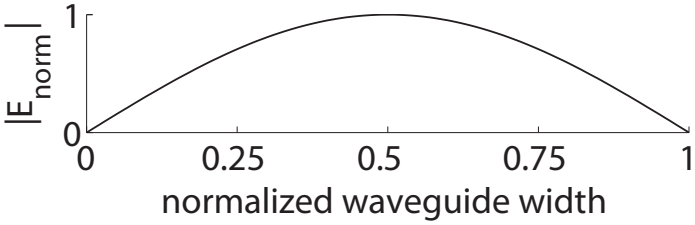
A comparison of waveguide corners realized without and with the compensating structures is reported in Fig. 3.11: without protections, the corners are etched away and the waveguide has a triangular shape (Fig. 3.11a). When the proposed structures are used (Fig. 3.11b) the convex corners are very sharp, forming a 90° angle on the top side of the waveguide and with almost no residue visible at the bottom of the waveguide.



(a)



(b)



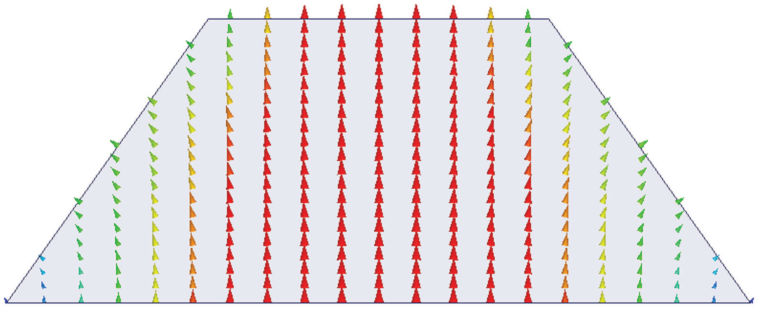
(c)

Figure 3.12: Electric field distribution of the fundamental (i.e., TE_{10}-like) mode for: (a) Waveguide I and (b) its ERWG; (c) ideal TE_{10} normalized electric field amplitude.

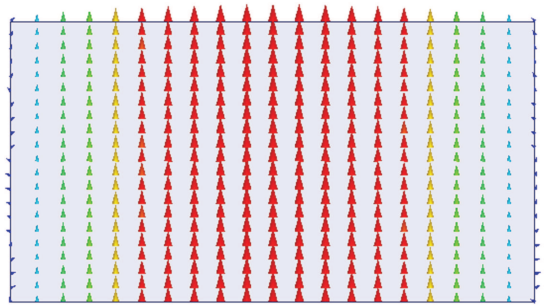
3.4 Numerical modal analysis of KOH waveguides

In order to analyze the modal behaviuor of KOH trapezoidal waveguides two structures from Table 3.2 were considered: Waveguide I with an AR smaller than 0.5, and Waveguide III an AR larger than 0.5.

Simulations of the electric fields in Waveguide I and III, together with their ERWG (see eq. 3.2), are reported in Fig. 3.12 and 3.13, respectively.



(a)



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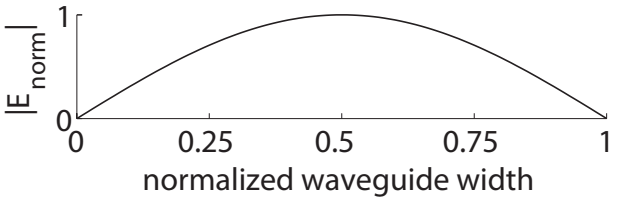


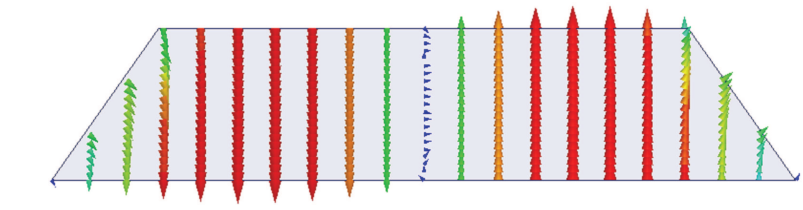
(c)

Figure 3.13: Field distribution of the fundamental (i.e., TE_{10}-like) mode for: (a) Waveguide III and (b) its ERWG; (c) ideal TE_{10} normalized electric field amplitude.

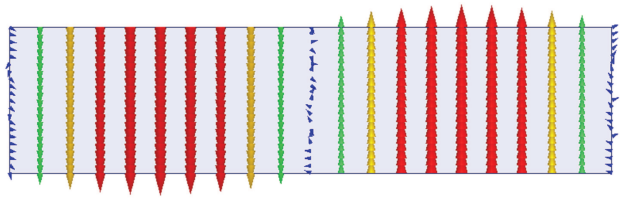
Comparing the field distributions of TWGs in Fig. 3.12a and 3.13a with their ERWG in Fig. 3.12b and 3.13b shows a similar pattern in the center region of the cross-section, independently of the aspect ratio. Minor differences are observed close to the lateral side walls: the trapezoidal shape of the walls creates a twist in the field direction because the field tangential component is always zero due to the boundary condition on a perfect metal. However, the contribution of the side wall region to the total power is very small, since in this region the electric field is zero (for RWGs) or close to zero (for TWGs). The above argument indicates that the field distribution of the two trapezoidal waveguides shows strong resemblances, mostly everywhere in the cross-sectional area, to the field of their equivalent rectangular waveguide, allowing the definition of a fundamental TE_{10}-like mode propagating in a TWG, regardless of the aspect ratio. Furthermore, HFSS simulations showed that the cut-off frequency of this TE_{10}-like mode is the same as the TE_{10} of the equivalent rectangular waveguide (see section 3.3).

Different considerations apply for the first higher order mode propagating in the waveguide. Depending on the aspect ratio, the TWG may exhibit a significantly different modal behaviour from the ERWG. Rectangular Waveguide I has an aspect ratio smaller than 0.5: the first higher order mode to be excited is therefore the TE_{20} (see Fig. 3.14b). The electric field has a sine variation along the horizontal direction, with two peaks (close to the side walls) and three nulls (two at the side walls, one in the center). Trapezoidal Waveguide I shows a similar behaviour (see Fig. 3.14a): since the aspect ratio is much smaller then 0.5, the two peaks of the electric field are situated far from the side walls. For these reasons, considerations analogous to those made for the fundamental propagating mode (e.g., TE_{10}) apply, and the first higher order mode in trapezoidal waveguides with aspect ratio smaller than 0.5 can be regarded as a TE_{20}-like mode.

Rectangular Waveguide III has an aspect ratio larger than 0.5: the first higher order mode to be excited is the TM_{01} (see Fig. 3.15b). The electric field is uniform in the horizontal direction, and shows a half-a-sine variation in the vertical direction. Trapezoidal Waveguide III presents a different scenario (see Fig. 3.15a): at the center of the waveguide along the vertical direction, the mode has a half-a-sine variation, as the rectangular TM_{01} mode does, but on the bottom face along the horizontal direction the mode shows a sine variation, resembling more a TE_{20}-like mode. HFSS simulations showed that the first higher order mode is excited at 123 GHz, which does not correspond neither to a TE_{20} nor a TM_{01} mode. As consequence of an aspect ratio close to 0.5, the field distribution is strongly perturbed with respect to the ERWG, since both the TE_{20} and the TM_{01} have a peak of the electric field very close to the side walls, where the vector is rotated



(a)



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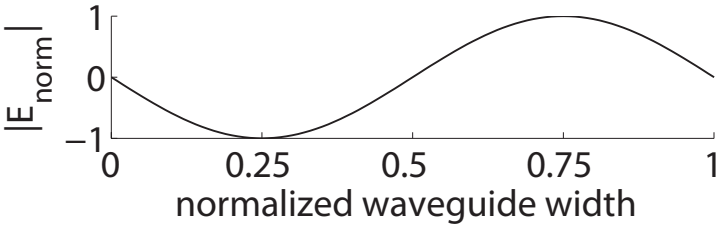
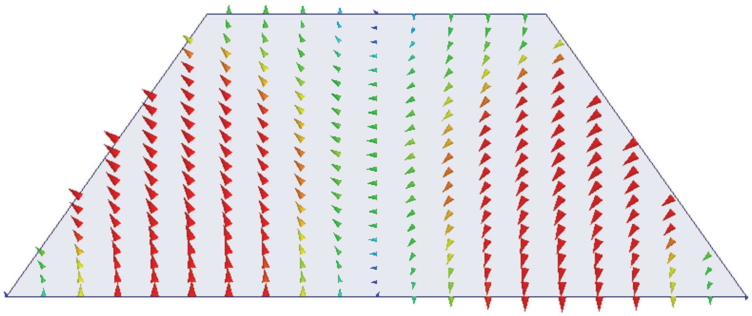


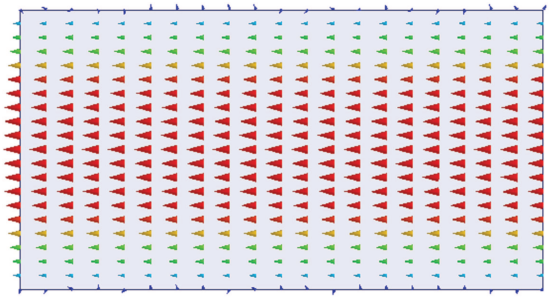
(c)

Figure 3.14: Field distribution of the first higher (i.e., TE_{20}-like) mode for: (a) Waveguide I and (b) its ERWG; (c) ideal TE_{20} normalized electric field amplitude.

because of the trapezoidal cross-section. Thus, no TE_{20}-like nor TM_{01}-like modes can be defined if the aspect ratio is close or higher than 0.5: the first higher order mode has no rectangular equivalent, and its cut-off frequency has to be evaluated from numerical simulations.



(a)



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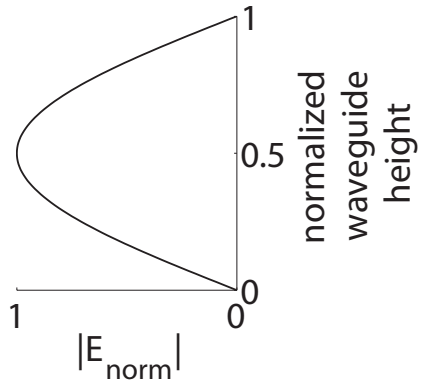


(c)

Figure 3.15: Field distribution of the first higher order mode for: (a) Waveguide III and (b) its ERWG; (c) ideal TM_{01} normalized electric field amplitude.

3.5 Measurement results

In this section, experimental results of KOH and DRIE etched waveguides are presented. The structures were characterized by means of their S-parameters measured by an Agilent E8361C Performance Network Analyzer (PNA) [143] with mm-wave module extensions to cover the 67-110 GHz band. Measurements up to 125 GHz were carried out using waveguide Tx-Rx modules provided by Anritsu [144]. The waveguides were connected to the coplanar measurement environment using the transition described in chapter 4, and the signal was delivered to the integrated structures using Cascade Microtech 110 GHz Infinity probes [103]. To remove the load of the transitions and extract the parameters of the waveguide (phase and attenuation constants), a de-embedding algorithm based on two waveguide sections with different lengths (L_1-L_2 de-embedding [145–147], see appendix C) was applied.

Simulations were carried out with HFSS software, setting the aluminum metal thickness to 1 μm and the bulk resistivity of the silicon substrate to 1250 Ω·cm; the propagation constant is extracted from the de-embedded S-parameters using the equations reported in [148].

3.5.1 KOH waveguide

Waveguides with three different cut-off frequencies were implemented and measured to validate the simulation prediction and performance. All the structures were manufactured on the same substrate and therefore have the same height, as reported in Table 3.2. Applying the L_1-L_2 de-embedding, the waveguide propagation constant $\gamma=\alpha+j\beta$, α and β being the attenuation constant and phase constant, respectively, was extracted from the measured S-parameters. The dispersion diagram (wave number β versus frequency) in Fig. 3.16a strongly matches the behaviour of the simulated ERWGs, where an equivalent width given by eq. 3.2 was used. Insertion losses are shown in Fig. 3.16b-d: above the cut-off, very low average losses of 0.1 dB/mm at 50 GHz and 0.2 dB/mm at 100 GHz are observed. The good agreement between ERWG simulations and TWG measurements confirms the possibility of defining a TE_{10}-like mode for trapezoidal waveguides independently from their aspect ratio.

The oscillations larger than 0.1 dB visible in Fig. 3.16b are caused by three factors. First, the de-embedding algorithm assumes that the four transitions, two for each structure, are identical (see appendix C), while this is not the case due to process inhomogeneities (this problem is described in more details in section 4.4.2). These differences result in an impedance and

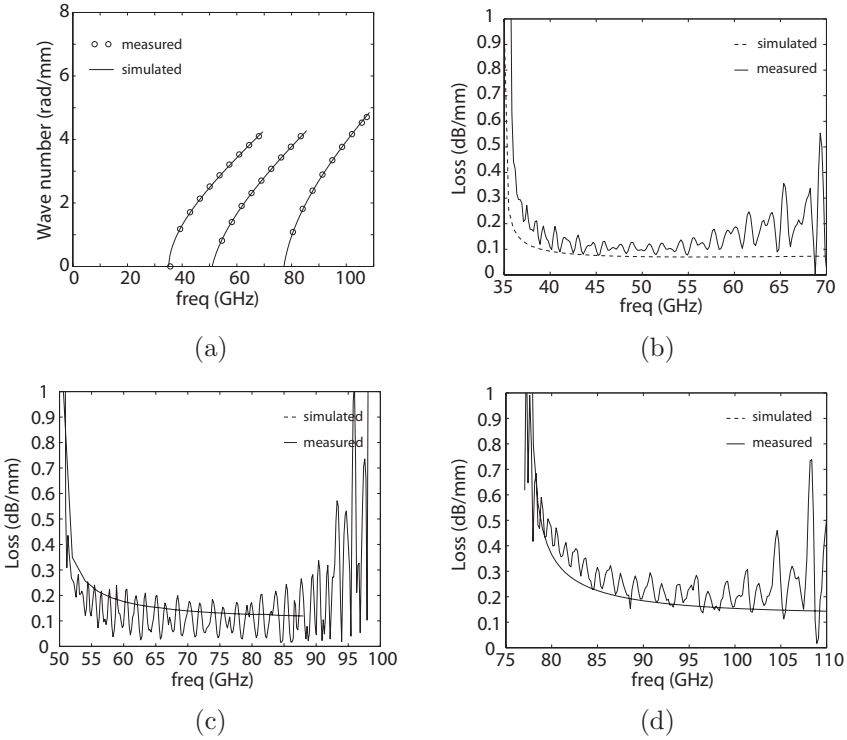


Figure 3.16: KOH waveguide, simulations (ERWG) versus measurements (TWG): (a) dispersion diagram and (b)-(d) losses for Waveguide I, II and III, , expressed as $10log_{20}(e^{-2\alpha d})$, choosing d = 1 mm.

length mismatch among the structures, producing a residual fluctuation in the de-embedded traces. Moreover, probe misplacement (i.e., landing accuracy in the order of ± 10 μm) at around 90GHz contributed to a random phase error between the structures. Finally, the waveguide losses are in the order of the calibration accuracy (i.e., $\pm$ 0.1 dB), which tends to expand the ripple intensity after the de-embedding step.

An overview of the waveguide performances is reported in Table 3.4. The ratios of the guided wavelengths in the silicon-filled and in an air-filled waveguide with the same cut-off frequency are greater than 2 as a result of to the high dielectric constant of the substrate used.

Table 3.4: Summary: KOH waveguide measurement results.

waveguide	I	II	III
mono-modal frequency band (GHz)	35[1]- 70[2]	50[1]- 100[2]	77[1]- 110[3]
average loss (dB/mm)	0.10[4]	0.10[5]	0.20[6]
average loss per wav. (dB/λ_g)	0.24[4]	0.16[5]	0.16[6]
wavelength ratio $\lambda_{g,air}/\lambda_{g,Si}$	2.5[4]	2.6[5]	2.2[6]

[1] cut-off of the fundamental mode (TE_{10}-like)
[2] cut-off of the first higher order mode
[3] maximum measured frequency. The cut-off of the first higher order mode is 123 GHz
[4] at 50 GHz
[5] at 75 GHz
[6] at 100 GHz

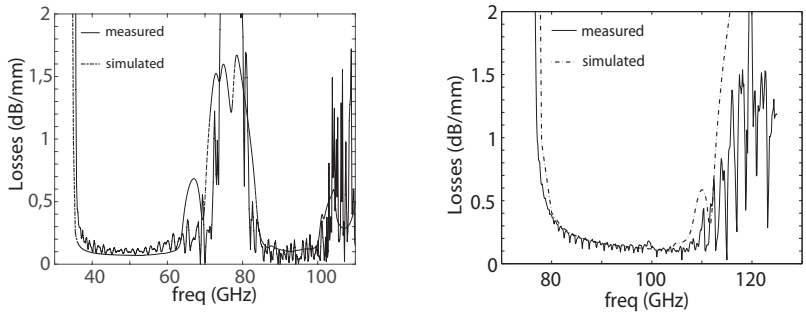
3.5.2 Validation of the modal analysis

To validate the modal analysis described in section 3.4, Waveguide I and III of Table 3.2 were analyzed inside and outside the mono-modal frequency range. Lumped rather than wave ports were used in simulation in order to excite at each frequency all modes propagating inside the waveguide and extract the total attenuation constant.

Fig. 3.17a compares the attenuation constant extracted from the measurements with that of its simulated ERWG: the agreement between the measured TE_{10}-like and the simulated TE_{10} mode is very good at and above the cut-off for both structures.

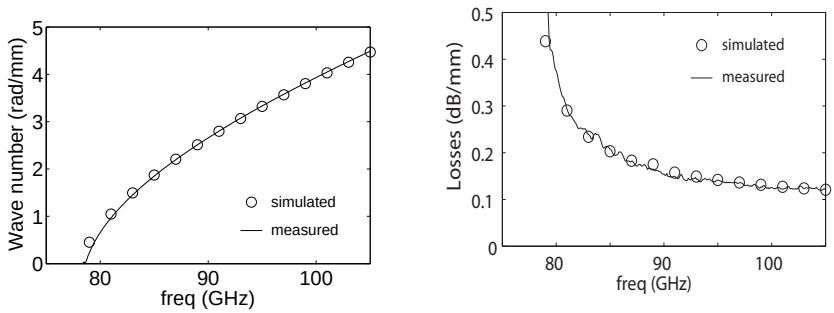
As the frequency approaches the cut-off of the TE_{20}-like mode of Waveguide I (i.e., 70 GHz, double of the fundamental mode), mode coupling between the propagating TE_{10}-like mode and the below cut-off TE_{20}-like mode takes place: as $\gamma=\alpha$ and $\beta=0$ for the TE_{20}-like mode [139], a large amount of reactive energy is stored inside the waveguide and most of the input power is reflected back, causing the peak in the attenuation constant visible in Fig. 3.17a. Well above the TE_{20}-like mode cut-off frequency, the peak disappears as the wave can propagate again inside the waveguide.

Waveguide III has instead an aspect ratio larger then 0.5: the first higher order mode has no rectangular equivalent (for this reason TWGs rather than ERWGs are simulated in Fig. 3.17b) and the behaviour reported in Fig. 3.17b correlates with the simulated cut-off frequency of 123 GHz.



(a) (b)

Figure 3.17: Simulated and measured attenuation constant of the fundamental TE_{10}-like mode for: (a) Waveguide I and (b) Waveguide III. Simulations refers to a TWG fed by lumped ports.



(a) (b)

Figure 3.18: DRIE waveguide, simulations versus measurements: (a) dispersion diagram and (b) insertion loss.

The strong oscillations above 100 GHz in the extracted losses are due to an overmode of the 1 mm coaxial connector (at the wafer probe) generating a standing wave and increasing the calibration error.

3.5.3 DRIE waveguide

For the DRIE waveguide of Table 3.1, the complex propagation constant in Fig. 3.18 extracted from the measured S-parameters shows excellent

Table 3.5: Summary: DRIE waveguide measurement results.

mono-modal frequency band (GHz)	77[1]-110[2]
average loss (dB/mm)	0.12[3]
average loss per wavelength (dB/λ_g)	0.15[3]
wavelength ratio $\lambda_{g,air}/\lambda_{g,Si}$	2.2[3]

[1] cut-off of the fundamental mode (TE_{10})
[2] maximum measured frequency. The expected cut-off of the first higher order mode is 154 GHz
[3] at 100 GHz

Table 3.6: Comparison of the losses in waveguides and integrated transmission lines.

Structure	freq. (GHz)	loss (dB/mm)	loss (dB/λ_g)
SU-8 micro-machined wav. [118]	100	0.13	0.5
Stacked silicon substrates wav. [149]	105	0.042	0.15[1]
Photo-imagable thick-film wav. [119]	100	0.95	1.0
BI-CMOS 130 nm microstrip [26]	100	0.7	1.1
BI-CMOS 130 nm shielded CPW [26]	100	0.7	0.77
Silicon-filled wav. (this work)	100	0.125	0.18
Silicon-filled wav. (this work)	100	0.121	0.15

[1] assuming that in [149] 0.042 dB/mm refers to 105 GHz

agreement with simulations both for the phase as well as for the attenuation constant. At 100 GHz, losses as low as 0.12 dB/mm were measured, corresponding to 0.15 dB/λ_g when normalized to the guided wavelength in a silicon waveguide. Taking advantage of the high dielectric constant of the substrate (ϵ_r=11.9), a guided wavelength reduction of a factor 2.2 at 100 GHz was achieved when compared to an air-filled waveguide with the same cut-off frequency. Table 3.5 summarizes the measurement results of the proposed plasma etched silicon-filled integrated waveguide.

Table 3.6 reports a comparison of millimeter-waves losses of common transmission line topologies such as microstrips, shielded CPWs and waveguides. Apart from stacked silicon substrate waveguides which use air as waveguide dielectric, it is evident that DRIE waveguides show the best losses performance, both per unit length (0.12 dB/mm) and per wavelength unit.

3.6 Conclusions

A new technology was presented that enables the integration of rectangular waveguides at millimeter-waves. Using high resistivity silicon substrates and continuous metallic side walls, integrated waveguides can be manufactured with a low cost process and without the need of any mechanical assembly operation. Two different etching mechanisms were reported, namely KOH and DRIE, and the performances of the resulting structures were compared in terms of their propagating modes and insertion losses. Experimentally, losses of 0.2 dB/mm for a KOH waveguide and 0.1 dB/mm for a DRIE waveguide at 100 GHz were measured.

Chapter 4

Coplanar to waveguide transition

4.1 Introduction

In the last decade, substrate integrated waveguides [28] have gained popularity as low-cost components to implement high quality interconnections [17, 28, 32, 121] and radiating elements [29, 31, 43] at mm-waves. The single conductor nature of SIWs requires to convert the classical quasi-TEM mode delivered from a coplanar or a microstrip environment into the fundamental mode for which the integrated waveguide is designed. To deliver energy to SIW components, electromagnetic coupling has often been employed to design vialess coplanar to waveguide transitions based on transverse resonating slots [66–69]. In [66] the waveguide was kept uniform at the transition (constant width), limiting the maximum length of the transverse slot to half a wavelength (at the cut-off frequency of the waveguide), which resulted in an impedance matching bandwidth of few percent. In [67, 68] a step discontinuity in the waveguide width was introduced at the transition, resulting in an overmoded section but allowing to achieve 40% relative bandwidth. To maintain the waveguide width constant, a tapered slot design was implemented in [69], which however required the patterning of the backs-side metal, thus increasing manufacturing complexity and costs.

In this chapter a CPW to SIW transition based on a U-shaped slot antenna employing a single metal layer with no step discontinuity nor backside patterning is proposed. The transition design methodology is described, critical dimensions are analyzed and empirical design equations are extracted and validated through simulations and experimental results.

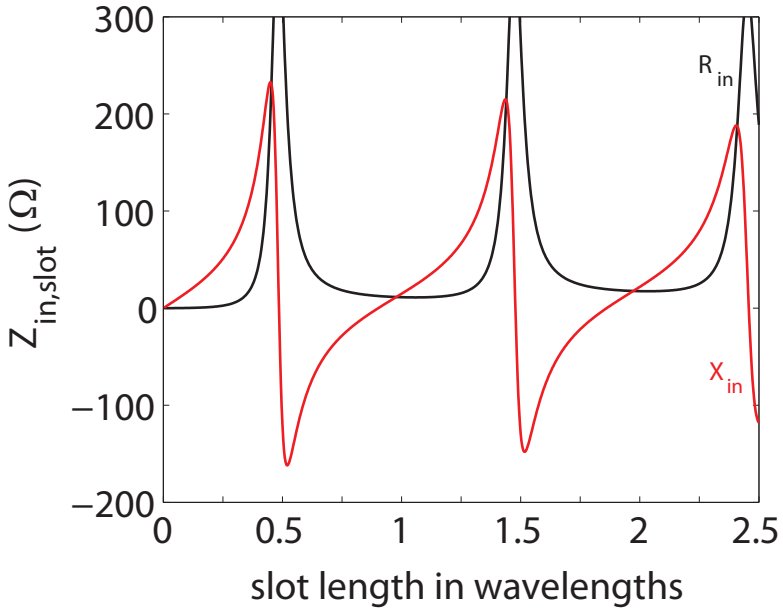


Figure 4.1: Simulated input impedance of a slot antenna as a function of its length. This figure was realized by designing a resonationg slot at 30 GHz in air (gap length: 10 mm; gap width: 20 μm) and sweeping the frequency.

4.2 Ultra-wide band U-shaped slot transition

The proposed CPW to waveguide transition is based on a CPW resonant slot antenna. In order to explain its ultrawide band behaviour and to extract simple design rules, the impedance and the matching bandwidth of a slot antenna need to be first recalled.

4.2.1 Dipole antenna input impedance

Fig. 4.1 shows the input resistance $Z_{in,slot}$ of a slot antenna, including several resonance frequencies (i.e., X_{in}=0 or $X_{in} \rightarrow \infty$). When the slot antenna is half a wavelength long, the input resistance is several hundreds of Ohms: the impedance curve is peaked and the Q-factor (associated to the antenna resonator) is very high, resulting in a narrow resonance bandwidth. On the other hand, when the antenna is one wavelength long, the input resistance is several tenths of ohms: the impedance curve is relatively flat and the Q-factor is low, resulting in a broadband resonance bandwidth and

easy matching to 50 Ω.

4.2.2 CPW to SIW slot transition

For the analysis of CPW to SIW transitions based on coplanar resonating slots, three wavelengths play an important role, namely the waveguide cut-off wavelength λ_{co}, the waveguide guided wavelength λ_g, and the slotline wavelength λ_{slot} [150]:

$$\lambda_{co} = \frac{c_0}{f_{co}\sqrt{\epsilon_r}} \tag{4.1}$$

$$\lambda_g = \frac{c_0}{f\sqrt{\epsilon_r}\sqrt{1-(\frac{f_{co}}{f})^2}} \tag{4.2}$$

$$\lambda_{slot} = \frac{c_0}{f\sqrt{\frac{\epsilon_r+1}{2}}} \tag{4.3}$$

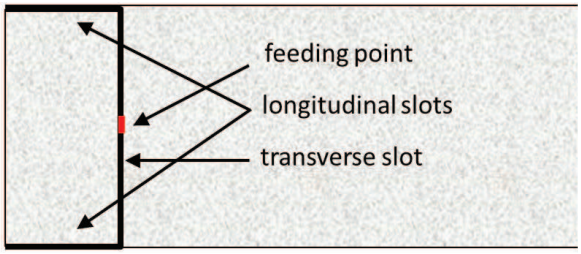
Note that λ_{co} is frequency independent, while λ_g and λ_{slot} decrease with frequency.

With respect to Fig. 4.1, for broadband operations the length of a transverse slot opened in the waveguide broad face needs to be one slotline wavelength λ_{slot} at resonance (second resonance mode). Nevertheless, the maximum length of the transverse slot is limited to $\lambda_{co}/2$ by the waveguide width. The resonance frequency f_r' of the slot occurs when its physical length $\lambda_{co}/2$ is equal to the resonance electrical length λ_{slot}, which by equating eq. 4.1 and 4.3 leads to:

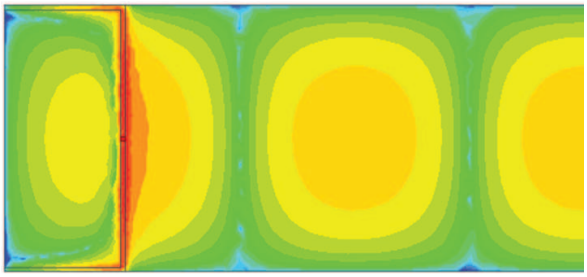
$$f_r' = 2f_{co}\sqrt{\frac{2\epsilon_r}{\epsilon_r+1}} \tag{4.4}$$

Eq. 4.4 shows that f_r' is always greater than $2f_{co}$, the frequency at which the TE_{20} mode starts propagating, resulting in higher losses and mode dispersion.

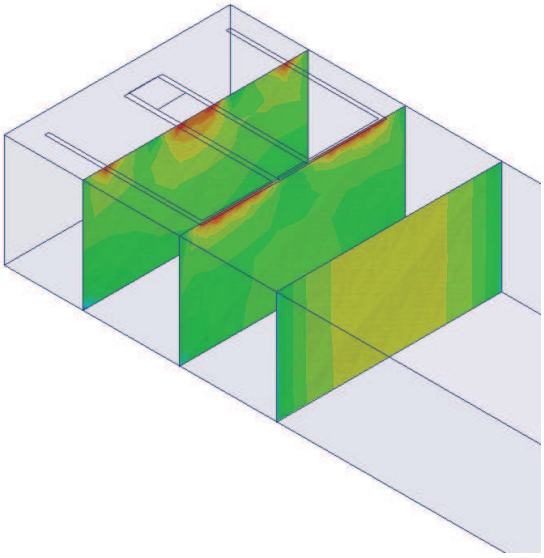
Note that the transition reported in [66] works below $2f_{co}$ because the $\lambda_{co}/2$ long slot is used on its first and thus narrow-band resonance mode (i.e., the slot is $\lambda_{slot}/2$ long), while the λ_{co} long slot used in [67] works on the second ultra-wide band mode (i.e., the slot is λ_{slot} long) but requires a step discontinuity in the waveguide width.



(a)



(b)



(c)

Figure 4.2: (a) layout, top (b) and cross-sectional (c) total electric field magnitude distribution in the coplanar U-shaped slot transition at $\sqrt{2}f_{co}$. The red dot in (a) represents the lumped port excitation; the waveguide is terminated with a wave port on the right side.

4.2.3 U-shaped slot transition

To accomodate a one slotline wavelength long slot on a $\lambda_{co}/2$ wide waveguide within the TE_{10}-TE_{20} waveguide mono-modal band and without introducing any discontinuity, the slot can be 90° bent close to the edges of the waveguide, as in Fig. 4.2a. The resulting slot antenna has a U-shape and can be used to couple energy from a CPW to the SIW. The electric field of the transverse $\lambda_{co}/2$ long slot exhibits a half-a-sine variation along the transverse direction (see Fig. 4.2b); its vertical component at the right edge of the slot(see Fig. 4.2c) matches the half-a-sine variation of the waveguide TE_{10} mode, coupling energy into the SIW. To maximize the coupling the transverse slot needs to be located $\lambda_g/4$ distant from the waveguide end wall, so that constructive interference between the waves propagating back (toward the back reflecting short) and forth (toward the transition transverse slot) occurs. The two parasitic longitudinal (i.e., horizontal) slots are used to increase the total length of the slot antenna to one λ_{slot} wavelength, but do not couple energy into the waveguide since they are located close to the side walls where the waveguide electric field vanishes.

To account for the effect of the longitudinal slots, assume that the longitudinal slots are $\lambda_{co}/4$ each, hence the transverse slot is $\lambda_{co}/4$ distant from the end wall and the total antenna is one λ_{co} long. At the frequency $\bar{f} = \sqrt{2} f_{co}$, the waveguide cut-off and guided wavelengths are equal (equate eq. 4.1 and eq. 4.3), and the transverse slot is properly spaced $\lambda_g/4$ away. Moreover, neglecting the influence of the waveguide side walls on the slot (this hypothesis is removed in section 4.3.2), the resonance frequency f_r of the antenna occurs at $f_r = f_r'/2$ since the slot is twice as long than in eq. 4.4:

$$f_r = \frac{f_r'}{2} = \bar{f}\sqrt{\frac{\epsilon_r}{\epsilon_r + 1}} \tag{4.5}$$

If the term "'+1"' is neglected (the error introduced by this approximation is smaller for higher dielectric constant substrates), then the resonance occurs at $f_r \approx \bar{f} = \sqrt{2} f_{co}$ close to $1.5 f_{co}$, which is at the center of the waveguide mono-modal frequency band.

Summarizing, making each longitudinal slot $\lambda_{co}/4$ long allows to align in the same frequency range, namely close to the center of the TE_{10}-TE_{20} bandwidth, both the frequency $\bar{f}$ at which the coupling of energy into the waveguide is maximized (the transverse slot is spaced $\lambda_g/4$ away from the waveguide end wall) and also the frequency f_r of the second resonance mode where broad impedance matching can be achieved (the total slot length is one λ_{slot}).

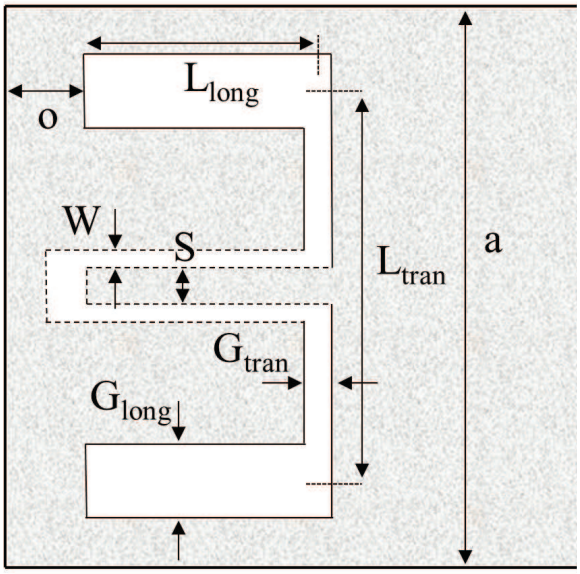


Figure 4.3: Geometrical parameters of the U-shaped slot transition; the dashed line indicates the CPW feed.

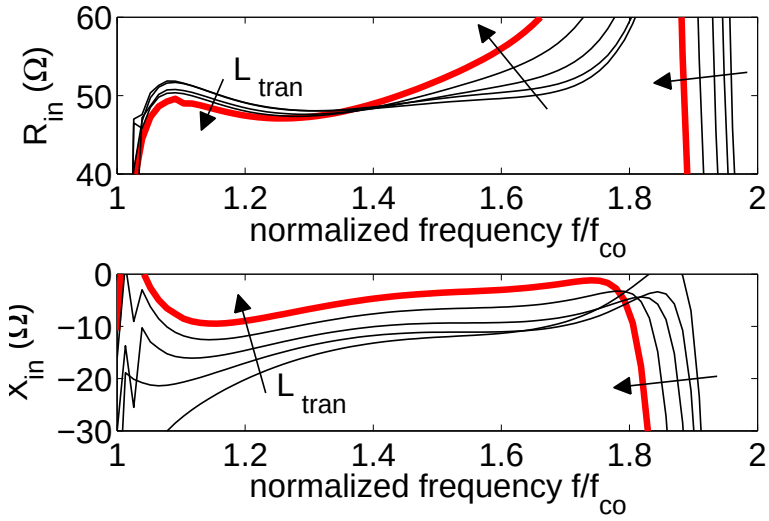
4.3 Analysis of the transition

Using a commercial EM simulator (i.e., Ansoft HFSS), a parametric analysis of the U-shaped slot transition on a waveguide with vertical side walls is carried out, and simple design rules are extraced to relate the slot geometrical dimensions to the transition input impedance $Z_{in} = R_{in} + jX_{in}$.

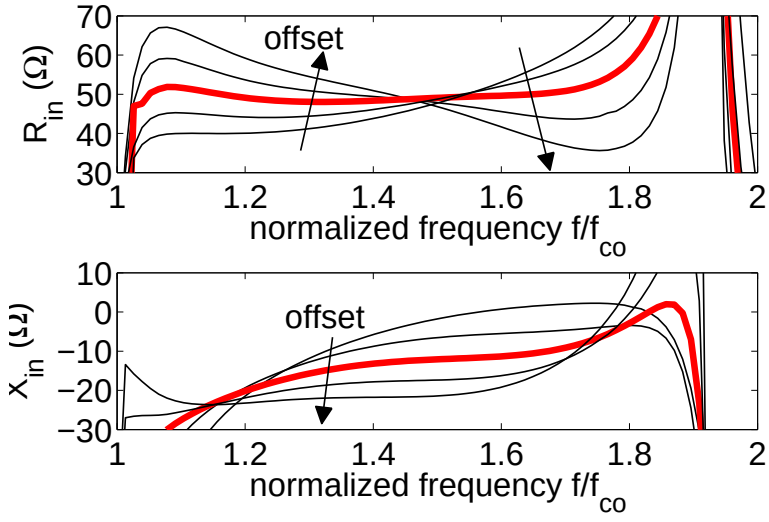
4.3.1 Parametric analysis

The transition design and the parameters analyzed are reported in Fig. 3: the total slot length $L_{tot} = L_{tran} + 2L_{long}$ is kept constant to one slotline wavelength; the 50 Ω CPW line used to feed the slots is excited with a lumped port, and the waveguide is terminated with a wave port on the other side.

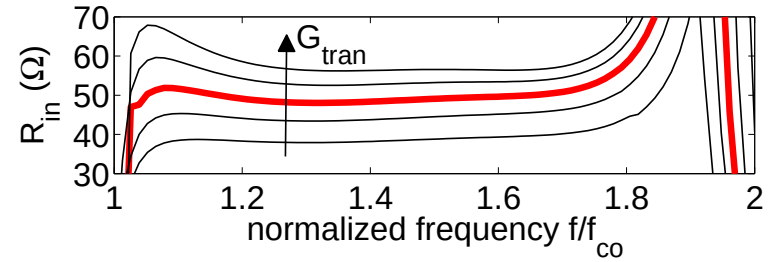
Ideally, the length L_{tran} of the transverse slot should be equal to the waveguide width $a = \lambda_{co}/2$ (see Fig. 3), however in a real structure this

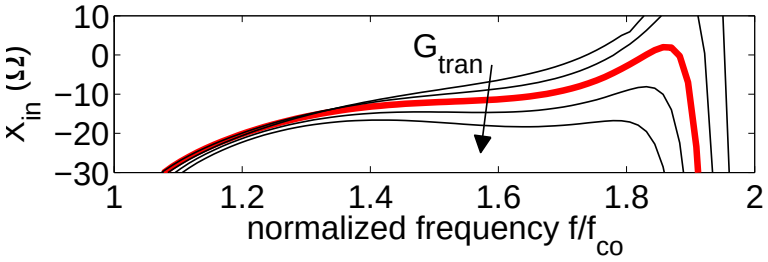

60
50
40
R_in (Ω)
L tran
1
1.2
1.4
1.6
1.8
2
normalized frequency f/f_co
0
−10
−20
−30
X_in (Ω)
L tran
1
1.2
1.4
1.6
1.8
2
normalized frequency f/f_co

(a)


70
60
50
40
30
R_in (Ω)
offset
1
1.2
1.4
1.6
1.8
2
normalized frequency f/f_co
10
0
−10
−20
−30
X_in (Ω)
offset
1
1.2
1.4
1.6
1.8
2
normalized frequency f/f_co

(b)





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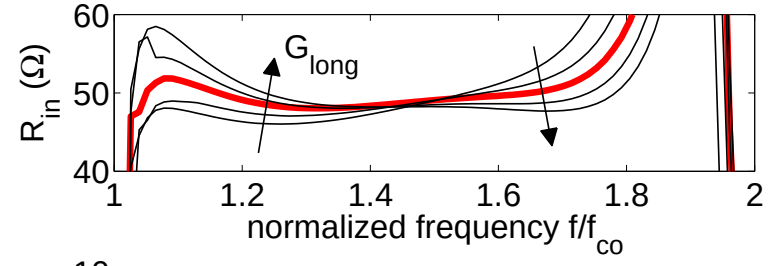
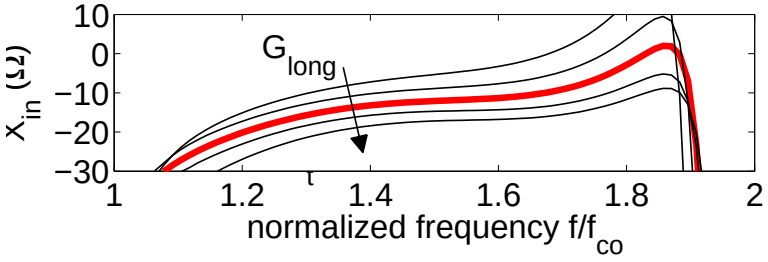




(d)

Figure 4.4: Influence of (a) the transverse slot length L_{tran}, (b) offset o, (c) transverse G_{tran} and (d) longitudinal G_{long} slot gap on the input impedance.

length is limited by the gap of the longitudinal slots to:

$$L_{tran}^{max} = a - \frac{2G_{long}}{2} \tag{4.6}$$

corresponding to the red curve in Fig. 4.4a. The gradient of the input reactance X_{in} with respect to the frequency is small, which is desirable for broadband operations. However, the gradient of the input resistance R_{in} rapidly increases above $\bar{f}$ because the slot is approaching its third resonance frequency (i.e., $\lambda_{co} = 1.5\lambda_{slot}$), characterized by a very high Z_{in}, which occurs at approximately $2f_{co}$. When L_{tran} is decreased, the third resonance is moved to higher frequency and the R_{in} gradient decreases, but at the expenses of the X_{in} gradient since the longitudinal slots become longer (L_{tot} is constant to λ_{co}) and the transverse slot is distant more than $\lambda_g/4$ from the waveguide end wall.

The offset o of the longitudinal slots is a critical parameter since it controls the distance of the transverse slot from the waveguide end wall, which should be $\lambda_g/4$ at $\bar{f}$. Increasing the offset, this distance increases and the standing wave between the slot and the end wall causes the large gradient of R_{in} (see Fig. 4.4b). Decreasing the offset instead, the longitudinal slots are placed close to the end wall, forcing the vertical component of the electric field across the slots to vanish, which results in increasing the gradient of R_{in}. A compromise is reached when the offset is equal to the longitudinal slot gap G_{long}, and R_{in} is rather constant over the frequency (red curve in Fig. 4.4b). The length of each longitudinal slot L_{long} is set to $\lambda_{co} - L_{tran}/2$ in order to place the resonance at $1.5f_{co}$ (see section 4.2.3).

As for a coplanar slot antenna, the gap G_{tran} of the transverse slot shifts upward or downward the input resistance curves and has little effect on the input reactance (see Fig. 4.4c). For the proposed U-slot transition, it was found from electromagnetic simulations that a small gap, e.g., one tenth of the transverse slot width (red curve in Fig. 4.4c), is sufficient to get $R_{in} = 50\Omega$.

Similar considerations apply for the gap G_{long} of the longitudinal slots (see Fig. 4.4d), but their proximity to the waveguide vertical walls introduces a capacitive loading effect that decreases the slot resistance. As result, the slots width have to be doubled with respect to G_{tran} (wider slots exhibit larger capacitance) in order to have a slot input resistance of 50 Ω. Note that the red curve in Fig. 4.4d corresponds to the optimum condition $G_{long} = o$, hence exhibiting the smallest gradient of R_{in}.

Table 4.1: Transition design parameters.

	waveguide		transition						CPW	
#	ϵ_r	f_{co}	f_r	L_{tran}	L_{long}	G_{tran}	G_{long}	o	S	W
1	5.5	35	52.5	1219	975	122	244	244	70	12
2	11.9	35	52.5	828	711	83	165	165	70	36
3	5.5	77	115.5	554	444	55	111	111	70	12
4	11.9	77	115.5	376	323	38	75	75	70	36

4.3.2 Design equations

Simple empirical design equations can be extracted from the parametric analysis once the substrate ϵ_r and the waveguide cut-off frequency f_{co} are fixed. Since λ_{co} in eq. 4.1 is frequency independent, it constitutes a convenient parameter to normalize all the transition dimensions. The total length of the U-shaped slot is one slotline wavelength at $1.5f_{co}$. From numerical simulations, it is found that a good compromise for the transverse slot length is:

$$L_{tran} = \frac{2}{3}a = \frac{\lambda_{co}}{3} \tag{4.7}$$

and consequently the longitudinal slots length is:

$$L_{long} = \frac{\lambda_{slot} - L_{tran}}{2} \tag{4.8}$$

where λ_{slot} is at $f = 1.5f_{co}$. The transverse slot width is set to have 50 Ω input resistance:

$$G_{tran} = \frac{1}{10}L_{tran} \tag{4.9}$$

The width of the longitudinal slots is choosen to be twice the required value to compensate for the loading effect of the waveguide vertical side walls, and their width is set equal to the offset:

$$G_{long} = o = 2G_{tran} = \frac{1}{5}L_{tran} \tag{4.10}$$

4.3.3 Design examples

To validate the proposed equations, different examples of U-shaped slot transition were designed using waveguides with two cut-off frequencies (i.e.,

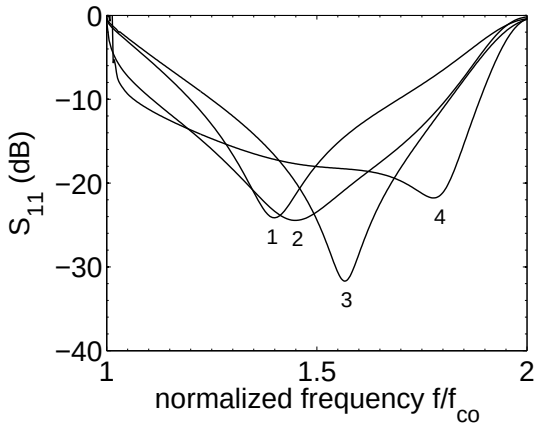


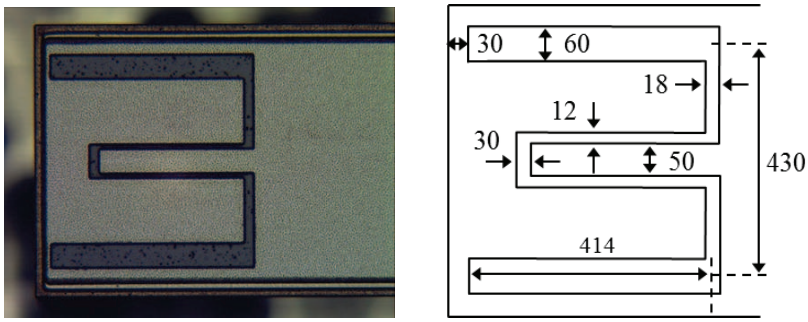
Figure 4.5: Simulated S_{11} of the transitions reported in Table 4.1. The exact position of the notch is affected by the variation of the CPW impedance over the frequency and can be shifted for instance by slightly changing the CPW gap.

35 and 77 GHz) and two substrate materials (i.e., glass and silicon). The geometrical dimensions are reported in Table 4.1, and the simulated results in Fig. 4.5: all the transitions are well matched, with the simulated reflection coefficient much below -10 dB for a frequency bandwidth larger than 36%. Although the matching bandwidth is centered around $f = 1.5f_{co}$, the shape and position of the S_{11} notch in Fig. 4.5 varies per design as the impedance of the CPW feeding line is not exactly constant to 50 Ω over the entire frequency range.

Transitions #2 and #4 (silicon substrate, ϵ_r=11.9) exhibit a band greater than transitions #1 and #3 (glass, ϵ_r=5.5) because, with the proposed design rules, the error committed by approximating f_r with $1.5f_{co}$ in eq. 4.5 (see section 4.2.3) decreases with increasing the dielectric constant.

4.4 Measurement results

Prototypes of the U-shaped slot transitions working in the W-band were manufactured using DRIE and KOH waveguides, and S-parameters measurements of two back-to-back transitions were performed with an Agilent E8361C PNA connected on both ports to Agilent mm-wave modules to cover the 67-110 GHz band. The waveguide cut-off frequency is 77 GHz, however measurements were performed up to 110 GHz (rather than $2f_{co}$=154 GHz)



(a) (b)

Figure 4.6: Coplanar to waveguide transition on the top face of a DRIE waveguide: (a) photo and (b) dimensions in micrometers.

due to instrumentation limitation. For this reason, the transition was designed by setting f_r to 94 GHz (i.e., $L_{tot} = \lambda_{slot}$ at 94 GHz rather than at $1.5f_{co}$=115.5 GHz) in order to achieve a lower S_{11} in the band of interest.

4.4.1 DRIE waveguide transition

The U-shaped slot transition implemented with DRIE waveguides is illustrated in Fig. 4.6 together with its dimensions.

Fig. 4.7a shows the measurement results of a section of plasma etched waveguide connected at the input and output using the proposed coplanar to waveguide transition: the input matching is below -10 dB for the entire measured frequency range 78-110 GHz. The S-parameters matrix of one single transition was extracted from the back-to-back measurements using both an L_1-L_2 [145–147] and a TRL [151] de-embedding algorithm, as reported in Fig. 4.7b, 4.7c and 4.7d. The L_1-L_2 and TRL de-embeddings give exactly the same result for the S_{11} of the transition (i.e., at the coplanar port): the input matching is better than -14.5 dB from 79 till 110 GHz, and simulations predict a relative bandwidth of 54% up to 135 GHz. At the waveguide port, both S_{22} measurements show a notch around 95 GHz not detected by simulations. L_1-L_2 gives a smoother curve compared to the TRL for the S_{21}, and an insertion loss for the transition of 0.6 dB at 100 GHz is calculated from it.

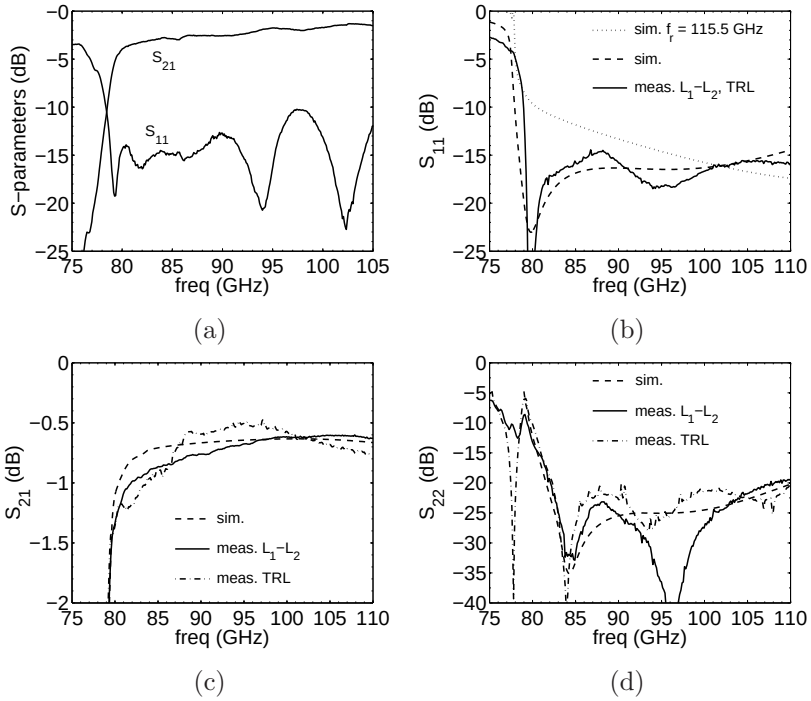
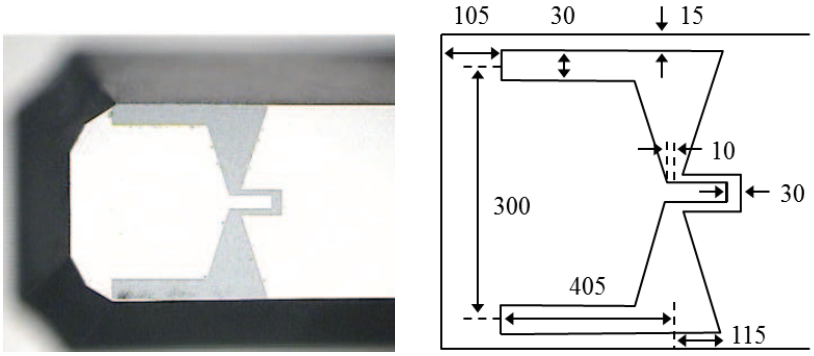


Figure 4.7: DRIE waveguide, S-parameters of: (a) two back-to-back transitions, (b-d) one de-embedded transition with f_r=94 GHz. As comparison, the simulated S_{11} of a non-optimized design with $f_r = 1.5 f_{co}$=115.5 GHz (curve #4 in Fig. 4.5) is also reported in (b), showing a worse input matching in the frequency range 75-110 GHz. S_{11} is at the coplanar port, S_{22} at the waveguide port; TRL and L_1-L_2 de-embeddings give the same result for S_{11}.

4.4.2 KOH waveguide transition

When the U-slot transition is implemented on a KOH waveguide, the width of the top face, given by eq. 3.3 is smaller than $\lambda_{co}/2$ due to the trapezoidal shape of the cross-section (see Fig. 3.1), thus the length of the transverse slot L_{tran} cannot be chosen according to eq. 4.7. A shorter slot causes a higher input impedance, which however cannot be lowered to 50 Ω by simply reducing the transverse slot gap (see Fig. 4.4c) as this would require a value of G_{tran} comparable to the manufacturing accuracy. The layout is hence modified as in Fig. 4.8: the longitudinal slots are located as



(a) (b)

Figure 4.8: Coplanar to waveguide transition on the top face of a KOH waveguide with cut-off at 77 GHz: (a) layout and (b) dimensions in micrometers. The CPW has a signal line and gap width of 50 and 15 μm, respectively.

close as possible to the waveguide side walls (a small distance of 15 μm is left to account for manufacturing and alignment tolerances during the metal patterning), while the reduced length of the transverse slot is compensated by tapering its gap width G_{tran}, which produces an increase of the slot capacitance and hence a decrease of the transition input impedance. The length of the longitudinal slots is then calculated using eq. 4.8 and assuming for L_{tran} the (ficticious) value given by eq. 4.7 rather than its (shorter) physical length.

The measured S-parameters of the U-shaped tapered slot transition are reported in Fig. 4.9a: the input matching is very poor, and a large discrepancy is visible with respect to the simulated results. By carefully investigating the transition under the microscope, it is possible to notice (see Fig. 4.8a) that the waveguide convex corners are not exactly sharp, even though the compensating structures described in section 3.3.1 were employed. The under-etching at the convex corners arose from the fact that the wafer was exposed to the etchant solution for an extra time, not taken into account in the design of the compensating structures, in order to remove all the silicon around the waveguide and to create a good contact between the waveguide side and bottom metal (see Fig. 3.2). The corners of the waveguides, which are located close to the end of the longitudinal slots, were altered each in a slightly different way due to processing inhomogeneities. To better study the effect of under-etching on the transition performances (e.g., impedance

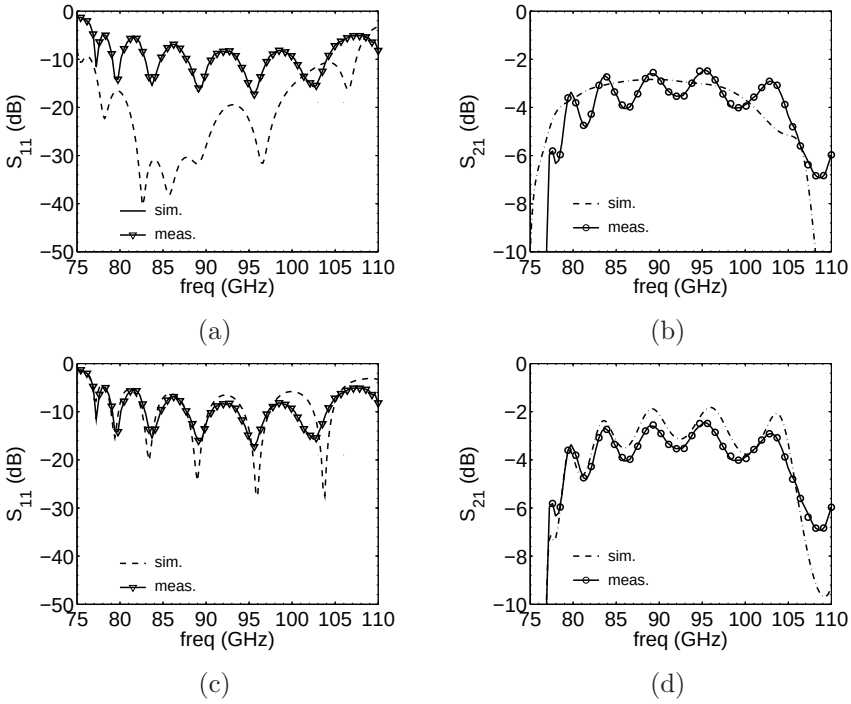
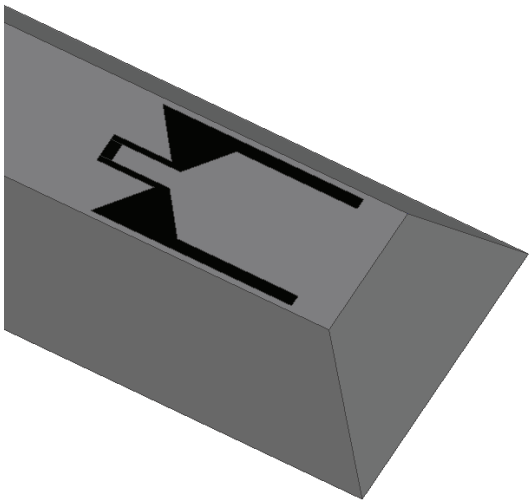


Figure 4.9: KOH waveguide with two back-to-back transitions: measurements vs. simulations (a)-(b) without and (c)-(d) with under-etching at the convex corners.

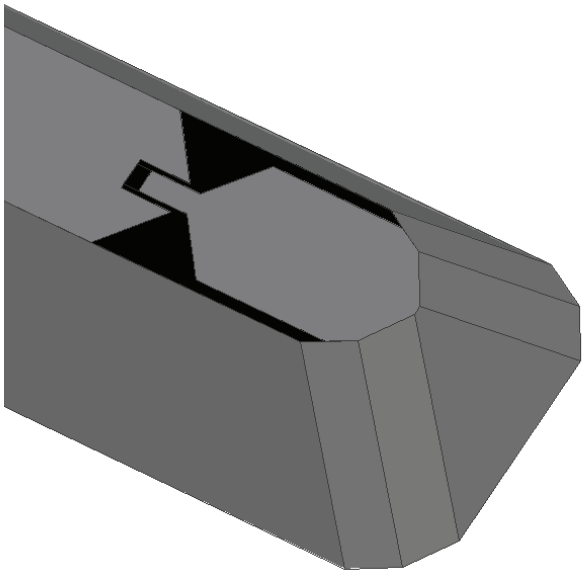
input matching), a model was built in the HFSS simulator, as in Fig. 4.10. Looking at the waveguide corners under the microscope (Fig. 4.9c), it was hypothesized that the etching extended for 50 μm under and for 100 μm around each convex corner, so that the waveguide side walls intersect with an angle of 152° (Fig. 4.10b) rather than 90° (Fig. 4.9c).

Finally, the measured S-parameters are compared to a simulation of the transition with under-etched corners (see Fig. 4.9c-4.9d): the agreement is good, and fully supports the explanation of the degraded waveguide performances. The small discrepancy between the peaks of the curves in Fig. 4.9b can depend on a shift on the exact position of the waveguide end walls due to manufacturing tolerances, or by a shift in probe placements during measurements.

The L_1-L_2 de-embedding gave good results in agreement with simulations for the waveguide propagation constant (see section 3.5.1), but in-



(a)



(b)

(c)

Figure 4.10: KOH waveguide transition: HFSS model (a) without and (b) with under-etching at the corners; (c) real structue.

consistent for the S-parameters of a single transition, suggesting that the four transition employed in the de-embedding are not exactly identical. A possible explanation could be that the KOH etching is more sensitive to manufacturing inaccuracies and process inhomogeneities when compared to DRIE because of the under-etching at the convex corners, which are located close to the longitudinal slots of the transition. The etching rate at the corners is much higher than along the <100> crystallographic direction, causing different offsets o from the waveguide end wall of the four tranitions employed in the de-embedding.

On the other hand, a TRL de-embedding was difficult to perform at those frequencies because of the uncertainty in defining the reference plane. The TRL sets in fact the reference plane at the center of the thru line and uses the sign of the reflected standard, a (non-deal) short or open, to determine the sign of one of the terms in the error network [151]. Because of the KOH waveguide tilted wall, the short posseses an extra length that can change the sign of phase of its reflection coefficient over frequency and cause

a mistake in the extraction of the error network if not carefully accounted for. Therefore, transition losses were for simplicity extracted by subtracting the waveguide losses to the L_2 structure (i.e., transitions plus waveguide section): as result, an insertion loss of 0.87 dB at 100 GHz was estimated for a single transition.

4.5 Conclusions

A CPW to waveguide transition based on a U-shaped slot antenna was presented: the ultra-wide matching bandwidth was explained in terms of input impedance and quality factor of a slot antenna, while the coupling from CPW to SIW mode was illustrated in terms of field distribution. A parametric analysis of the effect of the slot geometrical dimensions on the input impedance of the transition was carried out and discussed. Simple empirical design equations have been presented and validated on a transition realized in a silicon integrated waveguide technology. When compared to KOH waveguides, DRIE structures do not suffer from under-etching at convex corners, which translates in a superior control of the geometrical dimension and therefore a better impedance matching of the transition, whose measured $|S_{11}|$ is below -14.5 dB in the entire frequency range 79-110 GHz.

Chapter 5

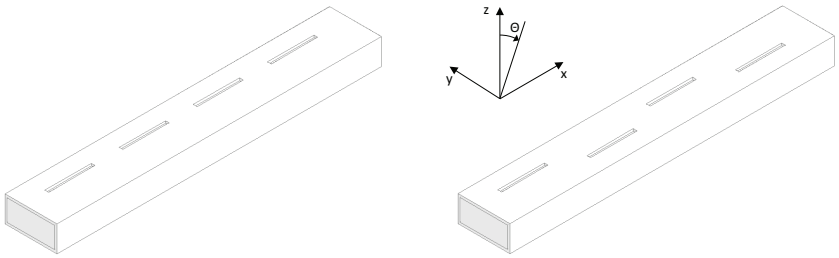
Frequency scanning array

5.1 Introduction

Radar and imaging systems employed for automotive [152], screening [128, 153, 154] or security [155, 156] applications require smart antennas with a high gain and angular resolutions. To focus the beam, dielectric lenses mounted on top of the antenna [44, 45] or array configurations [46, 47] can be employed. At mm-waves, the small wavelength in the order of few millimeters allows to realize compact on wafer arrays with a large number of elements but with a reduced area consumption.

The practical realization of smart antennas is hampered by the complex signal feeding distribution to the array elements [157–160] or by the interfacing with active circuits when quartz lenses or superstrates [161, 162] are employed. SIW offers the possibility to distribute the signal with low losses and cross-coupling effects over large distances, and can be interfaced with active circuits through the use of planar transitions and flip-chip assembly, but the low geometrical accuracy of the technology prevents the realization of antennas with low side lobe levels [163].

In this chapter, the silicon-filled waveguide manufacturing technology introduced in chapter 3 is employed for the realization of slotted waveguide arrays to be interfaced with imaging radar systems. First, the general principles of phased and of frequency scanning array antennas are recalled; after that, the design procedure of a travelling wave array in waveguide is outlined, and equations are obtained to optimize the far field pattern of the antenna. The choice of the power distribution radiated by the waveguide slots is discussed, and two solutions with a uniform offset and a Dolph-Tschebyscheff distribution are implemented and analyzed. Finally, the mea-



(a) (b)

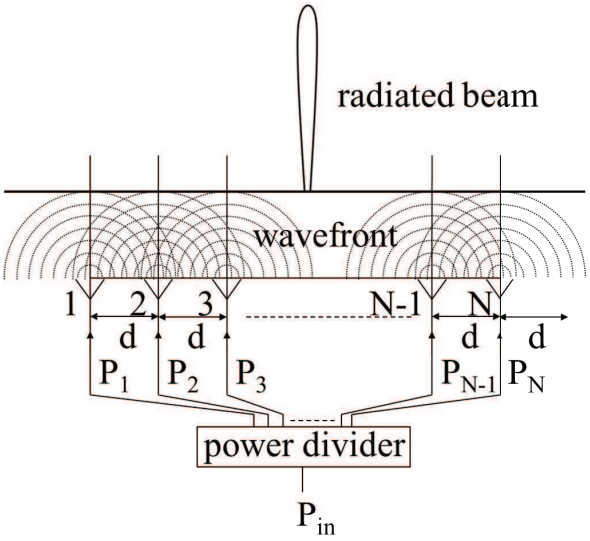
Figure 5.1: Slotted waveguide array with: (a) non-alternate and (b) alternate longitudinal slots in the broad face of the waveguide.

sured results (conducted and radiated) of arrays designed using both the KOH and the DRIE etching technology are presented.

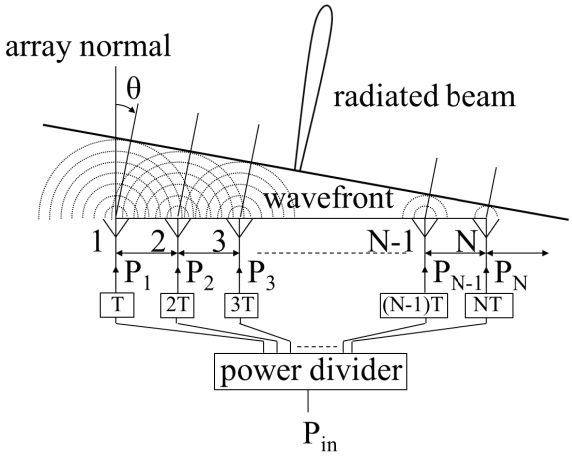
5.1.1 Travelling wave frequency scanning array

Fig. 5.1 reports an example of waveguide array, where metallic (non-alternate or alternate) slots have been periodically opened on the broad face of a waveguide and can radiate energy into free space. A slotted waveguide array is called resonant or travelling wave depending on the load used to terminate the waveguide [59]. In the first case, the array is terminated on a highly reflective load (e.g., short) that gives rise to a standing wave distribution of currents and voltages along the waveguide. In the second case instead, the array is terminated on a low reflective (e.g., matched) load that produces a travelling wave pattern of currents and voltages, minimizing the mismatch and increasing the input matching bandwidth.

Array antennas are usually employed to focus the radiated power in one main beam, whose direction depends on the particular array geometry. In order to steer it, phased array topologies employ the relative phase offsets (i.e., the time delays in time domain) of the signals feeding the array radiators [164]. To understand the working principle, let us consider the linear array reported in Fig. 5.2a: the input signal is split into N signals with equal amplitude and phase which feed the N radiators. As each antenna radiates, the wave fronts proceed in phase and constructively interfer with each other: the resulting wave front is parallel to the array line, and the main radiated beam is ortogonal to it (broadisde direction). The width of the main beam is instead controlled by the array factor, and becomes narrower as the number of elements N is increased [51]. In Fig. 5.2b instead,



(a)



(b)

Figure 5.2: Array interference: (a) input signals are in phase, the radiation is broadside, i.e., normal to the array line; (b) input signals are delayed with respect to each other, the radiation is at an angle θ with respect to broadside.

the input signal is split into N signals of equal amplitude, but with a time delay multiple of a given quantity T. When the wave fronts add up, constructive interference does not occur along the array line because the fronts have different delays; as result, the direction of the main beam is inclined of an angle θ with respect to the array normal:

$$sin\,\theta = \frac{c_0 T}{d} \tag{5.1}$$

where c_0 is the speed of light in free space, and d is the periodic spacing of the antennas. Therefore, a 1D spatial scanning can be performed since the angle θ is controlled by the delay T.

A special situation occurs when the delay T depends on the frequency of the signal feeding the antennas, so that the angular steering can be controlled by changing the frequency, An example of such a structure, called frequency scanning array, is the slotted waveguide array of Fig. 5.1, where the time delay block of Fig. 5.2b is realized with a section of waveguide of length d. The phase offset betwen the signals feeding two consecutive slots is given by the waveguide phase constant β multiplied by the spacing d. Since β varies with the frequency, the main beam angle can be steered with frequency, and the scanning angle is given by:

$$sin\,\theta = \frac{\lambda_0}{\lambda_g} - \frac{\lambda_0}{2d} \tag{5.2}$$

where λ_g and λ_0 are the guided and free space wavelength, respectively.

5.2 Analysis of a frequency scanning array

In [58, 59] the radiation of a linear array of isotropic sources excited by a TEM travelling wave was analyzed: the relation between the phase constant and the frequency is linear, and general closed form relations to impose the existence of only one main lobe in the radiation pattern were derived. In this section, similar relations are derived for the case of a slotted waveguide array with non-alternated slots, where the linear array of sources (i.e., the slots) is excited by a TE_{10} travelling wave, whose relation between the phase constant and the frequency is non-linear.

Consider an infinite array with slots aligned along the x direction ($\theta = \pm\pi$ in polar coordinates) and the array normal along the z direction ($\theta = \pm\pi/2$), as in Fig. 5.1a. The radiating slots act as a periodic load for the waveguide and impose a periodicity condition to the field inside the strucure, which can therefore be expressed in the form of a Floquet wave [59].

A discrete number of spatial harmonics associated with the TE_{10} mode propagates inside the waveguide, each with phase constant given by:

$$\beta_m = \beta_0 - \frac{2\pi}{d}m \qquad m = .., -1, 0, +1, .. \tag{5.3}$$

where d is the spacing between the slots, β_0 is the phase constant of the unloaded structure, and m is the index of the m-th spatial harmonic.

In the general case of a wave travelling in the +x direction and uniform in the y direction, the electric field for z>0 can be expressed as [165]:

$$E(x,z) = \hat{y}e^{-j\beta_m x}e^{-j\sqrt{k_0^2-\beta_m^2}z} \tag{5.4}$$

The m-th spatial harmonic can be either a *slow-wave* or a *fast-wave* depending on its phase velocity $v_{p,m}$ that varies with frequency. When the wave is fast, the phase velocitiy $v_{p,m}$ is higher than the free space velocity c_0 (i.e., $|\beta_m| < k_0$ since $v_{p,m}$=w/β_m and $c_0 = w/k_0$): the root $\sqrt{k_0^2 - \beta_m^2}$ is real, and eq. 5.4 describes a wave that radiates into free space at an angle θ, measured with respect to the array normal, given by:

$$sin(\theta) \approx \frac{\beta_m}{k_0} \tag{5.5}$$

When the travelling wave is slow, the root is imaginary and θ becomes complex: eq. 5.4 describes an evanescent wave, which does not propagate nor radiate energy inside the visible region (i.e., the angular region delimited by -$\pi < \theta < \pi$) for any real value of θ. Similar considerations apply when the travelling wave is no longer uniform along the y direction, but a waveguide TE_{10} mode that radiates energy into free space through discrete slots, provided the slots only introduce a small perturbation to the mode field distribution.

A useful tool to analyze the radiative behaviour of the array is the Brillouin diagram [59, 60] which reports the normalized free space wavenumber $k_0 d$ versus the waveguide phase constant β_md, and is depicted in Fig. 5.3 in the case of non-alternate slots (see Fig. 5.1a) and TE_{10} mode waveguide excitation. The diagram is periodic of 2π, and each curve corresponds to the m-th spatial harmonic of eq. 5.3 associated with the TE_{10} mode. Note that these spatial harmonics are all propagating at the same frequency, unlike waveguide higher order modes (e.g., TE_{20} or TM_{01}) that start propagating at higher frequencies.

The fast wave region (FWR) indicates the part of the Brillouin diagram for which a propagating wave is fast and corresponds to the region $k_0 d > |\beta_0 d|$ in Fig. 5.3. At any frequency, all the harmonics lying outside the

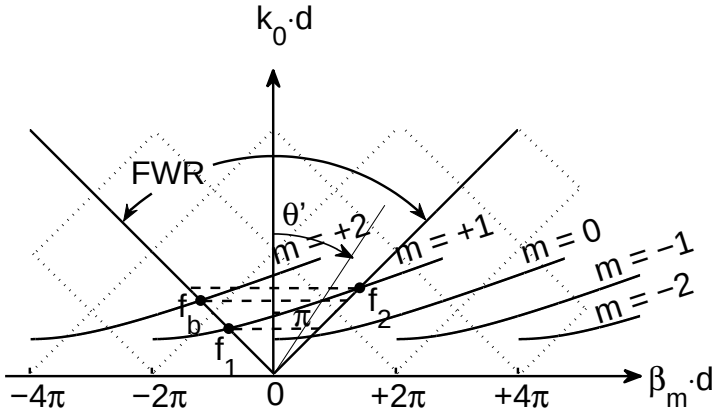


Figure 5.3: Brillouin diagram of a slotted waveguide with $f_b < f_2$ and non-alternate slots; only the TE_{10} mode is considered. The FWR is the region of plane between the two straight lines of equations $k_0 d = -\beta_0 d$ and $k_0 d = +\beta_0 d$.

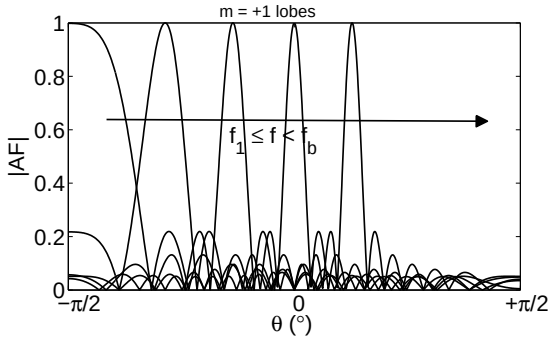
FWR are bound (i.e., slow) and do not radiate energy into free space, while all the harmonics inside the FWR radiate energy

Consider for instance the first harmonic (m=+1) in Fig. 5.3. At frequency f_1, the harmonic crosses the line $k_0 d = -\beta_0 d$ and enters the FWR, hence radiating energy at an angle θ related to the θ' angle in Brillouin diagram (see Fig. 5.3) by:

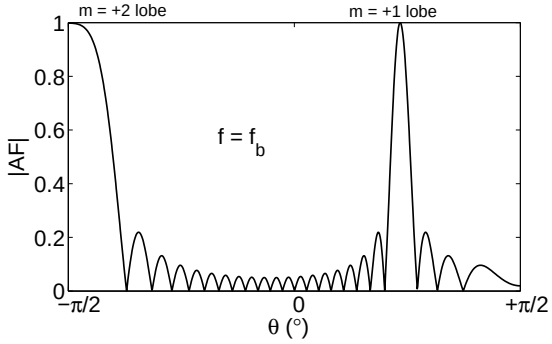
$$sin(\theta) = \frac{\beta_m}{k_0} = tan(\theta') \tag{5.6}$$

which gives $\theta = -90°$ since $k_0 d = -\beta_0 d$ at f_1.

In a similar way, the situation can be explained looking at Fig. 5.4a, where the array factor is plotted with respect to the observation angle θ. The array factor, as the Brillouin diagram, is periodic of period 2π, and the part of the visible region $-\pi/2 \leq \theta \leq +\pi/2$ corresponds to the FWR, that is $-\pi/4 \leq \theta' \leq +\pi/4$ in Fig. 5.3. The main beam (i.e., unitary amplitude) that appears at θ=$-\pi/2$ is associated to the m=+1 harmonic entering the FWR at f_1 in Fig. 5.3, while the harmonics located outside the FWR correspond to the other (periodic) peaks of the array factor located outside the visible



(a)



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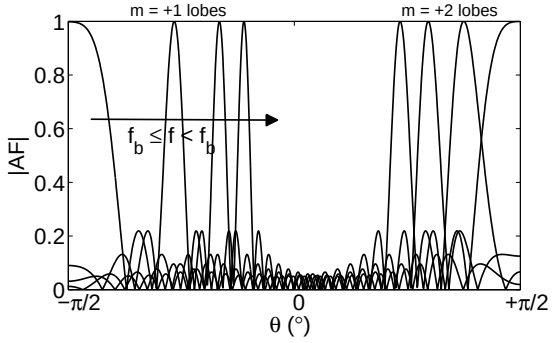


(c)

Figure 5.4: Array factor: (a) only the m=+1 harmonic in the FWR, with the main lobe moving right as the frequencty is increased from f_1 to $f < f_b$; (b) at frequency $f = f_b$, the m=+2 harmonic enters the visible region (i.e., FWR), and two peaks appear in the radiation pattern; (c) for any frequency $f_b \leq f \leq f_2$, both the m=+1 and the m=+2 harmonics are present inside the visible region and radiate energy. Note that the beam in (a) is wider at endfire and narrower at broadside.

region and not plotted in Fig. 5.3. At any frequency, the number of main beams in the array factor between $-\pi/2 \leq \theta \leq +\pi/2$ is equal to the number of spatial harmonics in the FWR.

The array factor is plotted in Fig. 5.4a only for $-\pi/2 \leq \theta \leq +\pi/2$ since it is symmetric (i.e., even function) with respect to the array axis z=0: for each main beam at an angle $\overline{\theta}$ in the z>0 semispace, there is another main beam, not shown in Fig. 5.4a but still located inside the visible region, at $2\pi - \overline{\theta}$ in the z<0 semispace. The far field radiation pattern of the array is obtained by multiplying the field of the single element (i.e., the slot) with the array factor [51]. A waveguide slot can be approximated with an isotropic radiator in one semispace, e.g., z>0 or $-\pi/2 \leq \theta \leq +\pi/2$, for which therefore the far field radiation pattern can be approximated with the array factor. In the semispace z<0 or $\pi/2 \leq \theta \leq 3/2\pi$ the slot radiates a negligeble amount of energy, so that the peak at $-\overline{\theta}$ of the array factor is cancelled out by the field of the slot. As result, the number of peaks of the array factor between $-\pi/2 \leq \theta \leq +\pi/2$ is equal to the number of main lobes in the array far field pattern, while the array factor outside this range can be neglected.

As the frequency is increased above f_1, the main beam is shifted to higher scanning angles θ, and the operating point in the Brillouin diagram of Fig. 5.3 moves along the line of equation:

$$kd = p\beta_m d \tag{5.7}$$

The angular slope p is the ratio of the wave velocity in the waveguide to the speed of light:

$$p = \frac{v}{c} = \frac{kd}{\beta_0 d} = \frac{1}{\sqrt{\epsilon_r}} \frac{1}{\sqrt{1 - (\frac{f_{co}}{f})^2}} \tag{5.8}$$

where f_{co} is the waveguide cut-off frequency. At frequency f_2, the beam points at $+90°$ before leaving the FWR after a $180°$ angular scanning. However, at frequency $f_b < f_2$ the second harmonic (m=+2) enters the FWR and radiates energy (or equivalently the second harmonic enters the $[-\pi/2,+\pi/2]$ visible region in Fig. 5.4b) and two main lobes appear in the radiation pattern. Finally, as the frequency is further increased, both main lobes are shifted toward higher angles, so that for all the frequencies $f_b \leq f \leq f_2$ two main lobes appear in the radiation pattern. Note that all the harmonics with $m \leq 0$ in Fig. 5.3 (partially) lie outside the FWR (i.e., in the invisible region): since they cannot provide a $180°$ angular scanning, they will not be considered in the rest of the analysis.

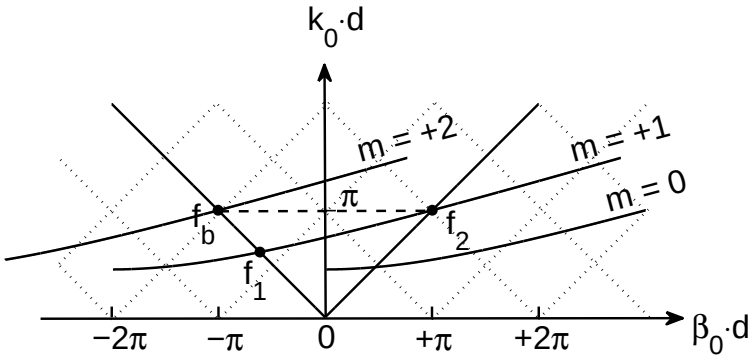


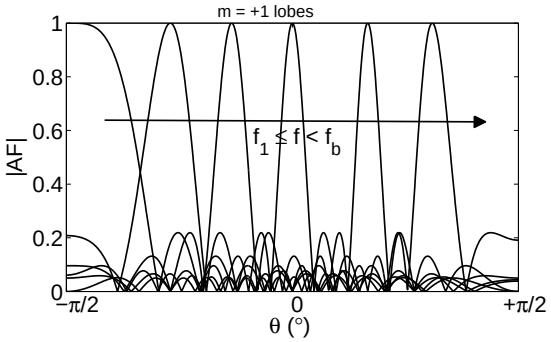
Figure 5.5: Dispersion diagram of a slotted waveguide with $f_b = f_2$ and non-alternate slots.

The situation is different in Fig. 5.5, where eq. 5.3 is plotted for a lower value of the slope p. The first harmonic (m=+1) leaves the FWR at f_2 crossing the point (π, π): since the Brillouin diagram is periodic of 2π, at the same frequency $f_b = f_2$ the second harmonic (m=+2) enters the FWR crossing the point $(-\pi, \pi)$. Therefore, for all the frequencies $f_1 \leq f < f_2$, only one main lobe appears in the radiation pattern (see Fig. 5.6), which corresponds to the energy radiated by the m=+1 harmonic of the TE_{10} mode.

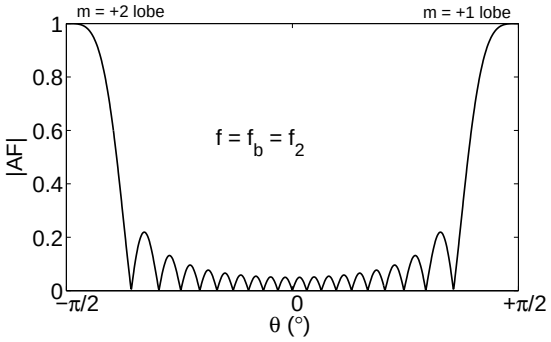
In general, in order for the m-th spatial harmonic to radiate between f_1 and f_2 while all the other harmonics are bound, the curve $kd = p\beta_m d$ has to cross the FWR below the point (π, π):

$$kd = \frac{1}{\sqrt{\epsilon_r}} \sqrt{(\beta_m d)^2 + \left(\pi \frac{d}{a}\right)^2} \Bigg|_{\beta_0 d = \pi} < \pi \tag{5.9}$$

where β_m and β_0 are related by eq. 5.3. Using the expression of the array factor, a relation between the periodic spacing of the slots and the frequency at which broadside radiation occurs can be found.



(a)



(b)

Figure 5.6: Array factor: (a) only the m=+1 harmonic in the FWR for any frequency $f_1 \leq f \leq f_2$, (b) the m=+2 harmonic enters the FWR at $f = f_b = f_2$.

5.2.1 Array factor

The array factor $f(\theta)$ of N radiators (e.g., slots) fed with signals equal in amplitude and progressive phase is given by [51]:

$$f(\theta) = e^{j\frac{N-1}{2}} \frac{sin(N\frac{Y}{2})}{Nsin(\frac{Y}{2})} \tag{5.10}$$

$$Y = -\beta_m d + k_0 d sin\theta \tag{5.11}$$

where θ is the observation angle, $-\beta d$ is the progressive phase between consecutive elements, and β is the phase constant β_m of the m-th harmoninc

in the FRW.

If all the radiators are isotropic, the main beam in the far field pattern of the array occurs at the direction given by $Y = -2\pi m$ where eq. 5.10 has a maximum, and the nulls are located at $Y = -\pi m$. Using eq. 5.8, the variable Y can be written as

$$Y = 2m\pi \frac{f}{f_c} \frac{p_c}{p} (psin\theta - 1) \tag{5.12}$$

where f_c is the broadside center frequency (main beam pointing at $\theta = 0°$), and p_c is p at f_c (see eq. 5.8).

The slot spacing d can be found considering eq. 5.11 at broadside frequency and equating it to $Y = -2\pi m$ where the main beam occurs:

$$d = m\lambda_{gc} \tag{5.13}$$

where λ_{gc} is the guided wavelength λ_g at f_c.

Therefore, eq. 5.9 which imposes the exsistence of only one main lobe in the FWR can be rewritten as:

$$\frac{d}{a} < \sqrt{\epsilon_r - (2m+1)^2} \tag{5.14}$$

where the quantity under square root has to be positive:

$$m < \frac{\sqrt{\epsilon_r} - 1}{2} \tag{5.15}$$

This inequality can be satisfied by none, one or more values of m depending on the choice of the dielectric material. Moreover, substituting eq. 5.13 into eq. 5.14, a relation for the cut-off frequency is found:

$$f_{co} < \frac{f_c}{\sqrt{1 + \frac{(2m)^2}{\epsilon_r - (2m+1)^2}}} \tag{5.16}$$

For a given material, eq. 5.15 imposes which spatial harmonics can be used, and eq. 5.16 an upper limit to the waveguide cut-off frequency.

As showed in section 3.5.2, the losses of an unloaded (i.e., no slots) waveguide are low around the center of the mono-modal bandwidth (i.e., well above the cut-off of the fundamental mode but well below the cut-off of the first higher order mode), which occurs at around $1.5f_{co}$ for a waveguide with an aspect ratio of 2:1. Therefore, if more choices of the index m that satisfies eq. 5.15 are possible, it is preferable to work with the spatial harmonic for which the ratio f_c/f_{co}, limited by eq. 5.16, can be set to 1.5.

5.2.2 Frequency scanning range

Referring to Fig. 5.5, if f_1 and f_2 are the lower and higher frequencies at which the beam is pointing at $-90°$ and $+90°$, respectively, [58] found that:

$$\frac{f_1}{f_c} = \frac{p_1}{p_c}\frac{1}{1+p_1} \tag{5.17}$$

$$\frac{f_2}{f_c} = \frac{p_2}{p_c}\frac{1}{1-p_2} \tag{5.18}$$

where p_1 and p_2 are the values of p evaluated at f_1 and f_2, respectively (see eq. 5.8). For a travelling wave inside a waveguide, eq. 5.17 and 5.18 are not in the explicit form since f_1 and f_2 are also contained inside p_1 and p_2. Therefore, substituting eq. 5.8 into the expressions of p_1 and p_2, two quadratic equations are obtained:

$$(\epsilon_r - 1)f_1^2 + 2\frac{f_c}{p_c}f_1 - \epsilon_r f_{co}^2 - \frac{f_c}{p_c}^2 = 0 \tag{5.19}$$

$$(\epsilon_r - 1)f_2^2 - 2\frac{f_c}{p_c}f_2 - \epsilon_r f_{co}^2 - \frac{f_c}{p_c}^2 = 0 \tag{5.20}$$

Solving the equations and considering only positive roots, an explicit closed form expressions for f_1 and f_2 is obtained in terms of only the material dielectric constant and the design center frequency:

$$f_1 = \frac{-\frac{f_c}{p_c} + \sqrt{\epsilon_r(\epsilon_r - 1)f_{co}^2 + \epsilon_r\left(\frac{f_c}{p_c}\right)^2}}{\epsilon_r - 1} \tag{5.21}$$

$$f_2 = \frac{+\frac{f_c}{p_c} + \sqrt{\epsilon_r(\epsilon_r - 1)f_{co}^2 + \epsilon_r\left(\frac{f_c}{p_c}\right)^2}}{\epsilon_r - 1} \tag{5.22}$$

Moreover, the frequency bandwidth Δf needed to perform a $180°$ phase shift of the beam is given by:

$$\Delta f = f_2 - f_1 = \frac{2}{\epsilon_r - 1}\frac{f_c}{p_c} \tag{5.23}$$

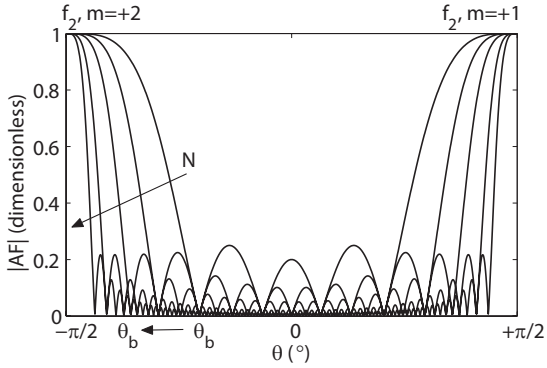


Figure 5.7: Array factor at frequency $f_b = f_2$, critical permittivity given by eq. 5.24, and number of slots equal to: 5, 10, 20, 50 and 100. As the number of the slot increases, the first null of the m=+2 beam is shifted rightward to the edge of the visible region.

5.2.3 Finite length array

Eq. 5.9 was used to impose the existance of only one harmonic in the FWR for all the frequencies $f_1 \leq f \leq f_2$. However, the equation was derived only analyzing the Brillouin diagram; to understand how the finite number of array elements N affects eq. 5.9, it is useful to analyze the radiation pattern at the frequency f_2 for the critical condition:

$$m = \frac{\sqrt{\epsilon_r} - 1}{2} \tag{5.24}$$

If the harmonic m=+1 is considered, eq. 5.24 is satisfied by the critical dielectric permittivity ϵ_r=9, and the corresponding radiation pattern is the one already discussed in Fig. 5.6b, where the main lobe of the m=+2 harmonic enters the visible region at θ=-90° when the m=+1 is leaving it at θ=+90°.

If the array were infinite, the radiation pattern would have zero beam width (Dirac delta), and as ϵ_r is increased just above the critical value, the Delta dirac beam associated with the m=+2 harmonic would be completely moved outside the visible region. For a finite array however, the beam has a finite width, and at the critical ϵ_r of 5.7 a tail of the m=+2 beam is still located in the visible region (see Fig. 5.7). As the number of slot is increased, the beam width is reduced (the tail shifts leftward) but the peak associated with the m=+2 mode remains at the angle θ=-90°.

In order to completely shift the m=+2 main lobe outside the visible

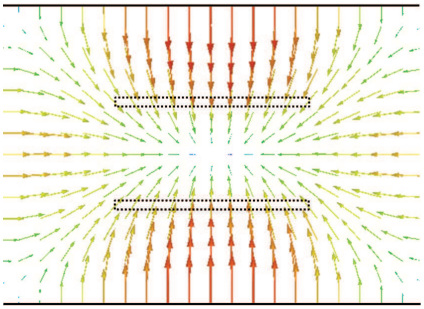


Figure 5.8: Surface currents on the top face of a waveguide excited by the TE_{10} mode.

region for all the frequencies $f_1 \leq f \leq f_2$, the first adjacent zero θ_b has to be placed [58] at θ=-$\pi/2$ at f_2; clearly, the fact that the m=+2 lobe lies in the invisible region at f_2 guarantees that the lobe will stay in the invisible region for all the frequencies $f_1 \leq f \leq f_2$. For the generic m-th radiating harmonic, the position of the zero θ_b is given by:

$$Y_b = -2m\pi + \frac{2\pi}{N} \tag{5.25}$$

where Y_b is Y for θ=θ_b. Writing eq. 5.12 at f_2 and equating to eq. 5.25, the following condition is obtained:

$$m < \frac{1-p_2}{2p_2}\left(1-\frac{1}{N}\right) \tag{5.26}$$

which relates the spatial harmonic index m, the number of elements N and the cut-off frequency f_{co} contained in p_2. Substituting eq. 5.8, 5.18 and 5.22 into eq. 5.26, an explicit condition for the cut-off frequency is obtained:

$$f_{co} < \frac{f_c}{\sqrt{1+\frac{(2m)^2}{\left(1-\frac{1}{N}\right)\epsilon_r-\left(2m+1-\frac{1}{N}\right)^2}}} \tag{5.27}$$

Note that this reduces to eq. 5.16 for N going to infinity.

The number of slots N also controls the array beam-width, but the closed-form relation depends upon the power distribution radiated by the slots and is therefore here omitted.

5.2.4 Frequency scanning array with alternate slots

The radiating slots can be alternated with respect to the center of the waveguide, as illustrated in Fig. 5.1b. Since the surface current that excites the slots changes sign crossing the center line of the waveguide, two slots on the top face of the waveguide will be excited by a current with the same amplitude, but opposite sign (i.e., with a π phase offset), as shown in Fig. 5.8. As result, the electrical distance -βd between adjacent slots in Fig. 5.1b is increased by an extra factor π: for the same electrical distance (i.e., for radiating at the same frequency scanning angle), the slots can be spaced closer, thus reducing the length of the array (note instead that for the same number of slots the beam width increases since the physical length of the array in terms of free space wavelength decreases). Alternate arrays are not presented in this work, but relations similar to those of a non-alternate array are reported for completeness in appendix D in order to obtain a radiation pattern with only one single main lobe.

5.2.5 Design procedure

In the previous sections a set of equations was derived in order to compute for a given design center frequency the geometrical and material parameters of the array so that only one mode radiates energy into the far field region. When considering a waveguide array, the choice of the material is usually constrained by process technologies available, while the number of radiating slots depends on the desired beam-width. The set of equations presented provides a simple design flow to settle the cut-off frequency and the number of radiators based on the operating frequency. Therefore, the design procedure of a travelling wave slotted waveguide array with non-alternate slots and a single 180° frequency scanning beam can be summarized as it follows:

1. Choose the broadside frequency f_c and the material ϵ_r.
2. Choose the mode m which satisfies eq. 5.15 and, if possible, sets f_c to $1.5 f_{co}$.
3. Determine the slot spacing d from eq. 5.13
4. Choose a cut-off frequency f_{co} which satisfies eq. 5.16.
5. Compute the lower f_1 and higher f_2 frequencies with eq. 5.21 and 5.22.
6. Choose the minimum number of elements N which guarantees the required array beam-width and satisfies eq. 5.27.

5.3 Design of a uniform offset array

To show the possibility of integrating waveguide arrays at mm-waves using both the KOH and the DRIE waveguide technology of chapter 3, slotted waveguide arrays were considered, employing the design procedure described in section 5.2.5.

The resonance frequency and the radiation efficiency of a slot on the broad face of a waveguide are a function of its geometrical parameters (see Fig. 5.9) [166,167], namely its length, width, and offset (with respect to the center plane of the waveguide).

The first design to be considered is a simple uniform offset array, whose length only limited by the size of the IC wafer. As radiation element, resonant slots with a small offset from the center of the waveguide were considered, as they cause low power reflections and small return loss degradation, when, for instance, compared with narrower slots with large offsets.

The array is uniform in the sense that all the slots have the same geometrical dimensions, and hence the same resonance frequency (i.e., 93.1 GHz) and radiation efficiency, while the power radiated by each slot decreases as the travelling wave propagates along the array. Note that in a conventional uniform array (narrowest beam for a given number of slots) instead, the power radiated by each slot has to be constant, and therefore the slots dimensions have to vary along the array. During the thesis work, the choice of realizing a uniform offset array was motivated by the need to quickly provide a waveguide antenna layout for further developing the SIW technology, while larger efforts were spent for the design of a Dolph-Tschebyscheff array, as explanained in section 5.4.

The design parameters of the uniform offset array, both in KOH and in DRIE technology, are reported in Table 5.1. The slot offset was set to a few microns (the manufacuring accuracy is in the order of 0.5 μm), which corresponds to a radiation efficiency of few percent. As a drawback however, a significant amount of power is dissipated by the load terminating the array. Note that the slot spacing is 44 μm larger the value given by eq. 5.13 because of a design error.

The radiation patterns were simulated by means of Ansys HFSS software and are reported in Fig. 5.10: the KOH array achieves a narrower beamwidth when compared to the DRIE array since a larger number of slots, 36 instead of 29, is used.

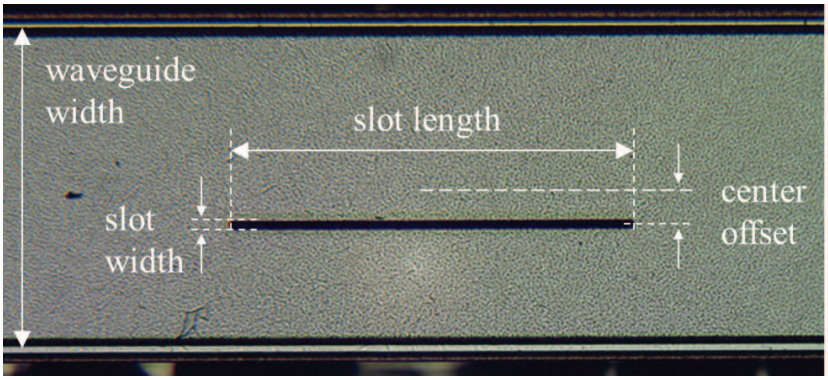


Figure 5.9: Geometric dimensions of a slot in the broad face of a rectangular waveguide.

Table 5.1: Design parameters of the uniform offset array, using a KOH or a DRIE waveguide.

waveguide	KOH	DRIE
number of slots	36	29
power delivered to the load (%)	24	40
array length[1] (mm)	65	50
array width (mm)	0.76	0.56
slot width (μm)	10	10
slot offset (μm)	4	10
slot length (μm)	604	616
slot period (μm)	1660	1660

[1] including the transitions

5.4 Design of a Dolph-Tschebyscheff array

In order to minimize the side lobes level (SLL) in the radiation pattern, the power radiated by each array slot can be chosen according to a Dolph-Tschebyscheff distribution, that allows to achieve the lowest SLL possible for a given beam width [50, 51].

The first step for the design of a Dolph-Tschebyscheff travelling wave

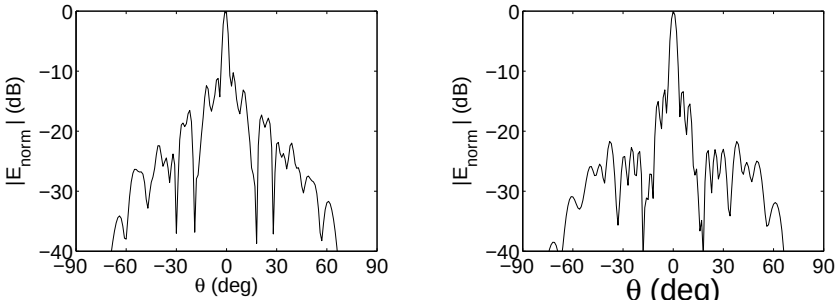


Figure 5.10: HFSS simulation (H-plane radiation pattern) of the uniform offset array using (a) a KOH and (b) a DRIE waveguide. The array was excited and terminated with wave ports.

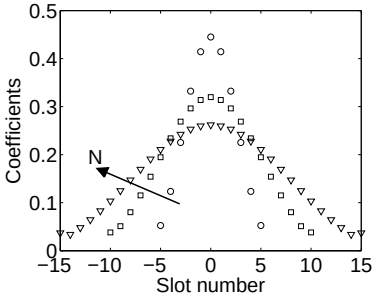
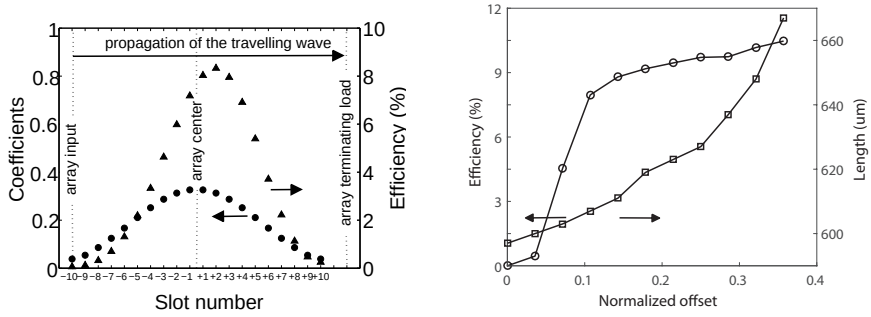


Figure 5.11: Coefficients of a Dolph-Tschebyscheff array with a side lobe level of -40 dB for the number of slot N=11, 21 and 31.

array is to fix the residual power to be dissipated by the terminating load P_l and the number of slots N (i.e., the array length). As the power lost in the load increases, the array bandwith becomes broader, but at the expenses of a lower radiation efficiency. As a compromise for for travelling wave arrays, a $P_l/P_{in} = 0.1$ is usually chosen [51].

The number of array elements (i.e., slots) controls the (effective) area and hence the beamwidth. The size of the array, measured in terms of free space wavelengths, increases with the number of slots: the array near field extends over a larger area, and the far field, which is its Fourier transform, is more directive (i.e., the power is focused in a narrower beam). As result, a simple approximation [50] gives (the formula is strictly true for a uniform



(a) (b)

Figure 5.12: 20 element Dolph-Tschebyscheff array, relation between the slot efficiencies and: (a) the Dolph-Tschebyscheff coefficients, including slot efficiency and (b) the slot geometrical dimensions on a DRIE waveguide. The slot efficiency is defined as the ratio of the radiated to the input power. The offset step in (b) is 10 μm, equal to minimum dimension guaranteed by the DRIE process for a slot, and normalized to half of the waveguide width. The slot width is fixed to 10 μm, the slot resonant frequency to 94 GHz.

power distribution):

$$HPBW = \frac{101.7}{D} = 101.7\frac{\lambda_0}{2Nd} \tag{5.28}$$

where HPBW is the half-power beam width (i.e., the angle under which half of the power is radiated) in degree, D is the array directivity, λ_0 the free space wavelength, and d the distance between adjacent slots. For the uniform offset array, eq. 5.28 provides only approximate values, as the power radiated by the slots is not equal but decreases exponentially along the array. For Dolph-Tschebyscheff array instead, the relation between half-power beam width and directivity still holds as long as a beam broadening factor is introduced in eq. 5.28 [50] (1.31 for a SLL of 30 dB).

Arrays with a small HPBW (i.e., large N) do not only require a large area consumption, but also high manufacturing accuracies. The situation is illustrated in Fig. 5.11 that reports the normalized Dolph-Tschebyscheff coefficients for an array with 11, 21 and 31 elements; each slot is associated with a coefficient that represents the power the slot has to radiate [51]. As N increases, the power is spread over a larger number of slots and the curve in Fig. 5.11 becomes flatter: the difference between adjacent coefficients decreases, hence the power distribution needs to be implemented with a higher

accuracy, being the slot geometrical dimensions related to the efficiency and in turn radiated power.

As example, Fig. 5.12a reports the Dolph-Tschebyscheff power distribution of a 20 element array where 10% of the input power is dissipated in the terminating load. The initial and final slots radiate a small amount of power, while the most power is radiated in the central part of the array. The Dolph-Tschebyscheff coefficiencts are symmetric with respect to the center of the array: for each slot of index (+n) that radiates a certain amount of power $|a_n|^2/2$, there is a corresponding slot (-n) on the opposite side of the array that radiate the same power $|a_n|^2/2$. However, the travelling wave exciting the slots is attenuated as it propagates along the waveguide, hence the slot efficiencies in Fig. 5.12a are not symmetric but shifted toward the terminating load: the (-n)-th slot closer to the array input is excited by a larger power and therefore needs to be designed with a lower efficiency with respect to its corresponding (+n)-th slot, that also radiates an $|a_n|^2/2$ power, closer to the array terminating load.

To find the slot geometrical dimensions corresponding to the radiation efficiencies of Fig. 5.12a, the look-up table of Fig. 5.12b is built with the aid of HFSS simulator. The slot is moved along the waveguide transverse direction, from the center, where the slot does not radiate, toward the side wall. For each offset step, the length is iteratively adjusted to keep the resonance at the desired frequency (i.e., 94 GHz), and a value of efficiency is extracted from the simulator. In order to accurately implement the Dolph-Tschebyscheff distribution of Fig. 5.12a, the slot width was kept constant to 10 μm for all the slots: narrower slots would be too sensitive to manufacturing tolerances on the slot width, while wider slots would exhibit a too sharp variation of the efficiency with the offset (several percent for an offset variation of few microns) and would thus be too sensitive to manufacturing tolerances on the slot offset. The bending down of the slot efficiency for normalized offsets larger than 0.1 is due to the higher reflection losses caused by the slot (the port impedance used in simulation was not adjusted for each slot offset as that would not be realistic in the design of a frequency scanning array).

5.4.1 Numerical optimization for multiple reflections

The design of a Dolph-Tschebyscheff array starts with fixing the number of radiating slots, the power to be dissipated in the terminating load and the desired side lobe level; after that, the normalized powers (i.e., efficiencies) radiated by the slots are computed by the correspondent Dolph-Tschebyscheff polynomial coefficients [51]. However, resonant slots cause a

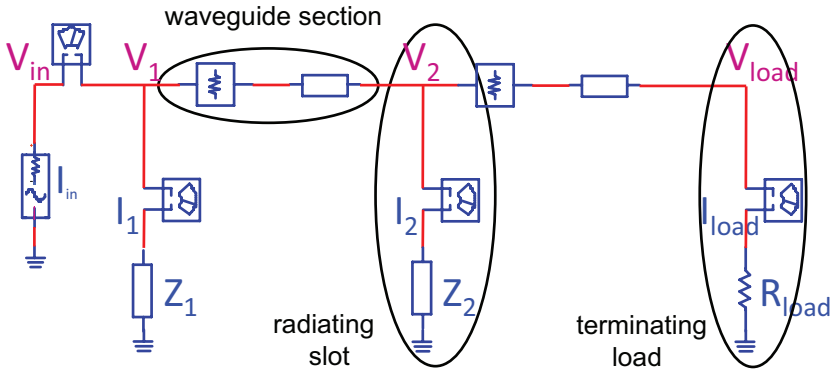


Figure 5.13: ADS schematic circuit used for reducing multiple reflection between slots at resonance (broadside radiation).

perturbation in the superficial currents flowing on the top face of the waveguide and introduce multiple reflection between adjacent slots, causing the slots to radiate a different amount of power than the designed one.

In order to obtain an accurate Dolph-Tschebyscheff distribution of the radiated powers, the mismatch caused by each slot needs to be accounted for. Using Agilent ADS simulator, the array is modelled at the broadside frequency using the schematic circuit of Fig. 5.13. The lossy waveguide is represented as a cascade of lossless transmission lines connected in series with an attenuator: the electrical delay of the line is calculated combining eq. 5.13 and 5.3 (the spatial harmonic m=+1 is considered), while the corresponding losses are computed according to the measured attenuation constant of Fig. 3.18b. Each slot is modeled as a parallel impedance, whose resistive part [51] is found by equating the slot radiated power (i.e., Dolph-Tschebyscheff polynomial coefficient) to the resistance dissipated power [168–170], while the reactive part is given by [166, 167]. On the right side of Fig. 5.13, another resistor is added which represents the terminating load of the travelling wave array.

Therefore, a numerical optimizer within the ADS environment is employed to tune the values of the resistances. For each resistor, the simulator computes the voltage accross it and the current flowing thru it: the power dissipated by each element is calculated and compared to the desired Dolph-Tschebyscheff power distribution, normalized to the sum of the powers dissipated in the resistors (i.e., radiating slots and terminating load) and in the attenuators (i.e., waveguide losses). The iterative optimization procedure converges when the distance between the power radiated by each slot

Table 5.2: Design parameters of the Dolph-Tschebyscheff array using a DRIE waveguide.

number of slots	20
array length (mm)	47[1]
array width (mm)	0.56
slot width (μm)	10
minimum slot length (μm)	598
maximum slot length (μm)	611
minimum single slot efficiency (%)	0.01
maximum single slot efficiency (%)	9.00
slot period (μm)	1613
side lobe level (dB)	30
power delivered to the load (%)	10

[1] including the transitions

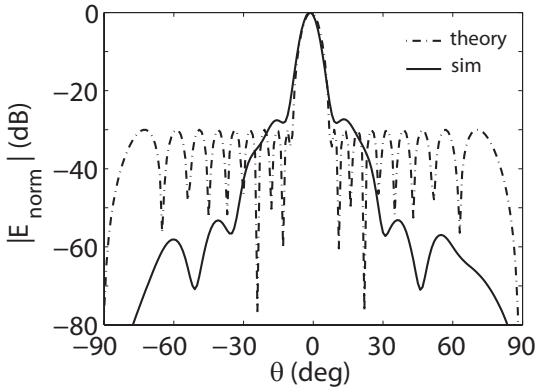


Figure 5.14: Theoretical and HFSS simulated (H-plane) radiation pattern of the Dolph-Tschebyscheff array using a DRIE waveguide.

and the ideal Dolph-Tschebyscheff distribution is within the chosen error. The optimizer returns, for each slot, the optimal value resistance which also takes into account multiple reflections. The resistance is associated to a radiation efficiency, and therefore, through the look-up table of Fig. 5.12b, to the slot geometrical dimensions (i.e., lengths and offsets).

The parameters of the Dolph-Tschebyscheff array designed with the above-described flow are summarized in Table 5.2; the radiation pattern computed with HFSS is shown in Fig. 5.14, and compared to theory. The agreement for the main lobe is satisfactory, but not for the side lobes: the theoretical radiation patter shows 18 side lobes in total (i.e., number of slots minus two), but only few of them are reconstructed by HFSS, which is probably not able to simulate radiation from the low-efficiency initial and final slots in such a long structure.

When compared to the simulated pattern of the uniform offset arrays reported in Fig. 5.10a and 5.10b, the Dolph-Tschebyscheff array shows a side lobes level -14.5 dB lower (-27.5 dB compared to -13 dB) due to the power distribution implemented. The HPBW is 4.4° higher (7.9° compared to 3.5°) because of the use of a lower number of slots (a 20 slot uniform array would exhibit a HPBW of 5.1°) and of the Dolph-Tschebyscheff tapering.

5.5 Antenna measurement setup

In order to perform radiation pattern measurements of on wafer antennas [171, 172], a near field system developed at Delft University of Technology was used [173]. The system is reported in Fig. 5.15. The antenna under test (AUT) is connected to one port of the PNA [174], while the other port is connected to an open-end WR-10 air-filled waveguide, which acts as a probe antenna, sampling the electric field in the near region of the AUT on a rectangular plane at a fixed step (i.e., $\lambda_0/2$), as showed in Fig. 5.15d. The far field is then calculated using a fast Fourier transform (FFT) algorithm. Note that the chuck which holds the antenna wafer in place is made of metal, so that an antenna is automatically grounded when placed for measurements even though it was designed on an ungrounded substrate.

The vertical distance between the probe antenna and the AUT is determined according to two contrasting requirements. The distance should be small in order for the probe antenna to sample the field in the near region of the AUT. When the distance is too small however, the near field of the AUT is modified by the presence of the probe antenna, and the reconstructed far field is therefore altered. On the other hand, the distance should be large for the probe antenna to work in its far field region (only the AUT is required to work in its near field region). As the distance increases however, a larger near field scanning plane is required to allow the field of the AUT to drop below a certain magnitude (usually, -30 dB) with respect to the peak, increasing the measurement time of a square factor. As best choice therefore, a vertical distance from the AUT equal to the start of the far field region of the probe antenna is considered during measurements.

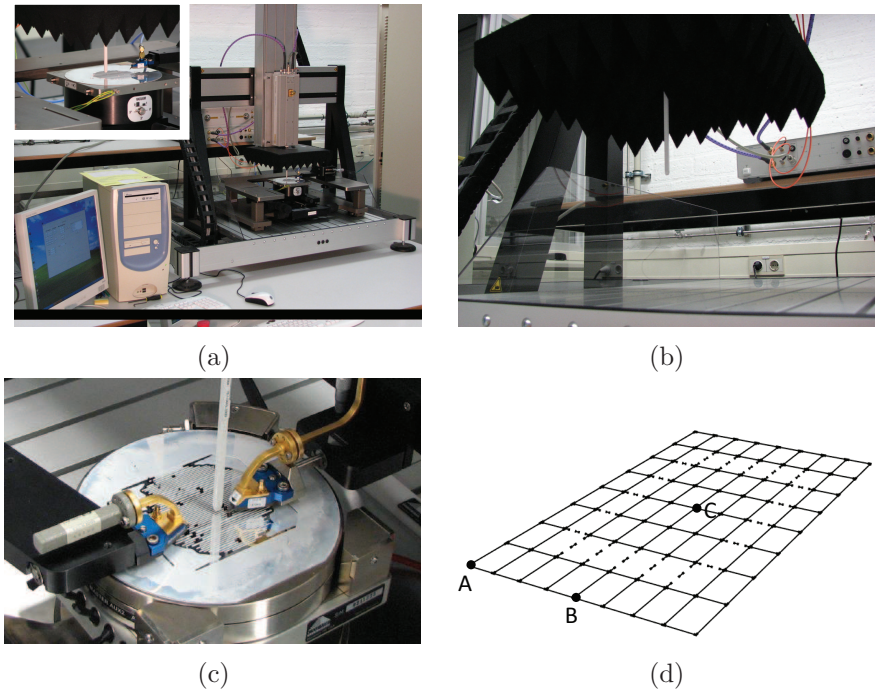
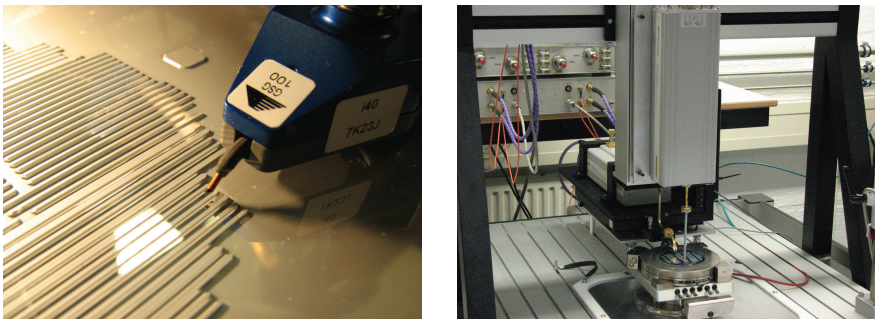


Figure 5.15: Near field measurement system: (a) setup overview, (b) detail of the waveguide probe antenna, (c) antenna under test detail, and (d) near field scanning plane. The metal chuck under the wafer acts as a back-reflector. Point A is at the edge of the scanning plane, point B at the middle along one scanning direction, point C where the AUT is located.

5.6 Frequency scanning array measurements

KOH and DRIE arrays with uniform offset and with a Tschebyscheff power distribution are experimentally characterized in terms of conducted (i.e., S-parameters) and radiated (i.e., employing a near-field antenna system) measurements. The S-parameters are measured with an Agilent PNA-X platform [175] using mm-wave module extenders (e.g., WR-10) from OML [176], and the coplanar to waveguide transition is contacted using a Cascade Microtech infinity probe [103] (see Fig. 5.16a).

The radiation performances are evaluated with the custom near-field antenna system described in section 5.5, where an open ended WR-10 waveguide probe from NSI [177] is used to sense the field above the structure.



(a) (b)

Figure 5.16: (a) zoom on the coplanar probe above KOH waveguides, and (b) a test wafer under the near field measurement setup.

The antenna is terminated on the other side on a second waveguide to CPW transition: the 50 Ω terminated load is either provided by anoter infinity probe that contact the transition (uniform offset arrays, KOH and DRIE) or by an integrated resistor connected at the end of the CPW transition between the signal and the ground plane (Dolph-Tschebyscheff array). The near field scan is performed over a 40 mm × 20 mm plane at a distance of approximately 5 mm from the antenna. Note that the proximity of the on-wafer feeding probe (see Fig. 5.16b) limits the near field scanning plane and therefore reduces the accuracy of the side lobes close to the end-fire directions in the reconstructed far field radiation pattern [178].

5.6.1 KOH uniform offset array

Three examples of uniform offset KOH etched arrays were manufactured and measured with different length and slot count, namely 12 (Fig. 5.17a), 24 (Fig. 5.17b) and 36 (Fig. 5.17c) elements. The energy was fed inside the structures using the coplanar to waveguide transition reported in Fig. 5.17d and analyzed in chapter 4.

The shift of the broadside frequency 1.2 GHz lower than the designed value (i.e., 94.4 GHz) can be explained by inaccuracies of the grinding back step of the manufacturing process (see section 3.2.1) for KOH waveguides. An increase in the waveguide equivalent width of 11 μm with respect to the expected value (i.e., 560 μm) corresponds to a substrate 15.5 μm thicker, as waveguide width and substrate height are related in the KOH process due to the oblique etching angle. As eq. 5.13 still holds and the slot distance d is fixed by the array geometry, the ratio f_{co}/f_c in λ_{gc} needs to stay constant,

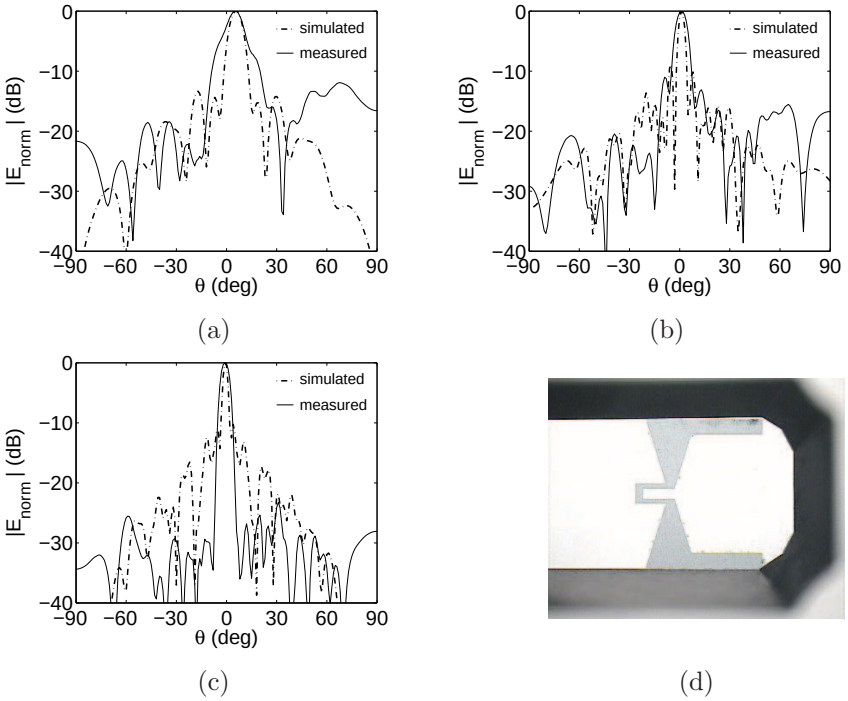
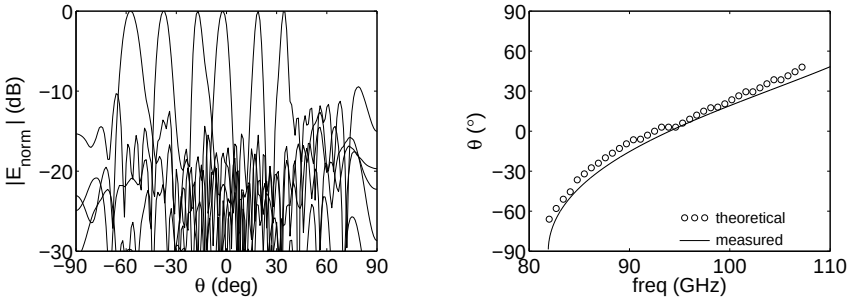


Figure 5.17: Radiation pattern of a KOH uniform offset array at broadside (93.2 GHz) with: (a) 12, (b) 24, and (c) 36 elements; the coplanar to trapezoidal waveguide transition used (d): metal in white, waveguide side walls in black, transition slot in grey.

and at a change of waveguide width of 11 μm, contained in f_{co}, corresponds a change of f_c of 1.2 GHz.

The discrepancy in the beam width and side lobes between simulations and measurements can be instead explained by the small length, comparable to the array length, of the scanning plane available for the near field measurements: the presence of the wafer probe limits the mechanical movements of the scanning probe antenna (see Fig. 5.16b), and results in a poor angular resolution and accuracy toward end-fire direction of the reconstructed radiation pattern. Specifically, the 12 slot array was measured using 21 points longitudinally and 21 points transversally spaced of half a wavelength at 100 GHz, for a scanning plane 30 mm x 30 mm large; the field decay is only -6 dBc in the longitudinal direction and -15 dBc in the transverse direction. The 36 slot array was measured using 61 points lon-



(a) (b)

Figure 5.18: KOH uniform offset 36 element array: (a) radiation pattern at different frequencies and (b) scanning angle versus frequency.

gitudinally and 21 points transversally spaced of half a wavelength at 100 GHz, for a scanning plane 90 mm x 30 mm large; the field decay is -28 dBc in the longitudinal and -16 dBc in the transverse direction.

The 36 elements uniform offset array (Fig. 5.17c) exhibits a measured half-power beam-width of 5°, which corresponds to a directivity of 13 dB according to eq. 5.28 (directivity could not be directly measured). As already discussed, this result is an underestimation of the directivity as the equation hold only for uniform arrays, where all the slots radiate the same amount of power, while the proposed array only exhibits a uniform offset of the slots. In Fig. 5.18a the radiation pattern for different frequencies (i.e., scanning angles) is reported: the main beam scans from an angle of -58° at 82.7 GHz to +34° at 103.5 GHz (see Fig. 5.18b), achieving a beam steering capability of 92° with a bandwidth of 20.8 GHz and a side lobe level (SLL) of -23 dB. A summary of the array performances is reported in Table 5.3.

5.6.2 DRIE uniform offset array

Fig. 5.19a reports the normalized radiation pattern of a DRIE integrated array, measured and simulated, with a uniform offset distribution. Broadside radiation occurs at 94.5 GHz with a SLL of -13 dB, the HPBW is 3.9° and corresponds to a directivity of around 14.2 dB.

The theoretical [59], simulated and measured scanning angles (i.e., the direction of the main beam in the radiation pattern) versus frequency are reported in Fig. 5.19b. Considering frequency modulated continuous-wave applications where a side lobe level of at least 10 dB is required [179], the scanning range of the proposed array goes from almost -36° at 87 GHz to

Table 5.3: Measured performances of a KOH uniform offset 36 element array, as designed in Table 5.1.

array type	uniform offset	
waveguide etching	KOH	
	simulated	measured
center frequency (GHz)	94.4	93.2
scanning angle (°)	86	92
bandwidth (GHz)	20	20.8
HPBW (°)	3.5	5
SLL (dB)	13	23
directivity (dB)	15	13[1]
gain (dB)	3.9	

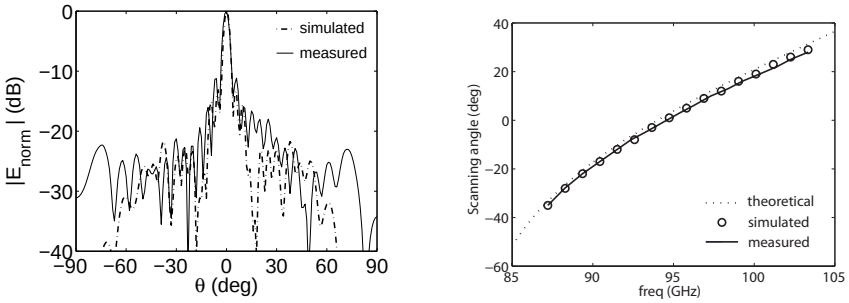
[1] extracted from the measured HPBW

Table 5.4: Measured performances of a DRIE uniform offset 29 element array, as designed in Table 5.1.

array type	uniform offset	
waveguide etching	DRIE	
	simulated	measured
center frequency (GHz)	93.4	94.5
scanning angle (°)	63	63
bandwidth (GHz)	80	17
HPBW (°)	3.5	3.9
SLL (dB)	13	13
directivity (dB)	15.8	14.2[1]
gain (dB)	5.8	

[1] extracted from the measured HPBW

+27° at 103 GHz; the scanning capability is thus 63° using a frequency bandwidth of 17 GHz (relative bandwidth of 17%). The performances of the DRIE uniform offset array are reported in Table 5.4.



(a) (b)

Figure 5.19: DRIE uniform offset array: (a) broadside (94.5 GHz) radiation pattern and (b) scanning angle versus frequency.

5.6.3 DRIE Dolph-Tschebyscheff array

Fig. 5.20a reports a comparison between simulations and measurements of a DRIE Dolph-Tschebyscheff array. The SLL is -23 dB at the broadside frequency (i.e, 96 GHz); the HPBW is 8.5°, higher than the DRIE uniform offset array presented in section 5.6.2 because of the Dolph-Tschebyscheff tapering and the use of a lower number of slots (see Table 5.1 and 5.2). It is interesting to notice that all the side lobes in Fig. 5.20a have almost the same height, as the theory of a Dolph-Tschebyscheff array predicts [50]. The good agreement between the simulated and measured main beam provides a further validation of the accuracy of the integration process described in section 3.3.

In Fig. 5.20b the radiation patterns for different frequencies are reported, and in Fig. 5.20c the theoretical [59], simulated and measured scanning angles are shown: good agreement of the angles is observed. The scanning angle goes from -46° at 87 GHz to 42° at 109 GHz, for a beam steering capability of 82° using a frequency bandwidth of 22 GHz (relative bandwidth 23%). A shift of 1.5 GHz was observed between the simulated (94.5 GHz) and measured (96 GHz) broadside frequency, which can be explained by manufacturing tolerances in the order of 1 μm for a full mask process, and uncertainties in the knowledge of the deielectric constant of the silicon in the order of three tenths (a low frequency value was used in the array design) that changes the broaside direction according to eq. 5.13.

Fig. 5.21 reports the simulated peak gain of the array (without transition), with a maximum value of 6.9 dB at broadside and a 3 dB bandwidth of 9 GHz from 90 to 99 GHz, limited by the use of resonating slots as ra-

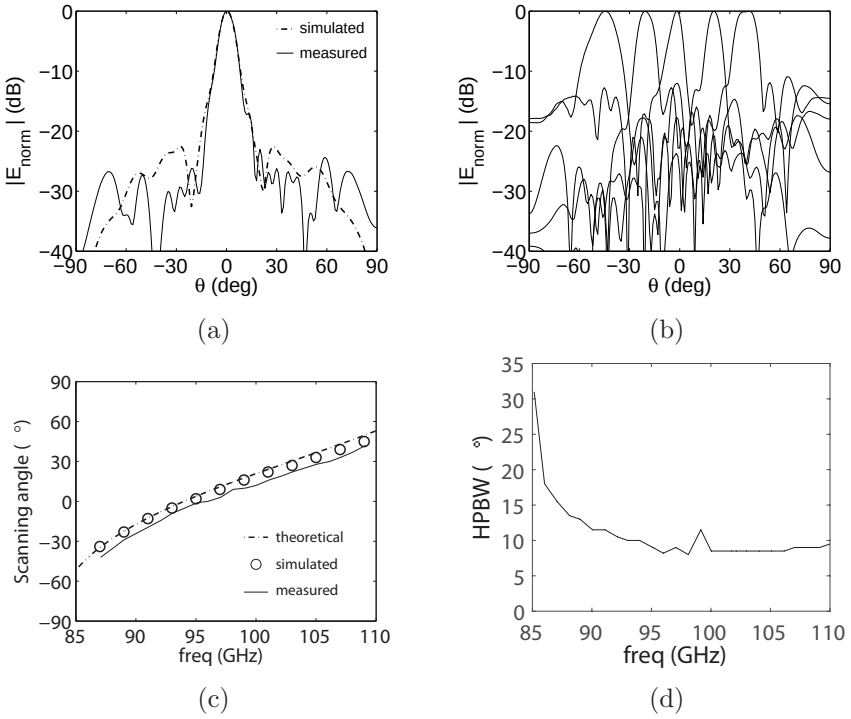


Figure 5.20: DRIE Dolp-Tschebyscheff array: (a) radiation pattern at broadside (96.0 GHz) and (b) at different frequencies, (c) scanning angle and (d) HPBWsimulated gain versus frequency.

diating elements, which exhibit a small resonating bands of few gigahertz. Considering an extracted directivity of 12.4 dB, the array losses are in the order of 5.5 dB. The coplanar to waveguide transition feeding the array account for 0.6 dB dB of losses (see section 4.4.1). The distance between the feeding transition and the last slot of the array is around 37 mm, resulting in waveguide losses in the order of 0.12 dB/mm * 37 mm = 4.4 dB (see section 3.5.1). The remaining (5.5-4.4-0.6) = 0.5 dB are dissipated in the load, corresponding to a P_l of approximnately 10%. A direct measurement of the array gain is presented in section 6.3.2.

The input matching for the array at the coplanar port (i.e., including the transition described in chapter 4) is below -15 dB in the frequency range between 80 and 110 GHz (see Fig. 5.22a). The ripples that can be seen around 96 GHz are caused by multiple reflections between the slots, mini-

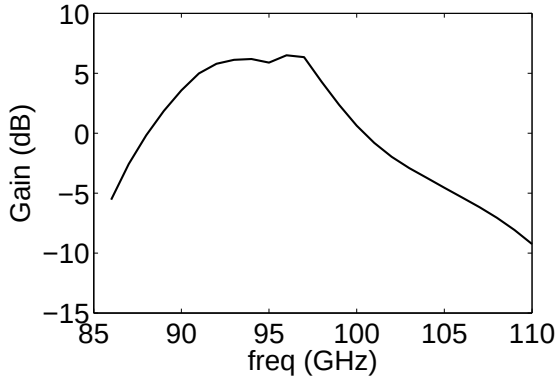


Figure 5.21: Simulated gain of the Dolph-Tschebyscheff array; no direct measurement of the antenna gain could be carried out with the near field setup of section 5.5.

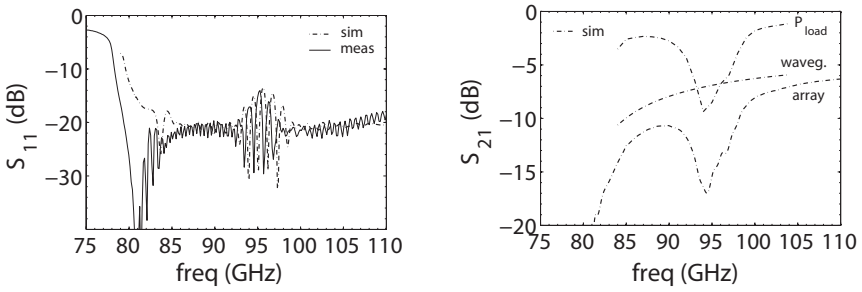


Figure 5.22: DRIE Dolph-Tschebyscheff array: (a) HFSS simulated and (b) measured S-parameters. In (b), the S_{21} of the whole array and of a waveguide of equal length (including transitions) is reported: their difference represents the power delivered to the load. Because of the integrated matched load on the terminating port of the array, S_{21} could not be experimentally determined.

mized but not eliminated through the optimization routine of section 5.4.1, whose distance becomes exactly one guided wavelength at that frequency (see eq. 5.13).

The insertion loss of the array could not be directly measured because of the presence of the matched load and is reported from simulations in

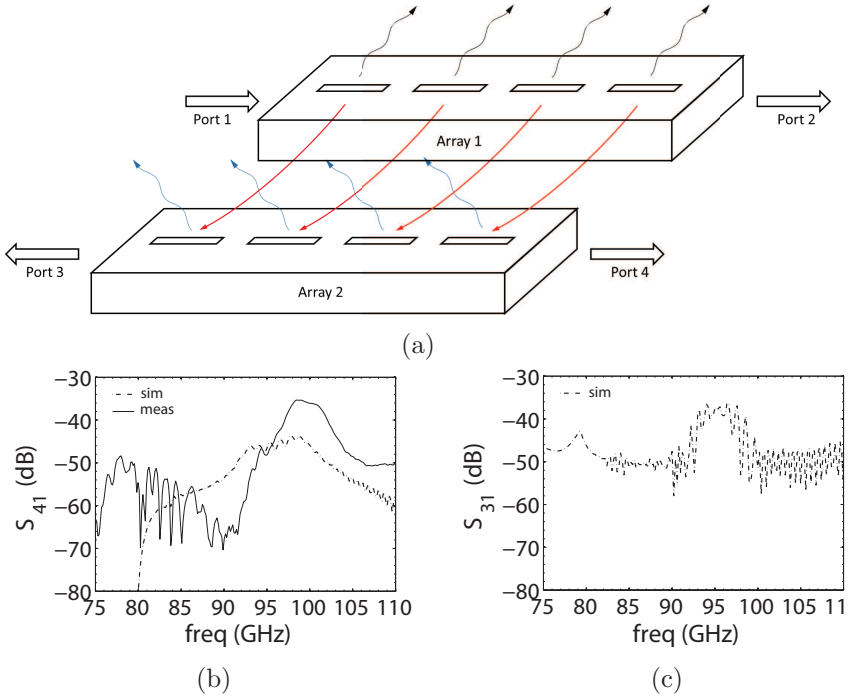


Figure 5.23: DRIE Dolph-Tschebyscheff array: (a) two closely spaced array, cross-coupling for reversed (b) and non-reversed (c) feeding. In (a), part of the energy radiated by the Tx (in black) couples with the Rx (in red), and is reirradiated (in blue) or delivered to the Rx output. The matched loads are on port 2 and 3 in (b) and on port 2 and 4 in (c).

Fig. 5.22b. The S_{21} of the array resembles the one of a waveguide (without slot) close to cut-off, but presents a dip of about 7 dB around 95 GHz (the resonance frequency of the slots), that corresponds to the power radiated by the array at broadside, and is almost identical to the simulated gain of the array (i.e., 6.9 dB). To better understand the situation, the S_{21} of a waveguide as long as the array is added in Fig. 5.22b, in order to account for dielectric and metallic losses into the array. As in a lossless array the input power is either radiated or dissipated inside the load, the P_l of the lossy array can be calculated by subtracting the S_{21} of the waveguide (i.e., the losses) from the S_{21} of the array, hence obtaining the S_{21} of the lossless array. At 95 GHz, the value is -9.4 dB (see Fig. 5.22b), which corresponds to a P_l of 12% and well matches the design target of 10% at broadside.

Table 5.5: Measured performances of a DRIE Dolph-Tschebyscheff 20 element array, as designed in Table 5.2.

array type	Dolph-Tschebyscheff	
waveguide etching	DRIE	
	simulated	measured
center frequency (GHz)	94.4	96.0
scanning angle (°)	84	82
bandwidth (GHz)	22	22
HPBW (°)	7.9	8.5
SLL (dB)	30	23
directivity (dB)	13.4	12.4[1]
gain (dB)	6.5	6.8[2]

[1] extracted from the measured HPBW
[2] measured in section 6.2.2

In FMCW radar applications with separate transmitting and receiving antennas it is crucial to guarantee a good isolation between closely spaced elements (see Fig. 5.23a), especially when different antennas are used to transmit and to receive the signal. Fig. 5.23b shows the cross-coupling of two reversed arrays, probed at opposite sides, and spaced at distance of a quarter lambda at 100 GHz (the physical dimension of the measurement probes did not allow probing both arrays from the same side, as in real applications). As a result of the opposite probing, at each frequency the Tx and Rx look at complementary angles: the power radiated by the Tx at an angle of θ couples to the Rx and is partially reirradiated at an angle of $90° - \theta$ before reachng the output probing point. Since very narrow slots are opened on the top face of the waveguide, the near field coupling is weak: the average measured coupling is well below -40 dB, with a peak of -35 dB around 100 GHz. Note that in simulations the cross-coupling peak occurs at 96 GHz, where both arrays radiate energy in the same direction (i.e., broadisde), while in measurements the peak is shifted toward 100 GHz. For comparison, the simulation of the array cross-coupling for both arrays are fed by the same side, which corresponds to the practical user case is reported in Fig. 5.23c: the cross-coupling is similar to Fig. Fig. 5.23b, with a peak of -35 dB around 95 GHz.

Although the directivity could not be direclty measured, it is worth to report indirect results. Closed form equations for a Dolph-Tschebyscheff power distribution [50, 51] give a directivity of 12.4 dB, which is close to 13.4 dB obtained in simulation. A summary of the overall performances of the array is reported in Table 5.5.

5.7 Conclusions

Employing two novel technologies developed at Dimes and MiPlaza labs, travelling wave arrays based on a slotted waveguide topology were designed, integrated and characterized. A parametric study of the power radiated by each slot was performed, and the results were used for the implementation of a power distribution according to the Dolph-Tschebyscheff coefficients, which minimizes all the secondary lobes in the far field pattern. Design equations for frequency scanning arrays in waveguide were obtained, and a general design procedure was introduced to facilitate the choice of the waveguide cut-off and dielectric material once the operating frequency has been fixed.

Measureement results of uniform and Dolph-Tschebyscheff arrays using KOH and DRIE waveguides were presented, showing good performances of the designed structures in terms of scanning angle, beam width and side lobe levels. In particular, the DRIE technology allows the patterning of metal structures with an accuracy around 0.5 μm and a minimum gap width of 10 μm, one order of magnitude better than what offered by a PCB process. As the higher accuracy enables a finer tapering of the power radiated by each antenna, DRIE arrays can be designed with a larger number of elements (20) than PCB arrays (typically less than ten), which reflects in smaller beam widths (8.5°) and better side lobe levels (-23 dB).

The manufacturing accuracy together with the demonstrated good correspondence between measured and simulated results indicates that the proposed technology can be a potential candidate for the integration of antennas in mm-wave high performance systems.

Chapter 6

94 GHz radar demonstrator

6.1 Introduction

The development of integrated millimeter-wave systems has recently triggered the interest of a wide research community due to the large worldwide license-free bandwidths that are available in the mm-wave region, allowing to target high performance systems for industrial, scientific and medical applications, including broadband communication at 60 GHz and 122 GHz, imaging radar at 96 GHz and 140 GHz, and radio location at 120 GHz [105].

Mm-wave systems employing multiple antennas or smart antennas with electrical beam steering capabilities require technology platforms for the realization of antenna beam forming networks (e.g., phased array) and system level assembly (e.g., interfacing high gain antennas to ICs). On the other hand, technology platforms based on PBCs suffer from poor geometrical resolution which limits the component bandwidths and from material softness that complicates the system assembly [43].

In this chapter, the potentialities of the DRIE waveguide technolgoy for the realization of mm-wave systems based on narrow beamdwidth active antennas are explored. As example, building blocks of a passive beam forming network for high gain array antennas with fixed radiating beam are designed and experimentally characterized. Afterwards, a highly co-integrated beam steering antenna prototype for 3D imaging based on a 94 GHz FMCW radar chip and a frequency scanning phased array antenna is assembled and tested.

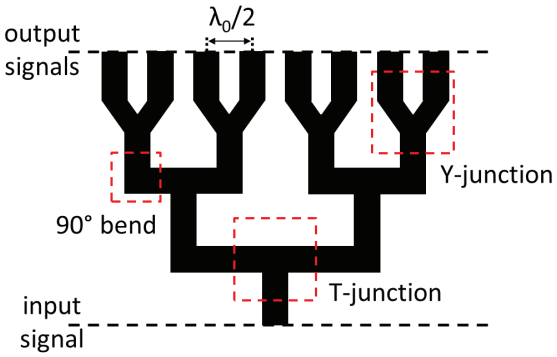


Figure 6.1: 1:8 balanced corporate power divider. As each splitting block preserves the longitudinal symmetry, the output signals are in phase.

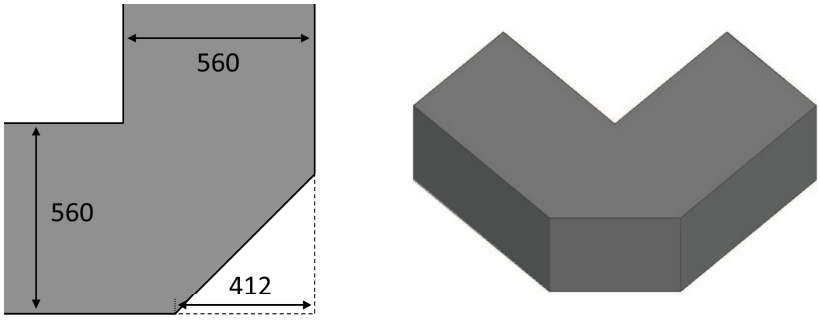
6.2 Corporate power divider

A balanced corporate power divider for the beam forning network of high gain antennas is illustrated in Fig. 6.1. The input signal propagating along a transmission line is progressively split into N in-phase output signals along the tree branches; the design is balanced in the sense that the electrical distance from the input to each output is constant and hence N in-phase signals are generated.

The power splitter of Fig. 6.1 can be used as passive BFN for the excitation of a linear array of antennas for broadside radiation. Moreover, if the N antennas at the output of the power splitter are replaced by N frequency scanning arrays, the antenna topology of Fig. 1.6b, but with steering capability only limited to one plane, is realized.

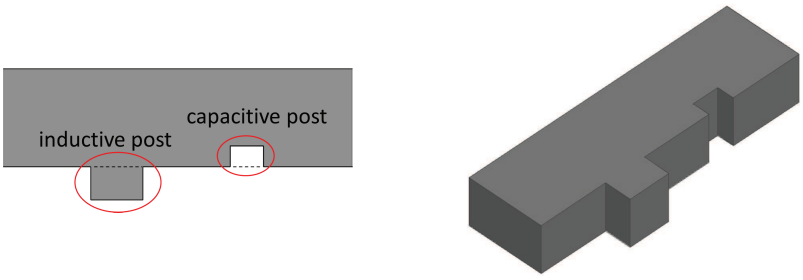
To split the signal and keep the geometrical longitudinal symmetry, the power divider makes use of a cascade of T-junctions and 90° bends (see Fig. 6.1), whose distance progressively decreases along the BFN. The last splitting of the signal requires the ability to implement one T-junction and two 90° bends in a limited space, as the array elements are spaced from each other half a free space wavelength to avoid grating lobes in the radiation pattern. When this is not possible (e.g., large width of the transmission line), the last signal splitting can be realized with a Y-junction component, which can be thought as the combination of a T-junctions and two 90° bend in a single and more compact element.

6.2.1 Design of Y- and T-junctions



(a) (b)

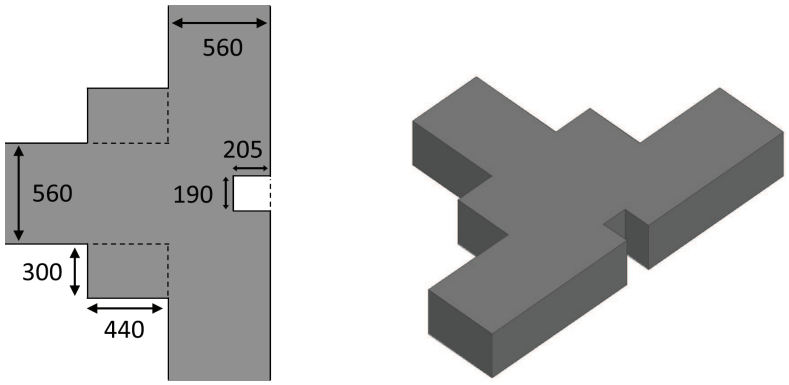
Figure 6.2: 90° bend: (a) top and (b) perspective view: corner mitering is used to achieve input matching. The dashed line in (a) corresponds to an unmatched 90° bend; dimensions are in micrometers.



(a) (b)

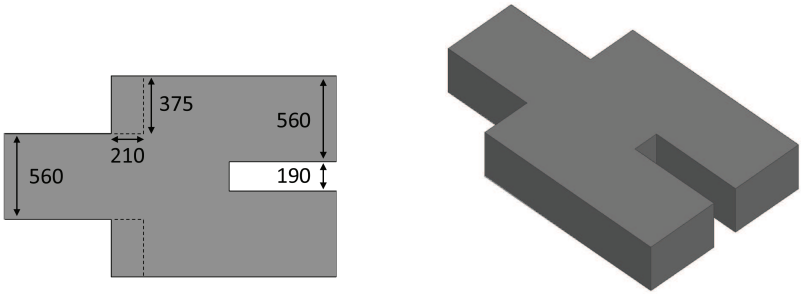
Figure 6.3: Reactive post: (a) top and (a) perspective view. The dashed line in (a) corresponds to waveguide with no reactive posts.

The DRIE technology presented in chapter 3 is employed for the design and realization of 90° bend, T-junction and Y-junction components in waveguide for WR-10 band operation. As transmission line, a waveguide



(a) (b)

Figure 6.4: T-junction: (a) top and (a) perspective view; a capacitive and an inductive post are used to achieve input matching. The dashed line in (a) corresponds to an unmatched T-junction; dimensions are in micrometers.

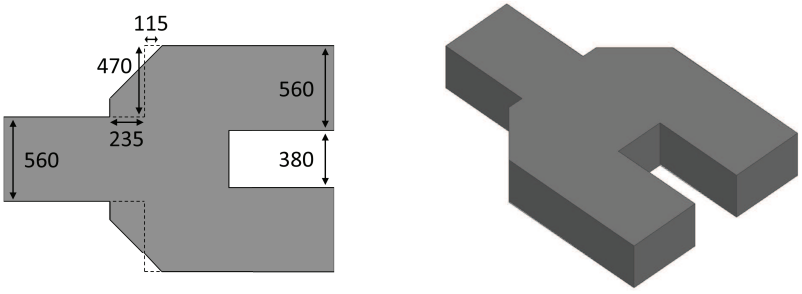


(a) (b)

Figure 6.5: Y-junction with a waveguide spacing of 190 μm: (a) top and (a) perspective view; an inductive post is used to achieve input matching. The dashed line in (a) corresponds to an unmatched Y-junction; dimensions are in micrometers.

of width 560 μm and height 280 μm (nominal cut-off frequency 77 GHz) is considered.

The design strategy of a 90° bend in waveguide resembles the one of bends in microstrip line [180]. The waveguide surface currents encounter a discontinuity in correspondence of the bend (see Fig. 6.1a), where the



(a) (b)

Figure 6.6: Y-junction with a waveguide spacing of 380 μm: (a) top and (b) perspective view; an inductive post is used to achieve input matching. The dashed line in (a) corresponds to an unmatched Y-junction; dimensions are in micrometers.

waveguide cross-section becomes larger and its (effective) impedance decreases [139]. To compensate for that, the 90° corner is mitered under an angle of 45°: a numerical simulator (i.e., HFSS) is employed to determine the exact amount of mitering that provides good input matching. The optimized dimensions of the 90° bend are reported in Fig. 6.2 together with a perspective view of the component.

In a Y- or T-junction component, the signal propagating along a waveguide is split in two in-phase signals propagating along the orthogonal direction. To compensate for the discontinuity and achieve impedance matching, reactive loading elements need to be used [180]. While bulk waveguides make use of snall capacitive posts placed inside the structure [181], only thru-wafer inductive and capacitive posts as the ones in Fig. 6.3 are considered for DRIE waveguides in order to keep the manufacturing process simple. Note that the width of the capacitive post is limited by the aspect ratio of DRIE trenches, and cannot be smaller than 280 μm high (see section 3.2.2).

The layout of a matched T-junction component is reported in Fig. 6.4. As the waveguide cross-section becomes larger in correspondence of the T-junction (capacitive loading, lower impedance), a capacitive post can be used [180]. From HFSS simulations, the etched post should be 60 μm wide (and 280 μm long), which however cannot be manufactured. To solve for this, the width of the post is set to its minimum value (i.e., 190 μm) and

two inductive posts (see Fig. 6.3a) are added half a cut-off wavelength from it to improve the matching (see Fig. 6.3a).

The layout of a Y-junction with a distance of 190 μm between the two branches is presented in Fig. 6.5. As the (minimum) trench width prevents the use of capacitive posts, the junction is matched by adding inductive posts as in Fig. 6.4a. When the distance between the Y-junction branches is enlarged of a factor two (i.e., 380 μm), good impedance matching can be achieved by using inductive posts in combination with corner mitering as in Fig. 6.6.

6.2.2 Measurement results

Bend and junction components were manufactured using the DRIE waveguide technology and measured in a back-to-back configuration using an Agilent E8361C PNA [143] and two Agilent mm-wave module extensions to cover the WR-10 band; coplanar to waveguide transitions (see chapter 4) were employed to interface the waveguide components to the planar ground-signal-ground (G-S-G) on wafer probe environment.

A perspective view of the manufactured T-junction component including 90° bends is reported in Fig. 6.7a. Above cut-off, the structure is well matched below -10 dB up to 109 GHz, with an insertion loss (single T-junction plus two 90° bends) of 1.0 dB at 110 GHz. Note that the measured cut-off frequency of the DRIE waveguide (i.e., 78.5 GHz) is 1.5 GHz higher than the nominal value as previously discusses in section 5.6.3.

The Y-junctions with waveguide spacing of 190 μm and 380 μm are reported in Fig. 6.8 and 6.9, respectively. The structures are matched from 78 to 110 GHz, with an insertion loss of 0.7 dB at 110 GHz.

Measured performance of the junction components are summarized in Table 6.1. Using these components, a beam forming network in waveguide for the excitation of an 8-element linear array with fixed radiating beam can be realized with an insertion loss of 5.9 dB at 110 GHz (i.e., three T-junctions and four Y-junctions).

6.3 94 GHz FMCW phased array radar

To further showcase the potentialities of the DRIE technology for beam steering mm-wave systems, a prototype of smart antenna in waveguide based on a 94 GHz FMCW phased array radar for imaging application was implemented.

The system architecture of the smart antenna is illustrated in Fig. 6.10: a saw-tooth FMCW signal is generated at 94 GHz, amplified and transmit-

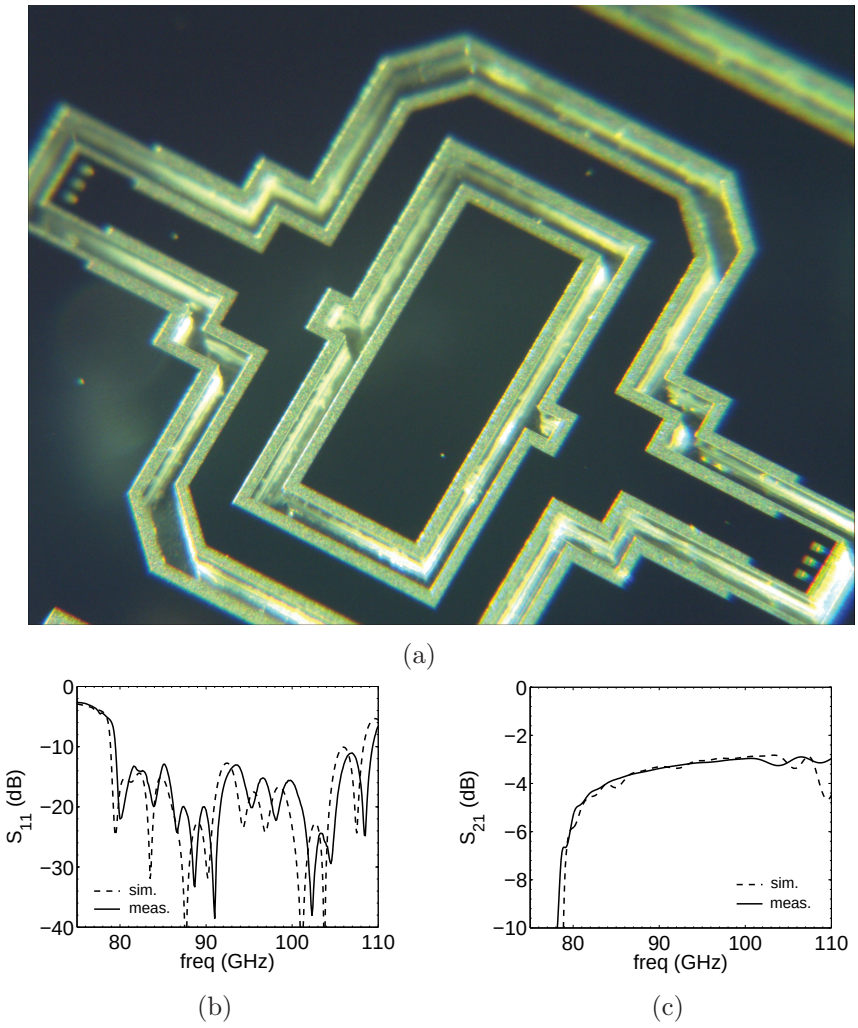


Figure 6.7: Two back-to-back T-junctions in silicon substrate integrate waveguide technology: (a) microscope photo and (b)-(c) S-parameters. As a consequence of the two step metallization process (see section 3.2.2), the first metal deposition is covered with an oxide layer and only the second metal deposition (around and inside the vertical trenches) is visible under the microscope.

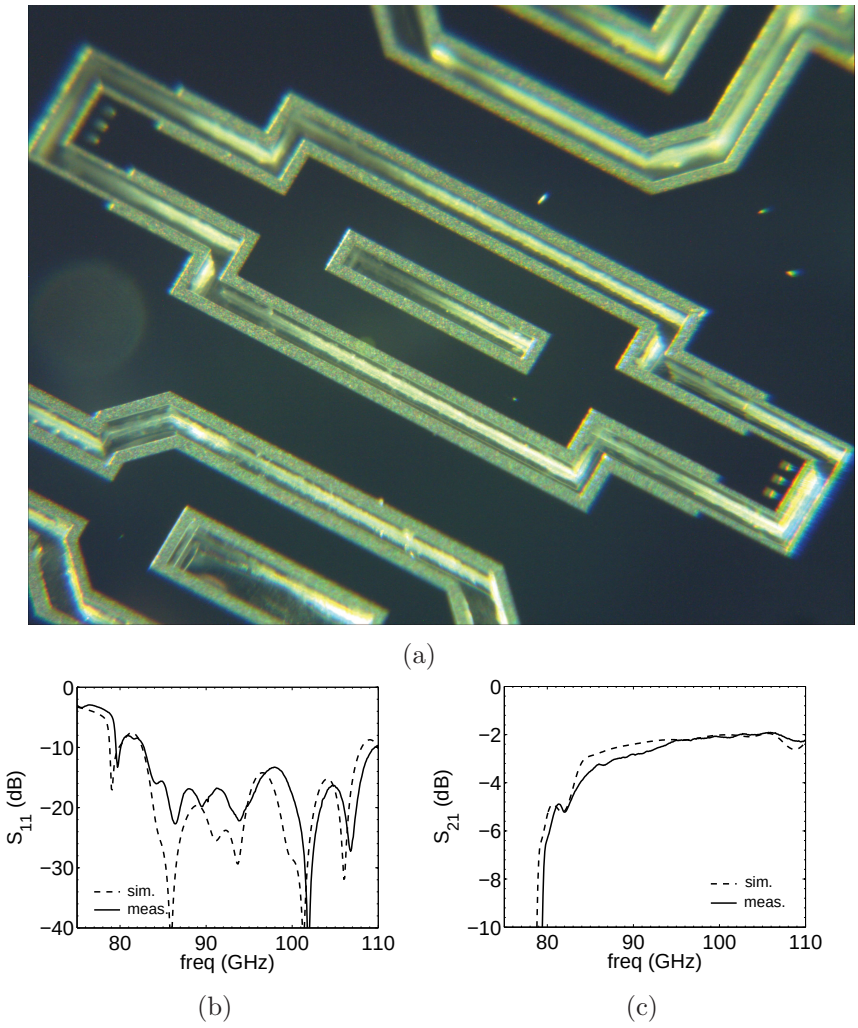


Figure 6.8: Two back-to-back Y-junctions with a waveguide spacing of 190 μm: (a) microscope photo and (b)-(c) S-parameters.

ted by a high gain phased array antenna. When hitting a target, an echo signal is scattered back and collected by a second phased array antenna. The received signal goes then through a noise amplifier and a down-converting mixer, whose other input signal is provided by the directional coupler in

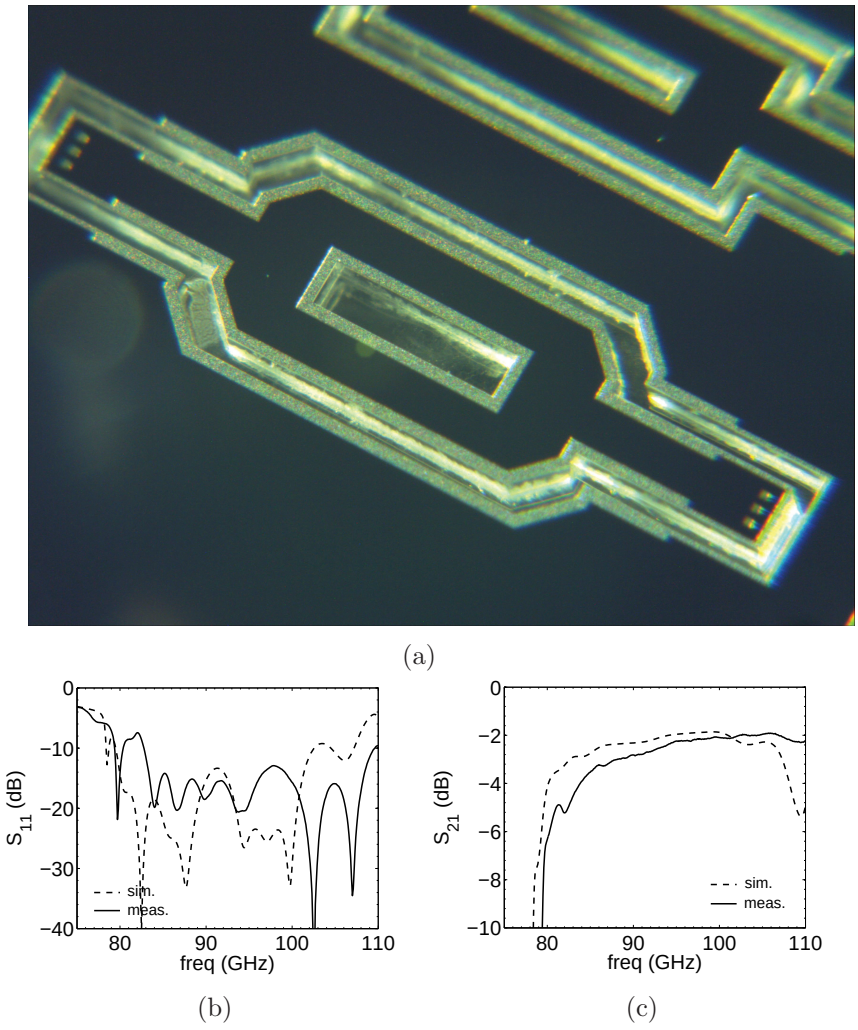


Figure 6.9: Two back-to-back Y-junctions with a waveguide spacing of 380 μm: (a) microscope photo and (b)-(c) S-parameters.

Table 6.1: Summary: performances of junction components in DRIE waveguide technology.

junction	T[1]	Y (750 μm)	Y (940 μm)
matching bandwidth[2] (GHz)	79-109	79-110	79-110
insertion loss[3] (dB)	1.0	0.7	0.7

[1] including two 90° bends
[2] S_{11} < -10 dB
[3] of a single component, at 110 GHz, de-embedded of the transition and waveguide sections

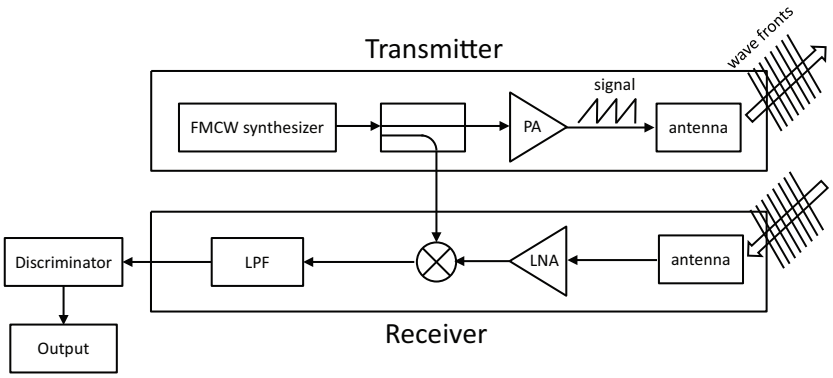


Figure 6.10: System architecture of the FMCW radar smart antenna, including: a power amplifier (PA), a low noise amplifier (LNA) and a low pass filter (LPF).

the transmitter path. After a filtering stage, the signal feeds a discriminator block and reaches the output stage, which provides the target 3D location.

To detect the target distance, the radar Tx channel generates a chirp signal with a linear variation of the frequency over time that is transmitted by the Tx phased array antenna. A fraction of this signal goes through the directional coupler to the Rx channel and is compared by the mixer block to the echo produced by the target. As the chirp frequency continuosly changes with time, the difference in frequency of the two signals is proportional to the round trip time of the signal propagating from the Tx antenna to the

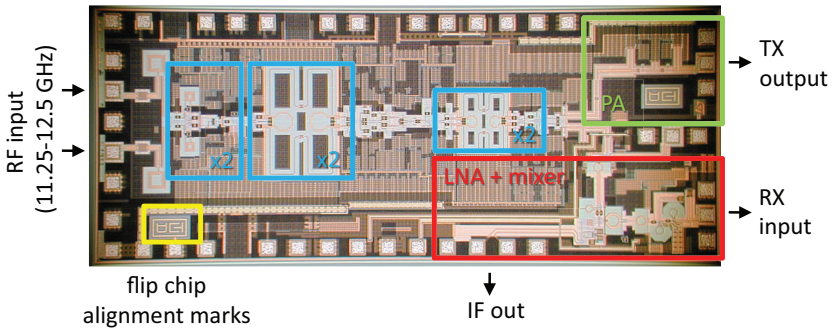


Figure 6.11: Radar chip: complete 94 GHz up-converter and receiver in Bi-CMOS 130 nm, integrated in ST 9MW technology.

target and back to the Rx antenna. The distance of the target is equal to the speed of light in vacumm times half the round trip time, while its angular position is determined by the phase distribution (in one plane) and the operating frequency (in the orthogonal plane) of the Tx and Rx frequency scanning phased array antennas.

6.3.1 System assembly

For performance optimization, the active radar transceiver and the passive high gain antenna are realized on different substrates and then interfaced together.

The transceiver chip, shown in Fig. 6.11, is manufactured in 130 nm Bi-CMOS technology. A single transceiver chip is 1.2 mm x 3 mm in size, and contains a PA, an LNA, a mixer, and three times-two multiplicator blocks that up-convert the FMCW input signal from 11.25-12.5 GHz to 90-100 GHz. The Tx and the Rx antennas are formed each by four linear arrays of frequency scanning arrays, placed in an interdigit configuration as in Fig. 6.12; with the spacing between two consecutive Tx (or Rx) frequency scanning arrays that needs to be smaller than half a free space wavelength. The possiblity of using an interdigit configuration which requires to accomodate one Tx plus one Rx antenna within half a free space wavelength was only made possible by the high dielectric constant of the silicon dielectric filling the waveguides.

The frequency scanning array makes use of the antenna layout described in chapter 5 and is interfaced in a broadband fashion to the active chip by means of flip chip assembly and of the planar transition presented in chapter 4. Flip chip interconnection is preferred to bond-wire or ribbon-

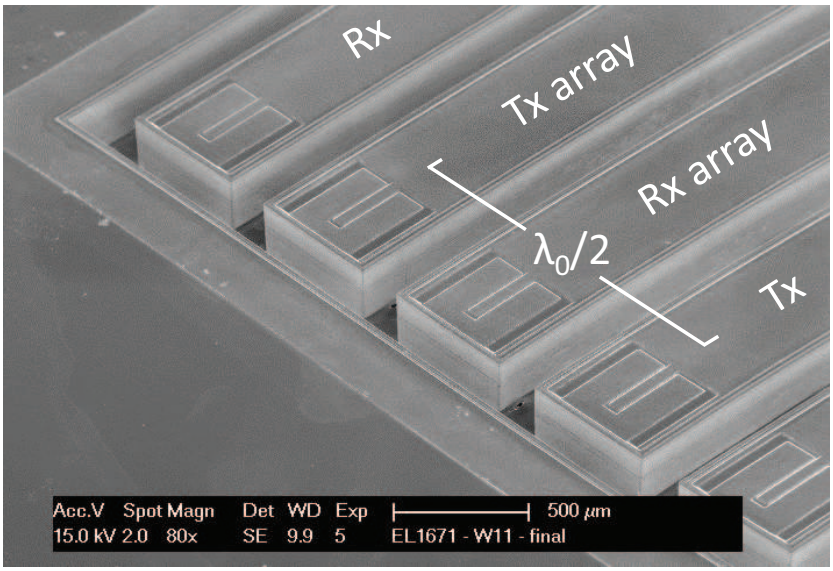
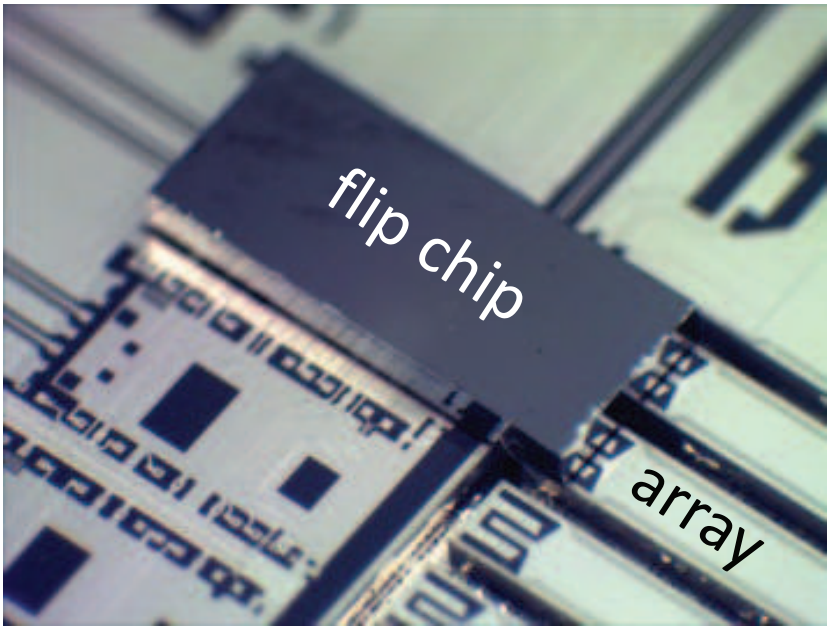


Figure 6.12: Radar antenna: the Tx and Rx frequency scanning arrays are placed in an alternate configuration; only five of the eight arrays are (partially) shown here.

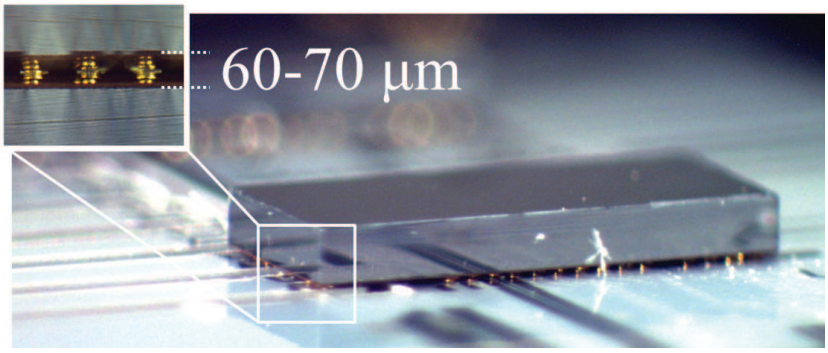
cord bonding techniques since it presents lower insertion losses and larger bandwidths at millimeter-waves. To motivate this, consider that the S_{21} of a series inductor in a 50 Ω system can be expressed by [182]

$$S_{21} = \frac{2Z_0}{2Z_0 + j\omega L} \tag{6.1}$$

At 94 GHz a flip-chip interconnection with 60 μm high solder bumps (self-inductance of 56 pH [65]) produces an insertion loss of 0.45 dB, while an interconnection based on a 0.5-1.0 mm long bond wire (wire diameter 25 μm, self-inductance 0.4-0.8 nH [64]) causes 8.2-13.7 dB of loss. Compensating capacitors in the order of few femtofarads at mm-wave can be added at the output of the bond wire, but this technique is only effective in a narrow bandwidth around the resonant frequency of the so-formed LC resonator. As example, using a metal-insulator-metal (MIM) capacitor and a 0.4 nH bond-wire with quality factors of 20 and 50 at 94 GHz [183], respectively, a 3-dB bandwidth of 14 GHz (relative bandwidth 15%) is obtained. As bond-wire interconnections at 94 GHz would limit the bandwidth of the developed broadband waveguide components, flip chip assembly is hence preferred.



(a)



(b)

Figure 6.13: Photo of the radar Tx-Rx unit: (a) top and (b) side view. The flip chip (in black) lies on top of two Dolph-Tschebyscheff waveguide arrays (in white).

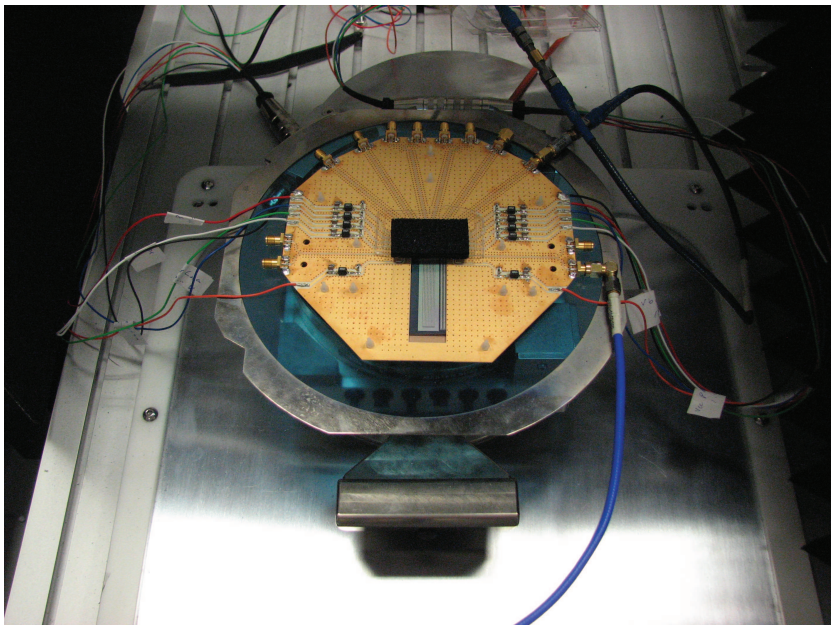


Figure 6.14: 94 GHz FMCW radar assembled on a PCB. A 0.5 cm layer of absorbing material (in black) is placed on top of the flip chip to damp radiation leakages of the coplanar to waveguide transition caused by the flip chip assembly.

A photo of the assembled radar frontend, with only one chip mounted on the antenna, is shown in Fig. 6.13: the FMCW chip (in black) is connected to a pair of Tx-Rx waveguide arrays using gold stud bumps with a height of 60-70 μm after thermo-compression, as shown in the inset of Fig. 6.13b. Such bumps are also used to connect dc biasing, radio frequency (RF) input and intermediate frequency (IF) signal lines to the FMCW chip.

Finally, the radar frontend was mounted on a PCB for DC and low frequency signal routing. Fig. 6.14 shows a photo of the 94 GHz FMCW radar system; because of limited accuracy (> 20 μm) of the flip chip machine, only one transceiver chip (instead of four) could be successfully mounted above the antenna, and only a single Tx-Rx channel, with (frequency) scanning limited to one dimension, was experimentally characterized.

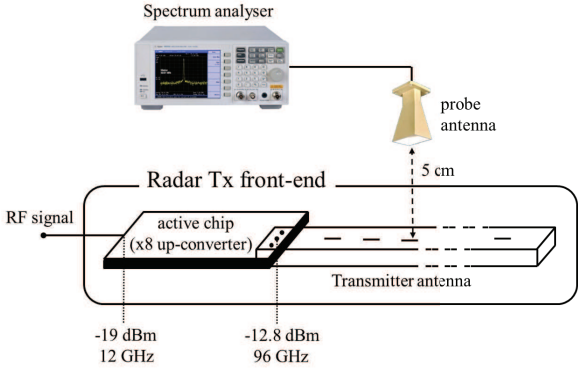
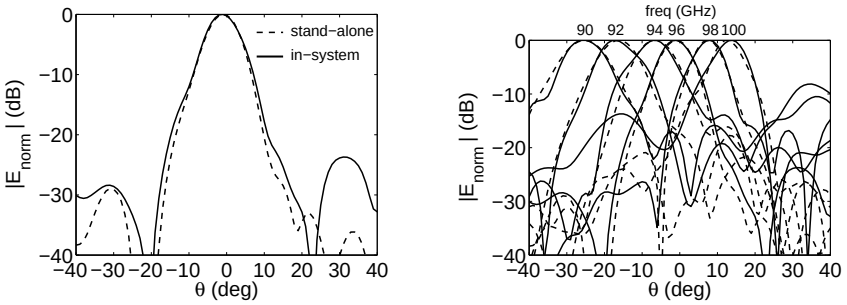


Figure 6.15: Measurement setup of the radar transmitter front-end at broadside. The power level and the frequency of the signal are also reported.



(a) (b)

Figure 6.16: Measured radiation pattern of the stand alone (before flip chip) and in-system (after flip chip): (a) at broadside frequency (i.e., 96 GHz) and (b) versus frequency.

6.3.2 Measurement results

To characterize the performances of radar Tx antenna and measure the gain of the Dolph-Teschebyscheff array, continuous wave signals were employed. The transceiver losses after flip-chip assembly were first characterized with on-wafer measurements on dummy silicon substrates (i.e., without antenna): feeding the circuit with a continuos wave signal of -19 dBm at 12 GHz, an output power of -12.8 dBm at 96 GHz was measured.

After the system assembly (i.e., IC with antenna), the output of the chip could not be accessed by wafer probes anymore, hence a radiation

measurement was carried out to verify the up-converter performances. A 10 dB standard gain horn antenna was placed above the center of the array at a distance of 15 cm, as shown in Fig. 6.15, and connected to a spectrum analyzer, which measured a received power P_r of -53.5 dBm at 96 GHz. The power P_t transmitted at the input of the antenna was then calculated using the Friss transmission equation [51] (all the terms are expressed in decibels):

$$P_r = P_t + \left(\frac{\lambda_0}{4\pi d}\right)^2 G_t G_r - IL_{trans} - IL_{wav} \tag{6.2}$$

where the distance d between the two antennas (i.e., 15 cm) was increased of $\lambda_0/3$ to account for the phase center shift of the horn antenna [51], the transmitter antenna gain is G_t, the receiver antenna gain is 10 dB, the transition insertion loss IL_{trans} is extracted from measurements, and IL_{wav} is the insertion loss of the waveguide section used to connect the horn antenna to the spectrum analyzer (waveguide attenuation constant 2.73 dB/m from component specifications). Assuming that the output power of the IC after dummy flip chip and antenna flip chip remains unchanged, a transmitter antenna gain of 6.84 dBm is obtained, which very well agrees with the value of 6.9 obtained in simulation (see section 5.6.3). Note that this number is a bottom line for the array gain: in fact, if the above assumption of equal output power of the IC is not true in reality, the array gain needs to be larger than 6.84 dB in order for the power meter to receive -53.5 dBm. Similar considerations apply in the case the power reaching the matched load on the other side of the array is higher than the designed 10%.

Note that eq. 6.2 is stricly true only in the far field region of the two antennas. Due to size limitations of the measurement setup, the array under test was used within its near field region (far field starting at around 1.6 m), but well outside its reactive region (arond 12 cm). To the best of the authors knowledge however, no straighforward formula exists for a power budget calculation in the near field of the AUT. The Friss formula is therefore only reported as a first order approximation, but nevertheless provides reasonable results for the transmitted power.

After this step, the horn antenna is replaced by an open-ended waveguide probe and the radiation pattern of the radar transmitter is measured with the near field system described in section 5.5. Fig. 6.16a shows a good agreement of the main beam in the far field pattern at broadside of the Dolph-Tschebyscheff array when standing alone and embedded in the system. The boresight direction is shifted of less than 1° in the whole range, which corresponds to an alignment error [184] of the center of the near field scanning plane with respect to the antenna under test of less than 200 μm

(the alignment was performed only by visual inspection).

The side lobe around -30° to the left of the main lobe is practically unchanged, while the side lobe on the right increases from -36 dB to -24 dB due to radiation from the flip-chip substrate. Note that the coplanar to waveguide transition that interfaces the active chip to the substrate is based on a resonant slot design, which normally radiates a small amount of energy (approximately $\epsilon_r^{(-3/2)}$ [185], i.e. 2.4%) into free space rather than inside the waveguide. HFSS simulations confirm that this fraction significantly increases when a component with a high dielectric constant (i.e., the active chip) is mounted on top of the transition (the soldier bumps height is only 60-70 μm). Since the power radiated by each array slot of the frequency scanning array is quite small (see Table 5.2), the transition contributes to the near field of the array by creating an unwanted side lobe around +30°. Therefore, the reconstructed far field of the radar transmitter is not accurate toward the +90° end-fire direction, and only the angular range between -40° and +40° is shown in Fig. 6.16b. Changing the frequency of the synthesizer from 11.25 GHz to 12.5 GHz, the direction of broadside radiation is steered: the main beam scans from -26° at 90 GHz to 14° at 100 GHz, for a total scanning capability of 40° using a frequency bandwidth of 11% (i.e., 10 GHz).

6.4 Conclusions

The possibility of using the DRIE technology platform developed at Dimes T.C. for the design of high performance mm-wave system has been experimentally demonstrated. A number of waveguide components for the realization of passive beam forming networks for high gain antennas have been designed and characterized. Finally, the waveguide antenna of a 94 GHz FMCW imaging radar sensor was successfully assembled and tested at system level in continuos wave mode.

Using silicon SIWs, high-performance mm-wave systems featuring multiple antennas and/or smart antenna operations can be manufactured with high reproducibility and cost competitive level.

Appendix A

Transmission line modeling

The voltage V and current I distributions on a generic lossless two-conductor transmission line can be found by solving the telegrapher equation [90]:

$$V(z) = Ae^{-j\beta z} + Be^{+j\beta z} \tag{A.1}$$

$$I(z) = \frac{A}{Z_i}e^{-j\beta z} - \frac{B}{Z_i}e^{+j\beta z} \tag{A.2}$$

The intrinsic characteristic impedance Z_i, the propagation constant β and the intrinsic phase velocity v_i are given by, respectively:

$$\beta = k_z = \frac{\omega}{v_i} \tag{A.3}$$

$$v_i = \frac{1}{\sqrt{L_t C_t}} \tag{A.4}$$

$$Z_i = \sqrt{\frac{L_t}{C_t}} \tag{A.5}$$

where the term "intrinsic" refers to the fact that no loading element (i.e., the varactors diodes) has been introduced yet.

A transmission line can be modeled as a cascade of sections with infinitesimal length, each containing a series inductance L_t and a parallel capacitance C_t per unit length (see Fig. A.1a). In terms of lumped components, if the length ℓ of the section is finite but much smaller than the

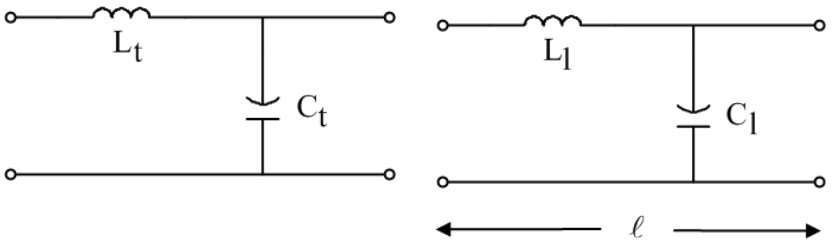


Figure A.1: A section of a lossless transmission line: (a) infinitesimal length and (b) finite but small compared to the wavelength length.

guided wavelength ($\ell \ll \lambda_g$), an inductance L_l and a capacitance C_l can be used (see Fig. A.1b). The constitutive relations become:

$$v_i = \frac{1}{\sqrt{\frac{L_l C_l}{\ell^2}}} \tag{A.6}$$

$$Z_i = \sqrt{\frac{L_l}{C_l}} \tag{A.7}$$

Note that L_t and C_t are per unit length (i.e., distributed elements) since they refer to a section of infinitesimal length, while L_l and C_l are not, since they refer to a section of small but finite length (i.e., lumped components).

The phase shift ϕ_l experienced by a wave travelling along n sections ℓ of the line is simply given by:

$$\phi_l = n\beta\ell \tag{A.8}$$

where β is the phase constant of the line.

Appendix B

Diode parallel model

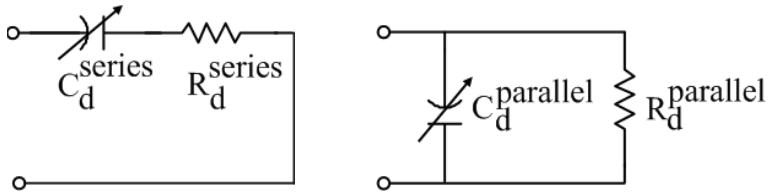


Figure B.1: Simple varactor diode: (a) series and (b) parallel model.

A varactor diode can be modeled as a variable capacitance and a series resistance which accounts for the losses, as shown in Fig. B.1a. The impedance Z_d^{series} at the terminals can be expressed as a function of the diode Q-factor Q_d:

$$Z_d^{series} = R_d^{series} + \frac{1}{j\omega C_d^{series}} = \frac{1}{j\omega C_d^{series}}(1 + j\frac{1}{Q_d}) \tag{B.1}$$

where:

$$Q_d = \frac{1}{\omega R_d^{series} C_d^{series}} \tag{B.2}$$

A parallel model is also possible, where the diode conductance is in parallel with a susceptance (see Fig. B.1b). The admittance $Y_d^{parallel}$ is given by:

$$Y_d^{parallel} = G_d^{parallel} + j\omega C_d^{parallel} \tag{B.3}$$

where:

$$G_d^{parallel} = \frac{1}{R_d} \frac{1}{1 + Q_d^2} \tag{B.4}$$

$$C_d^{parallel} = \frac{C_d}{1 + \frac{1}{Q_d^2}} \tag{B.5}$$

Appendix C

L_1-L_2 de-embedding algorithm

Consider the system in Fig. C.1, where two back-to-back transitions are connected to a section of waveguide. The transitions are assumed to be identical (same S-parameter matrix) and all the component reciprocal; the total system is therefore also symmetric and reciprocal. The S-parameters measured at the terminals of the system can be expressed as:

$$S_{11}^M = S_{22}^M = S_{11} + \frac{S_{21}^2 S_{22} e^{-\gamma l}}{e^{+\gamma l} - S_{22}^2 e^{-\gamma l}} = S_{11} + S_{22} S_{21}^M e^{-\gamma l} \tag{C.1}$$

$$S_{21}^M = S_{12}^M = \frac{S_{21}^2}{e^{+\gamma l} - S_{22}^2 e^{-\gamma l}} \tag{C.2}$$

where γ=α+jβ and the superscript "'M"' stands for "'measured"'. Note that S_{ij}^M and S_{ij} are the S-parameters of the total system and of the transition, respectively.

Eq. C.1 and C.2 form a system of four complex unknowns (S_{11}, S_{21}, S_{22}, and γ) in two equations. Measuring the S-parameters of the total system for two waveguide lengths L_1 and L_2, the following system of four equations in four unknowns can be written:

$$S_{11}^{M_1} = S_{11} + S_{22} S_{21}^{M1} e^{-\gamma l_1} \tag{C.3}$$

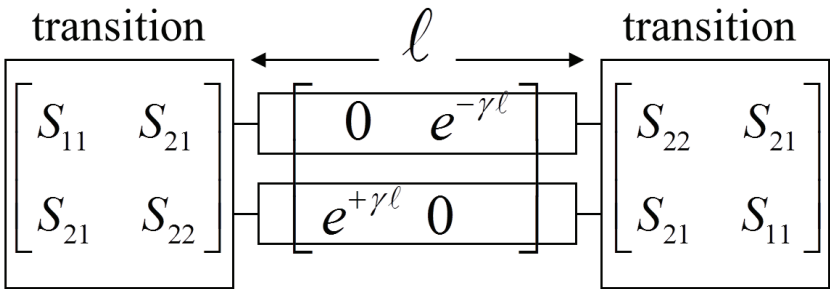


Figure C.1: Schematic representation in terms of S-parameters of a waveguide connected with two identical transitions.

$$S_{11}^{M_2} = S_{11} + S_{22}S_{21}^{M2}e^{-\gamma l_2} \tag{C.4}$$

$$S_{21}^{M_1} = \frac{S_{21}^2}{e^{+\gamma l_1} - S_{22}^2 e^{-\gamma l_1}} \tag{C.5}$$

$$S_{21}^{M_2} = \frac{S_{21}^2}{e^{+\gamma l_2} - S_{22}^2 e^{-\gamma l_2}} \tag{C.6}$$

where $S_{ij}^{M_k}$ are the S-parameter of the k-th measurement. To solve the system, compare eq. C.3 and C.4 for S_{22}:

$$\frac{S_{11}^{M_1} - S_{11}}{S_{21}^{M_1}e^{-\gamma l_1}} = \frac{S_{11}^{M_2} - S_{11}}{S_{21}^{M_2}e^{-\gamma l_2}} \tag{C.7}$$

subtract eq. C.3 and C.4 for S_{22}:

$$S_{11}^{M_1} - S_{11}^{M_2} = S_{22}(S_{21}^{M_1}e^{-\gamma l_1} - S_{21}^{M_2}e^{-\gamma l_2}) \tag{C.8}$$

and take the ratio of eq. C.5 and C.6:

$$\frac{S_{21}^{M_1}}{S_{21}^{M_2}} = \frac{e^{+\gamma l_2} - S_{22}^2 e^{-\gamma l_2}}{e^{+\gamma l_1} - S_{22}^{M_1} e^{-\gamma l_1}} \tag{C.9}$$

The system can now be rewritten as:

$$S_{11},\, \gamma: \qquad \frac{S_{11}^{M_1} - S_{11}}{S_{21}^{M_1}e^{-\gamma l_1}} = \frac{S_{11}^{M_2} - S_{11}}{S_{21}^{M_2}e^{-\gamma l_2}} \tag{C.10}$$

$$S_{22},\ \gamma: \qquad S_{11}^{M_1} - S_{11}^{M_2} = S_{22}(S_{21}^{M_1} e^{-\gamma l_1} - S_{21}^{M_2} e^{-\gamma l_2}) \tag{C.11}$$

$$S_{22},\ \gamma: \qquad \frac{S_{21}^{M_1}}{S_{21}^{M_2}} = \frac{e^{+\gamma l_2} - S_{22}^2 e^{-\gamma l_2}}{e^{+\gamma l_1} - S_{22}^{M_1} e^{-\gamma l_1}} \tag{C.12}$$

$$S_{21},\ S_{22}: \quad S_{21}^{M_1} = \frac{S_{21}^2}{e^{+\gamma l_1} - S_{22}^2 e^{-\gamma l_1}} \tag{C.13}$$

where on the left side the unknowns for each equation are reported. Eq. C.11 and C.12 contains the same unknowns, but with a different exponent of S_{22}:

$$S_{22}^2 = \frac{S_{21}^{M_2} e^{+\gamma l_2} - S_{21}^{M_1} e^{+\gamma l_1}}{S_{21}^{M_2} e^{-\gamma l_2} - S_{21}^{M_1} e^{-\gamma l_1}} \tag{C.14}$$

$$S_{22} = \frac{S_{11}^{M_2} - S_{11}^{M_1}}{S_{21}^{M_2} e^{-\gamma l_2} - S_{21}^{M_1} e^{-\gamma l_1}} \tag{C.15}$$

Taking the ratio of eq. C.14 and C.15 and comparing with eq. C.11:

$$\begin{aligned} e^{+\gamma(l_2-l_1)} + e^{-\gamma(l_2-l_1)} &= 2cos[\gamma(l_2-l_1)] = \\ &= \frac{(S_{21}^{M_1})^2 + (S_{21}^{M_2})^2 - (S_{11}^{M_2} - S_{11}^{M_1})^2}{S_{21}^{M_1} S_{21}^{M_2}} \end{aligned} \tag{C.16}$$

the following system is obtained:

$$\gamma = \frac{1}{l_2 - l_1} arccos[\frac{(S_{21}^{M_1})^2 + (S_{21}^{M_2})^2 - (S_{11}^{M_2} - S_{11}^{M_1})^2}{2 S_{21}^{M_1} S_{21}^{M_2}}] \tag{C.17}$$

$$S_{11} = \frac{S_{11}^{M_1} S_{21}^{M_2} e^{-\gamma l_2} - S_{11}^{M_2} S_{21}^{M_1} e^{-\gamma l_1}}{S_{21}^{M_2} e^{-\gamma l_2} - S_{21}^{M_1} e^{-\gamma l_1}} \tag{C.18}$$

$$S_{22} = \frac{S_{11}^{M_2} - S_{11}^{M_1}}{S_{21}^{M_2} e^{-\gamma l_2} - S_{21}^{M_1} e^{-\gamma l_1}} \tag{C.19}$$

$$S_{21}^2 = \frac{2 S_{21}^{M_1} S_{21}^{M_2} sin[\gamma(l_2 - l_1)]}{S_{21}^{M_2} e^{-\gamma l_2} - S_{21}^{M_1} e^{-\gamma l_1}} \tag{C.20}$$

The system can now be solved in a straightforward way.

Appendix D

Frequency scanning array with alternate slots

Fig. D.1 reports the Brillouin diagram of a waveguide array excited by a TE_{10} mode where the slot are in alternate positions with respect to the waveguide center plane, as illustrated in Fig. 5.1b. The phase constant of the travelling wave is given by:

$$\beta_n = \beta_0 - \frac{2\pi}{d}m - \frac{\pi}{d} \qquad m = .., -1, 0, +1, .. \tag{D.1}$$

where the factor π/d takes into account the alternating of the slots that adds an extra 180° to their electrical distance. This means that two consecutive slots physically spaced of $\lambda/2$ are electrically spaced of λ. The condition for having only one main lobe in the radiation pattern can be derived from eq. 5.9, using for β_m the expression given by eq. D.1.

The array factor $f(\theta)$ is still given by eq. 5.10, where the extra 180° shift is taken into account in Y:

$$Y = -\beta d + kdsin\theta - \pi \tag{D.2}$$

Using eq. D.1, an explicit expression for Y is obtained:

$$Y = (2m-1)\pi\frac{f}{f_c}\frac{p_c}{p}(psin\theta - 1) \tag{D.3}$$

The slot spacing d can be found considering again eq. 5.10, which has a maximum at $Y = -2m\pi$, and equating it to eq. D.2 for $\theta = 0°$ and $f = f_c$,

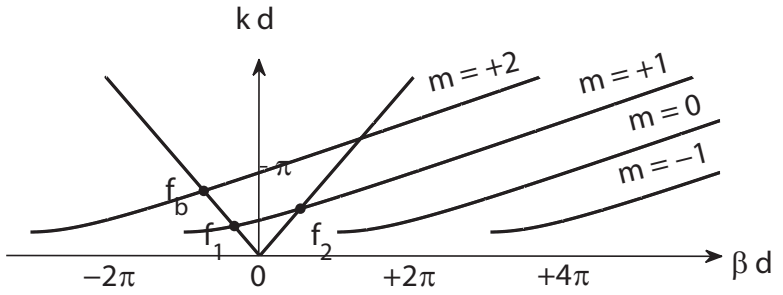


Figure D.1: Brillouin diagram of a waveguide array with $f_b < f_2$ and alternate slots; only the TE_{10} mode is considered.

gives:

$$d = (m - \frac{1}{2})\lambda_{gc} \tag{D.4}$$

This expression simply states that the slot period needs to be reduced of a factor $\lambda_{gc}/2$ (i.e., 180°) with respect to the non-alternate case, since an extra 180° is achieved by alternating the slots.

Substituting the expression of d into eq. 5.9, the condition for having only one main beam becomes:

$$\frac{d}{a} < \sqrt{\epsilon_r - (2m)^2} \tag{D.5}$$

where the quantity under square root has to be positive:

$$m < \frac{\sqrt{\epsilon_r}}{2} \tag{D.6}$$

For a given material, this expression can be satisfied by none, one or more values of m. Using eq. D.4 into eq. 5.14, an upper limit for the cut-off frequency is found:

$$f_{co} < \frac{f_c}{\sqrt{1 + \frac{(2m-1)^2}{\epsilon_r - (2m)^2}}} \tag{D.7}$$

Again, eq. D.6 indicates which modes can be used, and eq. D.7 sets a limit to the waveguide cut-off frequency, once the substrate material of the array is fixed.

Proceeding in a way similar to the non-alternate array, the lower and higher frequencies f_1 and f_2 are found as:

$$f_1 = \frac{-\left(\frac{f_c}{p_c} - \frac{c}{2d}\right) + \sqrt{\epsilon_r(\epsilon_r - 1)f_{co}^2 + \epsilon_r\left(\frac{f_c}{p_c} - \frac{c}{2d}\right)^2}}{\epsilon_r - 1} \tag{D.8}$$

$$f_2 = \frac{+\left(\frac{f_c}{p_c} - \frac{c}{2d}\right) + \sqrt{\epsilon_r(\epsilon_r - 1)f_{co}^2 + \epsilon_r\left(\frac{f_c}{p_c} - \frac{c}{2d}\right)^2}}{\epsilon_r - 1} \tag{D.9}$$

where the factor $c/2d$ takes into account the alternating of the slots. Therefore, the frequency range Δf needed for a 180° scanning of the radiated beam is given by:

$$\Delta f = f_2 - f_1 = \frac{2}{\epsilon_r - 1}\left(\frac{f_c}{p_c} - \frac{c}{2d}\right) \tag{D.10}$$

which is smaller than the non-alternate case due to the factor c/2d.

The design procedure of a travelling wave slotted waveguide frequency scanning array with alternate slots follows what outlined in section 5.2.5, once the expressions for alternate slots are considered.

Appendix E

Dolph-Tschebyscheff array slot dimensions

The Dolph-Tschebyscheff array was designed fixing the slot width to 10 μm, the slot period to 1613 μu, while the slot offset and length were tailored as in Table E.1 for the targeted radiation efficiencies and resonance frequency of Fig. 5.12a.

A metal thickness of 5 μm was assumed in simulation.

Table E.1: Slot dimensions of the Dolph-Tschebyscheff array of chapter 5.

Slot number	power coeff.	offset μm	length μm
1	0.1182	2	597
2	0.1660	3	598
3	0.2641	4	599
4	0.3817	6	598
5	0.5121	7	599
6	0.6461	8	600
7	0.7727	11	601
8	0.8803	14	603
9	0.9587	19	603
10	1.0000	26	605
11	1.0000	30	607
12	0.9587	33	608
13	0.8803	30	607
14	0.7727	25	605
15	0.6461	17	604
16	0.5121	12	602
17	0.3817	8	600
18	0.2641	3	598
19	0.1660	2	597
20	0.1182	2	597

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Summary

Mm-wave passive components for integrated phased array antennas

Sensor devices are pervading everyday life in order to increase our ability of understanding or being aware of something.

Sensors are defined by the object or element they are able to sense (distance, pressure, temperature, etc.) and the physical mechanism they employ (mechanical, electrical, optical, etc.). Electromagnetic sensors provide the unique ability of penetrating objects which are opaque to light (clothes, walls, rain, etc.) by collecting the energy transmitted by electromagnetic waves.

They have been traditionally employed only in specialized fields such as in military radars and spectroscopy due to their costs and complexity, but are recently gathering more interest in commercial applications, since they can take advantage of the acquired maturity of silicon technology above 30 GHz, capable of integrating several functionalities on chip for a small price. Commercial examples of such sensors include imaging radars for assisted driving systems, body scanners, and distance sensors for hostile environments (fog, dust, chemical vapors).

The research presented in this thesis is focused on the development of a new IC compatible technology platform, based on silicon integrated waveguides, for the realization of high performance passive components in the whole millimeter wave frequency bandwidth such as IC broadband interfaces, low loss interconnections and high gain antennas in the whole millimeter-wave frequency range.

Chapter 2 faces the design of analog electronically tunable phase shifters working at 50 GHz using a coplanar waveguide as transmission line for the smart antenna concept of Fig. 1.6. The controllable phase delay is achieved by periodically loading the line with reverse biased silicon-on-glass Schottky diodes, whose dc control voltage modifies the line unit length capacitance and hence phase constant and delay. At 20 GHz the phase

shifter exhibit insertion losses between 0.021 and 0.037 dB/° for the different biasing conditions, or equivalently a difference of 3 dB between maximum and minimum insertion loss (i.e., 6.7 and 3.8 dB, respectively) for a 180° total phase shift. Fixing the operating frequency to 50 GHz, instead, the structure achieves a total total phase shift of 244° by sweeping the diode voltage from -15 V to -1 V with a maximum insertion loss of 17 dB, which mostly arises when the diodes are biased close to the forward region.

Chapter 3 introduces a novel manufacturing technology based on IC-compatible steps enabling the realization of silicon-filled integrated waveguide interconnections with continuous metallic side walls. Using high resistivity silicon substrates and continuous metallic side walls, integrated waveguides can be manufactured with a low cost process and without the need of any mechanical assembly operation. Two different etching mechanisms were reported, namely KOH and DRIE, and the performances of the resulting structures were compared in terms of their propagating modes and insertion losses. Experimentally, losses of 0.2 dB/mm for a KOH waveguide and 0.1 dB/mm for a DRIE waveguide at 100 GHz were measured. For practical reasons (i.e., measurement setup available in the university lab), operating bandwidths around 50 and 94 GHz were targeted. The frequency scalability of the technology is experimentally demonstrated up to 130 GHz, while no measurements could be carried out in the deep mm-wave range due to the lack of hardware instrumentation.

Chapter 4 presents a planar transition based on a U-shaped resonant slot for interfacing SIWs to planar circuits in CPWs. The ultra-wide impedance matching bandwidth achieved by the transition is explained by means of the slot dipole antenna Q-factor; while the coupling from CPW to SIW mode was illustrated in terms of field distribution. A parametric analysis of the effect of the slot geometrical dimensions on the input impedance of the transition was carried out and discussed. Simple empirical design equations are presented and validated on a transition realized in a silicon integrated waveguide technology. When compared to KOH waveguides, DRIE structures do not suffer from under-etching at convex corners, which translates in a superior control of the geometrical dimension and therefore a better impedance matching of the transition, whose measured $|S_{11}|$ is below -14.5 dB in the entire frequency range 79-110 GHz.

Chapter 5 explores the realization of high gain smart antennas. A travelling wave slotted waveguide frequency scanning array topology is analyzed by means of the Floquet theorem and the (periodic) Brillouin diagram, which allow to extract sufficient design conditions to enforce only one spatial harmonic inside the (radiating) fast wave region of the array. Employing two novel technologies developed at Dimes and MiPlaza labs, travelling wave

arrays based on a slotted waveguide topologies were designed, integrated and characterized. A parametric study of the power radiated by each slot was performed, and the results were used for the implementation of a power distribution according to the Dolph-Tschebyscheff coefficients, which minimizes all the secondary lobes in the far field pattern. Design equations for frequency scanning arrays in waveguide were obtained, and a general design procedure was introduced to facilitate the choice of the waveguide cut-off and dielectric material once the operating frequency has been fixed. Measureement results of uniform and Dolph-Tschebyscheff arrays using KOH and DRIE waveguides were presented, showing good performances of the designed structures in terms of scanning angle, beam width and side lobe levels. In particular, the DRIE technology allows the patterning of metal structures with an accuracy around 0.5 μm and a minimum gap width of 10 μm, one order of magnitude better than what offered by a PCB process. As the higher accuracy enables a finer tapering of the power radiated by each antenna, DRIE arrays can be designed with a larger number of elements (20) than PCB arrays (typically less than ten), which reflects in smaller beam widths (8.5°) and better side lobe levels (-23 dB).

Finally, chapter 6 illustrates the potentialities of the proposed silicon SIW technology for the implementation of high performance highly co-integrated mm-wave systems. As demonstrator, a complete frequency-modulated continuous-wave 94 GHz radar sensor on silicon for 3D imaging is presented. The high gain antenna is implemented with a linear array of frequency scanning arrays (see Fig. 1.6b), interfaced to the active chips by means of flip-chip assembly and CPW-to-SIW transitions. In addition to this, key components as high-frequency electrically tunable distributed phase shifters and waveguide power splitters for the BFNs of high gain antennas are presented.

As conclusion, the experimental results provided throughout this thesis work indicates that the proposed silicon substrate integrated waveguide technology, based on DRIE etching and photo-lithographic metal patterning, is a good candidate for the realization of high performance mm-wave systems featuring multiple antennas and/or electronic beam steering with high reproducibility, cost competitive level, and frequency scalability in the whole millimeter wave range.

List of publications

Journal Papers

Vladimir Jovanovic; **Gennaro Gentile**; Ronald Dekker; Pascal de Graaf; Leo C. N. de Vreede; Lis K. Nanver; Marco Spirito, "Silicon-Based Technology for Integrated Waveguides and mm-Wave Systems," *Electron Devices, IEEE Transactions on*, vol. 62, no. 10, pp. 3153-3159, Oct. 2015.

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G. Gentile, K. Buisman, A. Aknoukh, L. N. C. de Vreede, and B. Rejaei, "50 GHz integrated silicon-on-glass Schottky diode tunable phase shifters", *Proceedings of the 10th ProRISK Workshop of the STW.ICT Conference 2007*, Veldhoven, The Netherlands.

Acknowledgments

And finally this page of the thesis, of my career, and of my life has arrived. While the last simulation, yes really the last is running, with everything ready to be updated and sent to printing, my thoughts are kind of blurred, while attempting to go back in time to write this page.

A page of my life is going to be closed soon, not after having been printed and hopefully successfully defended. Much time has passed from that 5th of March 2006 when I arrived at 23.00 to Delft station, half an hour earlier my appointment, didn't expect the train from Schiphol to be on time. It was snowing, lot of bikes, no one at the station, no smart phone, just waiting for a friend. An trilled by a new adventure, a new chapter, a new start, the first real start far from my home town and my family. Much water has passed since that day, and since that 15th of October 2006, when I officially started my phd and signed the contract. The memories are still clear impressed in my mind, but this is probably not the best place to narrate them.

It is instead time to give credit to all the people that have made this moment possible. Well, so much time has passed that the number of people has probably grown exponentially and would double the size of my thesis. Of course I could write the classical acknowledgment, where a long list of people is presented, starting from the supervisorS, with a big plural S for me, and the promoterS, with another capital S, and continuing with all the staff at the university, all the colleagues, the friends, inside and outside the TU, the volleyball, the Roze Blok, the Kratos, my housemates, my friends in my home town and my family. I could do that, but it would feel like compiling a shopping list for the supermarket, where you always try to write all in order not to forget anything.

I think people that are or have been important know that, without the need to see their name printed here. Instead, I would like to say a big and honest thank to all those people that added something to my life and to my personality, a nice moment, a skill, a knowledge, a defect, a smile or an

extra motivation for a deadline. It is sad to see that people that have been so close to you in a part of your life, then drift so far away. It is sad to see how we often miss the people we do not see, and we are bored from the ones we are with.

The last simulation has terminated, time to export the result and make the last figure. Ahi Delft, it has been a definite pleasure to meet you, it has been an adventurous journey, probably my first real ever, with lot of obstacles and a very unexpected end. Nevertheless, as Marcel Proust liked to say: "The real voyage of discovery consists, not in seeking new landscapes, but in having new eyes."

Good luck for the defence, Gennaro!

Curriculum Vitae

Gennaro Gentile was born in Naples, Italy, in 1983. He received the B.Sc. (cum laude) and M.Sc. degrees (cum laude) in electrical engineering from the University of Naples Federico II, Naples, Italy, in 2004 and 2006, respectively. He performed his M.Sc. thesis research at the Delft Institute of Microsystems and Nanoelectronics (DIMES), Delft University of Technology, the Netherlands, as part of the Erasmus international exchange program.

In October 2006 he commenced his Ph.D. work in Microelectronics at the same institute. The focus of his research consisted in the realization of passive components for integrated radar sensor at millimeter waves. From 2008 to 2012, he worked on the project "Merging Electronics and Micro & Nano-Photonics in Integrated Systems (MEMPHIS)", where he was involved in the development of a technology platform for the integration of mm-wave systems using metallic waveguides.

From September 2012 to August 2013 he worked on near-field characterization of antennas for novel communication links at the European Association of the National Metrology Institutes (EURAMET).

In September 2014, he joined Salusion B.V., a start-up company located in the YES!Delft incubator and active in the healthcare sector, where he was responsible for the optimization of RFID urine sensor for elder and handicapped people wearing incontinence material.

In July 2014 he joined NXP Semiconductors Germany, automotive department, where he is currently working on the realization of radar sensor in CMOS technology for advanced driver assistance systems (ADAS) and self-driving cars. His current interests include the optimization of RFID antennas in flexible electronics and the industrialization of integrated circuits for the commercial market.

Mr. Gentile was the recipient of the 2010 Best poster award at ProRISC workshop in Veldhoven, The Netherlands, the 2012 Student Grant from the IEEE European Microwave Association, the 2012 Gallium Arsenide (GAAS)

Association Student Fellowship, and the 2012 Research Excellence Grant from the EURAMET.