Design and Decentralized Control of Bi-directional Flyback

By

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1. Introduction

1.1. Motivation:

Access to electrical energy for all is very critical for reducing global poverty and for the sustainable development. Sustainable energy is the seventh goal of the 17th UN Sustainable Development Goals (SDGs), with a call to "ensure access to affordable, reliable, sustainable and modern energy for all."[1]. Target for sustainable development Goal 7 include universal access to energy services, increase renewable energy share in global energy mix, double the global rate of improvement in energy efficiency, facilitate clean energy research and the technology development by increasing international cooperation and upgrade infrastructure to ensure sustainable energy services for all in developing countries especially least developed countries. According to the state of electricity access report 2017 [1], about 15 percent (1.06 billion) of the global population still living without the access of electricity and a larger number of the population about 3.04 billion still relied on solid fuels and kerosene. While it is important to increase the penetration of electricity, it is more important to ensure that an increasing share of electricity come from renewable sources such as solar and wind to meet the sustainable development goal. Most of the population who does not have access to electricity are concentrated in Sub-Saharan Africa, South Asia, East Asia, and North Africa especially in rural and remote areas. Figure 1 shows the country wise energy access deficit. Countries are shown in the figure account for eighty percent of the population who don't have access to electricity. Most of these countries are potentially rich in solar energy as can be seen in Figure 2. Therefore, producing solar energy locally to meet the demand is a good idea.

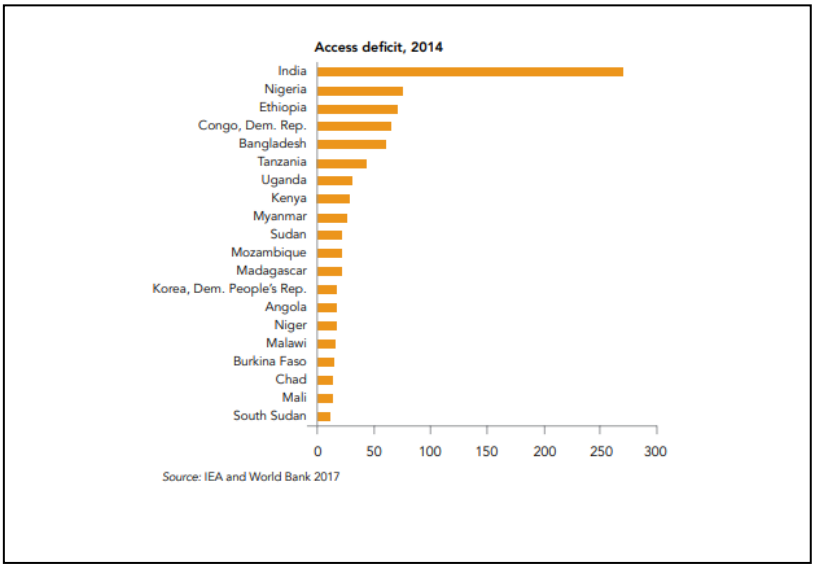


Figure 1: Electricity Access Deficit, 2014 [1]

As it is expensive and difficult, due to geographical conditions, to build new grid infrastructure to reduce the electricity access deficient, isolated microgrids (MGs) have been considered as a solution. Furthermore, most of the countries which are high electricity deficient as depicted in Figure 1 have good availability of the sun throughout the year. Therefore, solar based MGs have been proposed and designed to meet the electricity demand. Decreasing cost of PV panels, increasing global attention on renewable sources, low carbon emission, development in power electronics technology and the advancement in the storages technology are some other prominent reasons which are propelling the research in off-grid DC MG based on the solar as an energy source.

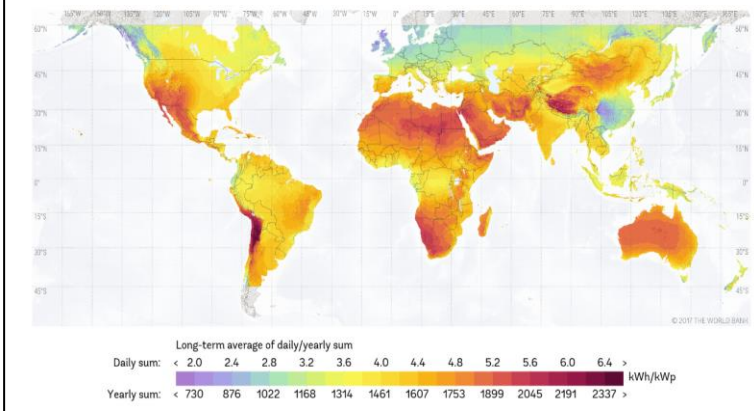


Figure 2: Solar Irradiance [2]

Solar Home system (SHS) has gained a lot of attention in the last few years and have been successfully deployed in many remote locations to provide the electricity to a household. However, due to the intermittent nature of solar power, these systems require a large storage system which makes these systems costly and not utilized to their full capacity. Interconnecting SHS has been proposed to form a voltage distribution network. Interconnecting SHS results in smaller SHS storage, high modularity, and better performance.

The backbone of the interconnected MG is power electronic converters. A solar home unit requires multiple converters based on its design. There are many aspects which needed to be considered while designing of these converters such as cost, switching between different modes depending on generation and consumption, power flow in a single SHS, power flow among SHSs, optimal use of PV, degradation of battery with time, high modularity, voltage regulation and load sharing between different PV units and storages units.

The considered SHS architecture for this thesis is shown in Figure 3. Overview of the SHS is being presented in section 1.1. This work proposed the design of flow converter and the selection of appropriate control strategy to ensure proper function of the interconnected solar home system.

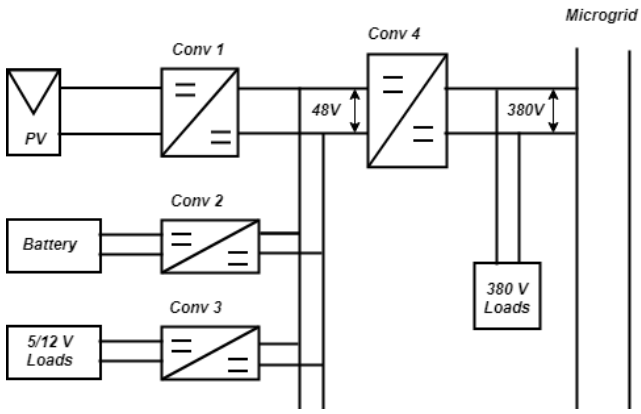


Figure 3: Architecture: Interconnecting SHS with modular growth for the sub-system

1.2. Overview:

Figure 3 shows the architecture of interconnecting SHS. The MG consists of several SHSs interconnected at High Voltage Bus (HVB). Each SHS includes 4 DC-DC converters: PV modules, battery, 5/12V loads and 380V loads. The four converters enable the power management of the SHS. A short description of all the components in the SHS is presented here.

1. Conv1: This is a unidirectional PV converter that also enables MPPT tracking. This converter will be referred to as solar Converter.

2. Conv2: This is a bidirectional battery converter that regulates the battery charging and discharging. This converter is called charge converter.

3. Conv3: This is a unidirectional load converter supporting two different voltage levels. This converter always works in VCM mode as the voltage at the output of this converter should be constant (5V or 12V).

4. Conv4: This is a bi-directional converter that serves as a link between SHS and the MG, and it is responsible for controlling the power flow in both directions. This converter will be referred to as flow converter.

5. 380V Loads: These loads are present at the output of converter 4 and the high voltage bus. High voltage bus is shared for each solar home system. Therefore, these loads are seen by all SHSs.

6. PV Modules: PV modules are used to generate the solar power. Solar converter enables the Maximum Power tracking of these modules.

7. Battery: Battery is used to store the energy when excess power is available and to provide the power when demand exceeds the PV generation.

8. 5/12 Loads: Future low voltage DC loads, e.g. Laptop, mobile, LED lighting, etc.

An overview of top-level specs for the converters is shown in Table I.

Table I: An overview of top-level specs for the converters.

S. No.	Parameter	Conv 1	Conv 2	Conv 3	Conv 4
1	Vin (V)	17	12	48	48
2	Vout (V)	48	48	48	380
3	Power (W)	200	100	100	300
4	Direction	Uni	Bi	Uni	Bi
5	Additional	MPPT	Overcharged protection	-	Isolation

1.3. Research Objective:

To design and build a bidirectional flyback converter that can enable decentralized power-sharing among interconnected solar home systems (SHSs)

Research Questions:

1. What is the most suitable converter topology for the flow converter and the charge converter in interconnecting SHS? (Ch2)
2. How to optimize the bidirectional flyback converter design for soft-switching enabling power-flow in both directions? (Ch3)
3. How to implement current control for complete power range in both direction? (Ch 4)
4. How to achieve decentralized control at the system level for the selected converter topology? (Ch 5)
    (a) How to implement the control for flow converter to enable the load sharing among SHSs?
    (b) How to implement coordinated control to fully utilize available PV power?

1.4. Contribution:

1. Hardware design of di-directional flyback flow converter.
2. Implementation of current control for flow converter and battery converter.
3. Implementation of input droop and output droop for flow converter.
4. Demonstration:
    (a) load sharing between two flow converters using the droop control.
    (b) voltage regulation at low voltage bus and high voltage bus.

2. Literature Review & Theory

2.1. Design Requirements of Flow Converter:

The major design requirements for the flow converter have been formulated here. These requirements form the selection criteria for converter topology and control methodology. In chapter 3 & 4, some additional requirements are added to this list.

1. The converter should be able to transfer 300W power from the low voltage side to high voltage side. The maximum power from the high voltage side to low voltage side is 200W.
2. Nominal voltage for the low voltage side is 48V, and for high voltage side is 380V. The converter should support power flow in both directions around the nominal voltages.
3. The converter should be able to work autonomously during all the MGs state without any communication requirement.
4. The control should enable load sharing and voltage regulation on high voltage bus (HVB) and low voltage bus (LVB).
5. The converter should be able to transfer power efficiently in both directions. To reduce the losses, the soft switching must be implemented.
6. The converter should be able to change the direction of power flow based on the operating state of the MG.
7. Galvanic Isolation: Isolation is a requirement for this converter as the converter is connected to HV side. Moreover, as the voltage step ratio (when transferring power from 48V to 380V side) is around eight, the transformer is required to match the voltage.
8. Operating frequency of the converter should be high enough to reduce the size of the converter. However maximum frequency should not cross 125KHz limit as it will increase switching losses and EMI.

2.2. Switching:

Switching plays a significant role in determining the power losses, and hence deciding the efficiency of the converter, especially, at high frequencies. The soft switching has been listed as a requirement in section 2.1. Power switching can be divided into two categories.

2.2.1. Hard Switching:

Hard switching refers to the switching phenomenon when both high voltage and high current is present during the switching period. The overlap area between the drain-source voltage and current in the MOSFET determines the losses [9]. Because during the hard switching both voltage and current are present, the losses are significant.

The switching losses can be decreased by increasing the rate of change of voltage or current or both at the time of switching. However, this would result in high electromagnetic interference (EMI). There are many standards in consumer electronics which restricts the EMI above a certain level.

2.2.2. Soft Switching:

The Soft-switching is commonly used to reduce the losses in the MOSFET. During the switching transition, either voltage or current (or both) is zero that results in zero overlaps between current and voltage waveform. Soft switching also includes switching the MOSFET off at reduced drain-source voltage using the parasitic resonance circuit; this kind of switching is called quasi-resonant switching or valley switching. Soft switching can be divided into three categories based on the voltage and current at the time of switching:

1.) Zero Voltage Switching
2.) Zero Current Switching
3.) Quai Resonant Switching

It is not always possible to turn on and turn off the MOSFET at zero voltage or current due to the practical restrictions in the design. In those cases, quasi-resonant switching is used to reduce the losses and keep EMI in an acceptable range. The switch is turned on when the drain-source voltage reaches to its minimum value [9]. Due to the lower voltage during the turn-on transition, quasi-resonant switching results in lower power losses and reduction in EMI. EMI reduction can be attributed to two reasons. First, because the voltage drops to the minimum before the transition happens, there is less voltage to fall in the same transition time; therefore, lesser dv/dt [9]. Second, the frequency is not constant when valley switching is used. Thus, RF emissions are spread in a frequency band, and that results in lower EMI [9].

2.3. Converter Topology Review for Flow converter:

There are a lot of topologies are available for the isolated bidirectional DC-DC converter (IBDC). In this section, most relevant ones are discussed. The selected topology must fulfill all the requirements listed in section 2.1.

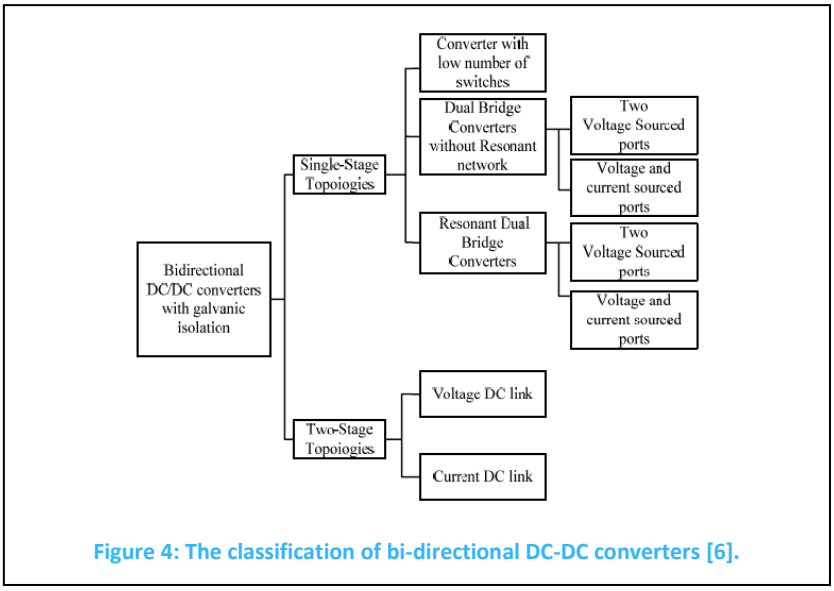


Figure 4: The classification of bi-directional DC-DC converters [6].

The classification of Isolated DC-DC Converter is shown in Figure 4 [6]. As two-stage topologies are more complex and costlier than single-stage topologies, two-stage topologies are omitted from the review. All the single stage bidirectional topologies have a common structure as shown in Figure 5 . First, DC voltage is converted to high-frequency AC; then this AC voltage is stepped up or stepped down using the high-frequency transformer. In the last step, the output voltage of the transformer is converted back to the DC [7]. The high-frequency transformer provides the galvanic isolation and the voltage matching. In this section, three topologies based on this structure is being considered for review.

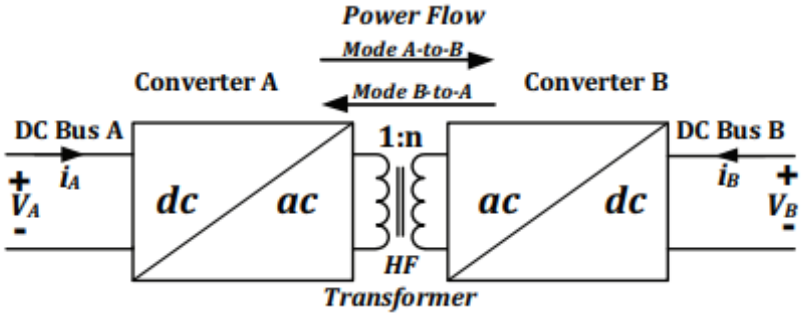


Figure 5: Basic Structure of Isolated Bi-directional DC-DC Converter [7]

2.3.1. Dual Active Bridge (DAB):

In Figure 6, the dual active bridge (DAB) converter is shown. DAB is voltage fed topology from both sides. Main components of the DAB converter are two full bridges, a high-frequency transformer, and two terminal capacitances. Each diagonal pair in a full bridge is turned on for 180-degree phase. For rest of the time, another pair of the full bridge is

turned on. Power flow is determined by controlling the phase difference between the two full bridges. The leakage inductance of the transformer is not shown in Figure 6; However, the leakage inductor appears in the calculation of power. Main advantages of DAB topologies are lower voltage stress across MOSFETs, equal current stress on all the switches, well documented current control method, higher bandwidth, faster response due to lack of passive components, the simple structure of transformer, possible operation at high frequency and implementation of soft switching without extra circuitry [7].

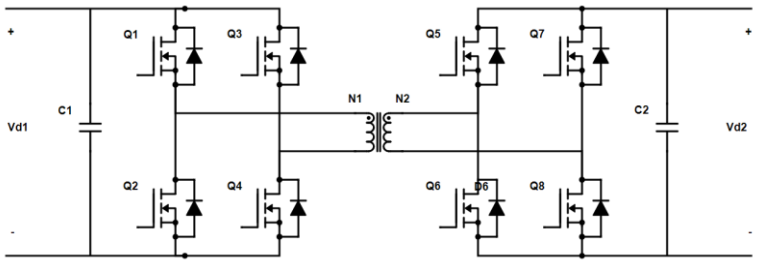


Figure 6: Dual Active Bridge Converter

DAB topology suffers from large component counts. All the eight switches and their gate controllers are always active irrespective of the direction of current flow. That results in high driver losses and complex control circuitry. The requirement of a proper mechanism to avoid DC saturation and highly sensitive phase generator make the control even more complicated. Different modifications of full bridge DC_DC topologies are presented in the literature to overcome the drawback of basic DAB topologies. However, this is not achieved without adding extra complexity to the circuit and increasing the cost. A review of modification of DAB topology has been presented in [6]. DAB with inductor tank, DAB with series resonant tank and DAB with the higher order resonant tank are the most famous adaptation of DAB topology.

2.3.2. Dual Half Bridge:

The second topology dual half bridge is shown in Figure 7. Unlike full bridge topology, half bridge converter has low ripple current. The dual half-bridge consists of voltage fed half bridge at one side and current fed half bridge at another side. Current fed side is generally connected to the storages unit to make charging and discharging current constant. Hence, increasing the lifetime of the battery [7]. Wide soft switching range, same device rating of switches as in DAB for the same power, more straightforward control, and half active component counts are other main advantages of Dual Half bridge scheme [7,8]. As one side is current fed in DHB, it requires a relatively bulky inductor to smooth out the current ripple. Due to this extra magnetic component requirement the size of the converter and the losses increase. However, that is compensated by lower switching losses as only four MOSFETs are used compared to eight in DAB [7].

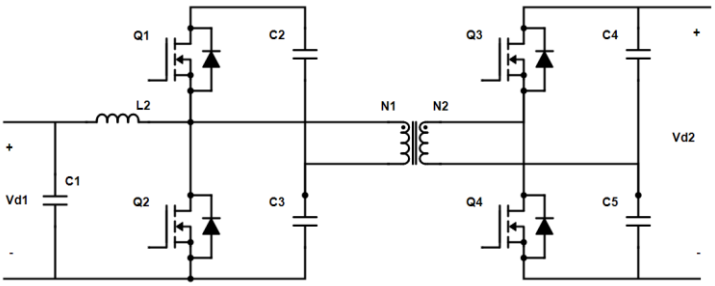


Figure 7: Dual Half Bridge Converter

2.3.3. Bidirectional Flyback:

Flyback has been very popular in low power application. Flyback has been used extensively used in wide range of application such as consumer applications, mobile and laptop chargers, high voltage supply to Cathode Ray Tube (CTR) in TVs and low-cost single and multiple output power supplies. The use of flyback was limited in high power application due to the large ripple especially in DCM and BCM mode and high voltage stress across the MOSFET. Due to the recent advancement in the switching technology, MOSFETs with higher breakdown voltage and low conducting resistance are available. This has enabled the use of flyback in medium power application. Uni-directional flyback can be adapted for bi-directional flow by replacing the passive diode with active MOSFET. Bi-directional flyback is shown in Figure 8. Compare to other bidirectional DC-DC isolated topologies, bidirectional flyback only require two MOSFET, out of which only one is active for power flow in one direction; other MOSFET works as a diode.

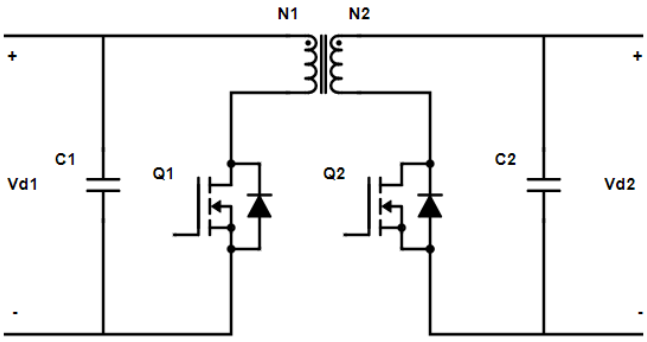


Figure 8: Bi-directional Flyback Converter

Operation of flyback can be divided into three modes: Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM) and Boundary Conduction Mode (BCM). Compare to CCM, BCM and DCM can incorporate the valley switching. In recent time, bidirectional flyback topology has been increasingly used as a charging/discharging interface converter between the DC bus and the battery. Summary of comparison of considered three topologies has been shown in Table II.

Table II: Comparison of isolated bidirectional topologies.

Comparison Criteria's	DAB	Half-bridge	Bidirectional Flyback
No. of Switches	8	4	2
Active switches	8	4	1
No of Switching per cycle	16	8	2
Changing the Direction of power flow	Implemented by the timing control	Implemented by the timing control	Extra Circuitry Needed
The rate of Current Change	High	High	Relatively Medium
Frequency	Fixed	Fixed	Variable

Comparison of dual active bridge, dual half bride and flyback is shown in Table II. Based on the literature review, bi-directional flyback is chosen for flow converter due to the simple design and control.

2.4. Type of Power Converters in DC Microgrid:

In the DC MG, DC sources, battery, load are connected to the MG either directly or by a DC-DC converter. These converters operate in different modes to ensure that MG is functional and reliable. Power Converters can be classified into three categories based on their mode of the operation [3].

2.4.1. Grid Forming Converters:

The grid forming converters are responsible for a generating a desired voltage for the MG. A grid forming converter is an ideal voltage source with zero output impedance. In DC MG, these converters control the voltage of the shared HV bus. If there are more than one converters are connected in parallel, at least one must be operated in grid forming mode.

2.4.2. Grid Feeding Converters:

Grid feeding converters are responsible for providing the required power to the connected system at the given voltage. Grid feeding converters do not regulate the voltage of PCC and operate in current control mode and power control mode. Power references or current references for grid feeding converters are generated based on the control strategy.

2.4.3. Grid Supporting Converters:

In DC MG, grid supporting converters regulate the voltage by injecting the power (or current) based on their droop profile. These converters can work with both VCM and

CCM. For VCM based converters, droop control can be adopted. Power is transferred based on the output voltage.

2.5. MG Coordinated Control:

Different methods to implement the coordinated control for the MG are available. These methods are classified based on the communication infrastructure. These classifications are [4]:

1.) ***Centralized Control:*** Communication is needed. Centralized controller collects all the information from all the distributed generators (DG), energy storages (ES), etc. Based on this information, centralized control takes decisions, and these decisions are communicated back to the local units to perform the regulation. Voltage regulation is very effective because the centralized controller has all the information at the time of decision. The high cost of communication infrastructure and not enough redundancy are significant disadvantages of centralized control. Centralized control also suffers from poor modularity as additional communication infrastructure is needed to add new local unit [4].

2.) ***Decentralized Control:*** Decentralized control is cheaper because high-speed communication and additional infrastructure are not needed. Multiple local controllers are present which sense the local information to perform the control functions. Poor voltage regulation and less control overload sharing are key disadvantages of decentralized control. This kind of control is plug-and-play in nature and highly modular [4].

3.) ***Distributed Control:*** Only low-bandwidth communication is needed. The central controller is absent, and the information is shared between the neighbors. Presence of low-bandwidth communication channel improve the load sharing compare to decentralized control [4].

4.) ***Hybrid Central Control:*** This kind of control is hierarchical. The hierarchical control levels are inspired from AC grid control. The primary control operates on the local level whereas the secondary control is a combination of decentralized control and centralized control which operates on the central level. Tertiary control is optional. Voltage regulation and load sharing are decent because of the availability of a separate communication link between local units and secondary control. Hybrid central control also has low modularity as centralized control [4].

5.) ***Hybridized Distributed Control:*** No communication link is required. Communication is performed using the line/bus only. The high-frequency AC signals are applied to communicate the information. Low cost, high modularity,

and high load sharing are the main advantages of hybrid central control. Voltage regulation is not very precise [4].

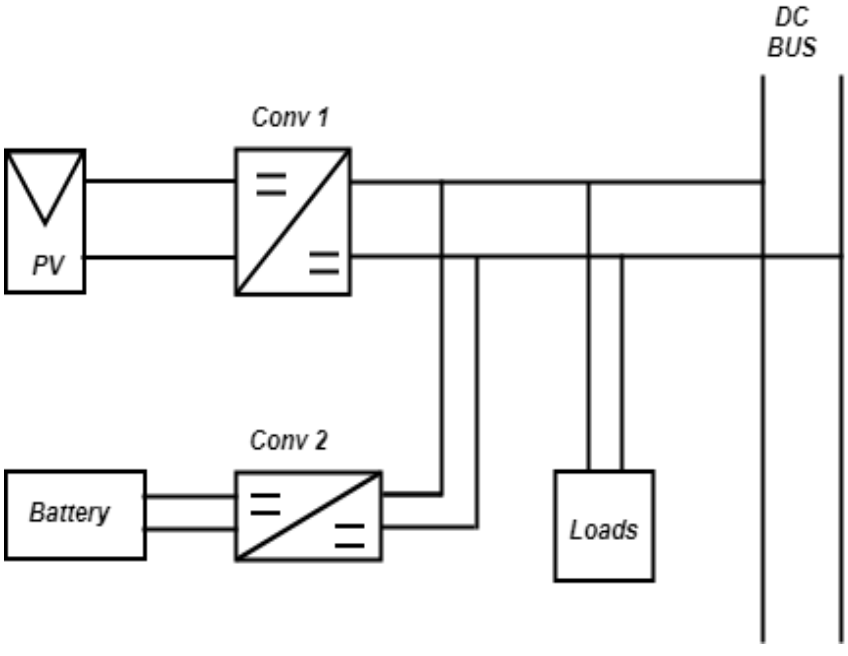
2.6. Decentralized Coordination Control:

Three different methods to implement decentralized control are being reviewed in [4]. Summary of these methods is being presented here.

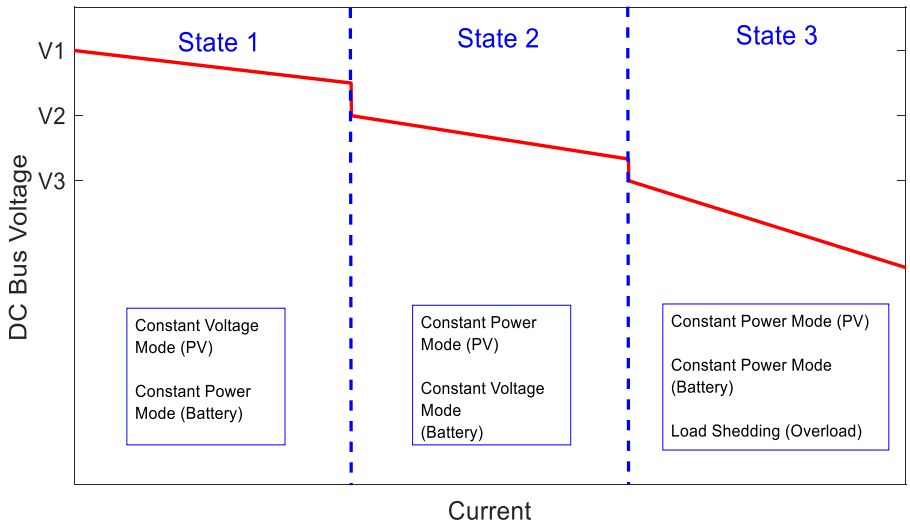
2.6.1. DC Bus Signalling (DBS):

DBS was first proposed in [5]. DBS is a low cost and effective coordination methods to control the MG in a decentralized manner where information is shared using the local bus voltage. Voltage variation is used to determine the role of the converters and their mode of operation. DC converters act as a grid forming, grid feeding and grid supporting based on the voltage at the local bus. Apart from reacting to the local bus voltage, converters can also determine the bus voltage. Droop control is typically used with DBS to ensure load sharing among parallel converters. Using the DBS, different power sources and storages unit can be prioritized to achieve maximum utilization of renewable distributed sources.

In [5], DBS is explained using an example of a two-source system which has been shown in Figure 9 (a). When the output load is low, PV operates in constant voltage mode and take the role of forming the grid. PV charges the battery and provides the power to the load. If the total load becomes more than the maximum power PV can provide, the system enters in the state 2. PV converter switches to constant power mode and battery control switches to constant voltage mode. As load increases, the battery provides additional power until it reaches to the maximum discharging capacity and system enters in state 3. In state 3, load shedding is performed to balance the power demand and generation.



(a)



(b)

Figure 9: (a) Two Source System (b) DBS Control Law

2.6.2. Adaptive adjustment of droop coefficient:

Control using Adaptive adjustment of droop coefficients is an improvement of conventional droop method. The value of droop coefficients is being revised based on the local information. For example, in an MG where multiple batteries are present in parallel, a higher droop coefficient is assigned to the battery with a low state of charge (SOC). Similarly, the lower droop coefficient is allocated to the battery with a high state of charge (SOC) [4]. Adjustment of droop can be linear or can follow some complex rule based on the requirement of the system. In Figure 10, linear and exponential droop adjustments are shown.

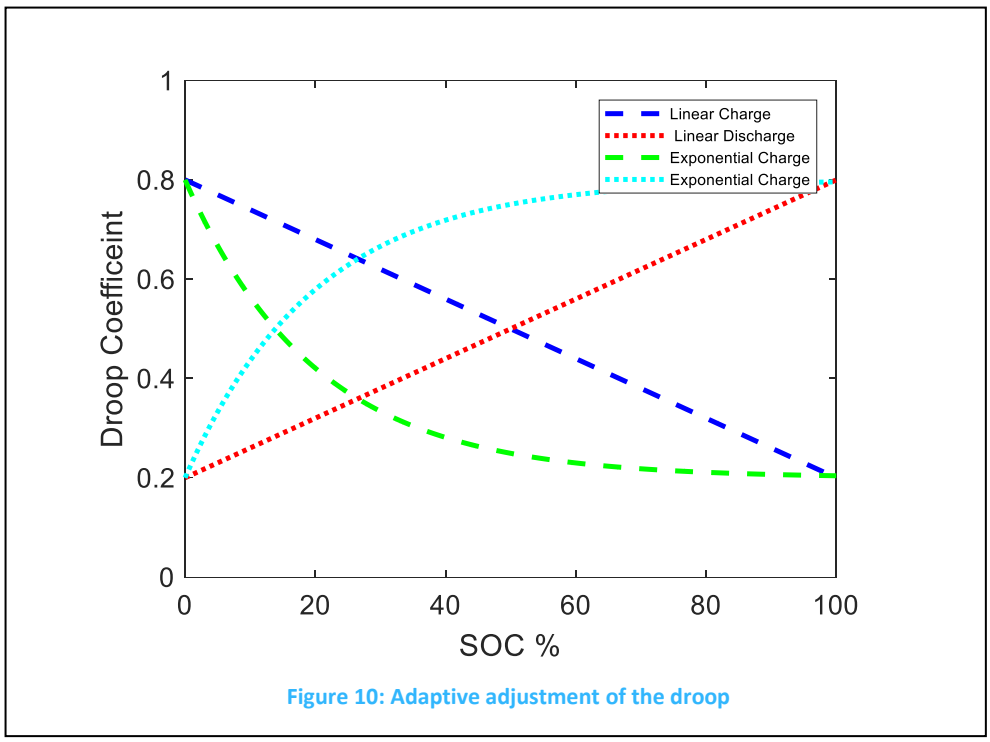


Figure 10: Adaptive adjustment of the droop

2.6.3. Power Line Signalling (PLS):

PLS is another coordination method which does not require a dedicated communication channel. In PLS, information is shared using the power lines as suggested by the name of the scheme. High-frequency signal is injected into the power line to communicate different messages. The major disadvantage of this scheme is that it requires a digital infrastructure to decode and encode the high-frequency signal. Unlike DBS and adaptive adjustment of droop coefficient method, voltage does not change with the output power and the state of MG, PLS control results in better voltage regulation and power quality.

In this project, DBS is selected to implement decentralized control because of its simple implementation and power-sharing capability.

2.7. Flyback with valley switching:

Flyback converters often use valley switching to reduce the EMI and the switch turn-on losses in the MOSFET. There are two kinds of operation possible with valley switching in flyback converters:

1. DCM with valley Switching (DCM-VS)
2. BCM with valley Switching (BCM-VS)

Flyback operation with valley switching can be divided into three periods irrespective of whether flyback is operating in DCM-VS or BCM-VS.

- $T_{ON}\ Period$
- $T_{OFF}\ Period$:
- T_{RES} Period

The switching period of flyback equates to the sum of these three periods.

$$T = T_{ON} + T_{OFF} + T_{RES} \quad (1)$$

The time balance equation can also be written in the form of the duty cycle

$$D_{ON} + D_{OFF} + D_{RES} = 1 \quad (2)$$

With,

- $D_{ON} = \frac{T_{ON}}{T}$, ON time Duty cycle.
- $D_{ON} = \frac{T_{Off}}{T}$, Off time Duty cycle.
- $D_{ON} = \frac{T_{RES}}{T}$, Resonance time Duty cycle.

Figure 11 shows the schematic of unidirectional flyback which is used to explain the theory.

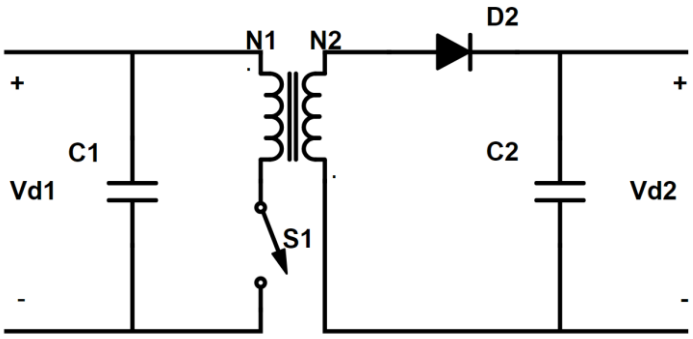


Figure 11: Unidirectional Flyback

T_{ON} Period:

At the start of this period, Switch S1 is turned ON, and input voltage Vd_1 appears across the inductor and current in the inductor starts to increase linearly. The current does not flow at the secondary side as diode D1 is in reversed bias. As the current increases, the energy stored in the coupled inductor also increases. The switch is turned off when sufficient energy is stored in the inductor to meet the power demand. Turning off the switch marks the end of this period. Calculations for vital parameters are as followed.

$$I_{LP} = \frac{Vd_1 * t}{L_p} \quad (3)$$

$$I_{LS} = 0 \quad (4)$$

$$V_{DS} = 0 \quad (5)$$

$$V_{SR,Diode} = Vd_2 + Vd_1 * N \quad (6)$$

$$I_{LP,peak} = \frac{Vd_1 * T_{ON}}{L_P} \quad (7)$$

$$E = \frac{1}{2} L_P {I_{LP,max}}^2 \quad (8)$$

$$P = \frac{1}{2} L_P {I_{LP,max}}^2 * f \quad (9)$$

Here,

- 0<t< T_{ON}
- I_{LP}: current through the primary inductance at time t.
- I_{LS}: current through secondary inductor at time t.
- N : turn ratio; $N = \frac{N_2}{N_1}$; $n = \frac{1}{N} = \frac{N_1}{N_2}$
- V_{DS}: Voltage across the drain and the source of switch S1.
- $V_{SR,Diode}$: reverse voltage stress across diode D2.
- $I_{LP,peak}$: is the maximum current through the primary inductor (at t=T_{ON})
- E: Input energy during one period of the converter.
- P: Input power of the converter.

T_{OFF} Period:

During this period, switch S2 is closed. Therefore, current cannot flow through the MOSFET. On the secondary side, the diode becomes forward biased and start conducting. The stored energy in the coupled inductor transfers to the output as the current decrease to zero from a maximum value in the secondry.

$$I_{LP} = 0 \quad (10)$$

$$I_{LS,peak} = I_{LP,peak} * n - \frac{Vd_2 * t}{L_S} \quad (11)$$

$$V_{Diode} = V_{Forward\ bias} \quad (12)$$

Here, $I_{LS,peak}$ is the peak current at the secondary at the start of $\boldsymbol{T_{OFF}}$ period

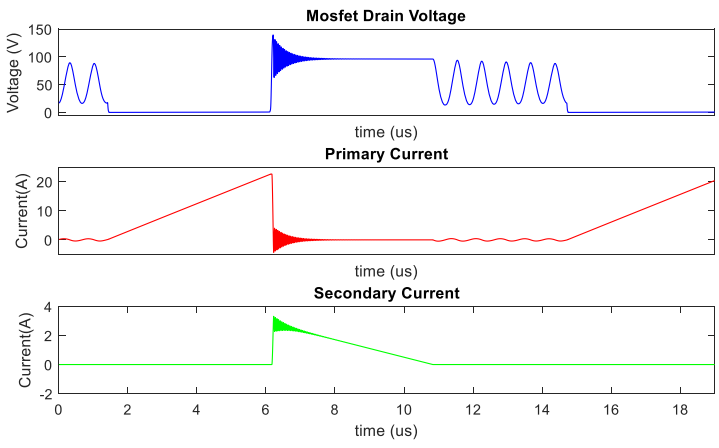


Figure 12: DCM-VS Waveforms

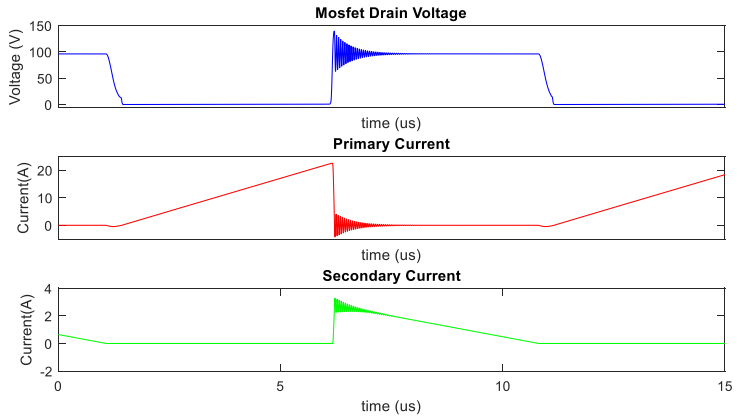


Figure 13: BCM-VS Waveforms

The transformer is not ideal in real life; the leakage inductor is always present as some flux always escapes the core and the windings. Due to this leakage inductor, current cannot change the direction instantaneously at the beginning of the T_{OFF} period. Also, diode capacitance must be discharged to zero before current can flow at the secondary side. As the current cannot start flowing instantaneously from the secondary winding, and the switch is also off, the current start to charge the capacitor across drain and source of the MOSFET. When the voltage at the drain reaches to $Vd_1 + \frac{Vd_2}{N}$, the diode starts conducting. Still current at the secondary cannot change abruptly due to the leakage inductance. The Current keeps charging the capacitance till the current at secondary reaches to the $I_{LP,peak} * n$. The energy stored in the leakage inductor and the parasitic capacitance oscillates with frequency f_{Ripple}. This oscillation causes the voltage ringing at the drain and current ringing at both sides. Voltage and current ripples are shown in Figure 12 and Figure 13 at the start of T_{OFF}. Due to the voltage ringing, the voltage stress is higher across the MOSFET resulting in higher breakdown voltage rating for the MOSFET. The voltage transients appear due to the resonance between leakage inductor and the parasitic capacitance across the drain and the source of the MOSFET. The frequency and the amplitude of voltage ringing can be calculated using eq. (13) and eq. (14) .

$$f_{Ripple} = \frac{1}{2\pi\sqrt{L_{Leakage}C_{Par}}} \quad (13)$$

$$V_{Ripple} = I_{P,max} * \sqrt{\frac{L_{Leakage}}{C_{Par}}} \quad (14)$$

The Voltage Stress:

$$V_{SR,MOSFET} = Vd_1 + \frac{Vd_2}{N} + V_{Ripple} \quad (15)$$

The voltage stress across the MOSFET can be decreased by placing an external capacitor across the switch

Resonance Period:

As soon as current decreases to zero in the secondary winding, the diode stops conducting. The input voltage appears across the series combination of primary inductance and the parasitic capacitanceresulting in resonance. The voltage magnitude of the resonance frequency is determined by the primary inductance and the parasitic capacitance across MOSFET. The voltage between the drain and the source of the MOSFET varies between $Vd_1 + \frac{Vd_2}{N}$ to $Vd_1 - \frac{Vd_2}{N}$. To achieve the valley switching switched is turned off at the valley of the voltage that is $Vd_1 - \frac{Vd_2}{N}$. In case if $Vd_1 < \frac{Vd_2}{N}$ then switch is turned on at zero MOSFET drain voltage to achieve zero voltage switching. Due to the leakage inductance, the amplitude of the voltage can be higher than $\frac{Vd_2}{N}$. This helps in achieving the zero switching even if $Vd_1 > \frac{Vd_2}{N}$. Due to the leakage inductance, zero voltage switching can be achieved for bi-directional power flow when the turn ratio is selected such that $Vd_1\ and\ \frac{Vd_2}{N}$ are nearly equal. The time-period of the resonance is calculated using eq (16)

$$T_{Res} = 2\pi\sqrt{L_{Leakage}C_{Par}} \quad (16)$$

DCM and BCM waveforms are shown in Figure 12 and Figure 13 respectively. The difference between these two modes is the switching instance. In case of BCM-VS, the switch is turned on at first valley of the voltage. In contrast to BCM-VS, the switch is closed at the nth valley when operating in the DCM-VS mode when n is larger than 1.

The duration of resonance period:

$$T_R = n * \pi\sqrt{L_{Leakage}C_{Par}} \quad (17)$$

Where n=1 is for BCM-VS, n>1 represents DCM-VS.

3.
Flow Converter Design

3.1. Flow Converter

The proposed bi-directional flyback converter is a flow controller which is responsible for connecting the SHS with the larger Microgrid. The primary functions of this converter are bi-directional power flow, load sharing and the voltage regulation at HVB. As decentralized control is selected to implement coordinated control in the MG, flow converter operates without any communication from other components. Limited information is communicated using the DC voltage at the LVB and HVB using DC bus signaling (DBS).

Figure 14 shows the simplified schematic of the bi-directional converter. This topology is inspired by unidirectional flyback; the secondary side diode is replaced by a MOSFET to make it bidirectional. During the transfer of power in any direction, only one MOSFET is active. The body diode of other MOSFET (not active) takes the role of the regular diode. Therefore, the component count remains the same as in unidirectional flyback.

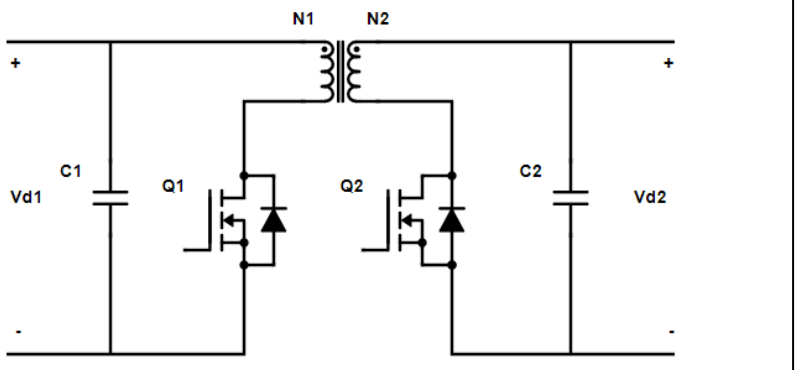


Figure 14: Schematic of Bi-directional Flyback

As discussed in the literature review that soft switching must be implemented to reduce the losses in the MOSFET, voltage ringing, and the EMI, flyback is being operated in the BCM-VS and DCM-VS,

3.2. Flow Converter Requirements

The requirements for the flow converter can be divided into three categories: a.) Power Stage Requirements b.) Local Level Control Requirements c.) System Level Control Requirements. The power stage requirements will be discussed in this section. The local level control requirements and system level requirements will be discussed in chapter 4 and chapter 5 respectively. The power stage requirements are the following:

1. Bi-directional Power Flow: Converter should be able to transfer power in both directions. The Maximum power that can be transferred from the low voltage side to the high voltage side is 300W. Flow converter should also be able to transfer 200W power from high voltage side to low voltage side. When delivering the power from the high voltage side to the low voltage side, charge controller and low voltage load controller present themselves as a load. 200W is the combined rating of charge converter and low voltage load converter
2. Input Voltage range: While delivering the power from the low voltage side to the high voltage side, low bus voltage is the input for the flow controller. As DBS is implemented to achieve fully decentralized control, the voltage at the low voltage bus can vary in a wide range. Flow converter should be able to work for the input voltage between 30V to 60V. While delivering power from HVB to LVB, however, HVB voltage is not expected to vary much as the only deviation is due to the droop implementation, the HVB voltage can change from 320V to 450V.
3. Soft switching: Soft switching must be implemented by changing the normal operating modes of flyback instead of the additional resonant circuit. The additional circuit increases the cost and complexity of the design.
4. Efficiency: Losses in the transformer, switches, gate circuit, and the capacitors should be minimized to achieve high efficiency. Reduction in power losses increase the utilization of power, thus reducing the electricity cost per unit, and it also reduces the complexity of heat management as low power losses result in less temperature deviation. However, it is not the most important goal of this work.
5. Galvanic Isolation: Isolation is a requirement for this converter as the converter is connected to 380Vside. Moreover, as the voltage step ratio (when transferring power from 48V to 380V side) is around eight, the transformer is required to match the voltage.
6. Operating frequency of the converter should be high enough to reduce the size of the converter. However maximum frequency should not cross 125KHz limit as switching losses will increase and EMI restriction will also come into the picture.

3.3. Frequency Selection:

When current control is implemented for the flyback converter, the frequency is not a controlling parameter; it is a result of the control. However, that does not decrease the importance of selecting the correct frequency for the maximum power transfer and complete power range. A proper selection of the frequency for the complete operation of the flyback results in smaller size, better efficiency, and better EMI compliance.

However, all of these cannot be achieved simultaneously. Furthermore, the cost is an additional restriction which must be considered.

It is a known fact that the size of the converter depends on the frequency. One of the bulkiest components in flyback is the transformer, and its size is inversely proportional to the frequency. In an ideal situation, we would like converter size as small as possible, so it is expected to choose a higher value of the frequency while choosing a core material which holds its magnetic property on this frequency. However, higher switching losses and EMI limit the frequency which can be used.

In the flyback BCM without valley switching, peak current through primary is independent of inductor value.

$$I_{LP,peak} = \frac{2 * P}{V_{d1} * D} \tag{18}$$

Eq. (18) can be modified for BCM-VS mode eq. (19)

$$I_{LP,peak} = \frac{2 * P}{V_{d1} * D_{ON}} * \frac{T}{T_{ON} + T_{OFF}} \tag{19}$$

Substituting the value of D_{ON}, T_{ON}, D_{ON} and D_{ON} $in\ eq.(19)\ yields$ in eq (20)

$$I_{LP,peak} = 2 * P * \left(\frac{V_{d1} + \frac{V_{d2}}{N}}{\frac{V_{d2}}{N} + V_{d1}(1 - T_{R,BCM}} \right) \tag{20}$$

As it can be seen from equation (19) that peak current does not depend on the frequency and the inductor value, therefore, winding wires must carry the same current for a specific power level irrespective of the selected value of frequency. At high frequency, skin effect limits the wire size. It is common to use litz wire for the transformer design at high frequency. If litz wire is used, then the diameter of a litz strand will decrease with the frequency. Therefore, to keep the total copper area the same, the number of strands must be increased; this will give effectively same DC resistance. If a small diameter litz wire is used, then winding area of the coil former is not fully utilized. Furthermore, it is not easy to manage a large number of strands in the lab. Therefore, if high currents flow in the winding, the frequency must be reduced for optimized operation of the converter.

In the recent times, Electromagnetic emission from home appliances has gained a lot of attention due to the increasing number of such devices. The combined effect of this emission can have an adverse impact on human health. Furthermore, electronic appliances are sensitive to EMI level. Therefore, proper attention should be given to reduce the EMI. Electromagnetic emission increases with the higher rate of change in

current or voltage. As the maximum peak current does not depend on the frequency selection, EMI increases due to the high rate of change for high frequency. A higher value of EMI results in corrupting the communication signal like RF. There is no EMI standard available right now for SHS system, but it is reasonable to expect that there would be similar standard as currently deployed in consumer electronics.

There are many controllers available in the market with a vast number of functionality. These controllers allow maximums frequency to go up to around 125KHz. While operating in QR or BCM-VS mode, power decreases This design aim to transfer maximum power transfer at 70KHz. Actual frequency can deviate when considered valley switching and the deviation in the value of components.

3.4. Design Parameters Calculation:

The calculation for vital parameters such as turn ratio, inductor value, maximum current number of turns is explained in this section.

3.4.1. Turn Ratio Calculation:

In BCM mode without valley switching, duty cycle does not depend on the value of power transfer. For BCM-VS switching, the value of duty cycle changes little due to constant resonance time. However, variation is not much as resonance time is small compared to the time period.

One of the main advantages of BCM-VS mode is that low turn-on losses because switch turns on at the valley or zero voltage. As we are designing a bi-directional converter, we must optimize turn-on losses for power flow in both directions. In that case, an obvious choice is a ratio of high voltage side voltage and low voltage side voltage.

$$N = \frac{V_{dH}}{V_{dL}} = \frac{380V}{48V} = 7.92 \quad (21)$$

As 7.92 is not the integer, this value can be round up or round down. N=8 will be used for the design calculation.

$$N = 8 \quad (22)$$

$$n = \frac{1}{N} = 0.125 \quad (23)$$

Furthermore, the power loss in the converter depends on the duty cycle of the waveform. In real life, the duty cycle of the converter is kept between 0.2 to 0.8 to increase the efficiency. When transferring the power (in BCM-VS), the selected turn ratio would result in a duty cycle of 0.5 at the nominal input and output voltage. Also,

for a wide range of variation in the LV voltage and HV voltage, the duty cycle remains between 0.3 and 0.7 as shown in Table III.

The losses in the core are dependent on the shape and duty cycle of the waveform. Figure 15 shows the loss ratio of a triangular wave and pure sine wave as function of duty cycle. The core losses are lower and constant for duty cycle between 0.3 and 0.7. The ratio of core losses when excited with a triangular wave and the sine wave is expressed as the function of the duty cycle in eq. (24).

$$Core\ Loss\ Ratio = \frac{2}{\pi^2 D(1-D)} \tag{24}$$

Table III: Duty Cycle calculation for different voltages level

LVB Voltage	HVB voltage	Duty Cycle	
		LV-HV flow	HV-LV flow
48	380	0,50	0,50
30	380	0,61	0,39
60	380	0,44	0,56
48	300	0,44	0,56
30	300	0,56	0,44
60	300	0,38	0,62
48	450	0,54	0,46
30	450	0,65	0,35
60	450	0,48	0,52

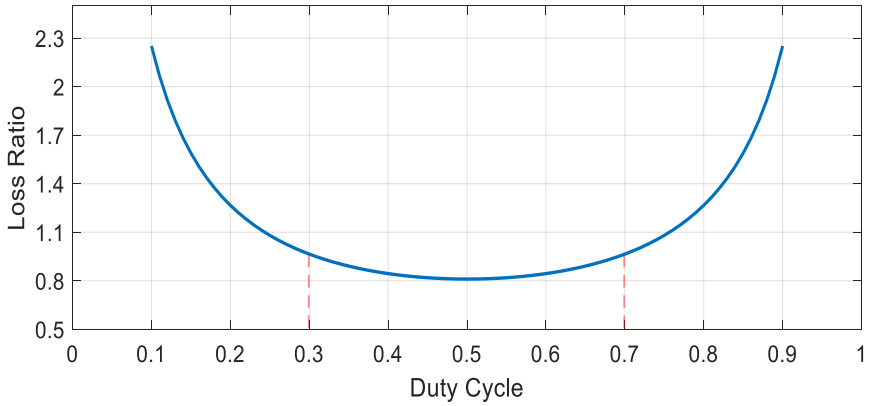


Figure 15: Loss ratio vs duty cycle

3.4.2. Inductor Calculation:

In the flyback circuit, the transformer is used to store the energy rather than instantaneous power transfer. It stores the energy during the turn-on phase and transfers the energy to the secondary side during the turn off time. During resonance time, energy is neither stored nor transferred. Therefore, the flyback transformer work as a coupled inductor which performs the function of energy storage, energy transfer and isolation [12]. The value of the inductor determines the frequency at which maximum power is delivered.

The value of the inductor L_L and L_H is first calculated by assuming that flyback is operating in genuine BCM Mode. Later, the correction factor is multiplied to correct the error due to valley switching.

$$L_{L,BCM} = 0.5 * \frac{(V_L * D_{BCM})^2}{f_{Pmax} * P_{max}} \quad (25)$$

with,

- $\mathrm{D_{BCM}}$: duty cycle in genuine BCM mode. The duty cycle for different LVB and HVB voltage is shown in Table III. For the calculation of the inductor, the duty cycle corresponds to nominal LVB and HVB voltage is used that is 0.5.
- $P_{max} = 330W$, the maximum power that to be delivered. The maximum power rating of the converter is 300W. 10% tolerance is taken considering the losses while designing the converter.
- $f_{Pmax} = 60KHz$, operating frequency corresponds to maximum power.

The correction factor must be multiplied to compensate for extra time due to the valley switching.

$$L_L = L_{L,BCM} * \frac{(1-\sqrt{k})^2}{(1-k)^2} \quad (26)$$

Here,

$$k = \pi^2 \frac{L_{1,bcm} * C_{L,par}}{(T_{Pmax})^2} \quad (27)$$

The high side inductor value can be written as multiplication of low voltage side inductor and square of turn ratio N.

$$L_H = N^2 L_L \quad (28)$$

Calculation of k depends on the value of $C_{1,par}$ and T_{Pmax}. Period T_{Pmax} itself depends on the inductor value. Therefore, a mathematical equation solver is needed to calculate the inductor value. However, one can simply use approximation value to calculated inductor values, and after the design, a check must be performed to check if all the parameters are in the expected range. The approximation results in a small error. The change in the inductor value, due to approximation or manufacturing error, would also cause a deviation in the frequency for maximum power transfer. Small deviation in the frequency does not have much impact on the performance and functionality of the converter.

The total parasitic capacitance between drain and source of MOSFET can be calculated using the following equation

$$C_{\mathrm{L,par}} = C_{\mathrm{L},oss} + C_{\mathrm{L},ext} + (C_{\mathrm{H},oss} + C_{\mathrm{H},ext}) * N\text{^}2 \quad (29)$$

$$C_{\mathrm{H},par} = (C_{\mathrm{L},oss} + C_{\mathrm{L},ext}) * n\text{^}2 + C_{\mathrm{H},oss} + C_{\mathrm{H},ext} \quad (30)$$

External capacitances placed between drain and source at both sides appear in the equations for total parasitic capacitance. The selection of external capacitance is based on the following two criteria.

- External capacitance is placed to ensure minimal turn-off losses. Usually, the minimum value of capacitance that results in minimal turn-off losses is selected.
- The capacitance value between drain and source of the MOSFET plays an important role in restricting the amplitude of the voltage ringing at the start of turn-off period. By placing an external capacitance, the oscillating voltage can be reduced. The selected value of parasitic capacitance should be such that voltage ringing at the drain of the MOSFET does not exceed the breakdown rating of the MOSFET.

Calculating the required value of external capacitance requires the accurate model of the MOSFET and the transformer. Generally, spice models provided by the manufacturer are not precise and results in significant error. Therefore, the external capacitance is selected based on the experiments. The capacitance value is increased till the turn-off losses, and voltage ringing at turn-off is reduced to a satisfactory level. As MOSFET is turned on at the valley, therefore, no extra losses due to high capacitance, as big as required external capacitance can be selected. In unidirectional flyback, there is no major disadvantage of the large external capacitance apart from the extra cost of the capacitance. In contrast, in bi-directional flyback, this capacitor will appear across the anti-body diode while transferring power in the opposite direction. This increases the coupling between primary and secondary, in our case low voltage side and high voltage side. It also increases the diode reverse recovery time hence decreases the efficiency of the converter.

3.4.3. Current Calculation:

3.4.3.1. Peak Current

The current in the inductor reaches its peak at the end of the turn-on period. The energy equation can be rewritten to obtain the equation for the peak current.

$$I_{L,peak} = \sqrt{\frac{2 * P}{L_L * f}} \quad (31)$$

$$I_{H,peak} = \sqrt{\frac{2 * P}{L_H * f}} \quad (32)$$

The eq. (31) and eq. (32) equation are valid for all three operating modes namely QR, DCM-VS, and FR mode.

3.4.3.2. Maximum Current

The maximum current of the flyback is the peak current through the inductor while delivering the maximum power. Maximum current can be calculated by putting maximum power value in eq. (33) and eq. (34)

$$I_{L,max} = \sqrt{\frac{2 * P_{max}}{L_L * f_{Pmax}}} \quad (33)$$

$$I_{H,max} = \sqrt{\frac{2 * P_{max}}{L_H * f_{Pmax}}} \quad (34)$$

3.4.3.3 RMS Current

For BCM-VS or QR mode, RMS current can be approximated using eq (35) and eq (36) if power flow direction is from low voltage side to high voltage side.

$$I_{L,rms} = I_{L,peak} * \sqrt{\frac{D_{ON}}{3}} \quad (35)$$

$$I_{H,rms} = I_{H,peak} * \sqrt{\frac{D_{OFF}}{3}} \quad (36)$$

If current direction is from high voltage side to low voltage side, rms current is calculated using e. (37) and eq. (38)

$$I_{L,rms} = I_{L,peak} * \sqrt{\frac{D_{OFF}}{3}} \quad (37)$$

$$I_{H,rms} = I_{H,peak} * \sqrt{\frac{D_{ON}}{3}} \quad (38)$$

3.5. Transformer Design:

In most of the power electronics converters works as an instant power transfer device. The primary function of a transformer is transfer of power efficiently and instantaneously from an external electrical source to an external load [12]. A transformer also provides the capability of stepping up and stepping down the voltage, isolation between the high voltage and low voltage side and, if needed, multiple outputs. To ensure that energy is transferred instantaneously, the transformer is designed to reduce the energy storage. Therefore, it is desirable that the magnetic inductance of the transformer is as large as possible.

However, the function of the transformer in the flyback is to store energy during the T_{ON} period of the converter and transfer the energy to during T_{OFF} period. Therefore, inductor plays an important role and determining the operating frequency.

The design of the transformer can be divided into 6 steps:

1. Selection of tentative core materials, core shapes, and core size.
2. Number of turns calculation for each selected core
3. Air Gap calculation.
4. Comparison of selected cores.
5. Wire selection for the winding and resistance calculation.
6. Calculation of winding losses, core losses, and total loss.
7. Selection most efficient core.

3.5.1. Core Shape, Size and Material Selection:

The first step of designing the transformer is a selection of tentative cores. There are some guidelines available regarding the selection of the core size and the material. However, these guidelines are not final. Selecting the core for flyback is an extensive process as transformer plays an important role in energy storage and transfer. Different core sizes with different material must be checked to optimize the efficiency and the size.

Table IV: Power Throughput for different core types at the 100KHz switching frequency.

Power Range (W)	Core Type
<5	RM4, P11/7, T14, EF13, U10
5-10	RM5, P14/8
10-20	RM6, E20, P18/11, T23, U15, EFD 15
50-10	RM8, P22/13, U20m, RM10, ETD29, E25, T26/10, EFD20
100-200	ETD34, ETD39. ETD44, EC41, EC52, RM14, P36/22, E30, T58, U25, U30, E42, EFD30
200-500	ETD44, ETD49, E55, EC52, E42, P42/29, U67
>500	E65, EC70, U93, U100, P66/56, PM87, PM114, T140

Table IV can be used to select the size of core and shape. ETD44, ETD49 and E42 are suitable for 300W bi-direction flow converter. E55, EC52, and U67 are too big for this application while P-type cores (Pot cores) are usually expensive. For the flow converter, the following four cores are being analyzed.

1. ETD44/22/15-3C90
2. ETD49/25/16-3C97
3. E42/21/20-N95
4. E42/21/20-N95

3.5.2. Number of turns Calculation:

Current in the transformer is proportional to the multiplication of number of turns and the flux density in the core. For a lower number of turns in the winding, flux density will be higher, and the transformer may get saturated. Even if the transformer is not saturated, there will be higher core losses at higher flux density. If a higher number of turns are selected, the resistance of the winding will increase.

Furthermore, the proximity effect also becomes significant with a large number of turns, hence higher winding losses. Therefore, a minimum number of turns must be selected such that maximum flux density is less than the saturation density with enough margin. The number of low voltages side winding turns can be calculated using equation ()

$$N1 = \frac{L_L * I_{1\mathrm{p,max}}}{A_{min} * B_{max}} \quad (39)$$

The saturation flux density, minimum area and the calculated number of turns for each core type is tabulated in Table V

Table V: Number of turns calculation

Core Name	B_{sat} (mT)	B_{max} (mT)	A_{min} (m^2)	N1	N2
ETD44/22/15-3C90	330	280	172	7	56
ETD49/25/16-3C97	330	280	209	6	48
E42/21/20-3C90	525	280	175	6	48
E42/21/20-N95	525	280	234	5	40

3.5.3. Air Gap Calculation:

The calculation of the air gap is explained in this section. The flux density remains same across the boundary if no charge is present at the boundary. It can be written in form of eq. (40). Here B_c is the flux density in the core and B_g is the flux density in the air gap.

$$B = B_c = B_g \tag{40}$$

Substituting B=uH in eq. (40) yields eq. (41).

$$H_c * \mu_c = H_g * \mu_g \tag{41}$$

$$N_1 * I_{L1} = H_c * l_c + H_g * l_g \tag{42}$$

From eq. (41) and eq. (42):

$$H_g = \frac{N_1 * I_{L1}}{l_g + l_e * (\frac{\mu_g}{\mu_e})} \tag{43}$$

Flux in the core can be written in the form eq. (46)

$$\emptyset = A_e * B = A_e * H_g * \mu_g \tag{44}$$

Substituting the value of H_g results in eq. (45)

$$\emptyset = A_e * \left(\frac{N_1 * I_{L1} * \mu_g * \mu_l}{\mu_l l_g + \mu_g l_l}\right) \tag{45}$$

$$N_1 * \emptyset = L_1 * I_{L1} = A_e * {N_1}^2 \left(\frac{\mu_g * \mu_l}{\mu_l l_g + \mu_g l_l}\right) * I_{L1} \tag{46}$$

Simplification of eq. (46) results in,

$$L_1 = A_e * {N_1}^2 \left(\frac{\mu_r * \mu_o}{\mu_r l_g + l_l}\right) \tag{47}$$

Rearranging the eq. (47) yields the equation for air gap.

$$l_g = \left(\frac{A_e * {N_1}^2 * \mu_r * \mu_o - l_l}{\mu_r * L_1}\right) \quad (48)$$

After the air gap calculation, it must be checked if air gap is not too large, otherwise above calculation will not hold, and leakage inductance becomes too high. The ratio of air gap and the square root of the core area should be less than 0.1.

$$\frac{l_g}{\sqrt{A_e}} < 0.1 \quad (49)$$

All the selected cores satisfy eq. (49).

3.5.4. Comparison of Cores:

The power losses in different components of converters are temperature dependent and generally increases with the temperature. In contrast, power cores are optimized for high temperature while operating on maximum power. The losses in power core increase with decreasing temperature at constant voltage and frequency. Therefore, core losses dominate at low or no-load conditions [16]. Consequently, it becomes important to select a core which shows perform optimally for full temperature range including the room temperature.

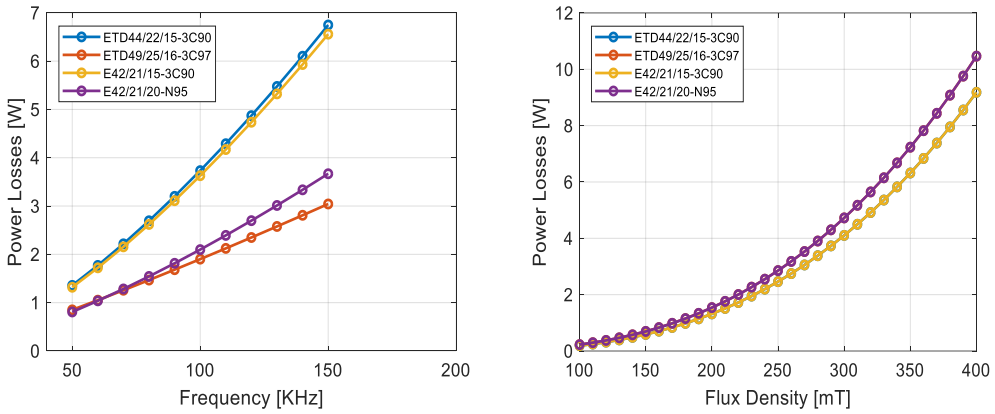
In this section, a comparison of the performance of selected cores based on the power losses is being presented. Power losses have been approximated using eq. (50) across the temperature, flux densities and the frequencies.

$$P_{core\ loss} = k f^x B^y (C_0 + C_1 T + C_2 T^2) V_e \quad (50)$$

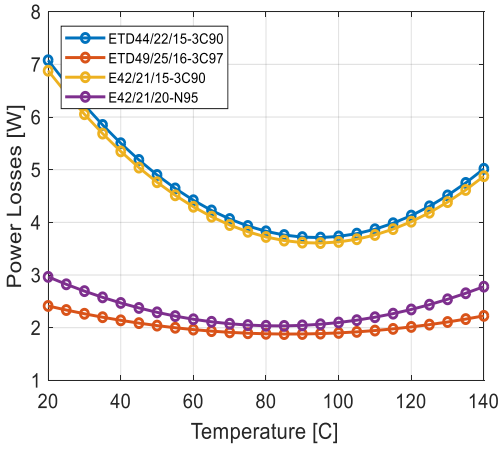
Here,

- k, x, y, C_0, C_1, C_2 are curve fitting coefficients. These values can be found in the respective datasheets.
- V_e: effective volume of the core.

Frequency versus power losses has been plotted in Figure 16 (a), flux density versus power losses in Figure 16 (b) and temperature versus power losses in Figure 16 (c). ETD49/25/16-3C97 performs better in all the simulated conditions compare to the other cores. Therefore, ETD49/25/16-3C97 is selected for the flow converter.



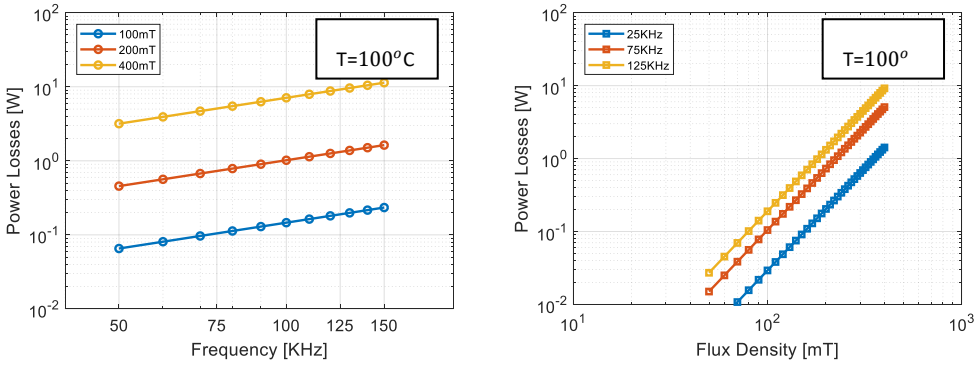
(a) (b)



(c)

Figure 16: (a) Power losses vs Frequency at B=250mT and T=100 (b) Power losses vs Flux density at f=125kHz and T=100 (c) Power losses vs Frequency at B=250mT and T=100

More power losses plots for ETD49/25/16-3C97 are shown in Figure 17.



(a) (b)

Figure 17: (a) Power losses vs Frequency (b) Power losses vs Flux density

3.5.5. Wire selection for the winding:

Maximum peak current at low voltage side is 30A. The litz wire cannot be used for low voltage side winding because a number of strands becomes too high for this current value. Also, a regular thick wire will result in very high resistance due to the skin effect. Therefore, copper foil is used for low voltage side winding. For high voltage side winding, litz wire is used as current is eight-time small compared to the low voltage side. The skin depth for the copper litz wire can be calculated using eq. (51)

$$\delta = \frac{1}{\sqrt{\mu_r \mu_o \sigma \pi f}} \tag{51}$$

Here,

- δ: Skin depth
- μ_r: relative permittivity of the material
- μ_o: permittivity in the air.
- σ: conductivity of mathe terial. For copper σ =1.68×10^{-8} Ω·m
- f = frequency; 125KHz

For copper skin depth at 125kHz is 0.183mm. A litz wire with the strand diameter of 0.2mm or less can be used. For the flow controller prototype, 0.2*20mm litz wire is used. The AC resistance of the winding is the function of the number of layers and the frequency. The ratio of ac resistance and dc resistance can be calculated using Dowell's eq. (52).

$$RF = \Delta' \left[\varsigma_1' + \frac{2}{3} \varsigma_w^2 (m^2 - 1) \varsigma_2' \right] \tag{52}$$

Figure 18 shows the resistance ratio versus frequency plot. The AC resistance increases with a number of layers and the frequency.

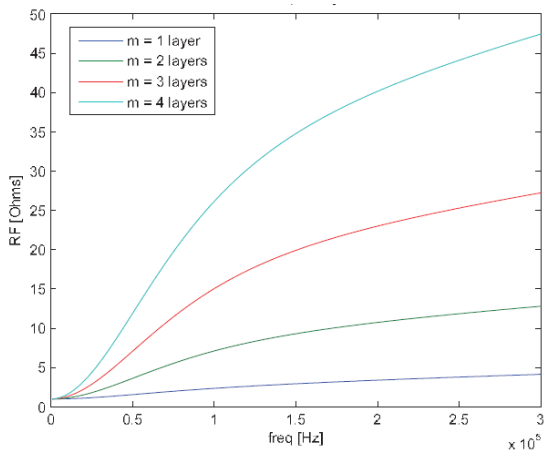


Figure 18: Resistance Factor variation with frequency

3.6. MOSFET Selection:

The following considerations should be taken into the while selecting the MOSFET for bi-directional flyback.

1.) ***Breakdown voltage:*** During the turn-off time, the sum of the input voltage, reflected voltage from the secondary side and the ringing due to the leakage inductance appears across the MOSFET. Therefore, MOSFET breakdown voltage should be higher than this sum. For the flow converter, when the power flow direction is from the low voltage side to high voltage side, the sum of the input voltage and the reflected output voltage is 98V. The voltage spikes are generally in the range 20-50 percent of the sum of the input voltage and reflected output voltage. It is wise to leave some margin; a decent margin is around 40 percent. Therefore, a MOSFET with a breakdown voltage of more than 200V should be selected. For a high voltage side, the breakdown voltage value is 8^{th} times compare to low voltage side MOSFET. Thus, MOSFET with breakdown voltage around 1500 volts is sufficient. A lower voltage rating of MOSFET can also be used, in that case, an external capacitor is placed across drain and source of the MOSFET to reduce the voltage ringing.

2.) ***Turn-on Resistance (R_{ON}):*** Total MOSFET losses in the converter is the combination of switching losses and conducting losses. The switching losses are lower compared to conduction losses because the switch is turned on at the valley or the zero-voltage resulting in low switch on losses, and switch-off losses can be minimized by placing an external capacitance. Therefore, it is important that a MOSFET with a lower value of turn-on resistance is selected to reduce the conducting losses. The turn-on resistance increases with temperature as shown in Figure 19 for STW21N150K5. Therefore, it is necessary to check the R_{ON} across the temperature not only on the room temperature. To ensure that the MOSFET junction temperature does not cross the limit set by the design, Ron must be checked at maximum allowed temperature.

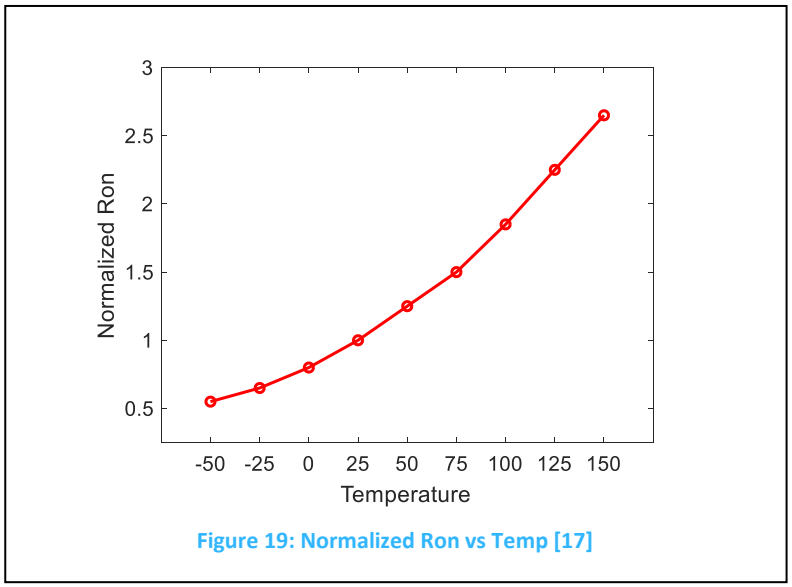


Figure 19: Normalized Ron vs Temp [17]

It must be noted that turn-on resistance is inversely proportional to the breakdown voltage. The breakdown voltage is increased by increasing the channel length in the MOSFET; this results in higher R_{ON}.

Reverse Recovery of the Diode: When switching from forward bias to the reverse bias, the diode has a stored charge that must be discharged before diode starts blocking the current in opposite direction. Reverse recovery characteristics are shown in Figure 20. Reverse recovery of the diode is not a very difficult requirement to meet when designing unidirectional flyback, and usually not considered in the design as a fast recovery diode can merely be used without any penalty. However, in the bi-directional flyback, the current during the turn-off period flows from anti-body diode of the other MOSFET. The reverse-recovery of these diodes is usually not as fast as these are not designed for this purpose. Moreover, if the external capacitor is placed to reduce the ringing and the turn-off losses, this exacerbates the diode recovery. During the reverse recovery time, current flows in the reverse direction before blocking the reverse current. This means that the output side capacitor is putting back the energy in the transformer. As soon diode stop conducting, this current is transferred to the primary side, the current starts from this value rather than zero at the beginning of resonance time. After the MOSFET is switched on, this current increase to zero, and later to the peak current value corresponding to the power level. Ideally, the secondary side should not put back energy in the magnetic; this increases the total period of one cycle that results in a low value of power for the same current, hence decreasing the efficiency. Furthermore, charging the magnetic in the reverse direction and then later discharging the magnetic also results in additional core losses and the conduction losses at the input side.

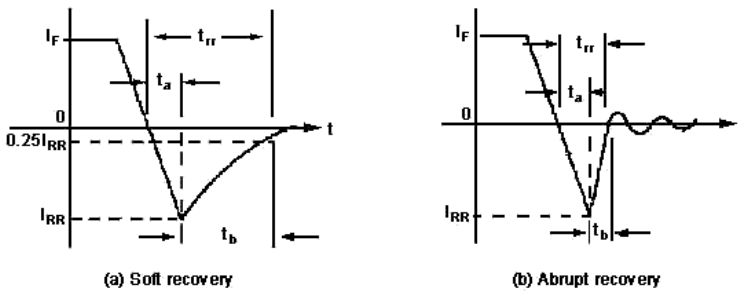


Figure 20: Reverse Recovery characteristics [16]

3.) ***Forward bias voltage of the reverse diode***: The forward bias voltage of the diode should be as minimum as possible to minimize conduction power losses in the diode.

4.) ***Automotive standard:*** The MOSFET be automotive standard to handle the high temperature.

It is not possible to find the MOSFET which is optimized for all parameters as some of the considerations are contradictory. After taking all the consideration in the account, IPB200N25N3 G is used at the low voltage side and STW21N150K5 is used at the high voltage side.

3.7. Power Loss & Efficiency Calculation:

The power losses in the flyback converter have been calculated using eq. (53) to eq. (58) for power direction flow from low voltage side to high voltage side:

1.) ***MOSFET Conduction Losses:***

$$PL1 = {I_{LV}}^2 * (R_{on} + * R_{sense,LV}) \quad (53)$$

It is assumed that the junction temperature of the MOSFET is 100^oC. That is the correct approximation when maximum power is delivered. However, for low power, the temperature will be around the room temperature.

2.) ***Diode Conduction Losses***:

$$PL2 == I_{HV,avg} * V_{sd} + {I_{LV,rms}}^2 * R_{sense,HV} \quad (54)$$

3.) ***Core Losses:*** Core losses are calculated using eq. (50).

4.) ***Gate Driver Losses:***

$$PL4 = Gate\ Driver\ Loss = Q_g V_g f v \quad (55)$$

5.) ***MOSFET Switching Losses:***

$$PL = Turn\ ON\ Loss + Turn\ OFF\ Loss \quad (56)$$

6.) ***Winding Losses:***

$$PL6 = {I_{LV,rms}}^2 * R_{Lw,ac} + {I_{HV,rms}}^2 * R_{2w,ac} \quad (57)$$

7.) ***Sense Resistors Losses:***

$$PL7 = {I_{LV,rms}}^2 * R_{sense,LV} + {I_{LV,rms}}^2 * R_{sense,HV} \quad (58)$$

The power losses in the flow converter for power flow direction from HV to LV can be calculated by replacing the parameters in eq. (53) to eq. (58)

3.8. Test Results & Simulations:

3.8.1. Flow Converter Results:

Based on the calculation in this chapter, flow converter modeling was performed in the MATLAB and power losses were calculated. In Figure 21, conduction losses, other losses and total power losses are plotted as a function of input power. The total Conduction losses include conduction losses in MOSFET, diode, windings and sense resistors. Other losses include core losses and switching losses in the switch. At high input power, the conduction losses dominate and determine the efficiency. At low input power, the conduction losses are smaller than core losses and switching losses. At low input power, temperature of the core is lower than optimized core temperature. Therefore, additional losses occur in the core.

In Figure 22, the simulated operating frequency and peak current is plotted as a function of input power. The maximum power (300W) is transferred at 65KHz. As the peak current decreases in the flow converter, the input frequency increases while input power decreases linearly with the peak current. At 125W power, frequency reaches the maximum value. The Frequency is kept constant till power drops below 90W. For power between 0 to 90W, the current is kept constant, and power decreases with frequency.

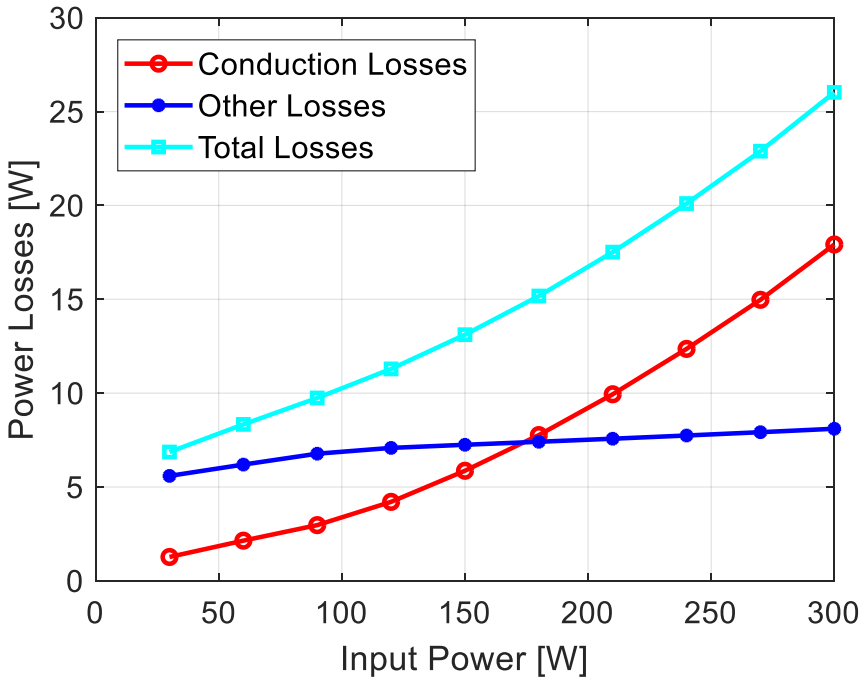


Figure 21: Power Losses (LV to HV power flow)

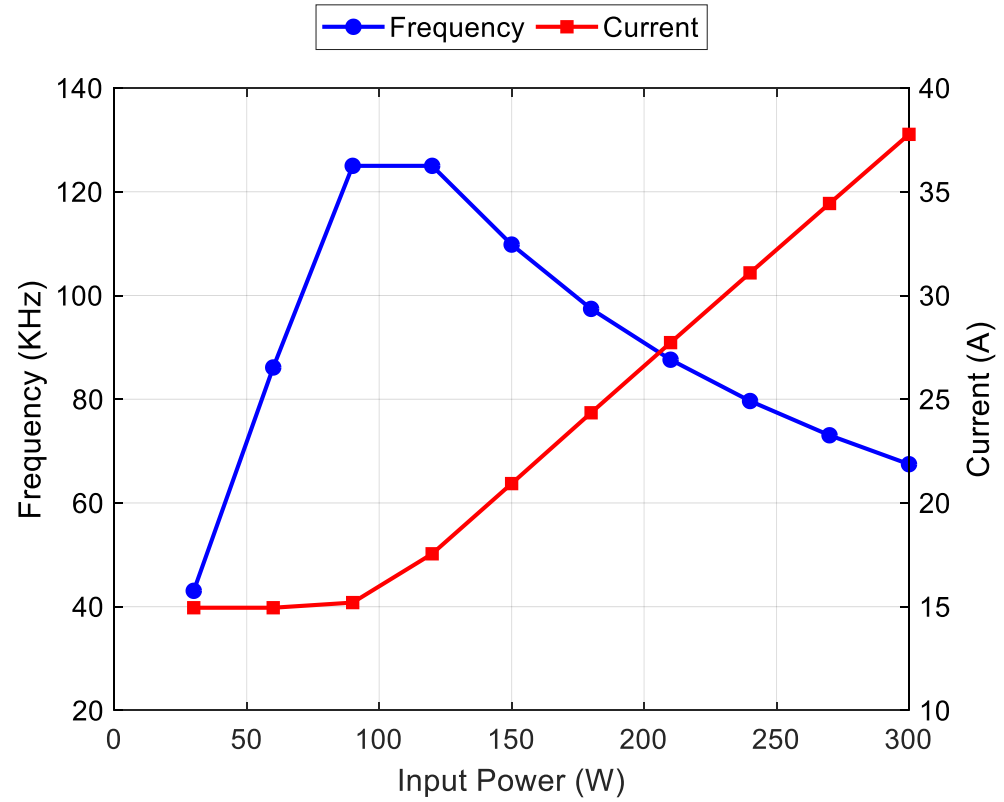


Figure 22: Frequency and current (LV to HV power flow)

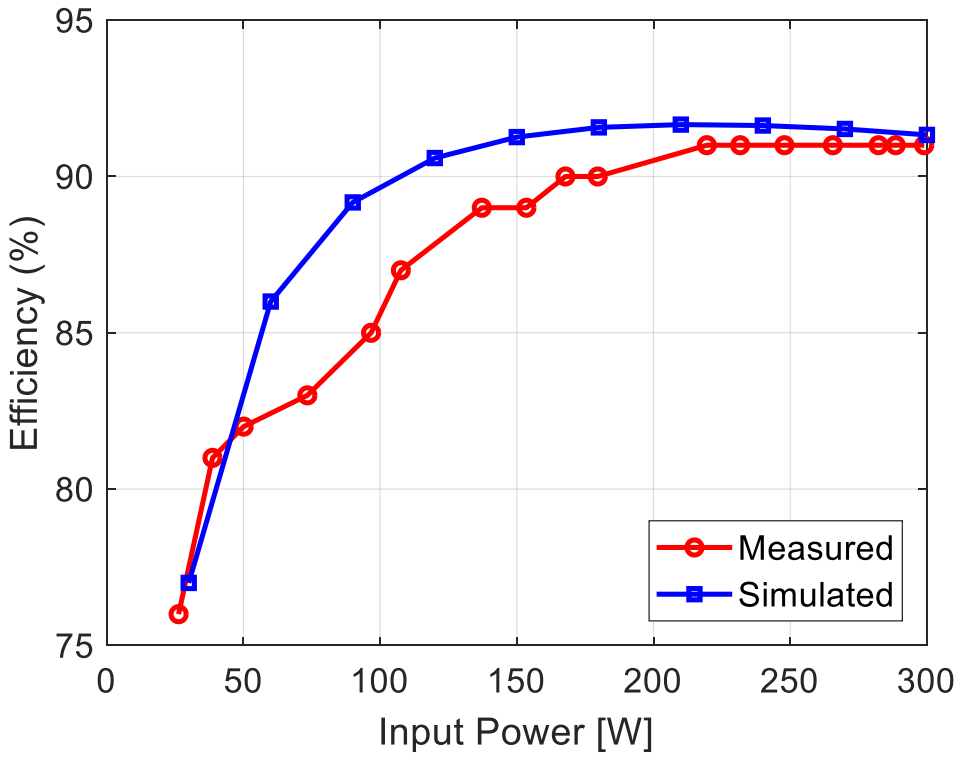


Figure 23: Frequency and current (LV to HV power flow)

A prototype of flow converter has been built and tested in both direction. The efficiency results are discussed in this section. In Figure 23, the simulated efficiency and measured efficiency of flow converters are compared. At high power, measured efficiency matches well with simulation results. For power range between 200W to 300W, efficiency is more than 90%. At the low input power efficiency is more than 75 percent. The drops in the efficiency can be attributed to core losses. For power flow between 50W to 150W, simulation efficiency and measured efficiency differs by 5%. This can be attributed to the effect of reverse recovery. The full impact of reverse recovery was not considered in the simulation. Due to the reverse recovery, peak current increase for same power level. It was observed during the testing that reverse diode of high voltage side has a very large reverse recovery time. When the frequency is higher, the effect of reverse recovery becomes more severe.

3.8.2. Charge Converter Efficiency Measurement:

A prototype of the charge controller (100W) was also built using the same topology as flow converter. However, best topology choice for charge controller is buck-boost not the flyback as isolation is not a requirement. The charge controller is being built for prototyping purpose only. In Future, the transformer can be replaced by a inductor without changing the control. In Figure 24, measured efficiency and the simulated efficiency of the charge controller have been compared. The charge converter shows excellent efficiency across the power level. Maximum efficiency is around 93 percent, and efficiency at low power is about 85% which is quite good. The efficiency will increase further if the transformer is replaced by an inductor for charge converter.

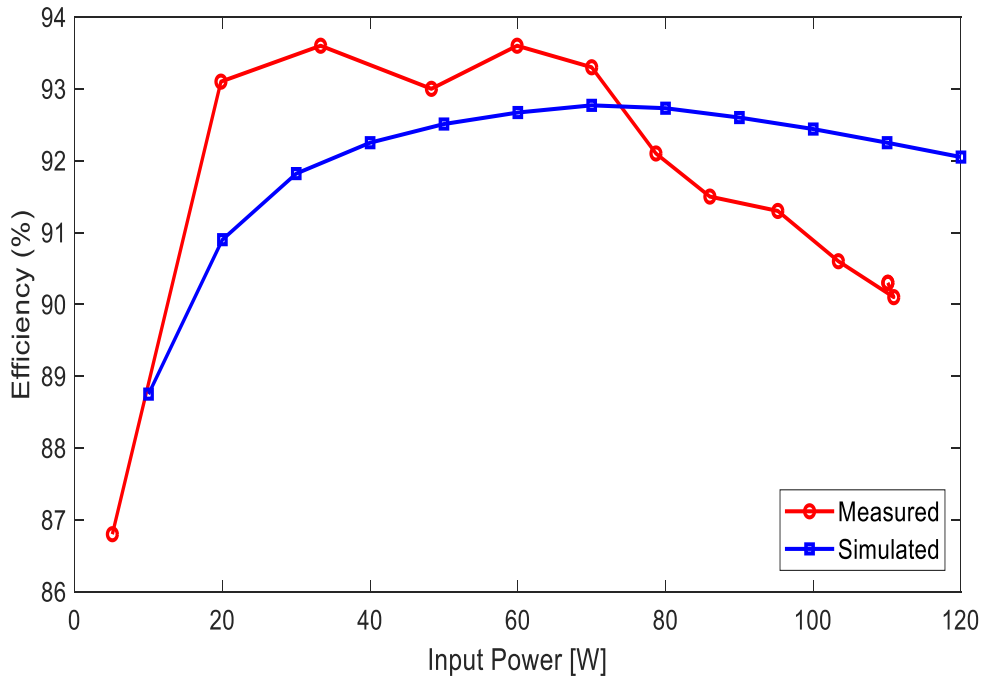


Figure 24: Charge Converter Efficiency Vs Input Data

4.
Converter Level Control

4.1. Converter Level Control Requirements:

Flow converter control can be divided into two categories: (1) Converter Level (2) System Level. In this chapter, converter level control will be discussed. System-level control will be addressed in chapter 5. The converter level requirements are the following:

1. The converter control must ensure the stable operation of the flow converter in both directions. The closed loop must be stable.
2. The converter control must enable the flow converter to transmit power in a complete range in both direction
3. The control must allow the flow converter to transmit power for a wide range of input voltage and output voltage.
4. The control must be able to provide over-voltage and over-power protection.
5. The control must be able to start the converter in a soft start mode.
6. The flow controller must have fast active control to limit the voltage deviation.
7. Simple Control: Flyback must have simple control to reduce the cost and the complexity of the design.

4.2. The Controller Description:

To implement all the listed requirements in section 4.1 NXP's TEA1753T [10,11] controller is selected. It is a sixteen-pin DCM/QR flyback controller with PFC. One control IC is needed for controlling the power in one direction. Therefore, the flow converter has two controller's ICs. Out of sixteen pins, eight pins have been used to implement the control for bi-direction flyback. Each pin with their functions, calculations, and circuits are explained in this section. The controller calculation is the same in both directions for almost all pins and features. Therefore, the calculation for one direction will be shown. If some functionality is only applicable in one direction or there is some difference in implementation, it will be explicitly mentioned.

1.) ***VCC:*** This is the supply pin of the controller, and the voltage on this pin is supplied by auxiliary winding. VCC is connected to the auxiliary winding through a diode as shown in Figure 25. The turns ration of the auxiliary winding must be chosen such that voltage on the VCC pin always remain in the range of 22 to 38V.

$$22 < VCC < 38 \quad (59)$$

The VCC voltage can be written as a function of turn ratio of the secondary winding and the auxiliary winding.

$$22 < \frac{N_{Aux}}{N_{Outp}} V_{out} < 38 \tag{60}$$

Eq. (60) must satisfy complete voltage range. That results in

$$N_{Out} \frac{22}{V_{out,min}} < N_{Aux} < N_{Out} \frac{38}{V_{out,max}} \tag{61}$$

The values for auxiliary winding for each controller have been tabulated in Table VI.

Table VI: Auxiliary Winding Calculation

Converter Type	Power Flow Direction	$V_{out,min}$	$V_{out,max}$	N_{Outp}	N_{Aux}
Flow Converter	LV to HV	330	430	48	4
Flow Converter	HV to LV	40	55	6	4

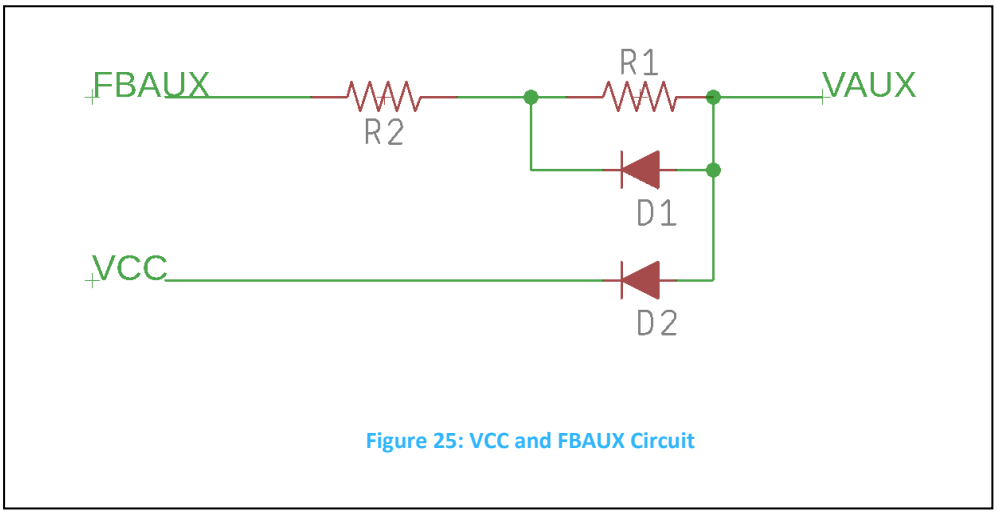


Figure 25: VCC and FBAUX Circuit

2.) ***GND:*** This is the ground pin of the controller.

3.) ***FBAUX:*** This pin is an input pin, and it has three main functions: demagnetization detection of the transformer, overvoltage detection (OVP) and overpower detection (OPP).

OVP and OPP Protection (Requirement 4):

The overvoltage detection and overpower detection is performed by sensing the current flowing from the auxiliary winding to FBAUX pin. The circuit for OVP and OPP voltage detection is shown in Figure 25. The resistor R1 and R2 determine the value of OVP and OPP. During the turn-off period, the voltage at the auxiliary winding is positive. Therefore current flows from auxiliary winding to FBAUX pin. If the current is found to

higher than 300uA, overvoltage at the output is assumed. The value of resistor R2 can be calculated using eq. (63)

$$I_{Aux} = 300uA = \frac{V_{Aux} - V_{clamp,FBAUX} - V_{f,D1}}{R2} \quad (62)$$

$$R2 = \frac{\left(\frac{N_{Aux}}{N_{OUT}} V_{OVP}\right) - V_{clamp,FBAUX} - V_{f,D1}}{300uA} \quad (63)$$

During the turn-on period, the voltage at the auxiliary pin is negative. Therefore, the current direction is from FBAUX pin to auxiliary winding. If current becomes higher than 100uA, overpower protection gets activated. Value of R1 can be calculated using eq. (65).

$$I_{Aux} = 100uA = \frac{V_{Aux} - V_{clamp,FBAUX}}{R2 + R1} \quad (64)$$

$$R1 = \frac{\left(\frac{N_{Aux}}{N_{IN}} V_{OPP}\right) - V_{clamp,FBAUX}}{100uA} - R2 \quad (65)$$

Table VII: OVP and OPP Resistance Calculation

Converter Type	Power Flow Direction	$V_{in,max}$(V)	$V_{out,max}(V)$	$R_1(k\Omega)$	$R_2(k\Omega)$
Flow Converter	LV to HV	60	430	120	280
Flow Converter	HV to LV	430	60	120	280

T values of R1 and R2, OVP and OPP voltage levels are tabulated in Table VII.

4.) ***VINSENSE:*** For this project, VINSENSE pin is used as a control to enable and disable the converter. When the voltage at this pin is more than the threshold voltage, the controller starts the converter.

5.) ***FBSENSE:*** This pin senses the current flowing at the primary side by sensing the voltage across the sense resistor. The voltage on this pin $V_{FBSENSE}$ is compared to $V_{Sense(fb)}$ voltage. When $V_{FBSENSE}$ reaches to $V_{Sense(fb)}$ level, MOSFET is switched off. $V_{Sense(fb)}$ is a function of the voltage on the FBCTRL pin V_{FBCTRL}. Therefore, the peak current at the primary is controlled by V_{FBCTRL} voltage. The relationship

between $V_{sense(fb)}$, V_{FBCTRL} and I_{peak} are given by eq. (66) and eq. (67) and eq.(68).

$$V_{Sense(fb)} = \begin{cases} 0.3 & V_{FBCTRL} < 1.5 \\ 0.66V_{FBCTRL} - 0.69 & 1.5 \leq V_{FBCTRL} \leq 2 \\ 0.63 & V_{FBCTRL} > 2 \end{cases} \quad (66)$$

$$I_{\text{peak}} = \frac{V_{Sense(fb)} - I_{adj(FBSENSE)} * (R3 + R4)}{R_{Sense}} \quad (67)$$

Here, $I_{adj(FBSENSE)}$ is a source current of 3uA from FBSENSE pin. The Recommended circuit for FBSENSE pin is shown in the Figure 26. The following function are performed using this circuit.

I. Soft Start of the converter.
II. Filtering out high-frequency disturbance to ensure MOSFET is switched off at the right time.
III. Adjustment of $I_{peak,min}$ and $I_{peak,max}$

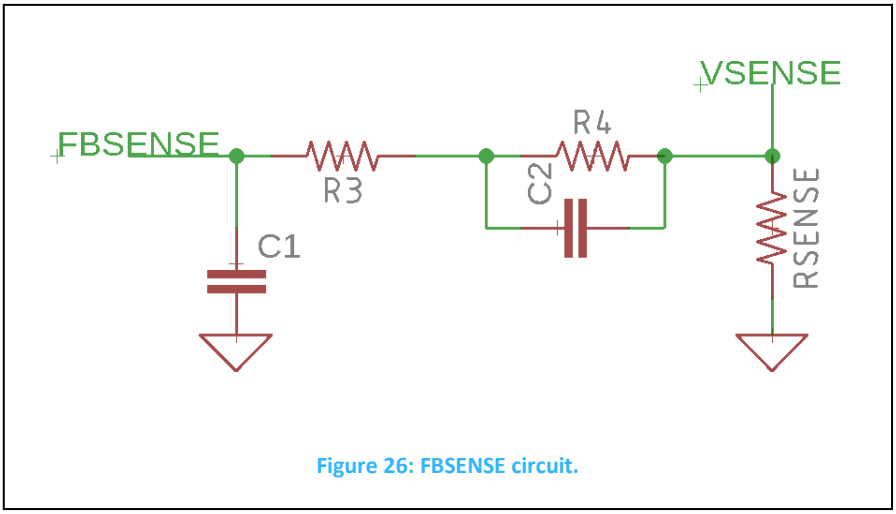


Figure 26: FBSENSE circuit.

Soft Start of the Converter (Requirement 5):

Soft start is one of the converter requirement listed in section 4.1. When the converter starts, the voltage on the output capacitor might be zero or very low depending on the state of the MG. If maximum power is transferred when the output voltage is low, it can result in very high inrush current and overshoot voltage. Therefore, a soft start feature must be implemented. Before starting the converter, the capacitor C2 is charged to 0.63V. After the C2 is charged to 0.63V, the controller begins the converter in soft start mode; the voltage on the capacitor C2 limits the peak current. As the capacitor C2 discharged by resistor R4, the peak current increase. During the soft start period, the primary peak current can be approximated using eq. (68)

$$I_{Peak} = \frac{0.63V - 0.63e^{-\frac{t}{R4*C2}}}{R_{Sense}} \quad (68)$$

FBSESNE pin Filter Design:

Due to the switching phenomenon and the leakage inductance, voltage disturbance appears across R_{Sense} resistor. These high-voltage disturbances, if propagated at FBSENSE, will activate the ESD protection. Therefore, a low-pass filter is designed to filter out high-frequency noises. The cut-off frequency is selected such that it filters-out high-frequency disturbances while not delaying the ramping voltage signal. The value of resistor R4 and capacitor C2 is much higher compared to R3 and C1. Therefore, the effect of R4 and C2 can be eliminated from the filter design. While designing the filter, MOSFET turn-off delay and internal delay of IC should also be taken into account. The maximum time constant can be calculated using eq. (69).

$$R3 * C1(ns) < \frac{\frac{I_{Peak,min} * L_P}{390 * 1e-9} - t_{int,delay} - t_{MOSFET,off}}{5.5} \quad (69)$$

$$R3 * C1(ns) < 220ns$$

C1 of 100pF and R3 of 1.5kohm is used in the design.

$I_{peak,min}$ and $I_{peak,max}$ Current Adjustment:

The maximum power in the flyback converter depends on the maximum current in the QR mode (explained in section 4.3). The maximum peak current level $I_{Peak,max}$ can be set by calculating the value of R_{Sense} using eq. (71). For low power level, controller enters in Frequency Reduction (FR) mode. In this mode, the frequency is decreased to reduce the power while keeping peak current constant $I_{peak,min}$. The current $I_{peak,min}$ can be adjusted by changing the value of series resistance R3 and R4 in Figure 26.

The value of R_{Sense} and series resistance R_{Series} (R3+R4) can be calculated using eq. (70) and (71)

$$R_{Sense} = \frac{V_{Sense(fb)max} - V_{Sense(fb)min}}{I_{Peak,max} - I_{Peak,min}} \quad (70)$$

$$R3 + R4 + R_{Sense} = \frac{0.3 * I_{Peak,max} - 0.63 * I_{Peak,min}}{I_{adj,FBSENSE} * (I_{Peak,max} - I_{Peak,\min})} \quad (71)$$

Here, current $I_{adj,FBSENSE}$ (3uA) flows through resistor R3 and R4 and create the voltage offset at pin FBSENSE. The value of R4 is usually much higher compared to R3 and R_{Sense}, therefore, R4 and R_{Sense} can be eliminated from eq. (70).

$$R3 \approx \frac{0.3 * I_{Peak,max} - 0.63 * I_{Peak,min}}{I_{adj,FBSENSE} * (I_{Peak,max} - I_{Peak,\min})} \quad (72)$$

6.) ***FBDRIVER:*** Gate driver for the MOSFET.
7.) ***HV:*** Valley sensing of the flyback.
8.) ***FBCTRL:*** Control input for flyback for direct connection of the optocoupler. The optocoupler connection at FBCTRL completes the closed loop. At a control voltage of 2V or more than 2V, the flyback delivers the maximum power. At 1.3V, flyback stop switching.

4.3. Mode of operation

The controller enables the flyback to operate in following three operating modes [10,11].

- Quasi-Resonant (QR) Mode,
- Discontinuous Conduction Mode (DCM) with valley switching
- Frequency Reduction (FR) Mode

These modes are selected by controlling the voltage on FBCTRL pin of the controller.

4.3.1. Quasi-Resonant (QR) Mode:

The Quasi-resonant mode is another name for BCM-VS. This mode is used to deliver the high and maximum power. In genuine BCM without the valley switching, the power is directly proportional to the primary inductor peak current and inversely proportional to the frequency. In BCM-VS, due to the extra resonance period, this relationship does not hold completely. However, as the resonance period is quite small compare to the time-period of flyback, the error is small and often neglected to assume a linear relationship between peak current and the power. The input power is related to peak current via the following eq. (73)

$$P = \frac{1}{2} I_{peak} \left(\frac{V_{d2} + N V_{d1} \left(1 - \frac{T_{RES}}{T}\right)}{V_{d2} + N V_{d1}} \right) \quad (73)$$

If the impact of the valley is neglected, eq. (73) can be modified to yield a linear relationship between input power and peak current,

$$P = K_{QR} I_{peak} \quad (74)$$

Here, $\mathbf{K_{QR}}$ is the coefficient of proportionality in QR mode.

The output power can also be written as,

$$P = \frac{1}{2} L {I_{peak}}^2 f \quad (75)$$

The operating frequency is calculated by equating eq. (75) and eq. (76)

$$f = \frac{1}{I_{peak}}\left(\frac{V_{d2} + NV_{d1}\left(1 - \frac{T_{RES}}{T}\right)}{L_P(V_{d2} + NV_{d1})}\right) \quad (76)$$

In this mode, output power is controlled by controlling the peak current through the primary inductor. During this mode, the voltage on the FBCTRL pin is more than 1.5. If V_{FBCTRL} is greater than two volts, maximum power is delivered. If V_{FBCTRL} is between voltage 1.5 and 2, and frequency is less than 125KHz , power and the frequency relate to the current via eq. (74) and eq. (76). As operating frequency increases with decreasing power in QR mode, frequency may increase to 125KHz before FBCTRL reaches to 1.5. In that case, flyback enters in DCM-VS mode. In Figure 27, the QR mode waveforms for flow converter is shown when transferring power from low voltage side to high voltage side.

Figure 27: QR Mode Waveforms

Here, Channel 1: Gate signal, Channel 2: Drain-source voltage, Channel 3: Diode voltage and Channel 4: Sense resistor voltage

4.3.2. Discontinuous Conduction Mode with valley switching (DCM-VS)

While operating in the Quasi-resonant mode, the frequency increases if the output power is decreased. The controller limits the frequency to f_{max} in order to limit frequency dependent losses. In our case, f_{max} is 125KHz. The controller uses a mechanism based on the timer to achieve this. In contrast to QR mode, the switch is not closed as soon as first valley is detected, the controller waits for timer to expire before turning on the switch at the next valley as shown in Figure 28. The frequency can deviate little bit from f_{max} depending on arrival of first valley after timer expires. However, the deviation is very small, and the operating frequency is never greater than f_{max}. During DCM-VS mode, V_{FBCTRL} is between 1.5V and 2V. If converter is designed in such a way

that, V_{FBCTRL} decreases to 1.5V before operating frequency reaches to 125KHz, DCM-VS mode is skipped.

Figure 28: DCM-VS Mode Waveforms

In DCM-VS, power is proportional to the square of the peak current.

$$P = K_{DCM-VS} * {I_{LP,peak}}^2 \quad (77)$$

Here, K_{DCM-VS} is coefficient of proportionality in DCM-VS mode.

4.3.3. Frequency Reduction (FR) Mode:

The FR mode is used to deliver the low amount of power. As V_{FBCTRL} reaches below 1.5V, FR mode is activated by the controller. Like DCM-VS, the MOSFET is turned on at the nth (n>1) valley of the voltage. However, unlike the DCM_VS, the frequency is not constant in FR mode. Current is kept constant, and frequency is decreased to reduce the power. At very low power, duty cycle becomes very low as shown in Figure 29. The linear relation between the power and the frequency is given by eq. (78).

$$P = K_{FR} * f \quad (78)$$

Here, K_{FR} is coefficient of proportionality in QR mode.

Figure 29: FR Mode Waveforms

4.4. Current Control of the Flyback Converter:

The flyback controller operates in three operating modes as explained in section 4.3. In this section, closed-loop current control scheme for all three modes are discussed. The current control scheme for Flyback BCM-VS is shown in Figure 30. The output voltage is compared to the reference voltage using an error amplifier to generate the error voltage. In typical flyback control, the error amplifier contains an integrator that results in zero steady state error. The output of the error amplifier is compared to the voltage at the sense resistor to determine the turn-off moment. The turn-on is determined by sensing the voltage at the auxiliary winding. Two conditions are checked: demagnetization of the inductor and the valley detection. As soon as diode stop conducting, the voltage across auxiliary winding becomes positive; that means demagnetization of the inductor is complete. However, this is not the optimum moment to turn on the switch as the voltage across drain and source of the MOSFET is still $V_{IN} + nV_{INOUT}$. Just after diode stop conducting, the resonance between primary inductor and the parasitic capacitance of the MOSFET starts. The MOSFET is switched on at the valley of the drain voltage determined by measuring dV/dt of the auxiliary voltage. In some controller, like one used in this project, there is one dedicated pin (HV) in the controller to just detect the valley.

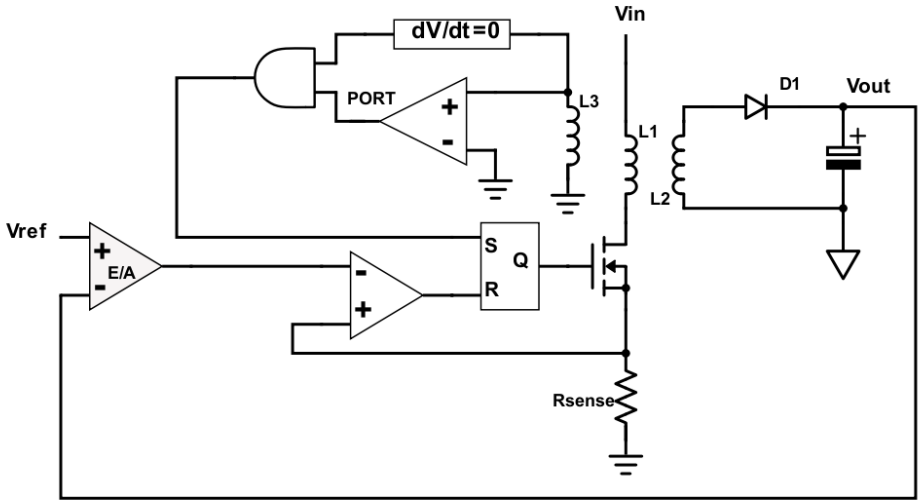


Figure 30: Flyback BCM-VS Controller

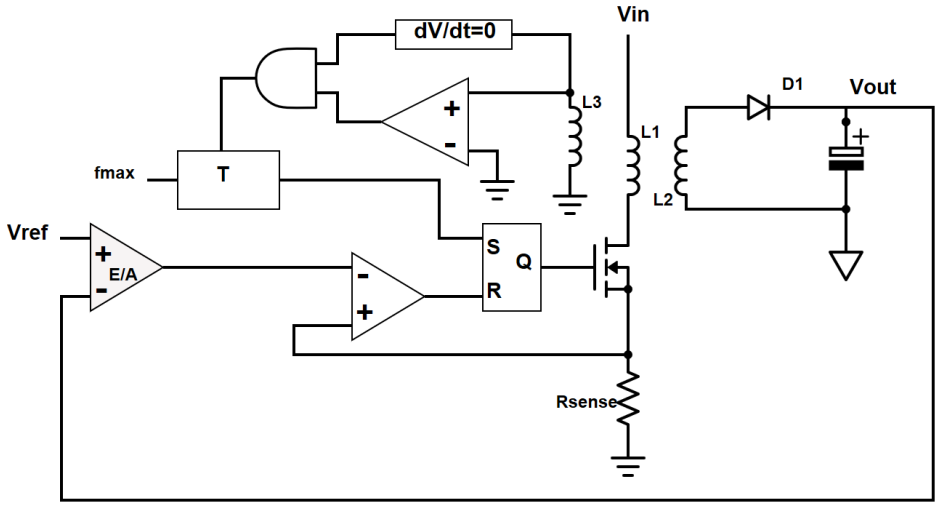


Figure 31: Flyback DCM-VS Controller

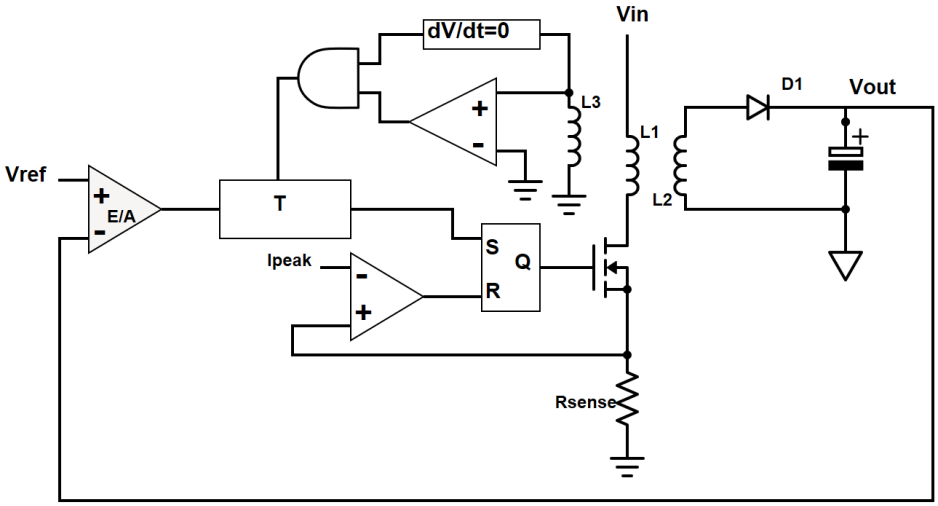


Figure 32: Flyback FR Mode Controller

Figure 32 shows the current control in FR mode. Unlike, BCM-VS and DCM-VS, the peak current remains constant. The output of the error amplifier is used to control the frequency. During this mode, turn on time of the MOSFET remains constant for specific input voltage. The turn-off time is changed to control the output power.

TEA1753 controller, the one used in the project, incorporate all three controllers. The combined control scheme is shown in Figure 33. The FBAUX, HV pins are used for demagnetization detection and valley detection respectively. The error amplifier is a combination of two parts: Inside the IC and outside the IC. Inside the IC, the voltage on FBCTRL is used to generate the voltage threshold $V_{Sense(fb)}$ which is then compared to the voltage on FBSENSE pin to determine turn-on time. The second part of the error amplifier is outside the IC which is designed according to the application, and it is the feedback element in the loop. This is being denoted by f in the Figure 33.

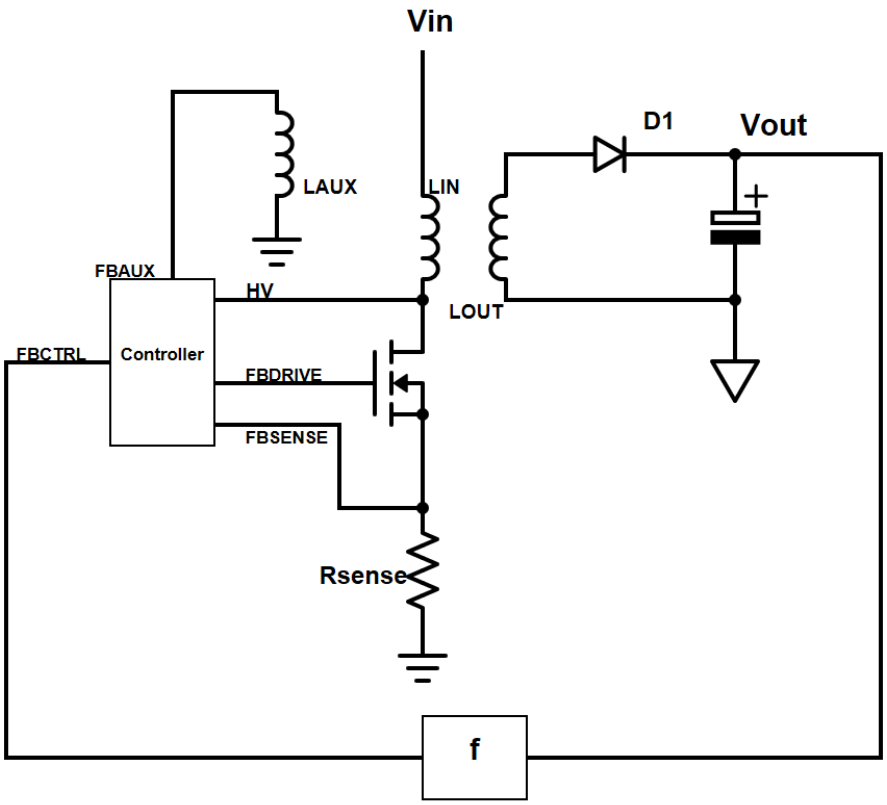


Figure 33: Flyback Control Scheme

4.5. Feedback Design:

Most of the textbooks show op-amp beings used in the error amplifier. However, in reality, TL431 is used to design the feedback loop. TL431 is a three-pin controllable voltage reference. 2.5V reference is generated at the ref pin. Using a voltage divider of two resistors, controllable voltage reference or error signal can be generated. In the SMPS application, TL431 is used to design a PI feedback loop as shown in Figure 34.

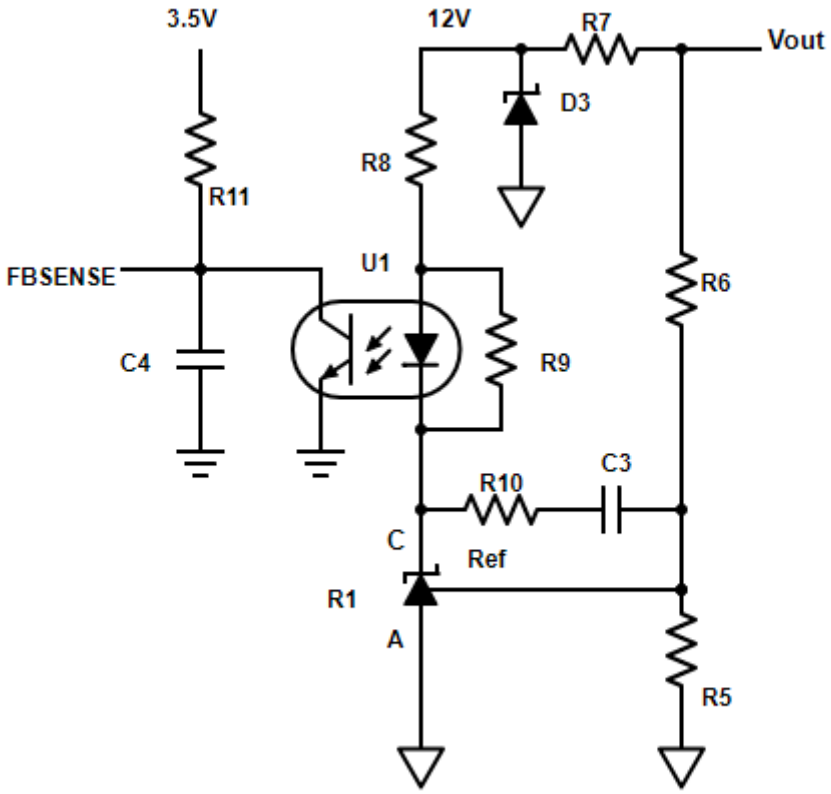


Figure 34: PI feedback circuit

Steady State Analysis:

If the circuit is properly biased, then the voltage reference of 2.5V is being generated by the voltage regulator. Therefore, the current through the resistor is constant and given by eq. (79)

$$I_{R5} = \frac{V_{Ref}}{R5} = \frac{2.5V}{R5} \tag{79}$$

The current through resistor R6:

$$I_{R6} = \frac{V_{out} - V_{Ref}}{R6} \tag{80}$$

In the steady state, the capacitor C3 becomes open. Therefore, the voltage at the output stabilizes to nominal voltage or steady-state voltage. The value of steady state voltage can be found by using the fact that at the steady state, the current through R5 and R6 are equal.

$$V_{out,final} = V_{Ref}\left(1 + \frac{R6}{R5}\right) \tag{81}$$

In the steady state, the voltage at the FBSENSE can be expressed as a function of cathode voltage.

$$V_{FBSENSE} = 3.5V - CTR * \left(\frac{12V - V_C}{R8} - \frac{V_{fd}}{R8} - \frac{V_{fd}}{R9}\right) * R11 \quad (82)$$

Here, CTR is the current transfer ratio of the optocoupler. Optocoupler is selected such that CTR is constant for complete operating range.

Closed loop system stability is listed as a requirement in section 4.1. To meet this requirement, PI feedback is designed. Integrated error ensures that steady state voltage error is always zero. The proportional error makes the system response faster. If the current through R5 and R6 are not equal, the voltage across capacitor C3 will change resulting in a voltage change at FBSENSE pin, hence a change in input power. If the output voltage is greater than the steady state voltage, the current in resistor R5 will be smaller than the current in R6, the voltage at the cathode will increase, the voltage at FBSENSE will decrease. Therefore, less input power will be delivered resulting in voltage decline at the output. Similarly, if the output voltage is smaller than steady-state voltage or nominal voltage, the voltage $V_{FBSENSE}$ will increase resulting in more input power. With current control implementation, Flyback in BCM-VS is characteristically stable.

Small Signal Analysis:

To understand the impact of the voltage disturbance and the load shedding, small signal frequency analysis is presented here. The transfer function G1 and G2 are defined as,

$$G1(s) = \frac{V_C}{V_{out}} = -\frac{\left(\frac{1}{sC3} + R10\right)}{R6} \quad (83)$$

$$G1(s) = -\frac{1 + sC3 * R10}{sC3 * R6} \quad (84)$$

$$G2\ (s) = \frac{V_{FBSENSE}}{V_C} = CTR * \frac{(R11||C4)}{R8} \quad (85)$$

The transfer function G3 can be obtained by multiplying eq. (84) and eq. (85).

$$G3\ (s) = \frac{V_{FBSENSE}}{V_{out}} = -CTR * \frac{R11}{(1 + sR11 * C4) * R8} * \frac{1 + sC3 * R10}{sC3 * R6} \quad (86)$$

From eq. (86) zero frequency and the pole frequency can be calculated using eq. (87), eq. (88).

$$f_z = \frac{1}{2 * \pi * C3 * R10} \quad (87)$$

$$f_{pole} = \frac{1}{2 * \pi * C4 * R11} \quad (88)$$

A capacitor of 10nf is placed at the FBSENSE pin, and R11 is an internal 3K resistance of the IC. From this pole frequency of 5.3KHz is obtained. For 50^o phase margin zero should be placed on 720Hz. To achieve the zero at 720Hz, C3=10nF and R10=22KΩ is used.

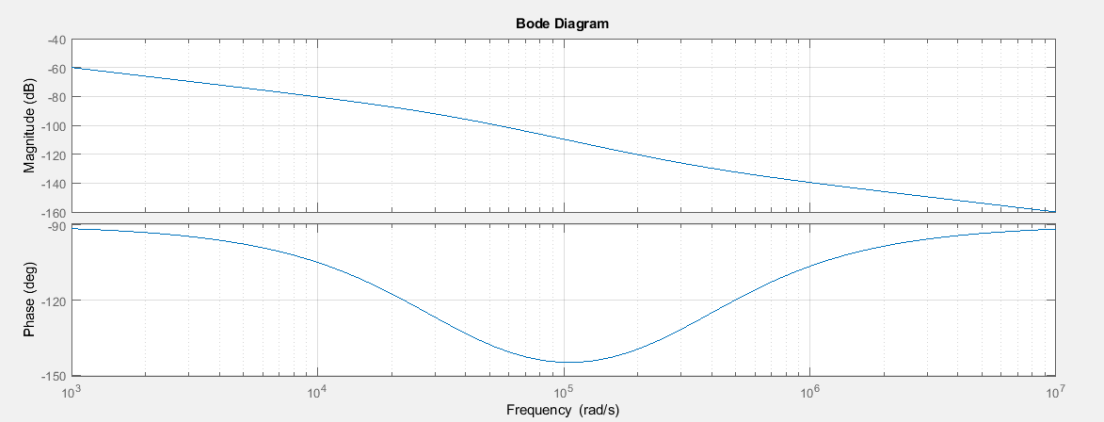


Figure 35: Bode Plot

5. System Level Control

5.1. Coordinated control

The control is an important part of the decentralized architecture shown in Figure 3. It is important to understand the top-level coordinated control goals of MG before deriving the control for the converters in the MG. Main control goals of coordinated control is being listed here:

1.) Maximum utilization of PV power.
2.) Power flow control between PV and battery unit in a single SHS unit. This power flow ensures that excess power from PV is stored in the battery and used later.
3.) Load sharing among all SHS unit must be achieved using the droop mechanism. SHS is connected to high voltage bus through flow converter. The flow controller of SHS not only see the load of that SHS, a combined load which is the sum of all individual loads at the high voltage bus is to be seen by all the flow controller. Hence, the load power must be shared among all flow converters with good voltage regulation. As an additional function, a way to vary droop coefficient and droop offset must be realized
4.) The coordinated control must be able to transfer the power among its components namely charge converter, battery, flow converter, PV and HV loads and low voltage in a reliable manner.
5.) Voltage regulation at the low voltage bus and high voltage bus.

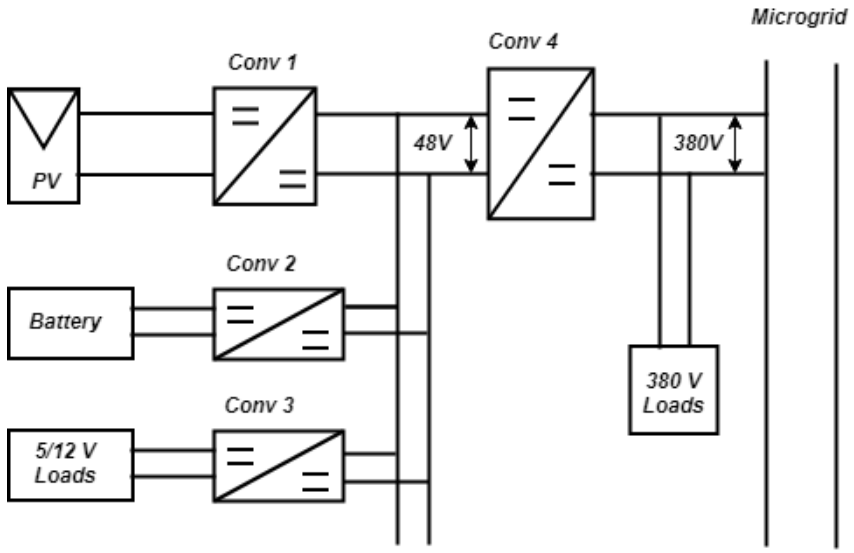


Figure 36: SHS Architecture

5.2. Operating mode analysis of SHS:

The SHS works in the different operating state depending on the state of batteries, PV units and the load connected at low voltage and high voltage bus. For each mode, the converters in the SHS operate in different modes. In this section, operating mode analysis of SHS is presented, and most important states are analyzed. The resulting coordinated control scheme is decided based on the goals listed in section 5.1.

State 1: Available PV power of an individual SHS is greater than the sum of charging limit, low voltage (5/12 volts) loads and required power sharing of flow converter according to the default droop equation.

$$P_{PV\_MPPi} > P_{LV\_loadi} + P_{Ch\_limi} + P_{HV\_load} * \beta_i \quad (89)$$

Here, P_{PV_MPPi} is the maximum power that can be generated from the PV of unit i at a given time. $P_{Ch_{limi}}$ is the charging limit of the charge converter of unit i. P_{LV_loadi} is the load connected to the low voltage bus of unit i. P_{HV_loads} is the total load present at the common high voltage bus. β_i is power sharing coefficient of flow converter, and β_i is determined by the droop factor. If droop constant is the same for all the flow converter in the MG, each flow converter will transfer the same power.

In the SHS, PV power is used to meet the load demand, in this architecture, low voltage load and high voltage load. Once the load demand is fulfilled, excess power is stored in the battery ensuring the maximum utilization of PV power. However, if at a given time, the excess PV power is higher than the battery charge limit as in this state, PV must be operated below MPP level to ensure the power balancing as in eq. (88). As PV is converter is providing power to all other converters, it takes the role of grid forming and works in constant voltage mode.

$$P_{PV\_i} = P_{LV\_load} + P_{Ch\_limi} + P_{HV\_loads} * \beta_i \quad (90)$$

$$P_{PV} < P_{PV\_MPPi} \quad (91)$$

State 2: Available PV power in SHS is higher than low voltage loads but smaller than the sum of low voltage loads, charging limits of the battery and the required power sharing.

$$P_{PV\_MPPi} < P_{LV\_loadi} + P_{Ch\_limi} + P_{HV\_load} * \beta_i \quad (92)$$

$$P_{PV_{MPPi}} > P_{LV_{loadi}} \quad (93)$$

Here, two options are available: either power-sharing coefficient β_i is decreased to reduce the power flow from LV to HV or battery charging is reduced, and if the required battery provides the power to the flow converter to meet high voltage load. In the SHS, power flow from LV to HV must get priority on battery charging as the primary goal of the coordinated system is to meet the demand, not the battery charging, the battery

should only be charged if excess power is available. The power balancing equation for state 2 are given in eq.(94) and eq.(95)

$$P_{PV\_MPPi} = P_{LV\_loadi} + P_{Ch} + P_{HV\_load} * \beta_i \quad (94)$$

$$P_{Ch} < P_{Ch\_limi} \quad (95)$$

State 3: The sum of available PV power and battery discharge limit is smaller than the sum of low voltage load and required power sharing of flow converter, but higher than low voltage load alone.

$$P_{PV\_MPPi} + P_{Dch\_limi} < P_{LV\_loadi} + P_{HV\_load} * \beta_i \quad (96)$$

$$P_{PV\_MPPi} + P_{Dch\_limi} > P_{LV\_loadi} \quad (97)$$

This means that generation in SHS does not have enough power to meet power demand. Because the demand is greater than the supply, the HV load must be decreased to meet the demand. This can be done by implementing a power droop with the input voltage. Due to the gap in the demand and supply, the voltage at low voltage bus decreases, The flow converter senses the voltage drop at the low voltage side and reduces the power by decreasing the power-sharing coefficient.

$$P_{PV\_MPPi} + P_{Dch\_limi} = P_{LV\_loadi} + P_{HV\_load} * \beta_{i,new} \quad (98)$$

$$\beta_{i,new} < \beta_i \quad (99)$$

State 4: The low voltage load is greater than the sum of PV power available, battery discharge limit.

$$P_{LV\_loadi} > P_{PV\_MPPi} + P_{Dch\_limi} \quad (100)$$

In state 4, the total supply of the SHS is lesser than low voltage loads. To meet the demand, flow controller will supply the power to low voltage side from high voltage side. The power flow direction change must be automatic. As explained in the state 3, power flow from LV to HV decreases if LV voltage decrease. At one point, power flow will become zero. After this, the flow converter will change the direction of power flow. Power flow from HV to LV can be expressed with a negative power-sharing coefficient as in eq. (101)

$$P_{LV\_loadi} = P_{PV\_MPPi} + P_{Dch\_limi} - \beta_{i,neg} P_{HV_{loads}} \quad (101)$$

State 5: If the sum of low voltage loads and high voltage loads in the MG is greater than the sum of total PV power and total discharging limits of the batteries.

Load shedding must be performed at the HV to balance the demand and supply.

5.3. Proposed Control Strategy:

Based on the operating state analysis of SHS in section 5.3, the control strategy for each converter is proposed in this section.

5.3.1. PV Converter:

In Figure 37, the control law for the solar converter has been depicted. During the state 1 of the SHS, available PV power in the SHS is greater than the sum of charging limit, low voltage load and required power-sharing from LV to HV, PV converter takes the role of grid forming at low voltage bus. For rest of the states, PV converter operates at MPP.

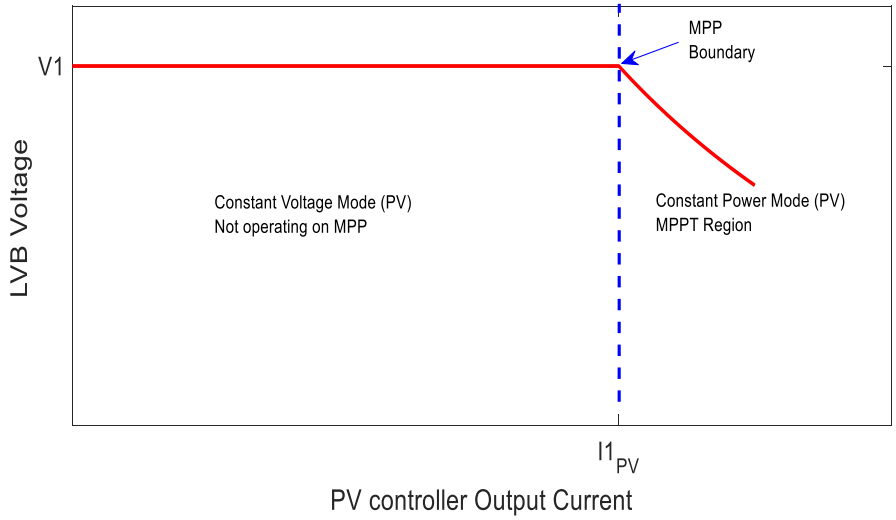


Figure 37: Control Law for PV Converter

5.3.2. Charge Converter:

In Figure 38, the control law for charge converter has been shown. If SHS is operating in state 1, there is enough excess power to charge the battery at charge limit power. If PV converter is not able to supply the sum of load demand and maximum charging power, the SHS enters in state 2, and the voltage at LVB decreases. The charge controller senses this voltage drop and reduces the charging power till equilibrium is reched. The charging power can be decreased by implementing the droop as shown in Figure 38. Between the voltage V2 and V3, charging power decreases from maximum to zero. If the voltage at LVB further decreases, charge converter changes the direction of power flow and start transferring the power to low voltage bus. When discharging, charge converter operates in constant voltage mode and keep the voltage at LVB constant. Charging limit and the

discharging limit can be set by the controller bases of State of Charge (SoS) measurement. Once the charge converter has reached to discharging limit, SHS enters in state 3. In state 3, charge converter operates in constant current mode or constant power mode. Power equilibrium is achieved by reducing the input power for the flow converter.

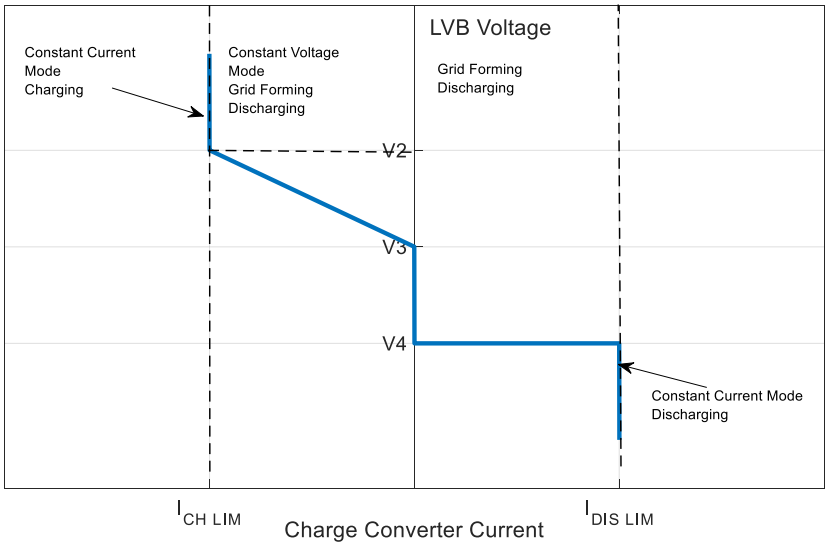
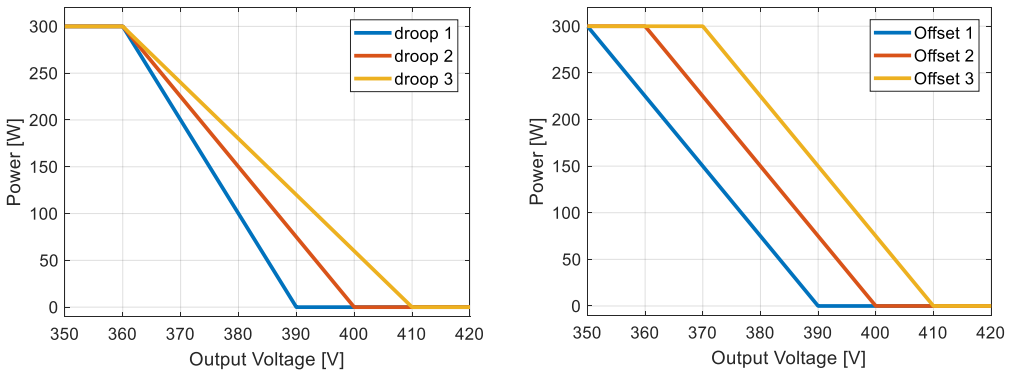


Figure 38: Charge Converter Control Law

5.3.3. Flow Converter:

The flow converter is responsible for controlling the power flow in both directions, and the control requirements are different in both directions. When transferring power from LV to HV, flow converter must share the HV load with other flow converters. This can be achieved by implementing the power droop with the output voltage (HV). Examples of ideal output droop are shown in Figure 39. The input power decreases with the output voltage linearly between the zero and the maximum power. In Figure 39 (a), three droop curves with different slopes are shown. If flow converters with different droops are connected in the parallel, converter with maximum droop slope with share less load. In Figure 39 (b), three droop curves with different offset are shown. The offset of the droop determines the output voltage points at which converter transfer maximum and zero power.



(a) (b)

Figure 39: Output voltage – Input power droop (a) with different droop factor (b) with different voltage offset.

In Figure 40, the control law for flow converter with respect to LV voltage is shown. If the voltage on the LV is greater than V5, the SHS operates in either state 1 or state 2. During these two states, power flow is determined by the droop coefficient and the HV voltage, the voltage on LV bus is higher than V5 and does not have any bearing on power flow. Once the voltage on LV bus drops below V6, SHS enters in the state 3. During the state 3, the power droop with input voltage also becomes active. As the voltage on the LV bus decreases, the power flow from LV to HV also decreases. In state 3, the power flow is a function of both input (LV) and output voltages. For a fixed HV voltage, input power and LV voltage follow a linear relationship, and for a fixed LV voltage, the relationship between input power and HV voltage is linear. At V6 voltage, power drop to zero. The converter changes the direction of power flow at V7 and enters in grid forming mode to keep the voltage constant at LV bus while transferring the power to low voltage loads.

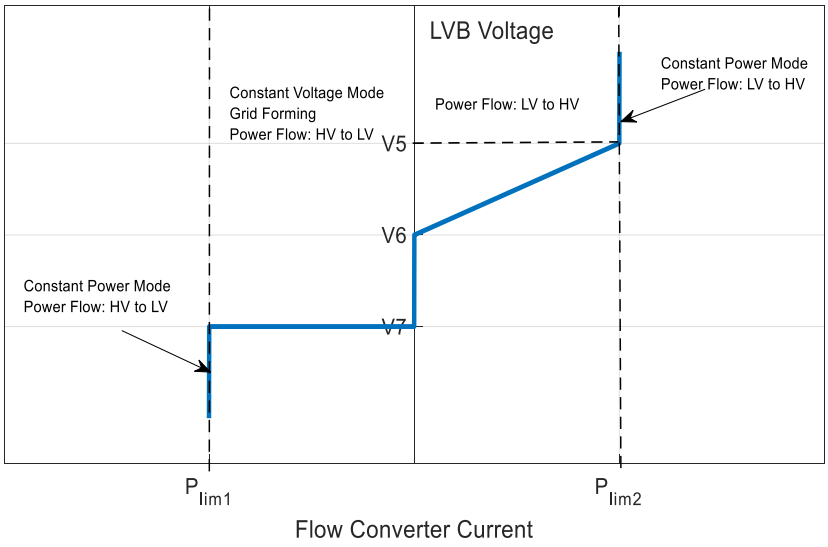


Figure 40: Flow converter Control Law

5.4. Droop Implementation:

Load sharing with other flow converters is a significant requirement for the flow converter, and this is achieved by implementing the power droop with the output voltage. As discussed in chapter 4 that the current control is implemented such that output voltage is constant in steady state for all the power levels. For this purpose, a PI controller was implemented in the feedback loop. To implement the droop the PI control is being replaced by the proportional control as shown in Figure 41. The cathode voltage V_C and voltage $V_{FBSENSE}$ can be calculated using eq. (102) and eq. (103).

$$V_C = 2.5V * \left(1 + \frac{R10}{R5}\right) - V_{out} * \left(\frac{R10}{R6}\right) \quad (102)$$

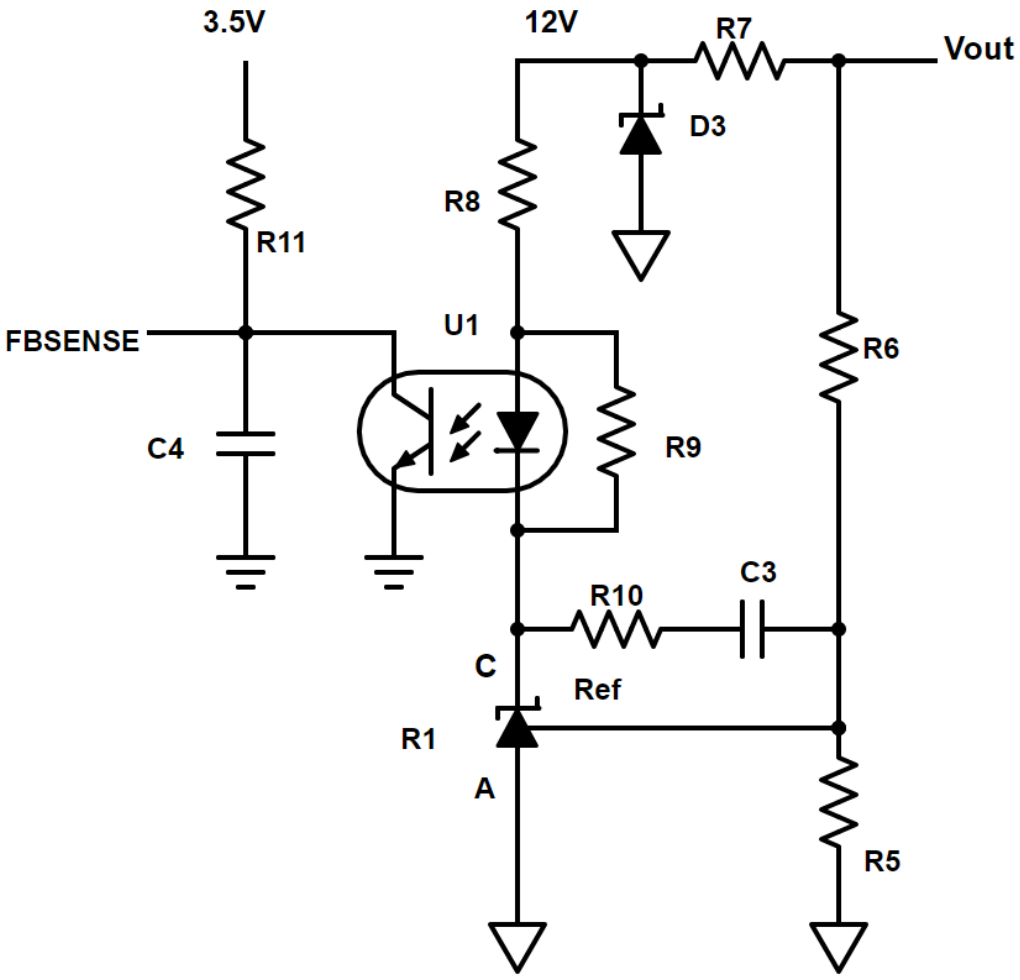


Figure 41: Linear feedback

$$V_{FBCTRL} = 3.5V - CTR * \left(\frac{12V - V_C}{R8} - \frac{V_{fd}}{R8} - \frac{V_{fd}}{R9}\right) * R11 \quad (103)$$

Eliminating the cathode voltage from eq. (103) using eq. (102) results in,

$$V_{FBCTRL} = 3.5V - CTR\left(\frac{12V}{R8} - \frac{2.5V}{R8}\left(1 + \frac{R10}{R5}\right) - \frac{V_{fd}}{R8} - \frac{V_{fd}}{R9} + \frac{R10}{R8 * R6}V_{out}\right)R11 \quad (104)$$

Eq. (104) can be rewritten as in,

$$V_{FBCTRL} = C + mV_{out} \quad (105)$$

Here, C is the droop offset and m is the droop slope.

$$C = 3.5V - CTR\left(\frac{12V}{R8} - \frac{2.5V}{R8}\left(1 + \frac{R10}{R5}\right) - \frac{V_{fd}}{R8} - \frac{V_{fd}}{R9}\right)R11 \quad (106)$$

$$m = -CTR * \frac{R11}{R8} * \frac{R10}{R6} \quad (107)$$

The resistor R6 only appears in the calculation of droop slope, not in the computation of droop offset. Similarly, The resistor R5 only appears in the calculation of droop offset, not in the calculation of droop slope. Therefore, the value of the slope can be changed by changing the resistor R6, and the droop offset can be changed by changing the value of resistor R5.

The slope of power droop with output voltage depends on the feedback slope and the slope between input power and V_{FBCTRL}. It must be noted that the relation between input power and V_{FBCTRL} voltage is not completely as shown in Figure 42 because the flyback operates in three different modes depending on $V_{FBSENSE}$ voltage, maximum frequency limit and minimum current limit set by the controller as discussed in section (). The input power in QR mode is proportional to input current. IN DCM-VS mode, input power is proportional to square of the peak current, therefore, proportional to square of control voltage. Therefore, it is important that converter operates in DCM_VS mode only for the small voltage range to linearize the slope. By selecting the proper inductor, the slope in the QR mode and voltage range in DCV_VS can be tuned. In FR mode, power is proportional to the operating frequency while peak current is constant. By changing the peak current, slope can be adjusted. In this project, the minimum peak current is set such that slopes in FR mode and QR mode are equal.

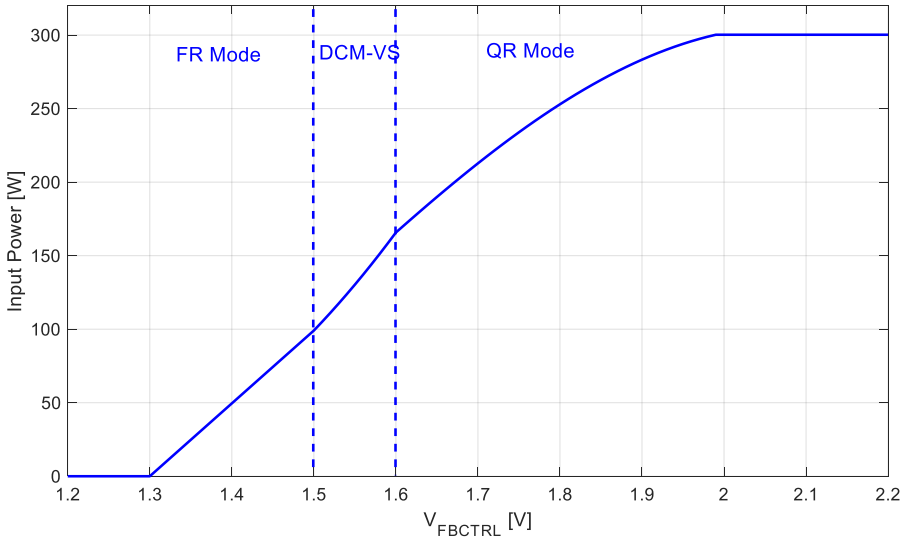


Figure 42: Input Power vs control voltage

Droop curves with different slope have been successfully measured for the flow converter. The slope of the droop was varied by changing resistor R6. These droop are shown in Figure 43. The droop curves mathes well with simulated curves.

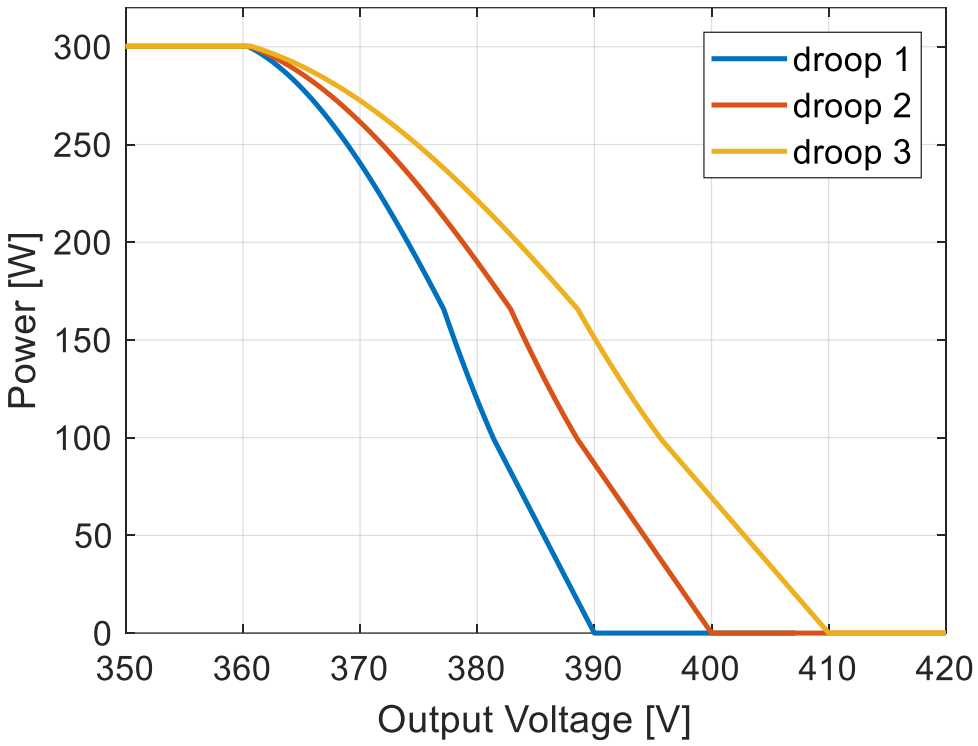


Figure 43: Input power variation with output voltage

6. Conclusions and Recommendations

6.1. CONCLUSIONS:

The aim of this project was to design the prototype for flow converter and to implement decentralized control. A prototype of flow converter was designed and tested for bi-directional power flow. Power droop is being incorporated in the constant current control scheme. The load sharing and voltage regulation using droop mechanism are also demonstrated.

- **What is the most suitable converter topology for the flow converter in interconnecting SHS. (Ch2)**

Three different topologies were considered in chapter 2 for the flow converter in the interconnecting system. The bi-directional was found most suitable due to its simple design and the control. Major advantages of flyback topology are well documented current control method, soft switching without any extra component, low components count.

- **How to optimize the bidirectional flyback converter design for soft-switching enabling power-flow in both directions?**

The optimization of the power stage of the flow converter was presented in chapter 3. The flow converter works in BCM and DCM mode with valley switching enabled. Compare to unidirectional flyback, bi-directional flyback has some additional challenges, e.g. reverse recovery of MOSFET diode, the impact of the parasitic capacitance of secondary side and implementation of valley switching in both directions. These challenges were taken into account in the design of the converter. The measured efficiency of the converter matches well with simulated results. At maximum power, the converter efficiency was around 90% that is quite good considering efficiency was not the primary objective of the thesis.

- **How to implement current control for complete power range in both direction?**

  The current control was designed using TEA1735 which is an analog flyback controller. The digital control was not used in the thesis. The feedback circuit is based on the PI control which enables the flow converter to transmit power in both directions.

- **How to achieve decentralized control at the system level for the selected converter topology?**

A coordinated control strategy was purposed in the chapter 5, and control laws for charge converter, PV converter, and flow converter were discussed. All the operating system of SHS were analysed to derive the operating mode of the flow converter in each state. The decentralized control for flow converter has been implemented using DC bus signaling with power droop. The voltage at the LV bus and HV bus are sensed or controller to perform the different function of the coordinated control.

- ***How to implement the control for flow converter to enable the load sharing among SHSs?***

The load sharing can be achieved using the power droop for flow converter. A control method to implement the power droop was presented and have been successfully tested on the prototype for flow converter. The power droop has been integrated inside the current control scheme.

6.2. Recommendation:

As the aim of the thesis was to design the prototype for flow converter and demonstrate the load sharing and voltage regulation, there are several recommendations which can be used for the next design of flow converter.

Synchronous rectification:

As the focus of this work was the demonstration of decentralized control in interconnected SHS, the efficiency was the not primary goal. Still, good efficiency was measured for the complete power range. In the next revision, synchronous rectification must be used to improve the efficiency of the converter.

Transformer Design:

The designed transformer was sub-optimum and has a very high leakage inductance. This had resulted in many problems during the testing and lower efficiency. A new design for the transformer to minimize the leakage inductance must be considered. The leakage inductance can be decreased by sandwiching the windings, using a bigger core and better manufacturing of the transformer.

Converter Size:

The flow converter is not optimized for the size as through-hole components were used. In the next revision, SMD components can be used to reduce the size.

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