Fabrication and Reliability Study of Parylene-Ceramic Based Flexible Interconnects For Implantable Devices

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Fabrication and Reliability Study of Parylene-Ceramic Based Flexible Interconnects For Implantable Devices

By

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ABSTRACT

The Flex-to-Rigid (F2R) platform is a generic IC-based technology platform that allows flexible sensors and electronics to be fabricated and integrated onto the catheters or guidewires of minimally invasive medical instruments. In this thesis, a process flow was developed for the fabrication of flexible metal interconnects based on the F2R platform using materials that are biocompatible for neural implants, namely parylene and titanium nitride.

A “parylene last” process flow was developed that allows a higher temperature budget of up to 400°C for IC fabrication, and enabled the addition of a ceramic encapsulation layer beneath the parylene encapsulation for improved adhesion and decreased permeability to moisture. For this process flow, two new technology modules were developed: the titanium buried mask and the aluminum etch stop layer. A device with working flexible interconnects connected to bond pads on a rigid silicon island was fabricated.

Evaluation testing showed that the interconnects were able to function after four weeks at accelerated aging conditions corresponding to four months in human body conditions, and were able to be bent to a diameter of less than 0.25 mm before device failure.

PREFACE

This thesis concludes my Electrical Engineering master's degree program. I would like to express my most sincere gratitude to my supervisor Prof. Ronald Dekker for giving me the opportunity to work on this project and for all the support and feedback he offered, and to my mentor Marta Kluba for her invaluable guidance both in the cleanroom and throughout the entirety of my thesis. I have learned so much from them both, and I'm proud to have contributed to this project.

I would also like to give thanks to the EKL colleagues and technicians for sharing their technical expertise, and also for making the cleanroom such a pleasant environment to work in. Finally, my thanks to the other master's students, Arshaad, Bart, Affan, Shinnosuke, Gandhika, and all the others, for their motivational support and advice.

D.Z. Wu
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1 INTRODUCTION

Bioelectronic medicine is a new method of treating chronic health problems using implantable devices to electrically stimulate, suppress, or record neural activity [1]. Currently, neurological disorders are most commonly treated by using chemical agents such as pharmaceutical drugs to affect the behaviour of the nervous system [2]. However, this method has several downsides. Chemical stimulation is not targeted to any specific area of the nervous system, and nerve cells are affected over a relatively large region, leading to unwanted side effects in the patient. Furthermore, the transfer of information across chemical synapses is slower, and it may take up to weeks for the effects of drugs to show.

By contrast, bioelectronic medicine such as deep brain stimulation (DBS) offers the advantage of being able to treat a disorder with no side effects by stimulating only the target nerve. The electrical stimulation is instantaneous, and the effects are easily reversible by turning off the stimulation [3]. A neural probe lead containing an array of microelectrodes is used to interface with the target nerve and electrical signals are delivered by a pulse generator, which is generally implanted in the chest of the user due to the large size of the packaged electronics.

The conventional lead design used for DBS is a probe tip 1.27 mm in diameter with four platinum/iridium cylindrical electrodes stacked along the tip, as can be seen in Figure 1 [4],[5]. However, this setup carries the risk of targeting errors when attempting to stimulate smaller regions in the brain, which will again cause side effects in the user [6],[7]. In order to address this issue, designs have been developed for directionally-segmented electrodes that would allow for radially directed electrical stimulation [7]. The lead is fabricated as a two-dimensional array of electrodes on a thin film, which can then be released from the silicon wafer and wrapped cylindrically around the probe tip. Proof of concept tests have shown that directionally segmented DBS leads allows for current steering, which reduces side-effects caused by stimulating nearby nerves, and also improves the spatial resolution and selectivity of the electrodes when recording signals [8].

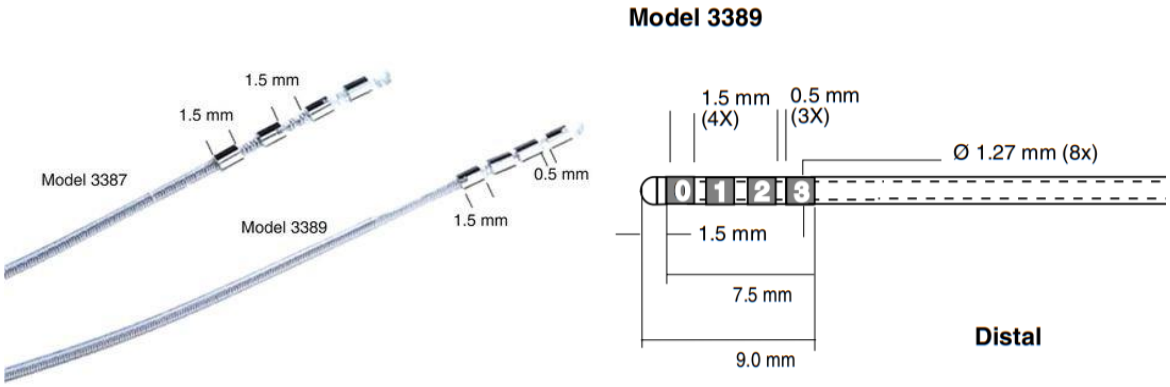


Figure 1: Electrodes on Medtronic lead model 3389 for DBS [4],[5].

Though segmented electrodes allow for more spatial resolution, higher current densities may occur depending on the geometry of the electrode, and programming the electrical stimulation becomes more complex [9]. If electronics for sensing and data processing could be integrated onto the probe lead, a closed loop system could further increase the effectiveness of deep brain stimulation.

The Flex-to-Rigid (F2R) platform is a generic IC-based technology platform based on a high temperature fabrication process that enables flexible sensors and electronics to be fabricated and integrated onto the tips of catheters or guidewires of minimally invasive medical instruments [10],[11]. As these tips are cylindrical in shape, it is difficult to use conventional rectangular ICs. F2R allows electronics of arbitrary shape and thickness to be fabricated as an array of semiflexible islands connected by flexible polymer-embedded electrical interconnects. The device is fabricated on a silicon wafer and kept attached using tabs of a material such as polyimide for easy handling, as can be seen in Figure 2(a). Once it is released from the frame, it may be bent around the catheter or guidewire and affixed using an adhesive as shown in Figure 2(b).

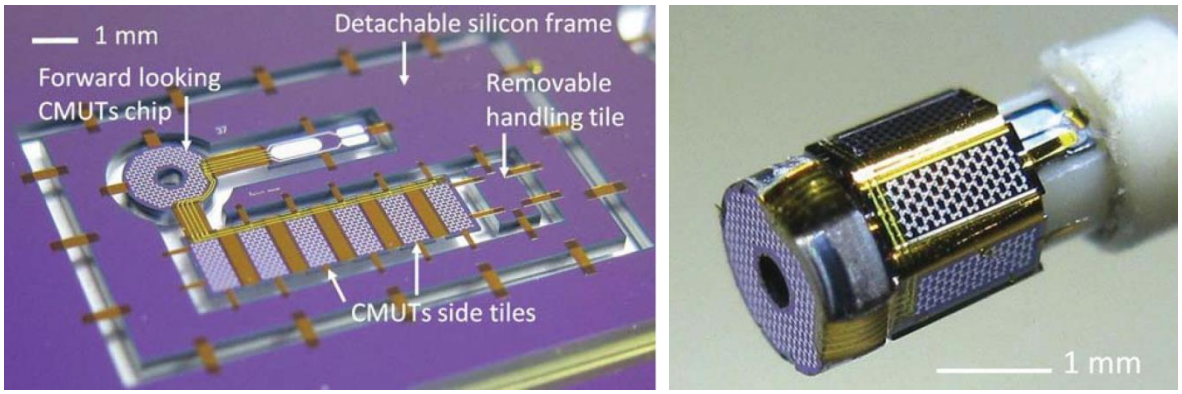


Figure 2: (a) F2R demonstrator in silicon frame; (b) Demonstrator released from the frame and integrated at the tip of a catheter [10].

F2R would prove highly advantageous to neural implant technology as it would allow for the fabrication of directionally-segmented DBS electrodes. It may also be used for integrating electronics into probe tips by fabricating silicon chips of arbitrary shape and thickness with flexible interconnects as part of a single process flow, resulting in fewer modular parts in the total device and decreasing the risk of device failure [10],[11]. A number of demonstrators have been designed to prove the functionality of the F2R platform. However, the demonstrators were fabricated with aluminum metallization and polyimide-embedded interconnects. As DBS probes are implanted in the user's brain for an extended period of time, the materials must be nontoxic to cells and must not provoke immunological responses from the body [12].

For biomedical neural implants, polyimide is not certified as a biocompatible implant material by the international standard ISO 10993 [13], and aluminum is not a noble metal, and therefore prone to corrosion. Thus, in order to utilize F2R technology for brain implants, the fabrication must be tested using materials compatible for brain implants.

1.1 Materials

The proposed material for encapsulating the electrodes and embedding the interconnects in is parylene C. For metallization, the two materials considered are platinum and titanium nitride. Parylene C and platinum have been used previously for neural implants, while titanium nitride has a higher resistance and is untested for neural implants but has the advantage of being readily available and easy to process in most cleanrooms.

1.1.1 Parylene C

Of the polyparaxylylene family of polymers, parylene C [poly(dichloro-p-xylylene)] is the most commonly used type for biomedical applications as it shows the most suitable electrical and moisture barrier properties. It is commercially available and FDA approved [13][14] with USP Class IV biocompatibility [15]. Properties of parylene include chemical and biological inertness and lower permeability to gasses and water than PDMS and polyimide [16]. It is particularly well-suited for neural implants which must interface with nerve cells and are surrounded by delicate glial cells or fibrous tissue.

Parylene C has a melting point of 290°C and a glass transition temperature of 90°C [15],[17]. At temperatures above the glass transition temperature, the polymer chains will rearrange to a crystal-like structure and the parylene becomes brittle and rigid [13]. Therefore, for a wafer deposited with parylene, processing steps must be kept at temperatures below 90°C to prevent cracking in the film [15],[17]. Furthermore, at temperatures above 100°C, parylene in atmosphere will oxidize [15]. The limited thermal budget is a large challenge when using parylene in microfabrication.

1.1.1.1 Parylene Deposition

Parylene C is deposited using chemical vapor deposition (CVD) polymerization. CVD is done via the sublimation of a dimer, para-xylene, at a temperature of 150°C in a vaporizer under vacuum [18]. The dimer gas flows into a pyrolysis furnace with a temperature set to 690°C, where the double-molecule structure of the gas transforms into monomer vapor. The vapor then enters the deposition chamber, which is at room temperature. The monomers bond in long parylene chains which are deposited on all surfaces of the deposition chamber. The result is highly conformal, pinhole-free, and stress-free layers of parylene with uniform thickness [19],[14].

The vapor condensation technique results in better step-coverage at the edges of underlying structures than other deposition methods such as spin coating.

1.1.1.2 Parylene Adhesion

Parylene C is permeable to water vapor and, if used for encapsulation, does not form a hermetic seal around the electronics. Though the material quickly becomes saturated with water vapor, as long as there are no open areas or voids on the inside of the encapsulation layer in which water vapor may condensate, the electronics will remain protected from corrosion [20]. To prevent the formation of voids, the encapsulation material must have good adhesion to the substrate, with no contaminants or foreign particles in between the layers [1].

It had been reported that parylene shows bad adhesion to some materials without the use of adhesion promoters that modify the surface properties of the polymer or the underlying layer [19][21]. It has also been indicated that the adhesion of parylene C varies widely depending on the material that the parylene C is deposited on [1]. As parylene C is hydrophobic, a common adhesion promoter for hydrophilic silicon and silicon-based compounds is A-174 silane, which is a molecule with a hydrophilic methoxy silane head that adheres to hydroxyl groups on the silicon surface and a methacryloxy tail that bonds to the parylene [22],[23]. Tests have been done on bonding strength between parylene and silicon nitride, and the adhesion force in a 90° Peel test was seen to increase from less than 10 mN/cm with no silane treatment to ~1000 mN/cm with a silane treatment [22].

Oxygen plasma treatments have also been shown to improve adhesion by making the surfaces of certain materials such as SiO_2 and SiN wettable to improve the effects of the silane primer, and by increasing surface free energy [13],[24].

1.1.2 Platinum

Platinum is one of the most commonly used metals for neural stimulation electrodes. It is a noble metal and thus relatively corrosion-resistant, biologically inert, and non-toxic [25],[26]. It has been proven capable of transferring charge with reversible reactions [27]. Current probe leads for DBS use electrodes of a platinum iridium alloy [28].

1.1.2.1 Platinum Deposition

Platinum may be deposited using physical vapor deposition (PVD), also called sputter deposition. By bombarding a target with ionized gas, atoms of the target are ejected from the surface and condense to form a thin film on the substrate. The film is conformal and has a relatively good step coverage due to the high energy of the atoms. For platinum sputtering, an inert gas such as argon is used [29].

Platinum will diffuse into silicon, changing the electrical properties and causing deep-level defects in silicon. There is the risk of contamination when processing wafers with platinum in many machines, if the exposed platinum comes into contact with chucks or contaminates furnace tubes. For this reason, the processing that may be done with platinum in the cleanroom is limited.

1.1.3 Titanium Nitride

Titanium nitride (TiN) is a metallic conductor that has been proposed as an electrode material for neural implants. It has good electrical conductivity and the window in which reversible reactions may be performed is higher than that of Pt. It also has large charge storage capacity and is chemically and mechanically stable [27],[30]. The resistivity of titanium nitride films varies with the nitrogen concentration during the deposition. For bulk TiN, the resistivity is 20 ± 10 μΩ·cm at 20°C [31].

TiN has been used as a biocompatible material for orthopedic implants and as hard coatings in medical instruments [32]. It has been used for cardiac pacemaker electrodes [30] and has been tested and shown to be non-cytotoxic [33], but investigations upon using TiN as a retinal implant material showed reduced cell numbers when the cells were in direct contact with the TiN surface, ostensibly due to surface structure of TiN [34]. Varying reports of biocompatibility have been given for TiN in several different reports, and the biocompatibility of TiN for use of neural implants is uncertain.

1.1.3.1 Titanium Nitride Deposition

TiN is deposited using PVD reactive sputter deposition. The technique is the same as is used for Pt sputtering, but the pure Ti target is sputtered in the presence of nitrogen, which is a reactive gas. The concentration of the compound may be adjusted with the gas flow. Argon gas is also used for a stable plasma for sputtering [29].

TiN is a material commonly used in IC fabrication and therefore has well-established deposition and processing technology. Unlike platinum, it may be processed in the cleanroom without the risk of contamination. For this reason, TiN may be more convenient to use, especially when preparing test wafers and short loops.

1.2 Aim of This Thesis

The main objective of this thesis is to produce a flexible device based on parylene with metallic interconnects, and to evaluate its flexibility and ability to survive aging effects using stress testing.

The broad goal is to develop a fabrication process for flexible electrodes and interconnects using materials that are suitable for neural implants. Previous work was done on this subject by A.I. Kanhai in his master's thesis "Flexible parylene-platinum based electrodes and interconnects", which investigated the use of parylene and platinum with the F2R platform [35]. Kanhai developed a fabrication process for platinum interconnects and electrodes with focus on minimizing particle contamination, investigating the adhesion of parylene to various materials using a cross cut test, investigating the patterning of parylene and platinum, and investigating the release of the flexible membrane of the device.

The previous work done by Kanhai indicated some difficulties caused by the presence of parylene on the wafer when etching platinum. Ion milling causes the formation of platinum fences due to the redeposition of platinum on the resist sidewalls. For other metals, these fences may be removed by wet etching, but a wet etching process is not defined for platinum on parylene [35]. There was also difficulty in removing photoresist since oxygen plasma could not be used due to the presence of parylene. These problems could be resolved by a process flow that allows parylene deposition to be done after the metallization is deposited and patterned.

This thesis uses the groundwork laid by Kanhai to improve the implantable flexible interconnects fabrication process. Platinum was intended as the metallization material but due to necessity and convenience, titanium nitride was also used. This process also introduces a ceramic layer in between the parylene and metallization in order to improve adhesion and reduce permeability of the encapsulation. The addition of the ceramics layer requires a change in the order of deposition and fabrication steps. It also allows for a higher temperature budget (up to 400°C) during the fabrication process by implementing the "parylene-last" approach.

In order to achieve this goal, two new technology modules are developed: a titanium buried mask for patterning the parylene, and an aluminum stop etch layer. Both technology modules are tested using short loops to investigate the deposition, lithography, and patterning of the structures. The technology modules are then integrated into the final process flow. The intrinsic stress in the ceramic encapsulation layers is also investigated, as is the lithography and pattering method.

Finally, two evaluation tests are performed. The first is an accelerated aging test in PBS at 57°C to check for water condensation in any voids that may form between the ceramic and parylene layers, and to assess the adhesion. The second is a bending test to test the minimum diameter the interconnects can be bent to before device failure occurs due to cracks in the metal lines.

1.3 Organization of This Thesis

Chapter 2 discusses the design of the device, with focus on the changes made to the masks and the fabrication process step order in relation to the previous work of Kanhai. Chapter 3 discusses the new technology modules introduced in this process flow, including the ceramic encapsulating layers, the titanium buried mask, and the aluminum etch stop layer. Chapter 4 discusses the final process flow and integration of the technology modules including the complications that were encountered

and the applied solutions. Chapter 5 describes the device evaluation process and results. Chapter 6 concludes the thesis, and offers recommendations for future work.

2 DESIGN

The goal of the project is to produce a device that demonstrates the ability to use F2R technology for neural implants. Therefore, two basic elements used in the electronics of DBS probe leads, electrodes and interconnects, are fabricated on the flexible parylene membrane.

Electrodes are electrical conductors used to record and stimulate electrical activity in cells. As they are intended to directly interface with the target nerve to deliver the signals, there are certain properties that must be considered when choosing design aspects, such as size, geometry, and material of electrodes used for neural implants.

Stimulating electrodes deliver charge in the form of biphasic current pulses. A high charge/phase will cause tissue degradation, while a high charge density will cause irreversible chemical reactions at the electrode-body interface during charge transfer [27],[36],[37]. Electrodes used for DBS typically have a surface area of about 0.06 cm^2, with a charge/phase threshold of 135 – 400 nC/ph and a charge density threshold of 2.3 to 6.7 $\mu C/cm^2$ [27]. Recording electrodes have smaller surface areas of less than 2,000 to 4,000 μm^2 and must have high signal to noise ratio to be able to distinguish the signal of interest from the noise that originates from both the firing of nearby neurons and the impedance of the electrode. Recording electrodes typically have impedances ranging from 50 kΩ to 1 MΩ [27].

Interconnects in integrated circuits serve as wiring. They are typically made of aluminum that is etched during the fabrication process in such a way that electrical connections are formed between the components, and, in typical integrated circuits, do not need to be flexible. However, for electronics integrated at the tip of probe leads, the interconnects must be able to wrap around the lead with the membrane.

The material for the flexible interconnects should also be low impedance to reduce noise and signal delay [27]. Furthermore, the Young's modulus of the interconnect material must be low enough so that the interconnects do not crack when the membrane is folded. The previous design by Kanhai proved able to be rolled to a diameter of < 1mm. The flexibility of the device developed here needs to be re-evaluated with the addition of the ceramic layers.

2.1 CERAMIC ENCAPSULATION

The added layer of ceramic between the parylene and the metallization encapsulates the metal lines of the electrode and interconnects and serves two purposes. The first is to improve the adhesion between the material used for the metallization and the parylene layer, as the adhesion of parylene to ceramics has been verified to increase from less than 10 mN/cm to ~1000 mN/cm using surface modification and adhesion promoters [24].

The second purpose of the ceramic layer is to compensate for the permeability of parylene to water vapor, while taking advantage of the structural biocompatibility of parylene over the rigid ceramics. A study has shown that a multilayer thin film barrier of alternating layers of parylene and ceramics like SiOx allows the oxide to make up for the gaps between the polymeric chains that allow molecules to pass through [38]. This method also uses parylene as a stress releasing layer for the oxide, since stress causes pinholes, cracking, and delamination of the oxide layers [38]. Compared to an

encapsulating layer of the same thickness using only parylene, the parylene oxide multilayer showed lower water permeation and water vapor transmission [38].

This project uses only one layer of parylene encapsulating the stack of ceramic layers consisting of silicon nitride and silicon oxide. The ceramic stack is about 900 nm thick in total, with about 450 nm of ceramic on either side of the metallization.

The order of the layers from the bottom to the top is as follows: a 50 nm layer of silicon nitride, a 400 nm layer of silicon oxide, the patterned metallization, a 15 nm layer of silicon nitride, a 400 nm layer of silicon oxide, and a final layer of 50 nm of silicon nitride. The outer encapsulating layers of silicon nitride have been proven to show good adhesion to parylene with the use of A-174 silane [22], and the 15 nm of silicon nitride improves adhesion between the metallization and the oxide layer. The use of SiN and SiO_2 layers stacked together decreases the possibility of pinholes that will penetrate through both layers.

2.2 Structure Design

The main parts of the device include the rigid silicon island and the electrodes and comb-meander structures, which are located on the flexible film. The locations of the structures are indicated in Figure 3. The structures are largely kept the same from the previous design fabricated by Kanhai with exception of the decreased length of the meander (and corresponding decrease in number of teeth of the comb), the rounding of all corners of 90° in the back side hard mask to reduce the breaking effects caused by the sharp edges of the silicon island after DRIE, and modification of the metal lines at the junctions to prevent angles of less than 45° in order to facilitate etching.

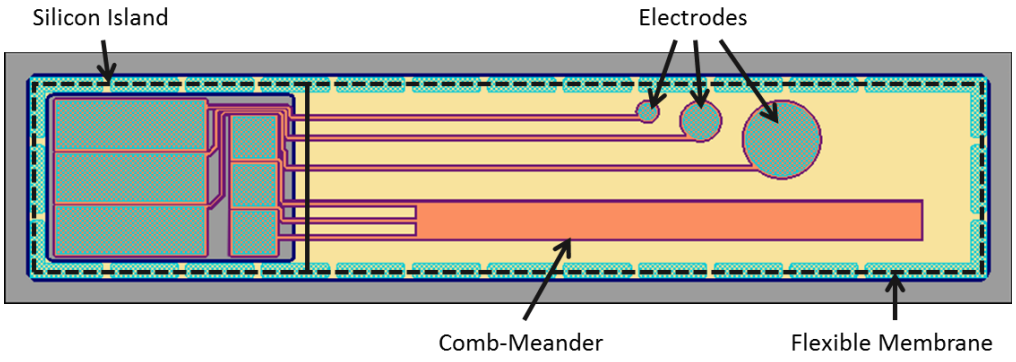


Figure 3: Labelled structures of the device.

2.2.1 Rigid Silicon Island

During the F2R process, silicon chips and the connecting flexible interconnects may be fabricated in a single process. The ability to fabricate these chips is demonstrated in this process with the rigid silicon island. For this device, the thickness of the silicon island was left at 400 µm, the original thickness of the silicon wafer. The shape of the island is determined by the back side PECVD oxide mask.

The rigid silicon island contains the bond pads connected to the electrodes and the comb-meander structure in order to allow electrical measurements to be made.

2.2.2 Electrodes

The electrodes are circular with radii of 185 µm, 370 µm, and 740 µm, which are on the scale of sizes used for stimulation. The sizes were kept the same as in Kanhai's project. They are connected to the bond pads on a rigid silicon island to make electrical connections possible. The size of the bond pads leading to the electrodes was also not changed, and is 3000 x 1000 μm^2 to allow for clamping during an electrochemical test in which constant electrical stimulation must be applied.

2.2.3 Comb-Meander Structure

The comb-meander structure can be seen in Figure 4 and is designed to evaluate the flexible interconnects. The width of all metal lines is 20 µm, not including the corners which are at 90° angles. The total length of the meander is approximately 126,500 µm, estimated by measuring at the center of the metal line.

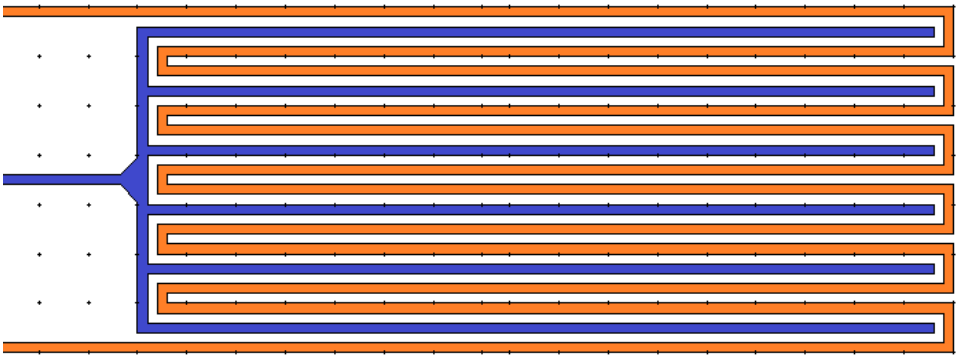


Figure 4: An example of comb (blue) and meander (orange) structures.

A change was made from the previous design in that the length of the comb-meander structure was shortened by one loop in order to move the metallization away from the edge of the membrane. The membrane will be manually cut from the silicon frame along the perforated edges, but the force of the knife causes some damage to the edges of the membrane, so moving the metal lines away from the perforated edge reduces the chance of errors due to handling.

The comb and meander structures are connected to bond pads on the silicon island. The bond pad sizes are 900 x 900 μm^2, as they only need to be touched down on using probe needles for impedance measurements.

2.3 "Parylene Last" Fabrication Process

A wafer with parylene on it may not be processed at high temperatures. Generally, the accepted practice is to limit the temperature to below 90°C. The changes made to the process flow from the previous work by Kanhai allow the first parylene deposition to be made later in the process, meaning the prior steps have a higher temperature budget.

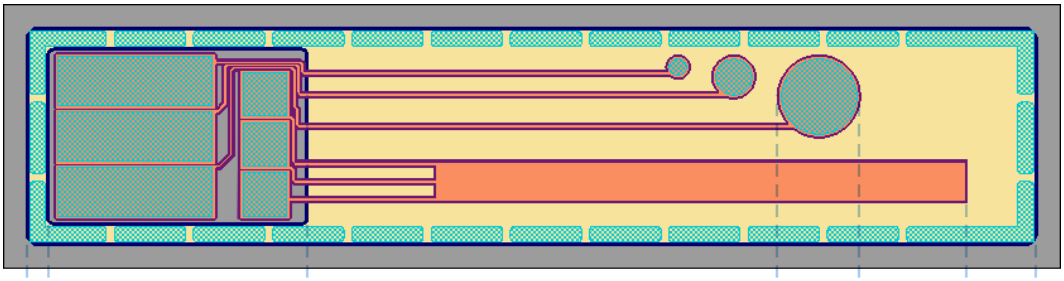
As can be seen from Figure 6Figure 5, the process flow begins with the deposition and patterning of the SiO_2 hard mask for the back side DRIE etch, along with the DRIE etch stop layers of SiO_2 and Al on the front side of the wafer. The SiO_2 etch stop layer is to prevent the DRIE from sputter etching the metal and also to provide insulation on the silicon island, while the Al etch stop is to protect the ceramic encapsulation layers. The first stack of ceramic encapsulation is deposited, followed by the metallization deposition and patterning, then followed by the second stack of ceramics. Next, all

ceramic layers are patterned and etched at once. At this stage, the electrode is fully encapsulated in ceramic aside from the bond pad and electrode openings. The first parylene deposition is done only after the ceramics and the metallization have been deposited and patterned. This approach allows for the PECVD ceramic deposition at high temperature, which would not be possible if a bottom layer of parylene had already been deposited.

A masking layer of Ti is deposited on the front side of the wafer. The top layer of parylene from the first parylene deposition is kept while the parylene on the back side of the wafer is etched, exposing the pre-patterned back side mask for DRIE. Deep reactive ion etching (DRIE) is used to remove the bulk silicon from the back side, followed by removal of the etch stop layers (SiO_2 and Al) until the bottom ceramic encapsulating layer is exposed. The second parylene deposition completes the parylene encapsulation on the back side of the wafer.

As the CVD results in a conformal layer of parylene over the entire device, the front side now has a second layer of parylene. This layer is removed from front side with an O_2 plasma etch. At the same time, the bond pads and electrodes are opened through the titanium buried mask. The buried mask is then removed. The end result is a metallization that has relatively the same amount of parylene thickness on both the front and back sides. Keeping the metallization in a neutral plane will prevent the metallization of the interconnects from breaking when the membrane is bent.

For a detailed description of the fabrication process, see Chapter 4.

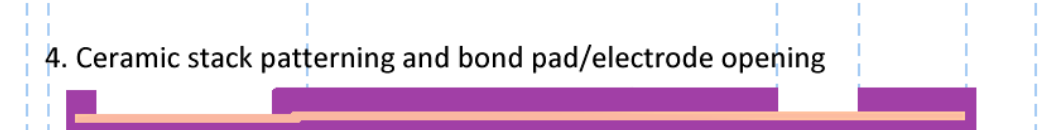


1. Front/back side PECVD oxide, back side DRIE hard etch mask patterning

2. Al etch stop layer deposition and patterning

3. 1st Ceramic dep, metallization dep/patterning, 2nd ceramic dep

4. Ceramic stack patterning and bond pad/electrode opening



5. 1st parylene deposition

6. Ti buried mask dep, back side parylene etch, Ti patterning

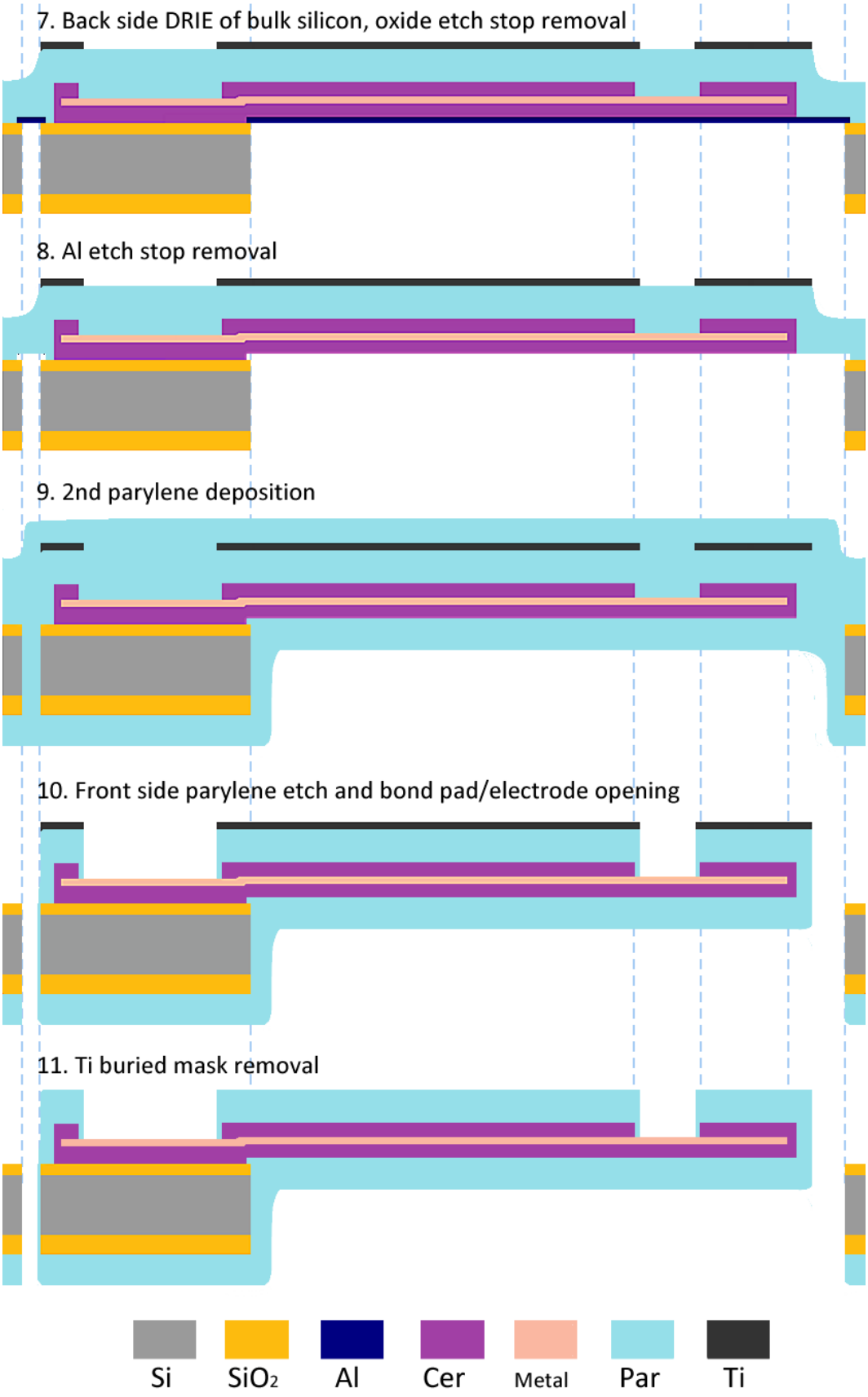


Figure 5: Simplified schematic flow of the full process.

2.4 Masks

Five masks were used for this process flow. Three of the masks were used directly or with minor modifications from the previous project, while two are introduced for this project. More details on mask modifications can be found in Chapter 4.3.

2.4.1 Hard Mask for DRIE

This mask is used for patterning the 6 µm of SiO_2 on the back side of the wafer. The SiO_2 will serve later in the flow as a mask for the deep reactive ion etching (DRIE) that will release the device from the bulk silicon, leaving a flexible membrane of electrodes encapsulated in parylene and ceramic. This mask also defines the boundaries of the silicon island, leaving the area around the bond pads inflexible in order to facilitate electrical measurements. It may be seen in Figure 6(a).

The modification made to this mask from the previous device was to round the corners of the release area in an attempt to mitigate cracks spreading from the junction of the membrane and the silicon island.

2.4.2 Aluminum Etch Stop Layer

This mask patterns the aluminum etch stop layer, which is used to protect the ceramic encapsulation layers from being etched during the removal of the SiO_2 stop layer after the DRIE back side etch. This is a new mask introduced in this process. The Al etch stop layer/mask must be larger than the area that will be released by the DRIE, but not underlay the ceramic layers so much that it becomes difficult to remove it with a wet etch. For more on this mask design, see Section 4.2.1. The mask may be seen in Figure 6(b).

2.4.3 Metallization

The metallization is patterned using the mask from the previous device, but a few loops of the comb and meander structures were removed in order to move the metal lines away from the edge of the device, as tearing of the membrane edges occurred when manually trying to cut individual dies out of the frame. The corners of the junctions of the metal lines are rounded and structured to prevent angles of less than 45° in order to ensure that the ceramic layers may be fully etched. It may be seen in Figure 6(c).

2.4.4 Ceramic Stack Mask

As the previous device did not have a ceramic encapsulating layer, this mask is a new design. The mask for the ceramic layers patterning is designed so that the ceramic encapsulation would extend beyond the metal lines by 50 µm. The ceramic encapsulation around the metal electrode pads are extended by 20 µm. The comb-meander structure is encapsulated in one block of ceramic due to the thin metal lines being in close proximity to each other. The metal bond pads on the silicon island are likewise encapsulated in one block, as the island is not flexible anyway.

The ceramic mask is also used to open the bond pads and electrodes with an exclusion of 20 µm for the bond pads and 10 µm for the electrodes so that during the step in which the ceramic is patterned and etched, the metal of the bond pads and electrodes will also become exposed during the etch. It may be seen in Figure 6(d).

2.4.5 Titanium Buried Mask

This mask is used to pattern the titanium buried mask which is deposited and patterned on the first parylene layer. After the second parylene deposition, this mask allows for the removal of excess parylene from the front side of the wafer, while at the same time opening the first parylene layer on the bond pads, electrodes, and the perforated line around the edge of the device so it may be removed from the frame more easily. As the locations of the bond pads and electrodes have not changed, this mask was used directly from the previous device. It may be seen in Figure 6(e).

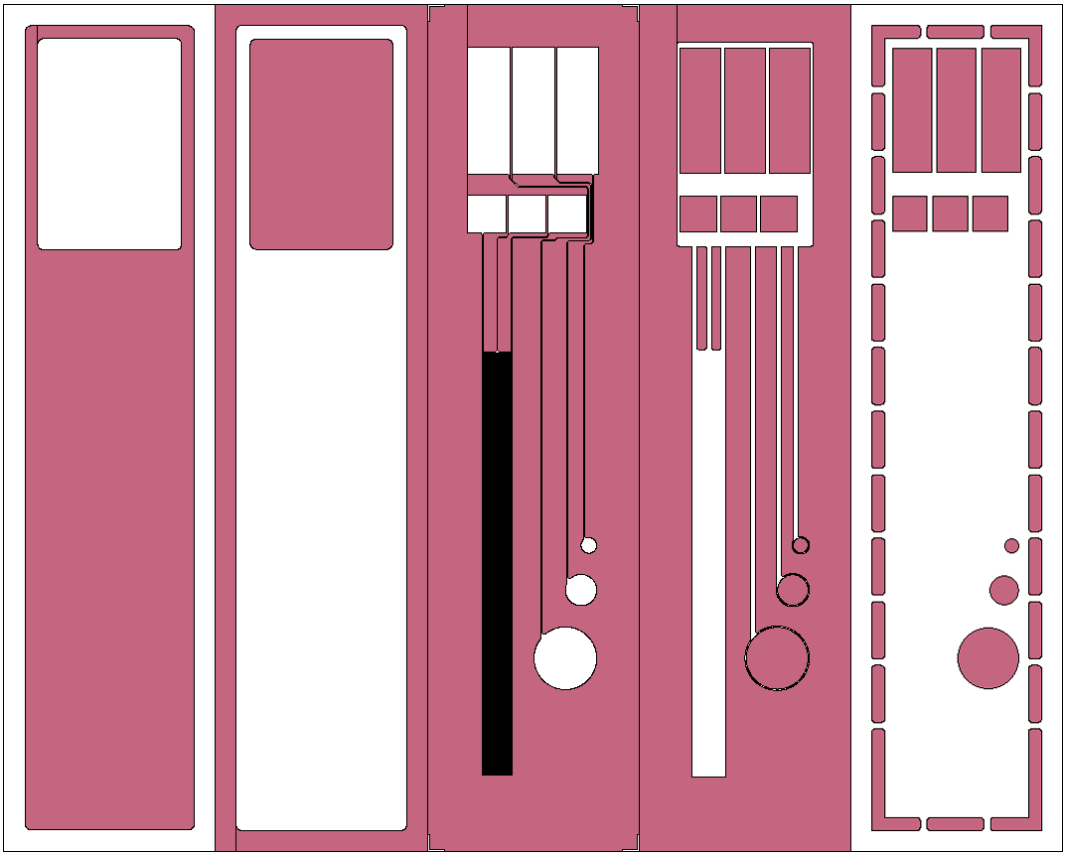


Figure 6: Masks for (a) hard mask for DRIE; (b) Al etch stop layer; (c) metallization; (d) ceramic layers; (e) Ti buried mask.

3 TECHNOLOGY MODULES

This device was based on the work done on the previous project, and therefore adhesion of parylene to underlying layers and design were not tested. The new technology modules introduced and developed in this project include the ceramic encapsulation, the titanium buried mask, the aluminum etch stop layer, and the use of titanium nitride as a metallization material.

3.1 CERAMIC ENCAPSULATION

The ceramic encapsulation is done using a combination of oxide and nitride layers. The total thickness is about 1 µm, with about 0.5 µm for the thickness of either the top or bottom encapsulating layer.

3.1.1 STRESS

The deposition of ceramic layers introduces stress to the wafer from both the microstructure of the film and the deposition process. The stress may be either tensile, where it is directed from the center of the wafer towards the edges and causes concave bending, or compressive, where it is directed in the opposite direction and causes convex bending. Tensile stress may result in cracks in the film, while compressive stress will cause the layers to buckle and compromise adhesion. For this reason, it is preferable to have tensile stress over compressive stress, though the tensile stress should still remain low (<100MPa) [36].

For the fabrication of a flexible device, stress in the layers will cause the released membrane to curl in the direction of the tensile stress. Too much stress will result in the released device folding or rolling up on itself, which is undesirable. To evaluate the stress in the final device, measurements were made of the stress in the ceramic layers at room temperature for each of the individual layers, as well as for layers in combinations with each other according to the order they would be deposited in for the actual device. The layers were deposited directly on 4" single side polished silicon wafers of thickness 500 µm. Stress measurements were made using the Flexus 2320-S.

The individual layers of SiN result in compressive stress, with the thinnest layer of 15 nm having high stress values approaching 100 MPa. However, the stress of the SiO_2 layer results in low tensile stress. Table 1 shows the stresses of the bottom half of the encapsulation (bottom stack), the top half of the encapsulation (top stack), and the full encapsulation, minus the metallization in between, and all of the layer combinations show low tensile stress.

Table 1: Stress measurements done on ceramic layers

Stack	Wafer Orientation [deg]	Stress [Mpa]	Radius [m]	Bow [µm]
Bottom Stack	0	7.57	6.92E+02	-1.31
	90	10.64	2.62E+02	-3.56
Top Stack	0	23.9	5.01E+02	-1.76
	90	24.84	2.51E+02	-3.69
Full Stack	0	27.03	3.13E+02	-2.67
	90	27.27	2.10E+02	-4.14

Note that, following convention, negative values indicate compressive stress while positive values indicate tensile stress.

Based on the stress measurements of the full stack, once the ceramic layers are deposited, they should not crack or buckle while on the wafer, and the effect of the ceramic layers on the curving of the released flexible device should be relatively minimal.

3.1.2 Patterning of Ceramic Layers

The specifications for the coating, exposure, and development of the ceramic stack were chosen based on knowledge from previous short loops and done using the automatic coater and developer. The photoresist used was AZ 3012 of thickness 2.1 µm to account for the topography of the structures which was, at this point in the process, greater than 1 µm. The exposure energy used was 200 mJ with a focus of 0 µm. Development was done in MF322 developer for 30 seconds using the recipe "Dev-SP1".

The ceramic layers were patterned via plasma etching in the Alcatel so that the ceramic would encapsulate the metal lines. During this etching step, the bond pads of the electrodes and on the silicon island were opened. The standard oxide etch recipe used was (CF_4: 50.0 Sccm, CHF_3: 25.0 Sccm, He: 40.0 Sccm, Power: 60 Watts). The approximate combined thickness of all layers to be etched was 915 nm of SiO_2/SiN. The etch time used was 24.5 min, which was calculated based on an etch rate of 39 nm/min for SiO_2 and 42 nm/min for SiN. Some overetching is done since the etch rate is different between the center of the wafer and the sides.

Beneath the ceramic layers, there is an etch stop layer of 400 nm SiO_2. After the etch, the SiO_2 etch stop layer thickness ranged from about 330 nm to 390 nm, indicating that the Alcatel etch is not uniform and the underlying layer is etched through by 10 nm to 70 nm. However, it is preferable that the underlying SiO_2 layer, which will be removed later in the process, is overetched somewhat to ensure the ceramic stack is fully etched.

3.1.3 SiN and Uniformity Mode

The ceramic layers were deposited using PECVD in the Novellus Concept One. Typically, the Novellus transfers the process wafer between eight chucks with deposition occurring for the length of time specified in the recipe on seven of the eight chucks, so the actual deposition time is seven times the recipe time.

As a layer of 15 nm is too thin for the standard deposition method, Uniformity Mode must be used. This mode requires eight wafers to be placed in the carrier. During deposition, each chuck holds one wafer and the deposition time specified in the recipe is the actual deposition time for each wafer. However, this results in less uniformity of layer thickness between the wafers. In order to keep the deposited thickness as consistent as possible, the process wafers should be placed in slots 3-6 of the carrier, as a test deposition of 15 nm of SiN on eight Si wafers showed the wafers in these slots to have the least variation. A representation of the Novellus chucks can be seen in Figure 7, with the numbers corresponding to which slot of the wafer carrier the wafer is taken from.

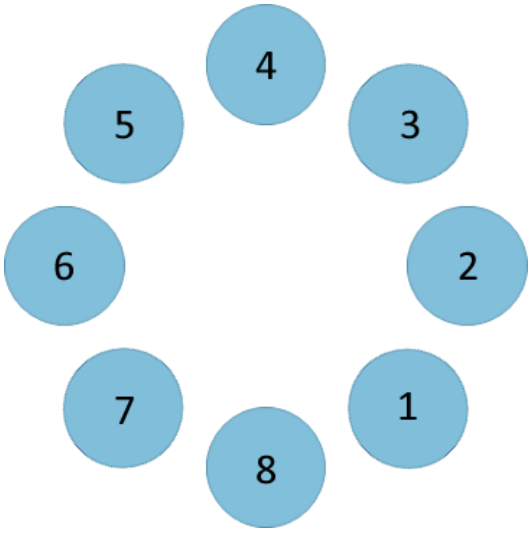


Figure 7: Representation of chucks in the Novellus and the corresponding wafer carrier slot in Uniformity mode.

3.2 TITANIUM BURIED MASK

The titanium buried mask is deposited after the first parylene deposition and serves two purposes: an etch stop that allows for the removal of the second parylene deposition from the front side while preventing the first parylene deposition from being etched, and to serve as a hard etch mask for opening the electrode bond pads.

Previous experiments using aluminum as a masking layer for parylene have shown that the aluminum has bad adhesion to parylene when wet etching. More importantly, the current process flow includes a step in which an aluminum etch stop layer is removed by wet etch, during which the buried mask is exposed to the wet etchant. Thus, the wet etch must be selective to the etch stop layer. Titanium was chosen as the material for the buried mask as it is not etched in the phosphoric/acetic/nitric acid mixture used for wet etching aluminum [40].

This short loop was used to fabricate the titanium buried mask for etching parylene. The parameters for coating, exposure, and development of the titanium mask were defined and several etch methods for the etching and removal of the buried mask were tested.

3.2.1 PROCESS

The short loop wafer scale fabrication of the Ti buried mask is illustrated in Figure 8. The fabrication was done on 4” single side polished silicon wafers (500 µm). The process began with the deposition of 400 nm of silicon dioxide (SiO_2) by plasma-enhanced chemical vapor deposition (PECVD) on the front side of the wafer.

Next, parylene was deposited using chemical vapor deposition (CVD). The amount of parylene dimer used for deposition was 7.25 g for a target layer thickness of 3 µm, which resulted in an actual thickness of 3.25 ± 0.15 µm across all five wafers. In order to improve the adhesion of the parylene layer to the SiO_2, an oxygen plasma treatment was done on the SiO_2 layer prior to and within one hour of parylene deposition, and the adhesion promotor A-174 silane was used as a primer for the deposition. As CVD results in a uniform layer over all exposed areas, the wafers have parylene on both the front and back sides.

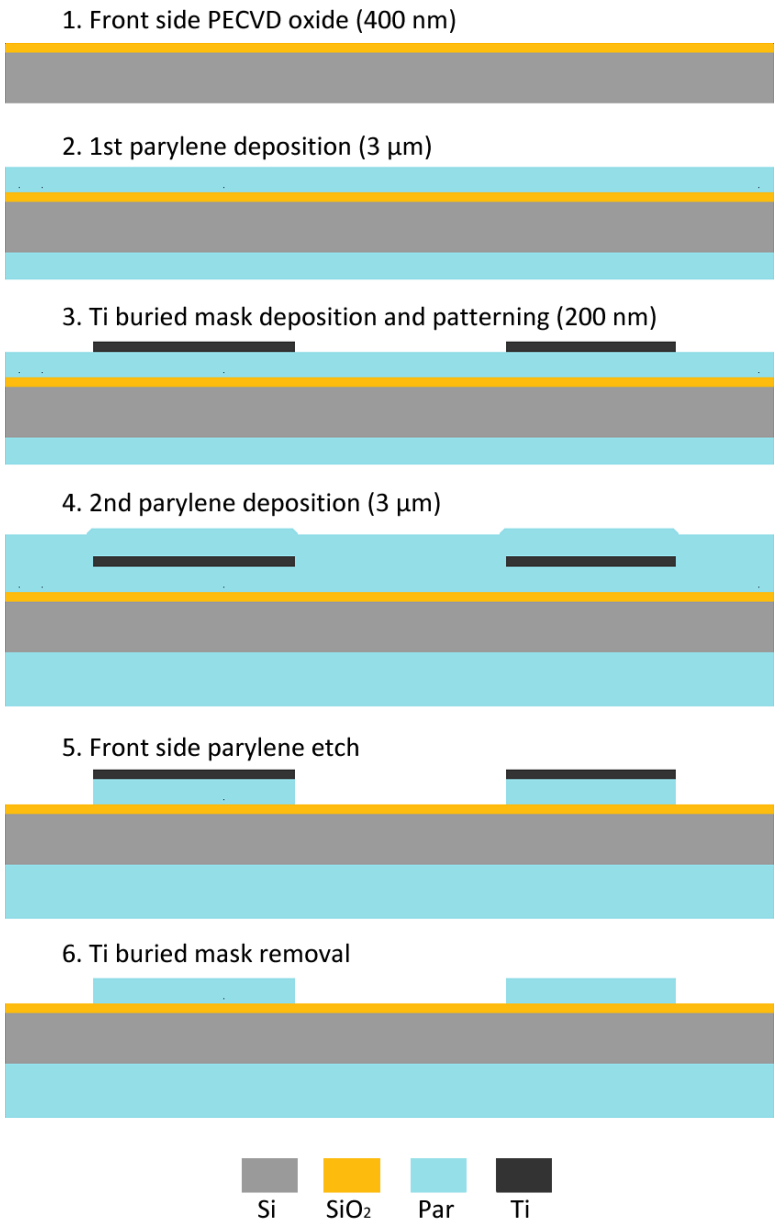


Figure 8: Ti buried mask short loop schematic.

A titanium layer of 200 nm was deposited on the front side of the parylene at 25°C as it was an existing titanium recipe at low temperature. Note that deposition using the Trikon Sigma 204 requires a carrier wafer to be used due to the parylene on the back side of the wafer.

The parylene on the back side of the wafer was then removed with an O_2 plasma etch in the Trikon Omega 201 using the recipe Par3 (O_2: 75.0 Sccm, CF_4: 5.0 Sccm, Power: 50 Watts). The Ti layer on the front side comes into contact with the chuck of the Omega during this step, so a test was performed to check that it is not damaged by scratches. The Ti layer will be used as a mask for the parylene etch, so damage to the layer may result in the parylene underneath the mask being etched. A particle measurement was run on the Ti layer using the REFLEX 300 Wafer Particle Measurement System before and after the plasma etch to detect any change in particles or scratches. The results may be seen in Figure 9, and indicate no significant difference in scratch numbers. The number of particles of size 0.172 µm increased, while the number of smaller particles decreased, but again, the change isn't

significant and the wafer will undergo cleaning. Thus, it was determined that the titanium layer is not damaged through contact with the chuck of the Omega.

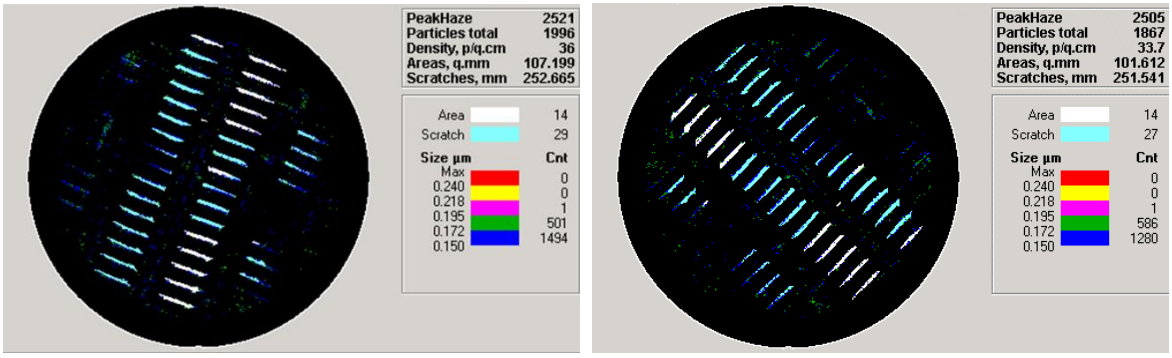


Figure 9: Scratch and particle count (a) before etch; (b) after etch.

Lithography and patterning were done on the titanium mask without exposing the wafer to high temperatures (above 100°C), and thus no recipes with the HMDS step done at high temperature may be used in the automatic coater. The mask chosen was a test mask with structures of varying sizes. AZ 3027 photoresist with thickness of 3.1 µm was used. Since the parylene layer on the back side of the wafer was removed in the previous step, the photoresist may be deposited automatically in the EVG 120 using the recipes "Only-SB on coater d" (a soft bake at 95°C for 80 seconds) followed by "Spec – 3027 – 3,1um – No HMDS no EBR" (3.1 µm of AZ3027 photoresist).

The exposure energy was set to 420 mJ/cm^2 with a focus of 0 µm. Development may be done automatically in the EVG 120 using the recipes "Only – SB – 3 min" (a bake at 95°C on a hot plate, used in place of the usual post exposure bake) and "1 – DEV – DP1 – No PEB". Again, this is to avoid exposing the wafer to high temperatures during the post-exposure bake or the hard bake. For the wafers intended to be wet etched, an extra bake was done in the Memmert convection oven at 80°C for 30 minutes to improve the adhesion of the photoresist to the Ti layer. This bake is not necessary for the wafers that will be dry etched. Note that after development, the sizing of the exposed masks was found to be 3 µm too large, indicating that the energy used for lithography is too high or the development was too long. However, the exposure energy and development was not optimized at this time, as the oversized structures were sufficient to continue the titanium buried mask short loop.

The titanium buried mask was etched using one of three methods: wet etching using a bath of hydrofluoric acid (HF), wet etching using the SC-1 etchant, and dry etching using the Omega recipe TinTiSVO (Cl_2: 30.0 Sccm, HBr: 40.0 Sccm, Power: 40 Watts). These methods are detailed in Section 3.2.2. The photoresist was removed using acetone spin cleaning, as the plasma strip cannot be used with parylene present on the wafers.

Photoresist residues were left on the edges of the structures after the photoresist was removed using acetone spin cleaning, as seen in Figure 10. However, this does not affect the parylene etch in later step, and the residues may be removed with a 1 min O_2 plasma etch.

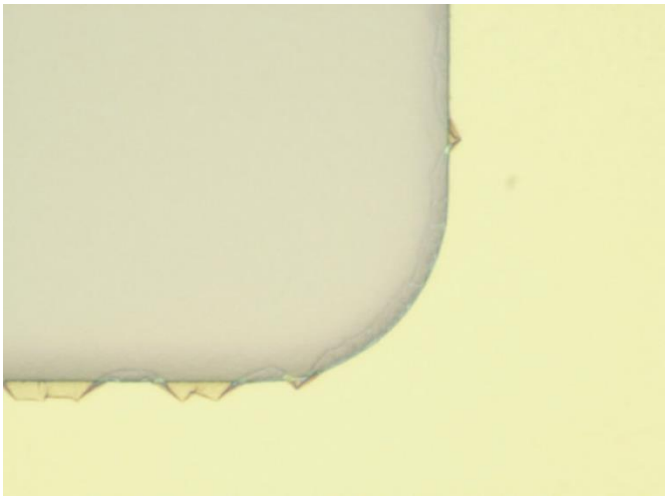


Figure 10: Photoresist residue film clinging to edges of structures.

A second parylene deposition of the same thickness of 3.25 ± 0.15 µm was done with use of the A-174 silane as a primer. Parylene to parylene adhesion is not be enhanced by the primer, but in the final process, there will be an exposed SiN layer on the back side. Furthermore, Kanhai's adhesion tests indicated that using A-174 would not decrease the adhesion of parylene to itself [35]. No oxygen plasma treatment was done prior to this deposition this time, as the O_2 plasma would etch the exposed parylene on the wafer. However, in later depositions, O_2 plasma would always be used, as it was determined that the etch rate of parylene is low enough that an O_2 plasma treatment for 1 minute will etch a negligible amount of the exposed parylene. This deposition was meant to mimic the second deposition in the final process that would serve to encapsulate the bottom of the device in parylene.

The parylene layers on the front side of the wafer were then etched in the Omega in one step using the recipe Par3 (O_2: 75.0 Sccm, CF_4: 5.0 Sccm, Power: 50 Watts). Parylene was etched all the way to the SiO_2 stop layer at locations where the Ti buried mask was opened. The first parylene layer was protected in the areas where the titanium mask remained.

Subsequently, the titanium mask was removed by wet etching in Ti etchant-1 for 3 minutes after a dip in Triton for 1 minute. Triton is used as a surfactant to decrease the surface tension on the etchant on the wafer, thus allowing for the clean etching of small structures [41].

3.2.2 Patterning of the Ti buried mask

In order to determine the best method of etching the titanium buried mask, three different methods were evaluated: wet etching using HF, wet etching using the SC-1 etchant, and dry etching using Cl_2: and HBr gasses.

3.2.2.1 HF Wet Etch of Titanium

The first method was to wet etch the titanium using a 0.5% hydrofluoric acid bath. Prior to the etch, the wafer was dipped into Triton for one minute. The wafer was then dipped in the HF bath until the Ti layer was visibly removed, which took 45 seconds, plus an overetch of 15 seconds for a total etch time of 1 minute. The wafer was rinsed in DI water for 20 minutes and examined under a microscope.

A thin grainy film was visible on top of the parylene through the microscope, which may be seen in Figure 11. The film was more prevalent near the edges of the wafer and can be seen clinging to the edges of structures in Figure 11. Returning the wafer to the HF bath for additional etching (up to 3 minutes) did not remove or cause any noticeable change to the film after the first water rinse, indicating that it is not pure titanium, as pure titanium would continue to be removed in HF. The film may be titanium trifluoride, which is produced from the reaction of Ti and HF, but TiF_3 decomposes in water and the film does not.

The photoresist was removed using acetone spin cleaning, and did not leave any of the residues seen in Figure 10.

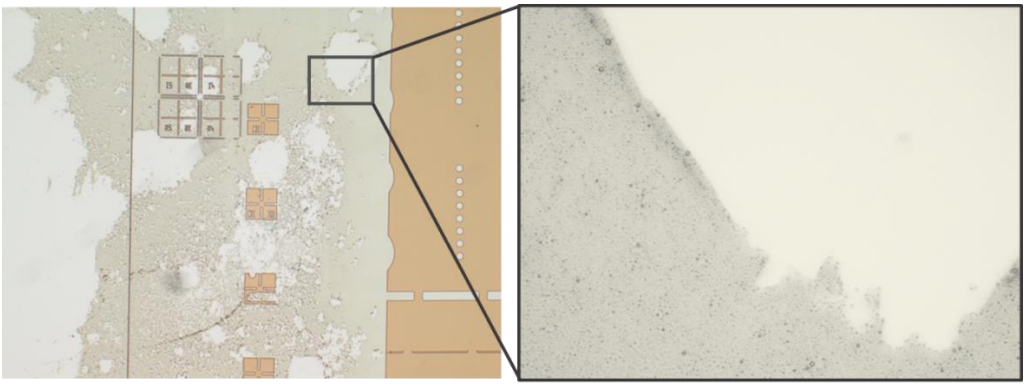


Figure 11: Film of Ti residue seen after HF etch on top of parylene around structures.

The film may be mostly removed by overetching in HF for 3 minutes continuously without stopping the etch with a rinse. However, this length of time causes the structures to be oversized by 8.1 um.

As HF is meant to be used for stripping Ti from a wafer rather than etching structures in controllable way, it was concluded that HF should not be used to etch the buried mask.

3.2.2.2 SC-1 Wet Etch of Titanium

The second method of wet etching was to use a solution consisting of 1 part H_2O, 1 part H_2O_2 31%, 1 part NH_4OH 28%. This etchant is the Standard Clean 1 (SC-1) solution used as part of the RCA clean procedure [42]. The wafer was dipped in Triton for 1 minute prior to the etch. The required etch time is variable based on the number of wafers etched and the age of the etchant. For a fresh batch of solution, it was found that 1.5 minutes was sufficient to etch the structures. Unlike the HF bath, SC-1 removed the Ti from the parylene cleanly, leaving no residues as seen in Figure 11.

The photoresist was removed using acetone spin cleaning, and did not leave any the residues.

Etching for too long results in uneven and cracked edges along the structures. The structures are also oversized by 2 µm. Figure 12 shows a comparison of a structure etched for 5 minutes versus a structure etched for 2 minutes.

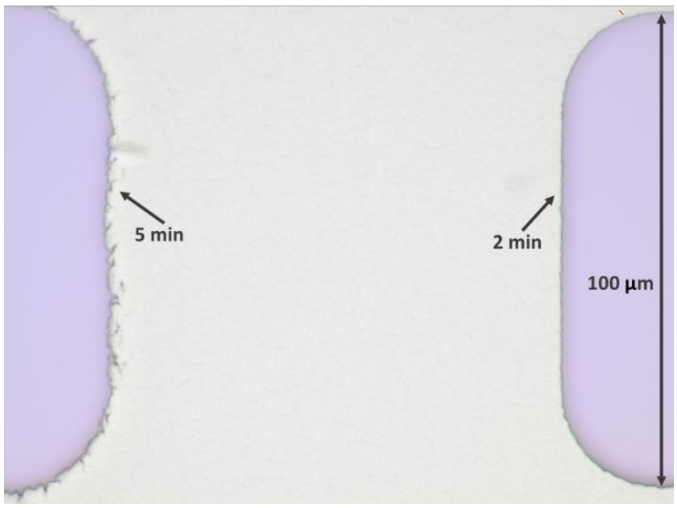


Figure 12: Structure edges after 5 minutes and 2 minutes in SC-1 etchant.

After the second parylene deposition and the parylene etch but before the removal of the titanium mask, a SEM inspection was done. As can be seen in Figure 13, the edges of the structures are jagged. The surface of the oxide also shows thread-like residues which are distributed evenly over the etched area, which can be seen in Figure 14.

Before the Ti mask was removed, a 5 minute O_2 plasma etch was done on the wafers that showed the threads on the oxide. However, the threads were not removed, indicating that they are not parylene that was micromasked by Ti residues. Acetone spin cleaning also did not affect the threads. It is possible that these threads are some titanium compound. However, in the final process, the parylene etch is the second to last step in the process, prior to the final step which is the removal of the Ti buried mask. The parylene etch will land on the metallization layer rather than on SiO_2, as the ceramic encapsulation is already open on the bond pads. No further time was spent on the identification or removal of the threads, since there may not be residue when the etch lands on a different material.

It was concluded that SC-1 is a viable way to pattern Ti, but careful monitoring must be done of the etch times.

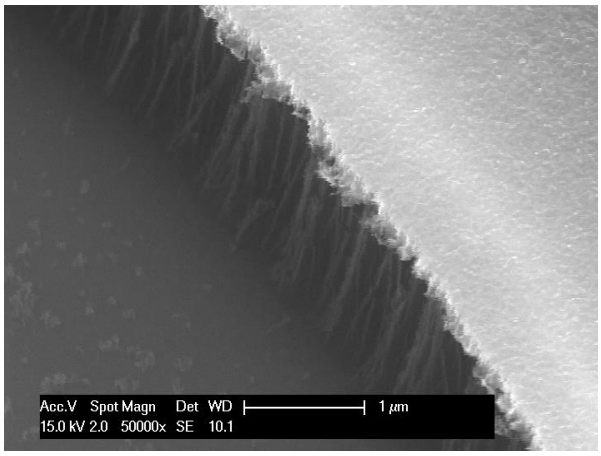


Figure 13: SEM photo of wet etched Ti edge.

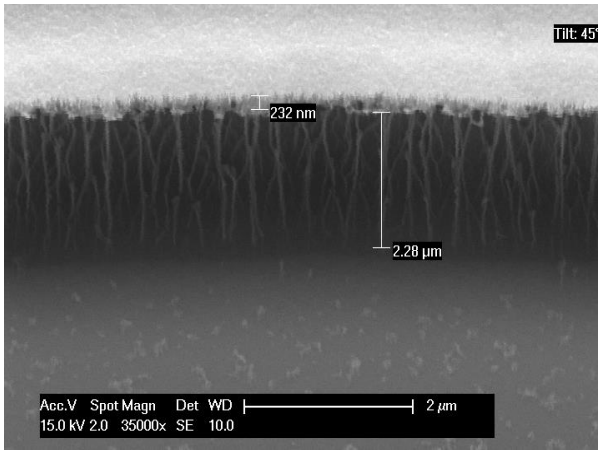


Figure 14: SEM photo of wet etched structure sidewalls with visible residues on SiO_2.

3.2.2.3 Omega Dry Etch of Titanium

The third method of etching was to plasma etch the titanium layer in the Trikon Omega 201 using the recipe TinTiSVO (Cl_2: 30.0 Sccm, HBr: 40.0 Sccm, Power: 40 Watts).

The structures were not opened fully after 2 minutes of etching. As can be seen in Figure 15, the edges of the structures still show residues of titanium on top of parylene. At the time, due to inconsistency with Omega performance and lack of availability, the Ti residues were removed with wet etching. The wafer was treated with Triton and wet etched in SC-1 for 30 seconds. However, the plasma etch should be used to etch the Ti mask fully in future process flows to avoid the extra unnecessary wet etch step.

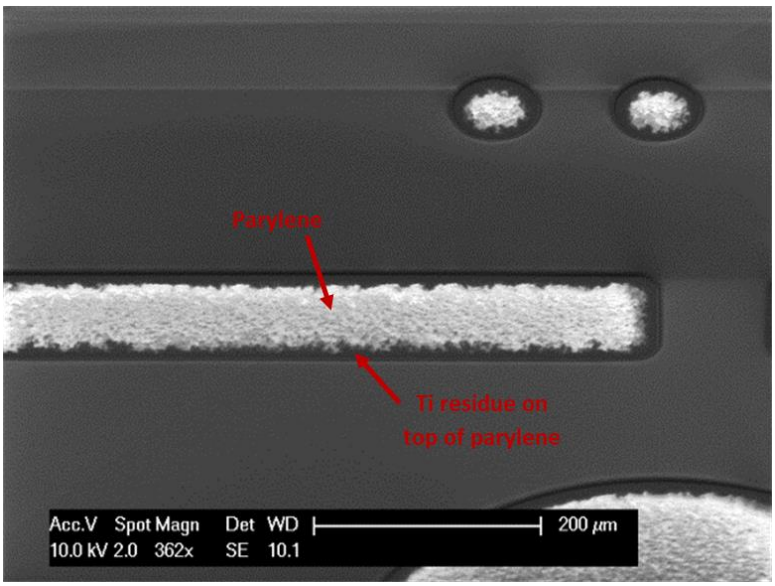


Figure 15: SEM photo of Ti residue around the edges of structures.

After the exposed parylene is etched, the SEM photos in Figure 16 show that the edges of the Ti structures are cleaner and more even than the Ti mask etched with SC-1. Again, the wafer shows threads at bottom of the structures, on the oxide surface.

The Ti layer was removed cleanly from parylene using SC-1.

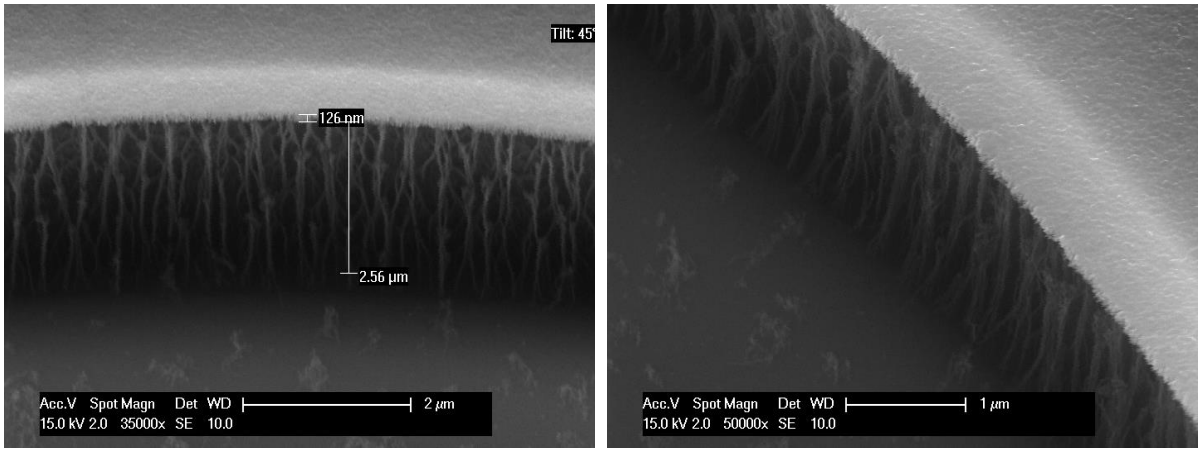


Figure 16: SEM photo of (a) dry etched structure sidewalls and (b) Ti mask edge.

3.2.3 Conclusion

It was concluded that a layer of 200 nm of titanium deposited using sputtering at 25°C may be used as a buried etch mask for parylene. The lithography parameters for the Ti mask were tested and found to produce a functional mask, though future work should reduce the exposure energy to prevent oversized structures. Due to time limitations, the appropriate exposure energy was not found, though based on the patterning of other metallic layers of similar thickness, an energy of 150 mJ/cm^2 is suggested.

Plasma etching produces the best results for the Ti hard etch mask, as etching the Ti layer in SC-1 produces jagged edges on the structures. By contrast, plasma etching produces even structure edges, but may require a dip in SC-1 to remove Ti residues if they are left on the surface of the parylene. The titanium buried mask maybe be removed cleanly from parylene using the SC-1 solution. The wafer should be dipped in Triton prior to any wet etching to ensure small structures are etched.

3.3 Aluminum Stop Etch Layer

The purpose of the aluminum etch stop layer is to protect the ceramic encapsulation layers from being etched when the silicon oxide stop layer is removed from the back side after the DRIE. Aluminum was chosen for the etch stop material as it is resistant to the dry etch that will be used to remove the SiO_2 layer, and, as previously mentioned, removal of the aluminum via wet etch will not affect the titanium buried mask. Pure aluminum is chosen over aluminum silicon since pure aluminum provides better masking, and may be removed more easily as wet etching will not leave silicon grain residues.

This short loop is used to define the most suitable thickness and deposition temperature for the aluminum stop etch layer. The layer should be pinhole-free, thus its thickness should be sufficient to protect the ceramic layers from the ion bombardment of the oxide plasma etch. However, the aluminum layer will eventually be wet etched from the bottom of deep DRIE structures, so the thickness should be thin enough that all aluminum can be removed without too long of an etch. The deposition temperature may also have an effect on the presence of pinholes, as deposition at higher temperatures will result in a layer with larger metal grains and potentially more pinholes. Thus, both thickness and deposition temperature of the Al deposition are varied.

3.3.1 PROCESS

The fabrication of the aluminum etch stop short loop is illustrated in Figure 17. The fabrication was done on five 4" single side polished silicon wafers (500nm). The process began with the deposition of 400 nm of silicon dioxide (SiO_2) by PECVD on the front side of the wafer.

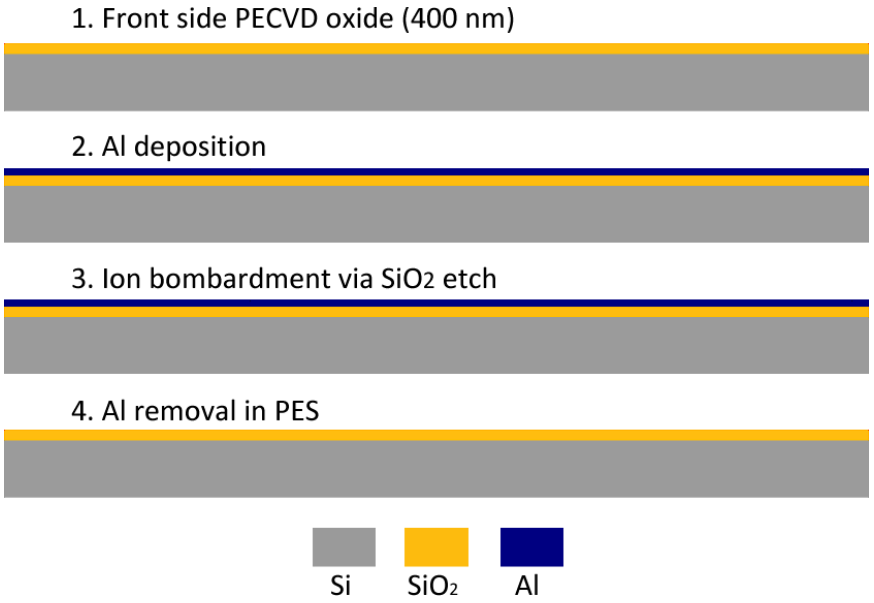


Figure 17: Aluminum etch stop layer short loop schematic.

For each one of the five wafers, a layer of sputtered Al was deposited using the Sigma. For this trial, the layers were chosen based on the existing recipes in the Sigma, with the variable parameters being the thickness of the layer and the deposition temperature. The deposited layers can be seen in Table 2.

Table 2: Thickness and deposition temperature of Al on test wafers

Wafer #	Al Thickness [nm]	Deposition Temp [°C]
1	60	25
2	100	350
3	200	25
4	200	300
5	250	50

The wafers were then etched in Drytek for 5 minutes using the stdoxide recipe (C_2F_6: 36.0 CC/sec, CHF_3: 144.0, Power: 300 Watts). The etch rate of silicon oxide using this recipe is 600 nm/min. The time to etch 400 nm of SiO_2 is theoretically 40 seconds, so there is an overetch time of 4.33 minutes. By etching for an excessive amount of time, it can be seen whether or not aluminum etch stop layer has any pinholes by examining the SiO_2 layer for defects. If defects are not present, the aluminum layer is sufficient protection for the SiO_2 layer, and can be used as an etch stop layer.

Note that in the final process, the layer protected by the Al etch stop will be SiN, but SiO_2 is used in this short loop as the etch rate of SiO_2 is faster than the etch rate of SiN in the Drytek, and therefore this layer is more sensitive to the etch through any pinholes, if they are present.

Following the plasma etch, the wafers were dipped in Triton for 1 minute and the Al layer was removed by wet etching in PES at 35°C until the Al was cleanly removed from the oxide (about 6 minutes). The theoretical etch rate is 220 nm/min, so the wet etching took longer than expected.

3.3.2 RESULTS

The oxide layer was inspected under the SEM for defects. For wafers 4 (200 nm at 300°C) and 5 (250 nm at 50°C), the wafers were given a scratch as an induced defect to provide a structure for SEM focusing. The particles caused by the induced defect charge under the SEM, resulting in some blurred photos, but with sufficient zoom it can be seen whether or not there are pinholes. The images from the SEM may be seen below.

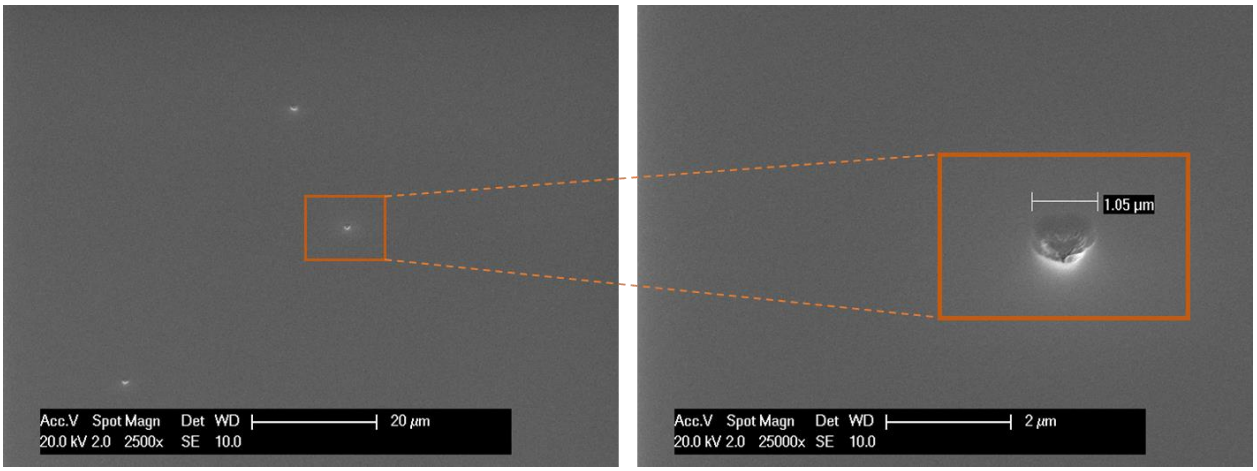


Figure 18: Wafer 1 (60 nm at 25°C) – rare defects of ~1um.

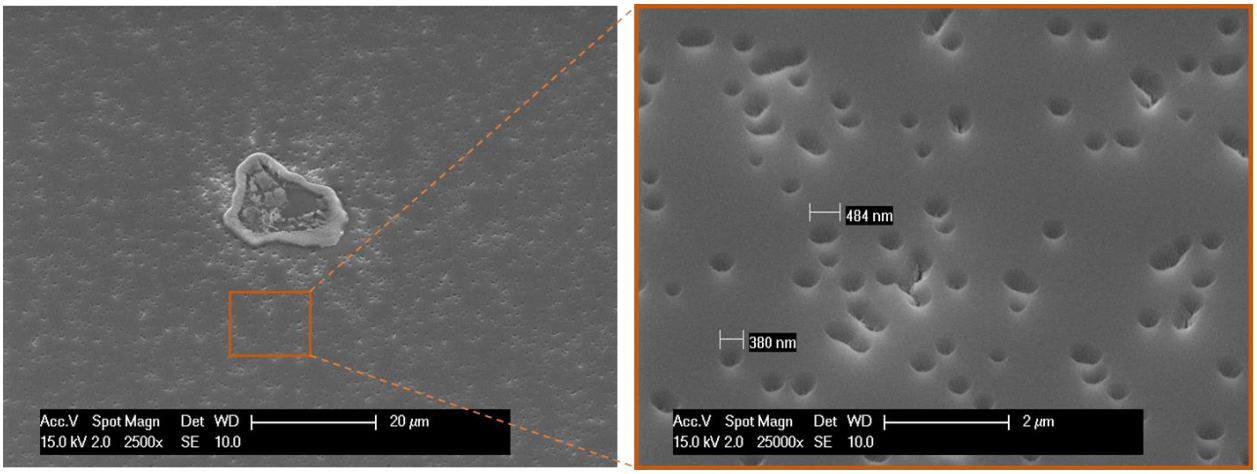


Figure 19: Wafer 2 (100 nm at 350°C) – frequent defects of ~400nm.

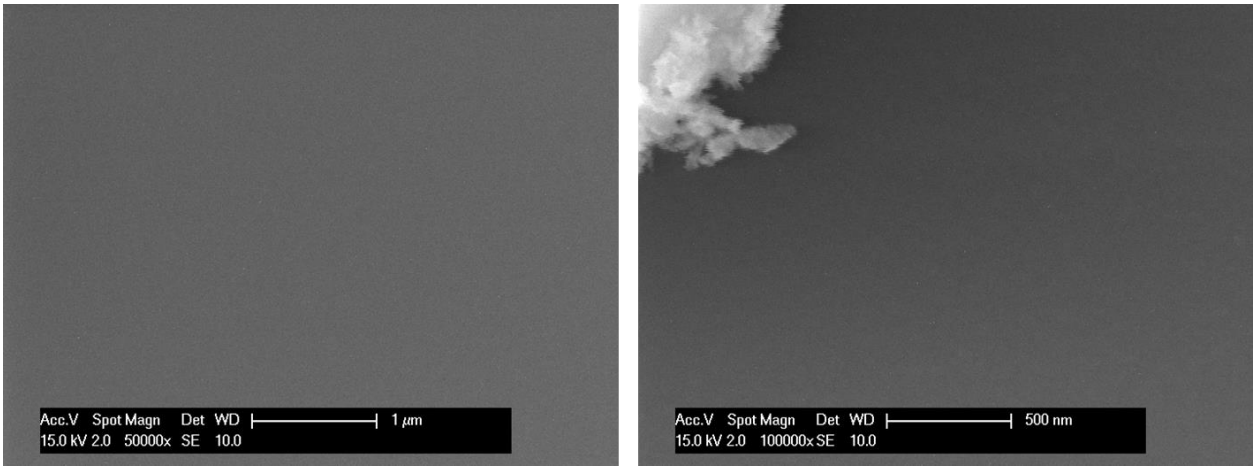


Figure 20: Wafer 3 (200 nm at 25°C) – no defects.

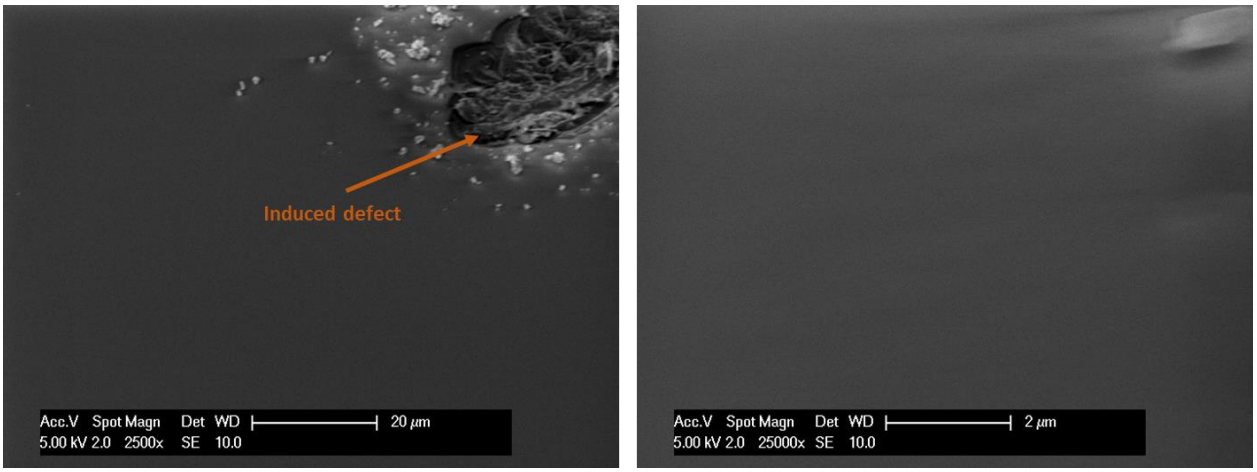


Figure 21: Wafer 4 (200 nm at 300°C) – induced defect and charged particles, no defects.

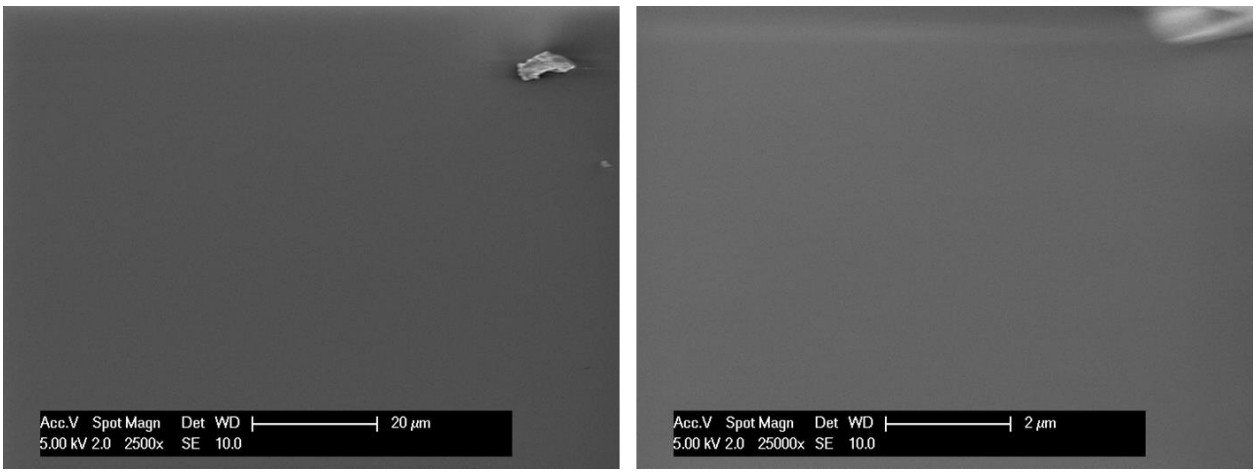


Figure 22: Wafer 5 (250 nm at 50°C) – induced defect and charged particles, no defects

From Figure 18, it can be seen that a layer of 60 nm is not pinhole-free and therefore too thin to serve as a stop etch layer. It will result in defects in the oxide or nitride layer underneath the aluminum. Figure 20 and Figure 21 show that 200 nm of aluminum will result in no defects in the

oxide, whether the deposition is done at low or high temperature. Figure 22 also shows that a thicker Al layer of 250 nm results in no pinholes.

From Figure 19, many defects were visible in the wafer that was protected by 100 nm of Al deposited at high temperature. It is possible that 100 nm deposited at low temperature would prevent pinholes in the oxide as the smaller grain sizes of the aluminum would cause fewer pinholes. However, in the final process, the process step after the deposition of the Al stop etch layer is the deposition of SiN at a high temperature (400°C), which would expose the Al layer to high temperatures and cause annealing of the Al anyway, causing the same effect as 100 nm of Al deposited at high temperature. The full table of deposition parameters and results may be seen in Table 3.

Table 3: Results of SEM inspection for different Al deposition conditions

Wafer #	Al Thickness [nm]	Temp [C]	Result
1	60	25	Showed rare defects of ~1um; layer is too thin
2	100	350	Many defects of ~400nm; 100nm may be viable if dep. at low temp
3	200	25	No defects visible
4	200	300	No defects visible
5	250	50	No defects visible

3.3.3 Conclusion

For the final process, 200 nm of aluminum deposited at 300°C was chosen as an etch stop layer, since it is thin enough to be easily removed. Furthermore, no changes to the Al layer due to temperature should occur during the next step, which is SiN deposition at high temperature.

3.4 Titanium Nitride as Metallization Material

Due to the difficulties in using platinum as part of the process flow, titanium nitride was used as a substitute for the metallization. The following section covers the deposition parameters of TiN and the compatibility of using TiN as a metallization material in the final process flow.

3.4.1 TiN Deposition Conditions

In order to determine good deposition conditions, several versions of the standard TiN deposition recipe used in Else Kooi Lab were made and variations of deposition power and nitride concentration were tested. Thickness was kept at 200 nm as previous experiments showed that a layer less than 100 nm had pinholes, and a layer thicker than 300 nm would cause buckling due to stress.

The details of the recipes tested are listed in Table 4. The layer of TiN was deposited on SSP wafers with 400 nm SiO_2 on the front side. Note that all TiN depositions include an underlying layer of 10 nm of Ti for adhesion.

Table 4: Deposition conditions of TiN and the resulting sheet resistance and stress

	Deposition Parameters				Measurements	
Recipe name	Thickness [nm]	Ar [%]	N2 [%]	Power [kW]	Sheet Resistance [Ω/sq]	Stress [MPa]
Ti10_TiN200_STD_6kW	200	20	70	6	16.41 ± 0.21	212
Ti10_TiN200_1kW_350C	200	20	70	1	84.36 ± 1.42	213
Ti10_TiN200_LowN350C	200	54	36	6	2.67 ± 0.23	517

From these results the standard recipe, Ti10_TiN200_STD_6kW, was chosen, as it has a lower stress of 212 MPa than the wafer sputtered with low N_2 concentration and lower sheet resistance of 16.41 ± 0.21 Ω/sq compared to the wafer deposited at low power. The main process flowchart was continued using these deposition conditions for TiN.

3.4.2 Effects of SC-1 Wet Etch on TiN

As the final process flow was originally developed for platinum electrodes, using TiN causes some problems in the fabrication. The biggest issue is that the bond pads of the TiN electrode are exposed during the step in which the Ti buried mask is wet etched in SC-1, and therefore will also be etched.

A test was done to check the effects of SC-1 on TiN. Two SSP wafers with 400 nm SiO_2 on the front side had 200 nm TiN deposited on them using the standard recipe. The sheet resistance was measured on both and found to be ~16 Ω/sq. One wafer was etched in a fresh batch of SC-1 for 6.5 minutes, rinsed, and the sheet resistance was measured again. The second wafer would undergo the same process, but after the SC-1 has been aged for 24 hours, as it was found that the etch rate of TiN in the aged solution would decrease.

The results may be seen in Table 5. Both wafers still have TiN on the surface and are still conductive after 6.5 minutes of etching, indicating that the etch rate of TiN was slower than that of Ti (a 200 nm layer of Ti is fully etched in 3 minutes in fresh SC-1). The wafer etched in the fresh SC-1 solution showed a greater average R_s of 235.46 Ω/sq, indicating that the layer is thinner. The variation in thickness of TiN across the wafer is also greater, represented by a larger standard deviation of 121.11 Ω/sq over the wafer after the etch. The etching of TiN was less drastic in the aged solution so as a temporary measure to preserve the electrode bond pads, the SC-1 etch in the final step of the process flow would be aged.

Table 5: Sheet resistance measurements of TiN layer before and after 6.5 minute etch in SC-1

SC-1 Age	Avg. Rs before etch (Ω/sq)	Avg. Rs after etch (Ω/sq)
Fresh (0 hr)	15.43 ± 0.15	235.46 ± 121.11
Aged (24 hr)	17.11 ± 0.20	134.43 ± 13.43

The effects of the aged SC-1 solution was tested on a test wafer that did not undergo the back side DRIE step and did not have flexible membranes. On the test wafer, both the Ti buried mask and the TiN electrode bond pads are exposed. The test wafer was etched until the Ti layer was removed. The resistance between the bond pads connecting the meander structure was measured before and after on several die with a digital multimeter and the resistance increased slightly from ~175 kΩ to 176 kΩ. Visual inspection showed that the TiN underneath the parylene is being etched away or

delaminating, as can be seen in Figure 23(a). Also visible on the bond pads are uneven spots of varying color, which can be seen in Figure 23(b). As these spots were not seen prior to the TiN wet etch, it is likely they show areas with uneven TiN thicknesses. The finished device is still conductive and can be used for electrical testing, but the undercut may have an impact on adhesion during reliability testing.

Again, as the final device uses Pt electrodes rather than TiN, this issue was not investigated further.

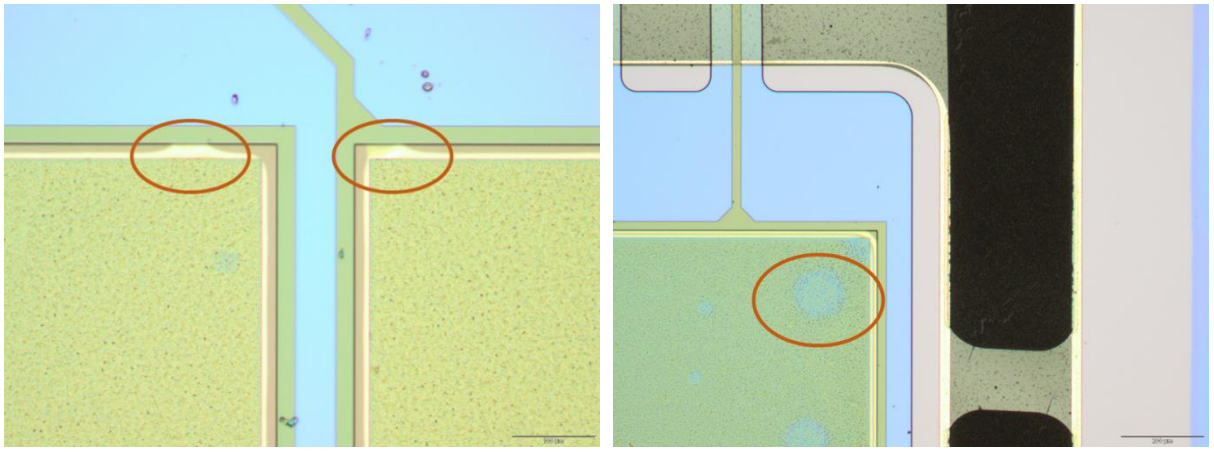


Figure 23: (a) Visible etching or delamination of TiN layer beneath the parylene encapsulating layer indicated; (b) Visible uneven spots on the TiN bond pad indicated.

3.4.3 Conclusion

Titanium nitride was chosen as a substitute for metallization material in place of platinum. The standard deposition parameters for reactive sputter deposition of TiN used in EKL was chosen as it showed the lowest layer stress and sheet resistance of the layers tested.

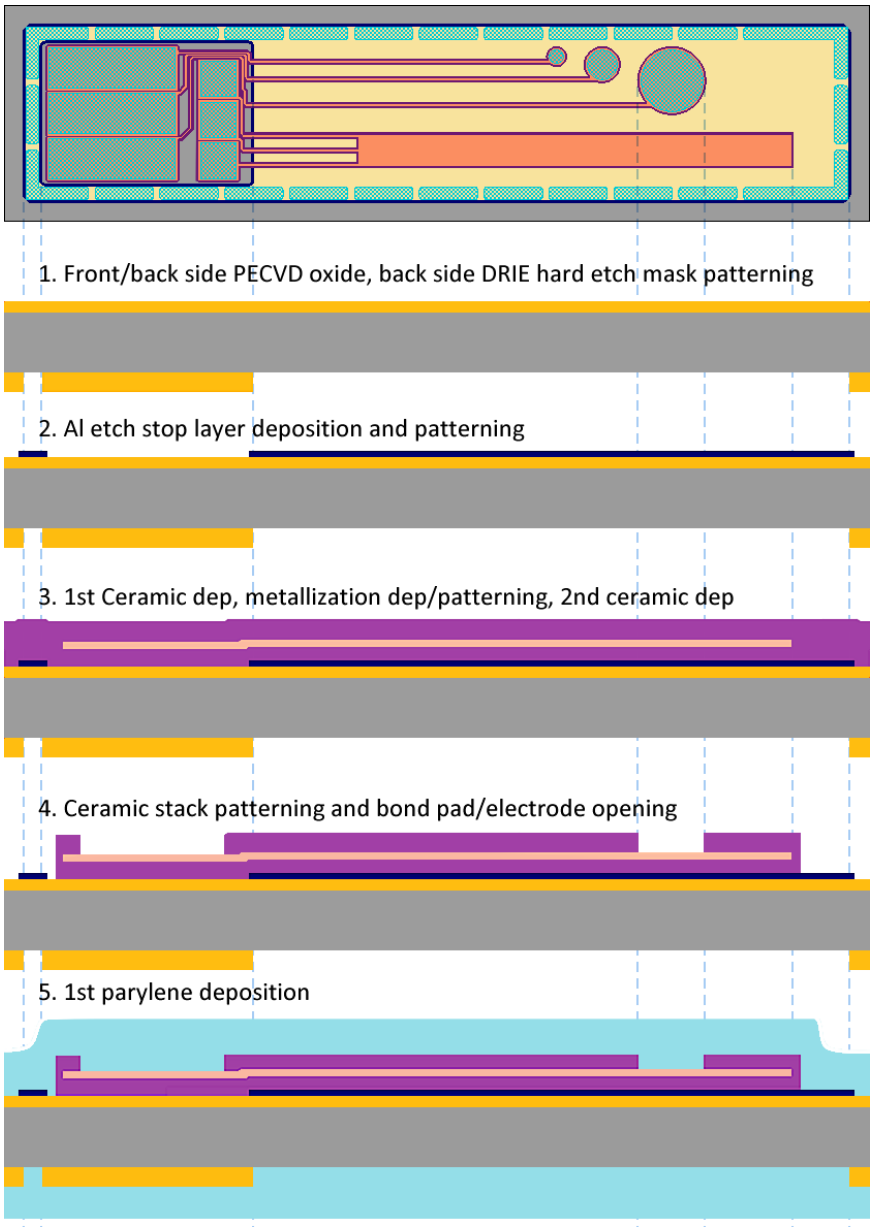
The process flow was not designed with titanium nitride as the metallization. There are certain steps that are not compatible with TiN, most notably the final removal of the titanium buried mask via wet etching. However, it was confirmed that for the purposes of this project, using TiN would still produce a device that can undergo evaluation testing.

4 DEVICE FABRICATION

In this chapter, the fabrication process for the TiN based device will be presented. The masks and technology modules introduced in the previous chapters are incorporated into the process flow, which may be divided into the main process steps: back side DRIE mask, etch stop layers patterning, ceramic encapsulation and metallization, first parylene encapsulation and buried mask patterning, device release via DRIE and etch stop removal, second parylene encapsulation and opening of structures, and final device release via cutting.

4.1 WAFER BASED FABRICATION FLOWCHART

The fabrication process for the device composed of electrodes and comb-meander structures is illustrated in Figure 24. Fabrication was done on 4" double side polished silicon wafers (400 µm thick).



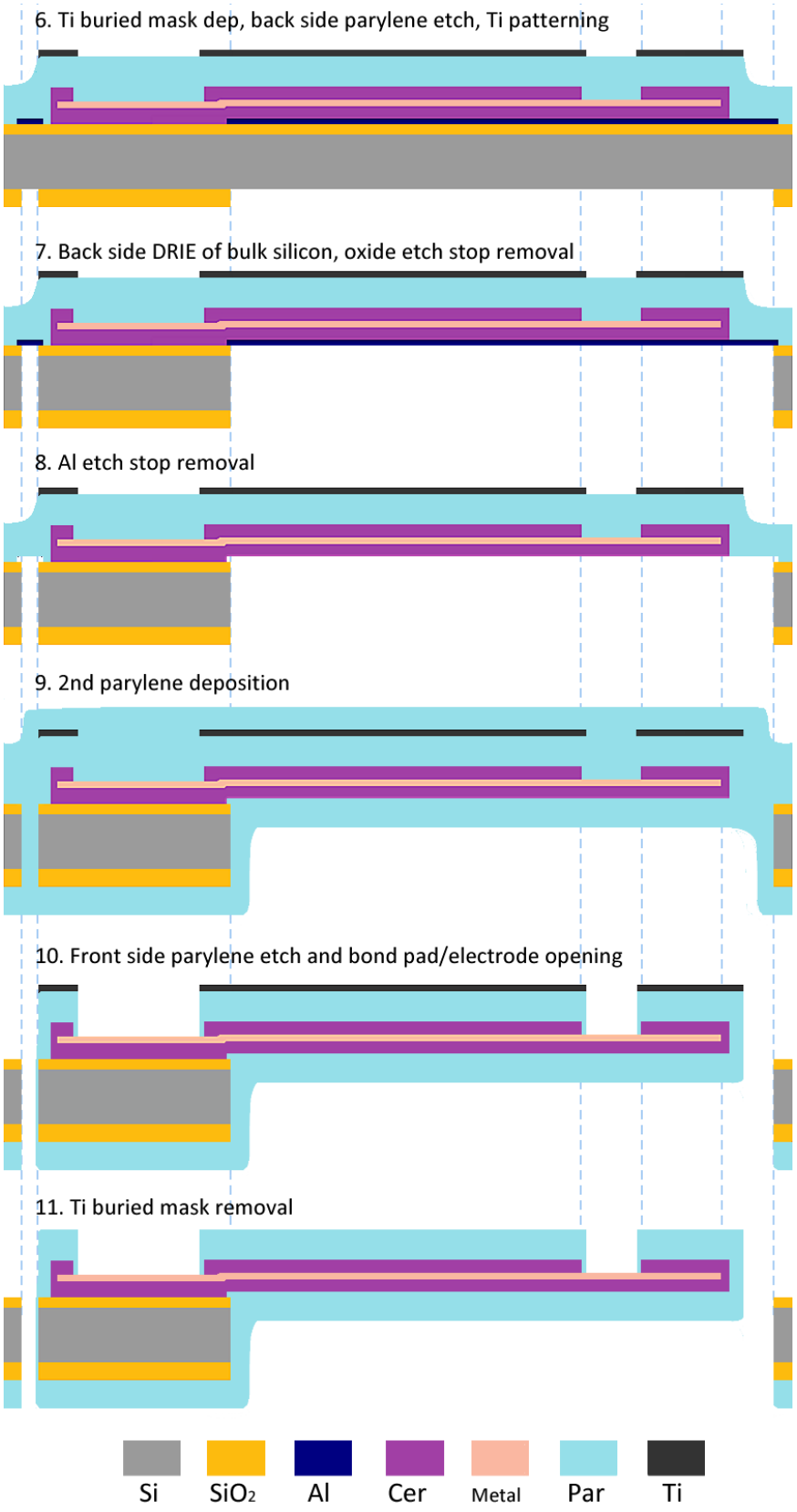


Figure 24: Simplified schematic flow of the full process.

4.1.1 Back Side DRIE Hard Mask and Front Side Etch Stop Layers (Steps 1 – 2)

The process began with the deposition of 6 µm of SiO_2 on the back side of the wafer for the back side DRIE hard mask and 400 nm of SiO_2 on the front side as an etch stop layer for the DRIE, and as an insulating layer on the silicon island, using plasma-enhanced chemical vapor deposition (PECVD). The back side SiO_2 was patterned with the release mask. This is shown in step 1 of Figure 24.

In step 2 an aluminum etch stop layer of 200 nm was deposited on the front side of the wafer using sputtering at 300°C. The etch stop layer was patterned and dry etched in the Omega using a three step recipe with the first step having parameters Cl_2: 30.0 Sccm, HBr: 40.0 Sccm, Power: 50 Watts, the second step having parameters Cl_2: 30.0 Sccm, HBr: 40.0 Sccm, Power: 40 Watts, and the last step having parameters Cl_2: 30.0 Sccm, N: 7.0 Sccm, Power: 0 Watts.

The Al mask must be large enough to cover the area that is exposed after the DRIE and SiO_2 etch stop removal in order to protect the ceramic encapsulation layer, but it should not extend too far underneath the bulk Si as it must be fully removed in the wet etch process in step 8. On a previous short loop, the sidewalls from the Rapier DRIE show negative sloping of 1.5° when visually inspected using the SEM. Based on this measurement, it was determined that the aluminum etch stop layer would be the same shape as the release mask expanded by 20 µm.

4.1.2 Ceramic Encapsulation and Metallization (Steps 3 – 4)

The first two layers of the ceramic stack, comprised of 50 nm SiN with 400 nm SiO_2 on top, were deposited using PECVD. The metallization layer for the electrodes was then deposited, patterned, and etched. The material chosen for the electrodes was intended to be 600 nm platinum in the final process flow. Titanium nitride electrodes etched from 200 nm of TiN with a 10 nm layer of Ti beneath the TiN for adhesion were also fabricated. The latter were originally to be used as test wafers, but due to the unavailability of certain platinum-processing machines, it became unfeasible to continue the process flow with platinum, and the processing of the wafers with Pt metallization stopped after deposition of the Pt layer.

For the wafers with TiN metallization, the TiN layer was deposited according to the parameters chosen in Section 3.4.1 and patterned with 1.4 µm of photoresist. The TiN layer was etched in the Omega with the recipe TinTiSVO (Cl_2: 30.0 Sccm, HBr: 40.0 Sccm, Power: 40 Watts). The etch rate was estimated to be 3 nm/s for TiN.

The top part of the ceramic stack was then deposited via PECVD and consists of 15 nm of SiN followed by 400 nm of SiO_2 followed by a final layer of 50 nm of SiN. The device at this stage can be seen in step 3 of Figure 24.

With the electrode metal lines fully encapsulated in ceramic, the ceramic layers were patterned. The resist thickness was 2.1 µm to account for the topography, which is ~1 µm in total at this point. The etch was done in the Alcatel using the standard oxide etch recipe (CF_4: 50.0 Sccm, CHF_3: 25.0 Sccm, He: 40.0 Sccm, Power: 60 Watts). The Alcatel was chosen as the bond pads of the electrodes are opened during this step, as can be seen in step 4, and if the metallization were platinum, contamination may be caused in some machines such as the Omega.

The first short loop that followed the major steps of the final loop was done entirely using masks from Kanhai's design, which did not include the masks for patterning the Al etch stop layer and the

ceramic encapsulation. Thus, these two layers remained as unpatterned layers in the trial device resulting from this short loop. Difficulties were encountered when releasing the device along the perforated edges due to the parylene and ceramics not being etched through fully. The stress in the thin ceramic film caused the membrane to tear during release along the edges of the device, especially at the edge of the silicon island, as seen in Figure 25.

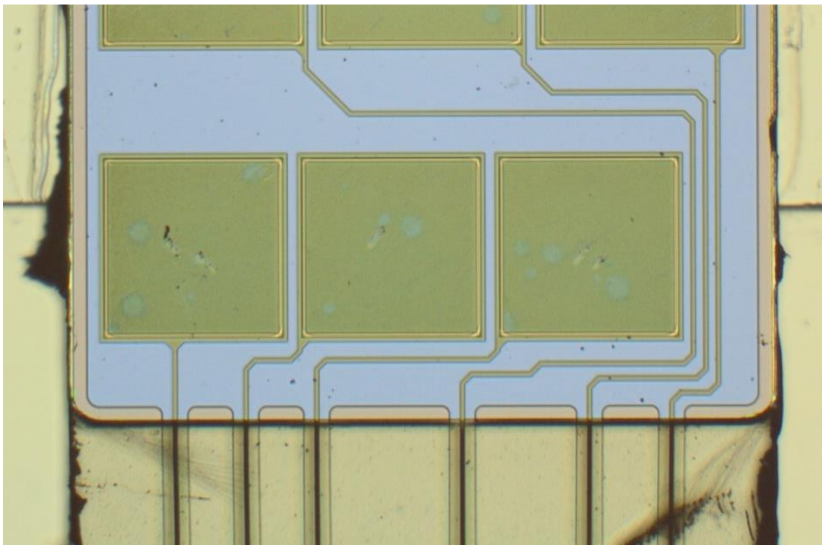


Figure 25: Location of where cracks spread from the corners of the silicon island where the edge meets the parylene membrane. Note that this image is of a device made with the rounded back side DRIE hard etch mask and not the prototype device.

In order to solve the tearing problem, the corners of the silicon island were rounded and the thickness of the parylene layers were increased to 6 µm for each deposition, up from the 3 µm used in the trial device. These changes, along with the patterned ceramic layers allowing the perforated parylene tabs to be fully etched through, solved the problem of the membranes tearing at the edges. The final device can be easily cut from the silicon frame.

4.1.3 First Parylene Layer and Ti Buried Mask (Steps 5 – 6)

The first parylene C deposition was done using Chemical Vapor Deposition (CVD) following an O_2 plasma treatment (1 minute at 600 Watts) to remove organic contaminants and enhance adhesion. Ideally, to avoid removing hydroxyl groups from the surface of the exposed silicon nitride, the plasma treatment should be of low power (less than 400 Watts). The deposition must be done within one hour of the plasma treatment. A-174 silane adhesion promoter was used for this deposition to improve the adhesion of parylene to the exposed SiN encapsulating layer. The amount of parylene dimer used was 13 g, which corresponds to a parylene layer of thickness 6 µm ± 0.5 µm. The thickness deposited on the wafer varies depending on which slot in the machine the wafer occupied, with the top wafer having the thickest layer. The wafer after the parylene deposition is shown in step 5.

The Ti buried mask is deposited and patterned using the parameters determined in the Ti buried mask short loop (see section 3.2). A 200 nm thick layer of titanium for the buried mask was deposited at 25°C on top of the parylene on the front side. A carrier wafer must be used for the deposition in the Sigma due to the parylene layer on the back side of the wafer.

The back side layer of parylene was then removed in the Omega using the recipe Par3 (O_2: 75.0 Sccm, CF_4: 5.0 Sccm, Power: 50 Watts). The Ti buried mask was patterned with a 3.1 µm layer of resist and dry etched using the recipe TiNTiSVO (Cl_2: 30.0 Sccm, HBr: 40.0 Sccm, Power: 40 Watts). The photoresist used to pattern the Ti was removed using acetone spin cleaning, as an O_2 plasma treatment long or powerful enough to strip the resist would also etch the parylene. Any PR residues clinging to the edges of the structures were removed with a one minute plasma etch in the Alcatel using the parylene etch recipe (O2 plasma: 70 sccm, Power: 60 Watts). The device at this point is shown in step 6.

For a future version of the mask, note that the Ti buried mask overlaps the DRIE area by 8.4 µm, as seen in Figure 26, and the openings are already oversized by 3 µm from either too high an exposure energy (420 mJ/cm^2) or the development time being too long. Due to the sidewalls of the DRIE etch being at an angle, the Ti buried mask needs to be increased in size around the release opening lines by 11.4 µm, or the DRIE sidewall profile needs to be changed.

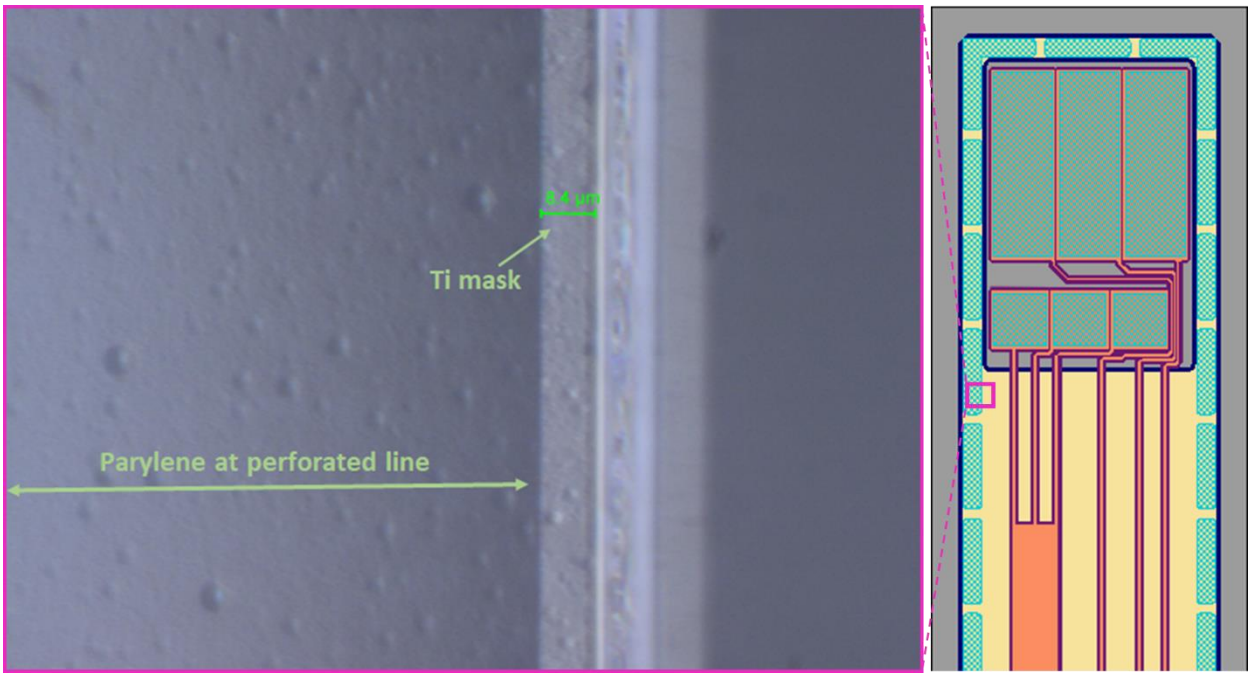


Figure 26: Ti buried mask for parylene etch overlapping the released area.

4.1.4 Back Side Release – DRIE and Stop Etch Layer Removal (Steps 7 – 8)

The bulk silicon was etched from the back side in the Rapier Omega i2L DRIE etcher, using the 6 µm SiO_2 back side DRIE hard mask deposited in step 1. The etch is finished when the 400 nm thick SiO_2 etch stop layer, deposited in step 2, is reached. To ensure high yield and prevent the membranes from breaking, the newly designed back side DRIE mask with rounded silicon structures was used. If platinum is used as metallization, extra steps must be taken during the DRIE to prevent contamination of the Rapier chuck. This process is detailed in Appendix A.1.

The SiO_2 layer was then dry etched from the backside using the Alcatel plasma etcher with the standard oxide recipe, as the Alcatel does not use clamping on the wafer, which may damage the membranes. The Al etch stop etch layer was removed by wet etching in PES at 20°C for 6 minutes. A long (1 hour) dip in the surfactant Triton is necessary as there are deep and hard to reach structures

from which the Al must be removed. After the Al wet etch, the wafer is rinsed in DI water for a minimum of 20 minutes.

As can be seen in Figure 27, the sidewalls of the bulk silicon show a negative slope of 1.5° after the DRIE. During fabrication of the final device, after the SiO_2 etch stop layer was removed (step 7 in Figure 24), it appeared that this Al etch stop sizing entirely covered any SiN that may be exposed. However, due to the titanium buried mask on the front side, it was not possible to check how far the Al extended underneath the bulk silicon until the Ti mask was removed. Upon inspection after step 11 in Figure 24 using optical microscope, it was found that aluminum was still on the device after the Al wet etch. As can be seen in Figure 28, the uneven edge of the Si island etched by DRIE can be seen from the front side. There is a gap, and the remaining Al edge.

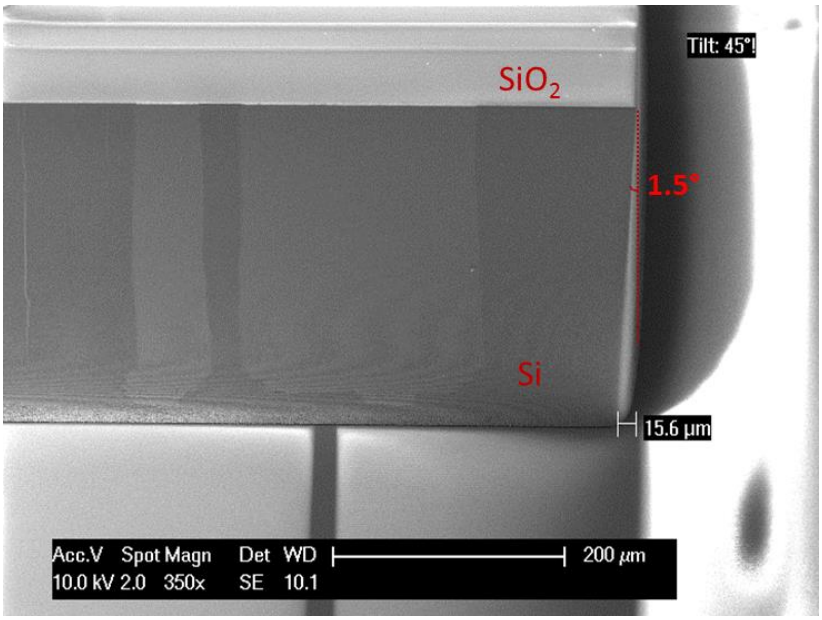


Figure 27: SEM photo showing negative sloping when bulk silicon is etched.

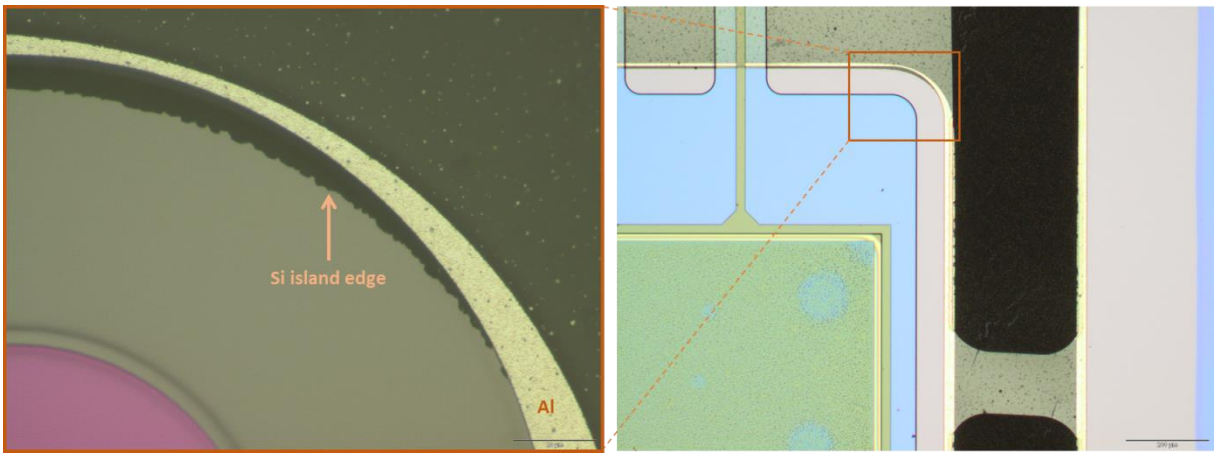


Figure 28: (a) Gap between DRIE silicon island and remaining Al etch stop; (b) Gap between DRIE silicon and Al etch stop zoomed out.

The Al remaining unetched after the PES bath is due to the SiO_2 layer between the bulk Si and the Al etch stop, which is dry etched from the back side after the DRIE using the Alcatel plasma etcher. As the plasma etch is anisotropic, the back side of the silicon island will mask some of the SiO_2 (Figure

29(a)). This results in a layer of SiO_2 that extends farther than the area opened by DRIE (Figure 29(b)), which then masks the wet etch of the Al layer. As can be seen from Figure 29(c), the gap between the Si island edge and the remaining Al shown in Figure 28 is part of the 400 nm SiO_2 etch stop layer.

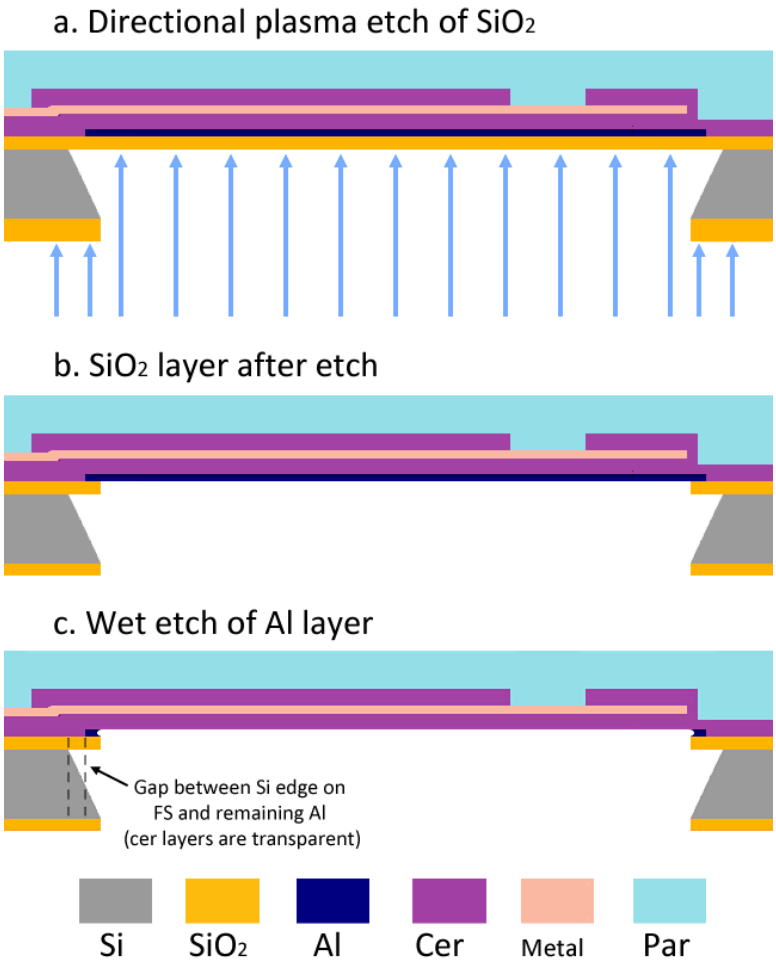


Figure 29: (a) Direction of dry etch to remove SiO_2 layer after DRIE (Step 7 in the full flowchart); (b) Al etch stop layer exposed after SiO_2 is etched; (c) the device after Al wet etch, with the location of the gap between Si edge and visible Al indicated. Angle of Si sidewalls is exaggerated.

In order to prevent Al from remaining after the wet etch, a DRIE recipe with straight sidewalls could be developed, or a more isotropic method of etching of SiO_2 could be used. In this flow, BHF wet etch cannot be used as the Ti buried mask is exposed on the front side and HF will strip Ti. The size of the Al stop etch layer could also be modified, as its sizing was not optimized in this loop, and a longer wet etch of Al could be done. However, the thickness of the Al is only 200 nm, so depending on how far the layer extends underneath the SiO_2, it may be difficult to remove from a deep structure.

Another point of note is that the Al residues remaining on the edges are uneven on all edges, indicating that there was some misalignment of the back side SiO_2 release mask and the front side patterning. To avoid this, the alignment of front and back side masks should be improved.

4.1.5 Second Parylene Layer, Parylene Etch, Buried Mask Removal (Steps 9 – 11)

The second parylene deposition (step 9) completes the parylene encapsulation of the device. The deposition was done with the same parameters as the first, using 13 g of dimer for a thickness of 6

µm ± 0.5 µm. An O_2 plasma treatment was done beforehand in the Alcatel (Power: 60 Watts) to remove contaminants from wafer surfaces, and A-174 silane adhesion promoter was used. Studies have shown that A-174 silane does not improve the adhesion of parylene on parylene [22], but Kanhai's adhesion tests also showed that it does not decrease adhesion. Furthermore, the bottom side of the ceramic encapsulation is exposed, so the choice was made to use A-174 silane.

At this point in the process, the metal electrode was fully encapsulated in the layers of ceramic and parylene. The wafer was then plasma etched using the Alcatel parylene etch recipe from the front side. This etched the second parylene deposition from the front side fully, resulting in the same thickness of parylene on both the front side and the back side of the device, which places the metallization in a neutral plane. The Alcatel etch also etched the parylene through the open areas in the Ti buried mask, releasing the device along the perforated edges and opening the bond pads and electrodes.

Finally, the Ti buried mask was removed using SC-1 (1 part H_2O, 1 part H_2O_2 31%, 1 part NH_4OH 28%). Note that when TiN is used as the metallization instead of Pt, the TiN will be etched in this etchant as well, though at a slower rate. The wafer with the finished devices still in the silicon frame may be seen in Figure 30. Figure 31 shows an angled view of the front side of several devices. The sidewall of the silicon island is visible through the transparent parylene membrane. The device after being manually cut out of the wafer frame can be seen in Figure 32.

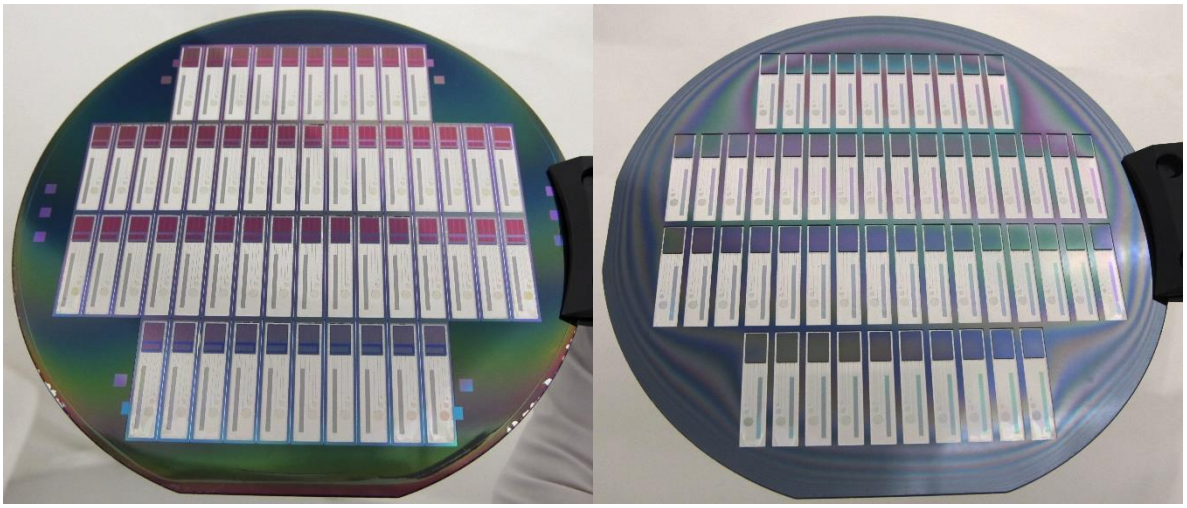


Figure 30: Devices still in silicon frame from (a) the front side of the wafer; (b) the back side of the wafer.

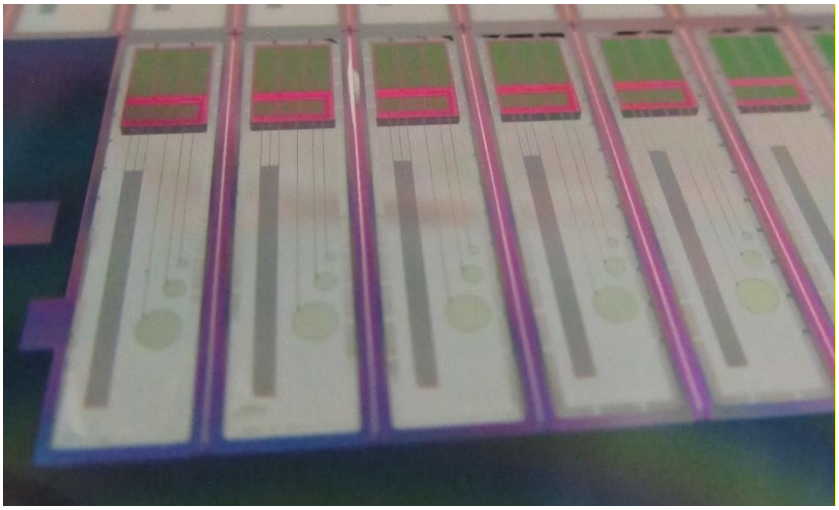


Figure 31: Angled view showing the sidewall of the silicon island from the front side.

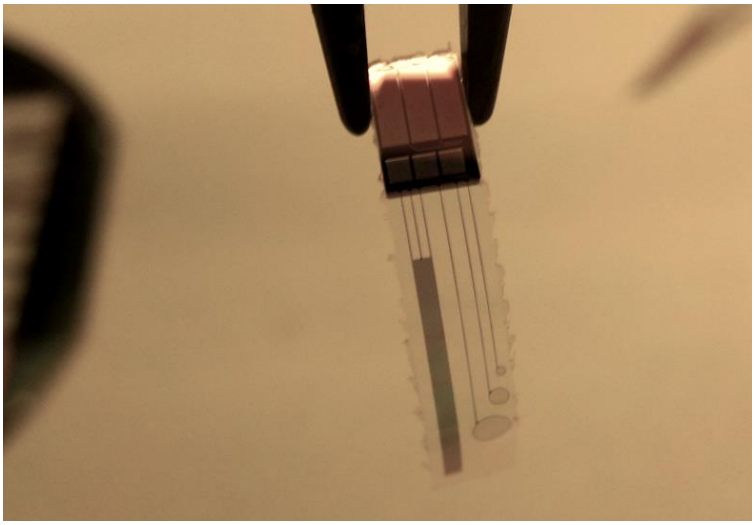


Figure 32: Released device cut out from the silicon frame.

4.2 Evaluation of the Fabrication Process

Optical and electrical evaluation of the functional structures on the devices was performed in order to determine the extent to which the fabrication process was successful in manufacturing the test devices.

4.2.1 Oxidation of TiN Electrodes in O_2 Plasma

Upon testing the conductivity of the exposed TiN bond pads of the finished device, it was found that the TiN on top of the silicon island is still conductive, but the circular electrode pads on the flexible parylene membrane are not. On a test wafer that did not undergo the DRIE step, the circular pads have not been released from the silicon substrate and are still conductive. By optical inspection (see Figure 33), there is still TiN visible on the bond pad. There are no cracks visible and it has not been etched away in SC-1. However, it is unknown if the thickness of the TiN layer has changed from the original deposition thickness of 200 nm.

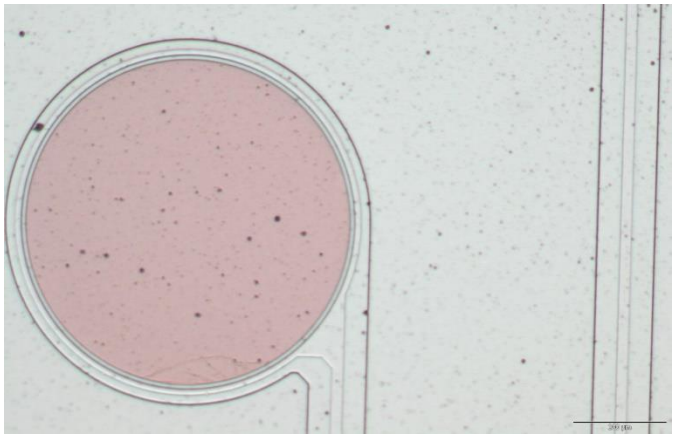


Figure 33: Front side of device showing TiN on electrode bond pads.

An explanation for the nonconductivity of the TiN on the membrane is that the TiN is oxidizing in the parylene etch done before the removal of the Ti buried mask, caused by the wafer heating in the Alcatel while being exposed to O_2 plasma [43],[44]. It is possible that the TiN on the bond pads on the silicon island oxidizes at a different rate from the electrodes on the membrane due to being at a different temperature, as the silicon island acts as a thermal conductor. It is also possible that a temperature-dependent reaction between parylene and TiN is occurring on the membranes, and not on the island.

An inspection was performed using both an optical microscope and the SEM to verify the cause of the nonconductivity and it was found that both the bond pads on the silicon island and the electrodes on the membrane show a layer of residue on the surface. In Figure 34(a), a conductive TiN bond pad on the silicon island is shown, with the layer of residue on top partially scratched off where it was contacted by a needle. This residue is also visible on the flexible bond pads, as seen in Figure 34(b).

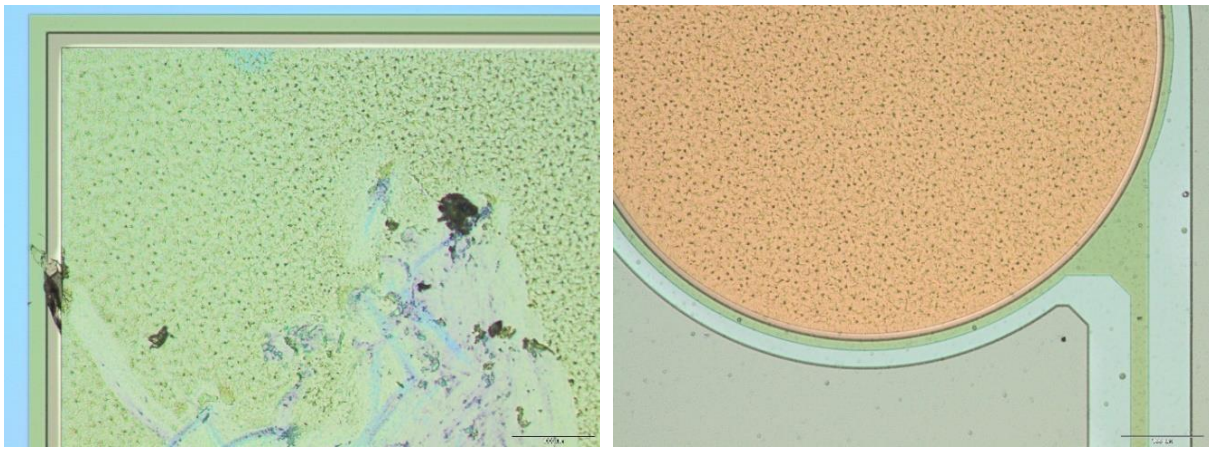


Figure 34: (a) Layer of residue on bond pad on Si island with scratches made by probe needle; (b) Layer of residue on bond pad on flexible membrane.

When the bond pads were examined in the SEM, this residue can be seen to charge under the electron beam, indicating that it is non-conductive. The scratches are also visible, and the underlying layer of TiN can be seen beneath it. Images from the SEM with the charging layer on top of TiN is shown in Figure 35. Therefore, it is likely the TiN on both the island and the membrane is oxidizing,

and the reason the TiN on the island is conductive is because the presence of the bulk silicon underneath allows the layer to be scraped off using needles or probes during resistance measurements.

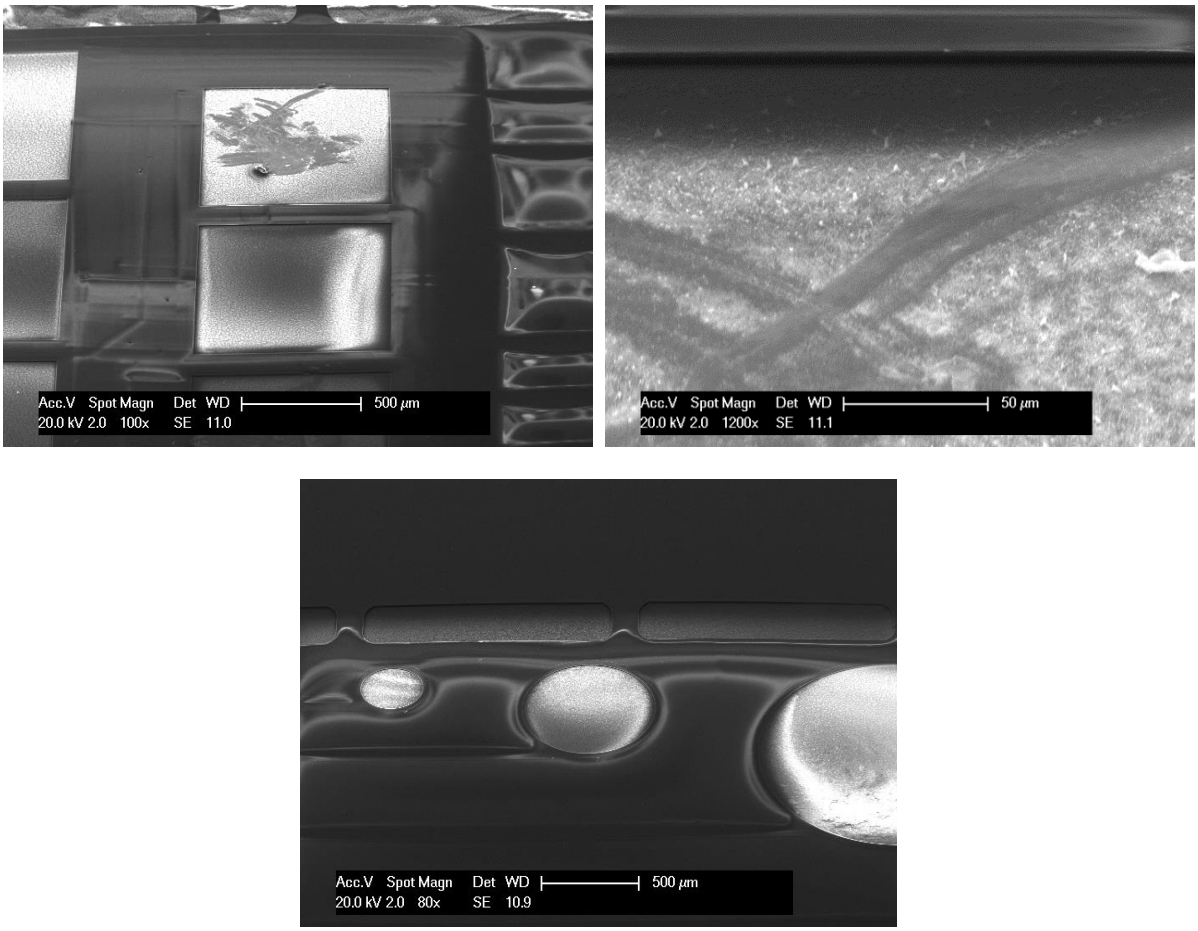


Figure 35: (a) SEM photo of a charging layer of residue on bond pads on a Si island with scratches made by probe needle; (b) Close up of the surface of a bond pad from (a); (c) SEM photo of charging layer of residue on the bond pad on a flexible membrane.

If this layer is indeed titanium oxide, it may be removed using a dry etch with gasses $O_2/CF_4/Ar$. However, as the final device will be made using Pt as the material for the electrode, further study of this problem was not done.

4.2.1 Parylene on Parylene Delamination

Several dies at the bottom edge of the wafer showed delamination of the two parylene layers, shown in Figure 36. The point at which the layers separated was at the bottom corners of the die. One device was examined by pulling apart the layers with tweezers and inspecting them under the microscope.

The top parylene layer (the first deposition) may be seen in Figure 37. The ceramic encapsulation and metallization adhere to the top layer, while the bottom layer has no structures adhering to it, as can be seen in Figure 38. The adhesion of the first parylene deposition (the front side layer) to the ceramic encapsulation seems to be stronger than the second parylene deposition (the back side layer).

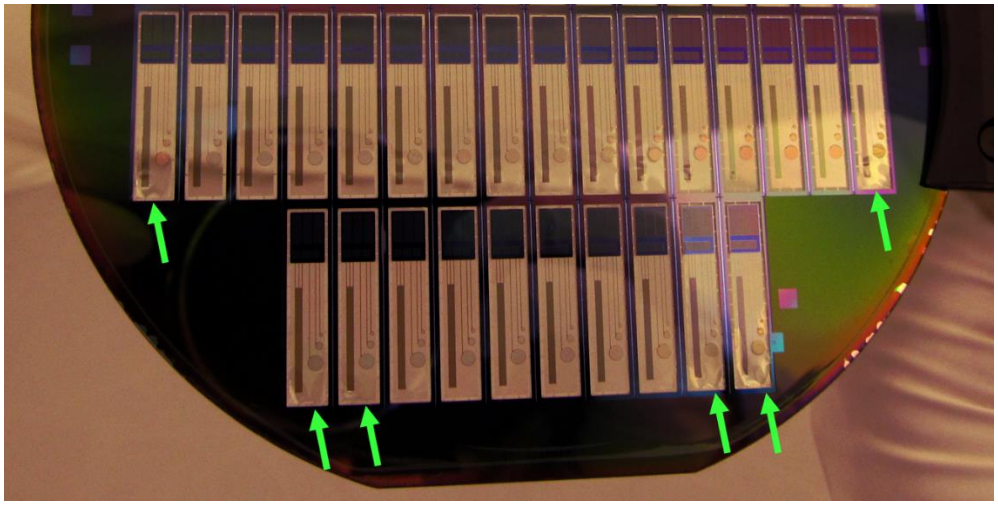


Figure 36: Dies with delaminating parylene membranes indicated with arrows.

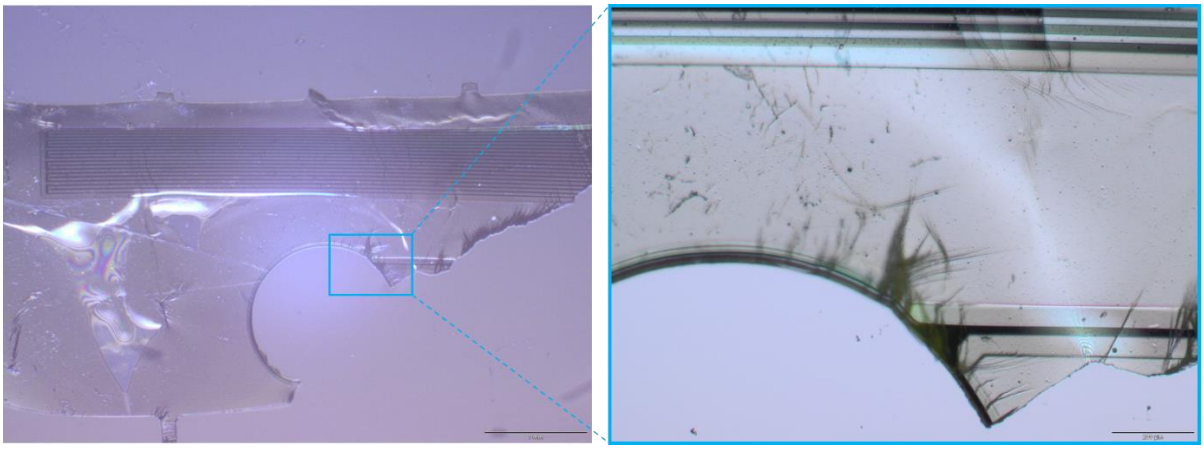


Figure 37: Top layer of parylene with metallization and ceramic encapsulation.

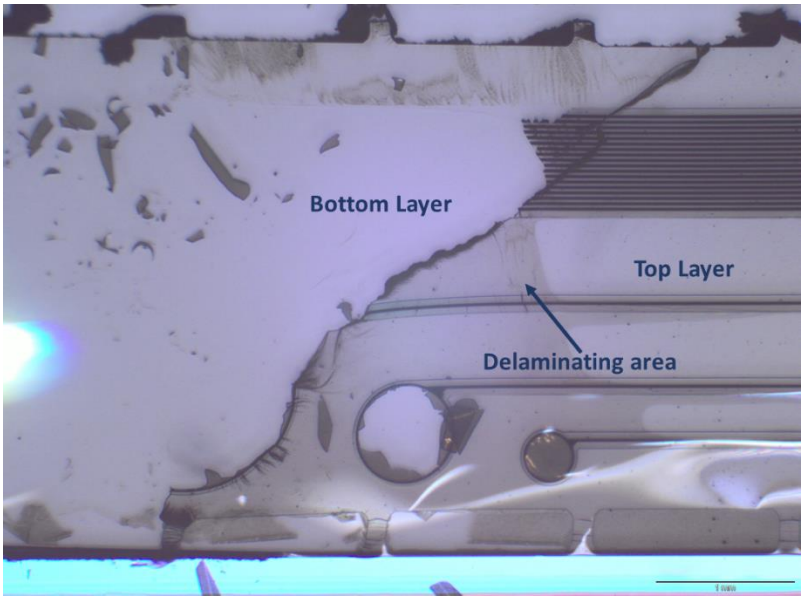


Figure 38: Section of device with torn off top parylene layer.

It is likely that the use of the O_2 plasma treatment before parylene deposition is decreasing the adhesion between the parylene layers. The O_2 plasma treatment was included in this process to clean the underlying layers before the parylene deposition, as the presence of contaminants will decrease adhesion, and there is exposed silicon nitride during the second parylene deposition. However, the O_2 plasma treatment also decreases the hydrophilicity of the ceramic layers, which may affect the use of A-174 silane.

The reason the delamination shows on the edges is most likely due to the treatment before the second parylene deposition being done in the Alcatel, which has varying etch rates from the center to the edge of the wafer. The O_2 plasma treatment done before the first deposition was done in the Tepla, so the treatment over the entire wafer would be more uniform.

Kanhai's adhesion testing reported good parylene to parylene adhesion, but his test did not include an O_2 plasma treatment. Studies have also indicated that O_2 plasma treatment decreases the adhesion between two layers of parylene C [22]. It is recommended that the O_2 plasma treatment be omitted from future parylene depositions for this process flow.

4.2 Conclusion

The fabrication process was successfully carried out and produced a device with comb and meander structures on which electrical measurements can be made. The fabrication of a rigid silicon chip with working interconnects was done in a single process flow.

The problem with tearing membranes when manually cutting devices out of the silicon frame was solved with the patterning of ceramic layers and the rounding of silicon island corners. Furthermore, during the DRIE etch of the bulk silicon, no membranes broke, so the new back side DRIE mask with rounded corners improved the yield.

Due to the substitution of titanium nitride in place of platinum for the metallization, the electrodes are not conductive and no electrochemical tests can be carried out. If the cause of the nonconductivity is due to the oxidation of the titanium nitride layer as hypothesized, this problem should be solved when platinum is used for metallization as originally intended.

The most critical optimizations required are to solve the masking of the aluminum wet etch and the delamination of the parylene layers. A different DRIE recipe that produces vertical sidewalls should be used to allow the aluminum etch stop layer to be removed fully, as aluminum is not a material that should be used in neural implants. Also, in order to improve the adhesion between the two parylene layers, the wafer should not be treated with O_2 plasma prior to parylene deposition.

Several minor aspects of the fabrication need to be optimized. These include the size of the aluminum etch stop layer and the size of the titanium buried mask, which are both dependent on the size and sidewall angle of the silicon island. Once the DRIE process is optimized to produce a sidewall with minimal negative sloping, the exposure and development parameters for the etch stop and buried mask can be optimized as well.

5 Testing and Results

Two evaluation tests were performed on the devices. The first was an accelerated aging test in PBS. As a neural implant must be able to survive for long term in moist conditions, this test monitored resistance changes in the metal lines over time in order to check for corrosion or moisture condensation in voids. The second was a bending test in which the flexibility of the devices was evaluated, in order to determine if this process may be used to fabricate devices that may be bent around a probe lead.

5.1 Accelerated Aging Test

During the accelerated aging test, the devices were placed in aggravated conditions of heat and humidity to simulate the aging of the device in body-like conditions. Resistance measurements of the comb-meander structures were made at certain time intervals in order to monitor variations in the resistance that would indicate changes in the device, such as corrosion of the metal lines or void formation in the parylene causing a short circuit between the comb and meander structures.

5.1.1 Test Setup

The devices were suspended in phosphate buffered saline (0.01 M phosphate buffer, 0.0027 M potassium chloride, 0.137 M sodium chloride, pH 7.4), and maintained at a constant elevated temperature of 57°C in an incubator.

For many polymers, the rate of aging is increased by a factor of *f*, following the approximation based on empirical observation that an increase of 10°C corresponds to two times the aging rate [45]. The equation for this approximation is:

$$f = 2^{\Delta T/10} \quad (1)$$

with ΔT being the difference between the elevated temperature at which the test is performed at and a reference temperature at which the effects of aging are evaluated. For implantable devices, the reference temperature is the body temperature of 37°C.

Based on the ASTM F1980 (American Society for Testing and Materials Standard guide for accelerated aging of sterile medical device packages), it is recommended that polymeric materials are tested in conditions less than 60°C, as higher temperatures may introduce nonlinearity in reaction rates and new failure modes that would not ordinarily occur at body temperature [46].

Given the above, an elevated temperature of 57°C was chosen for this test. This temperature results in a rate of aging increased by four times, while remaining below 60°C.

The total test time was chosen to be four weeks. With an elevated temperature of 57°C, this time corresponds to four months in human body conditions.

5.1.2 Procedure

Four batches of five devices each were made. Batch 1 was placed in the PBS and maintained at a temperature of 57°C, while being removed at certain time intervals throughout the month to monitor changes in the devices. The devices of Batch 1 were to be tested at times 0 hours, 6 hours, 24 hours, 48 hours, 1 week, 2 weeks, 3 weeks, 4 weeks, or until failure.

Batch 2 was also subjected to the accelerated aging conditions, but with measurements made at fewer time intervals in order to limit the amount of handling the devices are subjected to. These times were at 1 week, 2 weeks, 3 weeks, and 4 weeks.

One week after the beginning of the test, a new batch, Batch 3, was introduced, as Batch 1 showed many failures caused by the handling of the devices rather than aging. Batch 3 was to follow the same weekly monitoring procedure as Batch 2.

A reference batch is kept as a control sample, and is left at 20°C to check for aging effects.

Prior to performing the aging, resistance measurements were made between the two ends of the meander structure and between the meander and comb structures, according to the procedure described in section 5.1.3.

Each batch was affixed to a strip of silicon using carbon tape as shown in Figure 39. Batches 1, 2, and 3 were suspended above a container containing PBS at 57°C such that only the flexible membrane with the comb and meander structures are submerged, as can be seen in Figure 40(a). As parylene is hydrophobic, the membranes will float on the surface of the PBS unless a piece of silicon is inserted into the liquid to keep them in place. The containers are covered with aluminum foil to prevent the evaporation of PBS. PBS levels of all three batches must be monitored due to evaporation, and more PBS added when necessary.

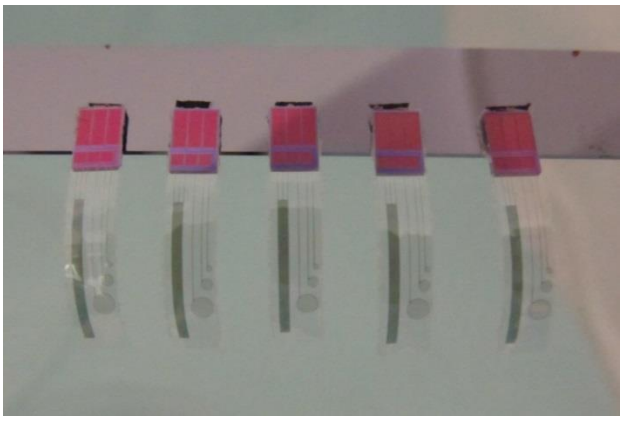


Figure 39: Five devices affixed to a strip of silicon.

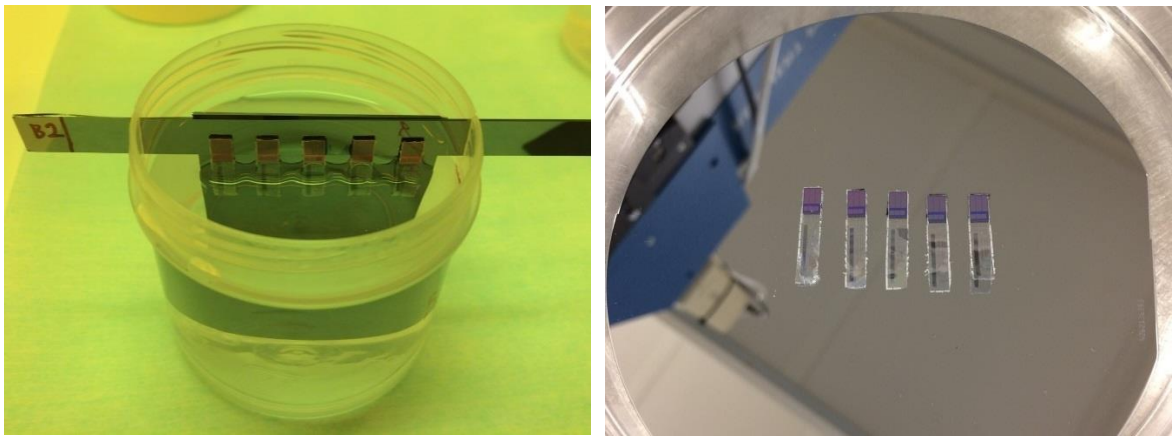


Figure 40: Set up for (a) Batches 1, 2, and 3; (b) Reference batch.

The reference batch devices were fixed to a silicon wafer, placed in a single wafer container as can be seen in Figure 40(b)Figure 39, and kept in CL100 conditions.

Before the measurements at the defined time intervals, the devices were removed from the incubator. The devices were rinsed in deionized water so no residues from the PBS remain when dry. The silicon strip with attached samples is taped using Kapton tape on a silicon carrier wafer, which is placed back in the incubator for 2 minutes to facilitate drying.

The resistance measurements were taken according to the process described in section 5.1.3. the metallization continuity was checked using the meander structure and the encapsulation reliability was evaluated using the comb structure. Once measurements were complete, the devices were returned to the incubator.

When appropriate, the devices were examined optically using a microscope. However, it was found after handling failures that it is better to limit the amount of handling the devices are subjected to.

5.1.3 Measurements

Batches 1, 2, and 3 were tested according to these resistance measurements at the beginning of the test (time: 0 hours) and the end (time: 4 weeks). In addition to these two times, the devices of Batch 1 were tested at times 6 hours, 24 hours, 48 hours, 1 week, 2 weeks, 3 weeks. Times may be accurate within 90 minutes, due to the time it takes for measurements, so the devices must be returned to the incubator within 90 minutes of being removed.

Two resistance measurements were made. The first was between the two bond pads of the meander (pads 1 and 3, indicated in Figure 41). The second resistance measurement was between one pad of the meander and the pad of the comb structure (pads 1 and 2 in Figure 41).

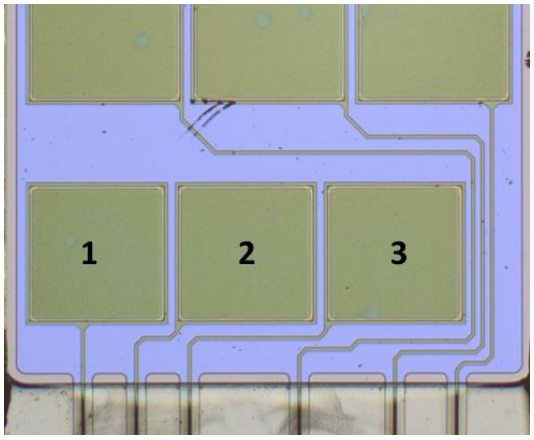


Figure 41: Labelled bond pads of the meander (1 and 3) and the comb (2).

5.1.3.1 Resistance Measurements of the Meander Structure

The theoretical resistance of the meander was calculated based on the measured sheet resistance according to the equation: [2]

$$R_s = 17.11 \frac{\Omega}{sq} \quad (2)$$

$$R = R_s * \frac{L}{W} = 17.11 \frac{\Omega}{sq} * \frac{126{,}500\ \mu m}{20\ \mu m} \quad (2.1)$$

$$R = 108.22\ k\Omega \quad (2.2)$$

The sheet resistance R_s = 17.11 Ω/sq was measured from a sheet wafer on which a 200 nm layer of TiN was sputtered using the same recipe that was used for the metal lines of the electrode. The length L = 126.5 mm is the approximate length of the meander. The width W = 20 µm is the width of the meander. Note that some variations of W and L due to the corners of the turns of the meander were not considered in this approximation.

In reality, the measured resistance of the meander structure tended to vary from 160 kΩ to 190 kΩ on devices taken from the center of the wafer, which is higher than the theoretical resistance. It is possible that the discrepancy in resistance values is caused by the oxidation of the TiN metal lines, as during the photoresist stripping step after the TiN metallization pattering, the metallization layer is exposed to O_2 plasma for ~15 minutes.

However, certain devices on the edge of the wafer showed a meander resistance of around 300 kΩ, especially near the top of the wafer where the bond pads are closest to the wafer edge (indicated in Figure 42). This resistance is likely caused during the patterning of the ceramic encapsulation layers, as the ceramic is etched in the standard oxide etch in the Alcatel (CF_4: 50.0 Sccm, CHF_3: 25.0 Sccm, He: 40.0 Sccm, Power: 60 Watts). The Alcatel etch is not uniform and etches ceramic faster at the edges of the wafer. The metallization on the edge of the wafer might be thinned from the physical bombardment or etched in the gasses, as CF_4 and CHF_3 have both been used for titanium etching [47].

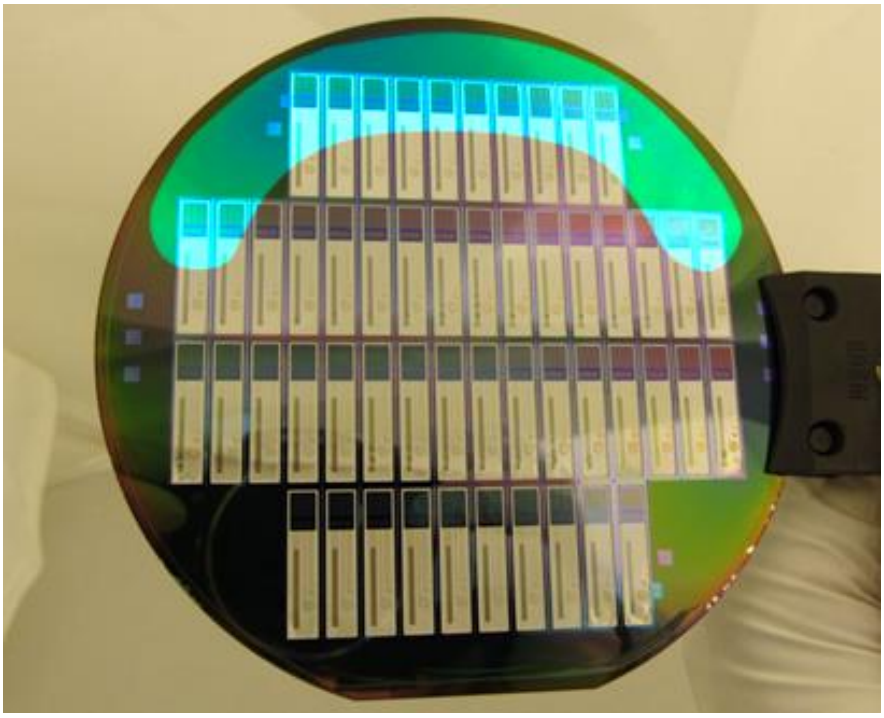


Figure 42: Highlighted area of the wafer that showed the most dies with high meander resistances (~300 kΩ).

Both oxidation and physical bombardment of the TiN metallization in the two Alcatel plasma etches would cause a decrease in the thickness of the TiN layer, leading to an increase in metal track resistance. If an average resistance of 175 kΩ is assumed for a device in the middle of the wafer, and assuming a constant resistivity, this meander resistance corresponds to a metallization thickness that is calculated as follows:

$$\rho = R_s * th = 17.11 \frac{\Omega}{sq} * 0.2\ \mu m \tag{3}$$

$$R = \frac{\rho}{th} * \frac{L}{W} \tag{3.1}$$

$$th = \frac{L}{W} * \frac{\rho}{R} = \frac{126{,}500\ \mu m}{20\ \mu m} * \frac{17.11\ \Omega/sq * 0.2\ \mu m}{175{,}000\ \Omega} \tag{3.2}$$

$$th = 0.124\ \mu m \tag{3.3}$$

This indicates a loss of ~76 nm of TiN, either through oxidation or etching, but as the time the TiN was exposed in the Alcatel etches is unknown, it is difficult to determine if the thinning of the TiN layer is the cause of the increased resistance. Again, these problems were caused by the substitution of TiN into a process flow meant for platinum metallization, so more time was not spent investigating the measured resistance. As the stress testing was performed by monitoring only the change in resistance, the discrepancy between measured and theoretical values that are within the same range did not impact the tests.

The resistance measurements of the meander structure that undergo accelerated aging test in PBS at 57°C were made using a manual probe station, the Cascade 33, by contacting pads 1 and 3 (Figure 41). A voltage sweep was done with limits from -10 V to 10 V, with a step size of 0.1 V. The current was measured, and the resistance may be calculated according to Ohm's law.

$$V = IR \tag{4}$$

Changes in the resistance were monitored throughout the testing period. Increasing or nonlinear resistance may be an indication of corrosion of the metal lines or bad adhesion to the ceramic layer. As the graph of current *I* vs. voltage *V* is plotted, any nonlinearities in the resistance become visible. Should the resistance become too high, the device was be considered broken, since an infinite resistance indicates an open circuit caused by a break somewhere in the metal line.

5.1.3.2 Resistance Measurements of the Comb Structure

The theoretical value of the resistance between the comb and meander structures is infinite, since the two structures should not be conducting. The measured value of the resistance is on the order of gigaohms (the measured current being on the scale of nanoamps) and is high enough to be considered infinite. This measurement is to ensure that at no point does the comb and meander become shorted together due to the diffusion of liquid into a void, which would indicate the lack of good adhesion between the metallization and ceramic layers, or the presence of a contaminant particle.

5.1.4 RESULTS

5.1.4.1 BATCH 1

Batch 1 may be considered a trial batch for the test set up. For Batch 1, both resistance measurements and optical examination under the microscope were performed. However, the process of taking optical measurements caused mechanical damage to the devices due to handling. As the membranes would not lie flat enough for focused optical microscope examination, they had to be repeatedly adhered to the carrier wafer with either DI water or isopropanol.

After 48 hours, the devices of Batch 1 started to indicate failures with open circuits between the two bond pads of the meander. When inspected optically, no appearance of void formation or increased defect sizes was evident around the comb-meander structure. The most likely cause of the failures was the spreading of cracks from the corner of the silicon island caused by the constant handling of the device. A comparison of device 1 at the beginning of the test and after 6 hours of soaking may be seen in Figure 43. No other significant differences were visible on the device. By one week, all devices in Batch 1 had failed due to an open circuit in the meander.

This hypothesis was corroborated by the resistance measurements of Batch 2 after 1 week, which had not been removed from the incubator. Four out of five devices showed meander resistances that were relatively the same as the initial measurements, indicating that most devices did not fail after a week of accelerated aging when they were not subjected to handling.

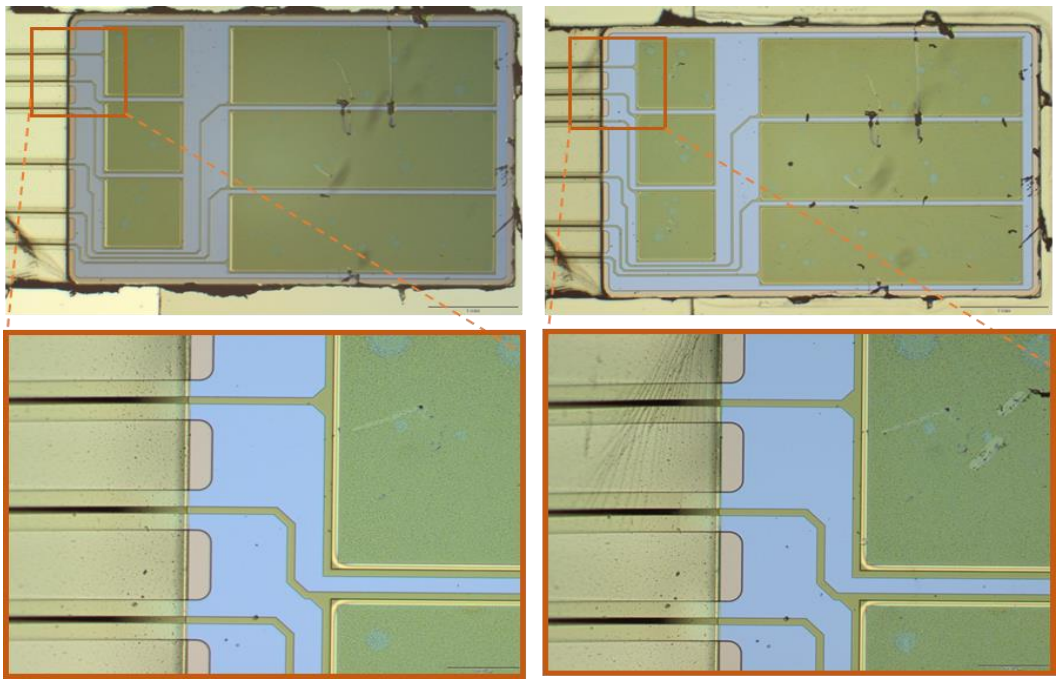


Figure 43: Device 1 at (a) 0 hours; (b) 6 hours with visible cracks in the membrane at the edge of the silicon island due to handling.

The table of average resistance measurements and the standard deviations for the meander may be seen in Table 6, with the failing values (higher than 1 GΩ) indicated in red. However, these failures were due to handling errors. Furthermore, the resistance measurements for the first 24 hours, which were performed primarily on Batch 1, used a voltage sweep from -5 V to 5 V before it was found that a sweep of -10 V to 10 V is necessary to see some nonlinearities in the resistance. Therefore, the

resistance measurements are considered invalid, as they do not represent aging effects on the devices, and are not analyzed in-depth.

Table 6: Batch 1 meander resistance measurement averages and standard deviations

Batch 1					
Time	Average Meander Resistance [Ω]				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	1.85E+05	1.90E+05	1.75E+05	1.80E+05	1.80E+05
6 hours	1.87E+05	1.94E+05	1.74E+05	1.80E+05	1.81E+05
24 hours	1.16E+09	1.91E+05	1.76E+05	1.80E+05	1.81E+05
48 hours	4.14E+09	4.64E+09	1.82E+05	3.81E+09	1.84E+05
1 week			1.49E+09		4.34E+09
Time	Std Dev of Meander Resistance [Ω]				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	3.84E+02	2.65E+02	3.56E+02	3.42E+02	3.83E+02
6 hours	3.09E+02	4.15E+02	3.33E+02	2.15E+02	3.46E+02
24 hours	5.16E+06	2.82E+02	2.51E+02	2.58E+02	2.63E+02
48 hours	2.35E+09	3.12E+09	5.71E+02	2.18E+09	1.31E+02
1 week			2.27E+08		4.75E+09

No differences were seen in the resistance measurement between the meander and the comb from the beginning of the test (time: 0 hours) to the point where each device failed the meander resistance test. As long as the resistance was above 1 GΩ, it was considered an open circuit. As can be seen from Table 7, no shorts were seen between any of the comb and meander structures, indicating that there were no voids caused by delamination between the metallization and the ceramic encapsulation that spanned the lines between comb and meander. It is possible that a void formed around a single metal line without touching the other lines, as this would not cause a short. Such a void would be expected to grow over time, however, eventually resulting in a failure.

Table 7: Measured open circuit between the comb and meander structures of Batch 1

Batch 1					
Time	Open Circuit Between Comb and Meander				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	✓	✓	✓	✓	✓
6 hours	✓	✓	✓	✓	✓
24 hours	✓	✓	✓	✓	✓
48 hours	✓	✓	✓	✓	✓
1 week	N/A	N/A	✓	N/A	✓

The conclusion from Batch 1 is that no changes occur in the devices for 48 hours of soaking at elevated temperature, so the other batches do not have to be monitored constantly for early failures. It was also determined that optical examination is not suited for this set up, yields few results that could be used as data, and causes mechanical failures unrelated to aging. It was determined that optical examination would not be performed for the rest of the batches.

5.1.4.2 BATCH 2

The resistances of Batch 2 devices were measured on a time interval of 1 week. The average resistances and standard deviations may be seen in Table 8. Values highlighted in red indicate failures due to open circuits, while orange values indicate changes in order of resistance that should be considered failures, but are not open circuits.

Table 8: Batch 2 meander resistance measurement averages and standard deviations.

Batch 2					
Time	Average Meander Resistance [Ω]				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	3.78E+05	1.89E+05	1.86E+05	1.80E+05	1.78E+05
1 week	7.38E+05	1.91E+05	4.79E+09	1.82E+05	1.78E+05
2 weeks	1.08E+06	1.91E+05		1.83E+05	1.79E+05
3 weeks	1.03E+06	1.90E+05		2.09E+05	1.81E+05
4 weeks	3.56E+07	2.04E+05		1.87E+05	1.39E+09
Time	Std Dev of Meander Resistance [Ω]				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	5.45E+03	2.89E+02	3.02E+02	2.50E+02	2.60E+02
1 week	4.69E+04	1.25E+02	4.34E+09	5.57E+01	1.52E+02
2 weeks	1.28E+05	7.76E+01		7.35E+01	7.26E+01
3 weeks	8.40E+04	1.02E+02		4.10E+03	9.23E+01
4 weeks	5.60E+07	2.64E+02		1.00E+02	8.21E+08

After one week, Device 3 showed an open circuit in the meander. There is reasonable evidence that Device 3 failed due to handling, as the adhesion of the device to the silicon strip failed and it is likely the failure happened while the device was reattached.

The meander resistance of Device 1 at time 0 showed a high resistance of 378 kΩ, indicating that it is likely a device from the edge of the wafer. It also increased in resistance over the course of the four weeks. By the end of week 2, it is ~1 MΩ in resistance. It is possible that the devices on the edge of the wafer corrode faster, if the metallization layer is already thin.

The standard deviations of the resistances of Device 1 is also higher than the other devices. For a linear plot of I vs. V, the standard deviation of meander resistance is on the order of E+02. A high standard deviation such as the value seen for Device 1 at 1 to 4 weeks indicates nonlinearity in the resistance measurements from the voltage sweep. The graph of the voltage sweep for Device 1, which had a high standard deviation of meander resistance, may be seen in Figure 44(a), while the graph for Device 2, showing a standard deviation on the order of E+02, can be seen in Figure 44(b). Device 1 also has a much higher average resistance.

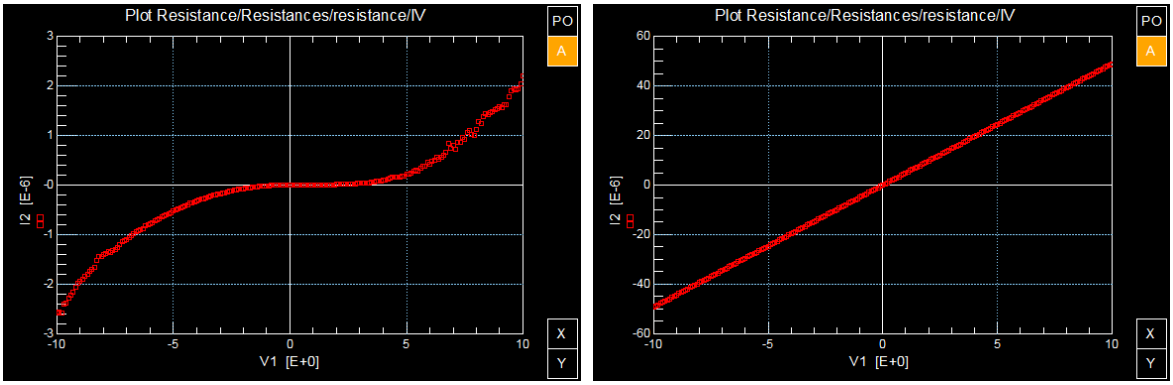


Figure 44: I vs. V curves at 4 weeks for (a) Device 1 showing nonlinear resistance over the voltage sweep; (b) Device 2 showing linear resistance over the voltage sweep.

A nonlinear resistance is not necessarily an indication of an open circuit (although this particular example is). It may indicate corrosion in the metal lines that has not yet resulted in a break. However, it is also possible a nonlinear resistance is due to the oxide punchthrough effect, where an applied voltage is high enough to break down an oxide layer and cause conduction. Assuming the TiN has been oxidized, this would explain the shape of the I vs. V curve: at lower voltages (-5 V to 5 V), the resistance is high, but the current at higher voltages indicates the meander is still conducting. As there is always some measure of inconsistency in the way the measurements are made, it is difficult to determine the cause of the nonlinearity in resistance.

Device 5 failed by the end of week 4 due to an open circuit. Upon optical examination, no voids or breaks in the metal lines are visible. The failure mode is unknown. As can be seen from Figure 45, the device showed wrinkles on the parylene membrane after being soaked for four weeks, possibly due to the parylene swelling, as the device straightens out after drying for 24 hours. The other devices from all batches that had been soaked for at least two weeks showed similar wrinkling, so it does not indicate device failure. However, it causes difficulties when doing the optical examination.

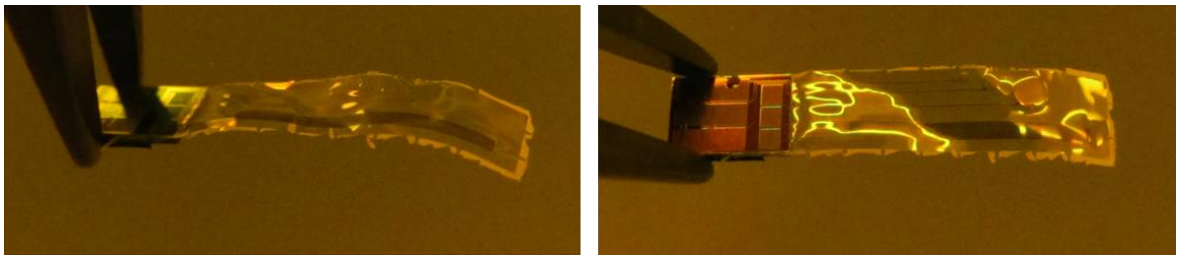


Figure 45: Device 5 from Batch 2 showing wrinkling in the parylene membrane after being soaked for 4 weeks.

No devices from Batch 2 showed a short between the meander and comb structures. The result may be seen in Table 9.

Table 9: Measured open circuit between the comb and meander structures of Batch 2

Batch 2					
Time	Open Circuit Between Comb and Meander				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	✓	✓	✓	✓	✓
1 week	✓	✓	✓	✓	✓
2 weeks	✓	✓	N/A	✓	✓
3 weeks	✓	✓	N/A	✓	✓
4 weeks	✓	✓	N/A	✓	N/A

5.1.4.3 Batch 3

Batch 3 was introduced to the test one week after the beginning of the test after all devices from Batch 1 failed. The voltage sweep limits for all tests were set to -10 V to 10 V. As can be seen from Table 10, no devices failed from Batch 3 after 4 weeks of being subjected to accelerated aging conditions.

Table 10: Batch 3 meander resistance measurement averages and standard deviations

Batch 3					
Time	Average Meander Resistance [Ω]				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	1.77E+05	1.74E+05	1.82E+05	1.79E+05	1.74E+05
1 week	1.78E+05	1.74E+05	1.82E+05	1.79E+05	1.74E+05
2 weeks	1.79E+05	1.74E+05	1.82E+05	1.79E+05	1.74E+05
3 weeks	1.81E+05	1.76E+05	1.82E+05	1.79E+05	1.74E+05
4 weeks	1.80E+05	1.74E+05	1.82E+05	1.79E+05	1.73E+05
Time	Std Dev of Meander Resistance [Ω]				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	9.97E+01	9.61E+01	1.10E+02	1.03E+02	1.18E+02
1 week	7.46E+01	7.53E+01	7.41E+01	7.24E+01	7.37E+01
2 weeks	1.22E+02	7.40E+01	5.49E+01	5.65E+01	6.31E+01
3 weeks	4.29E+02	1.28E+02	1.10E+02	5.65E+01	1.23E+02
4 weeks	2.34E+02	1.59E+02	1.46E+02	1.45E+02	8.65E+01

There is also no clear indication that the devices are increasing in resistance. Device 1 shows an increase for the first three weeks from 177 kΩ to 181 kΩ, but drops to 180 kΩ after week 4. The other devices do not change much in resistance. It is possible that the changes in resistance are due to the inconsistent measurement setup or bad contact with the bond pads, as during some measurements the devices moved when the needles came in contact with the bond pads due to bad adhesion with the silicon strip. For the last measurement at week 4, the devices had all come loose and were reattached to the carrier wafer to ensure that good contact was made. However, it is proven that some devices are capable of lasting for four weeks at 57°C in PBS without significant changes in resistance.

Again, no devices from Batch 3 showed a short between the meander and comb structures. The result may be seen in *Table 11*.

Table 11: Measured open circuit between the comb and meander structures of Batch 3

Batch 3					
Time	Open Circuit Between Comb and Meander				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	✓	✓	✓	✓	✓
1 week	✓	✓	✓	✓	✓
2 weeks	✓	✓	✓	✓	✓
3 weeks	✓	✓	✓	✓	✓
4 weeks	✓	✓	✓	✓	✓

As no failures were seen in Batch 3 after four weeks, they were returned to the accelerated aging conditions for further monitoring. The results of this test will be outside the scope of this project.

5.1.4.4 Reference Batch

The reference batch was meant as a control, and was left at 20°C and cleanroom humidity conditions for the duration of the test. The resistance measurements of the reference batch were taken at the beginning of the test (time: 0 hours) and at the end of the test (time: 4 weeks) to monitor for changes in devices not subjected to accelerated aging conditions. However, the meander resistances of all devices at time 0 were around 300 kΩ or higher. Unfortunately, the reference batch devices cannot be compared to the soak test devices, as the starting resistance is not comparable.

As can be seen from Table 12, the devices from the reference batch increased in resistance, except for Device 1, which decreased in resistance. Most devices also showed greater nonlinearity than the devices subjected to accelerated aging conditions in Batches 2 and 3. Again, Device 1 at week 4 showed more linear behavior than at the beginning of the test. Upon visual inspection, the top and bottom parylene layers on Devices 1, 2, and 5 had started to delaminate from each other in the manner described in Chapter 4.2.1. Device 1 and 2 are shown in Figure 46.

Table 12: Reference Batch meander resistance measurement averages and standard deviations

Reference Batch					
Time	Average Meander Resistance [Ω]				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	2.66E+05	3.25E+05	3.17E+05	5.52E+05	3.90E+05
4 weeks	2.26E+05	3.70E+05	1.22E+06	6.90E+05	1.03E+06
Time	Std Dev of Meander Resistance [Ω]				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	1.81E+03	7.51E+03	2.57E+03	1.78E+04	6.09E+03
4 weeks	3.36E+02	3.19E+03	1.04E+05	2.30E+04	1.01E+05

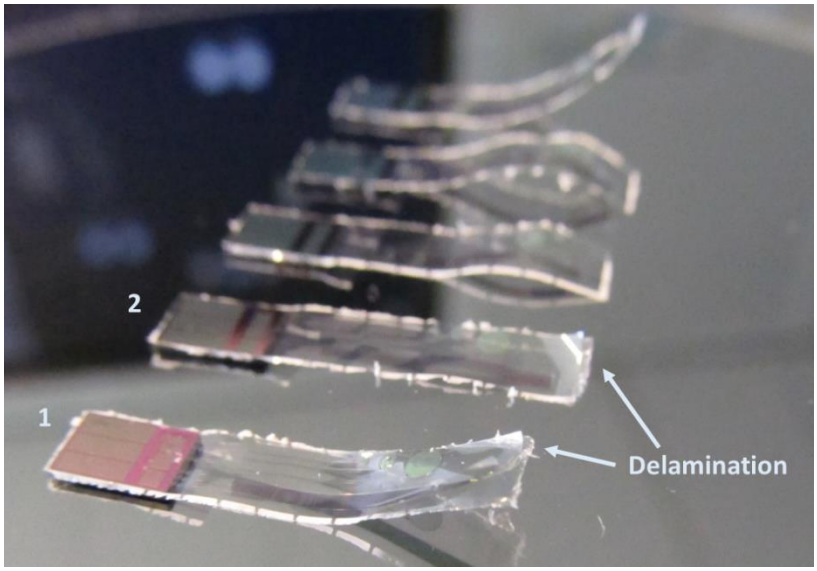


Figure 46: Delamination of parylene layers on Device 1 and 2 of the reference batch.

There are several possible explanations for why the measurements for the reference batch show different behavior from Batches 2 and 3.

The high resistance values caused potentially by more oxidized TiN and the parylene delamination suggest that all devices in this batch were taken from the edge of the wafer. Though an attempt was made to take devices for each batch from various locations on the wafer, the locations were not documented. This could also indicate that the edge devices show greater nonlinearity over time.

It is possible that the parylene delamination is exacerbated by being held at room temperature. There may be intrinsic stresses in the parylene layers that cause them to separate over time. It is also possible that the devices being kept at an elevated temperature in the incubator improves parylene to parylene adhesion. Thermal annealing at 200°C has been used to improve parylene to parylene adhesion [15], though there are no reports on adhesion enhancement at 57°C.

Unfortunately, given the data from the reference batch, few conclusions can be drawn. In order to test these theories, a new wafer needs to be fabricated to monitor the behavior of devices over time.

No devices from the reference batch showed a short between the meander and comb structures. The result may be seen in Table 9.

Table 13: Measured open circuit between the comb and meander structures of Batch 3

Reference Batch					
Time	Open Circuit Between Comb and Meander				
	Device 1	*Device 2*	*Device 3*	*Device 4*	*Device 5*
0 hours	✓	✓	✓	✓	✓
4 weeks	✓	✓	✓	✓	✓

5.1.5 Conclusions

As previously mentioned, Batch 1 may be considered a trial batch, as there are visible cracks in the membrane and the metal lines at the edge of the silicon island due to handling. The conclusions that

may be drawn from Batch 1 are that devices will survive for up to 24 hours at 57°C in PBS, so there is no need to monitor the devices for early failures.

Of the devices tested from Batches 2 and 3, seven out of nine survived for four weeks at 57°C in PBS, which corresponds to four months in body temperature conditions. Discounting Device 3 from Batch 2, which likely failed due to handling, two out of four devices survived from Batch 2 and five out of five devices survived from Batch 3, possibly because Batch 3 was handled with more care and experience. Four out of five devices from Batch 3 did not show an increase in resistance from the start of the test to the end. However, the setup of the test offered potential for inconsistent measurement, so the data may not be representative of a true aging test. Uncontrolled variables in the test included bad contact to bond pads or the oxide punchthrough effect due to the layer of titanium oxide on the bond pads, bad adhesion of the devices to the silicon test strip causing movement of the devices during measurement, and location of the device on the original wafer (edge vs. center). These variables should be limited as much as possible if the accelerated aging test were to be repeated.

5.1.5.2 Recommendations

Future recommendations would be to perform the accelerated aging test for a longer time. The weak point of the device design is the edge of the silicon island, as cracks originate from the corners even when they are rounded. Thus, handling should be limited. It may be possible to keep the devices in the silicon frame during the soak test instead of cutting through the perforated edges to release the device, which would also solve the problem of difficulties in optical measurements as the device would be kept flat.

Carbon tape should not be used to adhere the devices to the carrier as the devices may move when the needles come in contact with the bond pads, affecting the measurement. The silicon island of the device was adhered to the silicon strips in such a way that the parylene membrane would not bend on the silicon strip or stick to the adhesive, but if the devices are not adhered well, the island would tip at an angle during the measurement. A different, stronger adhesive that is resistant to moisture is necessary to prevent movement during measurement.

Fabricating the devices with platinum metallization would solve the measurement problems caused by the oxide layer on top of the bond pads. With more consistent resistances over the wafer, the causes of any changes in resistance could be narrowed down. As platinum will not oxidize, for example, the possibility of oxide punchthrough causing the nonlinear resistance measurements is eliminated. Using platinum metallization should also result in conductive electrodes, upon which electrochemical characterization could be performed using tests such as cyclic voltammetry and electrochemical impedance spectroscopy.

5.2 Bending Test

As the purpose of the process flow is to develop flexible devices meant to be wrapped around the tip of a catheter or guidewire, the interconnects must be capable of bending to a certain diameter without failing due to broken metal lines. The devices were placed on a tool similar to a vice with a millimeter screw to control the gap width defining the bending diameter. The gap was decreased in increments, and a resistance measurement was made between the two bond pads of the meander and compared to the initial measurement. An infinite or very high resistance measurement indicates

that the metal line has broken, and the diameter at which the line broke is the minimum bending diameter.

Note that the bending test will yield different results in the case of platinum electrodes, as the Pt metallization is less brittle than TiN and will be of a different thickness. However, using the TiN devices for the bending test can give an idea of how far the devices are able to bend with the brittle ceramic layers in place.

5.2.1 PROCEDURE

The bending tool may be seen in Figure 47, with a test device placed in the groove and affixed with a layer of thin double-sided silicon adhesive. The end of the device is affixed to the moving part of the vice with another piece of adhesive. The membrane is guided manually into the gap.

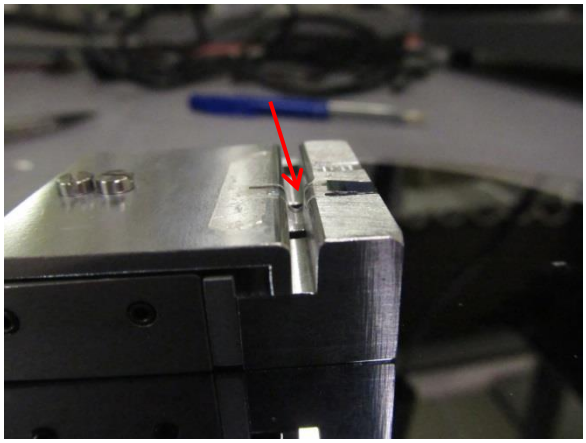


Figure 47: Bending tool with a device affixed and the membrane placed in a gap of 2 mm

The bending tool was taped onto a silicon carrier wafer and placed on the chuck of a manual probe station, which may be seen in Figure 48. A voltage sweep was done with the same parameters as for the accelerated aging test, with voltage limits of -10 V to 10 V and a step size of 0.1 V. The current was measured, and the resistance calculated according to Ohm's law.

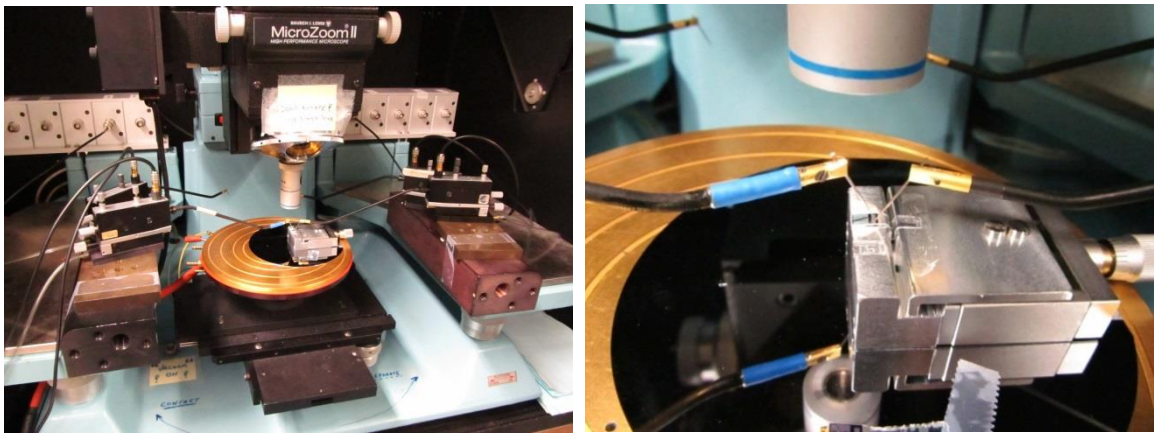


Figure 48: Bending tool on carrier wafer on the probe chuck with needles touching down on the bond pads.

The initial resistance measurement was made at a gap distance of 2 mm, since the device has been proven to be able to survive such a bending diameter during a test run. The resistance was then

measured at increments of 0.5 mm down to 1 mm, at which point the increment was decreased to 0.1 mm. At 0.5 mm, the increment was decreased further to 0.05 mm. For a full list of bending diameters, see Table 14.

The resistance was recorded for each bending diameter until the device failed.

5.2.3 Results

The resistance measurements made at each bending diameter may be seen in Table 14. Due to the limitations of the output data format from the probe station, the average value of resistance could only be estimated, and a value cannot be accurately given for the uncertainty. However, it is clear when the device has failed. The I vs. V curve from Device 1 at a bending diameter of 2 mm can be seen in Figure 49, with the calculated resistance indicated. The curve upon Device 1 failure at a bending diameter of 0.15 mm is shown in Figure 50.

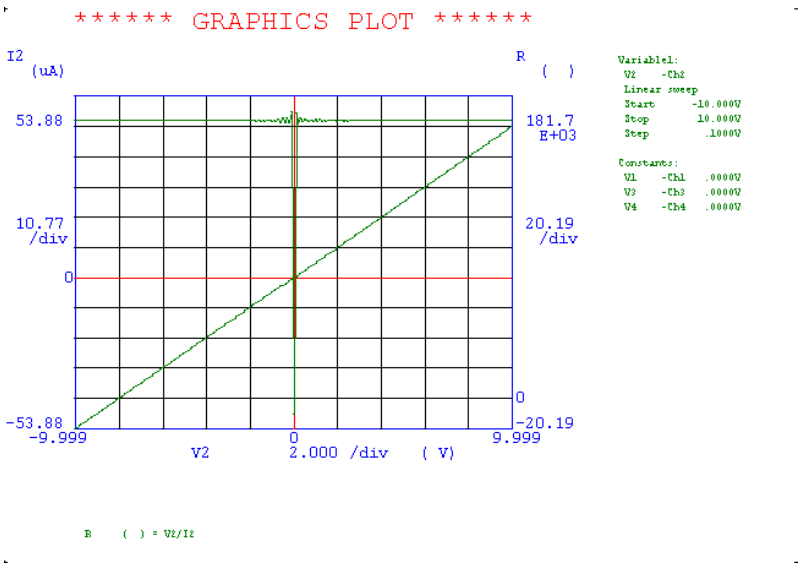


Figure 49: I vs. V plot for Device 1 with a bending radius of 2mm (beginning of test).

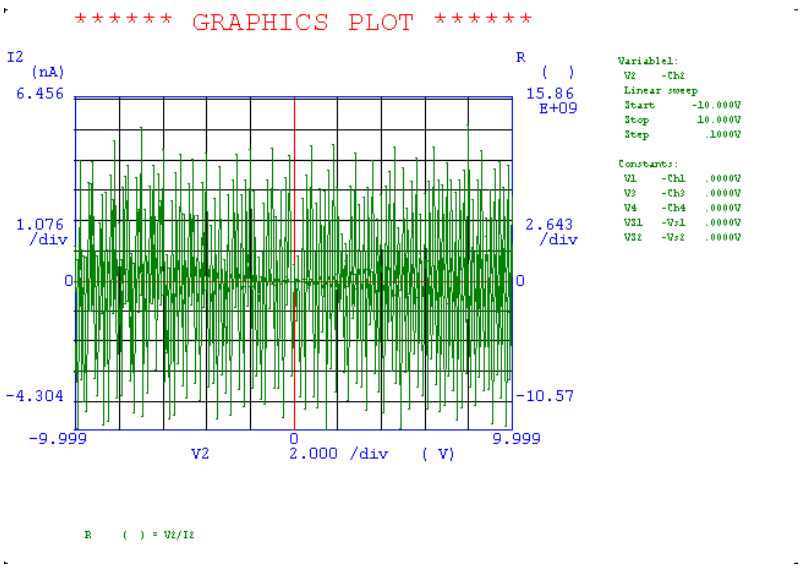


Figure 50: I vs. V plot for Device 1 with a bending radius of 0.15mm (on failure).

Device 1 failed at a bending radius of 0.15 mm, while Devices 2 and 3 both failed at 0.2 mm. Device 1 also sees an increase in the resistance once the bending radius has decreased below 0.5 mm. The other two devices did not show this trend, remaining at a constant resistance until failure. A more accurate method of resistance measurement that does not depend on an estimation from a graph should be done to check if the increase in resistance is a repeatable case. A plot of the results may be seen in Figure 51.

Table 14: Estimated meander resistance for bending diameter of the membrane

Diameter [mm]	Measured Resistance [Ω]		
	Device 1	*Device 2*	*Device 3*
2	185k	175k	173k
1.5	190k	176k	173k
1	187k	179k	171k
0.9	187k	177k	172k
0.8	185k	177k	172k
0.7	187k	176k	172k
0.6	185k	178k	173k
0.5	187k	178k	174k
0.45	197k	178k	172k
0.4	195k	178k	173k
0.35	200k	179k	171k
0.3	207k	178k	175k
0.25	195k	177k	174k
0.2	197k	∞	∞
0.15	∞		

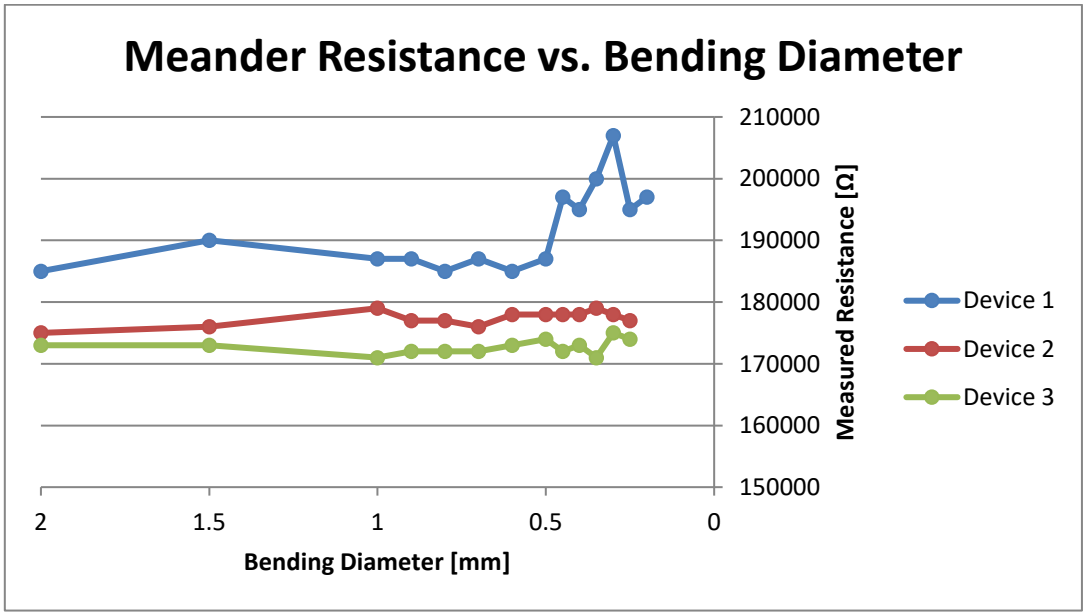


Figure 51: Resistance vs. bending diameter.

The devices were inspected optically and creases may be seen in the parylene membrane extending past the ceramics. No disconnects in the metal lines are visible, but any disconnects may be obscured by the cracked parylene.

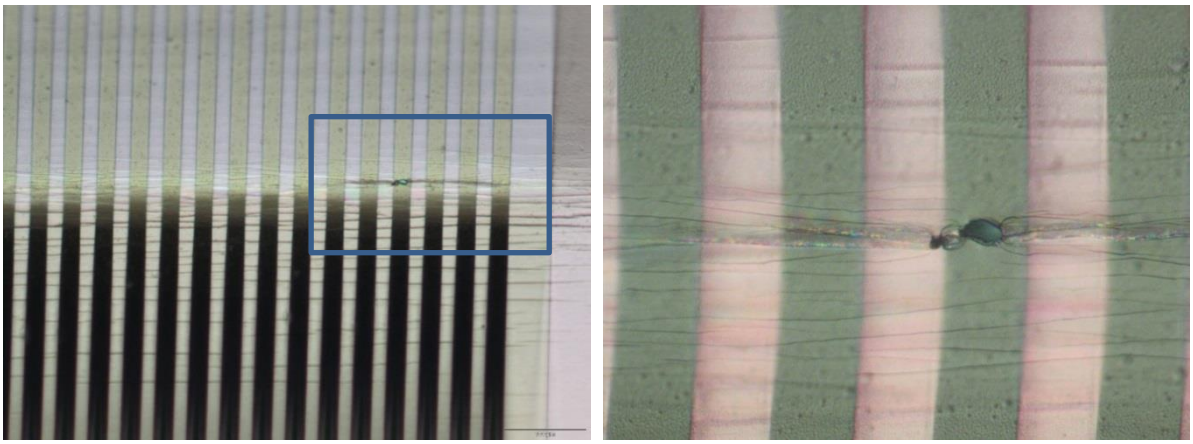


Figure 52: Device 2 after having been bent to .2 mm.

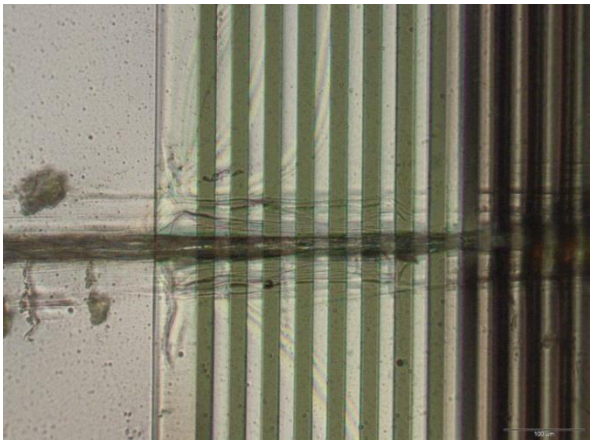


Figure 53: Test device that was folded and flattened completely.

5.2.4 Conclusions and Recommendations

All three devices tested were able to bend to 0.25 mm without failure. Two devices failed at 0.2 mm, while one device failed at 0.15 mm. For the two devices that failed at 0.2 mm, no observable differences in resistance, such as increases or nonlinearity, were observed. The slight increase in resistance in Device 1 was not seen again.

As one of the currently available lead kits for deep brain stimulation have a diameter of 1.27 mm [5], this process flow is capable of producing devices that may be bent to such a diameter, at least using TiN as metallization.

Recommended work would be to repeat the bending test using devices with platinum, as the results will be different. It would also be useful to continuously measure the resistance while decreasing the bending diameter to find the exact point at which the device fails and to see how the resistance changes around this point, but this was not possible with the available equipment. Another recommendation is to get more accurate resistance measurements, since the results from this test were estimated visually from the graphs and are therefore inaccurate.

6 CONCLUSIONS

In this thesis, a process flow was developed for the fabrication of flexible metal interconnects based on the Flex-to-Rigid platform. As the ultimate goal is to adapt F2R technology to be used for neural implants like deep brain stimulation electronics, the materials used for the interconnects must be biocompatible. The work done in this thesis is a continuation of Kanhai's work with focus on improving the adhesion and process flow of the parylene-based platinum electrodes and interconnects. However, due to the lack of platinum processing capability, titanium nitride was used as a substitution for platinum metallization.

This project introduced the addition of a ceramic encapsulation layer between the metal lines and the parylene encapsulation for improved adhesion and decreased permeability to water vapor. The order of the process flow steps was changed to incorporate the deposition of PECVD ceramic layers before the parylene deposition, which must be done at temperatures below 90°C. The "parylene last" approach demonstrated in this project allows for the wafer-scale fabrication of devices comprised of silicon chips with flexible interconnects in a single process flow by offering a less restricted temperature budget – up to 400°C – for IC fabrication.

The stress of the ceramic layers was found to be less than 100 MPa and tensile, indicating that the ceramic layers should not crack or buckle while on the wafer and the released membrane should show minimal curving. In order to incorporate the ceramic layers into the new process flow, two masks were designed and new technology modules were developed: the titanium buried mask layer for parylene patterning and the aluminum etch stop layer after the device release in DRIE.

For the titanium buried mask, a 200 nm layer of titanium deposited at 25°C was sufficient to mask the first parylene deposition. The lithography parameters were investigated to find the best method of performing the lithography, etching, and removal of the Ti layer at low temperature, and it was found that dry etching in gasses of Cl_2 and HBr produced the most even edges on the titanium structures. An efficient process flow step order for the deposition and patterning of the parylene and titanium layers was also investigated and confirmed to be compatible with the final process flow.

The optimal deposition parameters for the aluminum etch stop layer were investigated by depositing Al layers with different thicknesses and at different deposition temperatures on top of a layer of SiO_2, bombarding the surface of the Al in an SiO_2 plasma etch, and checking the underlying SiO_2 layer for defects that would indicate the presence of pinholes in the Al layer. An Al layer of 200 nm deposited at 300°C masked the SiO_2 well enough so that no defects were seen, and is thin enough to induce minimal stress to the stack and later be removed by wet etching in PES. Furthermore, since the layer is already deposited at high temperature, the following step of PECVD ceramic deposition at high temperature will not subject the Al to thermal modification.

The sizing of the Al etch stop layer was also investigated, and the etch stop was made to be 20 µm larger than the release mask based on the DRIE sidewall profile. However, after the wet etch intended to remove the Al etch stop layer, there is still aluminum remaining on the device, due to masking from the negatively sloped silicon sidewalls and the SiO_2 etch stop layer.

As titanium nitride was used for the metallization, a recipe was chosen for the deposition that resulted in relatively low sheet resistance and layer stress. The process flow confirmed that a 200 nm thick TiN metallization layer did not have pinholes or buckle due to stress, and would produce a device from which resistances could be measured. However, the exposed TiN was oxidized during several steps of the process flow, and etched during the removal of the titanium buried mask, resulting in higher sheet resistance of TiN than expected and difficulties when making electrical measurements.

The technology modules were integrated into the final process flow. Though the parylene to parylene adhesion needs to be improved, the "parylene last" approach resulted in the successful fabrication of a device with parylene and ceramic encapsulation. The device was released manually by cutting through the parylene tabs. The TiN electrode surfaces were oxidized and are not conductive, so no electrochemical tests can be carried out. However, the flexible interconnects were stress tested.

The first test performed was an accelerated aging test to check for corrosion of the metal lines or void formation, evaluated by measuring resistance to ensure there were no open circuits between the line of the meander and no short circuits between the comb and meander structures. After four weeks in PBS at an elevated temperature of 57°C in PBS (corresponding to 4 months of time at body temperature of 37°C), seven out of nine devices survived. The accelerated aging test included many uncontrolled variables, so it is uncertain if the data taken can be attributed to aging effects, but at least four devices showed no increase in resistance in the meander between the beginning and the end of the test.

The second stress test was a bending test to check the minimum bending diameter of the interconnects, evaluated by measuring changes in the resistance of the meander, with the device failing once the resistance indicated an open circuit. The devices were able to be bent to a diameter of less than 0.25 mm before breaks in the metal lines occurred. This bending diameter is smaller than state-of-the art neural probe lead kits, which have a diameter of 1.27 mm.

While several steps of the fabrication need to be optimized, the ability to successfully fabricate a device comprised of flexible parylene-based interconnects attached to a rigid silicon chip in a single process flow is demonstrated in this project. With some improvements to the process, flexible electrodes may be fabricated using this method as well.

6.1 RECOMMENDATIONS

Due to time limitations, work on this project was concentrated on developing a process flow and producing a device with working interconnects. Some steps in the process may be improved or investigated further.

The process flow was designed for metallization using platinum, so there are certain steps that are not compatible with titanium nitride. Using TiN as a substitution caused two main problems. The wet etch meant to strip the Ti buried mask would also etch the TiN electrodes, causing uneven metallization thickness on the bond pads and potentially bad electrical contact. Also, at several points in the fabrication process, the TiN was exposed to O_2 and CF_4 + SF_6 +O_2 plasma for parylene and ceramics etching respectively, which likely caused the oxidation/modification of TiN. This resulted in several complications, including a discrepancy between the theoretical and measured

resistances of the metal lines, variations in resistance between the center and the edge of the wafer due to the non-uniformity of the plasma etch in the Alcatel, and a layer of residue on top of the exposed bond pads and electrodes. Though electrical contact was still possible on the rigid bond pads, the electrodes on the flexible membrane were nonconductive.

The problems with TiN were not investigated further as using platinum for the metallization should solve them, since Pt stays inert when exposure to those conditions. If the fabrication is done with platinum, the reliability testing needs to be performed again, but it is likely that the resistance measurements would see less variability due to external factors such as bad contact to the bond pads, therefore providing more accurate data on aging effects.

Optical examination of the final device indicates that there is still Al present on the device, which needs to be removed to comply with the biocompatibility requirement. The main cause of this is that the slope of the bulk silicon sidewalls caused by the DRIE is masking the etch stop layers. A potential solution is to find a recipe for DRIE that results in more vertical sidewalls.

As both the sizing of the structures on the titanium buried mask and the aluminum etch stop layer are dependent on the area released by the DRIE step, once a new DRIE recipe is found and the sidewall angle is confirmed, the lithography parameters for the titanium buried mask and the aluminum etch stop layers may be optimized.

The membrane at the edge of the silicon island is prone to cracks and tearing. This problem was mitigated by rounding the corners of the silicon island, but cracks still originate predominantly from this point when devices are subjected to handling. A possibility to reduce handling errors is to put a drop of adhesive at the junction of the silicon island and the membrane so that the membrane does not break sharply at the edge. Alternatively, a new design for the silicon island may need to be developed.

Finally, several devices at the outer edges of the wafer showed delamination between the parylene layers from the two parylene depositions. The bottom encapsulating parylene layer from the second deposition separates from both the top parylene layer and the ceramics encapsulating the metal lines. Poor adhesion between parylene layers was not observed on devices in the middle of the wafer. This is likely due to the O_2 plasma treatment, which, for the second deposition, is done in the Alcatel and has non-uniformity between the center and edges of the wafer. O_2 plasma treatments should be omitted from the process flow, and only A-174 silane should be used as an adhesion promoter for parylene to silicon nitride adhesion. Another option for adhesion promotion is to activate the surface in a sputter etch for parylene to parylene adhesion. This change to the process flow is expected to increase parylene adhesion to both silicon nitride and parylene C.

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A.1 Device Release Using Back Side DRIE

When doing the deep reactive-ion etching (DRIE) step of the process flow in the Rapier Omega i2L DRIE etcher, the bulk silicon is removed from the device, leaving behind a membrane consisting of the parylene and ceramic encapsulation layers and the Al and SiO_2 etch stop layers. There is the possibility that the membranes will break during this step, exposing the metallization from the front side of the wafer to the Rapier chuck. The broken membranes can be seen in Figure A.54.

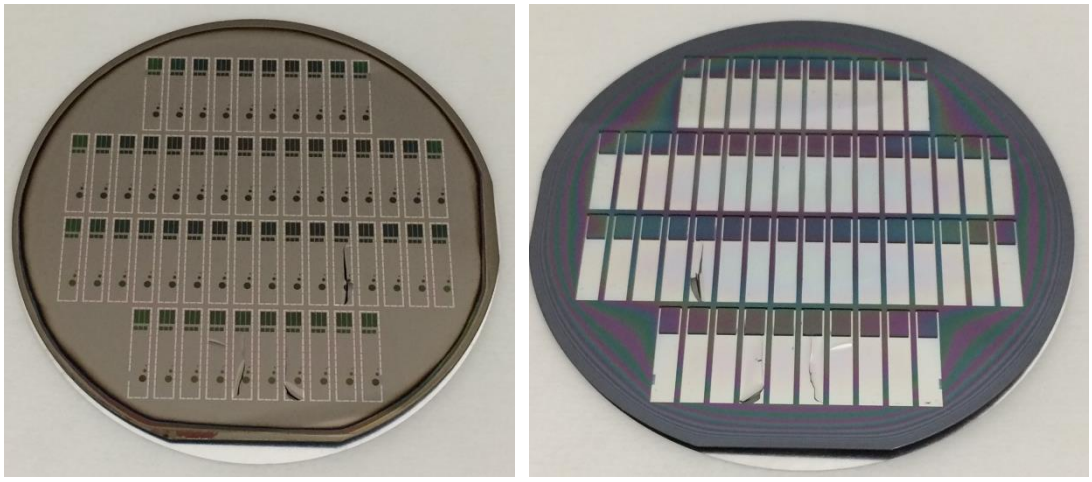

Figure A.54: Front side and back side of a wafer after DRIE with broken membranes. The back side DRIE hard mask used was the first version, with no rounded corners.

Performing the DRIE step on a wafer that uses platinum as the metallization material carries the risk of equipment or wafer contamination. Thus, the chuck must be protected from possible exposure when etching the bulk silicon. Several methods were investigated, including coating the front side of the wafer with a layer of photoresist or wax, or securing a carrier wafer to the process wafer using wax or tape. The following tests were developed as a means to find a sufficient protective layer for preventing platinum contamination on the chuck.

A.1.1 Process

The wafers used for these tests were 400 µm DSP wafers, with 6 µm of SiO_2 deposited on the back side, then patterned with the back side release mask and etched. 400 nm of SiO_2 was then deposited on the front side (step 1 in Figure A.54). This was followed by the aluminum etch stop layer deposition and patterning (step 2). The ~900 nm thick full ceramic stack was deposited with the same parameters as for the final flow, but with no metallization layer for the electrodes and no patterning of the ceramic (step 3). The parylene deposition was done after the standard O_2 plasma treatment (step 4). The amount of dimer used was 5 g, which corresponds to 2.4 µm ± 0.015 µm of parylene on the front and back sides. This was followed by 200 nm of Ti deposited on the front side (step 5), and then the back side parylene etch in the Omega, exposing the bulk silicon and the 6 µm SiO_2 backside mask (step 6). After the back side parylene is removed, the DRIE could be done (step 7).

Five wafers were prepared for this test. The goal is to maximize the process yield and minimize the risk of broken membrane and chuck contamination, and four methods of modifying the wafers for

the DRIE were evaluated: using the rounded release mask design, adding a reinforcing layer of photoresist, attaching a carrier wafer using wax, and the 2-step process.

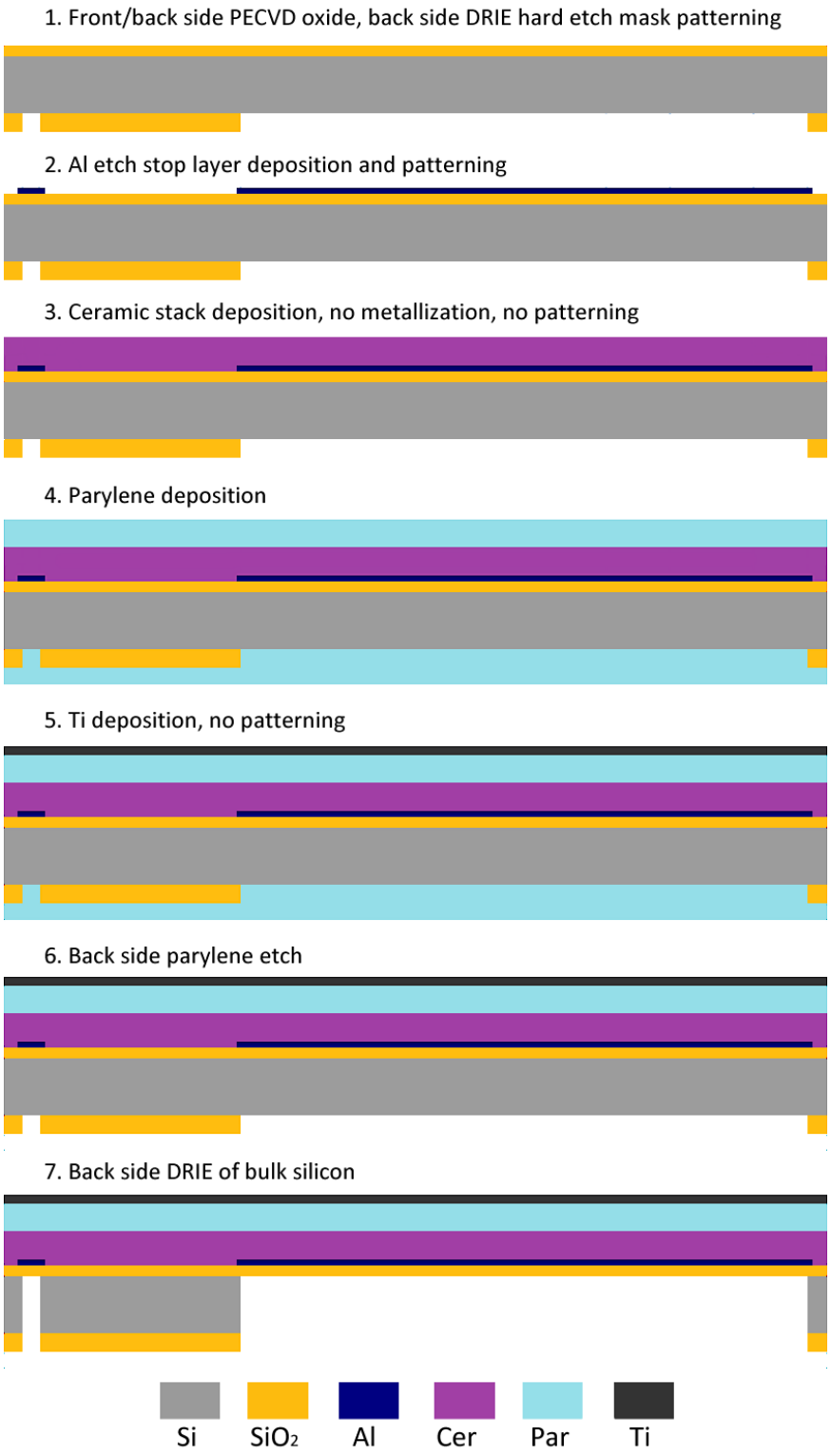

Figure A.55: Process flow for preparing DRIE test wafers.

A.1.1.1 Rounded Release Mask Design

Previous attempts at DRIE using Kanhai's mask without the rounded corners resulted in several broken membranes.

One wafer with the rounded release mask design (described in chapter 2), was etched for 470 cycles, a value calculated from the etch rate of a previous short loop, using the recipe 0_EKL_speed_10C_lowHe. No membranes broke. However, it was found that the etch rate of Si was faster than expected, at about 1.05 µm per cycle in the center of the wafer and 1.2 µm per cycle on the sides of the wafer, meaning that about 400 cycles would be sufficient to fully etch the bulk silicon. As no membranes broke, this method is sufficient for DRIE on non-contaminant containing wafers. The wafer after the DRIE is shown in Figure A.56.

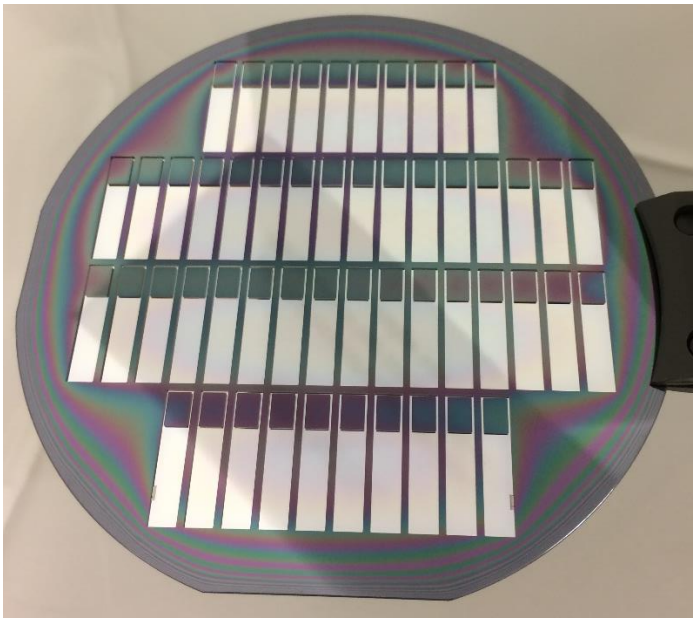

Figure A.56: DRIE done on a wafer with the rounded release mask with no broken membranes.

A.1.1.2 Photoresist Reinforcing Layer

The first method was the photoresist-protected wafer. The front side of the wafer that would face the chuck for a back side etch was coated with 3.1 µm of AZ3027 photoresist. The wafer was baked in the oven at 90°C for 30 min, then etched in the Rapier with the same recipe as the control wafer, resulting in three broken membranes. Thus, 3.1 µm of AZ3027 photoresist is not sufficient protection.

A.1.1.3 Carrier Wafer and Wax

The second method tested was to attach a carrier wafer to the front side of the process wafer using heat conductive wax. The process wafer had 2 µm of photoresist on the front side, in order to further protect the surface of the wafer from the wax, and underwent a 3 min hard bake at 95°C, followed by another 3 min hard bake at 95°C to harden the resist. On a hot plate at 50°C, wax was applied to the front side of a 300um DSP carrier wafer such that the entire middle of wafer was coated (Figure A.57(a)). The process wafer was aligned with the carrier wafer and placed on top, with the photoresist facing down. The wafer was then etched for 400 cycles in the Rapier. Some oxide remains on the wafer, as can be seen in Figure A.58(b).

It was found that the wax heated up in Rapier and the wafers became misaligned, so some taping would be required if this method were to be repeated (Figure A.57b). However, soaking for over 1 hour in either water or acetone, both of which the wax is soluble in, did not cause the wafers to separate. The wafers must be pulled apart, which causes the membranes to break and the process wafer to crack. This method of protection was abandoned for causing too much damage to the process wafer.

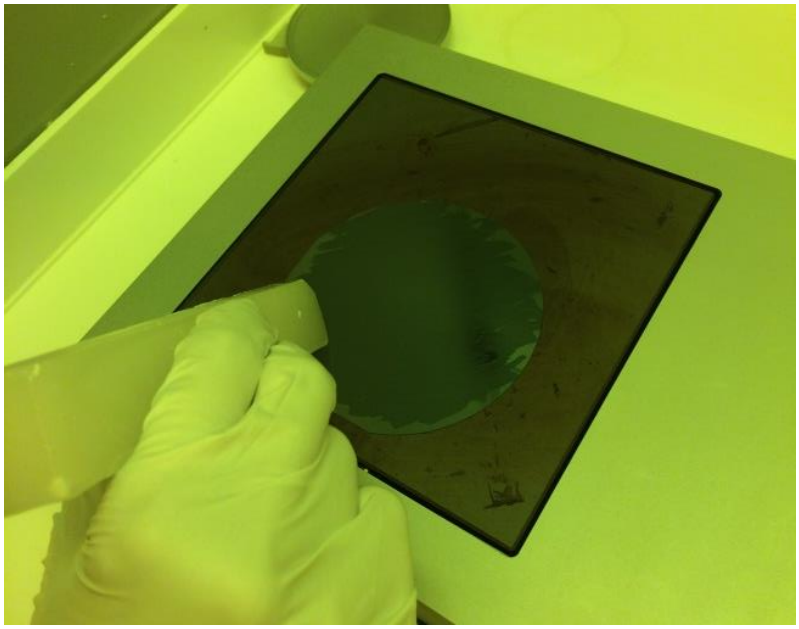

Figure A.57: Applying wax to carrier wafer.

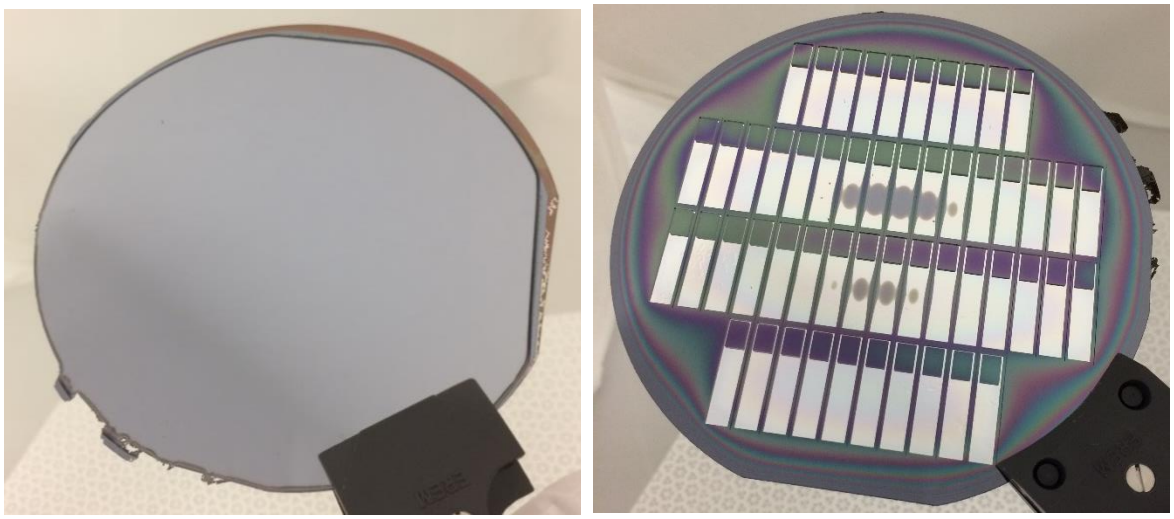

Figure A.58: Wafer misalignment after etch due to heating of wax from (a) the front side; (b) the back side. The center of the wafer shows some unetched oxide, but the DRIE was not completed.

A.1.1.4 2-Step Process

The last method tested was the 2-step process, in which a wafer is etched until there is thin layer of bulk silicon left, which is enough to prevent membranes from breaking. During the test the wafer was etched for 300 cycles, and the depth of the etch was measured using the Dektak. The center had 315 µm of Si etched and the side had 361 µm etched. The wafer is then attached to a carrier wafer with tape and the DRIE is finished, etching the remaining silicon.

The process wafer was aligned on top of a carrier wafer of SSP 500 µm with 2 µm SiO_2 from thermal oxidation on the front side, and taped on three sides. The locations of the tape are indicated by the arrows in Figure A.59(a). However, the carrier wafer was misaligned on one side, causing the tape on that side to come loose so the process wafer on top was seen to lift off with each cycle, and the result was that Ti was removed from the exposed areas on the front side, revealing the parylene layer. The front side of the test wafer after the etch is indicated in Figure A.59(b), with arrows indicating the locations where it was taped down. The red arrow indicates the misaligned tape.

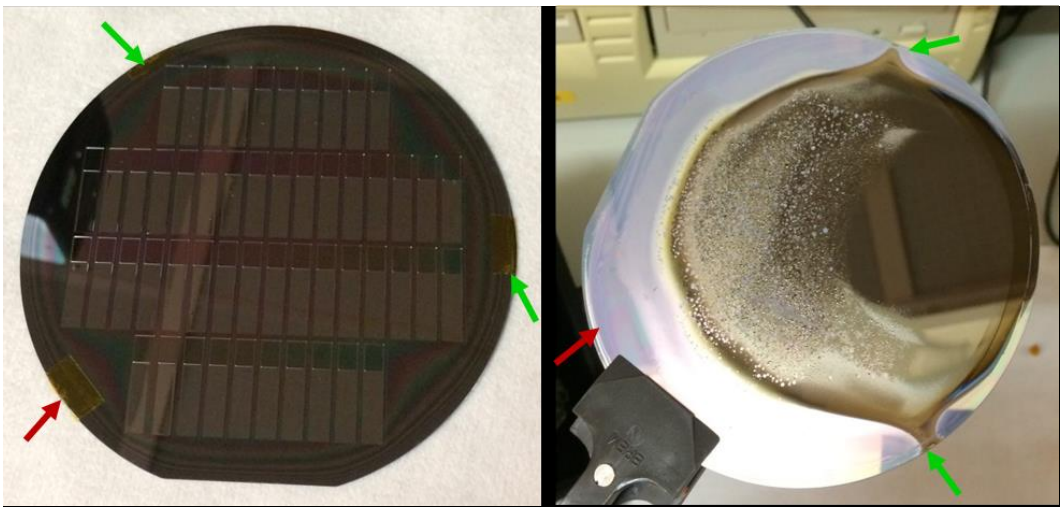

Figure A.59: (a) Process wafer with back side up taped where indicated to carrier wafer; (b) Front side of wafer after DRIE with removed Ti.

The etch was not completed. If the test were to be repeated, the 2-step method would be chosen for chuck protection. To reduce the chances of misalignment, the wafer should be taped on 4 sides. The edge of the wafer may be affected by the DRIE but the die in the middle of the wafer should be preserved. However, this test was stopped, and the process flow was continued with TiN used instead of Pt for the metallization.

A.1.2 Conclusion

The rounded back side DRIE etch mask design improves the yield, as no die broke on the test wafer etched with no carrier wafer, or on the final process wafer. It is unknown if it will prevent broken membranes entirely though, so a method of protecting the chuck must still be found.

Photoresist of a thickness of 3.1 µm does not prevent broken membranes, and may even cause them. It is not sufficient protection for the chuck.

Wax should not be used as it is very difficult to separate the carrier wafer from the process wafer.

Based on the results from this test, the 2-step option is the most viable method of protecting the chuck from platinum contamination in the case of broken membranes. However, it may lead to a yield loss on the edge die. The carrier wafer should be well-aligned and affixed to the process wafer.

A.2 FABRICATION FLOWCHART

Starting material:
4" double side polished wafers (Thickness 400 µm)

1. COATING AND BAKING
Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95°C for 1.5 minute.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co-3012-1.4-no EBR** (resist thickness: 1.4 µm). **Check that backside is clean before using stepper.**

2. ALIGNMENT AND EXPOSURE
Processing will be performed on the ASML PAS 5500/80 automatic waferstepper.
Follow the operating instructions from the manual when using this machine.

Mask: COMURK
Reticle ID: COMURK
Job: LITHO/epi0.0
Energy: 140 mJ/cm^2

3. DEVELOPMENT
Use the EVG 120 Coater/developer to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115°C for 1.5 minute, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100°C for 1.5 minute.
Always check the temperature of the hotplates first.

Use development program**: Dev - SP**.

4. INSPECTION: LINEWIDTH AND OVERLAY
Visually inspect the wafers through a microscope, and check the linewidth and alignment. No resist residues are allowed in openings or backside of wafer.

5. PLASMA ETCHING OF ALIGNMENT MARKS

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed !

(Use sequence **URK_NPD** for and set the platen temperature to **20 ºC** to etch ASML URK's into the silicon. Check if etched properly, check Si depth in Dektak, should be ~140 nm. Only then continue with next cleaning step.)

6. CLEANING PROCEDURE: TEPLA + HNO_3 100% and 65% (Si)

Plasma strip	Use the Tepla plasma system to remove the photoresist in oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use program **04**
Cleaning	10 minutes (15 minutes if acid is white) in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. Use wet bench "HNO_3 (100%)" and the carrier with the white dot.
QDR	Rinse in the Quick Dump Rinser with the standard program.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C (**check temp of bath**). Use wet bench "HNO_3 (65%)" and the carrier with the white dot.
QDR	Rinse in the Quick Dump Rinser with the standard program.
Drying	Use the Avenger "rinser/dryer" with the standard program, and the white carrier.

7. PLASMA ENHANCED SiO_2 DEPOSITION (6.0 µm) (BS)

Use the Novellus PECVD reactor to deposit a 6.0 µm thick SiO_2 layer.
Follow the operating instructions from the manual when using this machine.
The process conditions of the deposition program may not be changed !

Use ZeroStressOxide
Check logbook for time (previously: 84 s)

Measure SiO_2 thickness using LEITZ on test wafer. Check FS and BS for particles after deposition.

8. COATING AND BAKING HM FOR DRIE (BS)

Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3027M positive photoresist, and a soft bake at 95°C for 1.5 minute.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating Co-3027-4.0µm-NO EBR (resist thickness: 4.0 µm)

9. ALIGNMENT AND EXPOSURE (BS)

Check that wafer backside is clean before using stepper.
Processing will be performed on the ASML PAS 5500/80 automatic waferstepper
Follow the operating instructions from the manual when using this machine.

Mask: EC2228
Layer ID: RELEASE
Job: special/001project/EC2209/EC2209 → Note: EC2209 job is used since images on the reticles have correct position
Energy: 500 mJ/cm^2

Use backside alignment: P -> M, GLOBAL -> BACKSIDE4

10. DEVELOPMENT (BS)

Use the EVG 120 Coater/developer to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115°C for 1.5 minute, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100°C for 1.5 minute. Always check the temperature of the hotplates first.

Use development program: **Dev – DP1**.

11. INSPECTION: LINEWIDTH AND OVERLAY

Visually inspect the wafers through a microscope, and check the linewidth to ensure correct sizing of structures and alignment. No resist residues are allowed in openings or backside of wafer.

12. WINDOW ETCHING 6µm OXIDE (BS)

Use Drytek 384T plasma etcher with program **stdoxide**
Change the time to ~14 minutes (TEST ON ONE WAFER FIRST)
Follow the instructions when using this machine:

13. INSPECTION: LINEWIDTH AND OVERLAY

Visually inspect the wafers through a microscope, and check size. Oxide should be completely etched.

14. CLEANING PROCEDURE: TEPLA + HNO_3 100% and 65% (Si)

Plasma strip Use the Tepla plasma system to remove the photoresist in oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program **04**

Cleaning	10 minutes (15 minutes if acid is white) in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. Use wet bench "HNO_3 (100%)" and the carrier with the white dot.
QDR	Rinse in the Quick Dump Rinser with the standard program.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C (**check temp of bath**). Use wet bench "HNO_3 (65%)" and the carrier with the white dot.
QDR	Rinse in the Quick Dump Rinser with the standard program.
Drying	Use the Avenger "rinser/dryer" with the standard program, and the white carrier.

15. PLASMA ENHANCED SiO_2 DEPOSITION (400 nm) (FS)

Use the Novellus PECVD reactor to deposit a 400 nm thick SiO_2 layer.
Follow the operating instructions from the manual when using this machine.
The process conditions of the deposition program may not be changed !

Use ZeroStressOxide
Check logbook for time (previously: ~6.1 s for 410 nm)

Measure SiO_2 thickness using LEITZ. Check FS and BS for particles after deposition.

16. ALUMINUM DEPOSITION (200 nm) (FS)

Use Sigma recipe **Al_200nm_300°C** to deposit Al at high temperature (300°C).

17. COATING AND BAKING (FS)

Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95°C for 1.5 minute.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co-1.4-3012-no EBR** (resist thickness: 1.4 µm).

18. ALIGNMENT AND EXPOSURE (FS)

Processing will be performed on the ASML PAS 5500/80 automatic waferstepper.
Follow the operating instructions from the manual when using this machine.

Mask: EC2228
Layer ID: PAR1_VIA
Job: special/001project/EC2209/EC2209
Energy: 150 mJ/cm^2
Focus: 0 µm

Mask: COMURK
Layer ID: 1
Reticle ID: CLEARURK
Job: LITHO/clearurk
Energy: 150 mJ/cm^2
Focus: 0 µm

19. DEVELOPMENT (FS)

Use the EVG 120 Coater/developer to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115°C for 1.5 minute, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100°C for 1.5 minute.
Always check the temperature of the hotplates first.

Use development program**: Dev - SP**.

20. INSPECTION: LINEWIDTH AND OVERLAY

Visually inspect the wafers through a microscope, and check the linewidth and alignment. No resist residues are allowed in openings or backside of wafer.

21. AL ETCH AND OPENING OF ALIGNMENT MARKS (FS)

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed !

Use sequence **Al675TMP** with times 0:15/0:30/0:15 (first step always 15s. Keep consistent ratio of the last two step times)

22. CLEANING PROCEDURE: TEPLA + HNO_3 100% for Green Metals

Plasma strip	Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use program 4
Cleaning	10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%)" and the carrier with the red and yellow dot.
QDR	Rinse in the Quick Dump Rinser with the standard program.
Drying	Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.

23. STACK NITRIDE DEPOSITION (50nm) (FS)

Use the Novellus PECVD reactor to deposit a 50 nm thick SiN layer.
Follow the operating instructions from the manual when using this machine.
The process conditions of the deposition program may not be changed !
Use xxnm_std_sin
Check logbook for time (previously: ~2.35 s for 60 nm)

24. STACK OXIDE DEPOSITION (400nm) (FS)

Use the Novellus PECVD reactor to deposit a 400 nm thick SiO_2 layer.
Use ZeroStressOxide
Check logbook for time (previously: ~6.0 s for 400 nm)

25. TITANIUM/TITANIUM NITRIDE DEPOSITION (10nm/200nm) (FS)

Use Sigma recipe **Ti10_TiN200_STD_6kW** to deposit Ti/TiN at high temperature (350°C)

Deposit TiN using this recipe on extra test wafer to check the sheet resistance (and thus thickness) of the deposited layer. Previous sheet resistance measurement for this recipe: 17.11 Ω/sq

26. COATING AND BAKING (FS)

Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95°C for 1.5 minute.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co-1.4-3012-no EBR** (resist thickness: 1.4 µm).

27. ALIGNMENT AND EXPOSURE (FS)

Processing will be performed on the ASML PAS 5500/80 automatic waferstepper.
Follow the operating instructions from the manual when using this machine.

Mask: EC2228
Layer ID: METAL
Job: special/001project/EC2209/EC2209
Energy: 150 mJ/cm^2
Focus: 0 µm

Mask: COMURK
Layer ID: 1
Reticle ID: CLEARURK
Job: LITHO/clearurk
Energy: 150 mJ/cm^2
Focus: 0 µm

28. DEVELOPMENT (FS)

Use the EVG 120 Coater/developer to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115°C for 1.5 minute, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100°C for 1.5 minute.
Always check the temperature of the hotplates first.

Use development program**: Dev - SP**.

29. INSPECTION: LINEWIDTH AND OVERLAY

Visually inspect the wafers through a microscope, and check the linewidth and alignment. No resist residues are allowed in openings or backside of wafer.

30. METALLIZATION ETCH (FS)

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed !

Use sequence **TiNTiSVO** with times 0:30/1:00, check if fully etched. Change time of second step only, keep time 1 fixed.

31. CLEANING PROCEDURE: TEPLA + HNO_3 100% for Green Metals

Plasma strip	Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use program 4
Cleaning	10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%)" and the carrier with the red and yellow dot.
QDR	Rinse in the Quick Dump Rinser with the standard program.
Drying	Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.

32. STACK NITRIDE DEPOSITION (15nm) (FS)

Use the Novellus PECVD reactor to deposit a 15 nm thick SiN layer. Requires use of **Uniformity Mode** for a thin layer.

Use xxnm_std_sin

Check logbook for time (previously: ~4.3 s in Uniformity Mode for 16 nm)

Uniformity Mode: Requires eight wafers to be placed in the carrier. During deposition, each chuck holds one wafer. The deposition time specified in the recipe is the actual deposition time for each wafer. In order to keep the deposited thickness between wafers as consistent as possible, the process wafers should be placed in slots 3-6 of the carrier, as a test deposition of 15 nm of SiN on eight Si wafers showed the wafers in these slots to have the least variation. See Figure 60 for representation of chucks.

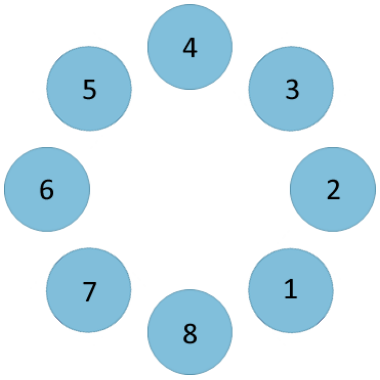

Figure 60: Representation of chucks in the Novellus and the corresponding wafer carrier slot in Uniformity mode.

33. STACK OXIDE DEPOSITION (400nm) (FS)

Use the Novellus PECVD reactor to deposit a 400 nm thick SiO_2 layer.

Use ZeroStressOxide

Check logbook for time (previously: ~6.0 s for 400 nm)

34. STACK NITRIDE DEPOSITION (50nm) (FS)

Use the Novellus PECVD reactor to deposit a 50 nm thick SiN layer.

Use xxnm_std_sin

Check logbook for time (previously: ~2.35 s for 60 nm)

35. COATING AND BAKING (FS)

Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95°C for 1.5 minute.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co-Topo-2.1-3012-no EBR** (resist thickness: 2 µm).

36. ALIGNMENT AND EXPOSURE (FS)

Processing will be performed on the ASML PAS 5500/80 automatic waferstepper.
Follow the operating instructions from the manual when using this machine.

Mask: EC2228
Layer ID: PAROPEN
Job: special/001project/EC2209/EC2209
Energy: 200 mJ/cm^2
Focus: 0 µm

Mask: COMURK
Layer ID: 1
Reticle ID: CLEARURK
Job: LITHO/clearurk
Energy: 200 mJ/cm^2
Focus: 0 µm

37. DEVELOPMENT (FS)

Use the EVG 120 Coater/developer to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115°C for 1.5 minute, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100°C for 1.5 minute.
Always check the temperature of the hotplates first.

Use development program**: Dev - SP**.

38. INSPECTION: LINEWIDTH AND OVERLAY

Visually inspect the wafers through a microscope, and check the linewidth. No resist residues are allowed in openings.

39. CERAMIC ETCH (FS)

Use the Alcatel plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed !

Use Oxide etch recipe, check if fully etched. Etch time ~24.5 min

40. CLEANING PROCEDURE: TEPLA + HNO_3 100% for Green Metals

Plasma strip — Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 4

Cleaning — 10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature.
Use wet bench "HNO3 (100%)" and the carrier with the red and yellow dot.

QDR	Rinse in the Quick Dump Rinser with the standard program.
Drying	Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.

41. TEPLA PLASMA O_2 TREATMENT

Use Tepla plasma system recipe number **2** to promote adhesion for the first Parylene deposition (makes surface more hydrophilic). Next step (Parylene deposition) has to be done within half an hour.

42. PARYLENE DEPOSITION 6 µm ± 0.5 µm (MEMS)

Use Parylene deposition chamber in MEMS lab
Use: 13g → 6 µm ± 0.5 µm with A-174 Silane *adhesion* promoter. Always 5 wafers in chamber (for consistent thickness)

43. MEASURE THICKNESS PARYLENE/ OPTICAL INSPECTION

Use LEITZ to measure the thickness of the parylene in the area where parylene is on top of only oxide at the edge of the die (see Figure 61). Use Par on Si, then subtract oxide (value from step 2) to estimate parylene thickness. Also inspect the surface for bubbles and uniformity.

Figure 61: Arrows indicate where parylene layer thickness may be measured using LEITZ.

44. BURIED MASK TITANIUM DEPOSITION (200nm) (FS)

Use Sigma recipe **Ti_200nm_25°C** to deposit Ti at low temperature (25°C). Temperature must be low for the parylene. No sputter etch before deposition. Use carrier wafer due to parylene on BS of wafer.

Before deposition perform a LUR (Leak-Up Rate) test of 1 wafer (if the batch has ~5 wafers).

45. PARYLENE ETCH (BS)

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed !

Use sequence **Par3** for 7:30 min, etch rate ~ 940 nm/min

The SiO_2 release mask can be slightly etched in that step as the Par3 recipe is not selective to the oxide.
After this step check the FS of the wafer for particles.

46. COATING AND BAKING (FS)

Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment.
NO HMDS, no temp > 100°C (only bake on coater 95°C)
Spin coating with Shipley SPR3027 positive photoresist.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use soft bake recipe: **Only-SB on coater** **or bake on HP @95°C for 90s**
Use coating recipe: **SpeCo-Topo-3027-3,1µm-no HMDS no EBR** (resist thickness: 3.1 µm).

47. ALIGNMENT AND EXPOSURE (FS)

Processing will be performed on the ASML PAS 5500/80 automatic waferstepper.
Follow the operating instructions from the manual when using this machine.

Mask: EC2209
Layer ID: ParOpen
Job: special/001project/EC2209/EC2209
Energy: 420 mJ/cm^2
Focus: 0

48. DEVELOPMENT (FS)

Use the EVG 120 Coater/developer to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 95°C for 3 minute, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100°C for 1.5 minute.
Always check the temperature of the hotplates first.

Use PEB recipe: **Only-SB-3 min on Developer** **or bake on HP @95°C for 3 min**
Use development recipe: **1-DEV-DP1-no PEB**

49. INSPECTION: LINEWIDTH AND OVERLAY

Visually inspect the wafers through a microscope, and check the linewidth and alignment. No resist residues are allowed in openings or backside of wafer.

50. TI BURIED MASK ETCH (FS)

Use the Omega plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed !

Use **TinTiSVO** recipe for 0:30/1:15 min, check if fully etched using Dektak.

51. PR STRIP (FS)

Acetone spin clean using Mapper recipe to remove photoresist. Resist residues may be left on edges of structures.

52. PR RESIDUE ETCH (FS)

Use Alcatel to etch photoresist residues using the **Parylene** recipe (O_2 plasma: 70 sccm, Power: 60W) Etch time: 1 min

53. DRIE ETCH BULK SILICON (BS)

Use Rapier to etch silicon using low pressure He recipe to prevent membrane breaking.
Stop on oxide.
Use recipe **0EKL_Speed_10C_lowHe** for 400 cycles (test etch rate on dummy wafer first, previously was ~1.05 µm/cycle)

54. MEASURE THICKNESS SiO_2 (BS)

Using LEITZ SiO_2 recipe to measure the BS oxide release mask thickness.

55. ETCH OXIDE (BS)

Use Alcatel for oxide etch **(no clamping on wafer due to membranes)**
Use oxide etch recipe for 14 min (etch rate 39nm/min) to remove 400 nm SiO_2 etch stop layer. Check the BS oxide release mask thickness on LEITZ, subtract from previous step measurement. To ensure that all 400 nm oxide is etched, ~500nm of the BS oxide release mask should be etched.

56. REMOVE AL STOP LAYER (BS)

Triton for 1 hour, remove Al using PES in SAL lab at 20°C. Etch for at least 6 min, check visual results due to varying etch rate. Rinse (1 hr) and spin dry, then leave in wafer box to dry (24 hr).

57. ALCATEL PLASMA O_2 TREATMENT

Use Alcatel plasma etcher to promote adhesion for the second Parylene deposition. 1 minute using the Parylene recipe (O_2 plasma: 70 sccm, Power: 60W). Next step (Parylene deposition) has to be done within half an hour.

58. SECOND PARYLENE DEPOSITION 6 µm ± 0.5 µm (MEMS)

Use Parylene deposition chamber in MEMS lab
Use: 13g → 6 µm ± 0.5 µm with A-174 Silane adhesion promoter. Always 5 wafers in chamber (for consistent thickness). Measure parylene deposition thickness on test wafer.

59. PLASMA ETCH PARYLENE 9µm (FS)

Use Alcatel to etch ~18 µm of parylene using the Parylene recipe (O_2 plasma: 70 sccm, Power: 60W)
Etch rate ~210 nm/min. Etch time total 90 min (~30 min for each 6 µm layer of parylene). Do three separate etches of 30 min each.

60. REMOVE TITANIUM BURIED MASK (200nm) (FS)

Triton for 1 hour, remove Ti using aged (24 hr) wet etchant SC-1 (1 part H_2O, 1 part H_2O_2 31%, 1 part NH_4OH 28%). 3 min etch time. Rinse (1 hr) and spin dry, then leave in wafer box to dry (24 hr).