Experimental Analysis and Circuit-Level Mitigation Strategies for Intermittent Errors in Resistive RAMs

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***Abstract*—Resistive RAM (RRAM) design optimization and error monitoring is crucial for memory storage applications but also to enable future brain-inspired systems beyond the capabilities of today's hardware. The figure-of-merit confirming the presence of resistive switching in RRAM devices is its resistance window expressed by the HRS/LRS ratio (High Resistance State over the Low Resistance State). This ratio guarantees the proper operation of the RRAM: the larger the ratio, the more reliable and robust the RRAM cell becomes in storing and retrieving data. From this perspective, this paper proposes an analysis of RRAM intermittent errors with respect to the RRAM resistance ratio. The impact of intermittent errors on the HRS/LRS ratio is analyzed at the RRAM cell electrical level using a dedicated test chip. Silicon measurements show that all detected RRAM intermittent errors directly result from resistance drifts due to ineffective programming operations. In view of these findings, intermittent error mitigation schemes are proposed to address these errors at the circuit level.**

***Index Terms*—RRAM, OxRAM, test, variability, reliability, emerging memory.**

I. Introduction

In RRAM, binary data is typically represented by two resistance states: a high resistance state (HRS) and a low resistance state (LRS), representing the '0' and '1' states, respectively [1], [2]. The difference between the HRS and LRS values is referred to as the resistance window. The resistance window is an important parameter of RRAMs as a larger resistance window leads to improved reliability [3]. The resistance window can be influenced by a variety of factors, including the type of material used for the memory element, the device geometry, and the processing conditions [4].

Although research is ongoing to develop new materials and optimize the device structure to achieve larger resistance windows and better performance for RRAMs, the technology still suffers from intermittent errors [5] and hard errors [6]. Hard errors are a permanent corruption of a memory cell resulting from physical defects, improper handling or incorrect usage of the memory cells, while intermittent errors, addressed in this study, are related to a random, recoverable upsetting of the information stored in a memory cell. Indeed, once the fabrication process is optimized, it has been demonstrated that RRAM resistance can unpredictably become stuck at one resistance state for some time and suddenly recover to normal operation [7]. This drawback of the technology results from the stochastic dynamics of the resistive switching (i.e., oxygen vacancies motion resulting in temporal variability [8], [9]). Hence, to provide high-grade RRAM solutions and accelerate RRAM integration in commercial products, a comprehensive understanding of intermittent errors is required to develop dedicated error-resilient architectures [10].

Although many publications have addressed intermittent errors in conventional Non-Volatile Memories (NVM) [11], much work, however, remains to be done regarding RRAM intermittent errors. Most prior work tackles hard errors following endurance cycling or retention tests [12]. For instance, it has been demonstrated in [13] that RRAM devices fail during cycling because of the degradation of their microstructure, often associated with the formation process of atomic vacancies in the insulator [14]. Also, thermal effects related to the high currents flowing in the LRS state can also contribute to accelerate the degradation of the insulator [15]. When it comes to intermittent errors, most of the work focuses on modeling [5] and system-level impact of intermittent errors [16], along with dedicated mitigation schemes [6], [17], [18]. These latter schemes have been addressed in several applications including RRAM-based neuromorphic systems [5]. Alternatively, in environments exposed to radiation, intermittent errors related to single-event-effect (SEE) have been extensively studied [19].

In this work, we do not investigate the physical, chemical, or thermal mechanisms responsible for the uncontrolled motion of oxygen vacancies, identified as the primary source of intermittent errors in RRAM [18]. Instead, we build on experimental data to present a comprehensive analysis of intermittent errors from an electrical perspective. Based on this analysis, we propose tailored design schemes that effectively address these errors while ensuring precise control of RRAM programming currents.

The main contributions of this article are the following:

- Intermittent errors are first detected by evaluating the resistance window of each cell of a RRAM test chip.
- After detection, a deep analysis of intermittent errors is conducted on individual cells.

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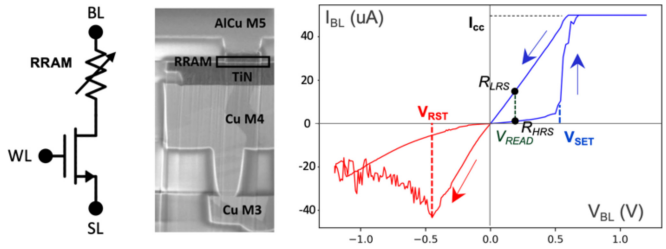


(a) (b) (c)

Fig. 1. (a) Symbol view of a 1T1R cell. (b) SEM cross section of the RRAM stack [20]. (c) RRAM I-V characteristic showing a hysteresis shape with RRAM key parameters highlighted (R_{LRS}, R_{HRS}, V_{SET} and V_{RST}).

- Experimental results are discussed, and intermittent error mitigation schemes are proposed.

Outcomes of this study are supported by experimental data related to an Oxide-based RAM (OxRAM) technology (*10nm-HfO_2/10nm-Ti/TiN* stack) [12].

The remainder of this paper is organized as follows. Section II introduces RRAM technology. Section III outlines the experimental setup used for detecting intermittent errors. Section IV focuses on the analysis of intermittent errors in RRAM. In Section V, mitigation techniques for intermittent errors are presented. Section VI discusses the occurrence of these errors and analyzes the results. Finally, Section VII concludes the paper.

II. RRAM Technology Background

Fig. 1a shows a basic 1T1R memory device where one NMOS transistor (W = 0.8 µm, L = 0.5 µm and V_{th} = 0.7 V) is connected in series with one RRAM cell. The RRAM resistive stack is integrated in the Back End Of Line (BEOL) of a 130 nm technology, between M4 and M5 layers as presented in Fig. 1b [20]. The RRAM stack is fabricated on S(100) undoped test wafers pre-oxidized with 500 nm wet silicon oxide. The Bottom electrode (BE) is made of a 150 nm TiN layer with a sheet resistance of 10-50 Ω/sq, prepared by physical vapor deposition (PVD) sputtering. A 10 nm Hafnium dioxide (HfO_2) layer is deposited at 320 °C by the reaction of O2 and tetrakis(ethylmethylamido)-hafnium [Hf(NMeEt)4] onto TiN in an atomic vapor deposition (AVD) chamber. Finally, a Ti/TiN bilayer stack is then deposited: HfO_2 is capped by a 7 nm ionized metal plasma Ti and a 150-nm PVD TiN acting as the top electrode (TE). Fig. 1c shows a typical 1T1R I-V characteristic. Based on this I-V curve, the memory cell operation can be seen as follows: after an initial electro-Forming (FMG) step, the memory element can be switched in a reversible manner between LRS and HRS. Resistive switching corresponds to an abrupt change between the HRS and the LRS. The resistance change is triggered by applying specific biases across the 1T1R cell, i.e., V_{SET} to switch to LRS after a SET operation and V_{RST} to switch to HRS after a RESET (RST) operation.

The voltage levels used during the different operating stages are presented in Table I, along with the expected resistance values. In the 1T1R configuration, during FMG or SET operations, the transistor controls the current level flowing through the cell according to its gate voltage bias. This clamping current is referred to as compliance current (I_{CC}). The read operation needs to be performed non-destructively to not modify the stored data. Typically, a small read voltage (around 0.1 V) is chosen to not disturb the current state of the cell. This allows for read operations to be performed repeatedly without affecting the reliability of the memory device. In practice, at the circuit level, the read operation is performed by measuring the resulting current associated with the LRS/HRS resistances to determine whether the cell is in logic '0' (HRS) or in logic '1' (LRS).

TABLE I
RRAM Cell Operating Voltages During FMG, RST, SET and READ Stages

	FMG	RST	SET	READ
WL	2 V	2.5 V	2 V	2.5 V
BL	3.3 V	0 V	1.2 V	0.1 V
SL	0 V	1.2 V	0 V	0 V
Resistance	10 kΩ	240 kΩ	15 kΩ	-

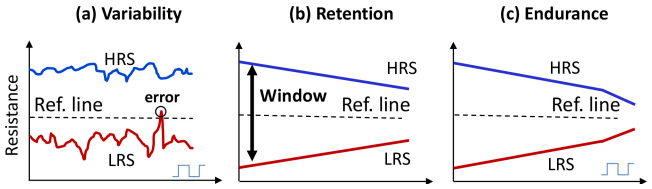


Fig. 2. Schematic diagram of the three standard RRAM reliability metrics (a) variability, (b) retention and (c) cycling endurance.

One of the most important challenges of RRAM technology is the control of the device variability (temporal and spatial) in both LRS and HRS states [21], [22]. In fact, variations of R_{HRS}/R_{LRS} are so unpredictable that they have been employed as an entropy source in True Random Number Generators (TRNG) [10], [23]. In addition to variability, over time, RRAM devices fail due to endurance or retention degradation [24]. Fig. 2 shows schematic diagrams of three RRAM critical reliability metrics: variability, plotted versus the number of programming cycles (Fig. 2a), retention, plotted over time (Fig. 2b) and cycling endurance (Fig. 2c), also plotted versus programming cycles. Note that retention and endurance are related to time-dependent reliability metrics whereas variability, as well as intermittent faults, are related to time-zero (i.e., independent of time) reliability metrics [25].

Also, no matter the reliability metric (variability, retention or endurance), the reliability evaluation process is periodically interrupted and the resistance window is assessed during a read operation [26]. Therefore, the reliability evaluation mainly cares about the resistance window and the capacity to maintain HRS and LRS levels on each side of the dashed reference line (see Fig. 2). Also, for retention and endurance, the initial resistance window value plays an important role as it constitutes the starting point of the degradation process. Hence, maximizing the resistance window at time zero and during the device lifetime is a key point to ensure functionality as well as reliability.

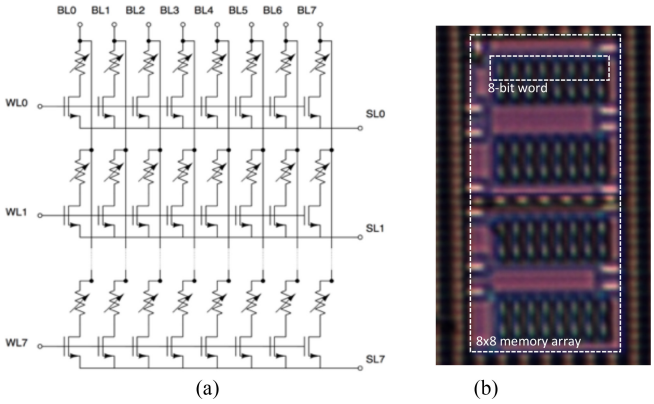


Fig. 3. (a) 8x8 RRAM memory array and (b) corresponding micrograph of the memory array test chip fabricated in a 130 nm CMOS technology.

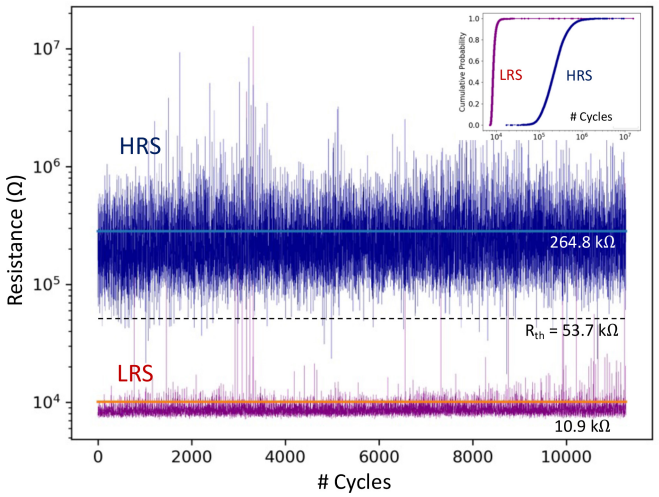


Fig. 4. R_{HRS} and R_{LRS} in logarithmic scale over 230 cycles applied to the 7x7 memory array (11 270 cycles). R_{th} (53.7 kΩ), HRS (264.8 kΩ) and LRS (10.9 kΩ) mean values are also provided.

III. Experimental Setup

A. Test Chip Presentation

Fig. 3a presents the test chip considered for measurements which is a classical 1T1R array. Memory cells are grouped to form eight 8-bit memory words. Word Lines (WL_X) are used to select the active row, Bit Lines (BL_X) are used to select active columns during a SET operation and Source Lines (SL_X) are used to RST a whole memory word or an addressed cell. To allow full flexibility during characterization, BL, WL and SL nodes are externally available. A Keysight B1500 semiconductor parameter analyzer is used for measurements [23]. During the RRAM cell programming, the extraction of R_{LRS} and R_{HRS} is achieved using 1 ms DC voltage sweeps with a 1 mV voltage step. The applied voltage incrementally increases and decreases and the current flowing through the cell is monitored at each voltage step, allowing an extraction of the I-V characteristics of each cell [27]. Fig. 3b presents a view of the fabricated memory array. Due to the limited pin out of the probe card, only a 7x7 memory array is available for our experiments (i.e., a subset of the 8x8 array).

TABLE II
R_{HRS} & R_{LRS} Distribution Parameters Obtained After 11 270 RST/SET Operations

Resistance state	Mean Value (kΩ)	Std. dev. (kΩ)
HRS	264.8	183
LRS	10.9	3.46

Before any operation, the memory array is first formed (FMG). Then, memory cells are RST one by one to extract the R_{HRS} value at 0.1 V. After RST, cells are SET to extract the R_{LRS} value, also at 0.1 V. The RST/SET process is repeated 230 times for the whole array in order to catch cycle-to-cycle (C2C) as well as device-to-device (D2D) variability. Hence, 11 270 (230 x 49) I-V characteristics are obtained for analysis. This number enables catching an acceptable number of failing cells without wearing out the memory cells. Indeed, our study focuses on detecting intermittent errors, which are not time-dependent. Consequently, each cell in the array undergoes only 230 programming cycles. Note that collecting I-V characteristics is a relatively slow process, compared to voltage pulse programming approaches, however, we believe that this is the best way to precisely extract R_{HRS} and R_{LRS} in each programming cycle.

B. Preliminary Results

Fig. 4 presents the evolution of R_{HRS} and R_{LRS} extracted at 0.1 V in a logarithmic scale versus the number of programming cycles. Considering the memory array of Fig. 3a, the programming operation (RST followed by a SET operation to extract HRS/LRS levels) is performed line by line, starting from WL0 to WL7 to cover the whole memory array. For each line, the bit line number is increased up to the end of the line (WL0-BL0 to WL0-BL7, WL1-BL0 to WL1-BL7, and so forth). This operation is repeated 230 times. When analyzing Fig. 4, many HRS and LRS level overlaps are clearly visible (i.e., resistance ratio < 1). Fig. 4 inset uses a cumulative distribution function (CDF) to show from a different perspective how HRS and LRS levels differ and overlap. Also, HRS fluctuations are more pronounced compared to LRS ones, which is a common feature of the considered technology [28]. This observation is confirmed by R_{HRS} and R_{LRS} distribution parameters summarized in Table II.

HRS mean value is equal to 264.8 kΩ whereas the LRS one is equal to 10.9 kΩ, resulting in an average resistance window of 253.9 kΩ and an average resistance ratio of 24.3. The HRS standard deviation is equal to 183 kΩ, much higher compared to the LRS one, equal to 3.46 kΩ. A threshold resistance R_{th}, represented as a dashed line in Fig. 4, allows **distinguishing** HRS and LRS resistance states. Although the R_{th} can be set dynamically, an optimal fixed R_{th} value is usually calculated according to (1) [29], with a value equal to 53.7 kΩ in our study. This approach of calculating R_{th} ensures that the threshold takes into account the variability of both HRS and LRS resistances, providing a more robust and dynamic method for distinguishing between the two states,

TABLE III
R_{HRS}/ R_{LRS} RATIO DISTRIBUTION

Ratio range number	Ratio range (R_a)	Number of RST/SET cycles	%	Current margin (A)
1	*0< R_a <1*	6	0.053	-
2	*1< R_a < 2*	4	0.035	1.74e-08
3	*2< R_a < 3*	5	0.040	2.84e-07
4	*3< R_a < 4*	7	0.062	3.44e-07
5	*4< R_a < 5*	15	0.13	7.70e-07
6	*5< R_a <6*	31	0.27	1.78e-06
7	*6< R_a <7*	38	0.33	3.98e-06
8	*7<R_a <10*	320	3.78	4.07e-06
9	*10< R_a <15*	1522	17.28	4.38e-06
10	*15< R_a <20*	1823	33.46	4.87e-06

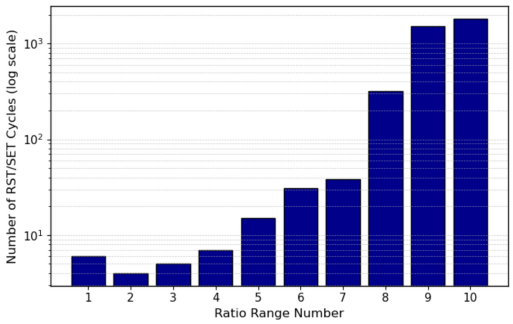


Fig. 5. Ratio range number versus the number of RST/SET cycles in log scale.

especially in cases where the states are not symmetrical [30].

$$R_{\text{th}} = \sqrt{264.8\ x10.9} = 53.7\ k\Omega \quad (1)$$

IV. ANALYSIS OF RRAM INTERMITTENT ERRORS

A. Intermittent Error Detection

Table III presents the number of programming cycles associated with specific R_{HRS}/R_{LRS} resistance ratios (referred to as R_a). These ratios are chosen to be lower than 20.

The ratio range number is given in column 1 while the corresponding ratio interval is given in column 2. The number of programming cycles falling in each ratio interval is presented in the third column. 6 cycles out of 11 270 provide a ratio *Ra* in the interval *'0 < Ra <1'*, which represents 0.053% of the total number of cycles (column 4). This scenario is the most critical one as it leaves no room for memory state differentiation (HRS and LRS states overlap). 4 cycles provide resistance ratios in the interval *'1< Ra <2'*. For the following ratio intervals, the number of cycles increases to 5, 7, 15 and 31. Then, the number of cycles increases exponentially up to 1,823 for increasing ratio range numbers.

Fig. 5 pictures the relationship between the ratio range number and the number of RST/SET cycles falling in each ratio range, in log scale. The bar plot shows an exponential-like growth in cycle count as the ratio range number increases, particularly beyond range 7. Ranges 8, 9, and 10 show a sharp increase, reaching up to 1,823 cycles for the highest ratio range.

Typically, the differentiation between the HRS/LRS memory states is achieved at the circuit level using sense amplifiers. In general, the current resolution of sense amplifiers used in non-volatile memories is typically in the range of microamps (μA) to nanoamps (nA). A higher resolution allows for better differentiation between the different states of the memory cells [31], leading to an improved read accuracy and reduced read disturb errors [29]. However, achieving high resolution requires additional complex circuitry, which increases the power consumption and manufacturing costs. To account for circuit level considerations, the HRS/LRS resistance margin (i.e., resistance difference) is transposed into a current margin. Column 5 of Table III presents the worst-case minimal current difference between the HRS and LRS states considering all the cycles of each resistance ratio interval. The reported current margins, varying from 17.4 nA to 4.87 μA, are extracted at 0.1 V. Note that these currents must be seen in the context of modern sense amplifiers which can reach a resolution of 50 nA [31].

Beyond the resistance ratio, the precise range of HRS/LRS resistance values also matters. Indeed, HRS/LRS ratios equal to 10:1 or 1000:100 give the same ratio (10), but if some devices operate in such different resistive ranges, it means the HRS of one device is lower than the other's LRS, which is undesirable. One way to address this aspect was to introduce the HRS/LRS currents, directly linked to the resistance range. Another safeguard implemented to prevent this situation involves verifying that the HRS and LRS resistances remain, respectively, higher and lower than the threshold resistance value R_{th} (see Fig. 4).

B. 2D Resistance Ratio Analysis

In this section, an analysis of the location of cells providing the smallest resistance ratios is conducted. In Fig. 6, a topological representation (i.e., bitmap) of the cells presenting resistance ratios *Ra* included in the first six resistance ranges of Table III is presented. *Ra* changes from ratio interval number 1 ('0< *Ra* <1') in Fig. 6a to ratio interval number 6 ('5< *Ra* <6') in Fig. 6f. For each bitmap, cells with a black color are associated with a resistance ratio out of the selected interval, whereas cells with a variable degree of gray are associated with resistance ratios included in the selected interval. For each cell location, the brightness of a cell reflects the number of cycles falling into the selected ratio interval, white color being associated with the maximal number of occurrences. For instance, in Fig. 6a, the cell at location (6;2) falls twice out of 230 in the interval '0< *Ra* <1' (white color). The cell at location (0;5) falls 2 times in this same interval (light gray), while the cell at location (0;2) falls 1 time in this interval (dark gray).

Fig. 6a and Fig. 6b show that the cell at location (6;2), highlighted in red, falls twice in the interval "0< *Ra* <1" and once in the interval "1< *Ra* <2", with no occurrence in other intervals. Regarding the cell at location (6;5), highlighted in orange in Fig. 6b, it is also included in bitmaps of Fig. 6c-f. The behavior of the above-mentioned cells along with those at locations (1;1) and (6;3) of Fig. 6.c will be further analyzed in the next section. Results from this primary analysis show that no specific topological pattern related to cells suffering from a

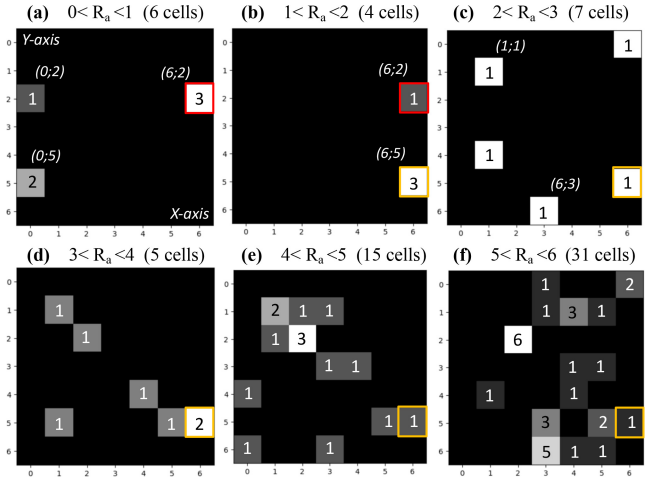


Fig. 6. Topological representation of cells presenting the lowest resistance ratios for the first six lines of Table III. *Ra* range varies from '0< *Ra* <1' (a) to '5< Ra <6' (f). For each bitmap, black color is associated with ratios out of the selected range. The brightness of a cell reflects number of programming cycles falling in the selected ratio range.

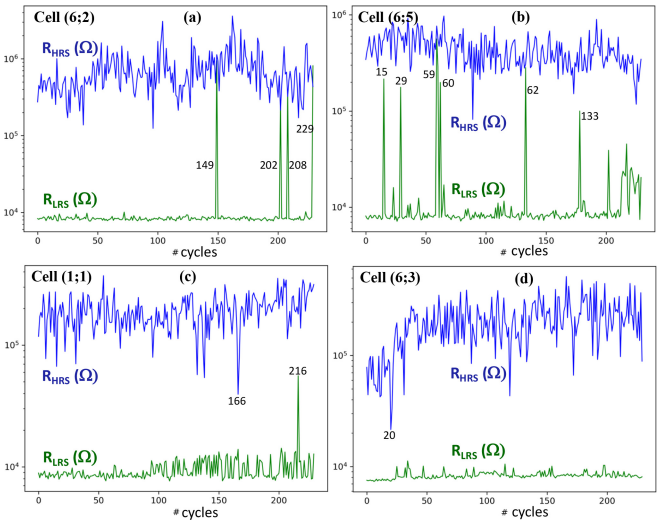


Fig. 7. HRS/LRS resistances in log scale over 230 programming cycles. Cells located at position (a) (6;2), (b) (6;5), (c) (1;1) and (d) (6;3) are analyzed. Cycles with low resistance ratios are pointed out by reporting the programming cycle number.

low resistance ratio can be detected, supporting the hypothesis of an unpredictable behavior of the technology.

C. Cell Tracking Analysis

In this section, a cell tracking analysis is conducted to monitor the evolution of the resistance of cells at locations (6;2), (6;5), (1;1) and (6;3) over 230 programming cycles. Fig. 7a shows the evolution of the HRS/LRS resistances of the cell located at (6;2) in log scale. At cycle 149, the resistance ratio decreases drastically while staying slightly >1. For cycles 202, 208 and 229, HRS and LRS states overlap. However, after these overlaps, the memory cells recover their normal operation with ideal resistance ratios, once again demonstrating the erratic behavior of this technology. In Fig. 7b the evolution of the HRS/LRS resistances of the cell located at position (6;5) is reported. For this cell, many cycles presenting a low resistance ratio are detected. Cycles 15, 59, and 62 have ratios <2, but >1. Cycles 29, 60 and 133 show ratios between 3 and 4. In Fig. 7c, the HRS/LRS resistances of the cell located at position (1;1) are presented. Two marginal ratio values are detected: one at cycle 166 (with a ratio between 2 and 3) and another one at cycle 216 (with a ratio between 3 and 4). Although there is no resistance overlap for these particular cycles, no reference resistance value R_{th}, that allows differentiating the HRS and the LRS can be extracted from the plot. Also, note that cycle 166 is related to an inefficient programming operation resulting in a low HRS while cycle 216 is related to an inefficient programming operation resulting in a high LRS. The same phenomenon is detected for cycle 20 of cell (6;3) in Fig. 7d, where a low HRS state is detected. This analysis shows that, for the four considered cells, no specific temporal pattern is detected, and all the cells subjected to intermittent errors recover their normal operation.

To understand quantitatively intermittent errors, a deep analysis is conducted at the I-V and R-V characteristics level. This analysis is carried out in order to understand the root cause of resistance ratio values far from the ideal ones. Fig. 8a and Fig. 8b present I-V and Log(R)-V electrical characteristics in the SET direction related to the 'defective' cycle 149 of cell (6;2). Defective cycle characteristics are presented in orange. This defective cycle is compared with a 'defect-free' one, related to the same cell and represented in blue. The defective cycle shows close HRS and LRS states, both associated with low current values, suggesting an issue related to the SET operation (i.e., cell stuck at HRS with low current values). Fig. 8c and Fig. 8d present I-V and Log(R)-V curves related to cycle 29 of cell (6;5). We can see that this cycle also suffers from an issue related to the SET operation (low LRS current correlated with a high LRS resistance when compared to a defect-free cycle). If we consider Fig. 8e and Fig. 8f, related to the cycle 20 of cell (1;1), we can see that this cycle has suffered an issue during the RST operation (high HRS current correlated with a low HRS resistance) resulting from an over-SET of the cell during the previous cycle (low initial LRS resistance).

Upon analyzing the measurement data, it becomes clear that some devices exhibit a defective SET process, indicated by the green peaks in Fig. 7. Conversely, other devices display a defective RST process, represented by the blue downward-oriented peaks in Fig. 7.

V. Intermittent Faults Mitigation Techniques

A. Mitigation Circuit for Intermittent Errors During SET

We show that intermittent errors in RRAM cells are strongly correlated with the programming current. Both excessive and insufficient programming currents can result in errors, as highlighted in [32]. To address this issue, Fig. 9 illustrates a schematic of a built-in current comparator integrated with the RRAM cell. The current comparator is specifically designed to continuously monitor the cell current, denoted as I_{cell}, during the SET operation. It ensures reliable operation by terminating

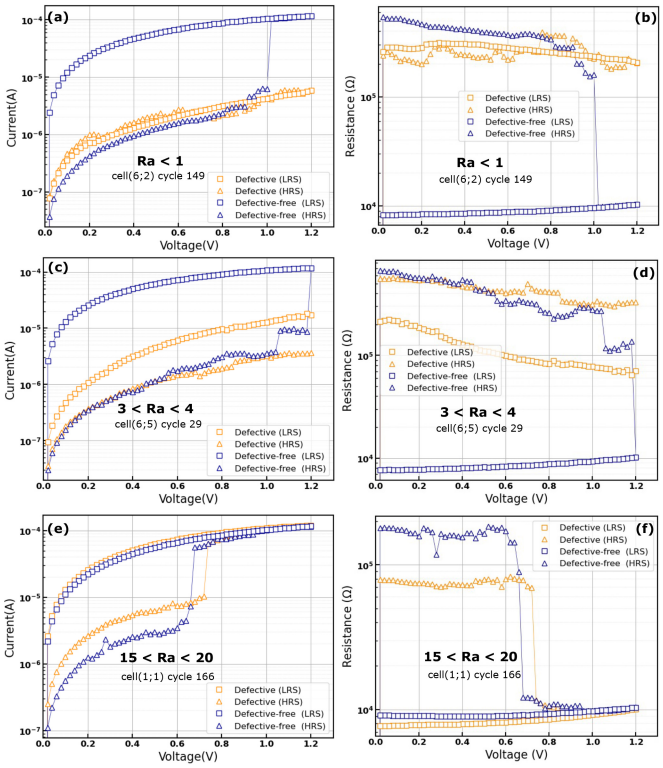


Fig. 8. Comparing defect-free and defective devices based on I-V and Log(R)-V curves for (a) (b) cycles 149 of cell (6;2), (c) (d) 29 of cell (6;5) and (e) (f) cycle 166 of cell (1;1).

the SET process as soon as I_{cell} matches a predefined reference current, I_{refS}. If the reference current is not reached, the SET operation is considered incomplete since the switching event is not detected. The comparator consists of a current differential amplifier (M2, M3) and two current mirrors (M1, M2 and M3, M4). The n-MOS current mirror pair (M1, M2) is used to copy the current of a constant current source I_{refS}. The current mirror (M3, M4) replicates and amplifies the current difference (I_{cell}-I_{refS}) that draws current from node *A*, node *A* being connected to the input of inverter I1. The key component of the circuit is the differential pair (M2, M3) that computes the difference between I_{refS} and I_{cell}. If (I_{cell}-I_{refS}) < 0, then I_{cell} flows through M2 and no current flows through M3. The inverter input *A* is set high and the comparator output *out* is set to low. When I_{cell} just exceeds I_{refS}, a current starts flowing through M3. This current is amplified and the inverter input *A* is grounded. As a result, the comparator output *out*, that will be used to terminate the SET operation, switches from low to a high. Note that a minimum current of 55 μA can be selected for the SET operation, as this is considered a reliable programming current for the technology under consideration [33].

Fig. 10 illustrates the implementation of the proposed SET current comparator at the RRAM memory array level. For clarity, only the current comparison stage of the current sensor is shown, along with four memory cells, with a single cell being addressed. During the SET operation, *WL0* is activated and a SET pulse is applied to *BL0* through the *BL* driver. As current flows through the selected cell, its resistance

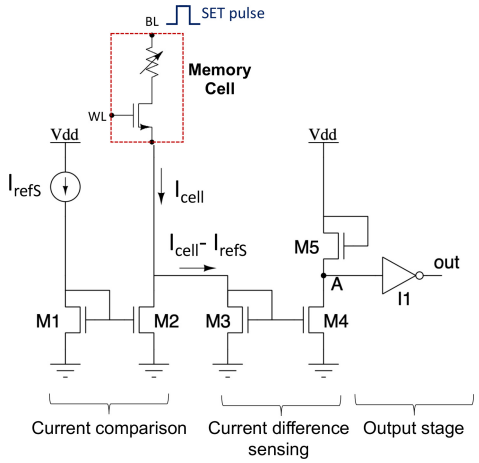


Fig. 9. Built-in current comparator for SET operations.

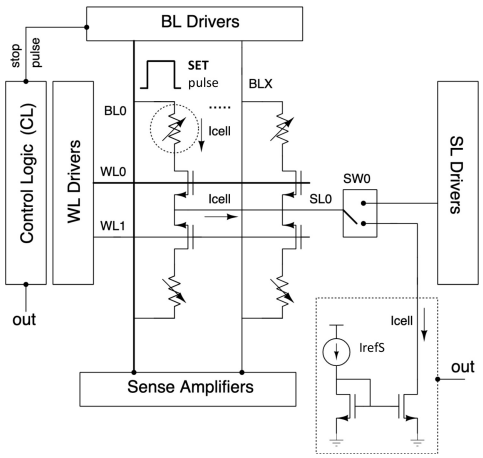


Fig. 10. SET current comparator integration at the memory array level.

decreases, allowing more current to pass as the SET pulse is maintained. When I_{cell} reaches the threshold I_{refFS}, the output signal (*out*), connected to the BL driver control logic, triggers the stop pulse signal, thereby terminating the SET operation. This programming approach enables precise control over the effectiveness of the SET operation through the *out* signal.

B. Mitigation Circuit for Intermittent Errors During RST

Similar to the SET operation, the programming current can be monitored during the RST operation to verify that the operation has been successfully executed. The RST current comparator used for this purpose is depicted in Fig. 11. The cell current I_{cell} is mirrored using an n-MOS current mirror (M1, M2) while the current mirror (M3, M4) is used to duplicate the reference current I_{refR}. In contrast to the SET operation, the RST operation is terminated when I_{cell} decreases down to I_{refR}, ensuring the switching event occurs. If the reference current is not reached, the RST operation is considered incomplete. As the cell current decreases during the RST operation, the current difference (I_{refR} - I_{cell}) is evaluated at node *A*. If (I_{refR} - I_{cell}) < 0, node *A* is set low and the *out* node is set high. If (I_{refR} - I_{cell}) > 0, node *A* is set high and the *out* node is set to low, which terminates the RST operation

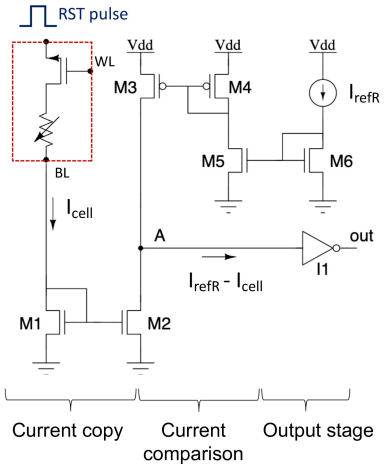


Fig. 11. Built-in current comparator for RST operations.

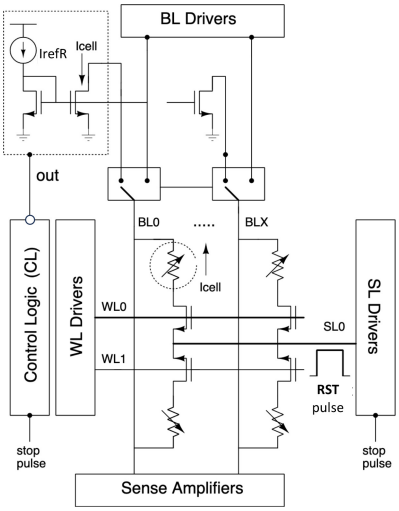


Fig. 12. RST write termination integration at the memory array level.

TABLE IV
REFERENCE CURRENT VALUES DURING RST & SET

	I_{refS}	I_{refR}	R
RST	-	3 µA	400 kΩ
SET	55 µA	-	10 kΩ

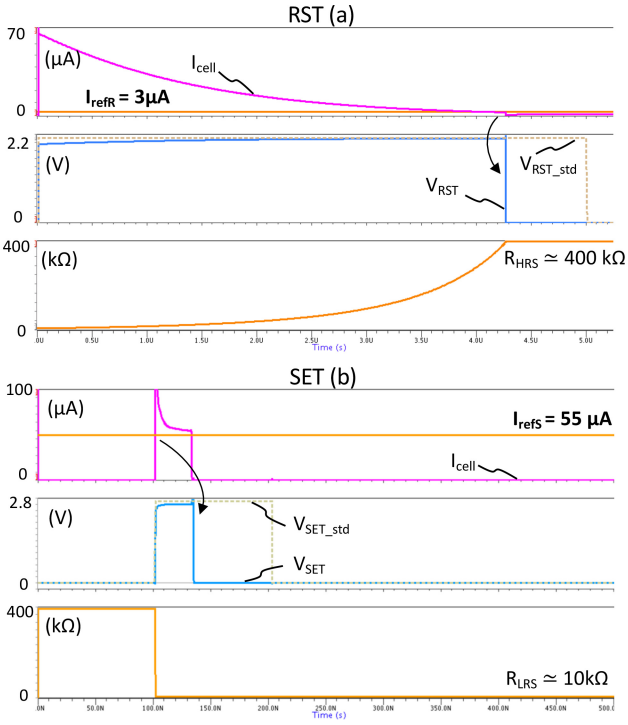


Fig. 13. Transient simulations after a) RST and b) SET operations achieved using the proposed RST and SET intermittent errors mitigation circuits.

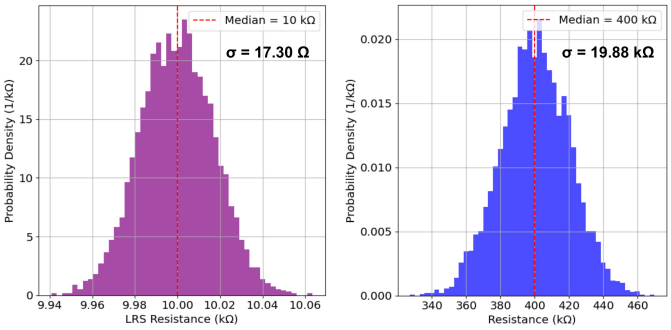
(*out* signal being active at a low level). Typically, I_{refR} is set to a few microamperes to limit the HRS resistance increase to a few hundred kΩ.

Fig. 12 illustrates the implementation of the proposed RST current comparator at the RRAM memory array level, where only the current copy stage of the comparator is shown. The RST operation is carried out by biasing the memory cell with the opposite polarity compared to the SET operation. *WL0* is first activated and a RST pulse is applied to *SL0* through the *SL* driver while *BL0* is connected to the current sensor input. When I_{cell} reaches I_{refR}, the *out* signal terminates the RST pulse through the control logic. Note that during a RST operation, as the current flows, the resistance of the cell increases, causing current to reduce.

C. Simulation Results

We have simulated the SET and RST intermittent errors mitigation circuits presented in Fig. 10 and Fig. 12 within a 1 Mbyte RRAM array (1024 WLs and 1024x8-bits BLs) using a 0.13µm CMOS technology and a RRAM model fully calibrated on silicon [34]. SPICE simulations have been performed using the *Eldo* simulator. Table IV presents typical values set for I_{refS} and I_{refR}, along with the associated RST and SET targeted resistance values. For the RST operation, a threshold of 3 µA is used to reach a 400 kΩ HRS resistance. For the SET operation, a resistance of 10 kΩ is targeted.

Transient simulation results are presented in Fig. 13 after RST and SET operations considering the reference currents presented in Table IV. During the RST operation (Fig. 13a), the cell current I_{cell} gradually decreases down to I_{refR} which is set to 3 µA. Beyond this point, the RST pulse is terminated limiting the HRS resistance value to 400 kΩ. The standard RST pulse V_{RST_std} is also presented and compared to the actual RST pulse V_{RST}. We can see that the standard RST pulse is terminated as soon as the cell current reaches I_{refR}. During SET (Fig. 13b), the cell current I_{cell} is continuously sensed and compared to the reference current I_{refS}. When I_{cell} reaches the reference current value which is set to 55 µA, the SET pulse V_{SET} is terminated. The standard fixed width SET pulse V_{SET_std} is also reported for comparison. We can observe that the I_{cell} current change is abrupt and induces an overshoot leading I_{cell} to exceed I_{refS}. It is also worth noting that the standard 100 ns SET pulse is remarkably short, which is a typical characteristic of RRAM SET operations [20].



(a) (b)

Fig. 14. Transient simulations after a) SET and b) RST operations achieved using RST and SET intermittent error mitigation circuits.

TABLE V
HRS AND LRS DISTRIBUTIONS MAIN PARAMETERS

State	Runs	Std. deviation (KΩ)	Median Value (KΩ)	Min value (KΩ)	Max value (KΩ)
HRS	5000	19.88 kΩ	400	311	464
LRS	5000	17.30 Ω	10	9.94	10.06

D. Variability Analysis

To evaluate the impact of technology-induced variability on the proposed design scheme, a Monte Carlo (MC) analysis is conducted to assess the robustness of the resistance control mechanism. The analysis incorporates realistic process variations since RRAM cell variability is modeled using a silicon-calibrated RRAM model tailored to the target technology [34]. In addition, the variability of the CMOS subsystem, including transistor mismatch, is also considered [35]. CMOS process variation parameters are extracted from STMicroelectronics fabrication corners (Crolles, France). In each MC simulation run, device parameters are randomly generated based on predefined statistical distribution models.

Fig. 14 illustrates the statistical resistance distributions resulting from the MC analysis. Fig. 14a shows the LRS distribution centered around 10 kΩ with a tight spread. The sharp peak and narrow standard deviation ($\sigma = 17.30$ Ω) reflect the accurateness of the SET mitigation circuit. Fig. 14b presents the HRS distribution centered around 400 kΩ with a relative broader spread. The wider dispersion ($\sigma = 19.88$ kΩ) and lower peak density of the HRS curve indicate a more important sensitivity to variability, typical of higher RRAM resistance states. MC simulation results are summarized in Table V.

VI. DISCUSSION

Overall results lead us to consider the RRAM as an analog device whose resistance can change within a large spectrum of values. Because of this, more states can be defined than just the logical '1' and '0'. This concept is shown in Fig. 15, where the gap between '1' and '0' represents an undefined state, denoted as 'U', which is circuit-dependent. 'L' and 'H' denote, respectively, an extremely low resistance state and an extremely high resistance state. Intermittent errors can arise

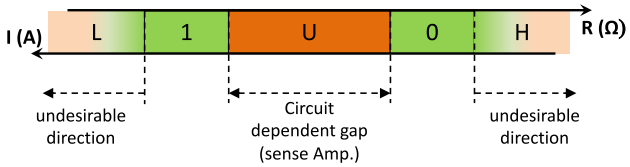


Fig. 15. RRAM analog behavior: resistance and current spectrums.

when HRS and LRS overlap or when the resistance values of HRS and LRS fail to consistently meet their expected ranges ('0' and '1', respectively). In such cases, the memory cell may intermittently fail to distinguish between logical states, leading to errors. In Fig. 15, the 'L' and 'H' states behave as a '1' with extremely high current or a '0' with extremely low current, respectively. However, these two areas are undesirable as they can lead to intermittent errors. Intermittent errors due to resistance states located in the 'L' and 'H' regions can be explained from a physical standpoint. If during a SET operation too many bonds between some of the metal and oxygen ions in the oxide layer break, too many oxygen ions are attracted to the TE, thus leaving oxygen vacancies behind acting as a conductive filament (CF). Therefore, the voltage applied to induce an efficient RST operation might not be high enough. In such cases, triggering the RST may require additional voltage stresses to get those oxygen ions to drift back, which means that the device could remain stuck in the LRS for some cycles. Conversely, if, in one cycle, the RST operation displaces too many ions, the following voltage applied to induce a SET operation may not be high enough, leading to the device being stuck in the HRS.

It has been demonstrated that integrating feedback circuits to monitor the programming current during the SET and RST processes can effectively mitigate intermittent errors and can be extended to address other defects inherent to the technology [36]. The proposed design enables real-time monitoring of post-SET and post-RST resistance values by observing the programming currents. This is accomplished by dynamically terminating the programming operation only once the desired current level is reached, otherwise, the programming operation is considered incomplete.

VII. DISCUSSION

The existence of significant and sudden fluctuations in RRAM resistances has been established experimentally: for particular programming cycles, intermittent resistance drops in isolated cells have been demonstrated after both SET and RST operations. In light of these findings, embedded monitoring circuits have been designed to guarantee reliable RST/SET operation. The effectiveness of SET and RST operations is achieved by dynamically tracking the programming current. The embedded monitors have been specifically designed to verify whether the cell has reached the desired resistance state.

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