

A modular DC/DC converter using SiC switches for railway applications

Design, implementation and evaluation

Delft University of Technology
Faculty of Electrical Engineering, Mathematics and Computer Science
DC Systems, Energy Conversion & Storage group

Master of Science thesis report
Erwin Mostert
January 2017



A modular DC/DC converter using SiC switches for railway applications

Design, implementation and evaluation

by Erwin Mostert (student number: 4177274)

In partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE
in Electrical Engineering

at Delft University of Technology

An electronic version of this thesis is available at <http://repository.tudelft.nl/>

THESIS COMMITTEE:

Dr. ir. H. Polinder

Dr. J. Popovic (supervisor TU Delft)

Dr. ir. M. Popov

W. Platschorre (supervisor Strukton Rolling Stock)

Abstract

Nowadays, most of the trains use some form of electric traction, whether this is full electric traction using overhead lines or diesel-electric traction using an on-board diesel generator to generate the electrical power. The voltages obtained from the overhead lines or generator could not be directly applied to the traction motors, as this voltage is too high or doesn't have the right form. Therefore power converters are needed.

The development of these power converters becomes more and more focussed on obtaining higher efficiency. Converter should be as small and silent as possible. This could only be achieved with wide bandgap switches, like silicon carbide switches, since they have low switching losses and can therefore operate at high frequencies, making the converter smaller and less noisy.

The power converters are usually designed for a specific input voltage and output power. This leads to high development costs, since there are a lot of overhead line voltages in existence and the output power is also always different for every train. To reduce the development costs, these converters should be modular. Then multiple modules can be connected in series and/or parallel to obtain the right input voltage rating and the right output power rating. But this comes at the cost of more complicated control.

During this thesis project, the opportunities for silicon carbide switches are explored. Then the ways of creating a modular converter are described. With this information, a modular converter is designed. This design is simulated and finally the electrical performance of a real module is compared to the simulation results.

Acknowledgements

This thesis was written by one person, but of course this thesis wouldn't be possible without other people.

First of all, I want to thank Strukton Rolling Stock (SRS), and especially Wim Platschorre, René van der Hoek and Rudi Broekhuis for offering me the opportunity to do my thesis project at SRS. At SRS, Kees van Noppen, Jaap Verschoor and of course Wim Platschorre, my supervisor, gave me support when I needed it, so I would like to thank them.

I also would like to thank Jelena Popovic, my supervisor at the TU Delft. Although I did my thesis at SRS, the meetings we had were very useful, since Jelena always gave critical feedback.

And of course I want to thank my family, friends and former colleagues at SRS for having fun during the time I wasn't working on my this project.

Contents

Abstract	i
Acknowledgements	ii
1 Introduction	5
1.1 Background	5
1.2 Research questions	5
1.3 Design objective	6
1.4 Thesis outline	6
2 Concepts for a modular SiC based converter	7
2.1 SiC semiconductor technology	7
2.1.1 Opportunities for SiC devices	7
2.1.2 Comparison between Si PN and SiC Schottky Diodes	8
2.1.3 Comparison between Si and SiC switches	9
2.1.4 Challenges in using SiC switches	12
2.1.5 Discussion	12
2.2 Architectures for modular converters	15
2.2.1 Switch level modularity	16
2.2.2 Converter level modularity	18
2.2.3 Discussion	20
2.3 Isolated topologies for modular converters	21
2.3.1 Forward based topologies	22
2.3.2 Push-pull converter	23
2.3.3 Flyback converter	25
2.3.4 Isolated Ćuk and SEPIC converters	26
2.3.5 Bridge topologies	27
2.3.6 Isolated resonant link converters	30
2.3.7 Discussion	33
3 Design of hardware and control system	34
3.1 Design specifications	34
3.1.1 Specifications for the complete converter	34
3.1.2 Specifications for one module	35
3.2 Hardware	36
3.2.1 Zero voltage switching	36
3.2.2 Transformer design	37
3.2.3 Obtaining the power rating	38
3.2.4 Dimensioning of filter components	39
3.2.5 Input capacitor	40
3.2.6 Gate driving	40
3.2.7 Evaluation by simulation	41

3.2.8	Iteration	42
3.2.9	Practical implementation	43
3.2.10	Hardware overview	45
3.3	Control system	45
3.3.1	Local control system	47
3.3.2	Global control system	51
3.3.3	Overview of full control system	54
4	Design evaluation & performance	57
4.1	Design evaluation of a single module	57
4.1.1	Switch tests	57
4.1.2	Full module without control	63
4.1.3	Full operation with control	65
4.2	Design evaluation of multiple modules	66
4.2.1	Test procedure	66
4.3	Conclusion	66
5	Conclusions & future work	68
5.1	Future work	68
A	Schematics and PCB	70
A.1	Schematics	70
A.2	PCB	79
A.3	Assembled module	80
B	Slope compensation	82
B.1	Origin of subharmonic oscillations	82
B.2	Slope compensation	83
B.2.1	Slope	83
B.2.2	Offset	83
B.3	Conclusion	84
C	Optical fiber	85
C.1	The MOSFET driver setup	85
C.2	Problems	85
C.2.1	dv/dt issues	85
C.2.2	Timing issues	85
C.2.3	Not turning off	87
C.3	Conclusion	87
	Bibliography	88

Chapter 1

Introduction

1.1 Background

Power electronics has changed the world of electrical traction in railways. The first electrical locomotives used DC motors in series with switchable resistors to control the speed. In the 1960's, the NS (Dutch Railways) started to experiment locomotives using thyristors instead of resistors. Later on, gate turn-off thyristors (GTOs) were used. Nowadays, new electrical traction converters are equipped with insulated gate bipolar transistors (IGBTs). But the development of railway traction systems didn't stop here. In the last few years, several SiC devices had become available on the market. These devices are able to switch high voltages and high currents very fast and with low losses. This will increase efficiency and power density.

Strukton Rolling Stock (SRS) is a company that designs (power) electronics for trains. They design motor drives, auxiliary power supplies, control systems, etc. They are using IGBTs as switch in their power converters. During the development of power converters, SRS is facing two major challenges:

1. Train builders want converters that are very small and efficient and the weight should be as low as possible. With the current Si IGBT technology, much power is dissipated as heat. At the same time, the weight should be low, so big heatsinks could not be fit in the design. Sometimes a forced airflow isn't even allowed and the converter should be cooled by the airflow caused by the speed of the train.
2. There exist a lot of power supply voltages for electrical traction. For example, trains in the German speaking countries, Sweden and Norway run on 15kV at 16.7Hz, trains in Belgium and Italy run on 3kV DC, trains in the Netherlands run on 1.5kV and trains in Denmark, France, the UK and on high-speed lines run on 25kV at 50Hz. Trams and metros generally run on 600V DC or 750V DC. These are the most common voltages in Europe, but there are more. Usually, the AC voltages are stepped down in the trains using a transformer, but the DC voltages are directly connected to the power converters. This means that every power supply voltage needs its own converter.

These challenges could be solved by using modular converters based on SiC switches. The SiC switches solve the first challenge, because they have low switching losses compared to Si IGBTs. The second challenge is solved by using some form of modular converter, in which the input voltage is divided over multiple smaller switches with a lower voltage rating.

1.2 Research questions

This thesis project has one main objective: "Design a high-voltage ($\geq 600\text{V}$) high-power ($\geq 1\text{kW}$) modular converter using off-the-shelf SiC semiconductor switches". This objective can be achieved by answering the following questions:

1. The main question related to SiC semiconductors: “What are the differences in using SiC semiconductors compared to using state-of-the-art Si switches?” This question is split up in the following questions:
 - (a) “How do SiC semiconductor switches in general compare to Si switches?”
 - (b) “Which types of SiC switches are commercially available and how do they compare?”
 - (c) “What are the challenges in using SiC semiconductor switches compared to Si switches?”
2. The main question related to modular converters: “What is the optimum form of modularity for achieving input voltage sharing in power converters for railway applications?” This question is split up in the following questions:
 - (a) “What forms of modularity for input voltage sharing exists and how do they compare?”
 - (b) “What is the best topology to use for a modular DC/DC converter?”
 - (c) “What is the best way to control the chosen form of modularity concerning voltage and current sharing?”

1.3 Design objective

The objective of this thesis is to provide a proof of concept for SiC devices and modular converters. The converter should be usable in trains, but doesn’t have to be a traction converter. During the project, it was decided that the converter should be a battery charger with the following specifications:

- Maximum nominal input voltage for the full converter: 3kV DC
- Maximum input voltage for one module: 1kV DC
- Output voltage: 140V DC

Detailed specifications for the converter are described in chapter 3.1.

1.4 Thesis outline

This thesis is organized in three chapters:

- Chapter 2: literature study and concept overview. This chapter gives an overview of relevant concepts for modular converters based on SiC switches.
- Chapter 3: specifications and design procedure. This chapter gives an detailed overview of the converter specifications and the choices that have to be considered during the design process. It also presents a simple control system for the proposed modular converter.
- Chapter 4: evaluation of the design. This chapter presents measurement results and discusses them.

Chapter 2

Concepts for a modular SiC based converter

To build a SiC based modular converter, several technologies and concepts have to be reviewed. First, the available literature on SiC is studied to make a good choice for a SiC switch and to discover all challenges that come with using SiC switches. Second, concepts for modular converters are reviewed and finally a review of converter topologies is presented, so that a suitable topology for a SiC based modular converter can be chosen.

2.1 SiC semiconductor technology

Silicon carbide (SiC) is a semiconductor material that is known for its superior properties for many years. Since the 1970s, researchers are working on the production of semiconductors based on this material. The material itself has properties that are much more attractive to use in semiconductors compared to silicon, but there were problems with producing large uniform crystals without defects. It was not until 2001 that the first commercially available power electronic device made of SiC was produced. The first devices were SiC Schottky diodes, but later also transistors were produced. First JFETs, but later also MOSFETs and even BJTs (called SJTs). The technology is now mature enough to compete with commercially available Si devices, especially in the voltage range between 900V and 1700V. At the moment of writing this thesis, researchers are still improving the quality of the SiC wafers and working on devices that are able to switch even higher voltages[37].

2.1.1 Opportunities for SiC devices

Commercially available SiC devices are usually made of 4H-SiC. 4H indicates the crystalline structure. The properties of this material are compared to the properties of silicon in table 2.1[40, 14]. This table shows that the breakdown strength of SiC is 10 times the breakdown strength of Si. This means that the epitaxial layer in power devices, whose purpose is to lower the electric field, can be 10 times thinner. Because this layer has a big contribution to the on-state resistance of power devices, the on-state resistance is significantly smaller for a SiC compared to a Si device with the same voltage rating. This effect is opposed by the fact that the electron and hole mobilities of SiC are lower compared to Si.

Both effects have a linear effect on the on-state resistance. This is shown in equation in equation (2.1), the relation between electron current density and applied voltage of the drift region[34]. In this equation, J_n is the electron current density, q is the charge of an electron, μ_n is the electron mobility, N_d the doping density, V_d the voltage drop across the drift region and W_d the thickness of the drift region. With this equation, the resistance of the epitaxial could be approximated. Since the resistance of this layer dominates the on-state resistance, the non-linear voltage drop in the

junction (for diodes and BJTs) or channel (field effect transistors) is neglected. This results in the approximation that the on-state resistance of a SiC device will be $\frac{30\text{kV/mm}}{300\text{kV/mm}} \cdot \frac{1400\text{cm}^2/(\text{V s})}{900\text{cm}^2/(\text{V s})} \approx 16\%$ of the on-state resistance of a Si device with the same voltage rating.

$$J_n \approx \frac{q\mu_n N_d V_d}{W_d} \quad (2.1)$$

Another property of SiC is that the band gap of SiC is almost 3 times the bandgap of Si. This wider band gap means that the temperature SiC devices can withstand is higher. Together with the higher thermal conductivity, this means that the power dissipated in a SiC device can be larger without causing thermal problems. Together with the lower on-state resistance, this results in a device with a much higher current rating compared to a device of the size and voltage rating made of Si.

Property	Si	SiC	GaN
Band gap [eV]	1.12	3.26	3.4
Electron mobility [$\text{cm}^2/(\text{V s})$]	1400	900	2000
Hole mobility [$\text{cm}^2/(\text{V s})$]	600	100	-
Breakdown field [kV/mm]	30	300	350
Thermal conductivity [$\text{W}/(\text{K cm})$]	1.5	4.9	1.3
Relative dielectric constant	11.8	9.7	-

Table 2.1: Physical properties of silicon and silicon carbide

Comparison between SiC and GaN

Another semiconductor material that is very promising is gallium nitride (GaN). Both semiconductor materials belong to the family of wide bandgap (WBG) semiconductors. Compared to SiC, all electrical relevant properties, except the thermal conductivity, of GaN are better (see table 2.1). But there are practical limitations in using GaN. The production of GaN is not mature enough to produce high voltage and high power GaN transistors. There are GaN devices with a blocking capability of 600V, but their current rating is not more than 17A with $R_{on} \approx 0.3\Omega$ [50]. Other GaN devices have voltage rating less than 200V or their current rating is lower than 10A and their R_{on} is relatively high[36]. This means the currently available GaN devices are not suitable for high-power applications. This is confirmed by multiple sources[14, 31] (and even by GaN transistor manufacturers[1]). There is also no literature that compares commercially available GaN switches with SiC switches. For these reasons, GaN devices are considered as not suitable for the desired application and not covered in the rest of this thesis.

2.1.2 Comparison between Si PN and SiC Schottky Diodes

SiC diodes are more mature than SiC transistors, are longer on the market and therefore more often used. The advantage of SiC diodes over Si diodes is that SiC diodes can be made with a Schottky junction instead of a PN junction and still block a high voltage[40]. Si Schottky diodes have a reverse voltage rating of a few 100V, while SiC Schottky Barrier Diodes (SBD) are available with reverse voltage ratings up to 1700V and current ratings of a few 10A. GeneSiC even provides diodes with a reverse voltage rating of 15kV, but with a current rating of 1A.

The great advantage of SiC SBDs over Si PN diodes is the fact that SBDs are majority carrier devices, while Si PN diodes are minority carrier devices. Minority carrier devices need some time to build up internal charge to increase the conductivity (conductivity modulation) at turn-on and to remove the internal charge during turn-off (reverse recovery or recombination). The conductivity modulation causes an increased forward voltage drop during turn-on, and the reverse recovery results in a current that causes losses in other components during turn-off. Since SBDs are

majority carrier devices, they don't suffer from conductivity modulation and reverse recovery. This means that the additional current flowing during turn-on and the reverse current flowing turn-off is to discharge respectively charge the junction capacitance. This current is usually smaller than the reverse recovery current of a comparable Si diode, so the associated losses are also smaller.

2.1.3 Comparison between Si and SiC switches

In the previous sections it was shown that, only based on the reasoning with the raw material properties, the on-state performance of SiC devices will be better than the performance of Si devices of the same type. But this rough comparison is not enough to state that actual SiC devices have a better overall performance than Si devices.

Because the thickness of the epitaxial layer increases with increasing blocking voltage, the blocking voltage levels of Si MOSFETs are generally limited to a few hundred volts. MOSFETs with higher blocking voltages have a high on-state losses. This is the reason why IGBTs are developed[2]. These devices are able to block more voltage with low on-state losses at the price of being a minority carrier device. This means that switching is slower and therefore more switching losses occur. This is the main reason why there is a lot of interest for SiC field effect transistors, which are able to block the same voltage levels as Si IGBTs, but have the low switching losses of majority carrier devices.

At the moment, there are a few types of SiC transistors available. These types are:

- JFETs: Junction Field-Effect Transistors, manufactured by USCi and Infineon
- MOSFETs: Metal-Oxide-Semiconductor Field-Effect Transistors, manufactured by Wofspeed (a daughter company of Cree), ROHM, STMicroelectronics and Microsemi
- SJTs: Silicon carbide Junction Transistors, in fact BJTs made of SiC, manufactured by GeneSiC
- Thyristors, manufactured by GeneSiC

Most SiC switches have a voltage rating of 1200V with current ratings up to 300A. There are also devices available which block 1700V. The thyristors are able to block 6500V and have a current rating up to 80A.

Manufacturers of SiC devices provide a lot of information on their devices and also compare them to Si devices. They claim their devices are better than Si devices. To verify this, independent researchers started to make their own comparison of both kinds of devices. Because MOSFETs are very common in power electronics, a lot of research was focused on the comparison between SiC MOSFETs and Si IGBTs. But there is also research done on other SiC switches.

Most of the time, the focus of the research is on a few figures. These figures are on-state resistance or forward voltage drop, turn-on losses and turn-off losses. Driving losses are usually not described, because they are very small compared to the switching losses and straightforward to calculate.

SiC MOSFETs

Because of their good properties, MOSFETs are most used devices in low voltage power electronics. MOSFETs are majority carrier devices, so they don't suffer from conduction modulation and reverse recovery. They are normally-off and the state of the switch is easily controlled by charging the gate. The on-state resistance and switching losses are relatively low. This is probably one of the reasons most of the semiconductor manufacturers focus on developing SiC MOSFETs.

To compare SiC MOSFETs with comparable Si IGBTs, several measurements are done on the switching losses of both Si IGBTs and SiC MOSFETs, which show that switching losses for SiC MOSFETs can be 4.7 times smaller than the switching losses of a Si IGBT. Also the switching losses in SiC MOSFETs are less dependent on the switched current than the losses in IGBTs[53].

It is shown that the forward voltage drop for the tested IGBTs is higher than the voltage drop over the tested SiC MOSFETs when the current is lower than about 220A (with $T_j = 20^\circ\text{C}$)[39]. After this crossing point, the voltage drop over the IGBTs is lower. This is because I_E (in IGBTs) is an exponential function of V_{CE} , while I_D (in MOSFETs) increases almost linearly with V_{DS} . The current value at which the voltage drops cross is of course dependent on the ratings of the device: a device with a lower current rating has in general a higher on-state resistance, which shifts the crossing point to a lower value. At increasing junction temperatures, the crossing point moves to lower current levels. This effect opposes the lower switching losses of the MOSFET.

Most papers show that it is possible to increase the switching frequency and decrease the size of the passive components by using SiC MOSFETs, with only a small decrease in total efficiency, thus increasing the power density. For example, Anthon[4] showed that the switching frequency could be increased from 20kHz to 100kHz with an efficiency drop from 98.8% to 98.3% and a decrease in the inductor size of 75%. A remark that has to be made is that the switch current was well below the crossing point described previously, so no conclusions can be drawn on the performance of the SiC MOSFETs compared to Si IGBTs at higher switch currents.

Driving In some situations, there is a possibility that the MOSFET will (partially) turn on. This could happen during fast switching of a high voltage level. This causes a high $\frac{dv}{dt}$. This in turn causes a current to flow through the parasitic capacitances of the MOSFET. The capacitances that cause (partial) turn on are the gate-source capacitance (C_{GS}) and the gate-drain capacitance (C_{GD}). When in a phase leg the upper MOSFET turns on, a current will flow through C_{GD} of the lower MOSFET to the gate. This current partially flows through C_{GS} and through the gate resistor R_G . This causes a voltage drop $V_{GS} \approx R_G C_{GD} \frac{dv}{dt}$, which could be high enough to (partially) turn the MOSFET on. This effect is called false turn-on[21, 26] and can degrade converter efficiency. The current flow during false turn on is illustrated in figure 2.1. The fact that the threshold voltage for a MOSFET has a negative temperature coefficient[15] will increase false turn-on at higher temperatures. False turn-on can be avoided by using a small value for R_G [22] or by avoiding resistive gate driving at all and using resonant gate driving[32].

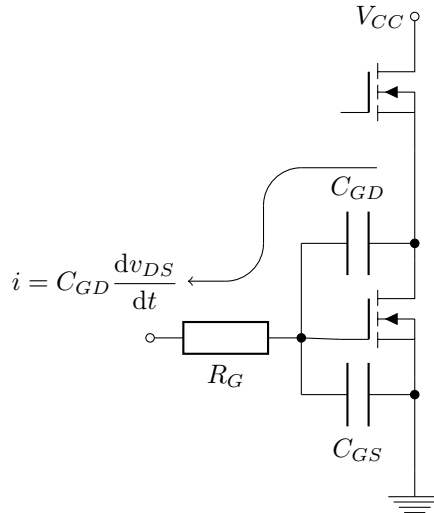


Figure 2.1: Illustration of $C_{GD}dv/dt$ induced false turn-on

Antiparallel diode IGBT modules usually contain a antiparallel diode to enable the use of the IGBT in bridge converters and inverters. MOSFETs have an intrinsic antiparallel diode, which is part of its semiconductor structure. This intrinsic diode is therefore called “body diode”. Body

diodes are usually not high quality diodes, as the semiconductor structure is optimized for the MOSFET and not for the diode. This can be overcome by placing a SiC Schottky diode antiparallel to the MOSFET. The current then flows mainly through the Schottky diode due to two reasons: the lower forward voltage (V_f) of Schottky diodes and their negative temperature coefficient. The lower V_f means that the linearized resistance (r_d) of the Schottky diode is lower than the r_d of the body diode. And even if their threshold voltages are close together, the negative temperature coefficient of the Schottky diode causes r_d to decrease, while the positive temperature coefficient of PN diodes, and thus the body diode, causes their r_d to increase. Due to this feedback loop, most current will flow through the Schottky diode.

SiC JFETs

The first available SiC transistor was a JFET. The switching performance of JFETs is approximately equal to MOSFETs[4]. However, JFETs have a big disadvantage compared to MOSFETs, that is JFETs are normally-on devices: without gate voltage, JFETs are conducting. V_{GS} has to be pulled to a negative value to turn a JFET off. This has two implications:

- To drive JFETs, a negative drive voltage should be generated from a positive voltage source.
- When the control of a driver or the driver itself fails, the JFET is turned on and dangerous situations, like short circuits, can arise.

The first problem is solved by using gate drivers with galvanic isolation. The second problem is solved in two ways: the creation of normally-off JFET and the use of a cascode configuration. The only company that produced normally-off JFETs, SemiSouth, has been closed, so the only remaining option is to cascode SiC JFET with a low voltage Si MOSFET. The basic schematic of such a cascode configuration is shown in figure 2.2. In this configuration, the JFET is always on and the MOSFET is used to switch the current. Because the JFET is able to block the high voltage, the MOSFET doesn't need to have a high V_{DS} withstand voltage. USCi even offers this configuration in a single device[52]. This configuration offers the advantage of driving the JFET in the same way as a MOSFET.

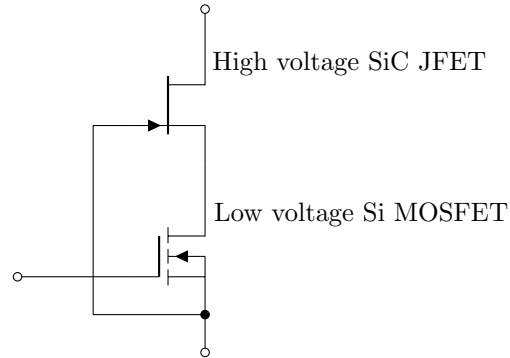


Figure 2.2: SiC JFET and Si MOSFET in a cascode configuration

Like MOSFETs, JFETs are voltage driven devices. But in general, the voltage required to turn off a JFET is bigger in magnitude than the voltage needed to turn on a MOSFET, so they are less sensitive to noise. This advantage of JFETs disappears when the cascode configuration is used.

There are studies which compare SiC JFETs and SiC JFETs in cascode configuration to each other. Intuitively, it can be said that the performance of a single JFET is better than the performance of a cascode configuration, because a cascode has two transistors in series. This means that the on-state resistance will be higher and probably the switching losses will also be higher. The first point is easy to understand, but the second point isn't true. The turn-on energy

for a cascode is higher than for a single JFET, but the turn-off energy is slightly lower[3]. The sum of both energies is indeed higher for a cascode than for a JFET, making the cascode configuration less efficient in a hard-switching converter, but it is a better choice in a converter with a soft turn-on due to ZVS or ZCS.

SiC Junction Transistors (SJTs)

SJTs are in fact bipolar junction transistors made of SiC. The only producer of these devices is GeneSiC. This could lead to a lower availability, which is a small disadvantage of the SJT. SJTs are, like IGBTs, minority carrier devices. This means that they have a lower specific on-state resistance compared to JFETs and MOSFETs[15]. As far as measured, their switching losses are a bit lower or comparable to the switching losses of MOSFETs and JFETs.

Driving The threshold voltage of SJTs is higher than the threshold voltage of a MOSFET and also less temperature dependent. And because of the fact that SJTs are in fact BJTs, they require a current to turn on and to stay on. A MOSFET only needs a small amount of charge to turn on, while a SJT needs a constant amount of power to stay on. This means that a SJT is less sensitive to noise, even at higher temperatures. The drawback of this is that drivers that are able to supply the gate currents needed to achieve a low on-state resistance at high temperatures are not very common.

2.1.4 Challenges in using SiC switches

There are several challenges in using SiC switches compared to Si IGBTs. SiC switches switch faster than Si IGBTs of the same ratings. For example, the Cree CAS300M17BM2[11] SiC MOSFET switches approximately 2 times faster than the SEMIKRON SEMiX353GB176HDs[12] Si IGBT. As this thesis is also about modular converters, it is likely that smaller switches will be used. Smaller switches, like the Cree C2M0080120D[9] SiC MOSFET, switch more than 10 times faster compared to the bigger Si IGBT. This makes high switching frequencies possible, but are also the cause of high $\frac{dv}{dt}$ and $\frac{di}{dt}$, which in turn cause EMI.

Problems due to high $\frac{dv}{dt}$ can always be traced back to parasitic capacitances, because these are the components that let current flow proportional to the $\frac{dv}{dt}$, as shown in the equation of a capacitor. These parasitic capacitances can be found on multiple places in the circuit. The capacitances between traces on a PCB is relatively low, but the capacitance between the windings of a transformer can be relatively high, which causes current to flow from the primary side directly to the secondary side. Another effect associated with high $\frac{dv}{dt}$ is called false turn-on and is described in section 2.1.3.

Another consequence of fast switching are high values for $\frac{di}{dt}$. High $\frac{di}{dt}$ will cause voltage drops across parasitic inductances. These inductances can be found in wires, PCB traces, component leads and within transformers. They affect the switching behaviour in a negative way by limiting the $\frac{di}{dt}$ and thus increasing switching times and losses. They also cause EMI when the current loops are not kept small. This EMI is caused by the fast-changing magnetic field within these loop inductances.

The results of these effects on the operation of the converter could be reduced by proper design of a converter based on SiC switches.

2.1.5 Discussion

In this section, the properties of the SiC switches discussed previously are discussed and a comparison is made between these switches to choose the most suitable switch.

The properties of the discussed types are summarised in table 2.2. This table gives a superficial overview of the switches. Based on this overview, the JFET is unfavorable because of its normally-on state. Therefore, in the more in-depth discussion, the JFET is left out.

Switch types	Normal state	Driving	Threshold
MOSFET	Off	Charge	Low
JFET	On	Reverse voltage	High
Cascode JFET	Off	Charge	Low
SJT	Off	Forward voltage & current	High

Table 2.2: Summary of properties of SiC switches

Losses

The most important benchmark for semiconductor switches are the total losses. Switches with low losses have a positive effect on the efficiency of a power converter. However, switching losses differ significantly from device to device, even within a class of switches. So it is hard to say that, for example, a SJT has less losses than a cascode JFET. This means that it is difficult to compare the types of switches on this property. Therefore a comparison is made between actual devices of different types.

Datasheets of all switches specify turn-on and turn-off losses. But most of the time, the measurement conditions differ a bit from each other. This means that these values could not always be compared. Therefore, some researchers did comparative studies on the switching losses. DiMarino compared multiple switches on their threshold and switching losses[15]. Based on his comparison, the Cree MOSFET has the lowest total switching losses and lowest turn-on losses. The SJT has the lowest turn-off losses. It should be noticed that the continuous current rating of the SJT (6A) and JFET (26A) were much lower than the current rating of the MOSFETs ($\geq 30A$). Because of this shortcoming, the switching losses stated in the datasheets are compared, as far as possible.

In this comparison, the switching losses for a number of SiC switches are taken from their datasheets. The switches are chosen based on their voltage and current rating. Their voltage rating is 1200V, while their continuous current rating at a junction temperature of $T_j = 100^\circ\text{C}$ is $I_d \approx 20A$. The selected devices and their relevant properties are shown in table 2.3. In this table, I_D is the continuous drain current rating of the switch, $R_{th,JC}$ is the thermal resistance between the junction of the switch and the case and $R_{DS(on)}$ is the on-state resistance of the switch.

Model	Type	I_D (DC, $T_j = 100^\circ\text{C}$)	$R_{th,JC}$	$R_{DS(on)}$ ($T_j = 100^\circ\text{C}$)
GA10JT12-247[17]	SJT	20A	0.88K/W	$\sim 125\text{m}\Omega$
C2M0080120D[9]	MOSFET	24A	0.6K/W	104m Ω
SCT2160KE[41]	MOSFET	16A	0.7K/W	$\sim 220\text{m}\Omega$
SCT20N120[46]	MOSFET	16A	1K/W	195m Ω
APT25SM120B[33]	MOSFET	17A	0.55K/W	168m Ω
UJC1206K[52]	Cascode JFET	22.5A	0.65K/W	71m Ω

Table 2.3: Properties of compared devices

Discussion on conduction losses Based on the information in table 2.3, the UJC1206K is the best switch, because it has the lowest on-state resistance and the one of the lowest thermal resistances. The second best is the C2M0080120D, because of its second best on-state resistance and a lower thermal resistance than the UJC1206K.

Discussion on switching losses The switching losses of these devices are compared based on the values stated in the datasheets. Except for the SCT2160KE, the conditions for all measurements were $V_{DS} = 800\text{V}$, $I_D = 10\text{A}$ and $T_j = 25^\circ\text{C}$. For the SCT2160KE, the test voltage was 600V , the other conditions were the same as for the rest. The switched load has an inductive character. The inductance is not always stated. The driving conditions also vary with each device. The results are shown in table 2.4. In this table, E_{on} is the turn-on switching loss, E_{off} is the turn-off switching loss, $E_{SW} = E_{on} + E_{off}$, R_G the gate resistance during turn-on and turn-off, $R_{G(on)}$ the gate resistance during turn-on, $R_{G(off)}$ the gate resistance during turn-off, L the inductance used in the test and V_{DS} the drain-source voltage used in the test.

Model	E_{on}	E_{off}	E_{SW}	Special conditions
GA10JT12-247	140 μJ	6 μJ	146 μJ	Driving conditions unknown
C2M0080120D	100 μJ	75 μJ	175 μJ	$R_G = 2.5\Omega$, $L = 142\mu\text{H}$
SCT2160KE	200 μJ	80 μJ	280 μJ	$R_G = 0\Omega$, $L = 500\mu\text{H}$, $V_{DS} = 600\text{V}$
SCT20N120	160 μJ	90 μJ	250 μJ	$R_G = 6.8\Omega$
APT25SM120B	225 μJ	55 μJ	280 μJ	$R_G = 2.5\Omega$, $L = 115\mu\text{H}$
UJC1206K	200 μJ	$\sim 50\mu\text{J}$	250 μJ	$R_{G(on)} = 2.1\Omega$, $R_{G(off)} = 20\Omega$

Table 2.4: Switching loss of devices

As stated before, the measurement conditions differ for each switch. This does not make a comparison impossible. The total switching losses for the SCT2160KE are higher than or equal to all other switches, even without a gate resistor and with a lower V_{DS} . The turn-on losses of the UJC1206K are already higher than the total switching losses of the GA10JT12-247 and the C2M0080120D, although the turn-on gate resistor is approximately equal of that used to test the C2M0080120D. Due to these facts, the UJC1206K and the SCT2160KE are less preferable than the other devices. The GA10JT12-247 and the C2M0080120D are the better ones based on their switching characteristics.

The placement of the SCT20N120 in this list is harder, the used R_G is higher than the one used for the C2M0080120D and the switching losses are also higher. The dependence of the switching losses on R_G is not shown in the datasheet. The only measurements that can be compared are the switching times. They are measured at $R_G = 0\Omega$, $V_{DS} = 800\text{V}$ and $I_D = 10\text{A}$. These values are only slightly smaller than those of the C2M0080120D with in an equal test setup, except for $R_G = 2.5\Omega$. Therefore it is expected that the SCT20N120 will perform worse than the C2M0080120D, because higher switching times usually mean higher switching losses. With all these observations in mind, the switch with the lowest switching losses at $R_G \approx 2.5\Omega$ will probably be the GA10JT12-247, followed by the C2M0080120D.

Ratio between conduction losses and switching losses The total losses of a switch are calculated with equation (2.2), in which P_{loss} the overall losses, $P_{conduction}$ the conduction losses, $P_{switching}$ the switching losses, d the duty cycle and f_{SW} the switching frequency. With $I_D = 10\text{A}$ and $d = 0.5$, the total losses for the GA10JT12-247, the C2M0080120D and the UJC1206K are calculated and shown in figure 2.3. From this figure it is clear that with $f_{SW} > 25\text{kHz}$, the SJT has the lowest overall losses, followed by the MOSFET. The cascode JFET ends up with the highest losses.

$$P_{loss} = P_{conduction} + P_{switching} = I_D^2 R_{DS(on)} d + E_{SW} f_{SW} \quad (2.2)$$

The decision has to be made between the GA10JT12-247 and the C2M0080120D. The losses of the GA10JT12-247 are somewhat lower than those of the C2M0080120D, but the thermal resistance is higher. At $f_{SW} = 200\text{kHz}$, the difference in temperature will be 6.5°C in favor of the C2M0080120D. Also, the driving of the C2M0080120D will be much easier, because of the fact that it is a MOSFET, which is a very common switch type for power converters. This makes

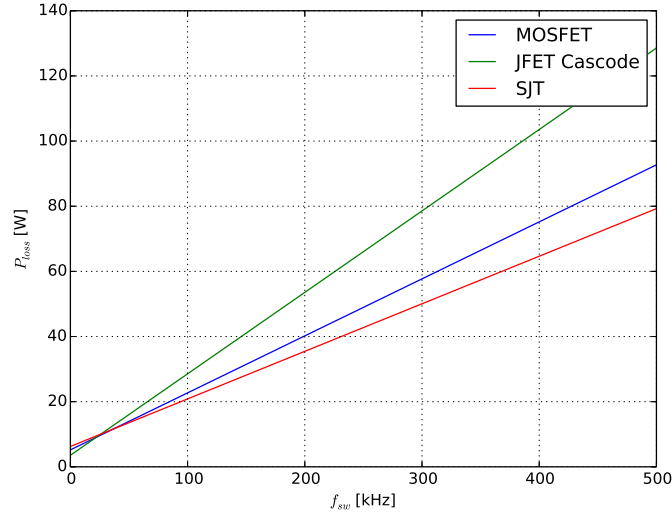


Figure 2.3: Overall losses of different switches

the C2M0080120D the best compromise between usability (driving, cooling) and efficiency (low losses).

2.2 Architectures for modular converters

As described in chapter 1, different countries use different power supply voltages for electrical traction. And even within countries the voltage could be different, depending on the application or location. For every power supply voltage, a new converter had to be designed. To overcome this problem, it is suggested to use a modular converter, in which the input voltage and the output power could be shared across multiple switches.

Besides voltage sharing over multiple switches, modularity can add some other advantages to power converters. Depending on the implementation, these advantages are:

1. Single design for multiple voltage and current ratings
2. Increased availability due to multiple modules and easy replacement of a broken module (when used in $N + 1$ setup)
3. Improved thermal design due to the spreading of losses over multiple components
4. Use of components with lower voltage and/or current rating, which could reduce component cost and increase efficiency
5. Instead of mounting bigger components in an enclosure by hand, the module could be fit on a PCB, which could be assembled automatically, reducing production time and cost

Although modularity can bring some advantages, they don't come for free. The price of these advantages is additional control. This control is needed to compensate for unequal voltage and/or current sharing of the modules. When the voltage sharing between modules is not equal, some modules will bear a higher voltage than others. This voltage could be higher than the rated voltage and the module will fail earlier than expected or it will fail immediately. This will cause additional voltage on the other modules, which will also fail. Failure in devices connected in series could also be caused by heating due to leakage currents. When the current sharing between modules is not equal, some modules heat up more than other modules, which will lead to increased degradation.

When finally one module fails, the other modules have to supply the additional current and will also fail. This shows that when the control of the voltage and current sharing is not done properly, a modular converter will be doomed to fail. Failure caused by these thermal effects is called a thermal runaway. An example of a measured runaway is shown by He[19].

A lot of research is done on modularity in the broadest sense. Modularity appears on multiple levels and can have multiple meanings. But most forms of modularity are not suitable for the purpose described above. All forms of modularity related to voltage sharing in DC/DC converters found in literature could be placed in one of two categories:

1. Switch level modularity
2. Converter level modularity

Both suitable categories are described in the following sections.

2.2.1 Switch level modularity

Switch level modularity is the implementation of a single switch with multiple devices, which could be connected in series, parallel or both, depending on the voltage and current levels. This is done to achieve an equivalent switch which is able to switch very high voltages or currents. This principle is shown in figure 2.4. Examples of this principle can be found in high current rectifiers for smelting furnaces, where multiple diodes are placed in parallel to conduct the high currents. Also inside IGBT or SiC MOSFET modules, multiple dies with a relatively low current rating are placed in parallel to obtain modules with a higher current rating[22]. Many HVDC converters place multiple semiconductor switches in series to switch the high voltages.

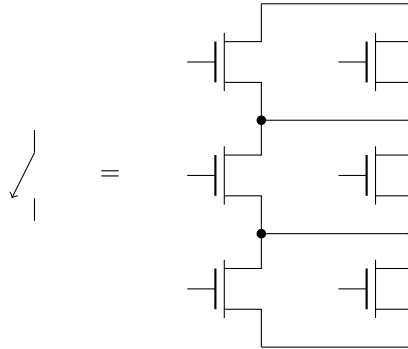


Figure 2.4: Principle of a modular switch

Voltage and current sharing

With this kind of modular converters, there are two classes of solving the voltage and current sharing problems. These classes are passive sharing and active sharing. Passive sharing methods put extra passive components in the circuit to balance the voltage or the current, but the driving of the switches is equal. Active sharing is mainly accomplished by adjusting the driving signals to the switches.

Passive voltage sharing Passive voltage sharing makes use of resistors placed in parallel to the switching devices. These resistors are dimensioned in such a way that the currents in these resistors dominate the leakage currents in the switches[54]. This is called static voltage sharing. Voltage sharing during transients (dynamic voltage sharing) requires an additional RC snubber. Incorporating resistors in a circuit inherently means increasing losses. Although this method of voltage sharing may function well and is very simple to implement, it adds losses to the converter. Adding losses to a converter by placing resistors should be avoided as much as possible.

Passive current sharing Passive current sharing can be done in 3 ways. These methods are:

1. The switches could be mounted to the same heatsink, so that their junction temperature is approximately equal. This means that the current flowing through them is also approximately equal and thermal runaway is avoided. Devices with an positive temperature coefficient for the on-state voltage drop don't even need to be thermally coupled, because when one device is carrying more current, it will heat up more and the voltage drop, and thus the (equivalent) resistance, increases. This will increase the current flow in the cooler device, ensuring approximately equal current sharing.
2. Resistors could be connected in series with the switches. These resistors have to dominate the internal resistances of the switches. In this way, the current sharing is determined by the resistors. This will cause the converter efficiency to drop, because of the additional conduction losses. The use of series resistors will also affect the operation of the converter due to the increased voltage drop across the equivalent switch, which makes it a less ideal switch.
3. Mutually coupled inductors could be connected in series with the switches[54]. Because of the coupling, the currents in all coupled inductors are forced to be equal. Unequal currents are eliminated by voltage drops caused by the mutual inductance. Although theoretically this method does not add losses to the circuit, the resistance of the wires of the inductors and the varying magnetic flux in the magnetic core used to couple the inductors will cause additional losses. Care has to be taken to avoid saturation because of the DC current flowing through the coils. These coupled inductors are also relatively big and cause additional parasitic inductances in the circuit (due to wiring, leakage inductances and magnetizing inductances). These parasitic inductances cause additional switching losses, because the rise and fall times of the current will increase.

Active voltage sharing There are some methods of controlling the voltage across the switch in an active way. Although many authors claim their method is very efficient, at the end they still use some form of passive voltage sharing[30, 8, 28, 8], while other methods regulate the gate voltage, which cause the switch to operate in its active region[24], increase switching losses by slowing the switching process down or affecting the switching process in another way[8, 19]. It can be concluded that every form of active voltage sharing adds losses to the converter and should therefore be avoided.

Active current sharing Active current balancing also relies on adjusting the switching trajectory. For example, Bortis[6] adjusted the switching delays and the slope of the collector current to obtain current balance. Switching with a lower slope means higher switching losses. Lobsiger[29] only used delays in the switching pulse, which results in a fair static current sharing, and during transients the currents are almost equally shared between the switches. One drawback is that the static current sharing is not perfect: after 6µs on-time, the currents slowly start drifting away from each other. This means that there is no real static current sharing. However, this should not be a drawback in converters with high switching frequencies and with positive temperature coefficients, like MOSFETs.

Requirements for the control system

The main principle behind switch level modularity is replacing one switch with multiple switches that behave as one switch. This means that, compared to a non-modular converter, the main control system that controls the switches doesn't have to change. But when active voltage or current sharing will be chosen, an additional control unit has to be designed which translates the signal for the equivalent switch to the real switches. The requirements for this additional control unit depends on the chosen form of voltage or current sharing.

Comparison with a non-modular converter

With this form of modularity, the filter and main control of the converter could be the same as a non-modular converter with the same voltage and power ratings. But when the power level changes, the full converter should be redesigned. An additional control unit is needed to translate the signal from the main control to the signals to the switches. With active voltage or current sharing, this control unit also controls the equal sharing of these quantities. This control unit has to include driver circuits for all switches and can become relatively complex with active voltage and/or current sharing, both in number of components and in software. To achieve voltage or current sharing, additional power dissipation in the form of resistive voltage/current sharing or non-ideal switching is necessary.

When the switches are connected both in series and parallel and there are more switches than necessary ($N + 1$ configuration), broken switches could be replaced without shutting down the converter, which increases availability.

Due to the fact that smaller components have a relatively big surface, thermal management for multiple small components is easier than thermal management for one big component. Depending on the configuration, the increase in effective cooling surface will be bigger or smaller. Mounting multiple switches on the same heatsink can introduce thermal coupling, which affects the increase in effective cooling surface negatively. This is because multiple switches are using the same part of a heatsink to dissipate their losses[42].

Using multiple smaller switches causes the total length of the connections (leads and traces) between the switches to increase, which increases the parasitic capacitance and inductance. This makes this form of modularity not well suited for fast switching converters with high $\frac{dv}{dt}$ and $\frac{di}{dt}$.

2.2.2 Converter level modularity

With converter level modularity, the converter is composed of multiple smaller full converters, which are connected in series or parallel to create the requested output voltage and power from the specified input voltage. The connection of the modules depends on the requirements for the converter. The way of connecting the modules is denoted as “IxOx”, in which the “I” stands for input, the “O” stands for output and the “x” can be replaced with an “S” for series or a “P” for parallel. An overview of which architecture to use is shown in table 2.5. The architecture for a ISOP (Input Series Output Parallel) converter is shown in figure 2.5.

	Low output voltage	High output voltage
Low input voltage	IPOP	IPOS
High input voltage	ISOP	ISOS

Table 2.5: Architectures and their applications

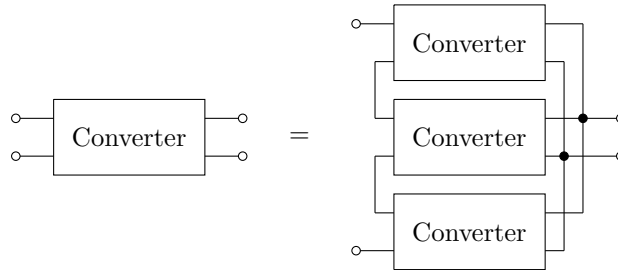


Figure 2.5: Architecture of a ISOP converter

Except for the IPOP architecture, all architectures in table 2.5 need a converter topology with galvanic isolation. This is because the series connection of the input or output causes the voltage

reference for each module to be different, which will in turn cause short circuits when connecting the modules to each other.

Because of the fact that in railway applications input voltages are high and output voltages are relatively low, while the power is high, the ISOP architecture will be best suitable architecture for railway applications. The rest of this section focusses on ISOP connected power converters.

Requirements for the control system

With converter level modularity, voltage and current sharing is achieved by using a special control system. In ISOP converters, the input voltage and output current for each module should be equal. When all modules are exactly equal, the control of one quantity also means the control of the other quantity, since the output voltage is equal for all modules. For example, when the output current is controlled and equal for all modules, the input voltage and current of all modules is also equal.

The easiest quantity to control is the output current by using a current mode control scheme. But since the input series connection is made with the aid of capacitors, a small disturbance in the input voltage of one module, due to switching or unequal capacitances, could lead to voltage overstress and breakdown. This is explained in the following way: when the output current is equally shared by all modules, the output power of each module is equal, since the output voltage is equal for all modules. Because all modules are equal, also the input power of each module is equal. The modules behave like constant power loads. When the input voltage of one module is slightly higher than the input voltages of other modules, less current is drawn by that module. But to lower the input voltage, the module should draw more current to discharge the input capacitor. In this way, the input voltage is increased more and more, until one module carries almost the full input voltage. To avoid this, both the input voltage and the output current should be controlled.

A lot of research is done on the control of ISOP converters. The main control objective of all control strategies is to obtain power balance, but the methods for achieving this balance differ. Kimball[27] proposed a sensorless current mode control, which is based on measuring the voltage across the output inductor to calculate the current flowing through it. To determine the voltage across the inductor, the total input voltage is used. Voltage measurement is usually done with the aid of a resistive voltage divider, which add losses. From this point of view, it is better to use a control strategy which uses current measurements, because these measurements can be done with less losses. Such methods are proposed by Sha[43] and Guo[18]. Their control systems show a pretty good static and dynamic performance. Disadvantages of their control system are that they are rather complex to implement and not flexible for the number of modules.

Comparison with a non-modular converter

With converter level modularity, a full converter has to be designed, but this has to be done only once. When one module is designed, only the connection between the modules have to be changed to change the input voltage and/or output power. These modules can be designed for lower input voltages and lower output power ratings. This means that not only the switches will become smaller, but also the passive components will become smaller, as the voltage and/or the current ratings will become smaller. This could reduce component cost. By putting the components on a PCB instead of mounting them in an electrical enclosure by hand can also reduce production time and cost.

The major difference between a non-modular converter and a converter level modular converter is the control. This control not only has to control the output voltage, but also the equal sharing of the input and output quantities. This makes the control more complex. To achieve voltage and current sharing, no additional power dissipation in the form of resistive losses or additional switching losses is needed.

As with switch level modularity, availability increases when there are more modules used than strictly necessary, because other modules can temporarily take over the load of the module that has to be replaced.

Due to the smaller components and smaller converters, heat is more easily dissipated. Because the connections between the modules are not part of the commutation loop and the commutation loops within the modules are smaller compared to a non-modular converter due to the smaller components used, the parasitics per commutation loop are also smaller, which make this form of modularity more suitable for high switching frequencies.

2.2.3 Discussion

In this section, the two suitable forms of modularity were described. The properties of both forms of converters are summarised in table 2.6 and explained below.

Property	Switch level	Converter level
Input voltage sharing	Passive or active, but always additional losses	Active control without additional losses
Input current sharing	Passive or active, but always additional losses or drift	Active control without additional losses
Control	Additional control for active balancing	Additional control
High frequency behaviour	Bigger commutation loops	Smaller commutation loops
Thermal management	Small increase in component area	Big increase in component area
Availability	Increase with $N + 1$ configuration	Increase with $N + 1$ configuration
Ease of manufacturing	Depends on power rating	Depends on power rating

Table 2.6: Summary of the properties of the two forms of modularity

Input voltage sharing With switch level modularity, input voltage sharing can be done passively or actively. Passive voltage sharing adds losses to the converter. Active voltage sharing is mainly done by adjusting the switching trajectory of the switch, which will increase the switching losses. Especially in high frequency operation, this is not favorable. With converter level modularity, the switching trajectory can still be optimal. To achieve input voltage sharing, only the moment of switching is adjusted by adjusting the duty cycle or on-time. This is in favor of converter level modularity.

Input current sharing With switch level modularity, input current sharing has the same disadvantages as input voltage sharing: it is always done with additional power losses. With converter level modularity, this is not the case, as the input current can be controlled by adjusting the on-time of the switch. Because the average voltage on the output inductor will change, the current through it will also change. The input current is directly related to the inductor current, so the input current will change.

Control With switch level modularity, additional control is only necessary when active input voltage or current sharing is used. With active input voltage or current sharing, the input trajectory is adjusted. This means that a very fast control system needs to be implemented to make this work, as the switching takes only a few tens of nanoseconds[9]. These control systems also need to measure voltages and currents very fast, which is also difficult to realize. Converter level modularity however doesn't need very fast control systems. A fast microprocessor is only needed for communication between modules.

High frequency behaviour With switch level modularity, the switches could be placed close together, but due to higher number of switches and the still relatively long connections between the

switches, the commutation loop increases and therefore switching behaviour is negatively affected by the increased parasitics. With converter level modularity, the switches are smaller and close together. And because the number of switches per module is small, the commutation loops are small, even smaller when one big switch is used. There is no commutation path between the modules. This is in favor of converter level modularity.

Thermal management With both forms of modularity, the bigger switch is replaced with multiple smaller switches. This increases the cooling area of the switches. This increase depends on how the switches are thermally coupled. When the switches are mounted to the same heatsink and the distance between them is small, the thermal coupling reduces the effective cooling area and thus increases the thermal resistance[42]. Although this is true for both forms of modularity and depends on the implementation, it is more likely that the modules in a converter level modular converter have their own heatsink, as these modules are standalone converters.

Availability The availability of both forms of modularity is equal and depends on the configuration and implementation. When hot swap is implemented and more modules than necessary are used in a configuration, one module can easily be replaced without shutting down a converter. When hot swap is not implemented, availability can still be increased relative to a non-modular converter, as spare parts will be smaller and thus cheaper to store in a warehouse. This means that the time needed to do a repair could be decreased.

Ease of manufacturing Ease of manufacturing depends for both forms of modularity on the power rating. When a module should have a high voltage or power rating, mounting on a PCB will not be possible anymore. This means that the ease of manufacturing compared to a non-modular high voltage/power converter can be decreased, because multiple modules have to be assembled. However, when the power rating of a module is small enough, the converter could be fit on a PCB, which could be assembled by machines, which will increase ease of manufacturing and reduce manufacturing time and cost.

Conclusion

From the observations explained above, it can be concluded that for high frequency operation, the converter level modularity architecture is the most suitable, as it has lower losses than switch level modularity and has smaller commutation loops, which means better switching characteristics.

2.3 Isolated topologies for modular converters

As described previously in section 2.2, the chosen form of modularity needs a galvanic isolated topology to avoid short circuits due to the different references of the input voltages for series-connected converters. But there is another reason a galvanic isolated topology is necessary for the proposed application of this converter. The application is a 140V battery charger, while the input voltage per module should be 1kV. Without a transformer, a very low duty cycle is needed to create such a low voltage from such a high voltage. The use of a transformer can adjust the duty cycle to a more practical value.

There are many isolated topologies known. Each topology has its own pros and cons and needs to be reviewed and compared to other topologies to determine the most suitable topology for the proposed application. To make a good comparison, each topology is evaluated and rated on the figures described below.

Voltage stress on components When the voltage stress on components is higher than the input voltage, the input voltage rating will be decreased when using the same components. Because it is preferable to have a high switch utilisation and an input voltage rating that is as high as

possible (which means less modules for the same input voltage), the voltage stress should be as low as possible.

The rating for this figure is the voltage stress across the switches, normalized to the input voltage.

Number and size of components The voltage stress will affect the voltage ratings of components. Components with a higher voltage rating are in general bigger in size. But the number and size of components is also affected by the topology itself. For example, a buck converter only uses 2 passive elements, while a Čuk converter already uses 4 passive components. A lower component count and physically smaller components are preferable.

Transformer size & complexity The total size of the converter is mainly determined by the transformer. Some topologies only use the transformer in one quadrant of the B - H curve. These topologies are called “single ended”. Topologies that use the transformer in 2 quadrants are called “double ended”. For high-voltage converters, a single ended topology is a disadvantage, because for the same flux swing, a bigger transformer is needed. This is due to the higher peak flux density in single ended topologies. On the other hand, a lower peak flux density with an equal flux swing (peak-peak value) doesn’t affect the core losses much. In high frequency converters, the power rating could be limited by the heat dissipated in the transformer.

Control Control should be easy to understand and easy to implement. Since the topology will be used in modular converters, not only the output voltage should be controlled. It is also important to control the output current to obtain input voltage sharing and output current sharing. The use of a simple control system is justified by the fact that the control system is not the main focus of this thesis.

Effects of parasitic components In some topologies, parasitic components can cause problems. For example, the parasitic inductances of transformers cause huge voltage overstress in forward converters. Because of this, lossy snubbers or additional transformer windings are added to the converter. Some other topologies doesn’t suffer from these parasitics or even use them to function, which is the case for resonant converters. The focus is mainly on the parasitic inductances of the transformer, as these parasitics have the biggest influence on the converter.

Documentation The topology should be easy to understand and design. To understand a topology, it is very helpful when proper documentation is available. The amount of documentation is also an indication of the “popularity” of a certain topology. When there is only a small amount of papers available about a topology, there is a high probability that that topology is never used in practice. But when there is a huge number of application notes, design guides, datasheets and websites available about a topology, this means that the topology is used in practice and that it is more or less a proven technology.

2.3.1 Forward based topologies

The forward converter is a modified buck converter with isolation. The basic layout is shown in figure 2.6. The transformer acts as a transformer in the sense that it is not used to store energy but to transfer energy.

Voltage stress Ideally, the transformer should not contain a magnetizing inductance. But since every transformer contains such a parasitic inductance, an additional winding needs to be added to create a freewheel path for the magnetizing current. This means that a three winding transformer has to be used. The third winding is connected to the input voltage through a diode. This means that the voltage on the switch during the off-period is higher than V_{in} . It is determined by the number of windings for the tertiary winding: the lower this number, the higher the voltage stress.

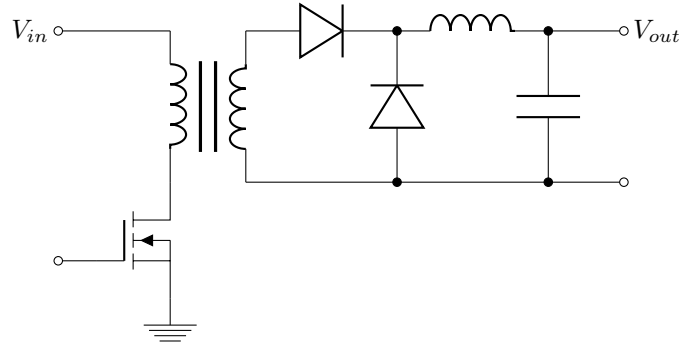


Figure 2.6: Ideal forward converter without demagnetizing winding

Rating: > 1

Number and size of components The need for a tertiary winding and a diode increases the component count. The parasitic inductances of the transformer could also be used to achieve resonant switching (with lossless snubbers or with the active clamp forward converter[49]), but this also increases the component count.

Rating: 0

Transformer size & complexity Based on the chosen variant, the transformer could be a simple two-winding transformer or a more complex three-winding transformer. This topology is single ended, which means a relatively big transformer needs to be used.

Rating: -

Control The freedom to choose the duty cycle is limited by the magnetizing inductance. With the use of the three-winding transformer and freewheel diode, the maximum duty cycle is related to the number of turns of the tertiary winding: the lower this number, the higher the maximum duty cycle is. The control complexity of the active clamp forward converter is increased by the fact that there is an additional switch which clamps the main switch voltage. Except from these remarks, the control of a forward converter is pretty straightforward, as it is basically a buck converter.

Rating: +

Effects of parasitic components As described before, the magnetizing inductance of the transformer gives several problems. But also the leakage inductance gives problems. Without active clamp forward topology, a snubber needs to be used to limit the voltage stress on the switch. However, when only a capacitor is placed in parallel with the switch, zero voltage switching could be achieved.

Rating: -

Documentation The forward converter is based on the buck converter, which is a topology quite often used. This means that most documentation available for the buck converter could also be used for the forward converter.

Rating: ++

2.3.2 Push-pull converter

The push-pull converter is another way to create an isolated buck converter. It is shown in figure 2.7. It is a variant of an interleaved forward converter constructed in which the two sub-converters share the same transformer.

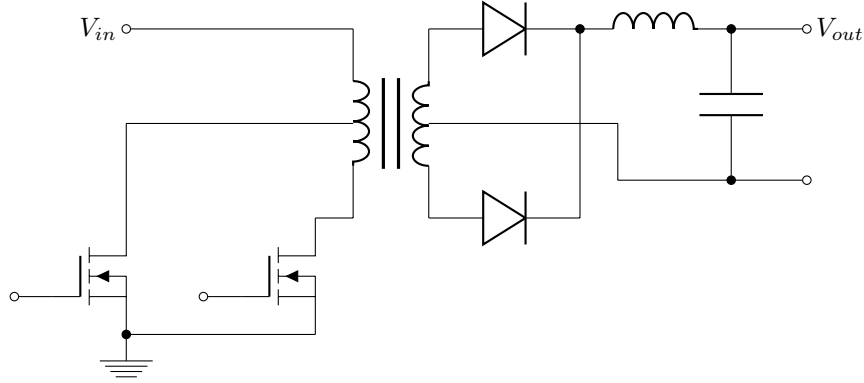


Figure 2.7: Push-pull converter

Voltage stress Because the push-pull converter has two series-connected primary windings, the voltage on the conducting winding is also present on the other winding. This will cause the voltage stress on the non-conducting switch to be double the input voltage.

Rating: > 2

Number and size of components Since the push-pull converter is a interleaved form of a forward converter, number of components is higher than for the forward converter. On the other hand, the frequency seen by the filter components is double the switching frequency of the primary switches. This enables the use of smaller filter components. So in the end, the size of the converter, except for the transformer, will be the same as for the forward converter.

Rating: $+$

Transformer size & complexity Because of the transformer winding arrangement, the transformer is operated in two quadrants of the B - H curve instead of just one quadrant. This means a relatively small core. But because of its winding arrangement, the transformer design will be more complex and the transformer still needs to be big.

Rating: $-$

Control To control this topology, current mode control is needed. When current mode is not used, it is possible that the magnetization will not be fully cancelled during a switching cycle[49]. Simulations reveal that with unequal windings for the primary side the magnetizing current will not increase to infinity. The current increase stops at a certain level. The result of the unequal windings is an offset in the magnetizing current. Care has to be taken to keep this current below the saturation current. Although the use of current mode control is a restriction in the control, it doesn't necessarily increase the control complexity, as current control is also needed to achieve output current sharing across multiple modules when using an ISOP architecture.

Rating: $+$

Effects of parasitic components The antiparallel diodes of the switches can form a freewheel path for the magnetizing current. When this happens, the switches are turned on with zero voltage. The magnetizing inductance can thus be used in a positive way. However, the leakage inductance could not be used in a positive way and causes additional stress on the switches. Snubbers need to be used to limit this additional voltage stress.

Rating: 0

Documentation As this converter is also a variant on the forward converter, there is also a lot of documentation available.

Rating: $++$

2.3.3 Flyback converter

The flyback converter is a modified buck-boost converter with isolation. It is commonly used in low power power supplies, such as mobile phone chargers. A flyback converter is shown in figure 2.8.

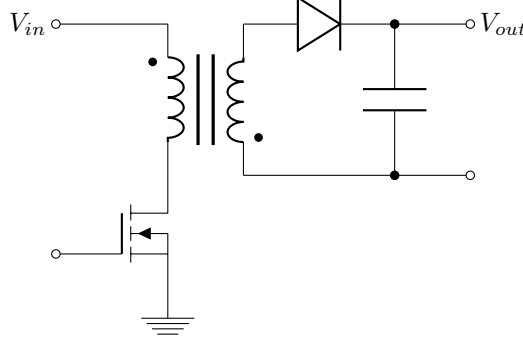


Figure 2.8: Flyback converter

Voltage stress The voltage stress is caused by the reflected output voltage and is thus directly related to the duty cycle. The minimum voltage stress is in equation (2.3), with V_{SW} the peak value of the switch voltage, V_{in} the input voltage, V_{out} the output voltage, N_p the primary number of turns of the transformer, N_s the secondary number of turns of the transformer and d the duty cycle. From this equation it follows that the voltage stress is always significantly more than V_{in} .

$$V_{SW} = V_{in} + \frac{N_p}{N_s} V_{out} = V_{in} + \frac{N_p}{N_s} \cdot \frac{d}{1-d} \frac{N_s}{N_p} V_{in} = V_{in} \frac{1}{1-d} \quad (2.3)$$

Rating: > 1

Number and size of components The popularity of the flyback converter for low power power supplies is mainly due to the small number of components required. The size of the capacitor should be relatively big, as the current flowing to the capacitor through the transformer is discontinuous. Snubbers which reduce the voltage stress on the switch caused by the leakage inductance of the transformer will increase the component count.

Rating: 0

Transformer size & complexity In the flyback converter, the transformer is used as an energy storage component. This means that the magnetizing inductance of the transformer should have a specified value to store the energy. The flyback topology is single ended, which needs a relatively big transformer. To avoid saturation, the transformer should be big or an airgap needs to be introduced. An airgap will decrease the coupling between the two windings and will therefore increase the leakage inductance.

Rating: --

Control The control of the flyback converter is pretty straightforward and does not require special measures to avoid unwanted effects such as transformer saturation. However, the duty cycle of the flyback transformer is limited by the transformer ratio. When the duty cycle is higher than this maximum, the converter starts to operate as a step-up converter.

Rating: +

Effects of parasitic components The leakage inductance of the transformer will cause voltage stress on the switches. Snubbers are required to avoid this. On the other hand, when a capacitor is placed across the switch, zero voltage switching could be achieved. The magnetizing inductance is used as an energy storage component and doesn't give problems.

Rating: -

Documentation This topology is a very often used topology, so a lot of documentation is available.

Rating: ++

2.3.4 Isolated Ćuk and SEPIC converters

Ćuk and SEPIC converters both have a isolated variant. These variants are shown in figure 2.9.

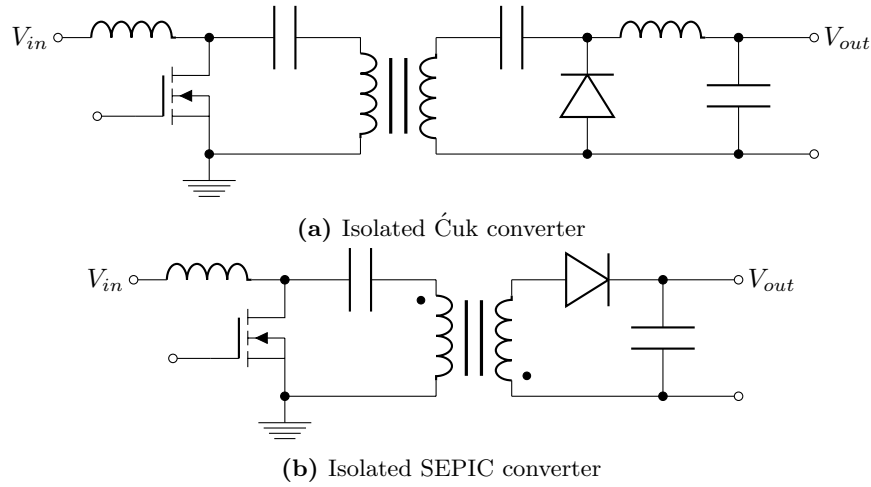


Figure 2.9: Isolated Ćuk and SEPIC converters

Voltage stress In steady state, the average voltage across the primary inductor of both topologies is 0V. This means that the voltage stress across the switch will always be larger than the input voltage. During the on-time, the voltage across the inductor is V_{in} , so during the off-time, the voltage has to be $\frac{1}{1-d} V_{in}$, which is always higher than V_{in} .

Rating: > 1

Number and size of components Both topologies need a relatively high number of passive components. For Ćuk converter, this number is 5, while this number is 4 for the SEPIC converter. However, the output capacitor for the SEPIC needs to be bigger than for the Ćuk, since the current to the output capacitor is not continuous. The capacitors connected to the transformer should be big in both converters to keep the voltage constant. The voltages across these capacitors depend on the transformer ratio (both Ćuk and SEPIC) and the values of their capacitances (only Ćuk), but in general these voltages will be bigger than the input voltage.

Rating: -

Transformer size & complexity In the Ćuk converter, the transformer is used as a transformer and not as an energy storage component. In the SEPIC converter, the transformer is used as an energy storage component, so the transformer should have a specified magnetizing inductance. Both topologies are single ended, so the transformer is relatively big.

Rating: -- (SEPIC)/- (Ćuk)

Control Both topologies have a high number of storage components. This means that the response of these topologies to transients are slow. This is a disadvantage because the output voltage will be less stable. Because the input-output relation of both topologies is the same as for the flyback converter, the duty cycle is limited by the transformer ratio.

Rating: -

Effects of parasitic components In both converters, the effect of the leakage inductance is that it will cause additional stress on the switch. In the SEPIC converter, the magnetizing inductance is used for energy storage. In the Ćuk converter, this inductance will cause more voltage stress on the switch. Resonant operation of both topologies is possible.

Rating: -

Documentation Both topologies are less common than the other topologies. As a result of this, less literature and design guides for these topologies could be found.

Rating: +

2.3.5 Bridge topologies

There are several topologies based on a bridge. These include the half bridge, the full bridge and the dual active bridge. These converters all have a buck output stage consisting of an inductor and a capacitor. This makes control easy. The basic principle for these topologies is the same, but their inverting or rectifying parts differ. Because these parts differ, the number of control schemes that can be applied also differ.

All these topologies have the advantage of operating the transformer in 2 quadrants. Although the component count could be somewhat higher compared to other topologies, bridge topologies need a smaller transformer and therefore have an advantage over other topologies. The bridge structure has the advantage of eliminating problems arising from parasitic inductances from the transformer, so no snubber components will be needed. These parasitics could even be used to achieve zero voltage turn-on.

All bridge converter have the same output stage as a buck converter. This means that most principles used to control a buck converter could also be applied to the bridge converters.

Half bridge converter

The half bridge converter is shown in figure 2.10. It uses two capacitors to create a midpoint voltage, which is half the input voltage.

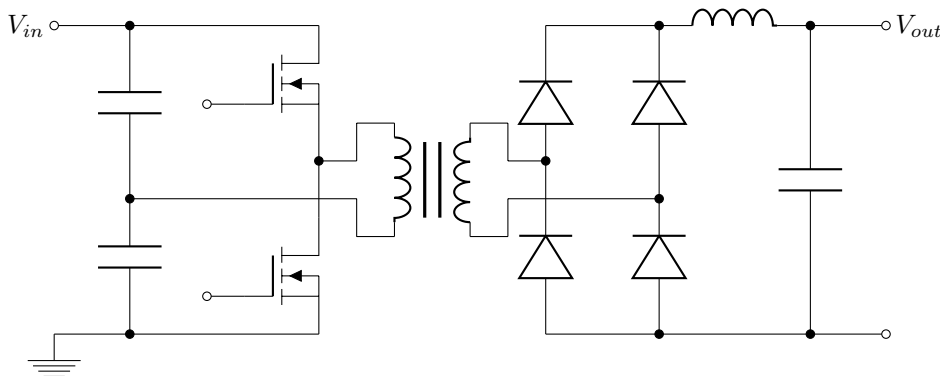


Figure 2.10: Half bridge converter

Voltage stress The voltage stress equal to the input voltage.

Rating: 1

Number and size of components The number of components for the half bridge converter is relatively high, as the bridge structure requires 4 components. The bridge capacitors need to be relatively big to keep the midpoint at $\frac{1}{2}V_{in}$.

Rating: 0

Transformer size & complexity As the applied voltage to transformer is $\frac{1}{2}V_{in}$, the volt-second product for the transformer is relatively low, which means that the transformer could be relatively small. But the currents are relatively big, which means that the wires, and thus the transformer, should be relatively big.

Rating: +

Control The half-bridge has the disadvantage that only one operating mode can be employed: bipolar switching. An advantage of the half bridge is that only 2 switches have to be controlled. Simulation results reveal that an unbalance in the on-time of the switches and unequal midpoint capacitors will not cause runaway of the midpoint voltage or magnetizing current. The converter responds in such a way that the volt-second balance is maintained. This avoids saturation, but affects the operation of the converter in the sense that the output voltage will be (slightly) different than expected.

Rating: +

Effects of parasitic components Bridge topologies doesn't suffer from additional voltage stress caused by transformer parasitics. These parasitics could be used for zero voltage turn-on. When the lower switch is turned off, the transformer current will flow through the antiparallel diode of the upper switch. When this is the case, the turn-on voltage of the upper switch is equal to the diode forward voltage, which limited to only a few volts.

Rating: +

Documentation This converter often used for higher power converters. This converter is operated in the same way as a buck converter, so there is much documentation available.

Rating: ++

Full bridge converter

The full bridge converter is shown in figure 2.11. Compared to the half bridge, the two midpoint capacitors are replaced by switches.

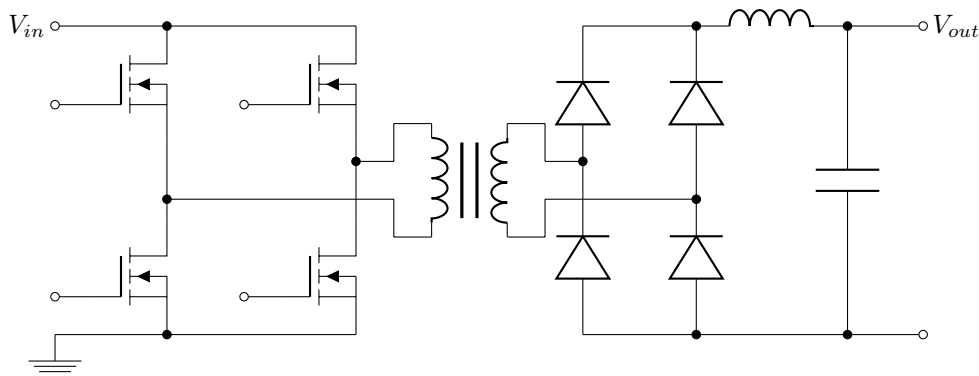


Figure 2.11: Full bridge converter

Voltage stress The voltage stress is equal to the input voltage.

Rating: 1

Number and size of components Compared to the half bridge, the number of components is the same, but the two big midpoint capacitors are replaced with switches. With phase shifted switching, the frequency seen by the output filter is double the switching frequency, so the size of the filter component could be reduced.

Rating: +

Transformer size & complexity As the applied voltage to transformer is V_{in} , the volt-second product for the transformer is relatively big, which means that the transformer should be relatively big. But the currents are relatively small, which means that the wires, and thus the transformer, should be relatively small.

Rating: +

Control The only problem that the control has to address is saturation of the transformer. When the on-times of the transistors differ too much, the volt-second balance will be violated and the magnetizing current will increase. The core of the transformer will saturate and the transformer starts to behave as an air core inductor.

The full bridge converter has more operating modes than the half bridge. These modes are: bipolar switching and phase shifted switching. In the unisolated full bridge converter, unipolar operation is also possible. But applying unipolar switching to a transformer will drive the transformer into saturation within a few switching cycles, because the transformer will not be demagnetized.

Rating: ++

Effects of parasitic components As for all bridge converters, no problems arise from the transformer parasites. They can even be used to achieve zero voltage turn-on[20].

Rating: +

Documentation With respect to the available documentation, the same can be said about the full bridge converter as for the half bridge converter.

Rating: ++

Dual active bridge converter

The dual active bridge is a combination of two full bridge converters, as shown in figure 2.12. One bridge is used as inverter, while the other is used as controlled rectifier. Because the inverting and rectifying stage are the same, the power flow can be bidirectional.

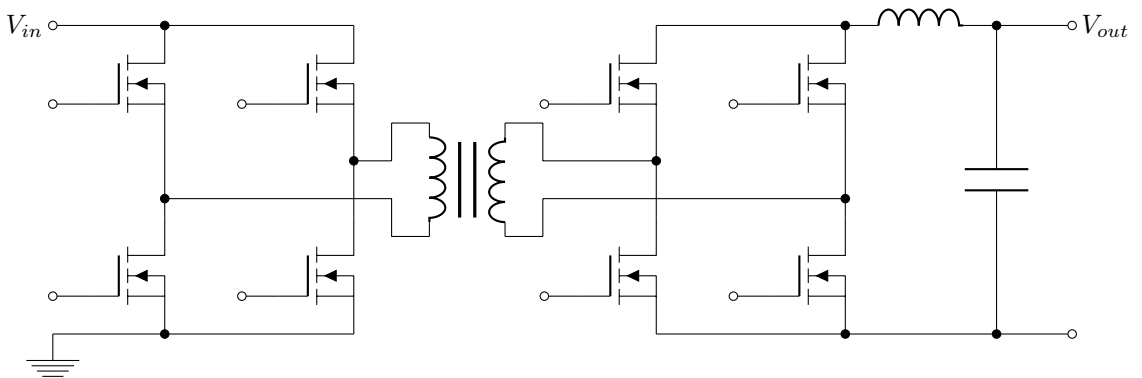


Figure 2.12: Dual active bridge

Voltage stress The voltage stress is equal to the input voltage.

Rating: 1

Number and size of components The number of components is increased compared to the full bridge converter. At the secondary side, the number of semiconductors will be doubled compared to a full bridge rectifier, since in reality the diodes are not replaced by the switches. The switches are placed in parallel to the diodes. The secondary switches also need a driver circuit, whereas the secondary diodes of a full bridge rectifier don't need drivers. The advantage is that losses in the secondary side are smaller, because the conduction losses for a MOSFET are lower than for a diode. This means that the heatsinks could be smaller.

Rating: -

Transformer size & complexity The transformer is the same as for the full bridge converter.

Rating: +

Control Because of the increased number of switches, control complexity is increased. The increased number of switches is because the converter is symmetric, which enables bidirectional power flow. The number of operation modes is therefore doubled compared to the full bridge rectifier.

Rating: +

Effects of parasitic components As for all bridge converters, no problems arise from the transformer parasitics.

Rating: +

Documentation Because this converter has a controlled inverter and a controlled rectifier, many control techniques could be applied. A lot of research is done on this converter. And because its output stage is the same as for a buck converter, a lot of documentation for the buck converter could also be applied to the dual active bridge converter.

Rating: +

2.3.6 Isolated resonant link converters

Hard switching causes high switching losses and parasitic components cause overvoltages and saturation. These problems can only be fully solved by soft switching topologies, which use the already present parasitics to create a resonant circuit. During the resonant oscillation, there are moments where the voltage across a switch or the current through a switch are zero. When the switch is turned at such a moment, there are no switching losses. In practice, there is always some delay from the controller to the switch, so there are still losses, but much less compared to hard switching. There are a few topologies that make use of soft switching. Two of them are covered in this section.

Parallel loaded resonant converter

A parallel loaded resonant (PLR) converter is shown in figure 2.13. The resonance is between L_r and C_r . Because the load is connected in parallel to a capacitor (C_r), this converter acts as a voltage source. The inverting and rectifying parts of the converter could differ from what is shown in figure 2.13. In fact, every kind of inverter (half bridge, full bridge or just a single phase leg with one end of the resonant tank connected to ground) and rectifier (full bridge or full wave) could be used.

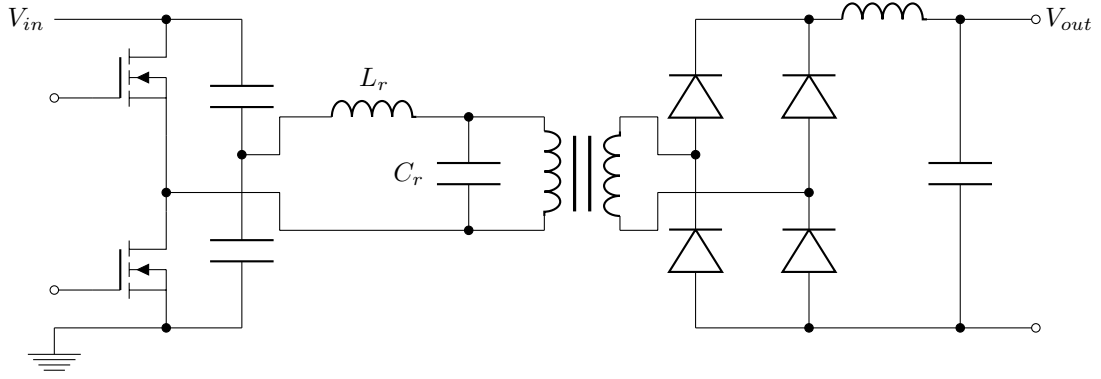


Figure 2.13: Parallel loaded resonant converter

Voltage stress In the parallel loaded resonant converter, the stress on the switch is equal to the input voltage, as the inverting part of the converter is equal to that of the half bridge converter. This part could also be replaced with a full bridge.

Rating: 1

Number and size of components In a parallel loaded resonant converter, the number of components is higher than for a normal bridge converter. This is due to the resonant tank circuit, consisting of a capacitor and an inductor. The components for the parallel loaded resonant converter should be relatively big in size to accomodate for the conduction losses created by the reactive current which keeps the circuit in resonance[55].

Rating: 0

Transformer size & complexity The transformer could be the same as for a normal bridge converter.

Rating: +

Control The control of the parallel loaded resonant converter is rather complex, as the input-output relation is based on the switching frequency. There are three operating modes: discontinuous mode ($f_{sw} < \frac{1}{2}f_0$), continuous mode below f_0 and continuous mode above f_0 [34]. Usually, the continuous mode operation above f_0 is considered as the best mode, because the switches are switching at zero voltage in that mode. ZVS is better than ZCS, because with ZCS the drain-source capacitor still needs to be discharged and thus creates losses.

Rating: -

Effects of parasitic components The transformer parasitics are not used in this topology, but they will not create additional stresses on the switches, since the voltage on one switch is always clamped by the other switch.

Rating: +

Documentation This converter is almost not used in practice. Therefore, there is very little documentation on this converter.

Rating: -

Other remarks Yang[55] claimed that the parallel resonant converter is not suitable for a converter with a wide input voltage range.

LLC converter

The LLC converter looks basically the same as a series loaded resonant converter, but is more frequently used. It is shown in figure 2.14. The difference is in the control of the converter. The LLC converter is called this way because the resonant components are two inductances and one capacitor. The advantage of this converter is that the parasitic inductances of the transformer (leakage inductance L_σ and magnetizing inductance L_m) could be integrated into the transformer. Just like for the parallel loaded converter, the inverting and rectifying parts could differ from what is shown in figure 2.14.

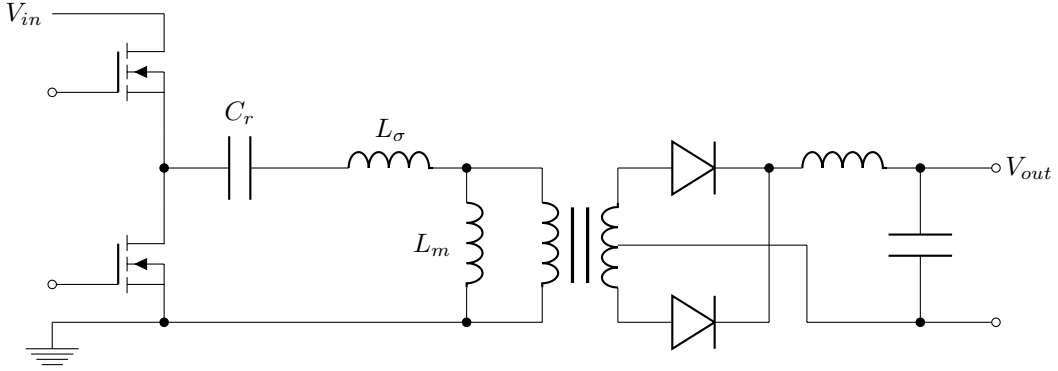


Figure 2.14: LLC hybrid resonant converter

Voltage stress As with all bridge converters, the voltage stress on the switch equals the input voltage.

Rating: 1

Number and size of components Compared to bridge converters, the component count is increased because of the resonant capacitor C_r . The resonant inductors could be integrated within the transformer and therefore do not increase the component count. But because of the reactive current needed to keep the circuit in resonance at light load[44], the physical size still needs to be relatively big.

Rating: +

Transformer size & complexity The transformer size and complexity is the same as for a bridge converter, except for the fact that the magnetizing and leakage inductances should have specified values. This will increase manufacturing complexity.

Rating: 0

Control Control of the LLC converter is approximately equal to the control of the parallel loaded resonant converter. When burst-mode control is used, the constant reactive current flow at light load is avoided[16]. Current mode control can also be used with this converter[23].

Rating: -

Effects of parasitic components In this topology, the parasitic inductances of the transformer are used as part of the resonant circuit.

Rating: ++

Documentation Compared to the parallel loaded resonant converter, there is much more documentation available on the LLC converter. However, compared to the buck-based converters, there is not much documentation available.

Rating: 0

Other remarks Yang[55] compared the series loaded resonant converter, the parallel loaded resonant converter and the series parallel loaded converter with the LLC converter and came to the conclusion that the latter was the most suitable converter for high voltages.

2.3.7 Discussion

Table 2.7 gives a summary of the ratings given in the descriptions of the topologies. From this table, it is clear that the full bridge topology is the best suitable converter, due to its simple buck-like control and its small transformer. Especially the phase shifted operation is suitable, as this topology adds almost no complexity to the control while reducing the turn-on losses and doubling the switching frequency seen by the filter components, thus reducing the size.

Topology	Voltage stress	Components	Transformer	Control	Parasitics	Documentation
Forward based	> 1	0	-	+	-	++
Push-pull	> 2	+	-	+	0	++
Flyback	> 1	0	--	+	-	++
Isolated Ćuk	> 1	-	-	-	-	+
Isolated SEPIC	> 1	-	--	-	-	+
Half bridge	1	+	+	+	+	++
Full bridge	1	+	+	++	++	++
Dual active bridge	1	-	+	0	++	++
Parallel loaded resonant	1	-	+	-	++	0
LLC	1	0	0	-	++	+

Table 2.7: Overview of isolated topologies

Chapter 3

Design of hardware and control system

This chapter describes the design of the converter. First, a detailed version of the design specifications is given. The actual design is then split into two parts: the hardware and the control system.

3.1 Design specifications

In the previous chapter, the concepts for the modular SiC based converter were reviewed. To design the converter, additional specification are needed. These specifications are split up in two parts. The first part contains the specifications for the complete converter. The complete converter consists of one or more modules. The second part contains the specifications of a single module.

3.1.1 Specifications for the complete converter

The complete converter has to satisfy the following specifications:

Requirements

1. The inputs of the modules have to be connected in series, while the outputs have to be connected in parallel (ISOP).
2. The input voltage ranges from 500V (lowest voltage in a 750V traction system) to 2kV (two times the highest voltage in 750V traction system^[7]).
3. The system should be able to operate without master module.

Wishes

1. Possibility of connecting multiple parallel branches of series connected modules to the same output.
2. The maximum input voltage is extended to 3.9kV (highest voltage in a 3kV traction system^[7]).
3. The modules should be hot-pluggable.
4. The system should be able to operate in $N - 1$ situations, which means that it should still operate when one module is out of service.
5. The modules should be able to operate in an interleaved way.

The requirement for ISOP follows from the fact that many converters for railway applications face a high input voltage due to the high traction system voltages. The lowest nominal DC voltage is 600V, while the highest nominal DC voltage is 3kV. There are higher traction system voltages (15kV and 25kV and on some lines even 50kV), but these voltages are AC and are usually stepped down with a transformer before they are connected to the power converters. The input voltage levels follow from the choice to make the whole system suitable for all DC traction system voltages.

The wishes for $N - 1$ operation and hot-pluggable modules follow from the wish to have a system with high reliability and availability. When one module fails, the whole converter should still be able to work and maintenance personnel should be able to replace the broken module without switching off the input power.

When the modules only operate with the presence of a fixed master module, this master module acts as a single point of failure. This should be avoided.

3.1.2 Specifications for one module

One module has to satisfy the following specifications:

Requirements

1. The topology is a full bridge.
2. The module is operated in phase shifted operation mode.
3. The switches to be used are Cree C2M0080120D SiC MOSFETs.
4. The input is separated from the output by galvanic isolation. The isolation level has to be at least 1.5kV.
5. The control system has to be able to control the input power to achieve input voltage sharing.
6. The maximum input voltage is 1000V.
7. The output current is limited during short circuit.
8. The output voltage is 140V.
9. The allowed peak value of the output voltage is 5% higher than the nominal output voltage.

Wishes

1. The switching frequency should be at least 30kHz.
2. The isolation level between the primary and secondary side of the converter should be at least 10kV AC.
3. The output voltage should be adjustable by choosing a different turns ratio for the transformer and by adjusting the feedback network.

The requirement for galvanic isolation follows from the chosen form of modularity. This is described in section 2.2. The input voltage rating follows from the fact that a Cree C2M0080120D MOSFET is selected to build the converter. This switch is able to switch 1200V. To have a safety margin, 1000V is chosen to be the maximum input voltage. The switching frequency should be above the audible spectrum (20Hz to 20kHz). To have some margin, the minimal operating frequency is chosen to be 1.5 times higher.

As the first prototype should be used as a battery charger, the output voltage should be 140V. To be able to use the converter for other purposes, the output voltage should be adjustable by changing the transformer winding ratio or the feedback network of the controller.

3.2 Hardware

With the design specifications, the hardware can be designed. The design of the hardware is done in several steps:

1. Transformer design
2. Design of the gate driving circuit
3. Obtaining the power rating
4. Calculation of the output filter components
5. Evaluation of the design using simulations and iteration when necessary

Switching frequency and duty cycle The converter is a phase shifted full bridge converter. This has some implications on the definition of the switching frequency and the duty cycle. The waveforms for one period are shown in figure 3.1. v_T is the voltage across the transformer and i_L is the inductor current. It is shown that the frequency of the inductor current is double the frequency of the primary side (f_{SW}). In this thesis, the switching frequency refers to the frequency at the primary side. The duty cycle is the time that the voltage across the transformer is nonzero divided by the period. This means that the definition of the duty cycle is the same for both the primary and the secondary side.

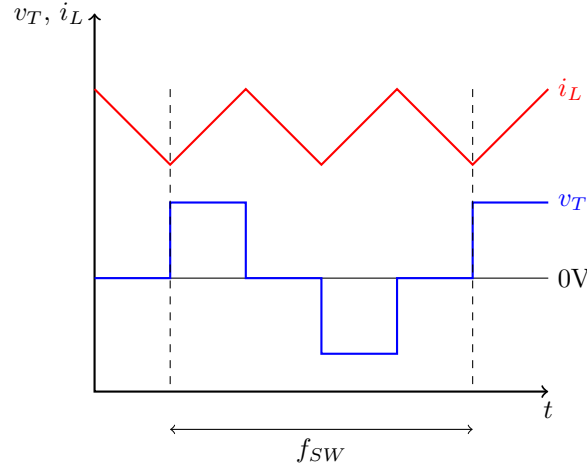


Figure 3.1: Waveforms of a phase shifted full bridge converter

3.2.1 Zero voltage switching

The converter is operated as a phase shifted full bridge converter. It tries to achieve zero voltage switching at turn-on of the switches. To achieve this, some resonance is needed. In this circuit, the resonance is between the output capacitances of the MOSFETs and the junction capacitances of the antiparallel diodes and the leakage inductance of the transformer.

The amplitude V_0 of this voltage oscillation is determined by equation (3.1) and the resonant frequency f_0 is determined by equation (3.2), with L the equivalent inductance, C the equivalent capacitance and I_{in} the input current of the converter.

$$V_0 = Z_0 I_{in} = \sqrt{\frac{L}{C}} I_{in} \quad (3.1)$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (3.2)$$

The equivalent inductance is simply the primary leakage inductance of the transformer. The magnetizing inductance of the transformer and the secondary side output inductance don't play a role in the resonant circuit, since these inductances are very big compared to the leakage inductance and behave as constant current sources. The capacitance of the secondary rectifier diodes is reflected by the transformer. The reflected capacitance is calculated with the data from the datasheet[13] and table 3.1 and equals 6051pF. The equivalent capacitance is calculated from the circuit shown in figure 3.2. In this figure is $C_{rect} = 6051\text{pF}$ the reflected rectifier capacitance, C_{oss} the output capacitance of the MOSFETs and C_j the junction capacitance of the antiparallel diodes.

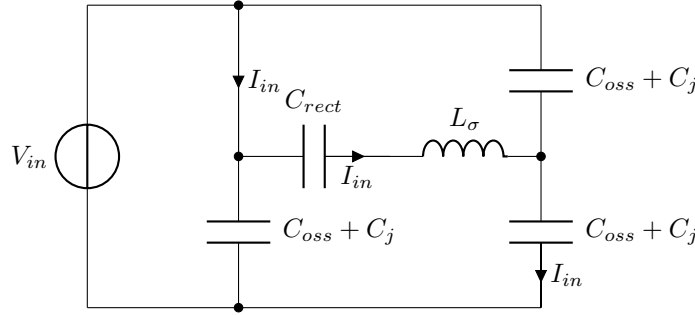


Figure 3.2: Resonant circuit just after a switch, in this case the bottom left one, has opened. The arrows indicate the input current flow as it was before the switch opened.

The equivalent capacitance is calculated with $C' = \frac{1}{2}(C_{oss} + C_j)$ (two capacitances in series, parallel with one capacitance) and $C = \frac{C' C_{rect}}{C' + C_{rect}}$. The value for C' is calculated with the values for C_{oss} and C_j from the datasheets[9, 10] and equals 371pF. With this value, C can be calculated and equals $C = 349\text{pF}$. The maximum input voltage is 1000V, so $V_0 > 1000\text{V}$. The minimum value for L_σ is then calculated with (3.3).

$$L_\sigma \geq C \left(\frac{V_0}{I_{in}} \right)^2 = 349\text{pF} \cdot \left(\frac{1000\text{V}}{I_{in}} \right)^2 \quad (3.3)$$

3.2.2 Transformer design

The transformer is designed in such a way that the duty cycle equals $d = 0.5$ when the input voltage is 750V, the center of the operating range of one module. The input voltage to output voltage ratio of a full bridge converter is given in equation (3.4), with V_{out} the output voltage, V_{in} the input voltage, d the duty cycle, N_s the secondary number of turns and N_p the primary number of turns. Using this equation, the transformer ratio equals $\frac{N_s}{N_p} = \frac{28}{75} \approx 0.373$. With these values, the boundaries of the duty cycle were calculated. This gave the result that d is always between 37.5% and 75%.

$$\frac{V_{out}}{V_{in}} = d \frac{N_s}{N_p} \quad (3.4)$$

Then the number of turns has to be calculated. This is done in the following steps:

1. Select a core shape and material

2. Select a switching frequency to obtain the volt-second product
3. Calculate the number of turns for the primary side with equation (3.5)
4. Iterate until a reasonable number of turns is obtained. Reasonable is around 50.

$$N_p = \frac{V_{in}d}{2f_{SW}B_{max}A_{min}} \quad (3.5)$$

In equation (3.5) is f_{SW} the switching frequency, B_{max} the maximum magnetic flux density in the core and A_{min} the minimum cross-section of the core. The factor two results from the fact that the volt-second product depends on the secondary frequency instead of the switching frequency.

The results of the process described above is shown in table 3.1. The calculations were done with $B_{max} = 300\text{mT}$, $V_{in} = 750\text{V}$, $d = 0.5$ and $f_{SW} = 100\text{kHz}$. The value of the magnetizing inductance is calculated using the A_L value as stated in the datasheet of the core shape.

Quantity	Value
Core shape	ETD 44/22/15[48]
Core material	N97 ($B_s = 400\text{mT}$ at $T = 100^\circ\text{C}$)[47]
B_{normal}	214mT
N_p	51
N_s	18
Turns ratio	0.353
L_m	11.4mH

Table 3.1: Parameters of the designed transformer

The windings are made using litz wire to reduce the skin effect. The windings are not interleaved to have some leakage inductance needed for ZVS. The parameters of the actual transformer are in table 3.2. The expected core losses are approximately 3.6W.

Winding	Magnetizing inductance	Leakage inductance	Wire resistance
Primary	10.2mH	12.3μH	1104mΩ
Secondary 1		1.08μH	19.1mΩ
Secondary 2		2.32μH	22.4mΩ

Table 3.2: Measured parameters of the transformer

3.2.3 Obtaining the power rating

In order to calculate the filter component values, the value of the average output current should be known. The value of this current follows from the power rating of the converter, as the output voltage is fixed to 140V.

It is assumed that the output power is limited by the maximum power dissipation of the MOSFET. Other components also have maximum allowable temperatures, but it is assumed that the losses are the highest in the MOSFETs. By using a heatsink and a suitable thermal pad, an equivalent thermal resistance of $R_{ja} = 6.2\text{K/W}$ is obtained. The maximum junction temperature T_j of the MOSFET is 150°C . In order to have some margin to the boundaries of the safe operating area, the maximum operating temperature of the junction is set to 125°C . As the worst case ambient temperature is approximately 45°C , the maximum power dissipation equals $P_{max} = \frac{125^\circ\text{C} - 45^\circ\text{C}}{6.2\text{K/W}} = 12.9\text{W}$.

The power loss in a MOSFET could be approximated by equation (3.6), with P_{loss} the power loss, I_{out} the output current, t_{off} the turn-off time of the MOSFET and $R_{DS(on)}$ the on-state

resistance of the MOSFET. The value of $R_{DS(on)}$ is $112\text{m}\Omega$, the on-resistance at $T_j = 125^\circ\text{C}$. Because of the ZVS at turn-on, only the conduction losses and turn-off losses are considered. The turn-off time is approximated by using the $\frac{dV_{DS}}{dt}$ of the switch. This value is obtained by simulating the gate driving circuit and is $40\text{kV}/\mu\text{s}$. By using these equations with $V_{in} = 1000\text{V}$ and $f_{SW} = 100\text{kHz}$, the maximum output current is approximately $I_o = 25\text{A}$.

$$P_{loss} = \frac{1}{2}V_{in} \frac{N_s}{N_p} I_{out} t_{off} f_{SW} + d \left(\frac{N_s}{N_p} I_{out} \right)^2 R_{DS(on)} \quad (3.6)$$

$$t_{off} = \frac{V_{in}}{\left(\frac{dV_{DS}}{dt} \right)} \quad (3.7)$$

3.2.4 Dimensioning of filter components

The filter components are calculated with the well known equations for the filter component values for a buck converter operating in continuous conduction mode steady state operation. These equations are modified to incorporate the transformer transfer ratio and are in equations (3.8) and (3.9). In these equations, ΔI is the peak to peak current ripple, ΔV the peak to peak output voltage ripple and T_{SW} is the switching frequency period time. The amplitude of the current ripple is chosen to be less than 15% of the average load current at $I_o = 25\text{A}$, so $\Delta I = 7.5\text{A}$. ΔV is set to 14V , the peak to peak value of the allowed deviation from the nominal output voltage.

$$L \geq \frac{1}{2} d T_{SW} \frac{\frac{N_s}{N_p} V_{in} - V_{out}}{\Delta I} \quad (3.8)$$

$$C \geq \frac{\frac{1}{2} \cdot \frac{1}{2} T_{SW} \cdot \frac{1}{2} \Delta I}{\Delta V} \quad (3.9)$$

The highest inductance is required with the highest input voltage. The required inductance with $V_{in} = 1\text{kV}$ is $53.2\mu\text{H}$ and the required capacitance as 670nF . This inductance value is not commercially available for the desired current levels. The highest available PCB mount inductor at the desired current levels has an inductance of $22\mu\text{H}$ and a saturation current of 26A . This limits the output current. The maximum current ripple with this inductance (at $V_{in} = 1000\text{V}$) is $\Delta I = 18.1\text{A}$, so the output current will be $26\text{A} - \frac{18.1\text{A}}{2} = 17\text{A}$. To keep the output voltage constant with an increased inductor ripple current, a bigger output capacitor will be used, since the calculated output capacitance is very low. The new output capacitance will be $1.62\mu\text{F}$.

As transients in the output current could cause output voltage overshoot, this has also to be considered during the design. The extreme case is examined: from full load current to no-load. This means that all energy stored in the inductor will charge the output capacitor. The energy in an inductor is $W_L = \frac{1}{2} L i_L^2$. The energy in a capacitor is $W_C = \frac{1}{2} C v_C^2$. It is assumed that the inductor is charged to $i_L = I_{sat} = 26\text{A}$ and that the capacitor voltage is equal to $v_C = V_{out,nom} = 140\text{V}$. The required capacitance to limit the voltage increase by $5\% \cdot V_o = 7\text{V}$ is calculated with equation (3.10), with $V_{C,max}$ the maximum output voltage and $V_{C,nom}$ the nominal output voltage. Using this equation, the required capacitance equals $7.4\mu\text{F}$. With this capacitor, the peak to peak voltage ripple during steady state and full load equals $\Delta V = 3.06\text{V}$. Due to the unclear definition of the duty cycle and switching frequency used during the first calculations, the capacitor used in the real circuit is a $6.8\mu\text{F}$ capacitor.

$$C = \frac{L i_L^2}{V_{C,max}^2 - V_{C,nom}^2} \quad (3.10)$$

3.2.5 Input capacitor

To create the ability of connecting multiple modules in series, the modules need to have a input capacitor. This capacitor also supplies the peak currents drawn by the converter and keeps the input voltage stable. The capacitance is calculated with the estimated maximum output load, the minimum input voltage and the estimated time for the control to take action when there is a difference in input voltages of multiple modules. The maximum output power is $140\text{V} \cdot 17\text{A} = 2380\text{W}$. The maximum input current occurs when the input voltage is at its minimum: $\frac{2380\text{W}}{500\text{V}} = 4.76\text{A}$. The maximum voltage drop is set to $\Delta V_{in} = 50\text{V}$ and the reaction time for the control is estimated at $136\mu\text{s}$. This makes the minimum value for the input capacitance $C_{in} \geq 12.9\mu\text{F}$. To have some margin for the implementation of the control, a $27\mu\text{F}$ capacitor is used in the circuit.

3.2.6 Gate driving

The MOSFETs need to be driven in order to switch. There are multiple methods of gate driving. Some of them are resistive gate driving and resonant gate driving. Strukton Rolling Stock developed a proprietary circuit to drive the gates of IGBTs. These methods are shortly reviewed to pick the right one.

Resistive gate driving Resistive gate driving is the most used method of gate driving. It consists of a powerful voltage source connected to the gate of the MOSFET through a resistor. Multiple variants of this driving technique exist. The driving could be made asymmetrical by using diodes or the driving speed could be increased by using capacitors. But the principle stays the same. The gate-source capacitance is charged through a resistor, which can create some problems. For example false turn-on, as described in section 2.1.3. Another disadvantage is that charging a capacitance with a voltage source through a resistor has a maximum theoretical efficiency of 50%, and in the end all energy put in the gate-source capacitance will be lost in the gate resistor while discharging the capacitance.

Resonant gate driving Resonant gate drivers use an inductor to drive the gate of a MOSFET. The inductor is used to create a current source. Charging or discharging a capacitance with a current source doesn't create losses. There are multiple circuits that are able to charge the inductor, for example a half bridge and a full bridge. In both circuits the bridge transistors can be used to clamp the gate voltage to the steady-state value with low impedance. This avoids false turn-on. The disadvantage of this way of gate driving is the fast signals needed to control the (dis)charging of the inductor. These signals need to be generated from a relatively big analog circuit or from a very fast digital circuit.

Proprietary driving circuit Strukton Rolling Stock developed several driving circuits which are based on the same idea. The idea is to drive the gate with a constant current. These circuits also include parts which can limit the $\frac{dv}{dt}$ and the $\frac{di}{dt}$. Driving a gate with a constant current is ideally lossless, but this constant current is created by using bipolar transistors in their active region, thus using them as controlled resistors. The feedback which creates the constant current works fine for IGBTs with a high gate-source capacitance, but simulations show that the reaction time of the feedback is not short enough to create a constant current. Before the feedback network can settle to a certain current value, the gate capacitance of the MOSFET is already charged. So for MOSFETs with a low gate-source capacitance this circuit doesn't have advantages over resistive gate driving and will increase the circuit complexity.

Decision & design Although resonant gate driving is theoretically the best way of driving a MOSFET, the practical implementation will increase design complexity a lot. The current source driver developed by Strukton Rolling Stock is useless for fast switching MOSFETs, so the MOSFETs will be driven by a resistive gate driver.

The value of the gate resistance is determined by several design constraints. These are:

1. No gate voltage oscillations. According to the SPICE model of the C2M0080120D, the sum of the inductances of the gate and source pins is 24nH. It is assumed that this inductance is for the full length pins, since much bigger IGBT modules, such as the SEMIKRON SEMiX353GB176HDs, with bigger current loops, have an $L_{CE} \approx 20\text{nH}$. It is therefore assumed that the real inductance is lower than the specified inductance. The total inductance in the driving path is estimated at 30nH. With $C_{iss} = 950\text{pF}$, the minimum gate resistance will be $R_G \geq 2\sqrt{\frac{L}{C}} = 11.2\Omega$.
2. The peak current should not be too high. The chosen gate driver has a peak current capability of 5A[35]. So the minimum gate resistance with a driving voltage of 20V (recommended by the datasheet[9]) will be 4.4Ω .
3. The switching losses of the MOSFETs should not get higher than 12.9W, as calculated in section 3.2.3. Simulations show that the gate resistor is limited to 19Ω .

Since the internal gate resistance of the C2M0080120D is 2.5Ω , the gate resistor will need to have a minimum value of 8.7Ω . When practical problems, such as EMI due to too fast switching, occur, the gate resistance could be increased to $19\Omega - 2.5\Omega = 16.5\Omega$ when necessary. The off-voltage is 0V and the on-voltage is 20V.

3.2.7 Evaluation by simulation

The converter as shown in figure 3.3 is put into LTspice to simulate the behaviour of the converter. The input voltage is 750V, so the duty cycle has to be $d = 50\%$. The 30nH represents the inductance of the wires from the voltage source to the module. The dead time for the switches is set to 100ns.

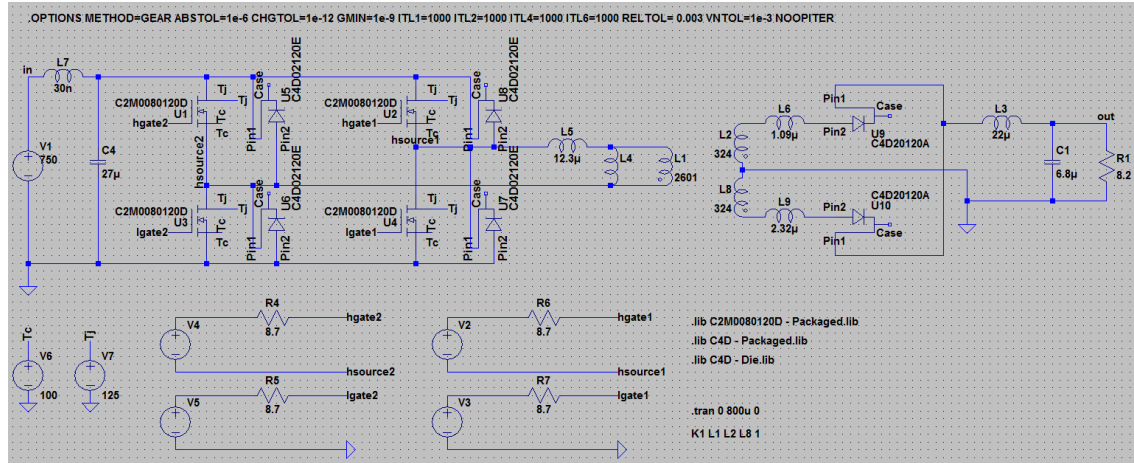


Figure 3.3: LTspice simulation circuit

Results

Some waveforms are shown in figure 3.4. In this figure, the light green curve is the voltage across the lower MOSFET of the left phase leg, the blue curve is the output voltage, the red curve is the voltage across the upper rectifying diode, the light blue curve is the current through the lower MOSFET of the left phase leg, the pink curve is the output inductor current and the grey curve is the current through the upper rectifying diode.

This simulation had some interesting results:

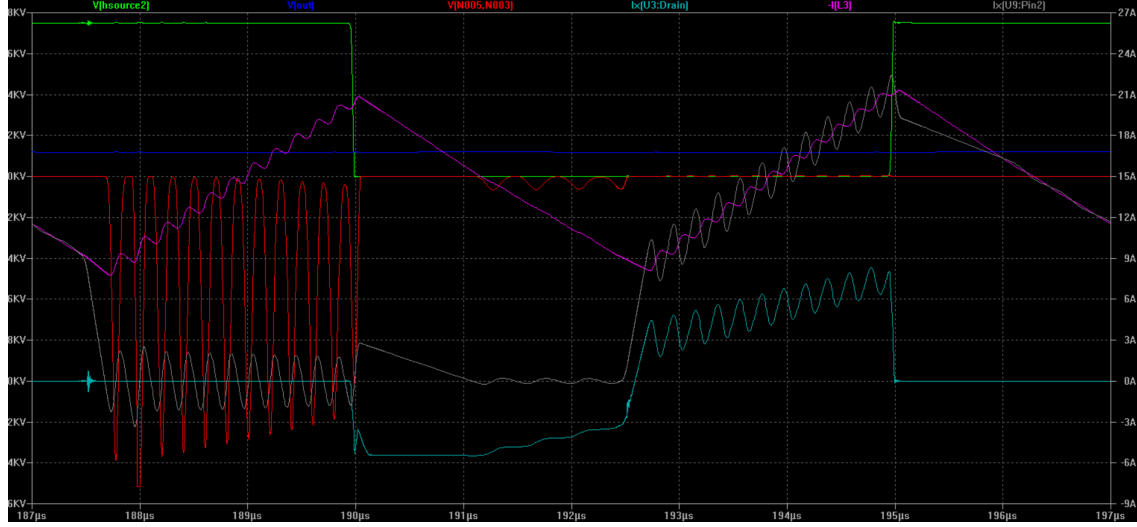


Figure 3.4: Simulation results

- The output voltage is much lower than 140V. This is primarily due to the voltage drop across the leakage inductances.
- The output voltage equals $V_{out} = 118V$, so $I_{out} = 14.5A$ and $P_{out} = 1.71kW$.
- The voltage across the diodes are oscillating during the off-period of the diodes. This causes oscillations in all current waveforms, except for the output current.
- The power dissipated by the MOSFETs in steady state differs per MOSFET, but is lower than 4.6W for all MOSFETs.
- ZVS is achieved in this simulation.
- Due to the oscillations, the losses in the diode are 15.6W per diode. This limits the output power.
- The losses in the magnetic core are 3W.
- The input power is 1.77kW, so the efficiency is 96.6%.

3.2.8 Iteration

As mentioned in the previous section, there are some problems with the first design of the converter that have to be solved before the circuit could be converted to an actual PCB layout.

Low output voltage

The first problem, the lower than expected output voltage, is mainly caused by the leakage inductances of the transformer. In the real converter, this problem is solved by the control system.

Diode oscillations

The oscillations on the secondary side are caused by the model of the actually used diodes, because the standard LTspice diode model didn't show oscillations. But the standard diode model has no junction capacitance and has no parasitic inductance.

The oscillations could be prevented by using a snubber. First a lossless capacitive snubber was tried, but this snubber distorts the inductor voltage too much, so a lossy RC snubber is tried. To

calculate the values for the resistor and the capacitor, the circuit is studied as a damped RLC circuit.

The solution of a damped RLC circuit is in equation (3.11). In this solution, the damping ratio ζ is given by equation (3.12) and the natural resonance frequency ω_0 is given by equation (3.13). The damped resonance frequency ω_d is given by equation (3.15). The time constant τ of this damped oscillation is in equation (3.14). The oscillation is considered fully damped out at $t = 5\tau$. In these equations, ϕ is the phase shift in the sinusoidal waveform, R is the damping resistance, L the inductance and C the capacitance.

$$v(t) = Ce^{-\zeta\omega_0 t} \sin(\omega_d t + \phi) \quad (3.11)$$

$$\zeta = \frac{R}{2} \sqrt{\frac{C}{L}} \quad (3.12)$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (3.13)$$

$$\tau = \frac{1}{\zeta\omega_0} \quad (3.14)$$

$$\omega_d = \omega_0 \sqrt{1 - \zeta^2} \quad (3.15)$$

The oscillation should be damped within 100ns to keep the influence on the duty cycle small, so $\tau \leq 20\text{ns}$. As the oscillation has a frequency of 5.06MHz and is almost undamped, $\omega_0 \approx \omega_d = 2\pi \cdot 5.06\text{MHz} = 31.8\text{Mrad/s}$. This means that to create $\tau \leq 20\text{ns}$, ζ has to be $\zeta \geq 1.57$. The oscillation is caused by the junction capacitance of the diode and the leakage inductance of the transformer. For the upper rectifier leg, $L_\sigma = 1.09\mu\text{H}$ and the pin inductances of the diodes are 6.5nH, so the total inductance is $L = 1.22\mu\text{H}$. This means that the junction capacitance C_j should be equal to $C_j = 811\text{pF}$.

With these values and equation (3.12), the desired resistance of the snubber could be calculated. The snubber resistance should be at least $R_{\text{snubber}} \geq 2\zeta \sqrt{\frac{L}{C}} = 120\Omega$.

To calculate the value of the capacitance in the RC snubber, the impedance of the RC snubber is derived and is in equation (3.16). This impedance has one pole at $\omega_P = 0\text{rad/s}$ and one zero at $\omega_Z = \frac{1}{RC}$. The zero is chosen at about half the resonance frequency, so $\omega_Z = 2\pi \cdot 2.5\text{MHz}$. With $R = 120\Omega$, $C = \frac{1}{\omega_Z R} = 531\text{pF}$.

$$Z_{RC}(\omega) = \frac{j\omega RC + 1}{j\omega C} \quad (3.16)$$

Iteration results

In the simulation, a 120Ω resistor and a 560pF capacitor were used for both rectifying diodes. The results are shown in figure 3.5. The colors of the curves have the same meaning as in figure 3.4. The losses are 10.7W for the diode and 13.8W for the snubber resistor. The output voltage is still 118V. The input power is 1.8kW and the output power is 1.71kW, so the efficiency is reduced to 95%.

3.2.9 Practical implementation

To implement this the simulated circuit, some practical aspects have to be considered. These are described in this section.

Processing unit

The module should be controlled by an FPGA. An FPGA has a limited speed, but can do many calculations in parallel, which makes it suitable for controlling the converter. Other options, such as a microcontroller (AVR/PIC/etc) or a microprocessor (ARM/x86) are too slow or too complex

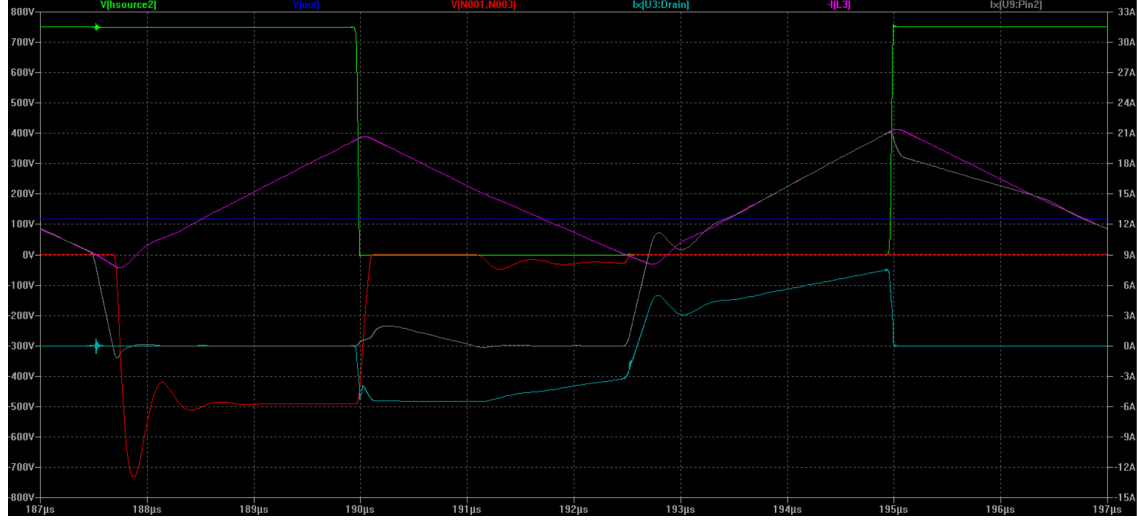


Figure 3.5: Simulation results with RC snubber across the diode

and are therefore not used. For practical reasons, the FPGA is not integrated on the PCB, but an evaluation board is connected to the PCB.

Thermal management

As already mentioned in this chapter, the components are cooled by heatsinks. This creates a problem. The heatsinks need to be grounded, as experience has shown that heatsinks at high voltage will create breakdowns. This is because particles in the air are attracted by the high potential. These particles create a sharp point with an increased electrical field, attracting more particles. Finally, the particles form a more or less conducting path from the high potential heatsink to the grounded enclosure, creating an earth fault.

Heatsinks at high potential should therefore be avoided. The heatsinks will be grounded. But the metal area of the MOSFETs which is in contact with the heatsink is connected to the drain, which will be on some point of time at high voltage, creating a short circuit. To overcome this problem, a thermally conducting but electrically insulating pad has to be placed between the MOSFET and the heatsink. This pad should have an insulation voltage $\geq 10\text{kV}$ and the thermal resistance should be as low as possible.

Intra-module communication

Within a module, some parts have to communicate with each other. These parts are on both the primary side and parts on the secondary side of the transformer. The primary part could be at high potential, while the secondary part is always grounded. The parts on the primary and the secondary need to communicate with each other. This is not possible without galvanic isolation. Galvanic isolation could be achieved by multiple methods. Some of these methods are transformers, optocouplers and optical fibers. Because of the wish for high insulation voltage ($\geq 10\text{kV}$), optocouplers are not suitable, as their insulation voltage is generally limited to a few kV. Transformers could be used, but these transformers need to transfer digital signals very accurate and also need to have a high insulation voltage. The last option is using optical fibers. Because of the length of these fibers, the insulation voltage could be very high. And because these fibers are flexible, the PCB design is less restricted by the communication. The last advantage of fibers is that they are not susceptible to and do not produce EMI. The communication within a module will thus be done with optical fibers.

In order to ease inter-module communications and reduce the number of optical fibers needed, the control system is connected to the secondary side of the module.

Inter-module communication

As will be shown in section 3.3, the individual modules need to communicate with each other to share the output currents and input voltages. Since the control system is connected to the secondary part of the modules, communication doesn't need galvanic isolation. Because a robust communication protocol is needed, communication will be done over a CAN bus.

Auxiliary power supply

The control system, communication systems, drivers, etc have to be powered. In the ideal situation, this power is drawn from the input voltage. But the input voltage can be as high as 1000V. It is difficult to create a self-starting step-down converter for this voltage levels. There are self-starting step-down converters with $V_{in} \leq 900V$, which is still not suitable for converters with a maximum input voltage of 1000V. Therefore, an additional lab power supply is used to create the voltages for the auxiliary power.

A 20V power supply is connected to the primary part of the module. In this way, the lower MOSFETs could be driven directly from this power source without conversion steps. The power for the upper MOSFETs, the input measurement circuit and the control system on the secondary side of the module is transferred through a transformer. This transformer is driven by a small full-bridge converter, which operates at 10kHz. A capacitor is connected in series with the transformer to avoid saturation. This transformer has 5 windings: one primary winding ($N = 20$), two windings for the drivers of the high side MOSFETs ($N = 20$), one winding for the input voltage measurement circuit ($N = 7$) and one winding for the secondary circuit ($N = 10$). The input voltage measurement circuit and the secondary circuit both run at 5V. The higher number of turns for the secondary circuit is needed to compensate for the voltage drop caused by the higher current.

The power for the control circuit is converted from the rectified transformer output voltage to 5V by an off-the-shelf buck converter. The 5V for the input voltage measurement circuit and the measurement circuits at the secondary side are made with a voltage reference. The 5V for the optic fibers is made with a linear voltage regulator.

PCB layout

Because the converter works at a high switching frequency and with high values for $\frac{dv}{dt}$ and $\frac{di}{dt}$, special attention needs to be paid to the PCB layout. Commutation loops need to be kept as small as possible to reduce the parasitic leakage inductance and reduce the emitted magnetic field. Traces with a high $\frac{dv}{dt}$ need to be as small as possible, to reduce the parasitic capacitance to other traces.

3.2.10 Hardware overview

The complete overview of the module is shown in figures 3.6 and 3.7. Figure 3.6 shows an overview of the signal paths within one module. A dashed line in this figure means that a signal is transmitted over an optical fiber. Figure 3.7 shows an overview of the power flow within one module.

The schematics, PCB layout and pictures of the assembled PCB are shown in appendix A.

3.3 Control system

The main goal of a control system for a power supply is to keep its output voltage constant. But input voltage and output current can (and will) change over time. Both quantities affect the output voltage. When using the most basic control scheme, constant frequency constant duty cycle control, the converter behaves as a simple transformer, so the output voltage is directly

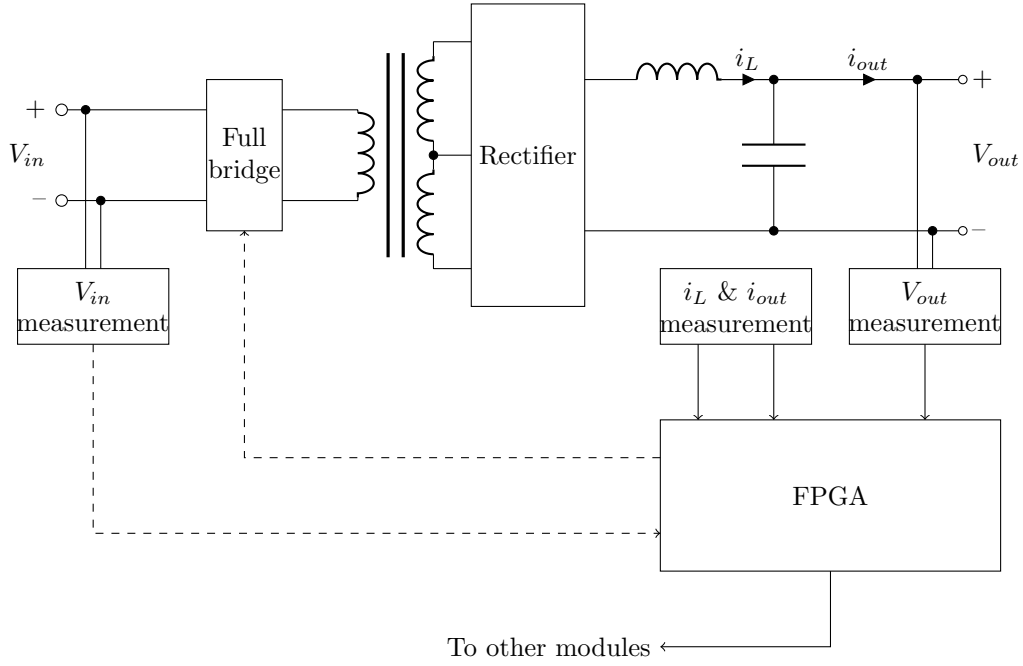


Figure 3.6: Signal flow within one module

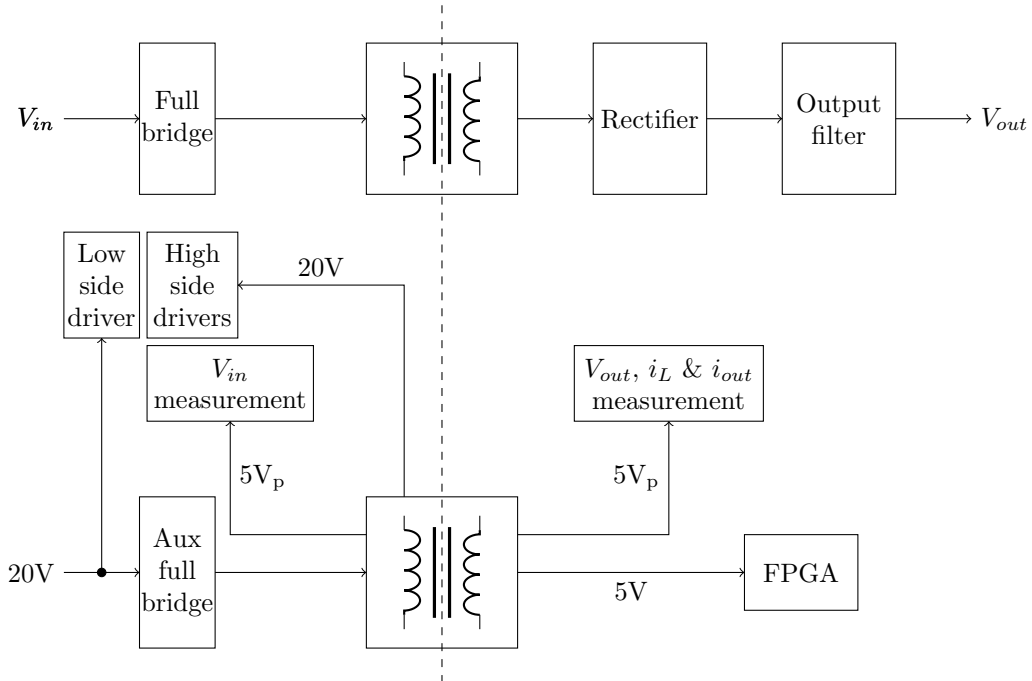


Figure 3.7: Power flow within one module

proportional to the input voltage. The output voltage should be constant with a varying input voltage. Keeping the output voltage constant with a varying input voltage is called line regulation.

When using the simple constant duty cycle control and having a low load current, the operating mode of the converter will change from continuous conduction mode to discontinuous conduction mode. The relation between the input voltage and the output voltage for a converter in discontin-

uous conduction mode is complex. The output voltage is related to d^2 , V_{in} and I_{out} . The output voltage shouldn't depend on the load current. Keeping the output voltage constant with a varying load current is called load regulation.

Modular converters don't only require line and load regulation, but also input voltage sharing and output current sharing. This means that the input power or the output power should be controlled.

One single module should be able to operate without other modules. This is achieved by splitting the control system in two parts: a global control system and a local control system. Each module contains both control systems, which means that the global control system is distributed. The local control system is the part that regulates the output current and output voltage, while the global control system regulates the output current sharing and input voltage sharing. The global control calculates the output current value for the local control system to achieve input voltage sharing and output current sharing.

3.3.1 Local control system

A lot of control schemes for switched mode power supplies have been developed during their existence. For simplicity, only a few of them are covered in this thesis. They are compared on their ability to control the input current, the output voltage and the output current and on the ease of implementation.

Voltage mode control

Voltage mode control is next to constant frequency constant duty cycle control the most simple form of control. It basically consists of a constant frequency sawtooth generator, a control voltage and a comparator. The control voltage is a constant voltage, while the amplitude and the ramp of the sawtooth are directly proportional to the input voltage. When the sawtooth is below the control voltage, the switch is turned on, and when the sawtooth increases to values above the control voltage, the switch is turned off. In this way input voltage feed-forward is created, so line regulation is accomplished. An overview of this principle is shown in figure 3.8.

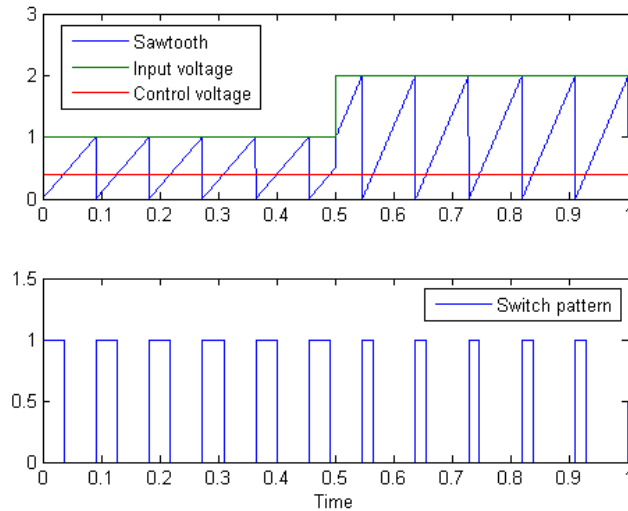


Figure 3.8: Basic waveforms of voltage mode control

Voltage mode control is basically designed to control the output voltage. This means that there is no control on the output current. Although this is not a problem for free-standing converters,

this makes it impossible to achieve output current sharing in a modular converter. For this reason, all forms of voltage mode control are useless for a modular converter.

Current mode control

Current mode control is basically voltage mode control with an additional inner loop to control the output current. In this way, one pole is removed from the transfer function[34], so its response to transients is better than the response of a converter controlled by voltage mode control. Another advantage of this control scheme is that the output current is directly controlled, which makes it possible to achieve output current sharing. This makes current mode control suitable for modular converters.

The most basic current mode control scheme consists of a latch, a clock source, a comparator and an error amplifier. The clock source sets the latch and turns the switch on. The latch is reset by the signal from the comparator. The comparator compares the inductor current level with a signal from the error amplifier. The signal from the error amplifier represents the peak inductor current at which the switch has to be turned off. This is the basic operation of current mode control.

This basic operation scheme has three problems. The first problem is that the switch is always turned on when the clock source triggers, even when the load current is very low. When there is no load, the switch is turned on, the inductor current rises and charges the output capacitor. Because the current in the inductor is then higher than the load current (which is 0A), the switch is turned off very fast. But for a very small time, the switch was on and the inductor was charged a bit. This current is then transferred to the output capacitor, raising the output voltage. The next switching period, this cycle repeats itself. This results in an ever increasing output voltage, because the capacitor is not discharged. In the end, this leads to the failure of the capacitor. To avoid this, the turn-on of the switch is prevented by an overvoltage protection. It compares the output voltage with the reference voltage. When the output voltage is greater than the reference voltage, the turn-on of the switch is prevented. This leads to pulse skipping.

The second problem is that the basic scheme is not short circuit proof. When the load current increases or when there is a short circuit, the output voltage drops. The basic control scheme tries to compensate for this by increasing the current. In this way, the current rises to dangerous levels which will destroy the converter. This problem is solved by applying an overcurrent protection. The overcurrent protection turns the switch off and prevents turn-on when the inductor current reaches a certain level. In this way, transformer and inductor saturation and overtemperatures are avoided. It also creates a soft start, since the inrush current is limited.

The last problem is that the controller gets unstable when $d > 50\%$. This phenomenon is called subharmonic oscillation. It could be solved by adding slope compensation[34, 25]. When no slope compensation is applied, the inductor current oscillates with a frequency lower than f_{SW} around the output current. This oscillation is undamped. When slope compensation is added, this oscillation is damped in a few switching cycles. This is illustrated in figure 3.9. Slope compensation is explained in appendix B.

The implementation of these solutions is shown in figure 3.10.

Simulation results for the local control system

From the reviewed control schemes, the current mode control scheme is the only suitable control scheme. Therefore, it is implemented in a simulation to verify its behaviour. This simulation makes use of ideal components. To make this control usable for the full bridge topology, a volt-second limit is introduced. This limit prevents saturation of the transformer. When the volt-second limit is reached, the polarity of the voltage applied to the transformer is reversed. In this way, overexcitation and thus saturation of the transformer is avoided.

The simulation parameters were as follows: $f_{SW} = 100\text{kHz}$, $L = 22\mu\text{H}$, $C = 6.8\mu\text{F}$, $V_{in} = 1\text{kV}$, $V_{out,set} = 140\text{V}$, $R_L = 9.3\Omega$, $I_{OCP} = 26\text{A}$, $t_{dead} = 100\text{ns}$, volt-second product limited to 279mT and a sample frequency of 1MHz .

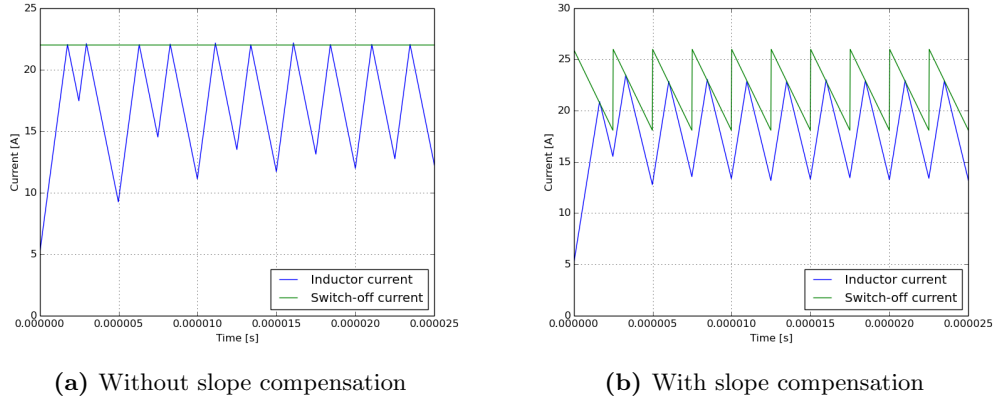


Figure 3.9: Effect of slope compensation

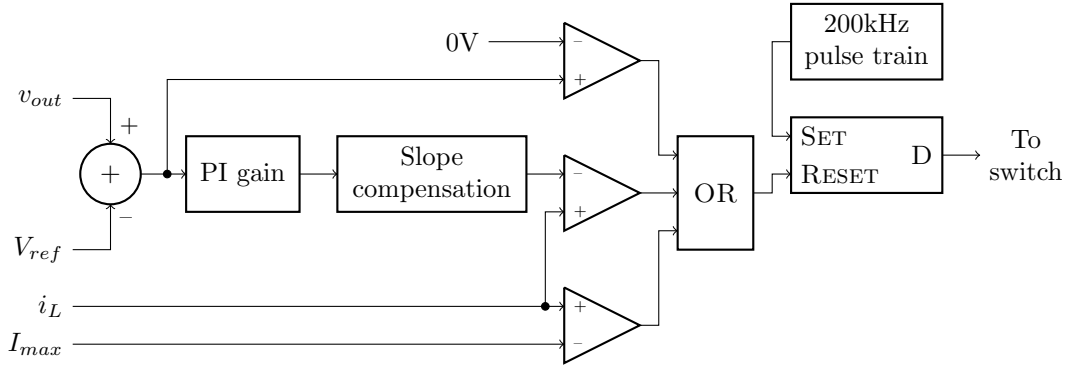


Figure 3.10: Current mode control with OVP, OCP and slope compensation

During the first simulations (with the volt-second limit turned off), it was observed that the OVP caused instability on the output voltage. This is shown in figure 3.11. This oscillation is caused by the fact that the converter turns off the switches when the desired output voltage is reached. Then it takes some time for the output voltage to decrease to the desired output voltage. During this time, the inductor current decreases to zero. At the moment the output voltage is decreased to the desired voltage, the load is fully supplied by the capacitor, which thus discharges even faster. During this fast discharge, the inductor current increases back to the output current level. When this current level is reached, the capacitor could be charged back to the desired output voltage.

The voltage drop depends on the moment at which overvoltage is detected. When an overvoltage is detected just after the switch is turned on, the inductor current will decrease a lot, because it has almost the full $\frac{1}{2}T_{SW}$ to decrease. But when overvoltage is detected just before the end of $\frac{1}{2}T_{SW}$, only a small oscillation is seen. The first scenerio can be seen at $t \approx 0.0002s$, while the second scenario can be seen at $t \approx 0.00027s$.

To avoid this problem, the original OVP rule ($v_C > V_{ref}$) is replaced by a more tolerant rule with hysteresis. Normal OVP also trips due to the normal ripple on the output voltage. To avoid this, the OVP level is set above the normal ripple. In the simulations, the new OVP level is set to 142V. When the OVP level is reached, the OVP stays on until the output voltage is lower than 140V. The result of this OVP scheme is shown in figure 3.12.

This scheme is tested with two scenarios. In the first scenario, the load is constant at full load and the input voltages are changed. First from full input voltage (1kV) to the minimum input voltage (500V) at $t = 0.0004s$ and then to nominal input voltage (750V) at $t = 0.001s$. The results of this simulation is shown in figure 3.13. With a lower input voltage, the current ripple is

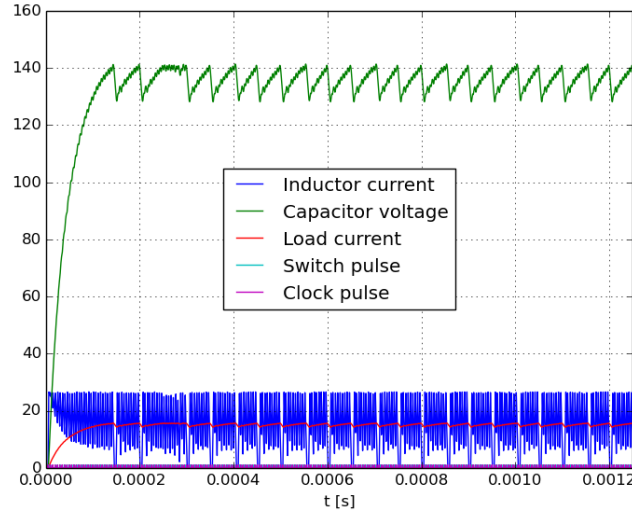


Figure 3.11: Unstable output voltage of a module due to OVP (without volt-second limit)

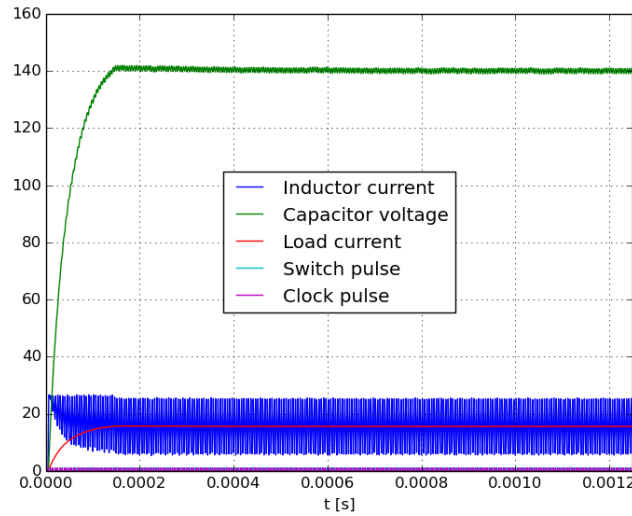


Figure 3.12: Output voltage with hysteresis in the OVP (without volt-second limit)

smaller, which is a result of equation (3.8) and slope compensation. With a lower input voltage, it takes more time to reach the desired peak inductor current level. During this time the slope compensation reduces the desired current level. The result is that these current levels intersect at a lower level and thus causing a lower current ripple. At $t = 0.0004\text{s}$, the minimum output voltage is 137V. The maximum output voltage is 142V. The “noisy” waveforms are a result of the volt-second limiter.

In the second scenario, the input voltage is kept at 1kV, but the load current changes. First, the load current equals 15A ($R_L = 9.3\Omega$). At $t = 0.0004\text{s}$, the load changes to $R_L = 1400\Omega$, creating a load current of 100mA. At $t = 0.001\text{s}$, the load is changed to $R_L = 2.7\Omega$. The result is shown in figure 3.14. From $t = 0.0004\text{s}$ to $t = 0.001\text{s}$, the output voltage is oscillating at a low frequency. This is because of the OVP. The output capacitor is charged to a voltage above 142V. Then the OVP turns on, turning the switch off. When the output voltage is below 140V, the switch

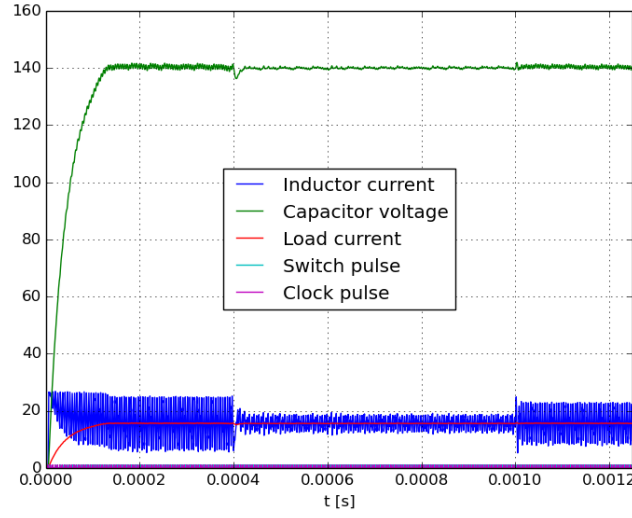


Figure 3.13: Simulation with changing input voltage

is turned on, charging the capacitor to a value above 142V. This cycle causes the oscillation and its frequency is dependent on the load, since the discharge of the output capacitor is simply an RC-network. At $t = 0.001s$, the output with $V_{out} = 140V$ is higher than the maximum current. The converter starts to behave as a current source and the output voltage drops to $V_{out} = R_L I_{max}$.

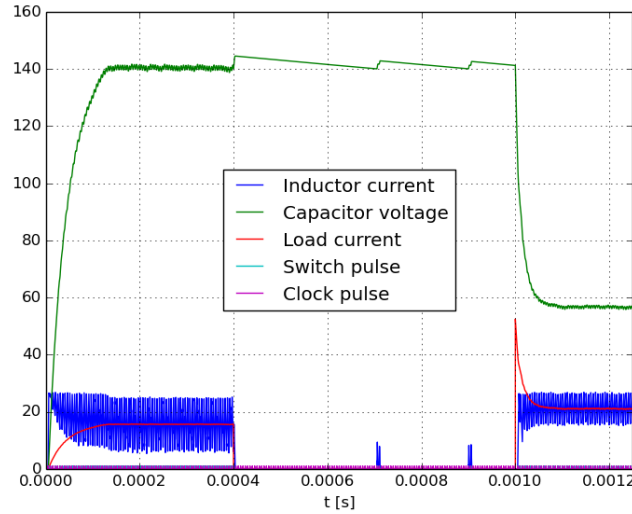


Figure 3.14: Simulation with changing output load

3.3.2 Global control system

Because multiple converters have to cooperate with each other, some additional control is needed. To achieve a stable input-series output-parallel connected converter, the input voltage and output current have to be controlled. In the ideal case, only the output current has to be controlled to achieve output current sharing (OCS) and input voltage sharing (IVS). This is achieved when all

modules are perfectly equal. But every component has some production tolerance and modules could be susceptible to EMI or other disturbances. For example, when one of the input capacitors has a lower capacitance than the others, the voltage across this capacitor will be higher than the voltages across the other capacitors. When the converters are equally loaded, this leads to instability.

To prove this, this situation is simulated. When OCS is achieved, the modules behave as a constant power load, since the output voltage and output current are constant and thus the output power is constant. This means that when the input voltage is decreased, the input current is increased. These constant power loads are placed in parallel with a capacitor. Multiple of these capacitor-load combinations are connected in series and a voltage is applied to this circuit. The circuit is shown in figure 3.15.

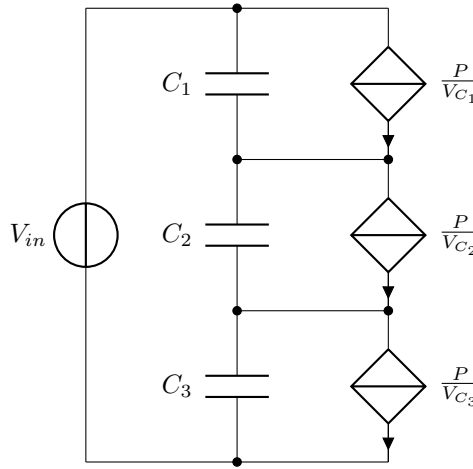


Figure 3.15: Circuit used to simulate input voltage sharing

The result of this simulation is shown in figure 3.16. This figure shows huge voltage steps, which will not occur in reality. These voltage steps result from the fact that there was no inductance and resistance present in the circuit, allowing for huge currents to (dis)charge the capacitors.

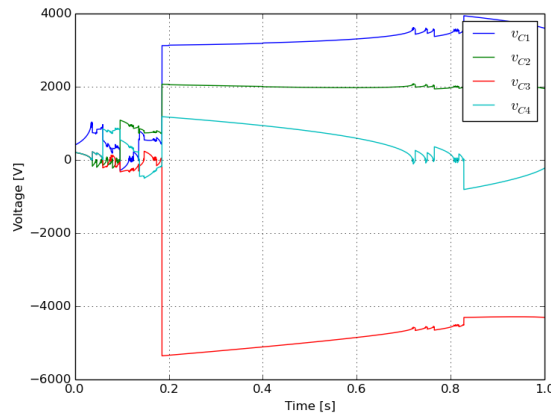


Figure 3.16: Simulation result of 4 modules with one input capacitance lower than the others

Output current sharing

Output current sharing is easily achieved. In the current mode control scheme, the output current is sensed. When all modules sense their output current and share them on a communication bus, the desired output current per module is calculated as the average of these currents. This current is then put into the local control system, which controls the inductor current. In this way, OCS is achieved.

Input voltage sharing

Input voltage sharing is more difficult to achieve, since there is no direct control over the capacitor voltage. The capacitor voltage could be regulated by regulating the input current. By increasing the input current, the capacitor is discharged and the input voltage is decreased.

The control is done by adding a correction term to the input current. This term is dependent on the error between the actual capacitor voltage and the desired capacitor voltage. The set value for the current of one module (module i) is given in equation (3.17). In this equation, $I_{out,i}$ is the set value for the average output current of module i , N is the number of modules, $I_{out,j}$ is the output current of module j , $V_{in,j}$ is the input voltage for module j and K is a scaling factor. This scaling factor is used to limit the increase in output current. This is needed because of the current limit of the local control system, which would introduce nonlinearities in the IVS control system. The result of this equation is that when the input voltage is higher than the desired value, the input current is increased, so the capacitor is discharged, the other capacitors are charged and input voltage sharing is achieved.

$$\begin{aligned} I_{out,i} &= \max(\bar{I}_{out} + K(V_{in,i} - \bar{V}_{in}), 0) \\ &= \max\left(\frac{1}{N} \sum_{j=1}^N I_{out,j} + K\left(V_{in,i} - \frac{1}{N} \sum_{j=1}^N V_{in,j}\right), 0\right) \end{aligned} \quad (3.17)$$

The result of the simulation with this control scheme enabled is shown in figure 3.17 (with $V_{in} = 1\text{kV}$ and $K = \frac{1}{64}$). In this simulation, there are four modules. The upper module has an input capacitor of $50\mu\text{F}$, the others have an input capacitor of $100\mu\text{F}$. The results show that the initial difference in capacitor voltage goes to zero. At $t = 0.2\text{s}$ and $t = 0.4\text{s}$, the voltage of the upper capacitor is increased by 10V , while the voltage on the second capacitor is decreased by 10V . Also this voltage difference disappears with time. Figure 3.16 shows exactly the same simulation, but with the control scheme in (3.17) turned off.

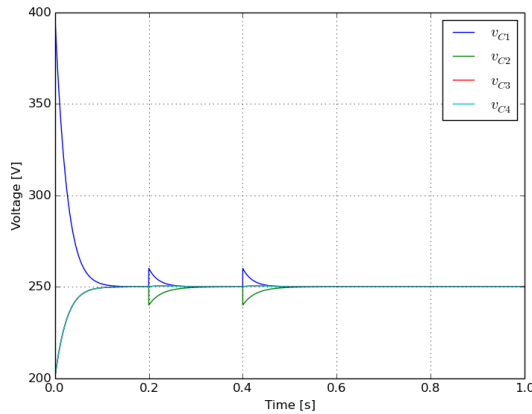


Figure 3.17: Simulation result of the control scheme for input voltage sharing

3.3.3 Overview of full control system

A full overview of the control system for module j is shown in figure 3.18. The block “Local control” is shown in figure 3.19. The block “Global control” is shown in figure 3.20.

The block “Local control” is fed with the actual output voltage and the desired output voltage. A controller with a PI gain generates a desired average inductor current level. The sign of the output of this gain (i_e) is also used to trigger the overvoltage protection. The peak value at which the switch should be opened (\hat{i}) generated from the average current by the slope compensation system.

The block “Global control” adds a term to the desired peak inductor current. The input for this block are all input voltages and output currents. With these inputs, the average input voltage and output current values are calculated. These values are the desired values. The correction term calculated by the global control $\Delta i_{out,j}$ is added to the desired peak inductor current to regulate the input voltages and output currents to the desired values.

The sum of the output signals of the “Local control” block and the “Global control” block is compared against the inductor current level. The i_e signal is compared against zero to check whether this signal is positive or negative. The actual inductor current is also compared against a maximum value to achieve overcurrent protection. When one of these comparisons give a logical one at the output, the reset signal becomes one and the SR-latch is not set. This means that there will be no voltage across the primary side of the transformer. The SR-latch is set by a 200kHz clock. The output of the SR-latch is connected to a volt second limiter, which limits the volt second product applied to the transformer. This avoids saturation.

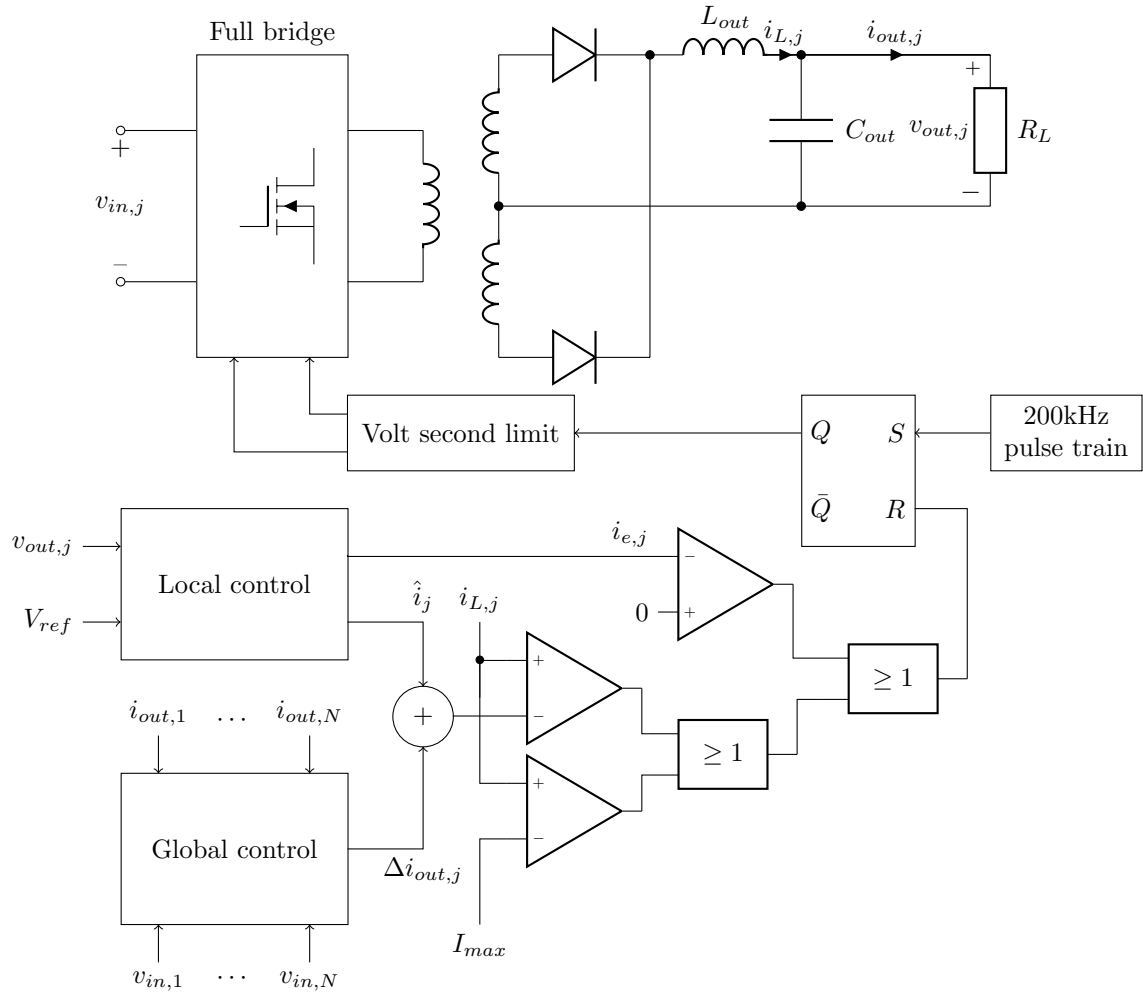


Figure 3.18: Overview of the control system

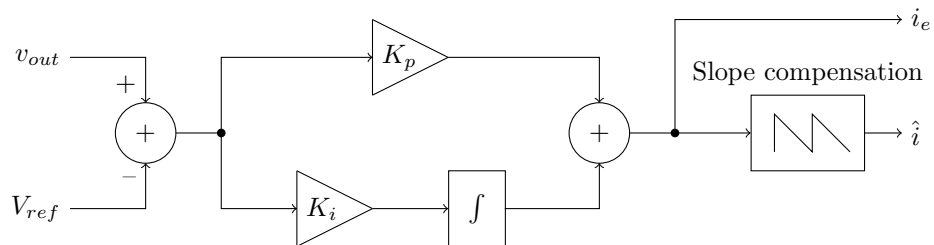


Figure 3.19: The “Local control” block

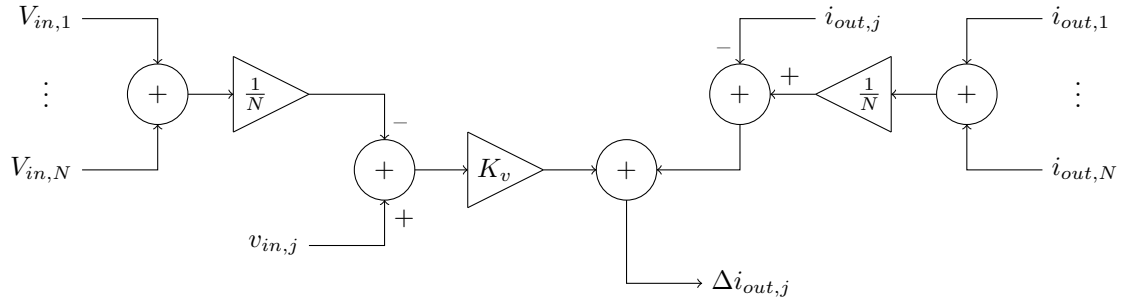


Figure 3.20: The “Global control” block

Chapter 4

Design evaluation & performance

This chapter describes the the design evaluation of the converter. This contains the test plan for the modules and the results of those tests. As a result of time constraints and difficulties during testing, only a single module is tested with constant frequency and constant duty cycle control. The tests that need to be carried out to complete the work on the modular converter are described in this chapter.

4.1 Design evaluation of a single module

4.1.1 Switch tests

To verify the used models, the MOSFETs are tested with a single pulse test. This test is often used to determine switching losses. The circuit for this test is shown in figure 4.1. The waveform that will be used to control the MOSFETs is shown in figure 4.2. At the first switching moment (at $t = 10\mu\text{s}$), the MOSFET turns on with zero current. At the second switching moment (at $t = 40\mu\text{s}$), the MOSFET turns off with a certain current. Between $t = 40\mu\text{s}$ and $t = 44\mu\text{s}$, the inductor current flows through the upper diode or the upper MOSFET and doesn't decrease significantly. Then, at $t = 44\mu\text{s}$, the MOSFET turns on with the same current as at $t = 40\mu\text{s}$. At $t = 48\mu\text{s}$, the MOSFET turns off. The inductor current then commutates to the upper diode or upper MOSFET and will decrease slowly due to the conduction losses.

This test is performed in two ways. The first way is a test using only the bottom MOSFET, while leaving the other MOSFET open. The second way is using both MOSFETs. During these tests, the waveforms are captured and compared to the simulated waveforms. In all test, the drain voltage of the lower MOSFET, the gate voltages of the lower MOSFET, the current through the lower MOSFET and the inductor current were measured.

Due to practical limitations, the maximum voltage that could be applied to the converter is 720V. Insulation tests showed that the converter could withstand at least 1.5kV AC for 30s.

Single pulse test with a single MOSFET

With the single pulse test on a single MOSFET, the signal in figure 4.2 is applied to the lower MOSFET (in figure 4.1, with gate G_2), while the upper MOSFET (G_1) is off.

Test procedure This test is done with a hand-wound inductor: a coil is wound around a toroidal core of which the magnetic properties were not known. The test started at a $V_{in} = 20\text{V}$. The input voltage was increased by 5V-steps. When the inductor started to saturate, more windings were added to reduce the flux density. This cycle was repeated until the maximum input voltage was reached.

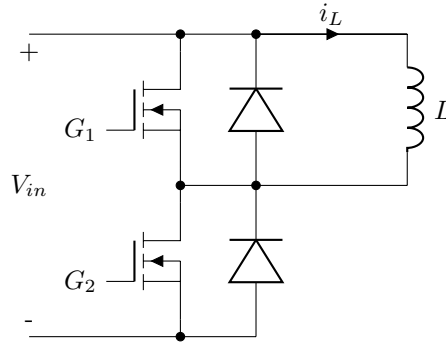


Figure 4.1: Circuit used for the single pulse test

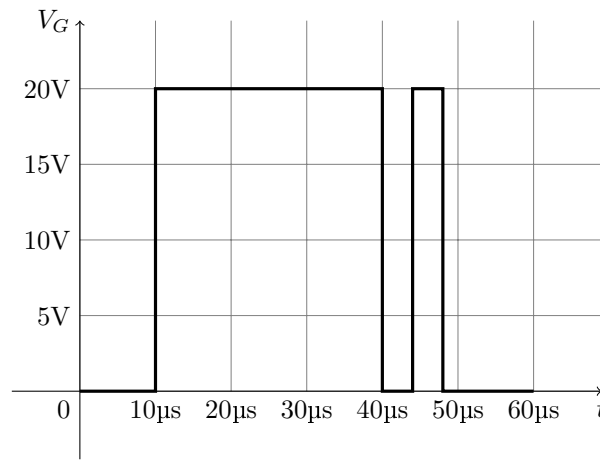
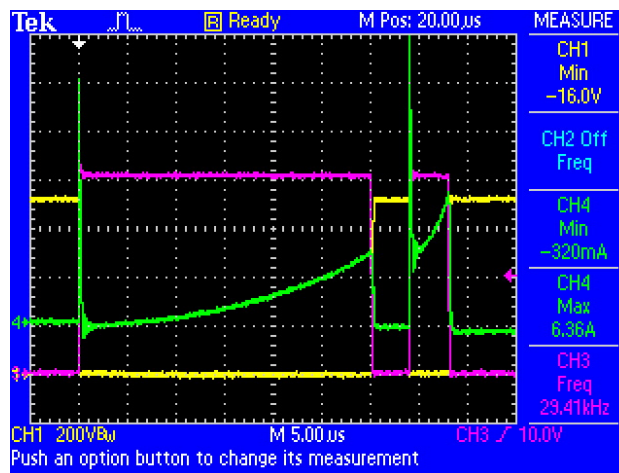


Figure 4.2: Bottom MOSFET gate voltage waveform of the single pulse test

Results In figure 4.3, an overview of the measured waveforms is shown. This waveform shows the drain voltage of the lower MOSFET (yellow line), the gate voltage of the lower MOSFET (purple line) the current through the MOSFET (green line).


 Figure 4.3: Overview of the single pulse test waveforms with $V_{in} = 720V$ (yellow: drain voltage, purple: gate voltage, green: drain current)

In figure 4.4, the simulation result and measurement of the second turn-on are shown. In figure 4.5, the simulation result and the measurement of the first turn-off are shown. The test voltage was 720V. At both switching instances, the current through the inductor is approximately the same ($I_L \approx 1.5\text{A}$).

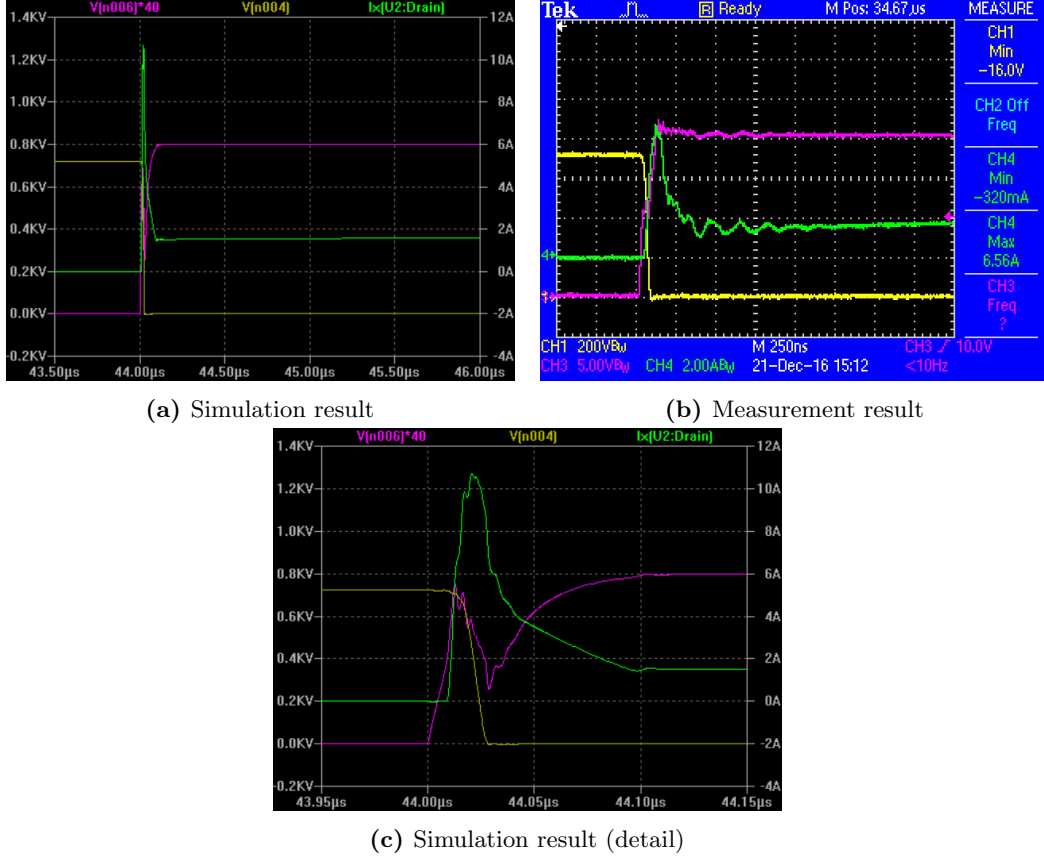


Figure 4.4: Comparison of waveforms at the second turn-on at $t = 44\mu\text{s}$ (yellow: drain voltage, purple: gate voltage, green: drain current)

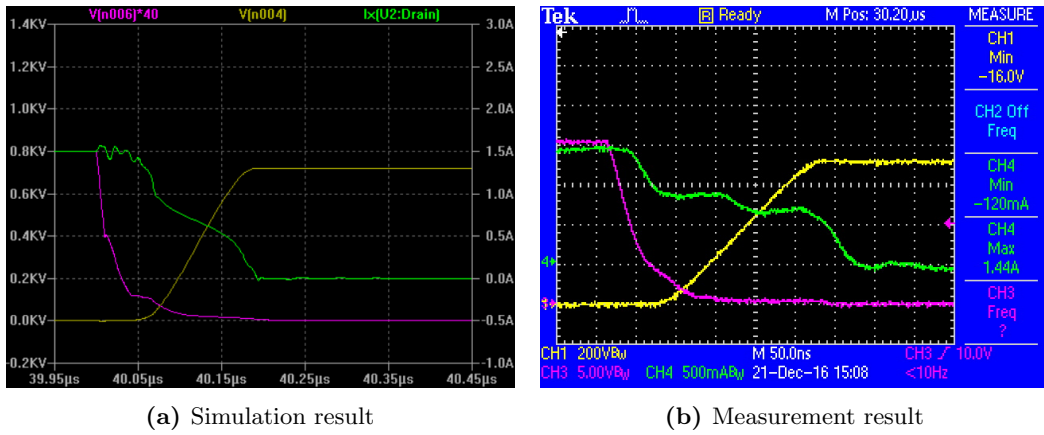


Figure 4.5: Comparison of the waveforms at the first turn-off at $t = 40\mu\text{s}$ (yellow: drain voltage, purple: gate voltage, green: drain current)

There are some differences between the simulations and the measured waveforms:

- The most notable difference is the switching time. In the simulation, the MOSFET switches much faster than in reality (20ns vs 50ns at turn-on, 100ns vs 200ns at turn-off). This higher $\frac{dv}{dt}$ also explains the higher peak in the drain current in the simulation. This current is a combination of the charging current of the drain-source capacitance of the upper MOSFET and the (dis)charging currents of the the junction capacitances of the body diodes and the antiparallel Schottky diodes.

The measured switching times differ from the measured ones due to parasitics that are not modelled in the simulation. When a parasitic inductance of 10nH is added in series with the MOSFETs, the turn-off switching time increases from 100ns to 150ns. On the other hand, the turn-on time doesn't change by adding parasitic inductances or parasitic capacitances, so the SPICE model of the switch also contains some faults.

- The gate voltage rises slower in the measurement and also shows some oscillation. This indicates that there is an underdamped LC oscillation, which is not modelled. The MOSFET current also shows an oscillation, which is not seen in the simulation. Similar oscillations in the gate voltage and drain current show up when an 300nH inductance is added between the input voltage source and the MOSFETs and an inductance of 10nH is added in series with the gate resistor.

However, the most remarkable observation is that the drain and gate waveforms are considerably different from the waveforms described by Mohan[34], in both the simulations and the real circuit.

During turn-off, the drain current reduces significantly during the drain voltage rise, something that is not to be expected from theory. This was solved by removing the top MOSFET from the simulation. This MOSFET, although constant off, caused these deformed current waveforms since it takes some of the inductor current during turn off to discharge C_{DS} .

During turn-on, the gate voltage rises very fast, almost to its steady state value. Then, as soon as the drain voltage starts to drop, the gate voltage also drops. This is caused by the voltage drop across the gate resistor, since the gate current increases very fast when the drain voltage drops. There is a small voltage drop present without the top MOSFET connected. This voltage drop is thus amplified by the top MOSFET. This voltage drop is not shown in figure 4.4b, but it is observed in other measurements.

During both turn-on and turn-off, there is no clear Miller platform visible in v_{GS} . Removing the top MOSFET creates a clearer Miller platform, although it still isn't like it should be. The waveforms of the "ideal" circuit (simulated with the built-in SPICE model of a STW11NM80[45]) and the circuit with the C2M0080120D are shown in figure 4.6a and 4.6b respectively.

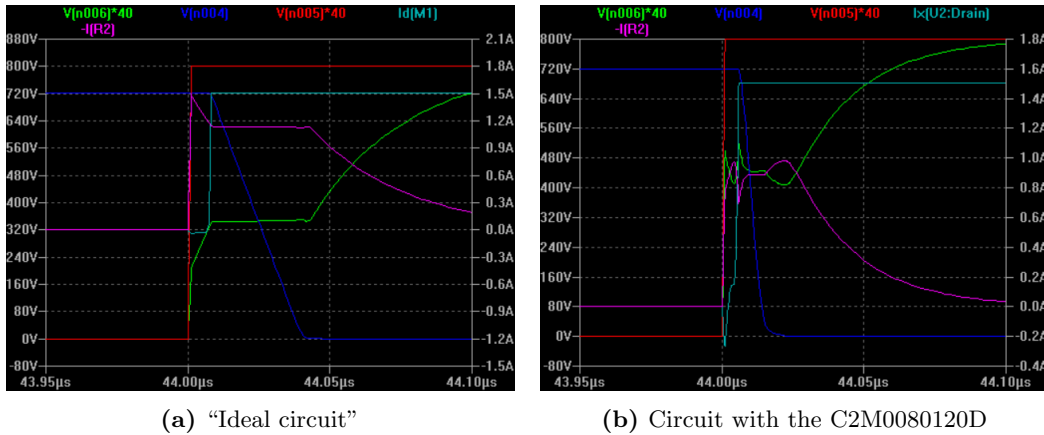


Figure 4.6: Differences between the turn-on waveforms (green: gate-source voltage, blue: drain-source voltage, red: gate driving voltage, light blue: drain current, pink: gate current)

Design evaluation During this testing phase, it was already observed that the gate resistance of 10Ω is really necessary. The circuit was also tested with $R_G = 5\Omega$ and $R_G = 0\Omega$. During these tests the gate driver broke down multiple times. This was probably due to the high current. With $R_G = 0\Omega$, the total gate resistance equals 2.5Ω and a current of 8A flows, which is more than the maximum current the driver is able to provide.

Another thing that was observed is that the optical fiber receivers are susceptible to EMI generated by the switching actions. The receivers of the top MOSFET were triggered by the switching actions of the bottom MOSFET, creating an oscillation in all measurable voltages and currents. The receivers were triggered because they are made of plastic and probably not shielded. Adding an external shield in the form of locally grounded sheet metal cover solves this problem.

During the measurements, it was observed that the current waveforms were not as expected. The drain current of the MOSFET didn't return to 0A when the MOSFET was turned off. The technical notes[38] revealed that the Rogowski coil used to measure the current is sensitive for fast changing voltages due to capacitive coupling of the fast changing voltage node with the Rogowski coil when $\frac{dv}{dt} > 100V/\mu s$. Since the lowest measured $\frac{dv_{DS}}{dt} \approx \frac{720V}{200ns} = 3600V/\mu s$ at turn-off, the Rogowski coil will definitely be disturbed by v_{DS} . To eliminate this effect, the current through the MOSFET is measured at the source of the MOSFET, since this node is at non-varying potential (ground).

Single pulse test with complementary MOSFETs

The single pulse test with complementary MOSFETs is the same as the single pulse test with one MOSFET, but now both MOSFETs in figure 4.1 are switching. It is used to verify the dead time and to check whether the switching behaviour changed compared to the single pulse test with a single MOSFET. The signal in figure 4.2 is applied to G_2 and the inverted signal with 200ns dead time is applied to G_1 .

Test procedure The test procedure is the same as for the tests with the single MOSFET. The only difference is that now the number of turns needed at a specific voltage is known from the previous test. These tests are performed on both the phase legs.

Results Since the dead time was set to 200ns in the controller, the measurement results should be exactly the same as the measurement results of the single pulse test with a single MOSFET. The rise-time at turn-off, which is bigger than the fall-time during turn-on, is 200ns, so the switching actions will not be affected by the switching of the complementary MOSFET. This is confirmed by both the simulation and the measurements.

Design evaluation During the process of increasing the input voltage, it was found that starting from a certain voltage level, the oscillations as seen in the single pulse test with a single MOSFET showed up again. This could not be the result of the EMI, since the fiber receivers are covered now. It appeared that when the fibers were pulled a bit out of the receiver, the oscillations disappeared. But it was not until the test of the full module without control (see section 4.1.2) that adjusting the length of fiber inserted in the receiver affects the delay introduced by the fiber receiver. This is explained in more detail in appendix C.

Dual pulse test with the complete full bridge

The single pulse test with the complete full bridge is a bit different from the previous tests. In this test, all 4 MOSFETs are used to apply a voltage across the inductor. This test is, like the previous test, mainly used to verify the integrity of the driving signals to the MOSFETs.

The signal that is applied to the MOSFETs differs from the previous tests. The MOSFETs are driven in such a way that the voltage across the inductor is equal to the waveform shown in figure 4.7.

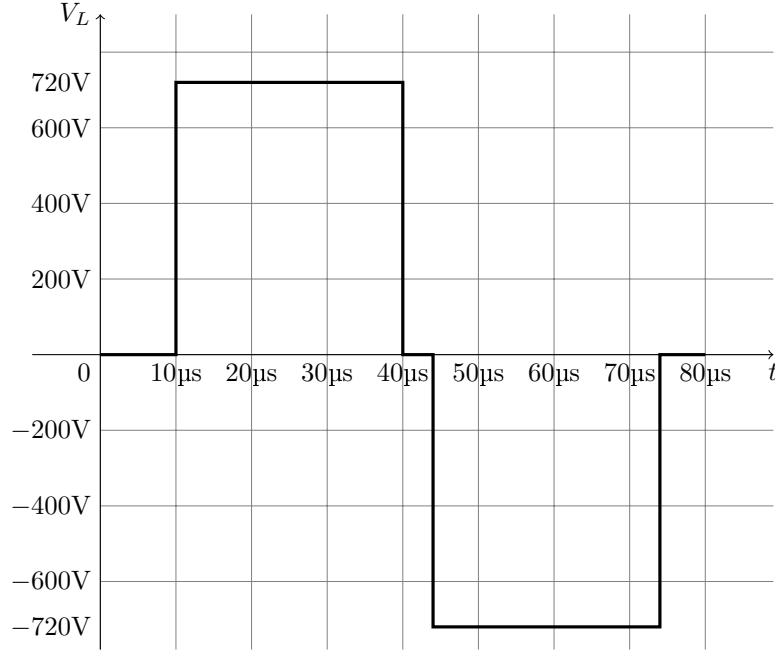


Figure 4.7: Desired inductor voltage waveform of the dual pulse test

Test procedure The test procedure is the same as for the previous tests.

Results The results of this test are shown in figure 4.8.

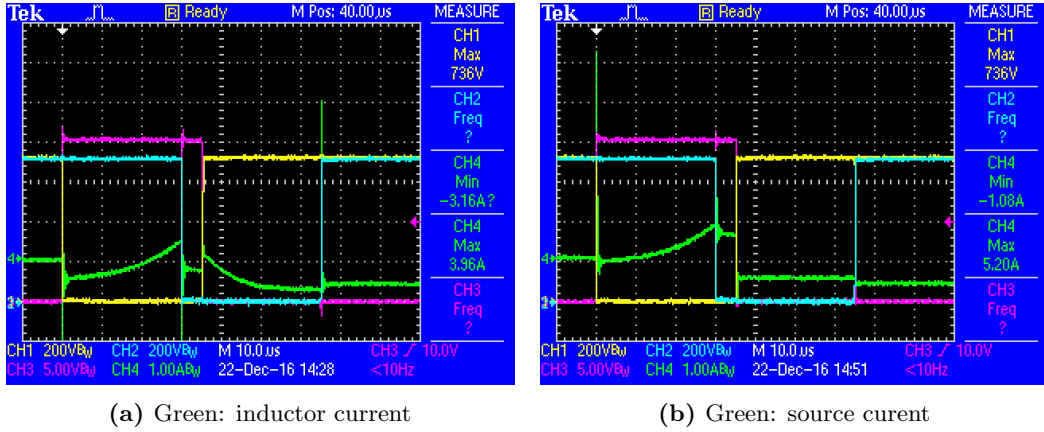


Figure 4.8: Overview of measured waveforms during the dual pulse tests (yellow: drain voltage of left phase leg, light blue: drain voltage of right phase leg, pink: gate voltage of bottom left MOSFET)

Figure 4.8a gives an overview of the measured waveforms: yellow is the drain voltage of the bottom left MOSFET, blue is the drain voltage of the bottom right MOSFET, pink is the gate voltage of the bottom left MOSFET and green is the inductor current. In this figure, the influence of the high $\frac{dv}{dt}$ on the current measurement is clearly visible. In this setup, the inductor current can only be measured at points with high $\frac{dv}{dt}$, which means that the current measurement is influenced a lot due to the capacitive coupling. This is clearly visible at the switching moments.

Figure 4.8b is almost the same as figure 4.8a, except that the source current of the bottom left MOSFET is measured instead of the inductor current. Also this figure shows some current steps, although they are smaller compared to the measured current steps in the inductor current. However, in the measurements of the MOSFET current in the single pulse tests, these current steps were almost absent. This is probably due to the new adjustment of the optical fibers, which cause the switching behaviour to be different compared to the single pulse test with complementary MOSFETs.

4.1.2 Full module without control

Before the full module with the control system is tested, the hardware should be tested. This is done by applying the pulse pattern used in the SPICE-simulation to the module. In this way, a fair comparison between the simulation and the real module could be made.

Test procedure In these tests, the input voltage is increased in steps of 50V. Then the number of switching cycles is gradually increased. First, the module performs only a few switching cycles to confirm its proper operation. This number is then increased up to 100 cycles, after which the converter is put into continuous operation.

For a certain input voltage, multiple test with a different load were performed to see the effect of the (partially) resonant switching. During the tests, the temperature of the different components was measured with a thermal imaging camera.

All tests were performed with a switching frequency of 100kHz (so an effective switching frequency of 200kHz), a duty cycle of 50% and a dead time of 200ns. At the start of the tests, all components were at room temperature. The thermal images were taken 10 minutes after the start of the test.

Results During these tests, multiple quantities were measured. The most important electrical quantities are summarized in table 4.1. In this table, η_m is the measured efficiency and η_s is the simulated efficiency. From this table it becomes clear that the module is operating in discontinuous conduction mode, since the output voltage is dependent on the load. The output voltage is also dependent on the output filter inductance.

From this table it also becomes clear that the efficiency is not clearly rising with the load current. Although the efficiency rises from a very low load (500 Ω) to a higher load (71 Ω) at $V_{in} = 250V$ from 58.8% to 79%, there is not so much increase when the load current increases more. With load currents higher than approximately 3.3A ($V_{in} = 500V$ and $R_L = 25\Omega$), the efficiency decreases.

When the load is “moderate” (the cases where $R_L = 71\Omega$), the calculated efficiency is pretty close to the real efficiency. The real efficiency is a few percent lower. This is due to the fact that the inductor losses are not simulated. Sometimes the real efficiency is higher than the simulated efficiency. This could be due to the fact that the snubber is also simulated, while it is not used in the real circuit. The snubber is also simulated to damp out the diode current oscillations, which are not present in the real circuit. With the diode current oscillations, the simulation and real circuit are even more difficult to compare.

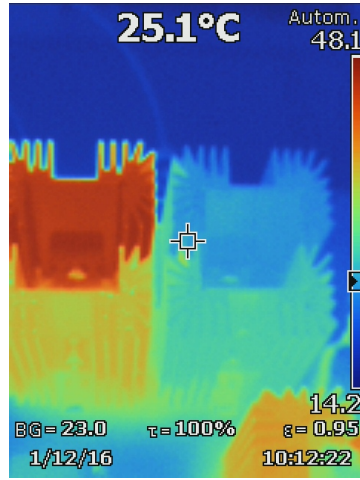
At low and high load currents, the real efficiency is very different from the simulated efficiency. At low load, the original inductor was used, which has high core losses. At high load, the difference in efficiency is probably due to the heating of the transformer windings, which increases resistive losses. This effect also happens in the self-wound inductor. The output filter inductor has core losses which are also not incorporated in the simulation. These losses increase when the inductor current and inductor current ripple increases. The rapid efficiency drop at the higher load currents also indicates resistive losses and core losses.

A major difference in the simulations and the real circuit is the output voltage. In some cases, the difference is less than 1V, but in one case the measured voltage is 10V higher than the simulated voltage. These differences could not be explained.

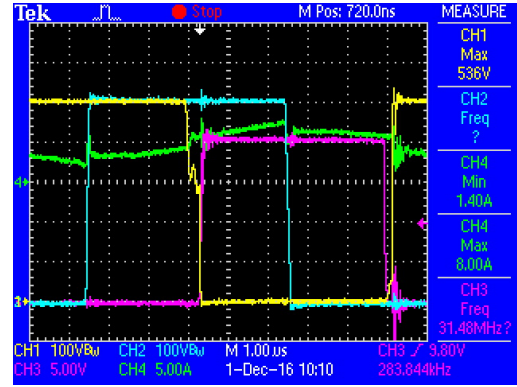
V_{in}	R_L	V_{out}	P_{in}	P_{out}	η_m	η_s	Remarks
250V	500 Ω	85.6V	25W	14.7W	58.8%	56%	
250V	71 Ω	62V	57.5W	45.4W	79%	87%	
250V	71 Ω	52.4V	50W	38.7W	77.4%	80%	Own inductor
350V	71 Ω	85.5V	127W	102W	80.3%	88%	
350V	71 Ω	72.8V	91W	74.9W	82.3%	82%	Own inductor
350V	13 Ω	56.1V	277W	226W	81.6%	94%	Own inductor
400V	71 Ω	82.9V	120W	97.1W	80.9%	84%	Own inductor
450V	71 Ω	93V	148.5W	121.8W	82%	85%	Own inductor
450V	25 Ω	74.7V	257W	208W	80.9%		Own inductor
500V	25 Ω	82.1V	310W	252W	81.3%	79%	Own inductor
500V	15 Ω	79.1V	565W	426W	75.4%	89%	Own inductor
550V	25 Ω	90.3V	374W	289W	77.3%	92%	Own inductor

Table 4.1: Measured electrical quantities during the full module tests

During these tests, also some thermal images were shot. These images show unevenly distributed switching losses. This is shown in figure 4.9a (a normal image of the module is shown in appendix A). The distribution of the switching losses is in accordance with the scope dumps, which show that some switching actions more resonant than others. This is shown in figure 4.9b. The yellow line is the drain voltage of the bottom left MOSFET and the blue line is the drain voltage of the bottom right MOSFET. It shows that approximately 40% of the turn-on of the bottom left MOSFET is resonant and that approximately 10% of the turn-off of the bottom left MOSFET is resonant. So the switching actions of the left phase leg are 75% hard switching. The blue line shows a relatively slow changing drain voltage without kinks, which indicates that the right phase leg switching fully resonant. This is confirmed by the simulations.



(a) Thermal image



(b) Switching actions (yellow: drain voltage of the left phase leg, light blue: drain voltage of the right phase leg)

Figure 4.9: Measurements with $V_{in} = 500V$ and $R_L = 25\Omega$

The difference in the amount of soft switching in the left phase leg and the right phase leg is due to the current levels at which the switching actions take place. In figure 4.9b it is shown that the right phase leg switches at instances where the absolute value of the primary transformer current is high, while the left phase leg switches at instances where the transformer current is low. (In figure 4.9b, the transformer current is green and has an offset due too the poor capability of the Rogowski coil to measure high frequency currents.)

Design evaluation The performance of the design was on multiple points different from the expected performance:

- At the beginning of these tests, the module waveforms starts to oscillate due to overlap in the on-time of the transistors in a phase leg. The secondary side of the transformer, except from the midpoint, was disconnected from the module, the oscillations were still there. When the midpoint was also disconnected, the oscillations disappeared. This means that the capacitive coupling between the primary and secondary side of the transformer induced currents in the secondary side of the module which influenced the control circuit. The use of Y-capacitors at the input of the module and a proper grounding scheme solved this problem.
- During these tests, the filter inductor was replaced. The PCB inductor has a saturation current of 26A, a rated current of 34A and the inductance was measured at 100kHz. The maximum operating temperature is 155°C. The measured temperature with $V_{in} = 350V$ and $R_L = 71\Omega$ was 97°C. With a higher load current, the temperature would certainly get above 155°C. This meant that another inductor had to be used. A hand-made inductor with an inductance of 57 μ H.
- In section 3.2.8 it is described that the rectifier diodes caused large oscillations in the diode currents. These oscillations in turn caused almost all waveforms to oscillate. But during the tests, no oscillations caused by the diodes was seen, even without the snubber. This is considered as a fault in the Cree diode model.
- The output voltages and efficiencies measured for the same setup could differ significantly between measurements. Dit was due the new adjustment of the optical fibers. The adjustment was almost the same, but the small difference were still enough to change the results significantly.

4.1.3 Full operation with control

In this test, the full local control system will applied to module. Due to time constraints, the module was not tested with current mode control. This section describes the steps that have to be taken to perform this test.

Test procedure This test differs from the test without control in a few ways. These differences need to be tested. The differences are:

- The output voltage should be constant with ($9A \geq I_{load} \geq 17A$).
- The output voltage should be independend of the input voltage when $500V \geq V_{in} \geq 1000V$.
- With low load or no-load, the output voltage has a bigger ripple compared to the output voltage at normal load. The frequency depends on the load current: the lower the load current, the lower this frequency. This is due to pulse skipping.
- During startup, the inrush current is limited.
- The inductor current and output current are limited. When the load current exceeds 17A, the output voltage drops.
- The volt-second limiter distorts the current waveform a bit.

Before the actual test can proceed, some other tests should be done. All control circuitry (sensors, comparators, DAC) have to be tested in combination with the FPGA. Then voltage can be applied to the input of the module. The initial voltage has to be low and should be gradually increased when the correct operation of the module at that voltage is proven. When the module works correctly, thing like OVP, OCP and the volt-second limiter can be tested.

4.2 Design evaluation of multiple modules

When one module is tested, the full converter should be tested. The full converter consists of multiple modules. The cooperation of these modules should be verified. This section describes which tests should be done to verify the operation of the full converter.

Due to time constraints, these tests are not performed. The performance of multiple modules is only verified by simulation, as described in section 3.3.

4.2.1 Test procedure

To perform these tests, several steps have to be taken.

1. First, the communication between two modules has to be tested with some test messages.
2. Then, two modules have to be connected to separate voltage sources with an equal voltage. The outputs of the modules are connected in parallel and a load is applied. This is to test the output current sharing control.
3. After the output current sharing test, the input voltage of one module should be changed. The module with the higher input voltage should now supply more current, since it thinks that this will discharge the input capacitor.
4. The second and third tests have to be repeated with 3 or more modules.
5. Then, two modules have to be connected in series. The output of the modules should not be connected in parallel. The modules should have an equal output load. This is to test the input voltage sharing.
6. The fifth test has to be repeated with one module having an additional capacitance connected to input to test the input voltage sharing when the input capacitances are unequal.
7. The fifth and sixth test should be repeated with 3 or more modules.
8. During the last test the inputs have to be connected in series and the outputs have to be connected in parallel.

After correct operation of the ISOP parts of the control (input voltage sharing and output current sharing) is confirmed, the full converter, consisting of multiple modules, should be tested for different situations, like load changes and input voltage changes.

4.3 Conclusion

The measurements reveal that the switching times of the real MOSFETs are approximately two times slower than the switching times predicted by the simulation. This could be partially explained by the parasitics that are not modelled. Switching with a complete phase leg doesn't affect the switching process, since the switching of the first MOSFET is completed before the second MOSFET starts switching.

The complete module is tested without control. This is to confirm the proper operation and to compare the real circuit to the simulated circuit. It was found out that the diode oscillations don't occur in the real circuit. The efficiency is at moderate load current a few percent lower than the calculated efficiency, but the measured output voltage differs significantly from the simulated output voltage. This could not be explained. The switching losses are not equally divided over the phase legs, which is predicted by the simulations and caused by the difference in the transformer current level at the switching moments.

Due to the problems that are mainly caused by the optical fiber receivers, the module is not tested with full input voltage, full output current and with the control system enabled. The test plan to perform these tests is described in this chapter.

The converter proved to be very unstable due to the sensitivity of the optical fiber receivers for electromagnetic and mechanical influences.

Chapter 5

Conclusions & future work

In this thesis, the ways of using SiC switches for power converters are explored. SiC switches have low switching losses and low switching times. Therefore, they enable converters with a high power density and small output filter components, reducing the converter size. It turned out that the SJT was the best device when only considering switching losses and that the MOSFET was the best device when also considering the driving circuit and thermal resistance.

Also, a proposal for a modular converter design is presented. First, the ways of building an input voltage sharing modular converter are described and evaluated. This led to the choice of using multiple standalone converters for building a modular converter. These modules are equipped with a control system that enables input voltage sharing and output current sharing. This control system is simulated to confirm the proper operation of this system.

With this more abstract design a real module is designed and implemented. The electrical performance of this module was measured and compared to the simulations. From these comparisons it can be concluded that the real module behaves very differently from the simulation. At moderate load, the efficiencies are close, but the output voltages could differ by 10V. These differences could be explained by increased conduction losses in the magnetics due to wire heating, core losses in the magnetics and problems with the optical fibers. Another difference between the simulations and reality is that the predicted diode current oscillations were not observed.

This leads to the conclusion of this thesis: the objective of designing a working modular SiC based converter is not achieved.

5.1 Future work

To achieve the initial goal of this thesis project, several steps have to be made:

- The models used in the simulation should be adjusted so that they are a better representation of reality.
- The first step is to design a new module with a reliable driving circuit for the MOSFETs. In this way, the driving signals doesn't get distorted and the real performance of the module could be obtained. Different optical fiber transmitters and receivers need to be used and to isolate the driving circuit even further from EMI a 4-layer PCB design should be considered.
- The communication system should be fully implemented.
- The electrical performance of a setup containing multiple modules should be evaluated.
- During the design, EMC is not considered. In a new design, EMC should be considered.

To achieve an even better converter, some research has to be done:

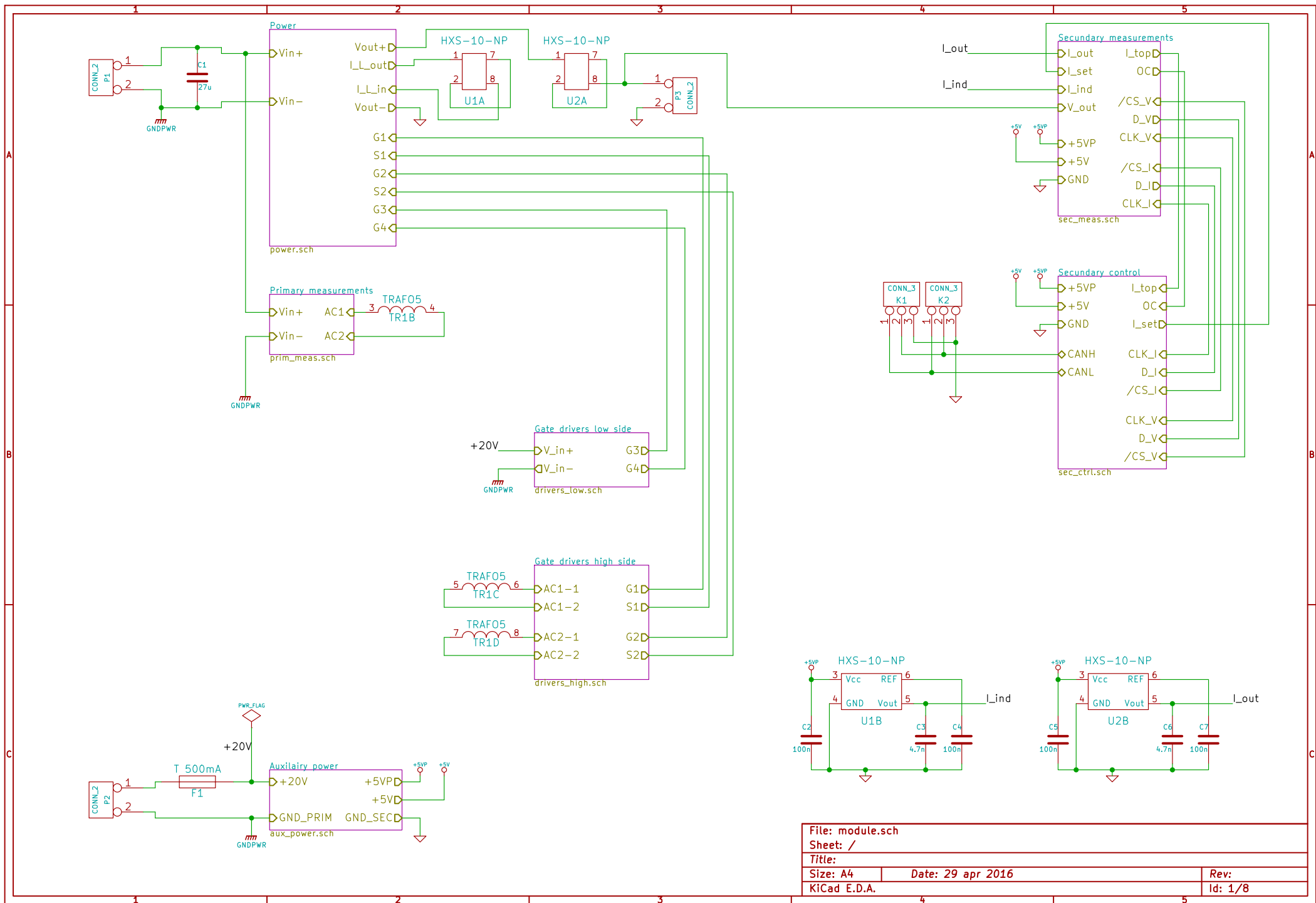
- Since the converter is a phase-shifted full bridge converter, the only losses in the transistors should be the turn-off losses. The datasheet of the SJT shows that its turn-off losses are very low compared to its turn-on losses and compared to the turn-off losses of a MOSFET. The use of a SJT instead of a MOSFET should be considered.
- Current practice for the control system implementation is to create a Simulink model to simulate the converter. When the results of this simulations satisfy the requirements, code is generated from this model. This code is then flashed into an ARM microprocessor. Although easy to work with, a lot of calculations have to be done and the code generated by this process is not very fast. When the switching frequency becomes higher, the control has to become faster. There is a probability that this speed could not be achieved with the described setup.
- The use of a shield between the primary and the secondary side of the transformer should be considered. This shield eliminates current flowing from the primary to the secondary through parasitic capacitances within the transformer, but generates more common mode EMI. This latter fact leads to the increased need for Y-capacitors, while the shield should eliminate the Y-capacitors. The effect of a shield should be investigated. It could be possible that a shield is not necessary when a less sensitive gate drive circuit is used.

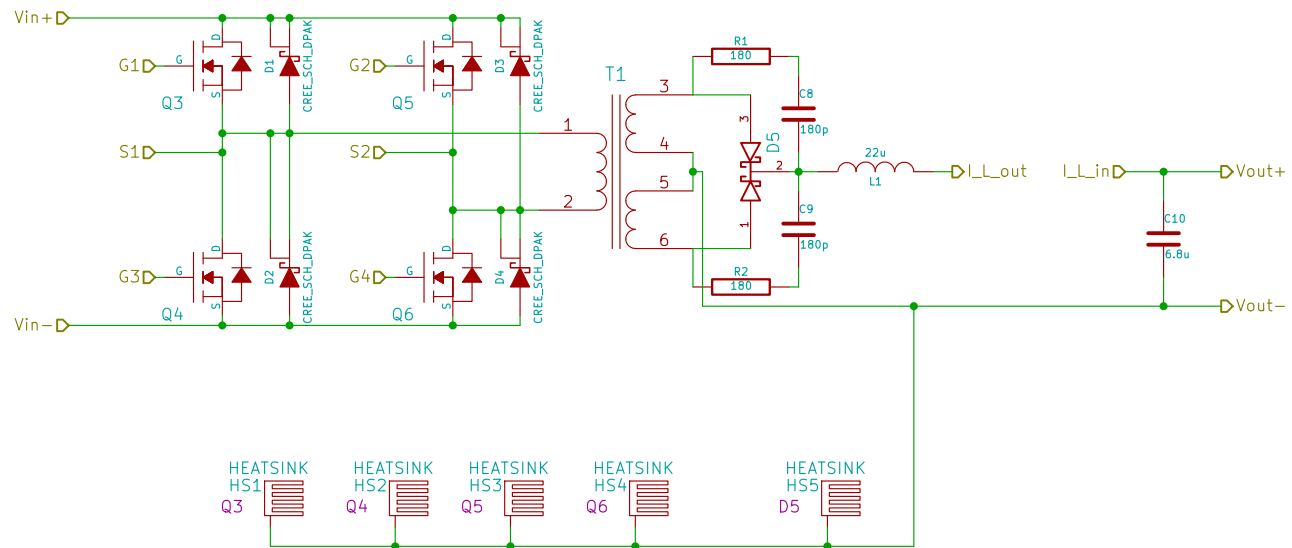
Appendix A

Schematics and PCB

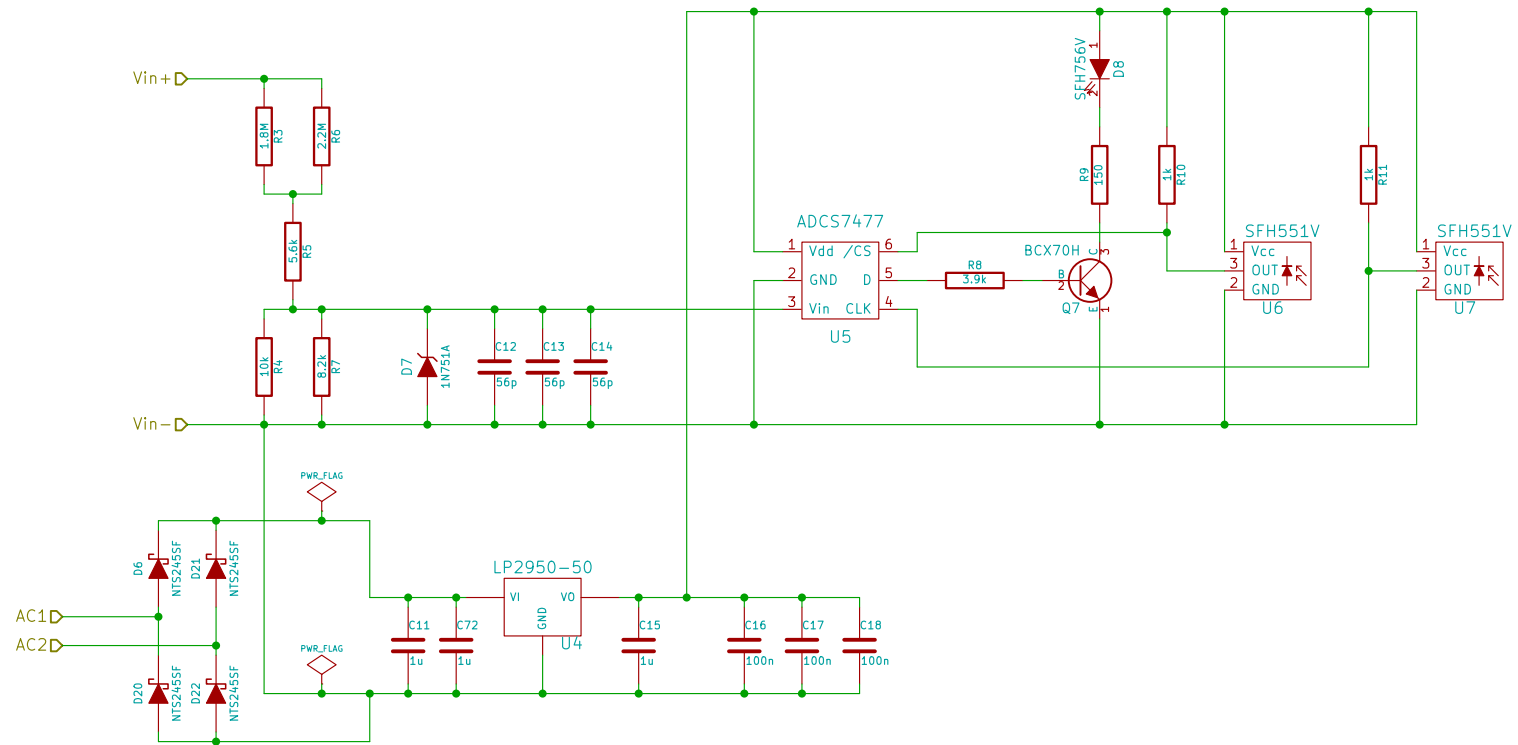
A.1 Schematics

The schematics of the module are shown on the next 8 pages.

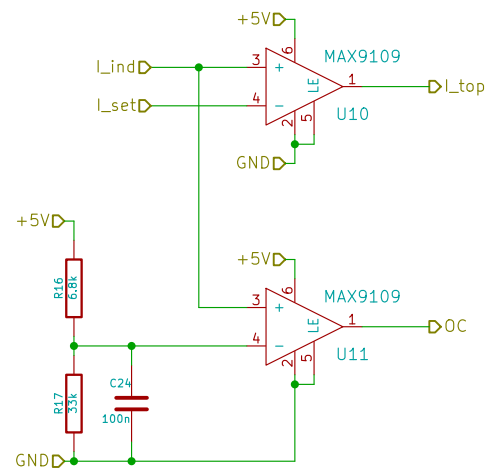
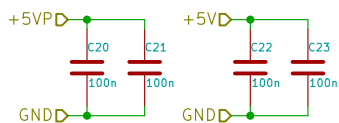
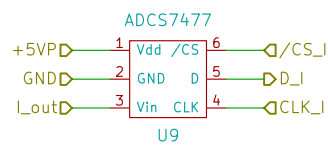
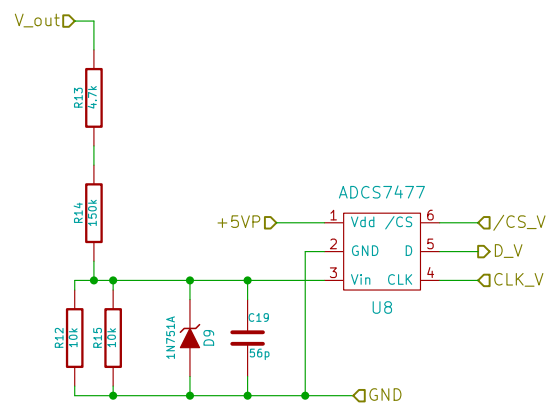




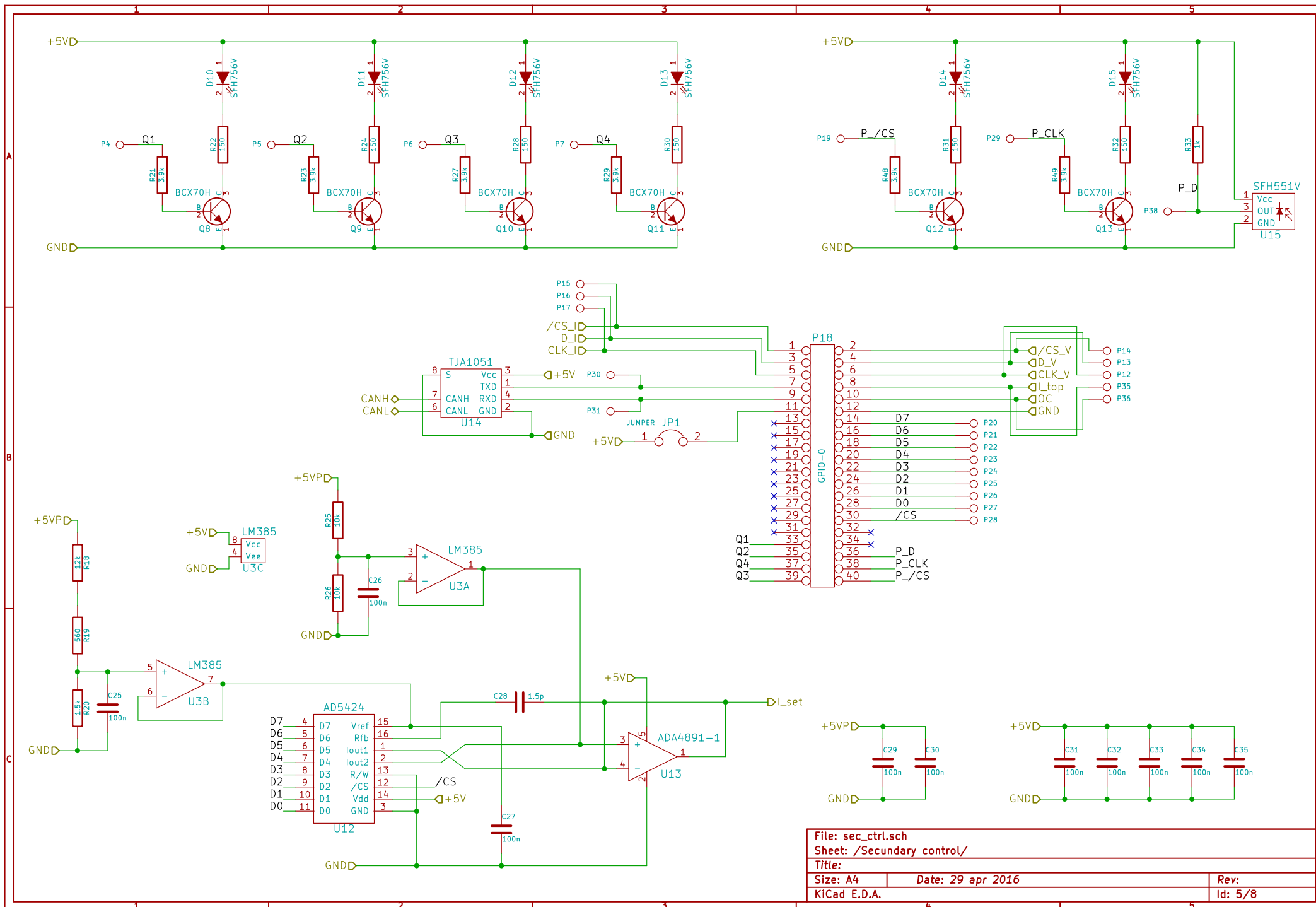
File: power.sch		
Sheet: /Power/		
Title:		
Size: A4	Date: 29 apr 2016	Rev:
KiCad E.D.A.		Id: 2/8

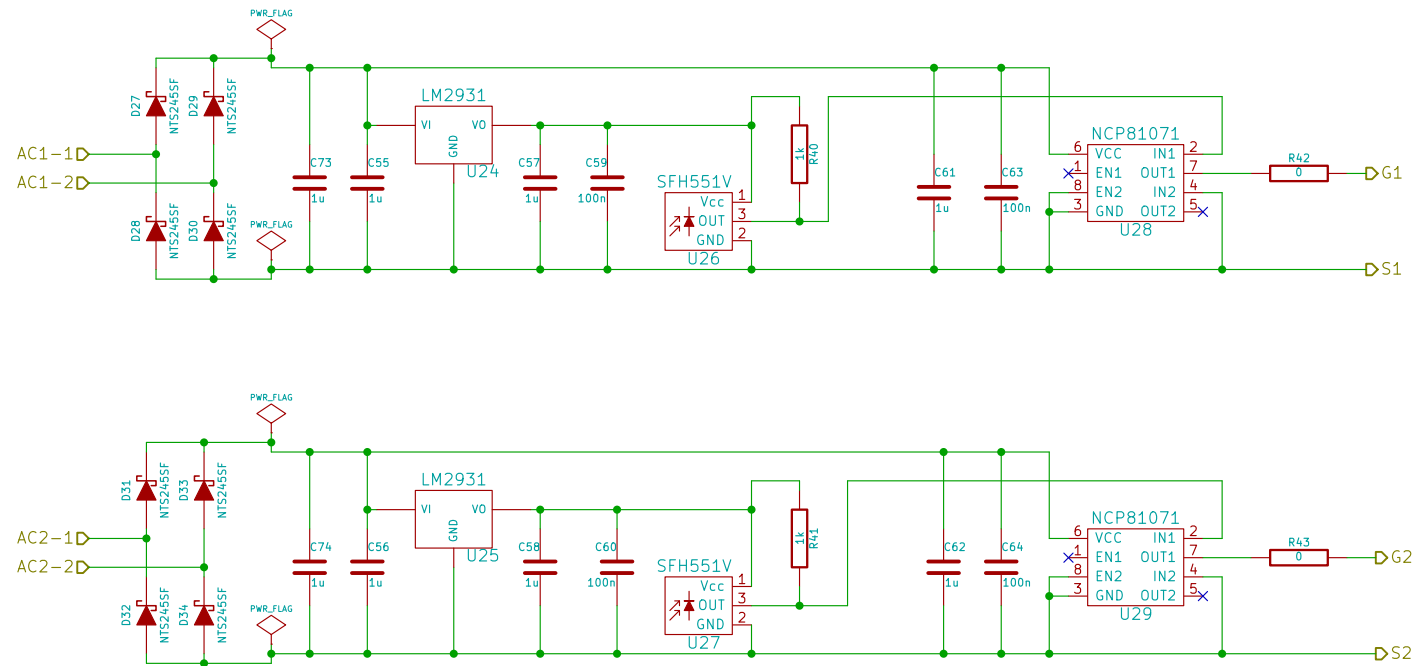


File: prim_meas.sch		
Sheet: /Primary measurements/		
Title:		
Size: A4	Date: 29 apr 2016	Rev:
KiCad E.D.A.		Id: 3/8

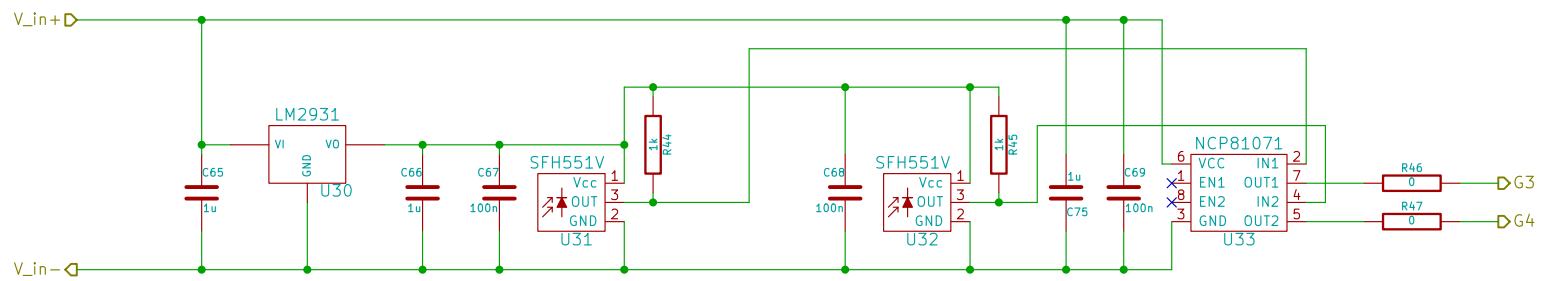


File: sec_meas.sch		
Sheet: /Secondary measurements/		
Title:		
Size: A4	Date: 29 apr 2016	Rev:
KiCad E.D.A.		Id: 4/8





File: drivers_high.sch		
Sheet: /Gate drivers high side/		
Title:		
Size: A4	Date: 29 apr 2016	Rev:
KiCad E.D.A.		Id: 7/8



File: drivers_low.sch		
Sheet: /Gate drivers low side/		
Title:		
Size: A4	Date: 29 apr 2016	Rev:
KiCad E.D.A.		Id: 8/8

A.2 PCB

The PCB consists of two layers. The front layer is shown in figure A.1, the back layer is shown in figure A.2.

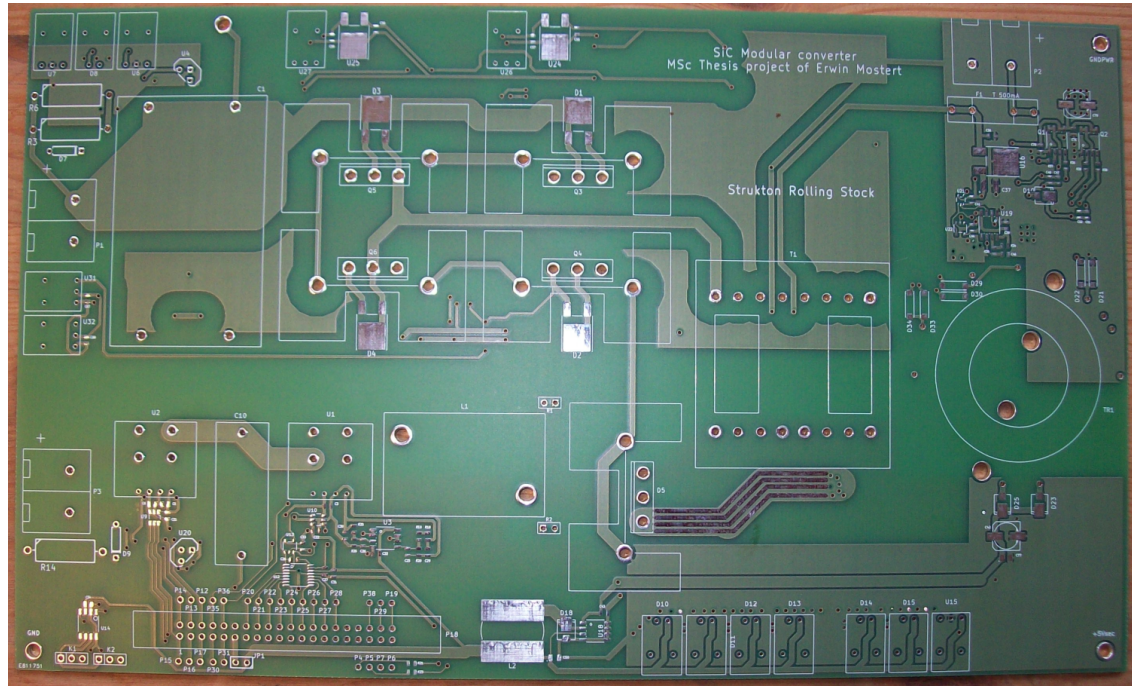


Figure A.1: Front layer of the PCB

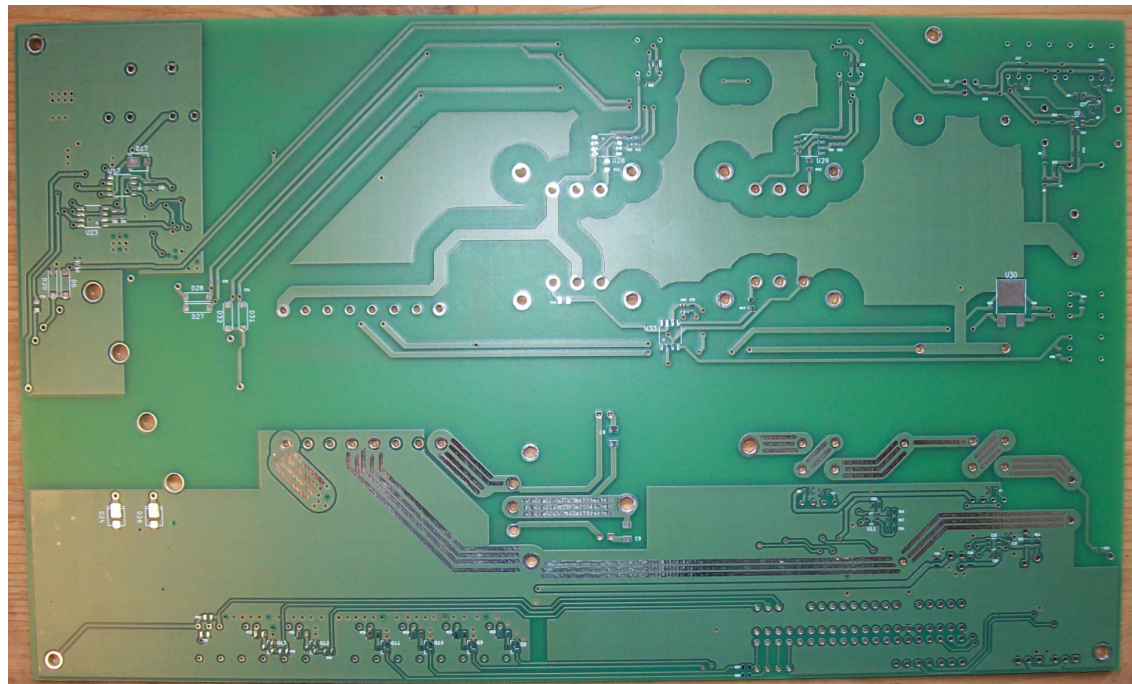


Figure A.2: Back layer of the PCB

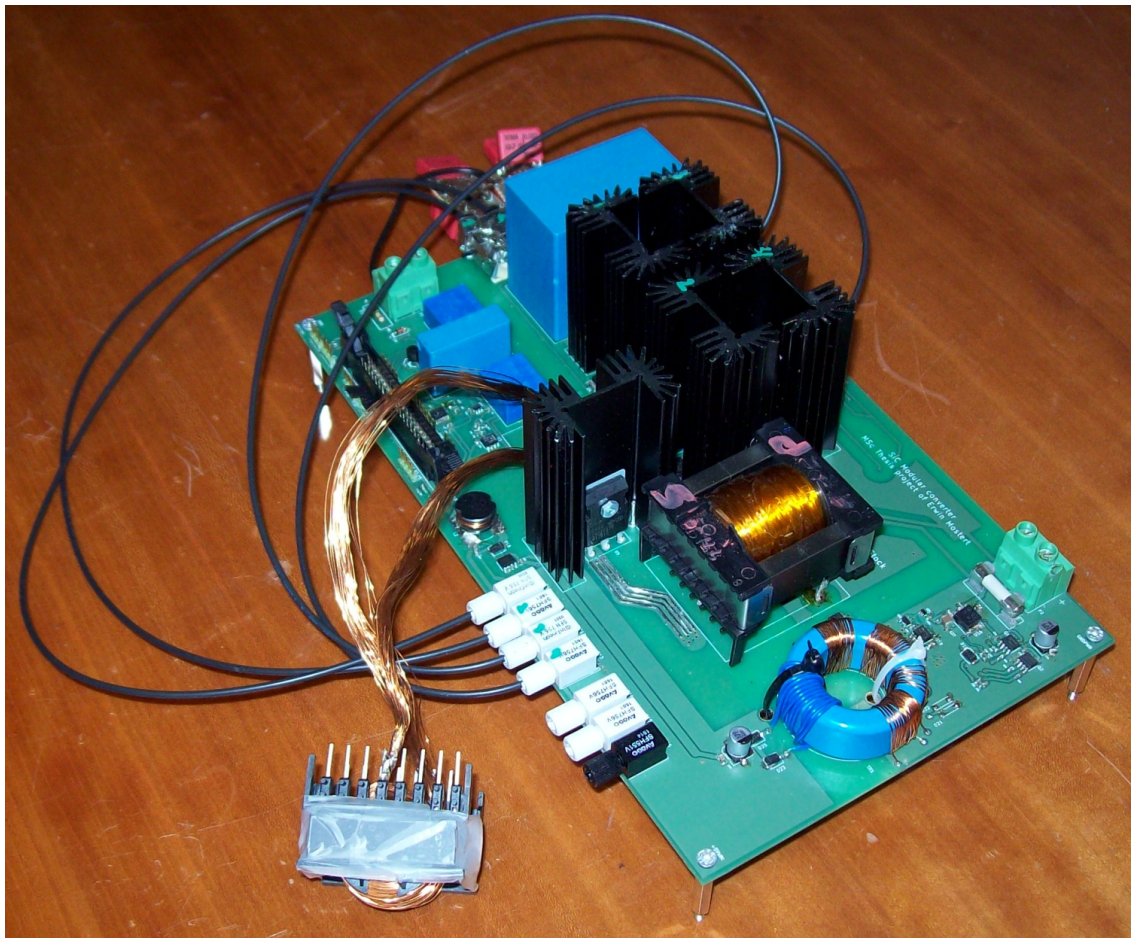


Figure A.4: Assembled PCB from the right

Appendix B

Slope compensation

Slope compensation is needed to prevent subharmonic oscillation of the inductor current in current control of a buck-based converter. This appendix explains the origin of these subharmonic oscillations and how the slope compensation should be implemented.

B.1 Origin of subharmonic oscillations

In steady state, the inductor current at the start of a switching period equals I_0 . During steady state, the inductor current at $t = T_{SW}$ also equals I_0 . At the start of each switching period, the inductor current is equal: $i_L(t) = i_L(t + T_{SW})$.

But during startup of the converter, this is not the case. The inductor current increases very fast due to the low voltage on the output capacitor. The capacitor charges. Then, the inductor current decreases. This decrease of current goes beyond the steady state value, because the capacitor is overcharged by the huge amount of energy stored in the inductor. The average inductor current oscillates around the expected inductor current. When this oscillation is damped, steady state is reached.

The slope of the current is s_1 during T_{on} and is s_2 during T_{off} . s_1 is linear dependent on the difference between the input voltage and the output voltage, while s_2 is linear dependent only on the output voltage. So independent on the input voltage, s_2 is a fixed constant, as long as the output voltage is kept constant. To keep the output voltage constant with different input voltages, the duty cycle needs to be adjusted. With a high input voltage V_{in} , the duty cycle d is small and the slope s_1 is high. With a low V_{in} , d is big and s_1 is low.

With current mode control, this oscillation is not fully damped. At the moment where the oscillation is almost fully damped, there exists a small difference between the expected I_0 and the real I_0 . This difference is ΔI_0 . Then the following happens: the current increases to the maximum value set by the current mode control with slope s_1 . The time at which the inductor current reaches the maximum current is in equation (B.1). Then the current decreases with slope s_2 . The current at $t = t_0 + T_{SW}$ is then in equation (B.2).

$$t = \frac{I_{max} - I_0}{s_1} \quad (\text{B.1})$$

$$I = I_{max} - s_2 t \quad (\text{B.2})$$

The situation is as follows: I_0 is the expected steady state value for $i_L(t_0)$, but the real value is $I'_0 = I_0 + \Delta I$. This creates a difference in the time the inductor current crosses the maximum current set by the control. This difference in time is called Δt and is calculated with equation (B.3). The difference in the current at $t = T_{SW}$, called ΔI_1 , is then calculated with equation (B.4). In (B.5), equations (B.3) and (B.4) are combined.

$$\Delta t = t_2 - t_1 = \frac{I_{max} - (I_0 + \Delta I_0)}{s_1} - \frac{I_{max} - I_0}{s_1} = \frac{-\Delta I_0}{s_1} \quad (\text{B.3})$$

$$\Delta I_1 = (I_{max} - s_2 t_2) - (I_{max} - s_2 t_1) = (I_{max} - s_2(t_1 + \Delta t)) - (I_{max} - s_2 t_1) = s_2 \Delta t \quad (\text{B.4})$$

$$\Delta I_1 = \frac{-\Delta I_0}{s_1} s_2 = -\frac{s_2}{s_1} \Delta I_0 \quad (\text{B.5})$$

When $d < 50\%$, $s_2 < s_1$ and $|\Delta I_1| < |\Delta I_0|$. The oscillation is further damped. But when $d > 50\%$, $s_2 > s_1$ and $|\Delta I_1| > |\Delta I_0|$. The oscillation is not damped at all and is even increased. But the inductor current is now lower than expected instead of higher, thus the capacitor is discharged. The next period, the value of i_L at the end of the period is bigger than expected, charging the capacitor. The oscillation in the output voltage grows until the maximum output voltage is reached. The converter switches off, letting the output voltage decrease. Then the whole cycle starts over again.

B.2 Slope compensation

To solve the problem of subharmonic oscillations, a slope is added to I_{max} . The slope has 2 properties: slope and offset. With the slope added, the value of I_{max} becomes dependent on time: $i_{max}(t) = I_{max} - st + I_{offset}$, with $i_{max}(t)$ the current value at which the switch should be turned off, I_{max} the output of the error gain, s the slope, t the time and I_{offset} the possible offset.

B.2.1 Slope

The new equation for $i_{max}(t)$ has some implications for equations (B.1) and (B.2). With slope compensation, these equations become equation (B.6) and (B.7) respectively. Equation (B.5) then becomes (B.8).

$$t = \frac{I_{max} - I_0}{s_1 + s} \quad (\text{B.6})$$

$$I = I_{max} + t(s_2 - s) - s_2 T_{SW} \quad (\text{B.7})$$

$$\Delta I_1 = -\frac{s_2 - s}{s_1 + s} \Delta I_0 \quad (\text{B.8})$$

To achieve stability, $|\Delta I_1| \leq |\Delta I_0|$, so $\frac{s_2 - s}{s_1 + s} \leq 1$ for all values of s_1 . This means that $s \geq \frac{1}{2}(s_1 - s_2)$. The value of $\frac{1}{2}(s_1 - s_2)$ has its minimum at $s_1 = 0$ ($d = 100\%$), so $s \geq -\frac{1}{2}s_2$. In [51] it is shown that with $s = -\frac{1}{2}s_2$, the average current becomes independent of s_1 .

B.2.2 Offset

The slope could be added to $i_{max}(t)$ with an offset. The question is now what this offset should be. The offset should be chosen in such a way that the average inductor current with slope compensation is the same as without slope compensation.

As the converter is not in steady state at the time the slope compensation does its work, calculating this value will be rather complex. To find a suitable offset, some values are tried in simulation. These values are based on the difference between $i_{max}(0)$ and $\lim_{t \rightarrow T_{SW}} i_{max}(t)$, which is $\Delta I_{max} = \frac{1}{2} \frac{V_{out}}{L} T_{SW}$. The first offset is 0, the second is $\frac{1}{2} \Delta I_{max}$ and the third is ΔI_{max} . Simulation results reveal that with $I_{offset} = 0$, the output voltage is lower than expected. With $I_{offset} = \Delta I_{max}$, the output voltage is higher than expected. With $I_{offset} = \frac{1}{2} \Delta I_{max}$, the output voltage is the desired output voltage.

B.3 Conclusion

Slope compensation is needed to stabilise a converter controlled by a current mode control scheme. The principle behind the instability is explained and the solution is presented: slope compensation. The slope should be $s = -\frac{1}{2}s_2$ and the offset should be $I_{offset} = \frac{1}{2}\Delta I_{max}$. The result is shown in figure 3.9.

Appendix C

Optical fiber

During the testing process of the converter, there were several problems. The origin of these problems were hard to trace. It turned out that most of these problems could be attributed to the optical fiber transmitters and receivers used.

C.1 The MOSFET driver setup

The circuit used during the tests is shown in appendix A. The driving signals are generated at the FPGA development board. These signals drive small transistors, which turn on the fiber transmitters. A cut optical fiber is inserted both the transmitter and the receiver. This fiber should be pushed in as far as possible. The position of the fibers is locked with the lock screw. This is the installation method described in the datasheet[5].

The receiver has an open collector output. When the receiver detects enough light, the output transistor is turned on. When a pull-up resistor is connected to the output, the output is low when the transmitter is turned on and is high when the transmitter is off. The MOSFET is driven by a driver IC with an inverted input stage, so the MOSFET is turned on when a low signal is applied to its input.

When a fiber is not connected or when there is no control signal from the FPGA, the MOSFET is driven low, because the fiber receiver is not activated.

C.2 Problems

C.2.1 dv/dt issues

During the single pulse test with a single MOSFET (see chapter 4), only the bottom MOSFET of a phase leg was used to switch. The top MOSFET was not driven and therefore driven low by the driver IC. When a certain input voltage was reached, the module starts to oscillate. Such an oscillation is shown in figure C.1. These oscillations have a high frequency. All measurable signals oscillated, so no clear cause could be found.

The problem was found when the fiber of the top MOSFET was removed from the receiver. The problem was not solved, but the waveforms changed. Covering the optical part to avoid the triggering of the receiver by ambient light did not change the measurement compared to only removing the fiber. Later it was discovered that these receivers were not shielded. Adding a locally grounded shield to the receiver solved the problem.

C.2.2 Timing issues

During the single pulse test with the full phase leg and later tests with the full bridge, the oscillations occurred again. The EMI could not be the cause, since the receivers were shielded.

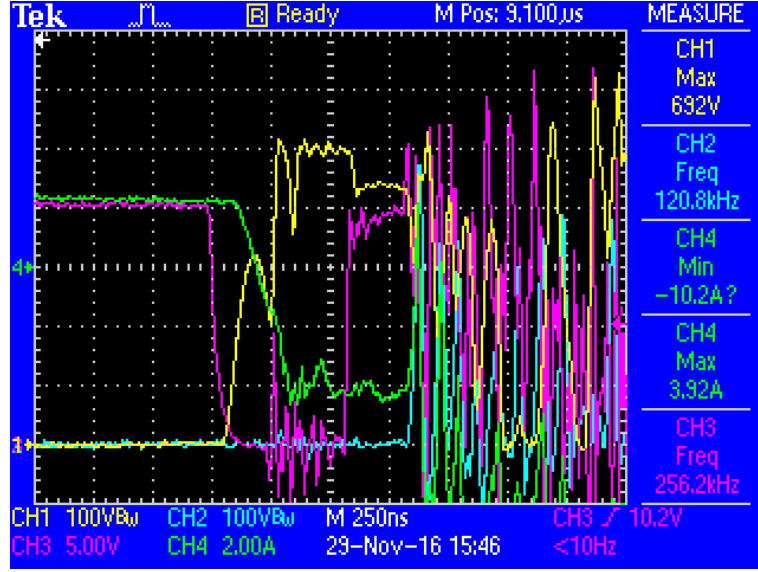


Figure C.1: Oscillation caused by optic fiber reciever. The oscillation starts at 50ns from the midpoint.

It was discovered that when the optical fibers were pulled a bit out of the fiber recievers the problems became less or disappeared. It was still unknown why this happens. Later it was discovered that pulling out the wires of the transmitter or reciever affects the delay in the optical signal path.

Pulling the fibers out of the transmitter or reciever increases the path the light has to travel from the transmitter to the reciever. The maximum play is estimated at 1cm. When the difference in optical path length is the cause of the delays, the maximum play in the delay is about $\frac{1\text{cm}}{3 \cdot 10^8 \text{m/s}} \approx 0.03\text{ns}$. But by pulling the fiber more or less out of the transmitter or reciever, the delays could be “adjusted” by about 400ns. It is believed that the delays are caused by differences in light intensity. Without adjusting the fibers, the dead time could be negative: an overlap was created.

Another problem was that these delays are not symmetric. This means that equal signals could rise at the same time, but one signal falls 120ns later than the other. This is illustrated in figure C.2. This is of course not a wanted situation, because it can cause the transformer to saturate.

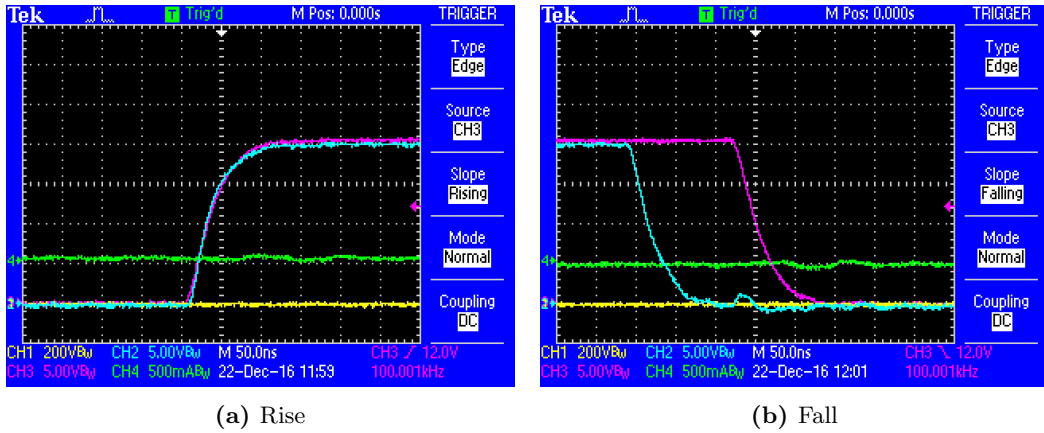


Figure C.2: Asymmetry in the fiber reciever output signals

C.2.3 Not turning off

The last problem occurs when some fibers are fully pushed in the transmitter and receiver. This is the normal installation method, but sometimes this caused the receiver to “saturate”: the output is constant low, independent of the optical signal. This is probably due to some sort of recovery current in the photo-diode when the light is absent. When there is such a current, the transimpedance amplifier within the receiver will still think that the photo-diode is illuminated.

C.3 Conclusion

The problems with the module were mainly caused by the fact that the optic transmitter and especially the optic receivers are not reliable. They caused the MOSFETs to turn on at the wrong time.

Bibliography

- [1] Technical Characteristics of GaN and SiC, 2013. URL <http://epc-co.com/epc/CEOInsights/FastJustGotFasterBlog/December2013.aspx>. 8
- [2] *Silicon carbide - the power semiconductor of the future*. ABB, 1996. 9
- [3] A.R. Alonso, M.F. Díaz, D.G. Lamar, M.A.P. de Azpeitia, M.M. Hernando, and J. Sebastián. Switching Performance Comparison of the SiC JFET and SiC JFET/Si MOSFET Cascode Configuration. *IEEE Transactions on Power Electronics*, 2014. 12
- [4] A. Anthon, Z. Zhang, and M.A.E. Andersen. Comparison of a State of the Art Si IGBT and Next Generation Fast Switching Devices in a 4kW Boost Converter. In *Energy Conversion Congress and Exposition*, pages 3003–3011, 2015. 10, 11
- [5] *SFH551/1-1 and SFH551/1-1V - Receiver with Digital Output Stage for Polymer Optical Fiber Applications*. Avago, 2011. 85
- [6] D. Bortis, J. Biela, and J.W. Kolar. Active Gate Controller for Current Balancing in Parallel Connected IGBT Modules in Solid State Modulators. *IEEE Transactions on Plasma Science*, 2008. 17
- [7] *BS EN 50163: Railway applications - Supply voltages of traction systems*. BS, 2004. 34
- [8] G. Chen, J. Zhang, and X. Cai. Adaptive Digital Gate Control for Series Connected IGBTs. In *Annual Conference of the IEEE Industrial Electronics Society*, pages 394–399, 2013. 17
- [9] *C2M0080120D Silicon Carbide Power MOSFET C2M™ MOSFET Technology*. Cree, 2015. 12, 13, 20, 37, 41
- [10] *C4D02120E Silicon Carbide Schottky Diode*. Cree, 2015. 37
- [11] *CAS300M17BM2 1.7kV, 8.0mΩ All-Silicon Carbide Half-Bridge Module C2M MOSFET and Z-Rec Diode*. Cree, 2015. 12
- [12] *SEMiX353GB176HDs SEMiX® 3s Trench IGBT Modules*. Cree, 2015. 12
- [13] *C4D20120A Silicon Carbide Schottky Diode*. Cree, 2016. 37
- [14] *Gallium Nitride (GaN) versus Silicon Carbide (SiC) In The High Frequency (RF) and Power Switching Applications*. Digi-Key, date unknown. 7, 8
- [15] C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, and P. Mattavelli. Characterization and comparison of 1.2 kV SiC power semiconductor devices. In *15th European Conference on Power Electronics and Applications*, pages 1–10, 2013. 10, 12, 13
- [16] W. Feng, F.C. Lee, P. Mattavelli, D. Huang, and C. Prasantanakorn. LLC Resonant Converter Burst Mode Control with Constant Burst Time and Optimal Switching Pattern. In *Twenty-sixth Annual IEEE Applied Power Electronics Conference and Exposition*, pages 6–12, 2011. 32

-
- [17] *GA10JT12-247 Normally - OFF Silicon Carbide Junction Transistor*. GeneSiC, 2015. 13
- [18] Z. Guo, D. Sha, and X. Liao. Input Voltage Sharing Control for Input-Series-Output-Parallel DC-DC Converters without Input Voltage Sensors. In *IEEE Energy Conversion Congress and Exposition*, pages 1307–1311, 2011. 19
- [19] W. He, P. Palmer, X. Zhang, M. Snook, and Z. Wang. IGBT Series Connection under Active Voltage Control. In *Proceedings of the 14th European Conference on Power Electronics and Applications*, pages 1–9, 2011. 16, 17
- [20] *Design of Phase Shifted Full-Bridge Converter with Current Double Rectifier*. Infineon, 2013. 29
- [21] S. Jahdi, O. Alatise, J.O. Gonzalez, P. Gammon, L. Ran, and P. Mawby. Investigation of Parasitic Turn-ON in Silicon IGBT and Silicon Carbide MOSFET Devices: A Technology Evaluation. In *17th European Conference on Power Electronics and Applications*, pages 1–8, 2015. 10
- [22] S. Jahdi, O. Alatise, J.O. Gonzalez, L. Ran, and P. Mawby. Comparative Analysis of False Turn-ON in Silicon Bipolar and SiC Unipolar Power Devices. In *IEEE Energy Conversion Congress and Exposition*, pages 2239–2246, 2015. 10, 16
- [23] Jinhaeng Jang, Minjae Joung, Seokjae Choi, Youngho Choi, and Byungcho Choi. Current mode control for LLC series resonant dc-to-dc converters. In *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 21–27, 2011. 32
- [24] S. Katoh, S. Ueda, and H. Sakai. Active-gate-control for Snubberless IGBTs Connected in Series. In *Annual IEEE Power Electronics Specialists Conference*, volume 2, pages 609–613, 2002. 17
- [25] S. Keeping. The Role of Slope Compensation in Current-Mode-Controlled Voltage Regulators, 2015. URL <http://www.digikey.com/en/articles/techzone/2015/jan/the-role-of-slope-compensation-in-current-mode-controlled-voltage-regulators>. 48
- [26] R. Khanna, A. Amrhein, W. Stanchina, G. Reed, and Z. Mao. An Analytical Model for Evaluating the Influence of Device Parasitics on C_{dv}/dt Induced False Turn-on in SiC MOSFETs. In *28th Annual IEEE Applied Power Electronics Conference and Exposition*, pages 518–525, 2013. 10
- [27] J.W. Kimball, J.T. Mossoba, and P.T. Krein. A Stabilizing, High-Performance Controller for Input Series-Output Parallel Converters. *IEEE Transactions on Power Electronics*, 2008. 19
- [28] T.C. Lim, B.W. Williams, S.J. Finney, and P.R. Palmer. Series-Connected IGBTs Using Active Voltage Control Technique. *IEEE Transactions on Power Electronics*, 2013. 17
- [29] Y. Lobsiger, D. Bortis, and J.W. Kolar. Decentralized Active Gate Control for Current Balancing of Parallel Connected IGBT Modules. In *Proceedings of the 14th European Conference on Power Electronics and Applications*, pages 1–10, 2011. 17
- [30] T. Lu, Z. Zhao, S. Ji, H. Yu, and L. Yuan. Active Clamping Circuit With Status Feedback for Series-Connected HV-IGBTs. *IEEE Transactions on Industry Applications*, 2014. 17
- [31] Mark LaPedus. What Happened To GaN And SiC? *Semiconductor Engineering - Manufacturing, Design & Test*, 2015. URL <http://semiengineering.com/what-happened-to-gan-and-sic/>. 8
- [32] J.M. Meyer. Resonant MHz Gate Drive. Master’s thesis, Technical University of Denmark, 2008. 10

- [33] *APT25SM120B Silicon Carbide N-Channel Power MOSFET*. Microsemi, 2015. 13
- [34] N. Mohan, T.M. Undeland, and W.P. Robbins. *Power Electronics - Converters, Applications and Design*. Wiley, 2003. 7, 31, 48, 60
- [35] *NCP81071A Dual 5 A High Speed Low-Side MOSFET Drivers with Enable*. ON Semiconductor, 2014. 41
- [36] *NTP8G202N Power GaN Cascode Transistor 600V, 290mΩ*. ON Semiconductor, 2015. 8
- [37] B. Ozpineci and L. Tolbert. Silicon Carbide: Smaller, Faster, Tougher. *IEEE Spectrum*, 2011. URL <http://spectrum.ieee.org/semiconductors/materials/silicon-carbide-smaller-faster-tougher>. 7
- [38] *RCTi and RCTi-3ph Technical Notes*. PEM, 2011. 61
- [39] J. Rabkowski and T. Platek. Comparison of the power losses in 1700V Si IGBT and SiC MOSFET modules including reverse conduction. In *17th European Conference on Power Electronics and Applications*, pages 1–10, 2015. 10
- [40] *SiC Power Devices and Modules - Application Note*. ROHM, 2014. 7, 8
- [41] *SCT2160KE N-channel SiC power MOSFET*. ROHM, 2015. 13
- [42] *Thermal resistance of IGBT Modules - specification and modelling*. SEMIKRON, 2014. 18, 21
- [43] D. Sha, Z. Guo, and X. Liao. Cross-Feedback Output-Current-Sharing Control for Input-Series-Output-Parallel Modular DC–DC Converters. *IEEE Transactions on Power Electronics*, 2010. 19
- [44] *AN2644: An introduction to LLC resonant half-bridge converter*. ST, 2008. 32
- [45] *STB11NM80, STF11NM80, STI11NM80, STP11NM80, STW11NM80: N-channel 800V, 0.35Ω, 11A MDmeshTM Power MOSFET in D²PAK, TO-220FP, I²PAK, TO-220, TO-247*. ST, 2011. 60
- [46] *SCT20N120 Silicon carbide Power MOSFET*. ST, 2015. 13
- [47] *SIFERRIT material N97*. TDK, 2006. 38
- [48] *ETD 44/22/15 Core and accessories*. TDK, 2013. 38
- [49] *Isolated Supply Overview and Design Trade-Offs*. Texas Instruments, 2011. 23, 24
- [50] *TPH3206PS GaN Power Low-loss Switch*. Transphorm, 2015. 8
- [51] *Modelling, analysis and compensation of the current-mode converter*. UNITRODE, 1999. 83
- [52] *UJC1206K SiC Cascode*. USCi, date unknown. 11, 13
- [53] G. Wang, F. Wang, G. Magai, Y. Lei, A. Huang, and M. Das. Performance Comparison of 1200V 100A SiC MOSFET and 1200V 100A Si IGBT. In *IEEE Energy Conversion Congress and Exposition*, pages 3230–3234, 2013. 9
- [54] B.W. Williams. *Power Electronics - Devices, Drivers, Applications, and Passive Components*, chapter Device Series and Parallel Operation, Protection, and Interference. B.W. Williams, date unknown. 16, 17
- [55] B. Yang. *Topology investigation of front end DC/DC converter for distributed power system*. PhD thesis, Virginia Tech, 2003. 31, 33