MSc Thesis

Understand the Physics of Solder Joint Degradation in Board Level Reliability Vibration and Thermal Cycle Test

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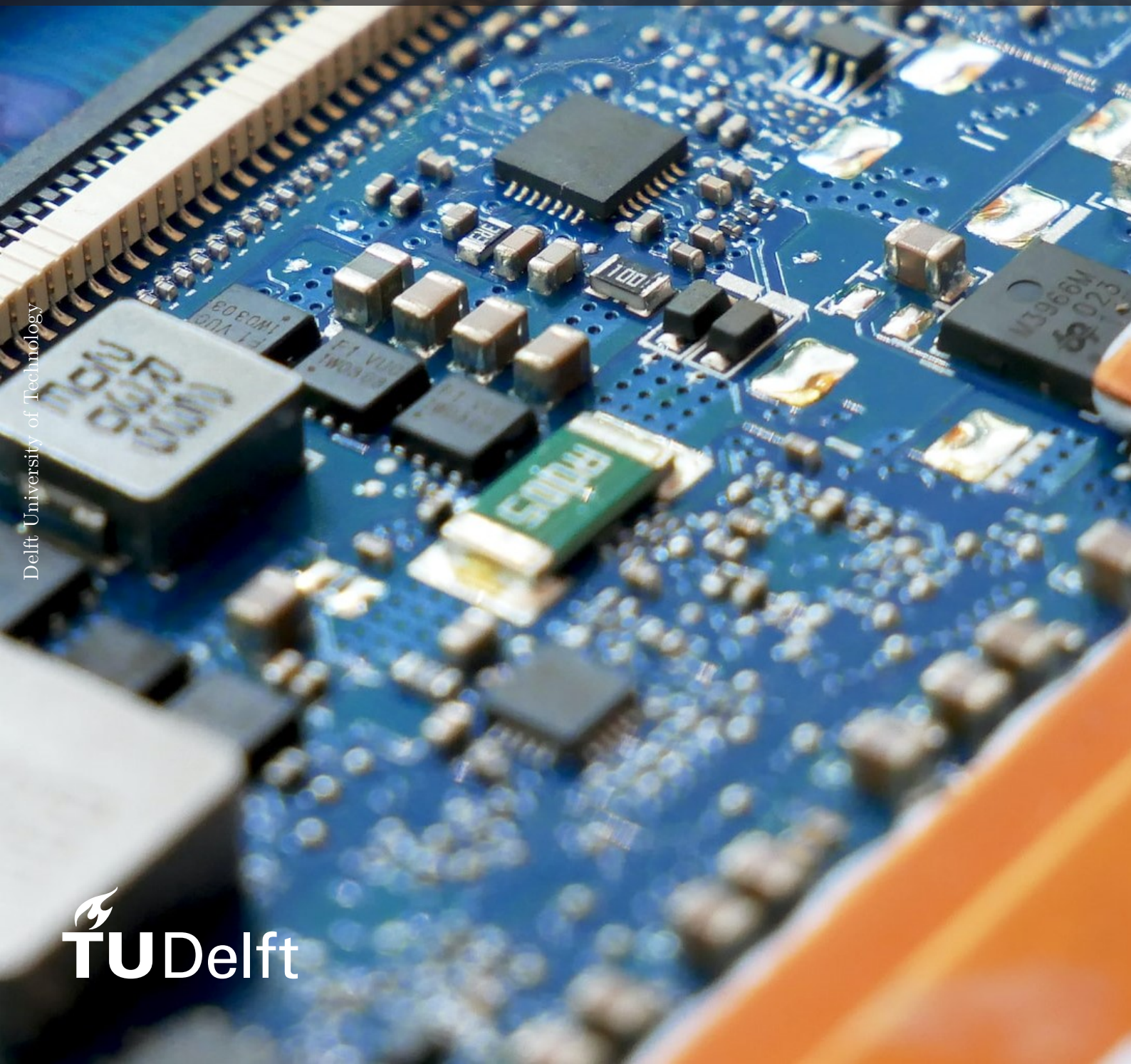

Delft University of Technology

TUDelft

Understand the Physics of Solder Joint Degradation in Board Level Reliability Vibration and Thermal Cycle Test

by

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TU Delft

PREFACE

Dear reader,

As my internship time at NXP Semiconductor draws to a close, I pause to reflect on the process of crafting this master's thesis. My entire thesis project was completed under the aegis of NXP. The aim of this endeavor was to understand the degradation process of solder joints, employing various measurement and sensing methods during board-level reliability tests. This project saw the development of effective methodologies, encompassing both hardware configurations and software solutions. The outcomes of this work hold promise in forecasting the lifespan of solder joints, eliminating failure due to solder cracks.

Throughout the journey of completing this project, I owe a profound debt of gratitude to a host of individuals who lent their guidance and unwavering support.

Firstly, my deepest gratitude goes to Prof. Willem van Driel. Without his guidance and the opportunity he presented for this internship, this journey would have been different. His passion and dedication have been a continuous source of inspiration.

I owe immense gratitude to Mr. Adwait Inamdar. Despite being in Delft, he has provided substantial assistance, spanning both academic guidance and administrative processes.

A special thank you to Dr. Jeroen Jalink, whose invaluable insights were the backbone of this project. I also received many administrative help from him.

To Mr. Varun Thukral, my daisy supervisor in NXP, whose commitment to setting time aside from his demanding schedule to deliberate on my project's progress, I'm immensely grateful. He can always provide insightful guides on my project and provide essential help. His fresh perspectives enriched this work significantly.

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The thanks to Mr. Stan Tielens and Mr. Paul van der Wel for their generosity in sharing their knowledge and experiences in measurement instruments gave me lots of sparks.

I wish to acknowledge the invaluable contributions of the Physical Failure Analysis team, notably Mr. Mohammed Achour, Mr. Eric Meeuwsen, Mr. Pieter Gommers, and Mr. Sander Wagemans. Their experience and hardworking progress were crucial to the project's outcomes. Also thanks to Dr. Abdellatif Firiti, Dr. Jinbo Wan, Ms. Hanxing Meng, Ms. Shuhan Yang, and Ms. Rianna Camille Ventura from the Electrical Failure Analysis team, they gave me a lot of assistants with the electrical measurement setup and helped me arrange the electrical instruments. The Package Innovation team, especially Dr. Jeroen Zaal and Dr. Michiel van Soestbergen, deserve special mention for their role in simulation modeling, and Mr. Geert de Cortie, Mr. Bob Knoppers from sample service for their hand-made solder cut and SMT.

To Dr. Hans Tuinhout, who generously shared insights, I extend my heartfelt gratitude. His contribution, particularly in providing samples was invaluable.

Lastly, I owe a profound debt of gratitude to all my educators who shaped my academic journey, and to my family and friends for their unwavering emotional and financial support.

Letian Zhang
Nijmegen, August 2023

Summary

Board-level reliability (BLR) looks at the reliability problem in the package and PCB interconnection, which is an important topic in microelectronics. The current criterion in the BLR test is to look if the connection is open, which can only detect the failure and there is no available method that can detect the degradation of the solder joints. This project mainly focuses on the degradation process of solder joints in board-level vibration tests and thermal cycle tests.

Two kinds of test vehicles are adopted in this project, one is a QFN56 package equipped with a four-wire resistance measurement circuit and the other one is a piezoresistive sensor, which can figure out the changes in stress distribution over two solder joints.

Special methods and test programs are developed tailored for the two aforementioned test vehicles, and some of the test results are collected and analyzed. Assisted by the failure analysis technique, the cross-section of the solder joint can be viewed and the crack length can be measured.

Findings in this study show the parameter shift during the solder joint degradation and also the mathematic model that describes the relationship between the crack length of the solder joint and resistance increment in electrical measurement. Moreover, with the statistical tools, we find the potential method that can considerably decrease the BLR test time by changing the failure criteria.

At the end of this thesis, the scope of this project is reviewed and an outlook of future work is proposed.

Contents

Nomenclature

Abbreviations

Abbreviation	Definition
BLR	Board-Level Reliability
CSV	Comma-Separated Values
CTE	Coefficient of Thermal Expansion
EBSD	Electron Backscatter Diffraction
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PXI	PCI eXtensions for Instrumentation
IMC	InterMetallic Compound
QFN	Flat No-leads Package
RDL	Redistribution Layer
SCPI	Standard Commands for Programmable Instruments
SEM	Scanning Electron Microscope
SMB	SubMiniature version B
SMT	Surface-mount technology
SMU	Source Measurement Unit
TC	Thermal Cycle
TCR	Temperature Coefficient of Resistance

Symbols

Symbol	Definition	Unit
a	acceleration	$[m/s^2]$
v	velocity	$[m/s]$
d	displacement	$[m]$
f	frequency	$[Hz]$
E	Young's modulus	$[Pa]$
h	thickness	$[m]$
F	force	$[N]$
R	resistance	$[\Omega]$
ε	strain	$[\mu m/m]$
σ	stress	$[Pa]$

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1 Introduction

In this chapter, the introduction of electronic packages and the role of electronic packages in our life are shown first in section 1.1. Then, the essential principles of microelectronics reliability and board-level reliability are introduced in Section 1.2, then follow-up by the relative board-reliability test methodologies, especially the state of the art of test methods adopted and researched in this project are shown in Section 1.3. Section 1.4 introduces different failure detection techniques for the test vehicles. Section 1.5 Summarize the outline of this thesis.

1.1. Electronic Package

Electronic packaging has been a key part of the semiconductor industry and has evolved over the last 5 decades. After the integrated circuit (IC) is fabricated and cut into the small die, it needs to be put inside an electronic package before goes to a real product. The main reason to use electronic packaging is to protect the silicon from being damaged and increase the reliability of the product. The package has the function of connecting the signal inside the die to the outside and managing and dissipating the heat generated by the die during operation [1]. With the development of the microelectronics industry, package technology has also developed and evolved. The requirement for package size, pin number, and reliability are also increased. The shape of the package is also developed from the leaded package to the lead-free package to meet this evaluated requirement. For the lead-free package, it can increase the component density of the electronic system because it can be soldered on both sides of the PCB without influencing the routing for inside layers of multi-layered PCB. In this project, two kinds of lead-free packages will be adopted and researched, one is the Quad Flat No-leads (QFN) package and the other one is Wafer-level Chip Scale Package (WLCSP). For the QFN package, because of the bug size, it's easier to manufacture and assemble. WLCSP is defined by the standard in [2] which states that the size of the package should not be a lot bigger than the chip. Because of the small pins, WLCSP can provide more solder joints in the same area and the parasitic effect caused by wire bounding can be decreased due to shorter wiring. As a result, the manufacturing requirement can also increase.

1.2. Microelectronics Reliability

This section will discuss the reliability theory and the classification of microelectronics reliability. Moreover, some common test methods in board-level reliability tests will also be discussed.

1.2.1. Theory of Reliability

Reliability problems refer to the consistent performance and dependability of a process over time. It denotes the process can consistently can give the same results under the same conditions. In engineering, the reliability problem is often associated with some methods to accelerate failure by loading controlled mechanical or thermo-mechanical stress. Knowing the failure situation under accelerated experiments, with proper modeling, we can predict the lifetime of the same product under real application environments. To describe the life of a product or system, we need to use some mathematics theories and expressions. The lifetime of the product can be predicted with a failure distribution function based on the experimental test data.

In mathematics, if the product only has two states: good and fail; we can use the probability density function $f(t)$, as the probability density of the product failure rate at any given time. The corresponding failure rate function over time $F(t)$ can be obtained by integrating this probability density function[3]:

$$F(t) = \int_0^t f(x)\,dx (0 \leq x \leq t) \tag{1.1}$$

For this kind of exclusive event, with probability theory, we can easily know the reliability function $R(t)$:

$$R(t) = 1 - F(t) = 1 - \int_0^t f(x)dx (0 \leq x \leq t) = \int_t^\infty f(x)dx \tag{1.2}$$

The relationship between the failure rate function and the reliability function is also shown in figure 1.1.

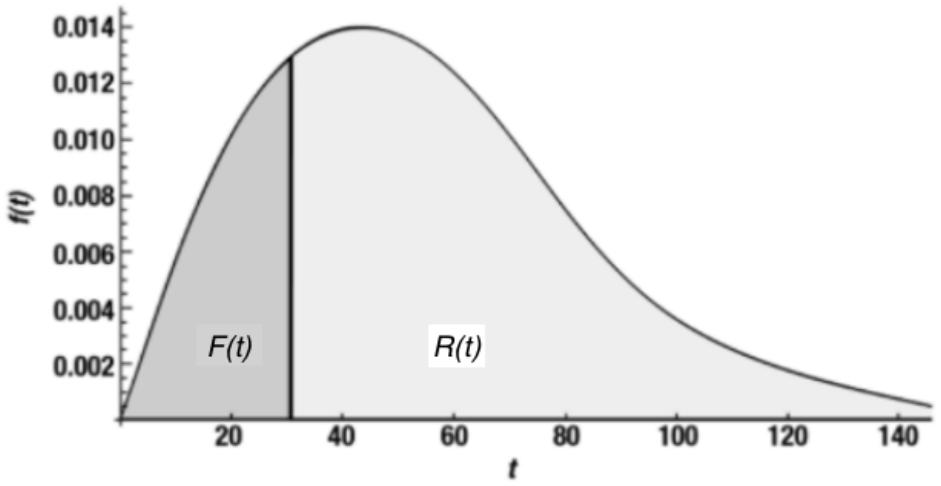


Figure 1.1: Relationship Between Probability Function and Reliability Function [3]

We can also calculate the hazard rate $z(t)$ of one product, or the condition failure density, which is used to describe the probability of failure in a certain moment. It can be calculated by:

$$z(t) = \lim_{\Delta t \to 0} \frac{F(t+\Delta t) - F(t)}{\Delta t} \frac{1}{R(t)} = -\frac{1}{R(t)} \frac{dR(t)}{dt} \tag{1.3}$$

In equation 1.3, if the hazard rate is a constant number, which means in each time, the failure probability is always the same, we can be called the hazard rate as failure rate λ, and the distribution of this product will be negative exponential distribution.

To improve the accuracy of the experiments and bring the experimental results closer to the real situation, and also to better understand the different failure modes, we should use a certain

number of samples for reliability tests. Based on the reliability test result of these test samples, we can use statistical methods to know the reliability function of the experimental dataset.

After getting the failure distribution function and parameter value, there is still another step to predict the real lifetime in applications. We can use the physical models to fill this gap. As most reliability tests can accelerate the failure process, these physical models we used are also called accelerated test models. However, this prediction is based on two assumptions. One is that the failure mode in experimental conditions is the same as that in actual applications. The other is that the mechanism causing this failure mode is identical. That is to say, every phase from the intact state to the failure state should exhibit the same characteristics.

1.2.2. Microelectronics Reliability Classification

Microelectronics reliability is focused on the reliability problem in the microelectronics area, which can also refer to the ability of a microelectronics device or a system to consistently perform a specified function under given conditions over a designated period. This requires that components do not fail or degrade to an unacceptable level throughout their intended life. The robustness of these devices is largely dependent on the quality and consistency of the materials used, the accuracy of fabrication processes, and the resilience of the devices to various operating conditions such as temperature changes, mechanical stress, radiation, and electrical load. We can divide microelectronics reliability into different levels, as shown in figure 1.2, these levels are package-level reliability (or first level), board-level (second level), module-level (third level) and system-level (fourth level) reliability [4], the propose and target of each of these levels are different.

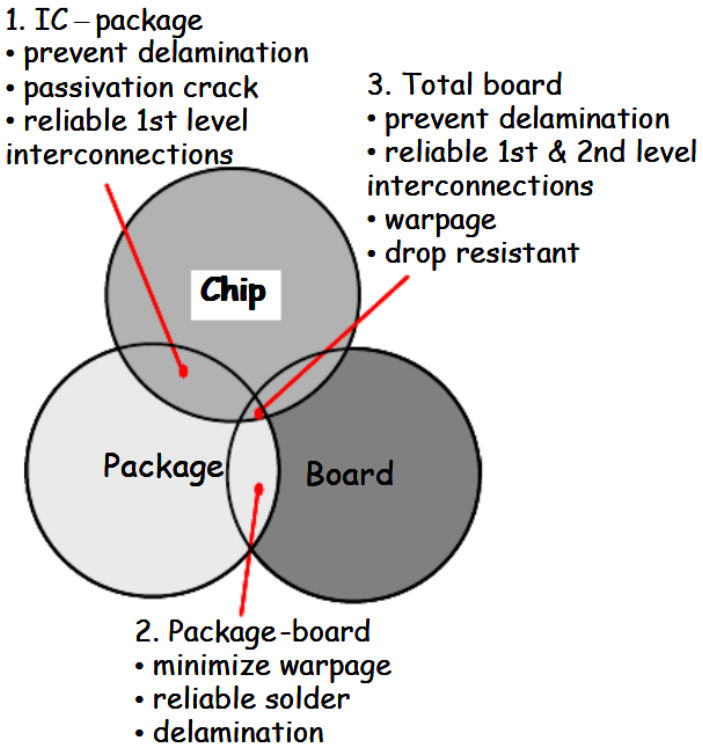


Figure 1.2: Different categories of microelectronics reliability [4]

As shown in figure 1.3. Package-level reliability primarily focuses on the durability of the electronic package, assessing its robustness in adverse conditions. However, this evaluation does not encompass the methodology employed for mounting the package on the PCB or the

rigidity of the package-PCB interface. Board-level Reliability (BLR) also called solder joint interconnect reliability, mainly focuses on the reliability issues of the interconnections between the package and the PCB [5], the main research focus of board-level reliability is on solder joints. Module-level reliability and system-level reliability are at even higher levels, which evaluate the reliability of the single module or the whole system. Failures at the module or system level can originate from inadequacies in solder-level reliability. By initially assessing board-level reliability when testing a module's reliability, we can establish a reliability margin for the PCB interaction. This ensures that any detected failures arise at the module level rather than being attributed to the board or package level failure. As a result, doing research on lower hierarchic levels of reliability like BLR can always be important.

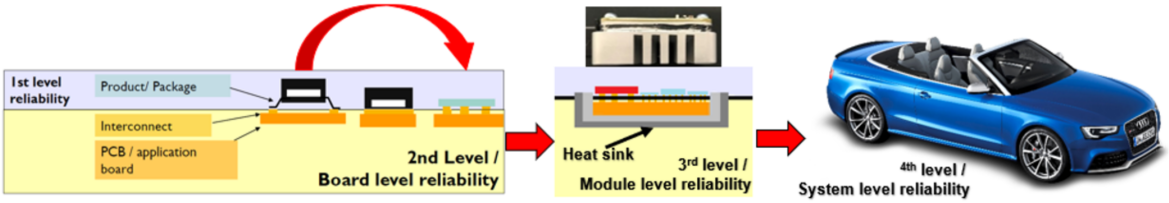


Figure 1.3: Schematic diagram of Different Level Reliability [6]

1.3. Board-level Reliability Test Methods

We stressed the PCB in a controlled manner, with the package to test the reliability of the solder joints using various methods. The BLR test methods mainly can be divided into two types: mechanical and thermo-mechanical tests. To elaborate, it contains a thermal cycle test, thermal shock test, bend test, vibration test, and drop test. In this study, some of these test methods will be involved which will be introduced in this section.

1.3.1. Thermo-Mechanical Test

The thermo-mechanical test is an important reliability test method to test if the product can meet the qualification requirements [7]. The thermo-mechanical test is a method to accelerate the failure caused by the temperature change during the product's whole life, which can lead to the failure of the interconnection between the package and PCB. This kind of failure mode can account for big proportions in the failure mechanisms [8], [9]. Thermo-mechanical tests primarily fall into two types: thermal cycle tests and thermal shock tests.

For the Thermal Cycle test (TC), PCBs are secured inside a thermal cycle chamber. Throughout a single cycle, the internal temperature undergoes four distinct phases: an ascent to a higher temperature, a high-temperature dwell, a descent to a lower temperature, and a low-temperature dwell. During the dwell phases, the temperature remains stable for a specified duration, ensuring that the solder joint's temperature becomes uniform and reaches the targeted level.

For the Thermal Shock Test, while this test also subjects the PCB to varying temperatures, its distinguishing factors are the ramp rate and soak durations. A thermal shock tester comprises a dual-chamber system: one chamber consistently maintains a high temperature, while the other retains a low temperature. The abrupt temperature transitions are facilitated by physically relocating the PCB fixture between these two chambers, resulting in a swift environmental temperature shift.

In essence, while both tests expose PCBs to fluctuating temperatures, the rapidity of temperature transitions and the approach used differentiate them.

In this project, we have also incorporated another thermo-mechanical test method, specifically a temperature-coupled bend test. Essentially, this method involves conducting a bend test within a temperature chamber. The chamber allows for ambient temperature modulation. Once the thermocouple, attached to the PCB, indicates the target temperature, the bend test commences, and relevant measurements are taken. Subsequently, the temperature is readjusted, paving the way for the next bend test iteration.

1.3.2. Vibration Test

The vibration test is a BLR test method that gives desired vibration movement to the PCB to realize a controlled mechanical load to the PCB. The hardware setup of the vibration test is shown in figure 1.4 , which includes the vibration controller system, amplifier, shaker and fixture with pillar, and control accelerometer fixed on.

The amplifier system contains some transformers that can generate very high currents with the desired frequency, there are also coils under the shaker that can generate a magnetic field by the time-varying current from the amplifier. Then, the shaker initiates vibrations under the influence of this oscillating magnetic field. The amplitude of the shaker vibrations is dictated by the magnitude of the drive current from the amplifier, while the frequency is contingent on the frequency of the magnetic field itself. Simultaneously, a fixture is affixed to the shaker armature with screws. This fixture is tailored to the PCB in use as an adapter, with dedicated screw holes designed for fixed into the shaker and pillar attachment. The purpose of the four pillars is to clamp but float the PCB and avoid contact between the PCB and the fixture. Only the four screw holes on the corners of the PCB are fixed to the pillars with the screws, the other part of the PCB can move up and down, which enables free vibration of the PCB.

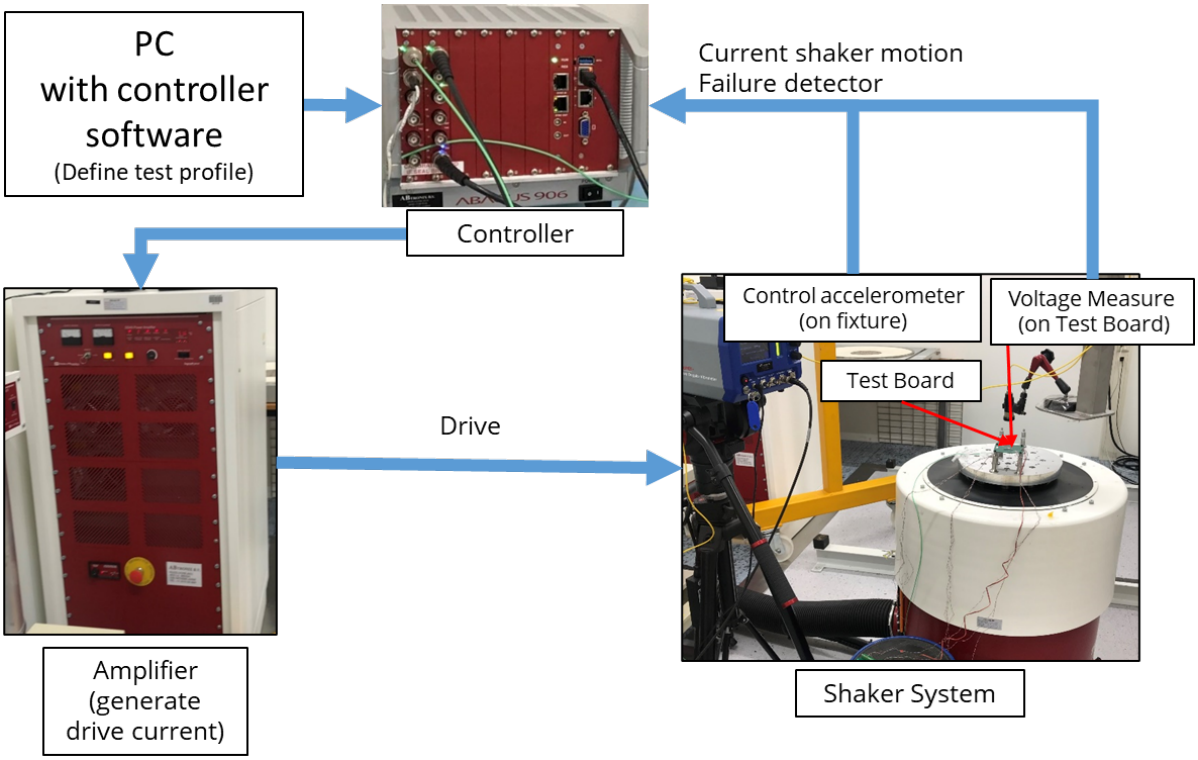


Figure 1.4: Schematic diagram of Vibration Test

As the load of the shaker can differ from the different fixtures and PCB. To ensure that the amplifier delivers the appropriate current, thereby guaranteeing the shaker's vibration

amplitude and frequency align with our required setup, we must have precise control over the conditions of the shaker's vibrations. The controlled feedback loop inside the vibration setup is important. The amplifier, control accelerometer, and vibration controller can form the control feedback loop. The control accelerometer fixed on the fixture can monitor the motion of the fixture, both the vibration frequency and the acceleration can be monitored and sent to the vibration controller. The controller can check whether the frequency and acceleration can meet with the user profile provided by the vibration program on the connected PC, and send further commands to the amplifier to adjust or maintain the magnitude and frequency of the output drive current.

The vibration frequency sweep method contains three methods: sweep sine, random frequency test, and dwell test. The sweep sine test is the test that the fixture only vibrates in a single frequency at a certain moment with desired acceleration. This technique serves to characterize the PCB's dynamic response. Paired with another motion detection method targeting the PCB's center, the approach involves the execution of a swept sine across a specified frequency range. This continuous monitoring of the PCB's center motion enables the capture of the resonance frequency, which is the time that the PCB exhibits maximal acceleration. The ratio of the PCB's peak acceleration to the fixture's acceleration is termed the "transfer factor", as referenced in [10]. Random frequency vibration test combines all the input frequencies at the same time, which is closer to a real application, but as it can excite multiple resonance modes, analysis can be difficult. The dwell test fixes the input frequency to one point, the shaker always shakes at a single frequency. But because the PCB resonance frequency can shift with aging, the dwell test cannot always be fixed to the resonance frequency.

The vibration test user profile can be assigned by the PC with controller software which is connected to the vibration controller, in most cases for sweep sine, the test program contains the vibration energy level or acceleration, vibration frequency range, and sweep rate. Vibration energy is quantified by the acceleration of the fixture, which directly influences the stress imposed on the PCB. An increased input acceleration can hasten failure; however, it also poses a risk of altering the PCB's failure mode or even causing direct damage. Conversely, excessively low input acceleration can prolong the test duration before a failure is observed.

The user profile can also assign the abort condition, which can be a command to stop the shaker when one of the measurement values exceeds a specific range, which can be used for stopping the shaker once we see failure in the PCB. In our experiment in this project, mainly sweep sine will be adopted as it can also characterize the resonance frequency of the PCB and always load the PCB in the range near resonance frequency.

1.3.3. Bend Test

Bend tests usually need an experimental setup as shown in figure 1.5, which includes a fixture system (load fixture and support fixture) that is directly in contact with the PCB under test, motor (or accumulator), and track can drive the load fixture and give bending force. The motor can also be used to measure the force on the load fixture and the displacement. The track is perpendicular to the specimen, which means that in the bend test, the motor can only move in a direction that's vertical to the specimen and give a uniaxial force.

With different fixtures, the bend test equipment can adjust the support span and different bend test methods, for the three-point bending test, only one contact point is needed for the load fixture, and the location of the load fixture should be in the center of the two support fixture. For four-point bending as shown in figure 1.5, the load span can also be adjusted by different requirements.

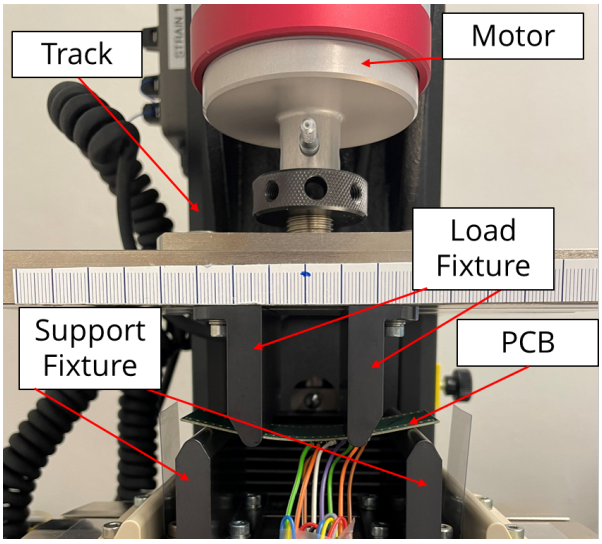


Figure 1.5: The experimental setup used for four-point bending tests

1.4. Failure Detection in BLR Tests

To monitor the situation of the solder joints during the board-level reliability test, in industry, a daisy chain can be adopted [11], [12]. A daisy chain is a conducting link that can cover all the connections between the package and the PCB, all the solder joints will be connected into a chain and the chain will show a high ohmic resistance once one of the solder joints shows open. Connect the daisy chain in series with a resistance and power supply, and continually monitor the voltage between the daisy chain during the reliability test. We can notice failure happens when the voltage between the daisy chain becomes as high as the power supply voltage. Whenever the daisy chain voltage is higher than the threshold voltage, we can call that an event. For different reliability tests, we can define the failure by counting the events. This approach consistently produces reliable outcomes and is supported by well-developed, related instruments. It's commonly used in industry in failure detection in board-level reliability tests. This method is not intended for measuring degradation. Therefore, this project aims to explore and investigate other advanced methods for detecting failure along with capturing degradation.

1.5. Outline

The rest of this report will be organized as follows:

- Chapter 2 gives the literature review related to the theory of board-level reliability test and the theory of measurement method during board-level reliability. The stress characterization of the package and potential sensor that can be applied to board-level reliability tests is also reviewed. Furthermore, the degradation and reliability prediction methods and promotional parameters that can be adopted are also reviewed. Lastly, the research motivation of this thesis is presented.
- Chapter 3 introduces the methodologies adopted by this project. Electrical degradation measurement methods development and improvement and physical degradation parameter measurement sensor comparison and characterization are also discussed. The working process of the adopted sensor is also shown in this chapter.
- Chapter 4 describes the reliability test process and failure analysis result. The board-level reliability test setup, test method development, and test result are discussed in this chapter. The test result from the microscopic physical level from failure analysis is also

shown in that chapter. The corresponding finding and relationship between the BLR test and failure analysis results are discussed.

- Chapter 5 contains the conclusion of this project and recommendations for further work.

2

Literature Overview

This charter will focus on the theory related to board-level reliability test theory and literature on stress distribution on the die after the packaging process. Some applications using sensor measurement results on degradation prediction and diagnose of microelectronic devices are also reviewed.

2.1. BLR Test Theory

When conducting board-level reliability tests, it is important to have a grasp of certain physical theories in order to properly set the parameters of the test profile. This section will review some of the fundamental formulas that are frequently utilized in board-level reliability testing.

2.1.1. Vibration Test Theory

In the vibration test, the resonance frequency, acceleration, peak displacement and peak velocity, and strain on the PCB are important, for these parameters, we can do some basic calculations on them.

Acceleration, Displacement, and Velocity

During the vibration test, if we assume the vibration is in dwell mode, the shaker can vibrate with controlled sinusoidal movement, which can be described by the following equation (sourced from [13]):

$$x = X_{max} \sin(\omega t) \tag{2.1}$$

Where x is the displacement of the shaker, X_{max} is the maximum movement of the shaker, ω is the angle frequency of the shaker and t is time. In industry, we commonly use the peak-to-peak displacement d as a parameter, which can be calculated by:

$$d = 2X_{max} \tag{2.2}$$

By differentiating the displacement x, we can calculate the velocity and acceleration of the shaker:

$$v = \frac{dx}{dt} = \omega X_{max} \cos(\omega t) \tag{2.3}$$

$$a = \frac{dv}{dt} = -\omega^2 X_{max} \sin(\omega t) \tag{2.4}$$

We also know the relationship between angle frequency and frequency:

$$\omega = 2\pi f \tag{2.5}$$

In the vibration test, the frequency f is what we commonly used. By combining equation 2.1 to 2.5, we can know the relationship between acceleration, vibration frequency, and peak-to-peak displacement is:

$$d = \frac{a}{2\pi^2 f^2} \tag{2.6}$$

When doing the vibration test on the PCB, the acceleration of the PCB at the center part is usually different from the shaker acceleration. The ratio between the shaker acceleration and the PCB acceleration is the transfer factor of acceleration[10]. In most cases, we only measure the PCB peak acceleration and resonance frequency, to know the peak-to-peak displacement of the PCB and the peak velocity of the PCB, we can use equation 2.6 and equation 2.7.

$$v = \pi f d \tag{2.7}$$

Resonance Frequency of PCB

According to Steinberg [13], we can assume the PCBs are flat rectangular plates. The resonance frequency of the PCB can be calculated by a sample model in that a rectangular plate is fixed by four edges. The boundary condition of the flat rectangular board is shown in figure 2.1, in which a and b are the length and width of the PCB respectively, and $4Z_0$ is the displacement of the PCB at the center part. With this boundary condition, we can know at the first order resonance frequency, the PCB plate can meet with the geometric deflection condition:

- at $X = 0$ and $Y = 0$, we have $Z = 0$
- at $X = a$ and $Y = 0$, we have $Z = 0$
- at $X = 0$ and $Y = b$, we have $Z = 0$
- at $X = a/2$ and $Y = b/2$, we have $Z = 4Z_0$

If we assume the x and y direction motion of PCB are independent, then in each direction, the PCB motion will follow the wave equation, and the solution to this partial differential equation follows sinusoidal distribution, we can also assume the total displacement is the combination of these two directions, for an arbitrary point in the plate, if we only consider the first resonate point, the displacement of the rectangular PCB is as follow (sourced from [13]):

$$z = 4Z_0 \times \sin(\frac{\pi x}{a}) \sin(\frac{\pi y}{b}) \tag{2.8}$$

We can verify if equation 2.8 is correct by putting the boundary conditions inside the equation 2.8 and checking if the equation can be satisfied. Moreover, if we consider the energy of the plate does not dissipate, which means the sum of kinetic energy and strain energy will stay constant, and they can transfer with each other. With some further calculation and considering the property of the PCB itself, we can know the resonance frequency of PCB can follow equation 2.9.

$$f = \lambda(\frac{1}{a} + \frac{1}{b})\sqrt{\frac{E \times h^3}{12 \times \rho(1 - \upsilon^2)}} \tag{2.9}$$

λ is a constant which depends on the clamping condition, a and b are the length and width of the PCB as mentioned previously. E is Young's modulus of the board, υ is the Poisson ratio of the board, h is the PCB thickness, and ρ is the density of the board.

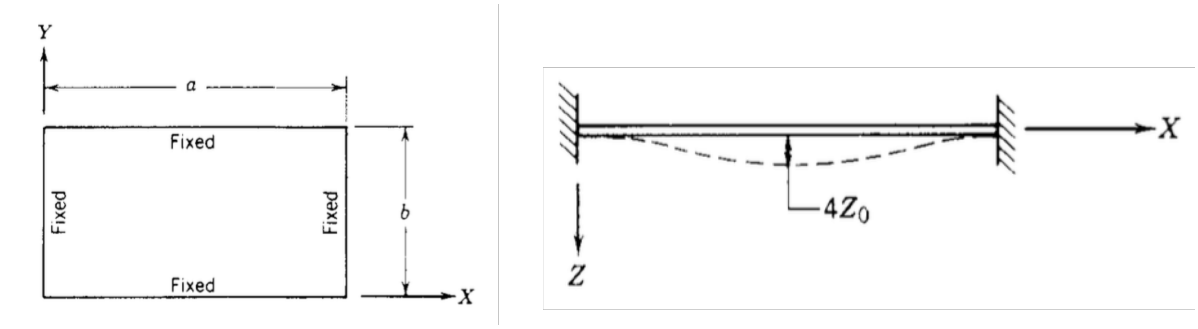


Figure 2.1: Boundary Conditions Used in Calculate PCB resonance frequency ($X-Y$ View and $X-Z$ View.[13]

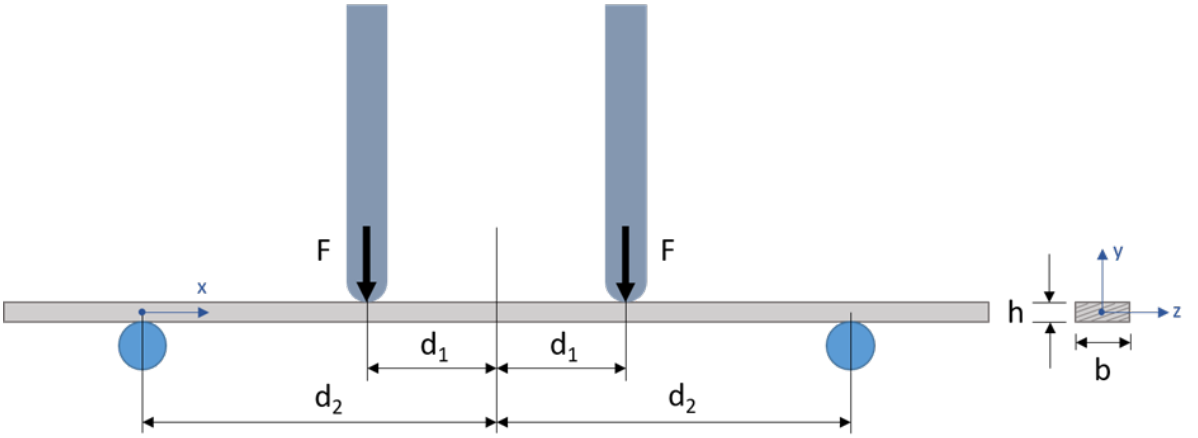


Figure 2.2: Schematic diagram of 4-point bending

2.1.2. Bend Test Theory

In the bend test, we can consider the PCB as a uniform beam. With beam theory [14], we can know the bending moment and the shear force at the cross-section of the PCB (beam). There are usually two kinds of bending methods for a bend test – three-point bending and four-point bending. The main difference between these two methods is that for four-point bending, the region between the two load pins have the same stress profile at any cross-section across the span.

A schematic picture of the four-point bending is shown in figure 2.2, in that figure, the load span is $2d_1$ and the support span is $2d_2$, the thickness of the specimen is h and the width of the specimen is b. With classical beam theory, we can calculate the area moment of inertia at the cross-section of the beam if we treat the beam as a rectangular specimen[14]:

$$I_z = \frac{bh^3}{12} \tag{2.10}$$

We can also draw the shear diagram and moment diagram of the beam in figure 2.3. We can see the moment diagram value between the two loading pins stays stable, then we can know the bending stress:

$$\sigma_{xx} = \frac{M}{I_z} y \tag{2.11}$$

We can know the max bending stress at the top layer of the beam ($y = h/2$):

$$(\sigma_{xx})_{max} = \frac{M_{max}}{I_z} y = \frac{6}{bh^3} F(d_2 - d_1) \tag{2.12}$$

Then we can know the value of the stable stress at the mid-span of the beam, i.e., the region between the two load pins. It's important to notice that equation 2.12 is only valid on the ideal beam, for a PCB, especially a PCB with components, using this equation to calculate the stress on the component may only provide a preliminary estimate.

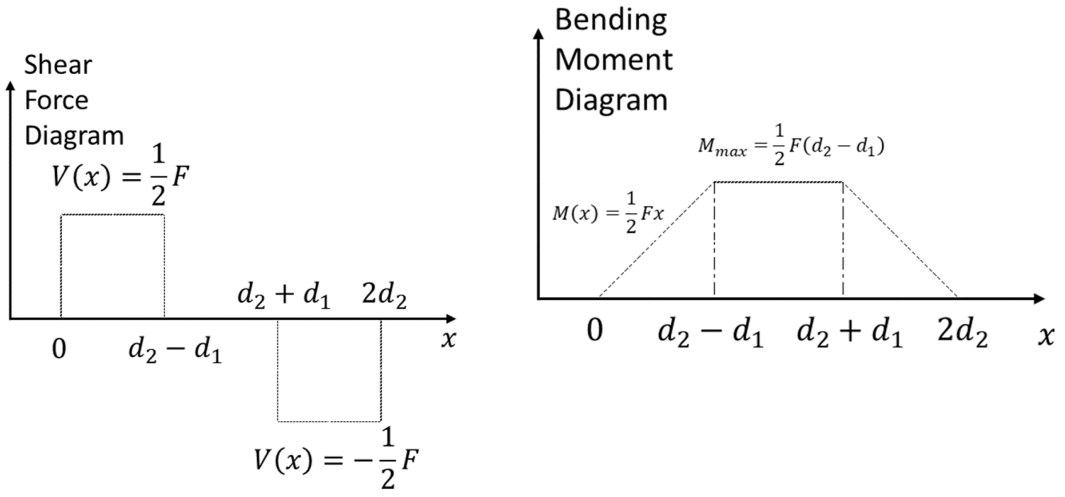


Figure 2.3: Shear force diagram and bending moment diagram of the beam. [14]

2.2. Recent Studies on Board-level Vibration Setup

In this section, literature related to board-level reliability test are reviewed. It comprised the research in the test specification, vibration test method, and failure criteria used in the industry.

For the current study of board-level vibration tests, on the component level, international standards and specifications are available such as JEDEC [15] and ISO [16]. However, there is no available standard for board-level vibration tests. To access reliability risk during the board-level reliability vibration test, different parameters during the vibration test needed to be accessed and the influence of these parameters will be reviewed. In [10] the influence of environment conditions and test parameters can influence the PCB dynamic response. It shows that the environment humidity, sweep rate in sweep sine vibration, and cable wire have a low influence on the resonance frequency and peak-to-peak displacement. In [17] the factors influencing the dynamic response of the PCB are studied. The result shows that changing the package and mounting an accelerometer can both influence the resonance frequency and peak acceleration.

For the measurement method of PCB motion during vibration test, accelerometersis the most commonly adopted sensor [15], [17], [18]. In [19] the PCB motion during vibration test is measured by LASER Doppler Vibrometer (LDV). LDV is a contactless method that can measure the resonance frequency and velocity of the PCB, which has a similar effect as an accelerometer after doing some sample calculations. In [16], [20], strain gauges are mounted on the PCB to measure the strain of the PCB and shift in resonance frequency. The strain gauge can be used to measure the deformation of the board. When PCB is deformed, the resistance of the strain gauge that is mounted on the PCB surface can change respectively, by using a bridge circuit to accurately measure the resistance change, together with the strain factor of the strain gauge [21], the strain value on the surface of the PCB can be measured. The strain value is defined by the increased length of the measurement area compared to the area length. However, less literature discusses the advantages and disadvantages of these measurement methods during

board-level reliability vibration test, and a comparison of these three measurement methods will be discussed in section 3.3.1

The paper [22] examines nonlinearity in vibration tests, noting that every system inherently displays nonlinear behaviors due to factors like geometry, material properties, or damping. During sweep sine vibration tests, the sweep rate and sweep direction can significantly influence nonlinearity. To mitigate the effects of cubic nonlinearity that commonly occur on resonance frequency, the study suggests keeping a lower input acceleration and ensuring the frequency sweep allows the system enough time to stabilize. However, even with these measures, factors like sweep direction can introduce discrepancies, leading to potential increases in the measured resonance frequency due to hardening cubic nonlinearity.

2.3. Studies on Thermal Cycle

There are already available standards for thermal cycle tests such as [23], [24], which we followed in this standard. Specifically, the temperature range we used is $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$, and with a dwell time of 10-15 minutes, the ramp rate is less than $25\,^{\circ}\mathrm{C}$/minutes.

Though thermal cycle reliability test methods are commonly used, there is no available literature discussing the stress undergone by the component during the thermal cycle test. Moreover, there are only limited publications on doing in-situ resistance or stress monitoring during the thermal cycle process. Among the available ones, only a few discuss the prognostic methods for solder joints.

2.4. Studies on Stress Sensor

One of the methods to directly measure the stress undergone by the silicon die can be using a stress sensor, in this section, different stress sensors are reviewed and discussed and related equations are shown.

One common stress sensor design is using piezoresistive cells which are fabricated as a rosette structure [25]–[29], as it looks like the strain gauge, this type of stress sensor also called semiconductor strain gauge, with different types of doping, wafer plane, and special angles orientation of rosette cell, this kind of stress sensor structure is capable of measuring all three stress components in a plane. The stress value can be calculated with the resistance change in different directions and different doping types. The stress is a second-order tensor with 9 components:

$$\bar{\bar{\sigma}} = \begin{pmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{pmatrix} \tag{2.13}$$

Where in most cases, we have a symmetric stress tensor, which has 6 independent terms because of the following relations:

$$\begin{aligned} \sigma_{12} &= \sigma_{21} \\ \sigma_{13} &= \sigma_{31} \\ \sigma_{32} &= \sigma_{23} \end{aligned} \tag{2.14}$$

To obtain complete information on the stress tensor, we need six linearly independent variables, which means we need two types of doping, and the rest of the three can be calculated by fabricating the sensor on (111) wafer, with 22.5° off-axis angle. The relative change of resistance in the piezoresistive cell can be written as [26]:

$$\frac{\Delta R}{R} = \Sigma_{\alpha}(\pi_{1\alpha}\sigma_{\alpha}l_1 l_2) \tag{2.15}$$

Where π value is the piezoresistive coefficients, related to the orientation inside the wafer and different types of doping, a reference value of piezoresistive coefficients can be found in [26]. σ is the stress value of different directions, α is the constant number from 1 to 6, which is the elements in the stress tensor, and l_1 and l_2 are direction cosines of the resistance orientation with the axis of the wafer. With some matrix calculation and angle transform, we can calculate the stress value with resistance change.

This kind of stress sensor can easily be fabricated at the surface of the wafer with a conventional process, it was widely used as a method to measure the surface stress state of the die inside the package. This type of sensor can be used to detect delamination and adhesive cracks within a package [26], [30]. However, there are some drawbacks of this stress sensor, first because of the fluctuations in the manufacturing process, precise calibration is necessary to calculate the undergo stress value. Secondly, since the resistance of the piezoresistance cell is sensitive to temperature changes, this calibration must also be performed at different temperatures. Another significant disadvantage is that these sensors occupy a large area, and different rosettes cannot always be fabricated on top of the solder, making it difficult to measure stress in the region directly above the solder joints.

Another type of stress sensor is also using piezoresistive cells, but it trades off the capacity to measure the value of the stress tensor with a decrease in the size of each cell. The stress sensor adopted in this project uses 2100 n-mono resistance cells distributed under two solder joints of WLCSP [31]. By simply comparing the change in conductivity of each of the cells to the value from the region far from the bump, a relative conductivity change pattern can be found, and the color pattern can be generated by the value. The color pattern is indicative of stress experienced by the component. By looking at the drift of the color before and after bump forming and PCB mounting, the author can find the stress distribution during these processes. The sensor result can also be used to trim the oscillator to decrease the variance of the result [32] and characterize the mismatch due to chip encapsulation [33]. In this project, the same sensor will be used during board-level reliability tests to capture the degradation of solder joints. The development of the test method can be seen in section 3.3.2.

2.5. Studies on Component and Solder Joint Degradation Prediction

There are already different packaging degradation prediction methods in the reliability of package level, such as in [34], the author used the thermal cycle method to accelerate the failure at the component level and use test vehicles that contain 3 rosette stress sensors. The result gives a part of the PHM (prognostics and health management) framework, which consists the data acquisition, data manipulation, health assessment, and damage quantification. The reference [30] provides some improvement and a machine learning algorithm, the author used thermal shock and designed a low strength package to accelerate some test vehicles with piezoresistive sensors in Thin Quad Flat Packages (TQFP). The in-situ measurement result can be transferred to the host and data processing. By using machine learning models to regress the measurement data and created a backpropagation neural network that gives a way to estimate the delamination. In [35], the author used the thermal shock test and use MOS based piezoresistive stress sensor to add the capacity of measuring out-of-plane stress. The new stress state information and the new machine learning model are capable to predict the delamination area location with high accuracy.

In [20], the author looks at the relationship between board strain and cycles to failure on solder joints, it uses a strain gauge on the PCB as an alternative to the solder joint strain. And it gives a rainflow algorithm-based method to predict the initiation location and direction of the crack in the BGA package. The application of these algorithms can be used to develop a health management model on products to access their reliability, which can be used for identifying the

part with high risk and long-term part-based warranty return data can be used to evaluate and select suppliers[36].

2.6. Motivation and Problem Statement

First, it has been established that the board-level reliability vibration test and thermal cycle test are critical methods to test solder joint reliability, but the physics of degradation for solder joint-PCB interface during board-level reliability test is not fully known. Moreover, the characterization of a degradation parameter during the board-level vibration test is not clear.

Secondly, the prevalent failure detection methods in both the vibration test and the thermal cycle test fall short in capturing the degradation process. The daisy chain structure further complicates the matter, making it impossible to directly monitor individual solder joints. To date, there is a lack of published methods that offer accurate resistance measurements indicative of solder joint degradation during board-level reliability tests. Furthermore, the critical corner solder joint's specific location and the QFN package's failure mode during such vibration tests are not clearly defined. Pertaining to the QFN package, there is an absence of a degradation model, particularly information concerning the failure-free region and activation energy during board-level reliability testing.

Piezoresistive stress sensors are available to monitor the stress on the die surface but the working temperature is critical and the size of the rosette stress sensor is not capable to measure the stress value under the solder joint. With the improved piezoresistive stress sensor, we are capable to measure a scale of less than one solder bump but there is no available publication that correlates the stress change to solder joint degradation.

There has been some research done on using stress parameters to define package delamination and utilizing those parameters to predict the delamination happens. However, there is a lack of research in defining methods and parameters to monitor and reflect solder joint degradation. This thesis aims to develope such a method, which in turn can improve the board-level reliability assessment significantly.

3

Methodology

This chapter gives a description of the methodology used in the development of board-solder degradation process measurement. The available test vehicles introduction is stated in section 3.1, electrical measurement requirements, methods, and improvement are discussed in section 3.2, the physical parameter used vibration are discussed in section 3.3, the comparison of these sensors and characterization are also shown in section 3.3. A flow chart to describe the whole process of this project is shown in figure 3.1.

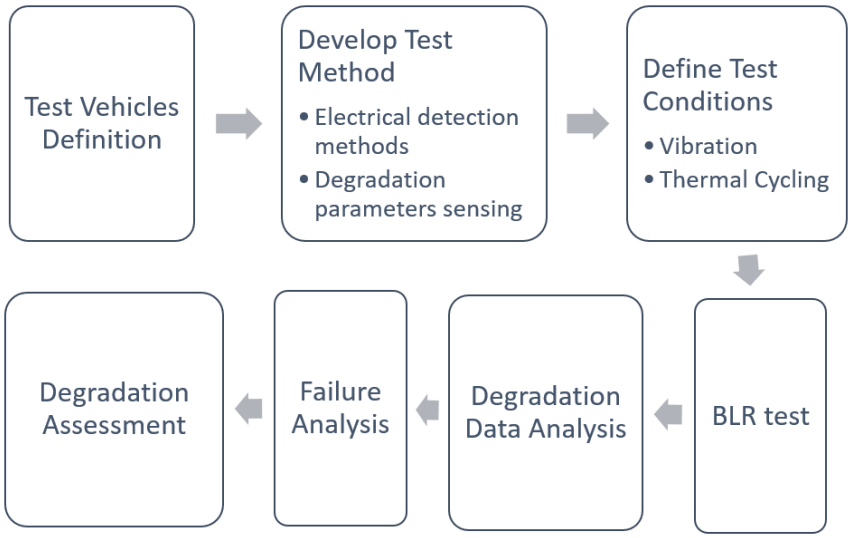


Figure 3.1: The flow chart of the methodology developed in this project

3.1. Test Vehicles

Test vehicles are circuits or ICs which are designed for evaluating the device characteristics [37]. In this study, two types of test vehicles with different packages are used.

The first test vehicle is PCB with QFN-56 package. Three components are mounted on the middle three places of the standard PCB used for drop test according to JEDEC standard [11], as the figure is shown in figure 3.2. In each corner of the PCB, a 4-wire the measurement circuit is embedded as shown in figure 3.3b, which can measure the resistance of one corner solder joint. The zoom-in picture of one component is shown in figure 3.3a, all of the four pins

are connected to the solder pads on the short edge of the PCB. The same 4-wire measurement structure is shown in all eight corner solders, so in total 24 test samples are available one PCB.

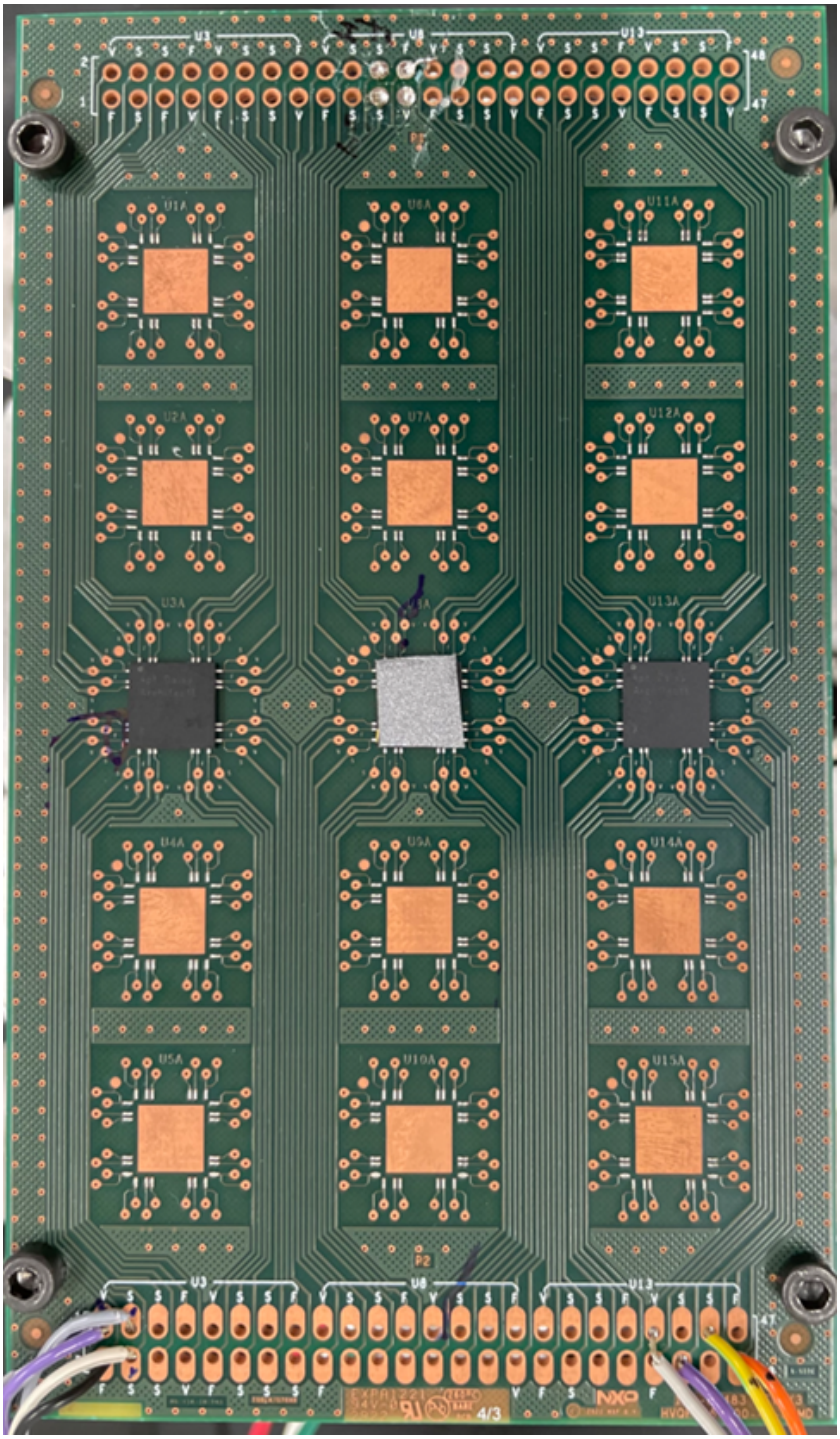
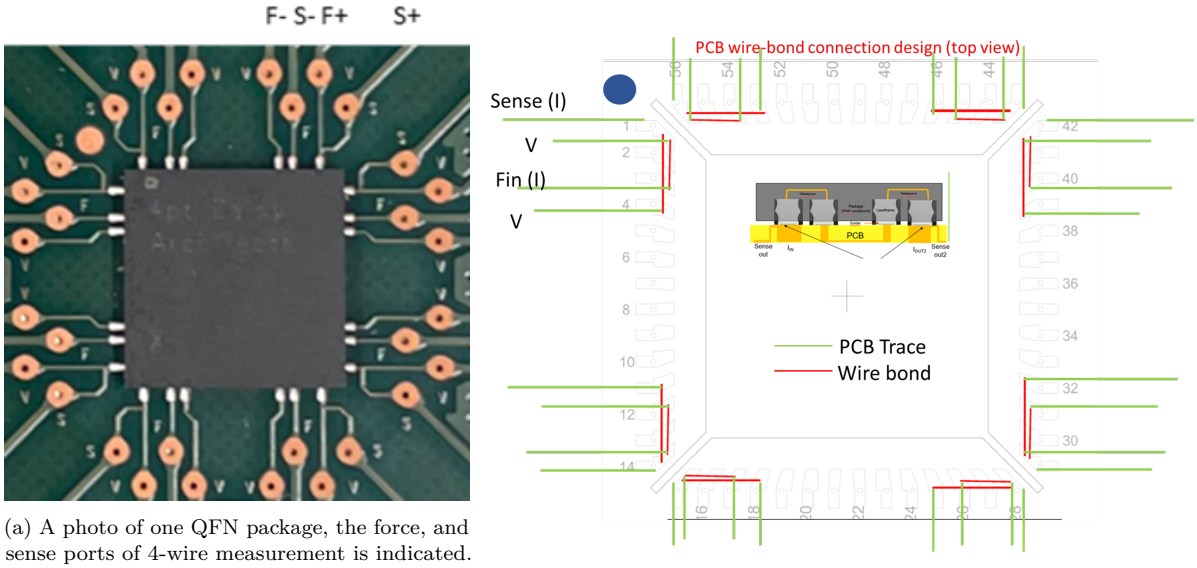


Figure 3.2: QFN package test vehicle PCB, side A where only corner solder joints are connected. The layout are follow [11]

The PCB has two sides, the difference is that on side A, as shown in figure 3.2, only three solder joints are connected to the PCB in each corner, for the rest pins, as well as the larger center pads (EPAD) are not connected to the PCB. This design accelerates failures, thereby reducing the time required for our characterization process. The other side (side B) uses



(a) A photo of one QFN package, the force, and sense ports of 4-wire measurement is indicated. This component is from side A.

(b) PCB trace and inner wire bound connection of the QFN test package

Figure 3.3: Picture and inner connection of QFN test vehicle package

the same 3 QFN components, the only difference is all the pins of QFN including EPAD are soldered, the same as in real applications. The components on that side suffered the same stress in the reliability test as the real product, which can be used to evaluate the board-level reliability of this package.

The second test vehicle was dedicated to the study of piezoresistive stress sensors. To achieve this, three unique PCB designs were employed, subjected to two specific manufacturing processes. Both of these two processes are packaged on WLCSP (Wafer Level Chip Scale Package). One of the packages is WLCSP9, which structure comprises eight units, organized in a 4×2 grid. Seven of these units feature different piezoresistive modules, providing diverse types of methods for evaluating stress distribution (such as resistance, current factor for MOS, and saturation collector current for bipolar transistors). Positioned centrally on the PCB, this 4×2 WLCSP9 package exclusively utilizes the n-type mono doping resistance piezoresistance module to measure the stress distribution [31].

Meanwhile, the more intricate WLCSP36 package, while boasting 36 units, only has nine bumps equipped with piezoresistive stress sensors designated for monitoring stress. This package is paired with two distinct PCB sizes: a smaller one where a single component is centrally positioned, and a larger one capable of simultaneously hosting and measuring four WLCSP36 components. Figure 3.4 offers a visual insight into one such stress sensor module. In this depiction, only two bumps (labeled “DUT array”) are designed for stress distribution surveillance, with the remaining seven dedicated to circuit connections. This strategic layout ensures can give a chance to monitor the change of stress distribution of the two bumps underneat, which can also somehow reflected the stress change in other bumps.

For the piezoresistive test vehicle, because of the asymmetry location of the bumps with sensor cells, we need to specially mention the location of each bump. For the piezoresistive sensor with the WLCSP9 package, a demonstration of the PCB and the location of the cells is illustrated in figure 3.5, we can see the two bumps with piezoresistive sensor cells are not the solder joints near the PCB edge. In addition, because the stress distribution pattern is from the view of the die, the location of the piezoresistive sensors cells is horizontally flip compare to the PCB view. For the WLCSP36 package, the location of the piezoresistive sensor cell is indicated in figure 3.6. The right bump in our future measurement result is the solder joint

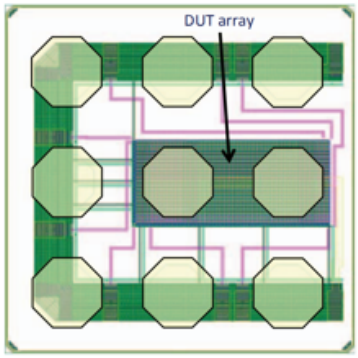


Figure 3.4: Picture of the stress sensor with 9 bumps, the shadow area indicated by "DUT array" is the region where the cells are located [31].

near the edge of the PCB.

When discussing the piezoresistive test vehicle, special consideration must be given to the spatial configuration of the bumps integrated with sensor cells, primarily due to their asymmetrical positioning. This detailed spatial orientation plays a pivotal role in data interpretation and any subsequent analyses.

In the case of the piezoresistive sensor equipped with the WLCSP9 package, a visual representation detailing the PCB and the respective positions of the cells is provided in figure 3.5. Here, it becomes evident that the two bumps integrated with piezoresistive sensor cells aren't positioned near the PCB edge. Given that the stress distribution pattern is visualized from the die's perspective, the piezoresistive sensor cells' placement appears horizontally flipped when compared to the PCB's view.

For the larger WLCSP36 package, the specific positioning of the piezoresistive sensor cell can be observed in figure 3.6. It's crucial to note that, in subsequent measurement results, the right bump corresponds to the solder joint adjacent to the PCB edge.

Understanding these nuances and orientations is essential for linking the measurement result with BLR test property, ensuring that any changes or anomalies detected by the sensors are correctly attributed to their precise spatial locations. This, in turn, can help us easier to understand the test result.

A summary of the two test vehicles can be found in the table 3.1

Test Vehicle Name	PCB Size (mm)	Package Size (mm)	Number of Samples
QFN (in figure 3.2)	132×77	8×8	24
$8\times$ WLCSP9 (in figure 3.5)	84×29	5.4×2.75	1
WLCSP36 Small (in figure 3.6)	53×20	2.8×2.8	1
WLCSP36 Big	132×77	2.8×2.8	4

Table 3.1: The information of test vehicles adopted

3.2. Electrical Degradation Measurement Method

In this section, the measurement method used in the QFN test vehicle is discussed. The measurement target is first discussed in section 3.2.1, measurement methods development is shown in section 3.2.2 to section 3.2.5, and then the final summary is given in section 3.2.6.

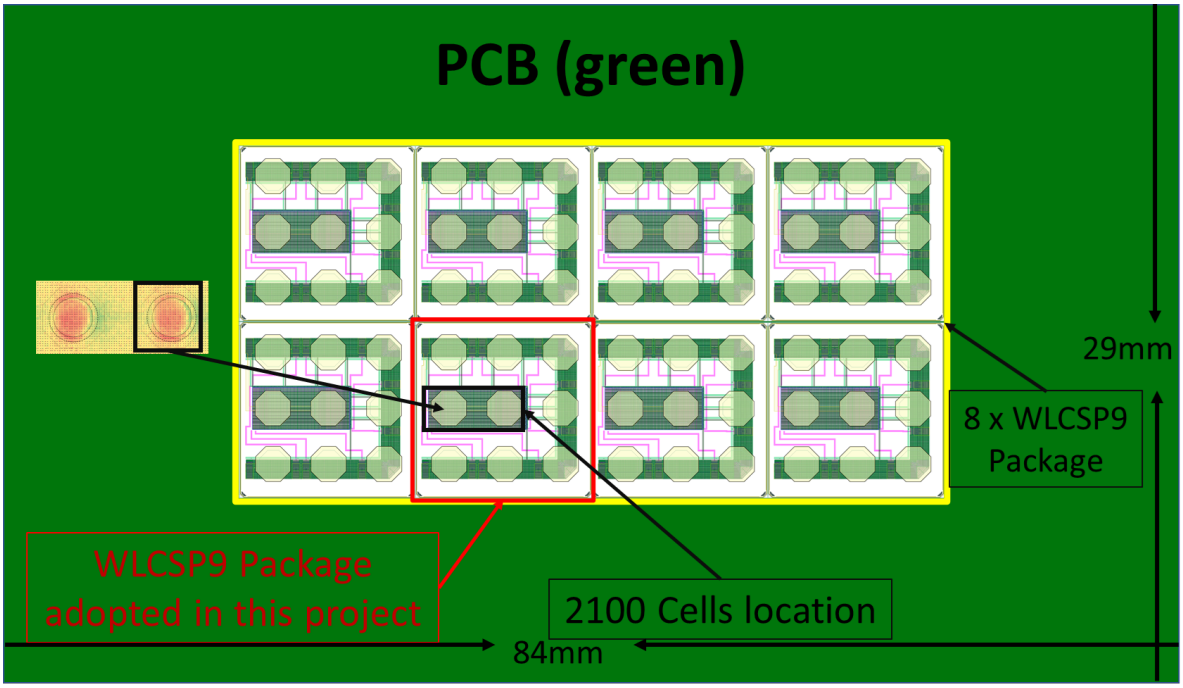


Figure 3.5: Piezoresistive cells location in PCB with 8 WLCSP9 package

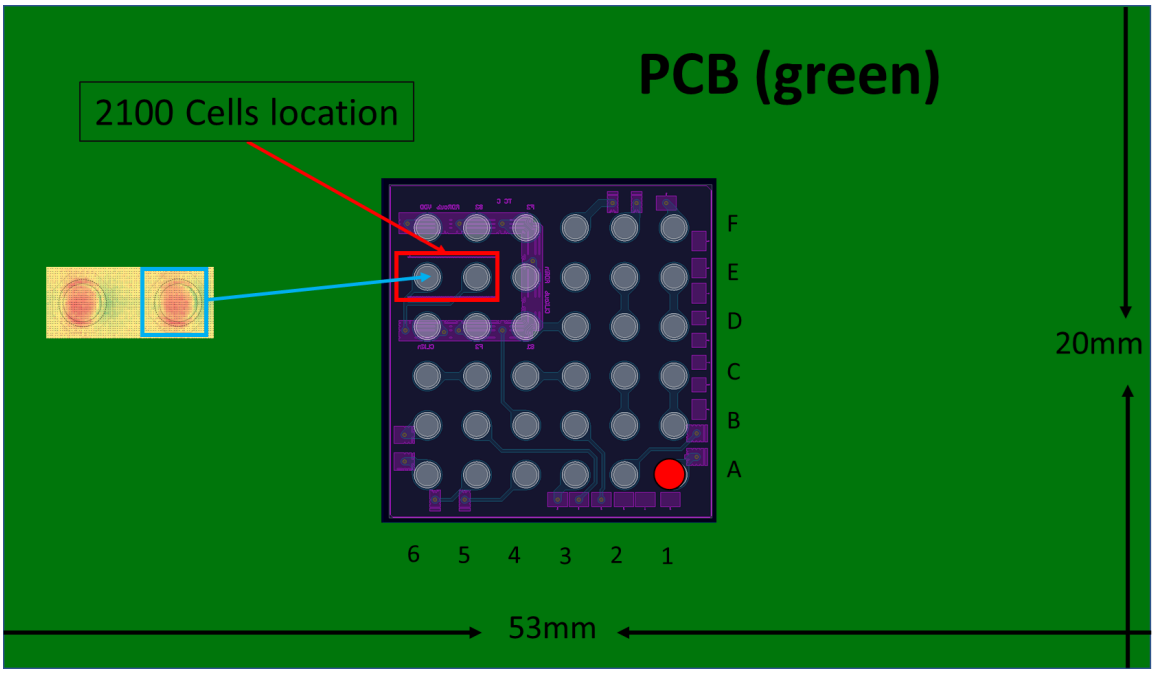


Figure 3.6: Piezoresistive cells location in PCB with WLCSP9 package

3.2.1. Electrical Measurement Target

The four-wire resistance measurement test vehicle can measure the resistance of one solder joint. The typical value of QFN package solder joint resistance is around 4 mΩ to 5 mΩ at room temperature. In order to know how much change of the resistance will happen when there is a crack in the solder joint, we implement an artificial process on the solder joint crack. By using a knife manually, The solder joint wax region was scratched to make a small crack. A Scanning Electron Microscope (SEM) photo of the cross-section is shown in figure 3.7. In the 30 seconds process of hand crack, with in-situ measurement, we can know the resistance change, the resistance measurement result is shown in figure 3.8. We can see that the crack happened between 15 to 20 seconds, and the resistance of the solder joint increased by 0.2 mΩ after the artificial hand-made crack, which gives us an impression of how much should our equipment be capable to measure. The requirement of our measurement device is to measure the resistance of 5 mΩ and can see a 4% change in the measurement result.

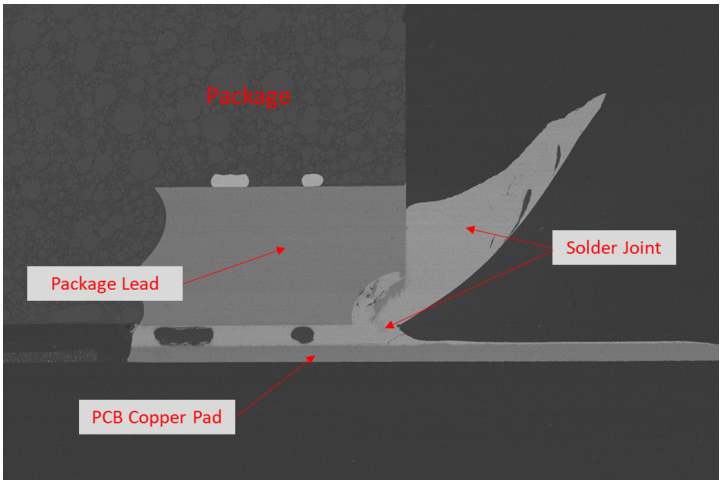


Figure 3.7: SEM Photo of hand-made crack on the solder joint, the small crack inside is caused by vibration

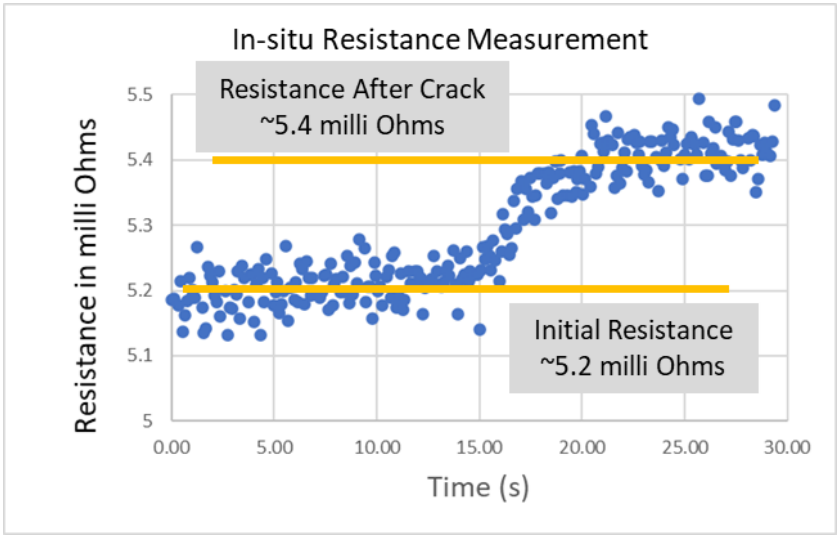


Figure 3.8: In-situ resistance measurement with the hand-made crack process

3.2.2. Electrical Measurement: 2-Wire Measurement

The 2-wire resistance measurement method involves connecting two wires to the resistance under test. By forcing a current through and measuring the resultant voltage, the resistance value can be deduced. Given the design of the sample schematic, this method is employed as state of art method during vibration tests for products designed with a daisy chain. As depicted in figure 1.4, the 2-wire setup can detect an open circuit within the daisy chain and subsequently signal the shaker to halt, which is integrated with the vibration controller. However, a notable limitation of the 2-wire method is the inclusion of the cable's own resistance in the measurement. This can result in readings that are erroneously high, as they combine both the sample's and the cable's resistances.

The state of art measurement method is based on 2-wire resistance measurement. By monitoring the voltage between the daisy chain (solder joint) and stopping the shaker once see there is an increase in voltage. The schematic of the 2-wire measurement is shown in figure 3.9. The readout voltage of the controller is about $2\,\mathrm{mV}$, which means the resistance of the cable and solder joint is in total around $2\,\Omega$. In order to detect the crack developing in the solder joint, we need to be capable to measure the voltage change of 0.01% of voltage change, that's impossible from the datasheet of the vibration controller [38]. Previous test data on vibration can also prove that: we didn't see any trend of increase of voltage before the sudden increase of voltage due to high resistance. In conclusion, for 2-wire measurement, the resistance of the cable count most of the result resistance value, it's almost impossible to measure the very small change of solder joint resistance, and the 2-wire resistance measurement method is not capable to monitor solder joint degradation.

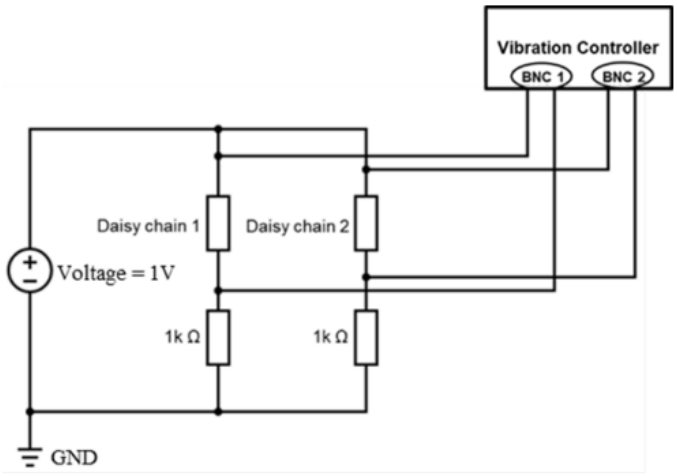


Figure 3.9: State of art: vibration controller 2-wire electrical measurement method (schematics) [39]

3.2.3. Electrical Measurement: Datalogger Method

Datalogger is also known as a data acquisition/switch unit mainly used for continuously logging voltage or resistance. With a multiplexer inside, many channels can be monitored simultaneously with a single instrument [40], widely used in reliability test labs. This section discusses the usage and improvement of datalogger in solder joint electrical tests.

The easiest way of using dataloggers to measure solder joint resistance is using the 4 wire measurement mode of datalogger, the current is forced by two channels and simulations measures the voltage from sense ports. There is only a limited range of the measurement, from $100\,\Omega$ to $100\,\mathrm{M}\Omega$, even though we can increase the resolution by increasing the integral number

of power line cycles, but it's not affordable to take 2 seconds to do one signal measurement (24 solder joint means 48 seconds). One result collected by datalogger 4-wire measurement of the QFN test vehicle is shown in figure 3.10, we can see the datalogger 4-wire measurement method shows the variance of $\pm 1.8\,\mathrm{m\Omega}$ which is enough for detecting and see the failure in one solder joint, but the increase of resistance before solder joint failure is not clear due to this high variance.

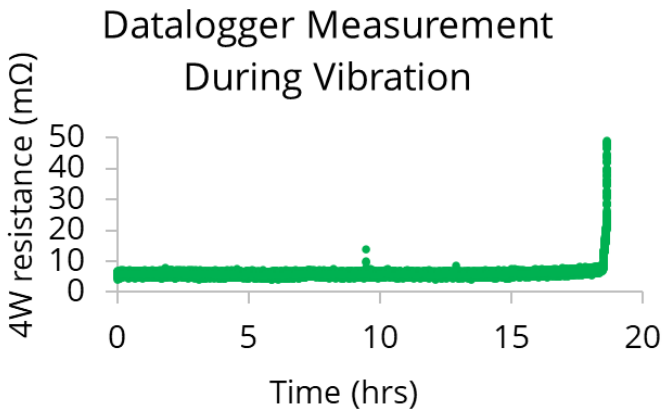


Figure 3.10: 4-wire measurement, state of art result [41]

To capture the degradation process of the solder joint and take advantage of datalogger that can support multiple channels, we can improve the measurement method. The main drawback of the datalogger 4-wire measurement setup is the force current is unknown and we cannot measure it directly. It is supposed to be very low for safety concerns so it's normal that we cannot use it to measure very small resistance. To solve that, we can try to increase the force current applied to the force ports. The lowest measurement voltage range of the datalogger is $100\,\mathrm{mV}$, then we choose force current as $0.5\,\mathrm{A}$ that can make sure the solder joint won't burn up due to the heat and the sense voltage can be in a reasonable value (about $2\,\mathrm{mV}$). In conclusion, we can use an external power supply force with a $0.5\,\mathrm{A}$ stable current and use dataloggers to sense the voltage between each of the solder joints, which can realize a variance of $\pm 0.013\,\mathrm{m\Omega}$. By continue monitoring the voltage of all the solder joints in the QFN test vehicle, we can see the degradation process of the solder joint.

After deciding on the test setup, to increase the flexibility of datalogger measurement, we can use the external connection method to control the datalogger and record the data. Connect the datalogger with a laptop with USB cable, and use the PyVisa library in Python to set up, control, and record data to and from the datalogger [42]. One benefit of external control is the elimination of button operation on the instrument panel, making instrument setup easy after program saving. This makes repeat testing possible and easier. Moreover, this method can add more information such as record time (which can be used for alignment with different data) into the logging result. Moreover, the CSV files generated by Python can be very easy for further data process and plotting.

3.2.4. Electrical Measurement: Source Measurement Unit

The source measurement unit (SMU) is an instrument that combines DC current source, electronic load, and a multimeter, by controlling the function, we can realize different kinds of measurement. The main usage of SMU in the electrical measurement of QFN test vehicles is doing a 4-wire measurement of resistance. The SMU has four ports, two of which can be current sources and the other two can be used to sense the voltage. By using the PyVisa library, we can

send SCPI (Standard Commands for Programmable Instruments) command to SMU [43] which is connected to the laptop by USB cable. The continuous resistance measurement data are logged in CSV (Comma-Separated Values) files using the ASCII encoding scheme and saved in the local drive of the laptop. SMU can have very high voltage sense accuracy, even though we decrease the source current to 10 mA, we can still get stable and fast resistance measurement results. The main drawback of SMU is it can only support one solder joint measurement simultaneously, making it impossible to monitor all solder joints in the test vehicles with SMU.

3.2.5. Electrical Measurement: PXI system

PCI eXtensions for Instrumentation (PXI) is a PC-based measurement system, with different plug-in cards connected with industry-standard computer buses, we can realize different measurement functions. In this project, we also assess and develop the electrical measurement method on our QFN test vehicle. One SMU card in the PXI system is adopted, and we use the 4-wire method to measure the resistance of the solder joint. The block diagram of the measurement using the PXI system is shown in figure 3.11. However, the measurement result shows that the value can depend on the status of the vibration amplifier, the result decreases significantly when starting up the vibration amplifier, and the result also fluctuates more when moving the connection cable. To understand the reasons behind this impact, we look at the principles of the vibration amplifier and shaker and try to find solutions.

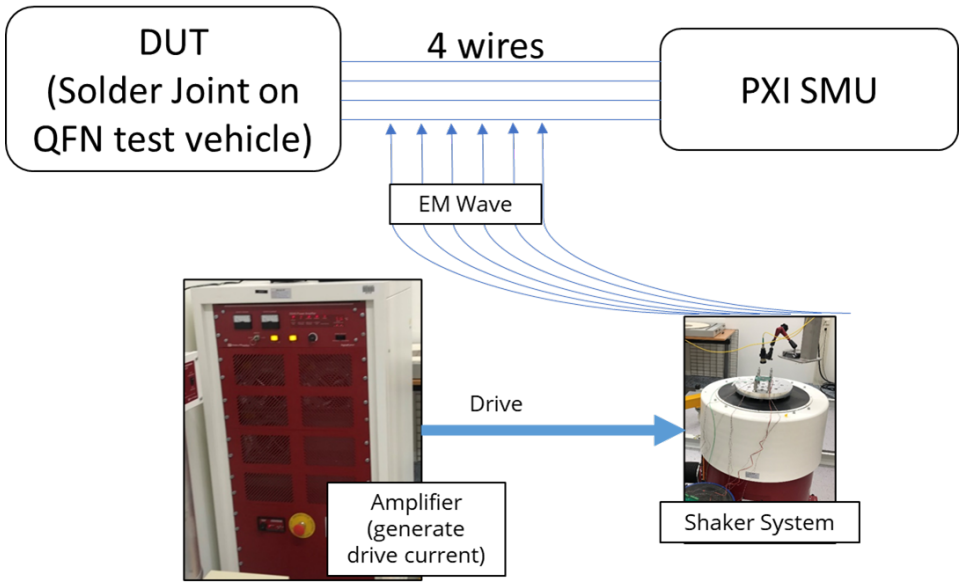


Figure 3.11: Test setup block diagram of electrical measurement with PXI

Given the suspicion that the interference might arise from the magnetic field generated by the shaker's internal magnitude, several solutions were explored. A possible approach is the use of twisted cables instead of ordinary wires. This might significantly reduce the impact of magnetic coupling. The idea behind using twisted cables to mitigate magnitude interference is illustrated in figure 3.12. Here, one might observe that each small circle possibly has an induced current due to the magnetic field. Yet, adjacent circles seem to have opposite directions of these induced currents. This arrangement is expected to counterbalance these currents to some degree. However, this expectation is based on the assumption of a uniformly distributed external interfering magnetic field, which might not be the case here. Areas closer to the shaker might have a more potent magnetic field than those farther away. Hence, the expected uneven distribution of this magnetic field could be why the twisted cables might not have completely

eliminated the interference with the PXI readings when the amplifier is active. Another attempt was made by shielding the wires with a metallic conductor. Using shielded twisted cables or wrapping the wires in aluminum foil, while grounding the foil or shield layer, seemed a promising way to reduce the interference. Unfortunately, this didn't seem to work as well as anticipated. This might be because we couldn't establish a complete equipotentiality for the shield layer, or perhaps the layer wasn't thick enough to prevent interference.

Additionally, employing these enhanced cables introduced another challenge. The wires, as depicted in figure 3.2, are soldered onto the edge of the QFN test vehicle PCB, which is subjected to vibrations. The twisted cables, being bulkier and stiffer than standard wires, might compromise the solder joints' reliability between the PCB and wires due to their weight and rigidity. As the PCB vibrates, these heavy and stiff cables might induce strain on the solder connections, potentially causing breaks at the PCB's connection points. Such disruptions might lead to unexpected shifts in the PCB's resonance frequency and potential reading anomalies.

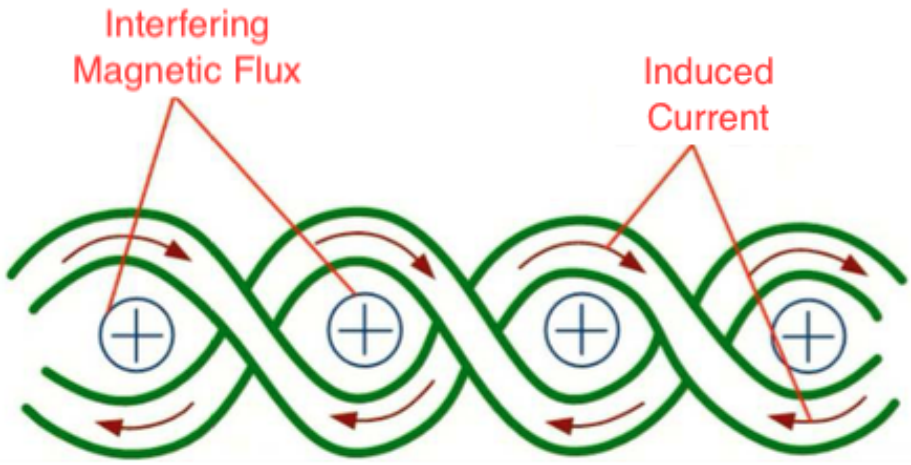


Figure 3.12: A schematic representation of how twisted pair cables can reduce interference from external magnetic fields

If replacing the cables doesn't effectively mitigate this interference, we can resort to other methods to isolate this influence. Another potential approach involves using physical isolation to separate the sources of interference from the sensitive devices. Above our vibration shaker, we could utilize a temperature chamber, a metal-encased chamber designed for conducting vibration tests at various temperatures. Since the chamber's outer wall is made of metal, it theoretically possesses the ability to insulate against external electromagnetic interference. Hence, we are considering placing this chamber atop the vibration shaker and housing our sensitive equipment within it for subsequent measurements. Furthermore, to further minimize the impact, we shortened the wires used. We reverted to using the original single wires, but halved their length, bringing the PXI instrument and the device being tested closer together. We also moved them to the opposite side of the vibration amplifier, all in an effort to mitigate this influence as much as possible. Ultimately, we discovered that while this interference persists, its magnitude has been considerably diminished. Particularly when we secure the position of the cable, the readings remain remarkably stable when the amplifier is activated. Consequently, we have decided to adopt the approach as our final test setup for PXI instrument. However, though the PXI system can have very high sample frequency, the measurement result is worse than the result from the datalogger and SMU, especially since the variance is higher than the other two kinds of instruments.

Measurement Methods	Logging Rate	Variance(mΩ)	Channel Number
Datalogger	2.7 Hz	±0.013	60
SMU	11.3 Hz	±0.004	1
PXI	1 kHz	±0.4	1

Table 3.2: Comparasion of Different Electrical Measurement Methods

3.2.6. Summary of Electrical Measurement Methods

After setting up all the electrical measurement methods and decide suitable configurations, we can compare them to determine which ones are most suitable for our electrical measurement. Three typical resistance measurement results for 10 minutes are shown in figure 3.13, and a comparison of these result sampling rate, and variance are shown in table 3.2. From table 3.2 we can see, SMU can show very low variance and acceptable sample rate and can be the most ideal instrument for our degradation electrical measurement. However, due to the channel number issues, we still need to use the datalogger to monitor more channels. For the PXI system, because the variance is higher than the resistance change during a crack on the solder joint, we may not be capable to capture the crack on the solder joint, we will not use this system on our final measurement setup.

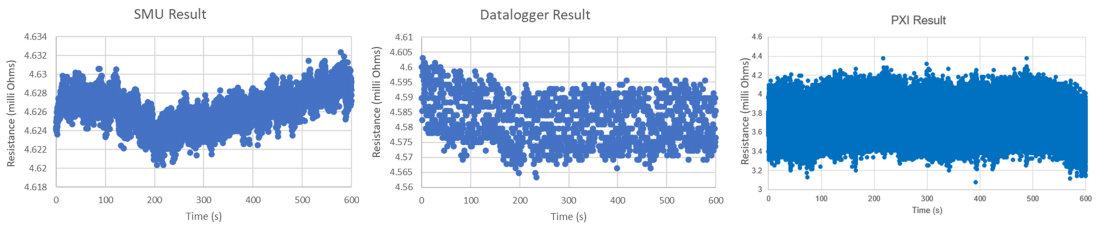


Figure 3.13: Electrical Measurement Result of Three Different Methods

3.3. Physical Parameter-based Degradation Sensing

The physical stress change on PCB with board level reliability test can be related to the health situation of PCB. These physical stress detection methods include sensors that can measure PCB motion during vibration tests and piezoresistive sensors that can describe some permanent change in PCB and solder stress. In this section, different methods that can be used as physical degradation parameters are discussed.

3.3.1. Degradation Parameters Sensor in Vibration

In vibration, the resonance frequency of PCB and the peak displacement of PCB are always of significance important, the change of peak displacement and resonance frequency can be linked to the physical property change of the PCB. The common trend is that the peak displacement will increase with the increase of the vibration bending cycle because of the FR4 material property and small cracks in the vicinity of the screw holes [10]. Three methods to access the PCB motion during vibration are accessed and the goal is to find one that is most suitable for sensing the peak acceleration and resonance frequency. The photos of three sensors are shown in figure 3.14.

The first sensor we use is the LASER Doppler Vibrometer (LDV). Which is working based on the Doppler effect, which can show the speed of the PCB with a reflection tape stick on the center of the PCB. The laser is the contactless measurement, and the small piece of tape stuck

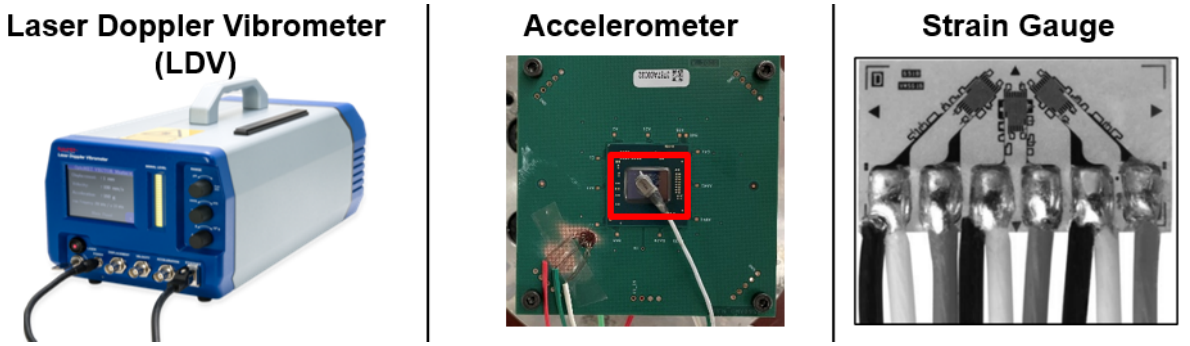


Figure 3.14: Three Sensors Used for Measure the Degradation Parameters in Vibration

on the PCB has a very low weight, the influence on the PCB motion is almost zero. The main drawback is the price can be costive and not possible to be used in real application PCB.

The second sensor is the lightweight accelerometer ($\leq 0.2g$, which can be glued on the center of the PCB and used coaxial cable to connect to the vibration controller. The accelerometer can sense the accelerometer and resonate the frequency during the vibration test.

The third sensor we use is the tri-axial strain gauge, which is three resistive foil with 0°, 45°, and 90°. The strain gauge is mounted on the PCB and whenever there is deformation, the resistance of the foil can change which can be sensed by the measurement equipment. With correlation to the input vibration response, we can determine the resonance frequency of the strain gauge, and by further simulation we can also indirectly know the peak displacement of the PCB and then can calculate the peak velocity and peak acceleration.

To evaluate these three types of physical degradation parameter sensors, we designed some experiments to observe their respective impacts on the vibration. We used the square PCBs with the BGA package in the center and subjected them to the same series of operation steps as described below:

1. Perform vibration test using LDV to measure the PCB motion
2. Glue the accelerometer on the center of the top side of the PCB and use both LDV and accelerometer to sense the vibration test
3. Remove accelerometer, mount two strain gauges, one in the center of the backside and the other one located 5.5mm from the packaging corner, shown in figure 3.15
4. Glue accelerometer and doing vibration test with three kinds of sensor
5. Repeat measurement to test repeatability

All of these processes are done with a sweep sine vibration test with the frequency range 350-550Hz, the sweep rate 1 Oct/min. The input accelerations include 1g, 5g, and 10g (where g is the acceleration due to gravity) and each test repeats three times to get the statistical results and check repeatability.

One observation from steps 4 and step 5 is that the measurement result can stay stable with repeat and all three measurement methods can show similar resonance frequency results (division less than 1Hz), and from steps 2, step 4, and step 5 we can see the acceleration result measured by LDV and accelerometer is similar, which means we can only adopt the measurement result from LDV for our further analysis.

We make a plot to show the relationship between the peak strain readout from the strain gauge and the peak acceleration of the PCB center. We only consider the maximum principal strain, the nominal strain with the highest magnitude. Principal strain can be calculated by

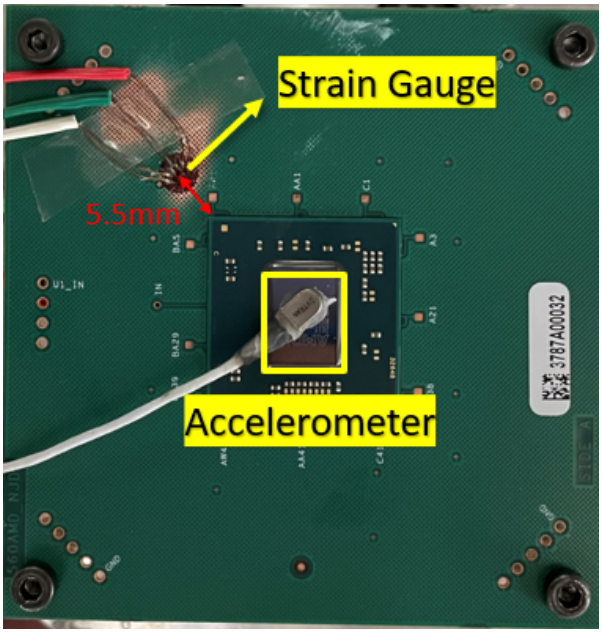


Figure 3.15: Location of Mounting Strain Gauge on top Side

[44]:

$$\frac{\varepsilon_1+\varepsilon_3}{2}+\frac{1}{\sqrt{2}}\sqrt{(\varepsilon_1-\varepsilon_2)^2+(\varepsilon_2-\varepsilon_3)^2} \tag{3.1}$$

where the ε_1, ε_2 and ε_3 are the strain value in 0°, 45° and 90°. Then we can plot the relationship between peak principal strain and peak acceleration in figure 3.16. Based on the plot, it appears that there is a linear relationship between peak acceleration and max principal strain, particularly at the location where the strain has a higher value (Strain gauge on the top side). The intercept can be attributed to the strain gauge not being nullified, which can be considered a consistent offset value.

To understand the effects of attaching an accelerometer and mounting a strain gauge, we looked into the LDV (Laser Doppler Vibrometer) measurement outcomes. All data was normalized using the 1g load measurement from the initial step, and the resulting changes in both the resonance frequency and accelerometer were plotted. As presented in figure 3.17a, the resonance frequency appears to remain remarkably stable, even with varying loads under the same PCB conditions, with deviations staying below 1%. There might be a minor impact on the resonance frequency due to the introduction of an accelerometer or the placement of a strain gauge, but this influence is minimal.

On the other hand, the normalized acceleration displayed in figure 3.17b shows more significant changes. When comparing the results of step 2 and step 3 with step 0, it's evident that both the accelerometer's attachment and the strain gauge's mounting can cause a reduction in peak acceleration. Furthermore, the larger decrease in acceleration in step 3 compared to step 2 suggests that the strain gauge might exert a more considerable effect on peak acceleration. Step 4 indicates another slight decrease when compared with steps 2 and 3, implying that the combined presence of the strain gauge and accelerometer might produce a cumulative, albeit limited, effect. However, the overall impact of either the strain gauge or the accelerometer on our acceleration measurements is considerable. As a consequence, we've chosen to exclusively use the LDV as our sensor for tracking physical parameters during vibration tests, ensuring that the PCB isn't affected by any additional weight and shift.

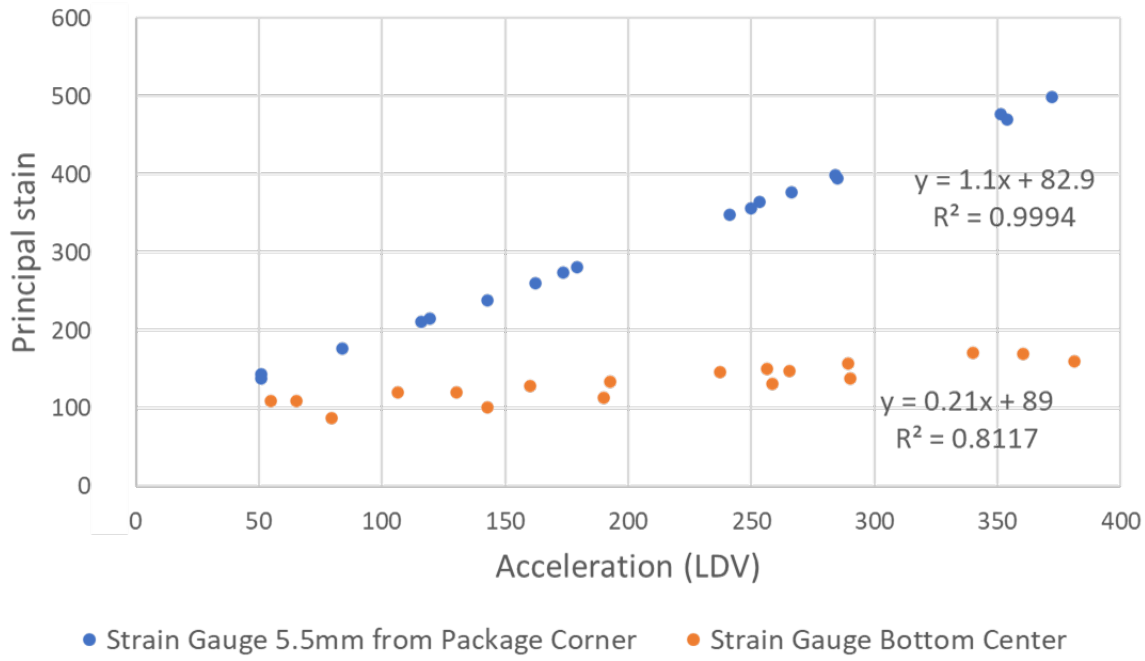


Figure 3.16: Relationship Between Peak Strain and Peak Acceleration, we can see the linear relationship between principal strain value and PCB center acceleration.

3.3.2. Degradation Parameters: Piezoresistive stresss Sensor

A piezoresistive sensor, specifically a stress sensor packaged on WLCSP, offers another avenue to illustrate the physical degradation of solder joints. This sensor is equipped with 2100 resistance cell arrays positioned atop 2 solder bumps. Capitalizing on the piezoresistive effect inherent to silicon devices, the stress experienced by each measuring cell is manifested in its resistance value.

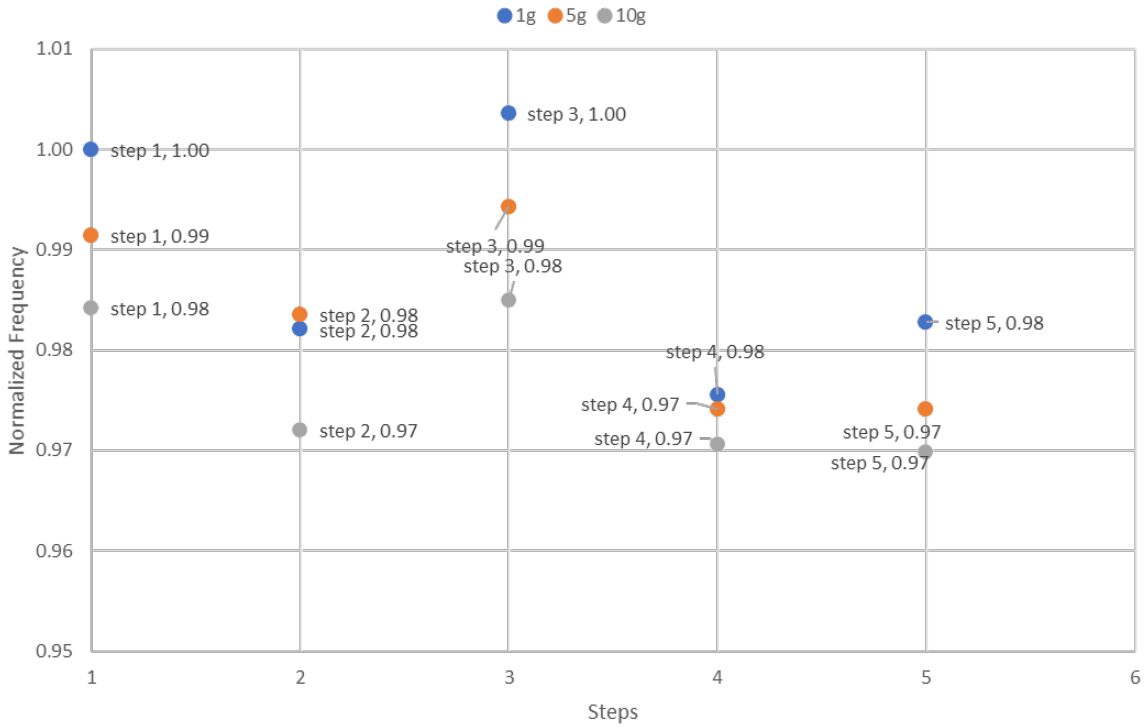
The initial distribution of values from the piezoresistive sensor is predominantly shaped by the packaging and Surface Mount Technology (SMT) processes. As outlined in section 2.4, this can be utilized to scrutinize the mechanical implications steered by these two procedures. Additionally, the emergence of a crack in the solder joint, stemming from the stress existence post-SMT, will alter the stress distribution beneath the cells, irrespective of the specific solder joint where the crack occurs. This is expected to result in a variation in the readout values. Such a phenomenon underscores the theoretical rationale behind employing the piezoresistive sensor to demonstrate the physical degradation trajectory in board-level reliability tests.

However, to implement the sensor and get the correct readout, some effort in the sensor setup, measurement program development, and data processing is required. The detail of the readout of the piezoresistive sensor will be demonstrated in section 3.4

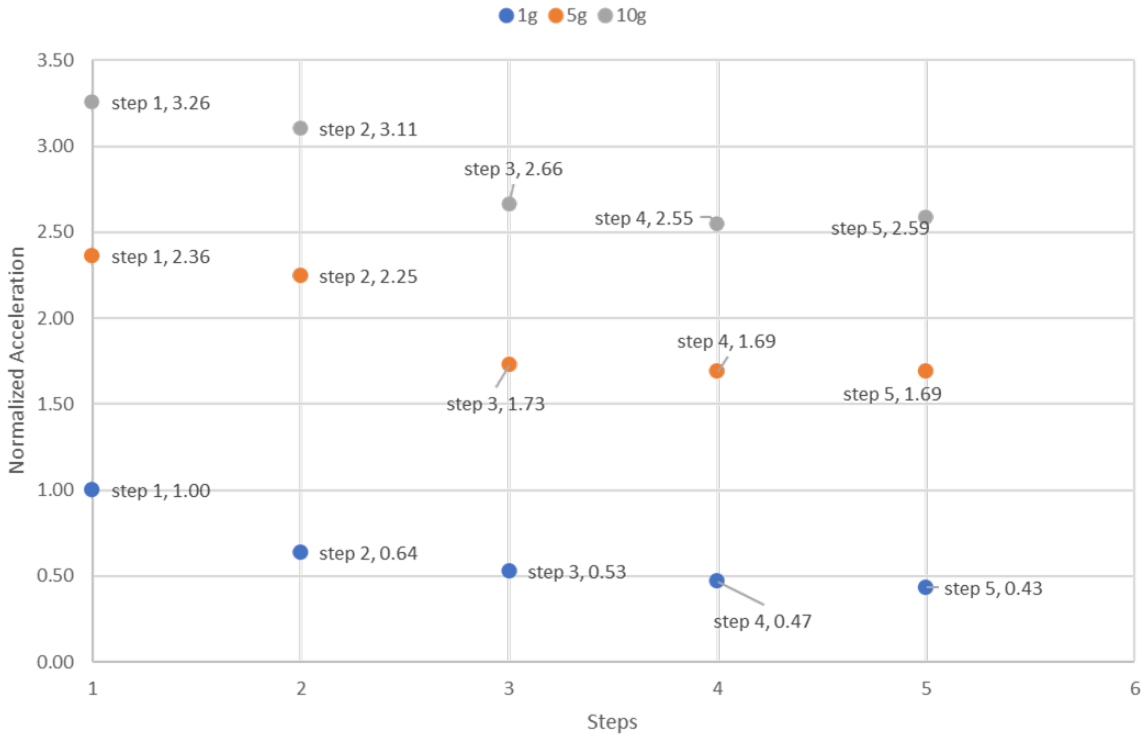
3.4. Readout of Piezoresistive Sensor

3.4.1. Piezoresistive Sensor Measurement Steps

To obtain resistance readouts from the piezoresistive cells, it is imperative to conduct measurements on the sensor. In the course of our measurement process, we successfully captured data from the piezoresistive sensor, revealing a stress difference distribution pattern that aligns closely with the one presented in the study [31]. A significant milestone in our efforts was the endeavor to slash the measurement time required for the sensor. The referenced study [31]



(a) Normalized resonance frequency



(b) Normalized Peak Acceleration

Figure 3.17: LDV Normalized Measurement Results. This graph illustrates the resonance frequency remains relatively consistent across different sensors, but there is a noticeable shift in peak acceleration when various sensors are mounted or glued onto the PCB

.

reported that a single measurement took up to 50 minutes, a duration that would be untenably lengthy if our aim was to track degradation after board-level reliability tests. With our test setup primed and the discerned pattern after our processing, we then proceeded to utilize this sensor in a series of board-level reliability tests.

The structure of a single piezoresistive sensor module structure is shown in figure 3.4. In total 8 bumps are required to do the measurement. We need to access all the 2100 piezoresistive cells by address selection and combine them with the data process, we can get the piezoresistive readout and can plot the distribution of stress pattern difference inside the region where the sensor cells locate.

The steps of measuring the piezoresistive sensor can mainly be divided into the following parts:

1. Select the cell required to measure and get the column number m and row number n,
2. Give the DC voltage supply between *VDD* and *GND*
3. Feed the *CLK* port with 100 cycles square signal
4. Feed the address signal simultaneously with the clock signal from *ADDR* port, only NO.m and NO. 70+n of the address signal are “1”, the rest should be “0”.
5. Force the force ports with 50 µA current and measure the voltage between the two sense ports
6. Calculate the resistance based on the measured voltage and current, record the result, and start from step 1 again.

3.4.2. Piezoresistive Sensor Single Cell Measurement

To complete the above measurement steps, and do measurements on our real PCB, the preparation and detailed process are discussed in this section.

Firstly, to realize the clock, address generation, and voltage/current measurement, the proper equipment need to be chosen based on availability. With careful selections, analog discovery 2 microprocessor and source measurement unit (SMU) are adopted. To connect all these instruments with the piezoresistive sensor PCB, a transform PCB is required.

The transform PCB is shown in figure 3.18. This PCB uses SMB (SubMiniature version B) connector to connect the force and sense signal, two separate connectors are reserved for signal demonstration during debugging. The stress sensor is connected to the PCB using header pins and header pin sockets. The whole piezoresistive sensor measurement block diagram is shown in figure 3.19

The initial trial is done on the test vehicle with 8 WLCSP9 modules with different cells inside each of the packages. The measurement is done step by step, by using the Waveform software provided by the manufacturer of analog discovery 2, we can generate a clock signal for a specified time length, and use the costume digital signal function to generate the address signal that satisfied the format described in section 3.4.1. Then use the SMU 4-wire measurement function to generate a 50 µA force current and measure the voltage, checking whether the resistance result can satisfy the theoretical value (around 2 kΩ). The initial measurement was not correct because a wrong stress sensor module was picked, with carefully checking the position of each module, we change the location of the header pin and got the desired result. Another job in that testing process is to try the highest clock frequency so that the PCB can work normally. With continually increasing the digital signal output frequency, we found the stress sensor can give in-range output with clock frequency up to 10MHz. After these trials, how to repeat the address select - SMU measurement 2100 times becomes a question.

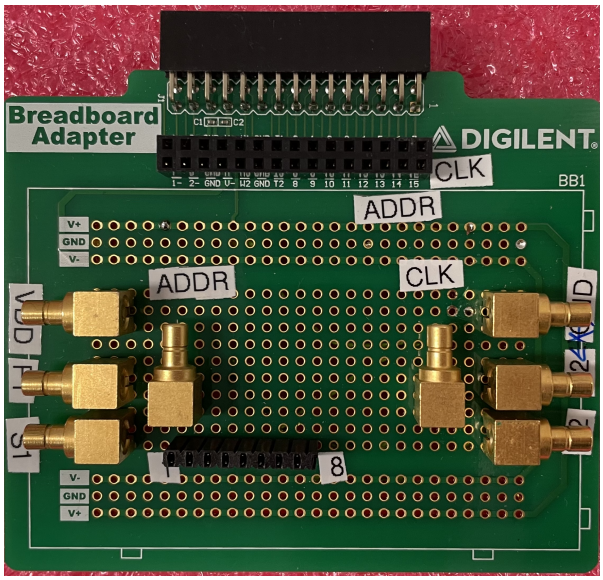


Figure 3.18: The Diagram of piezoresistive sensor measurement setup

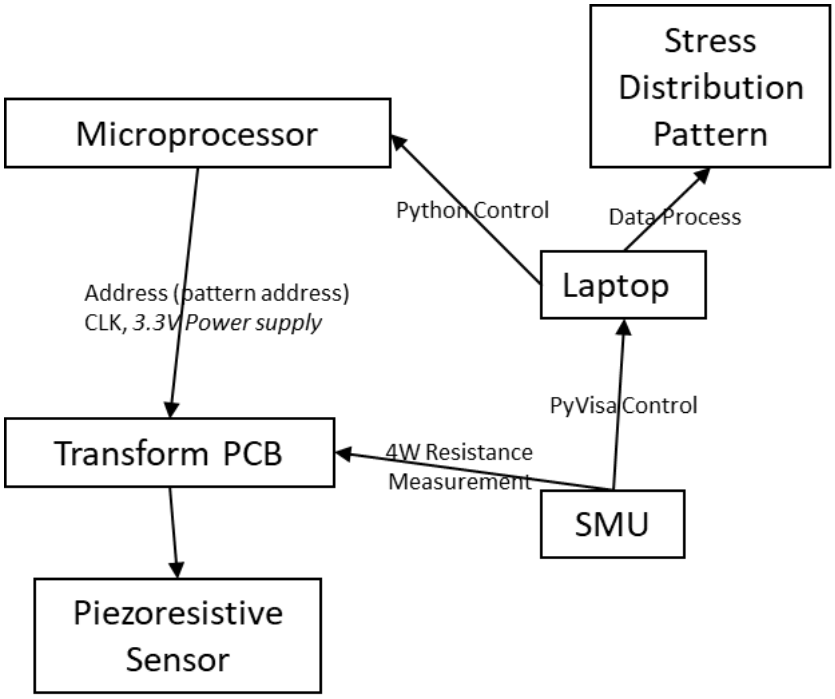


Figure 3.19: Photo of the transform PCB, Stress sensor can be connected with header pin socket indicated with number 1-8, Analog Discovery 2 can be connected by the black socket on the top side of the PCB, the SMB connector can be used to connect coaxial cable and for signal transmission.

3.4.3. Automation of Measurements

In figure 3.20, the unique addressing mechanism for accessing the 2100 sensor cells using a 100-bit address signal is illustrated. Within this scheme, a 100-bit address (represented by 9 bits in the figure) is fed into the sensor. Coordinated with the clock signal's rhythm, these bits sequentially populate the module. After 100 clock cycles, the register's value is locked in by ceasing the clock signal input. Both columns and rows utilize a binary system where the presence of a "1" activates a switch. Only when both a row and column switch are active, indicating "1", do the force and sense ports connect to the desired piezoresistive cell. As demonstrated in figure 3.20, a black block represents an active sensor cell, connected because its corresponding row and column registers both read "1". In contrast, the other cells remain inactive.

Given the intricacies of this addressing system, generating a comprehensive library with the addresses of all 2100 cells is paramount. Manually inputting these addresses, or even typing them out, would be a tedious endeavor. To streamline this process, a Python algorithm was crafted. It not only computes the addresses, based on column and row numbers but also translates them into the necessary 100-bit format. Specifically, this format comprises a single "1" within the initial 70 bits and another "1" among the concluding 30 bits.

The output from the Python program is a CSV file organized with 100 columns across 2100 rows, each row representing a unique sensor cell address. To mitigate potential issues from consecutively measuring adjacent cells, the measurement order of the 2100 cells is randomized. This ensures that each cell is accessed in a non-sequential manner, allowing for all cells to be measured over 2100 distinct measurements without introducing any biases from their positional adjacencies.

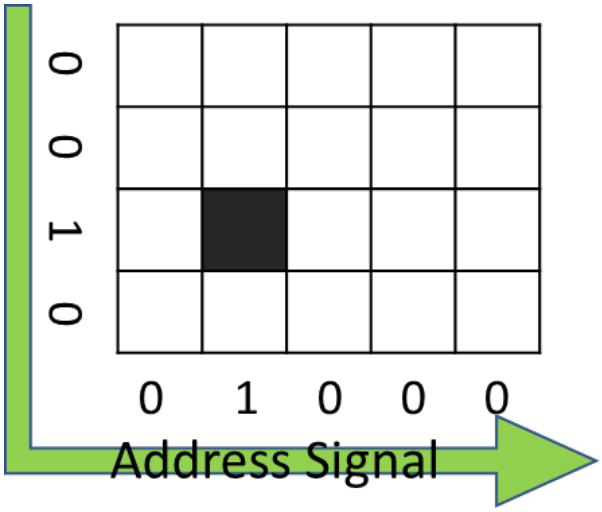


Figure 3.20: Schematic of the Address Selection Process in Piezoresistive Sensor

Once the address CSV file is generated, the next step is to automate the analog discovery output. We leveraged Python to craft a program that would auto-generate the required digital patterns. The manufacturer's provided package [45] enables Python to command the Analog Discovery 2, permitting custom digital output. The address and clock patterns are defined in a binary 0-1 array. Using the custom digital output functionality, we simply designate the output frequency and the port connected to our PCB.

The clock signal uses a 0-1 periodic array (comprising 200 bits) which is then converted into the C language byte format. For the address signal, the program sequentially reads each line of the address CSV file and transposes them into a compatible data format. The digital bit

output is set to operate at 20MHz, resulting in a clock signal square wave output of 10MHz.

The 3.3V power supply to the sensor is also powered by the analog discovery 2, by enabling one DC voltage output and setting the voltage level with Python program, a stable power supply can be implemented.

To gauge the resistance of each cell, a Source Measure Unit (SMU) is employed. To automate this process and mitigate human force, the Python script was further extended to incorporate automated measurement and recording features. Using the PyVISA library [42], the program communicates with the SMU. A standard USB A to USB B cable connects the laptop and SMU. Sending SCPI commands (Standard Commands for Programmable Instruments) [43] allows us to initialize the SMU, setting it to source current while measuring voltage. Utilizing a 4-wire measurement mode, the two force ports $F1$ and $F2$ link to the SMU's force high and force low, while sense high and sense low are connected to the $S1$ and $S2$ ports. To ensure that the SMU and Analog Discovery 2 share a common ground, the force low port on the SMU is also linked to the ground of the Analog Discovery 2, ensuring correct internal switch operation in the die.

After obtaining the voltage readout from the SMU and calculating the resistance using the supplied current of $50\,\mu A$, the data is logged 0.01s post Analog Discovery 2 feeding the address and clock signals. This ensures a stable readout. All resistance measurements are cataloged in a separate CSV file, timestamped to reflect the start time of the measurement. A comprehensive measurement will result in a CSV file with 2100 entries. These entries arranged chronologically, are then further processed to deduce resistance value and stress distribution pattern.

After the program was ready, some trial tests were done. There is an issue with the measurement result: there is about 1 in every ten measurements shows half, one-third, or even one-fourth of desired resistance result, and this issue cannot reappear with the measure one cell per time and cannot be solved by decreasing the clock frequency. After using the oscilloscope to trigger one peak of the address signal, we see the waveform like figure 3.21. We can see from figure 3.21, as the failing edge of the clock signal and address signal align with each other, and if there is a delay in the clock signal, the raising edge of the address signal may be earlier than the previous clock failing edge, which means two adjacent cells are connected in parallel. The measurement result is the parallel of two resistance and results in halving the readout. One of the best solutions is to shift the clock signal by quarter period to solve this issue. In practice, we double the length of the clock signal from "1010" binary signal to the "11001100" binary signal, and then we can shift it by one bit. The new waveform after shifting is shown in figure 3.22. The ensuing result is we have indeed reduced the frequency of the clock signal from the previous 10MHz to 5MHz. Yet, given the limitations of the microprocessor we have, it's unfeasible to elevate the digital output sample frequency to 40MHz. As a result, utilizing a 5MHz clock signal frequency gives the most optimal solution for our present circumstances.

After debugging the program and resolving the issues encountered, we can use this program for measuring the stress sensor.

3.4.4. Improvement on Measurement

In this section, we detail the functional enhancements and modifications made to the test setup subsequent to the completion of the preliminary measurement program.

The first improvement is because we have identified an issue where certain measurements can produce unusual and inconsistent values due to external interference or random noise. This is particularly prevalent in single-cell measurements, with very low probability. To ensure the accuracy and reliability of these measurements, we conduct a repeatability check after two consecutive measurements. If the results pass the p-test, we can accept the measurement as reliable. Alternatively, we may choose to disregard any abnormal results. The Python script

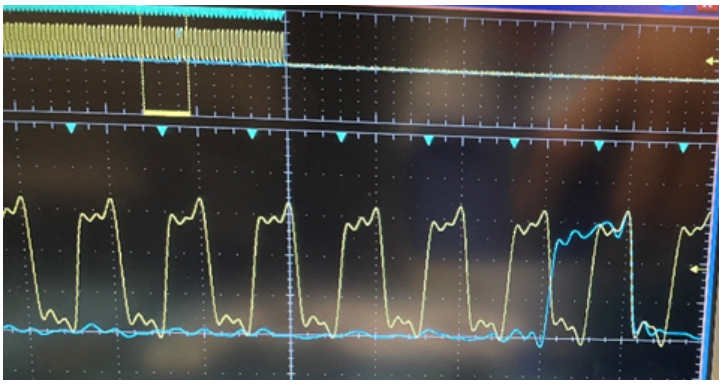


Figure 3.21: Oscilloscope graph: Waveform clock(yellow) and address (blue) signal, we see the failing edge of the address signal is aligned with the clock signal.

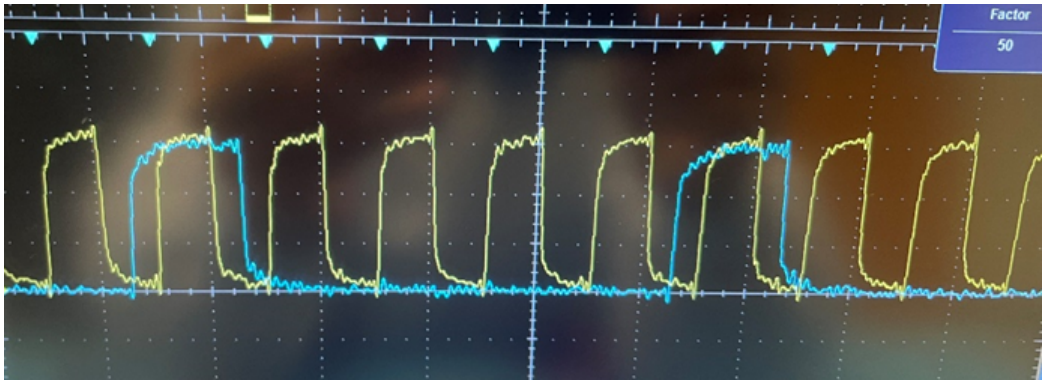


Figure 3.22: Oscilloscope graph: Waveform clock(yellow) and address (blue) signal, after delaying the clock signal with a quarter period, there is a time margin to make sure only one cell is connected.

now includes both the two-measurement and p-tests for added convenience.

The second enhancement pertains to a design amenable to thermal cycle tests. As referenced in section 1.3.1, two stable temperature regions exist within the chamber during thermal cycling. Given that solder joint failure typically requires several hundred cycles, indicative of a potential span of weeks, manual measurements are impractical for real-time tracking of the piezoresistive sensor's alterations. Hence, automation is essential.

Two primary solutions were contemplated. First, a thermocouple could continuously monitor and signal when the chamber reaches a stable temperature, triggering the piezoresistive sensor measurement. However, this necessitates an additional datalogger, complicating laptop connectivity, and poses challenges in ascertaining chamber temperature stability. Alternatively, leveraging the consistent cycle duration of the temperature chamber presents a more streamlined approach. Recognizing the fixed interval between two stability periods enables us to schedule sensor measurements at consistent intervals. By synchronizing the inaugural measurement with the initial stable temperature, subsequent measurements can consistently align with these stable periods.

Consequently, our code was modified in line with the latter strategy, empowering the program to assess the piezoresistive sensor during both high and low-temperature stability phases.

The third refinement relates to the thermal cycle test concerning our WLCSP36 piezoresistive sensor's large PCB test vehicle, as referenced in table 3.1. An additional connection is made to a dummy ground bump located at the center of the piezoresistive cell, as illustrated in figure 3.4. This bump is internally linked to the ground cell on its right through the RDL layer, with both bumps situated beneath the piezoresistive cells. Given that we've established pin connections to both solder bumps, there's potential to measure the resistance of the two solder joints.

Our devised setup involves connecting two wires to both of the corresponding PCB pins and deploying another SMU for four-wire resistance measurements during intervals when the piezoresistive sensor measurement is inactive. Two distinct SMUs, connected via different cables, operate in an alternating fashion. This allows for continuous resistance monitoring during temperature ramp-ups, ramp-downs, and stable periods within the chamber. The resultant resistance measurements will aid in drawing correlations between solder joint resistance and piezoresistive sensor readings.

3.4.5. Piezoresistive Sensor Measurement Data Pocess

The collected data only consists of the resistance of the cells, to make these data into the stress distribution pattern, a data processing step is required on the result resistance data.

To get the distribution, there are mainly five steps:

1. Convert the 2100 measurement values into a 30×70 matrix corresponding to the actual sensor cells' positions. (for measurement results with repeatability check, we can take the average value of two measurements after throwing away the bad value)
2. Take the reciprocal of the resistance values to obtain the conductance values for each cell.
3. Find the reference region and calculate the reference value of the conductivity comparison.
4. Compare the relative change of all values in the conductivity matrix to the reference conductivity value, use conditional formatting, and make color on the final matrix, which is the stress distribution matrix.
5. Make further results of the difference of the stress distribution matrix to get more results on the change of the stress distribution matrix.

For step three, to get the reference region, one of the common methods is to look at the region that can be considered "stress-free". Figure

3.23 shows the position of the two “stress-free” region, both of which consist of 30 cells. We can take the average conductivity value of these 60 cells as the reference conductivity value and use this value to do the relative change comparison in step 4. The conditional formatting in step 4 is the process that gives each cell a color based on the value, in this sensor measurement, we always use the red color means a positive high value, yellow means a 0 value, and green is a negative value in the relative change of conductivity. One example of the stress distribution patterns is shown in figure 3.24.

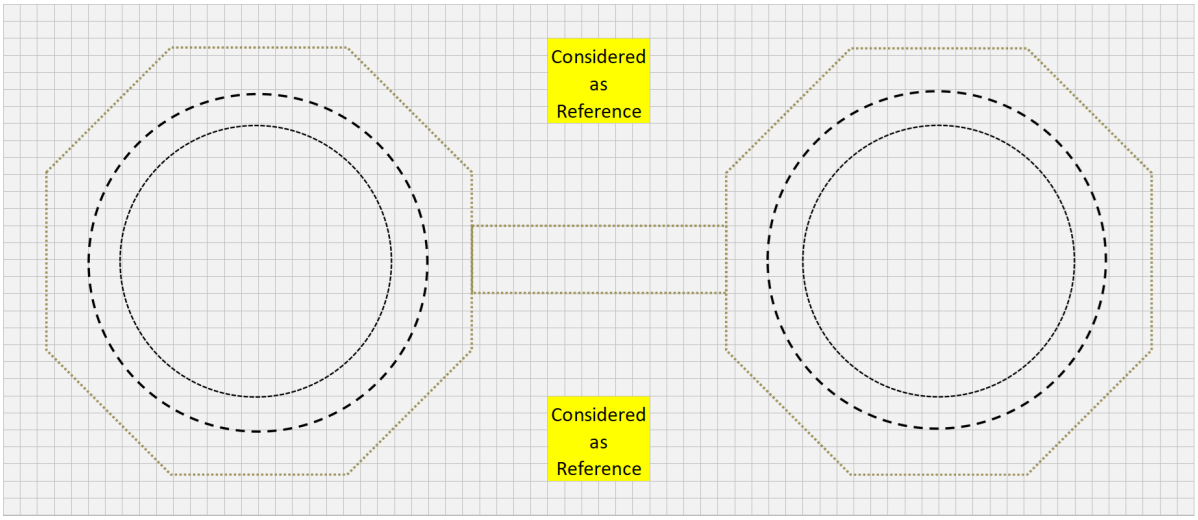


Figure 3.23: The distribution of the 2100 cells under the two bumps of the piezoresistive sensor test vehicles. The two regions with yellow shade are regions far from the solder joint, metal pad, and package edge, they are considered as the “stress-free” region

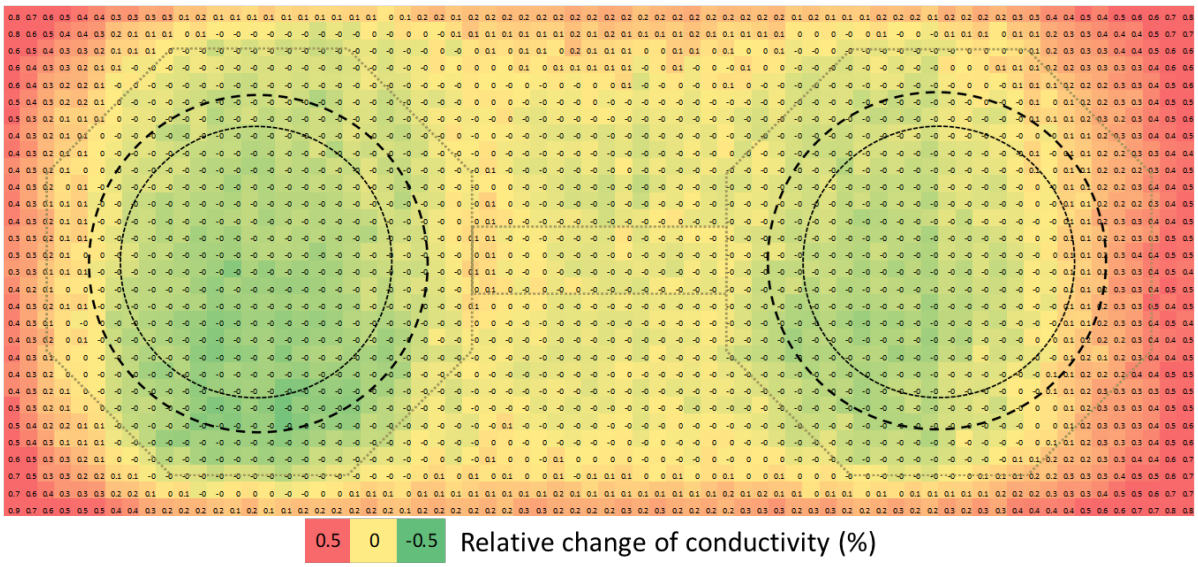


Figure 3.24: One example of the measurement result of piezoresistive sensor stress distribution pattern

In step 5, we mainly look at the difference between the current measurement and the first measurement and the current measurement between the last measurement. All results are exported into a single Excel file with different tabs for one measurement. The conditional formatting and the location of the two bumps (as shown in figure 3.23) are also inserted in the Excel file.

The methodologies adopted in this project are developed and improved. The next step is to use these methods introduced in this chapter in board-level reliability tests.

4

Reliability Test & Failure Analysis Result

After developing the method for measurement and characterizing the state of the test vehicles in chapter 3, we can start our reliability test and related failure analysis. This chapter will be divided into different reliability test methods. section 4.1 shows the vibration test setup and test result, section 4.2 shows the bend test applied on the piezoresistive sensor PCB, section 4.3 introduced the thermal cycle test result and section 4.4 shows some statistical result on the QFN test vehicle.

4.1. Vibration Test

In this section, the vibration test on two of our test vehicles will be discussed. The vibration test profile will first be discussed and then followed by the initial test result.

4.1.1. Test Setup

Two kinds of test vehicles will be used in the vibration test: the QFN package and the small WLCSP36 PCB. As shown in table 3.1, the size of two PCB is different, according to equation 2.9, the resonance frequency of these two PCB can be different. We will use two kinds of sweep sine vibration test profiles to test the two kinds of test vehicles separately.

QFN Test Vehicle

For the QFN test vehicle, the initial trail test was first done with low input acceleration and sweep sine between 10 to 1000 Hz and got the resonance frequency is about 365Hz. Considering there may be differences between different PCB, soldering the cables can have some influence on the resonance frequency, and resonance frequency will shift with board aging, we set the sweep sine frequency range between ±20%, which is 292Hz to 438Hz. This frequency range will be adopted for all vibration tests in this test vehicle.

For the input acceleration, we will propose 3g which is suitable to make the solder joint-PCB crack, and the result can be used to compare with previous results in other research [41]. Sweep sine is adopted, and for the sweep rate, to decrease the influence of nonlinearity, 1 oct/min will be adopted. A picture that the QFN test vehicle is fixed on the fixture is shown in figure 4.1.

During the vibration test, we monitored the resistance, resonance frequency, and peak acceleration of all 24 solder joints and the PCB. We employed an SMU and a datalogger to continuously measure the resistance. For each sweep, the resonance frequency and peak acceleration were recorded. The resistance measurement equipment was managed by a PC using Python and the Pyvisa package and resonance frequency and peak acceleration are logged

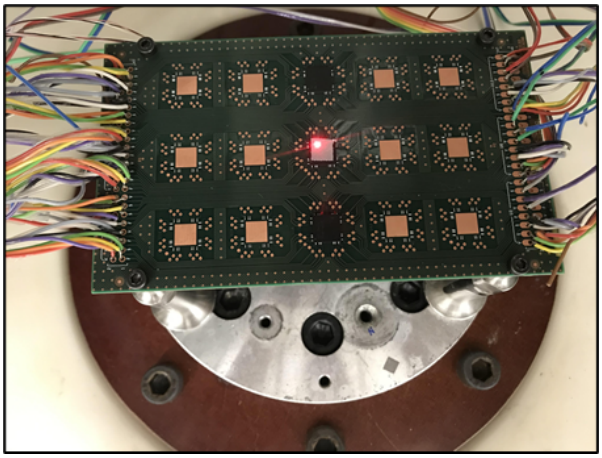


Figure 4.1: Picture of the QFN test vehicles fixed on the fixture. The center red point is the focus point of LDV, focusing at a reflection tape in the center of PCB.

by the software linked to the vibration controller. Failure was determined by detecting high ohmic resistance in a solder joint's readout. Upon detection, the SMU triggers the vibration controller via its digital I/O port on the rear panel. The test can be halted using the abort function upon receiving a high-voltage signal from the SMU's digital output line. Although the test is configured to run for 24 hours, it often concludes prematurely due to the SMU's trigger.

Piezoresistive Sensor Test Vehicle

With the same procedure on the WLCSP36 small PCB, we know the resonance frequency of the stress sensor is about 717Hz, and we can set the sweep range between 575 to 860Hz. The input acceleration is also set to 3g. A figure shows the PCB fixed on the fixture is shown in figure 4.2, it appears that since this PCB lacks screw holes, slits are made in the pillar that can hold the PCB edges during vibration. It is important to note that this may lead to variations in positioning if remount the PCB. Therefore, it is crucial to avoid handling the PCB once the vibration test has begun.

For the readout of the piezoresistive sensor, as shown in section 3.3.2, the readout of the piezoresistive sensor can take about five minutes, and during that time, the PCB should stay stable to get all the measurements of the 2100 cells with the same states. To realize that, we need to stop the shaker when we do the sensor readout. The stop-and-measure process can be realized with the SMU and a relay card. The final test setup is set to for every 20 minutes of vibration, the shaker stops for a while and waits for the measurement of the stress sensor.

4.1.2. QFN Test Vehicles Test Result

In total four PCBs of this test vehicle are tested in vibration. Two of them are with components on side A and the rest of two are with components on side B. A summary of the four PCB is shown in table 4.1. The sample size shown in table 4.1 is the number of solder joints that have measurement data (ignore defective solder joints or solder joints that don't apply measurement).

The first result from the vibration test is the resistance measurement result from the SMU and the datalogger. Apart from that, the readout of LDV can also be extracted and look at the resonance frequency and peak acceleration.

We can first look at the resistance change of the solder joint during the vibration test. Take the SMU measurement result from PCB #2, which is shown in figure 4.4 as an example. If we zoom in on each of the parts of the resistance result, we can see the resistance value mainly can be divided into four regions: stable region, increases region, ring bell region, and high ohmic

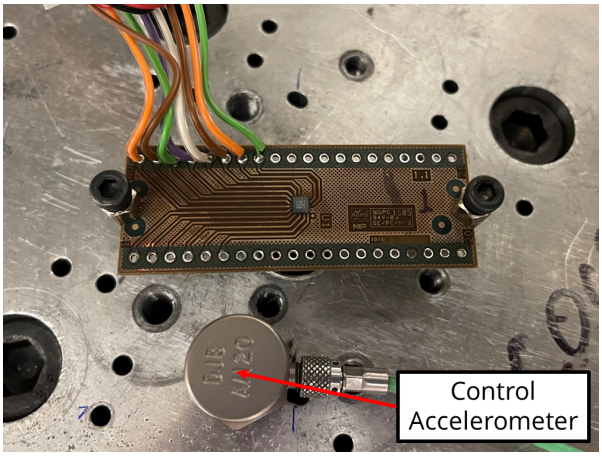
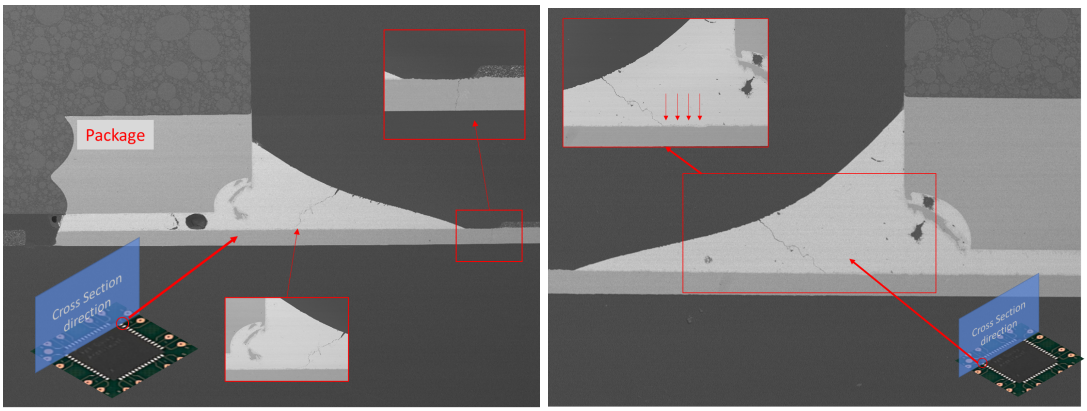


Figure 4.2: Picture of the small WLCSP36 vehicles fixed on the fixture.

PCB #	Side	Sample (Solders) Size	Long Edge Samples	Short Edge Samples
PCB # 1	A	9	6	3
PCB # 2	A	22	12	10
PCB # 3	B	23	11	12
PCB # 4	B	23	12	11

Table 4.1: Summary of QFN Test Vehicles PCBs.

region. To analyze the physics reality behind these regions, we use the cross-section method and planner lapping method to analyze the states of the solder joints and PCB. Though these methods are disruptive, we have repeat results in different solder joints, we can also summary what happens in each of these stages with separate failure analyses. Some of the cross-section photos are shown in figure 4.3, and further explanation of these photos will be shown afterward.



(a) The cross-section shows both PCB crack and solder crack

(b) The cross-section image shows solder crack reflecting the second stage of SMU measurement

Figure 4.3: Cross section photo shows different stages of the degradation and failure

In the last stage of the plot shown in figure 4.4a, we can see the high ohmic region. The resistance increased to 30 Ω, that's the part where the SMU output voltage is clamped by the voltage limit, the real measurement result is infinite resistance at that region. The link shows open in that region. We can zoom in on the y-axis and we can get figure 4.4b. In figure 4.4b we can see the resistance shows high fluctuation at the center of this measurement, like the sound profile of a ring bell. We call that region a ring-bell region. During vibration testing in this

region, there may already be some PCB crack happens and because the PCB is still vibration, the connection is properly linked, which shows the fluctuation of the resistance result. In that region, the connection is no longer reliable, and the product will no longer work properly if there is a small shaking. The failure analysis photo in figure 4.3a can also see there is another PCB crack on top of the solder joint crack. in figure 4.4c, we can see the slow increase of the resistance result of the solder joint, the resistance increased for in total of 0.4 mΩ, which is about 9% of the initial resistance. Failure analysis result in figure 4.3b also can show the solder joint crack.

(a) Resistance result of One solder joint, during whole vibration test

(b) Solder joint ring bell resistance region, zoom in on the y-axis of figure 4.4a

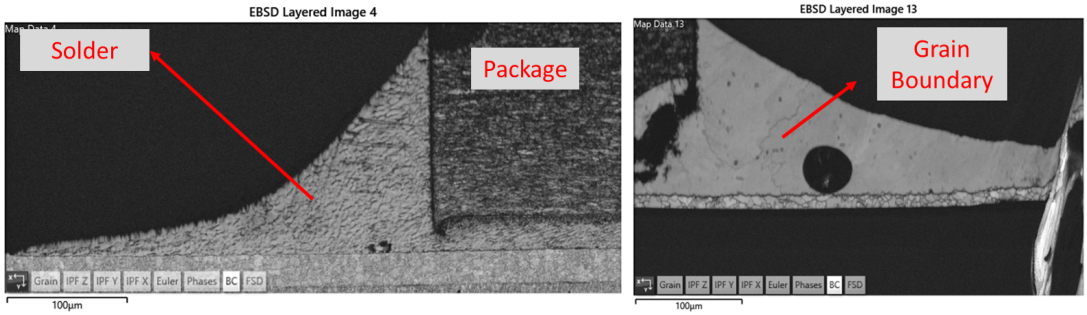
(c) The initial 7 hours of solder joint resistance

(d) The initial 10 minutes of solder joint resistance

Figure 4.4: The SMU measurement to fail resistance results for one solder joint

Figure 4.4d shows the initial 10 minutes of the resistance measurement, we can see there is a very small decrease in the resistance value, the phenomenon is observed in most of the solder joint resistance measurement results, but the reason for this response is not proven. That's may because of the increase in the grain size [46], which is due to the combination of small grains and can lead to a decrease of resistance in theory. In figure 4.5, two Electron Backscatter Diffraction (EBSD) photos are shown, which is a method that can perform quantitative microstructural analyses. Figure 4.5a is the reference microstructure of the solder joint, we can obverse the rough solder joint surface which indicates different small grains orientate randomly. Figure 4.5b shows the microstructure after some short time of vibration. Real solder crack is not observed in that process, but we can see from the smooth surface of the solder joint that the grain mainly becomes into three parts, divided by the crack-like line indicates in the photo. The comparison between these two EBSD photos can indicate the recrystallization and combination of small grain in the solder joint, which is considered to be the reason for the initial resistance decrease in the solder joint, but further statistical results are required to prove this phenomenon. The grain recrystallization process is also part of the degradation process, which indicates there

is no failure-free region in the vibration test because the physics property starts to change whenever we start the vibration test.



(a) EBSD results on a reference solder joint, we can see various grains inside the solder

(b) EBSD results on a solder joint after vibration, in figure 4.4d stage

Figure 4.5: The EBSD result of QFN test vehicles solder joint

The stage shown in figure 4.4c is where we are interested most, because during this region, there is already some damage or crack of the solder joint, and the damage can enlarge and lead to a failure finally. However, the slight increase in resistance will have little impact on the product's performance. This region can be called the degradation region, and we will look at the factor and give statistical parameters of the degradation region which can be used to alarm the solder joint crack. For the rest of the measurement results from both datalogger and SMU, we can all somehow see the different regions in the result, part of them shows full open, and part of the result only shows the initial state when we stop our vibration test. More analysis will continue in section 4.4.

The last two stages (ring-bell stage and open stage) are also observed in other literature using 2-wire measurement [47], [48], but the initial increment due to solder joint degradation is not captured.

The second test result for the QFN test vehicles is the physical parameter measurement. With LDV, we can measure the acceleration on the PCB over frequency. One example of this measurement result is shown in figure 4.6, we can see because of the hardening cubic nonlinearity of the PCB, the resonance frequency and peak acceleration of the two directions of sweep sine vibration test can show some difference, the response shows some delay than the real resonate frequency. As a result, we will divide the positive and negative sweep separately when we analyze the change in resonance frequency and peak acceleration over time. With the degradation of PCB and solder joints, the peak acceleration and resonance frequency of the PCB can shift over more sweep numbers. One example of these changes is shown in figure 4.7, which contains the result for more than 1000 sweeps.

To further analyze this data, we divided the resonance and peak acceleration measurement results into different groups, and by looking at the mean and average value of each of the groups, we can try to correlate the shift of parameters to the degradation of solder joints. As shown in figure 4.8, the resonance frequency for the negative sweep is analyzed. We picked every hundred sweeps into one group and calculate the mean value and standard deviation of each group. We can see from figure 4.8 that in the first seven groups, the resonance frequency can keep a linear trend of increase. However, this slope shows more increase in the eighth group, and in the same group, we see failure happens, which means the first fully open happens in that group. If we correlate the electrical measurement data, we see the first ring bell resistance measurement result (figure 4.4b) in group 7 and the first PCB copper trace fully open in group 8. We can relate the change rate of resonate frequency to the degradation and use the resonance frequency as a parameter to reflect the degradation in board-level reliability.

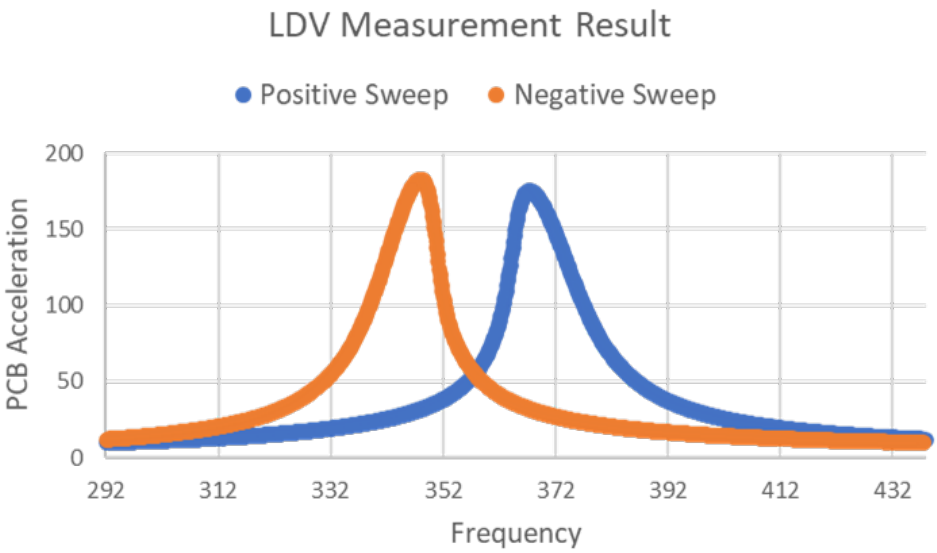


Figure 4.6: One example of PCB acceleration measured by LDV

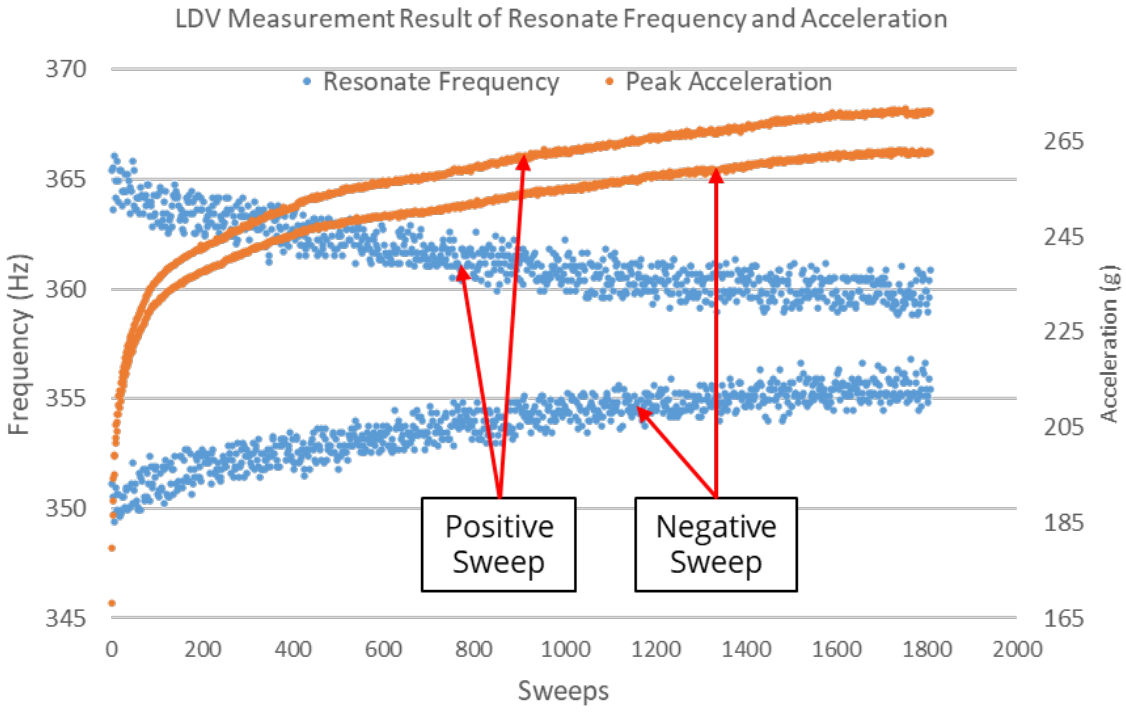


Figure 4.7: The change of resonance frequency and peak acceleration with the increase of vibration sweep numbers

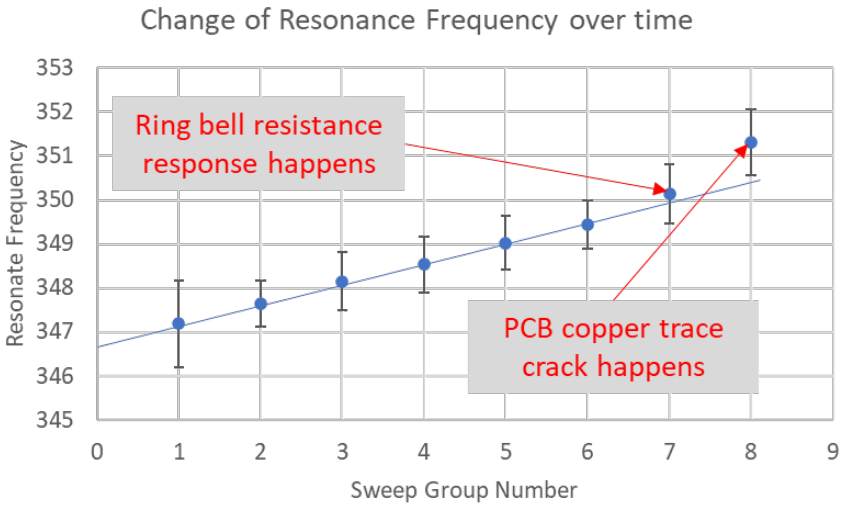


Figure 4.8: The change of resonance frequency over time of sweeps. Every 100 sweeps are divided into one group and the average and standard deviation of each group are displayed.

4.1.3. Piezoresistive Sensor Test Result

In total 30 times of sweep sine are applied to the PCB, which means in total 20 hours. The final piezoresistive sensor measurement result compared to the initial stress distribution pattern is shown in figure 4.9. We can see after 20 hours, the right bump shows a change in the stress distribution, the part toward the edge of the die shows a conductivity increase and the inner part shows a decrease of conductivity. That change is because the stress distribution under the edge bump changed, which can be linked to cracks in the solder joints.

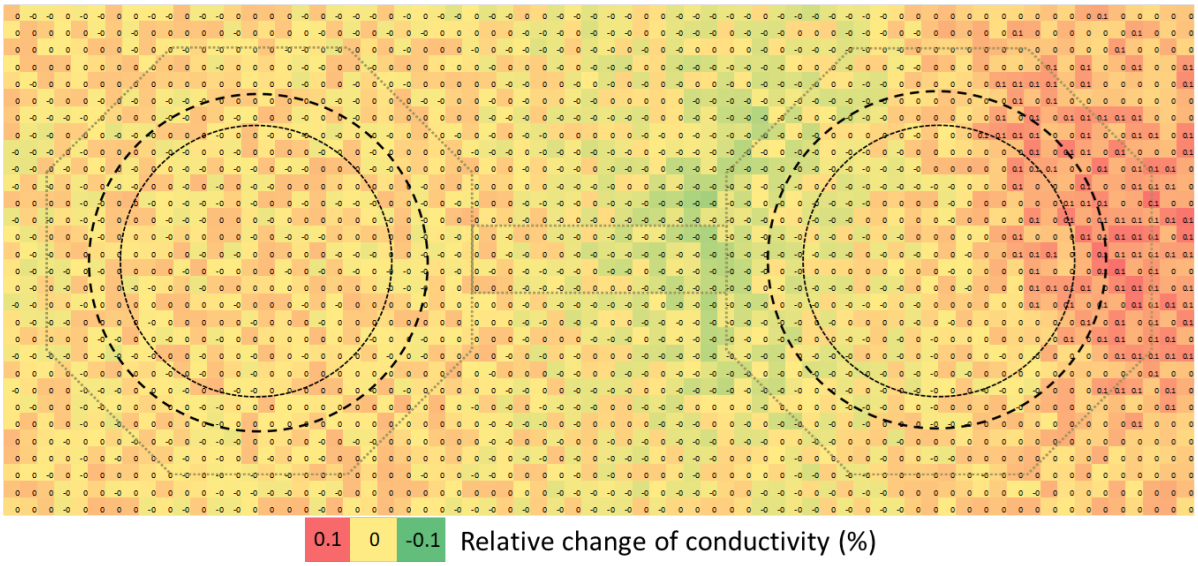


Figure 4.9: The stress distribution pattern change after vibration for 20 hours

To validate the assumption on the reason of the shift in stress distribution and find the root cause, we perform a cross-section on the solder joint and one of the cross-section results of the solder joint we are monitored is shown in figure 4.10. We can know the place where the crack occurs is under the area where we see the increase of conductivity in the stress distribution

pattern. We can also see from figure 4.10 that there is a defect on the solder joint that we are interested in, which may be the reason that the crack initiates and grow within 20 hours of the vibration test. That can be a clue that the piezoresistive sensor can be used as a physical parameter to module the solder joint crack.

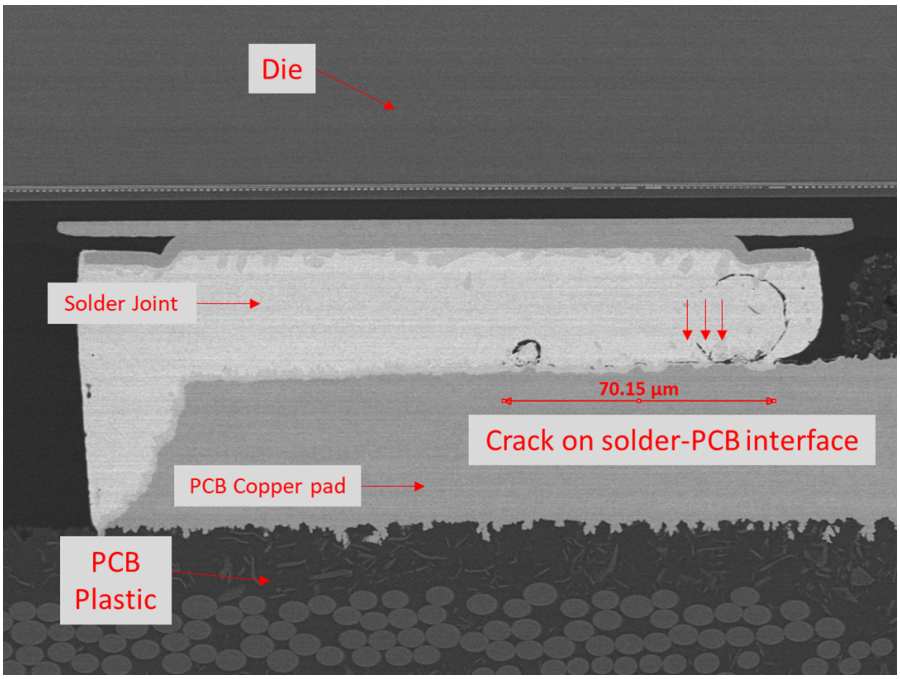


Figure 4.10: Cross-section image of solder joint crack after 20 hours vibration

However, for the vibration test on the big WLCSP36 test vehicles (shown in figure 3.1), the same phenomena didn't occur after more than 40 hours of vibration. For the big PCB, the resonance frequency is lower than the small PCB and the peak acceleration is higher than the small PCB. According to equation (2.6), the peak displacement of the big PCB is much higher than the small one, in other words, the stress applied to the die in the big PCB should be higher. However, though we double the test time, we didn't see the degradation of the solder joint. That may be due to the defect didn't exist in the solder joint we are monitoring on the big PCB and we can also know that a defect can accelerate the crack of the solder joint.

4.2. Bending Test on Piezoresistive Sensor

To look at the response of the piezoresistive sensor under different stresses and do characterization, we first do bend tests on the piezoresistive sensor, the test vehicle we used is the WLCSP9 piezoresistive sensor. The bending test is in two parts, the bend test at only room temperature (25 °C) and the bending test at different temperatures.

4.2.1. Test Setup

The profile for the bending test is detailed in table 4.2. We utilized a four-point bending test because it offers more consistent stress at the PCB's center, with the component-oriented downwards towards the bend tester. After reaching each displacement value, the fixture maintains that position and two measurements are conducted. Post each displacement, the motor resets to 0 displacements before commencing the next cycle.

To elucidate the piezoresistive sensor's response across various temperatures, bend tests were performed under differing thermal conditions ranging from −40 °C to 125 °C. A single PCB

was used in the study, and to ensure the sample won't be destroyed, the bending displacement was capped at 1mm. To minimize the amount of repeated bending, the PCB is first bent and then the temperature inside the chamber is adjusted during the test setup.

Load Span	Support Span
30mm	66mm

Table 4.2: Test Setup of Bending test

4.2.2. Bending Test in Room Temperature Result

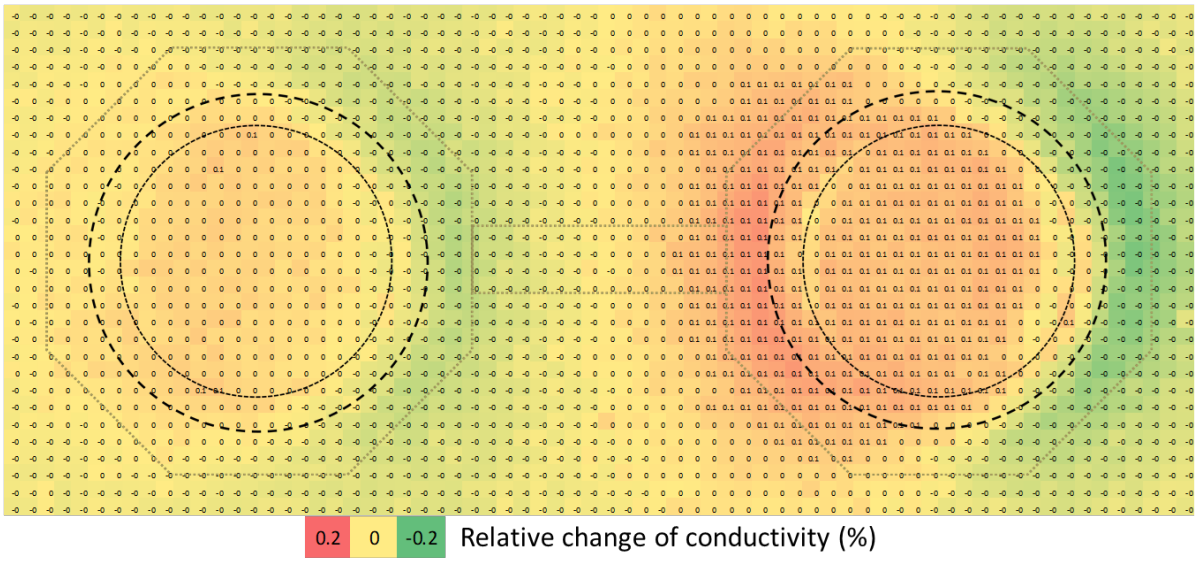
To look at the bending test result, the measurement data is first processed with the same data processing method mentioned in section 3.4.5, we can get the stress spatial distribution pattern under the two solder bumps. we can make a differential between two measurement results to see the influence of bending. If we consider the 0mm state as the reference state of the stress state and compare the result of all the bending displacement with the initial state we can know the influence of different bending.

Three results with small bending displacement are shown in figure 4.11, we can clearly see the color under the two bumps increased with the increase of bending displacement. We can look at this result on another side, considering the position of the two bumps: the right bump is toward the edge of the PCB and the left bump is near the center. We can look at the average conductivity change under the right bump and plot them with different bending displacements. One result of the relative change of conductivity under the right bump in small bending displacement is shown in figure 4.12, we can see, for small bending displacement, the relative change of conductivity or the increase of the red color in figure 4.11 can be linear.

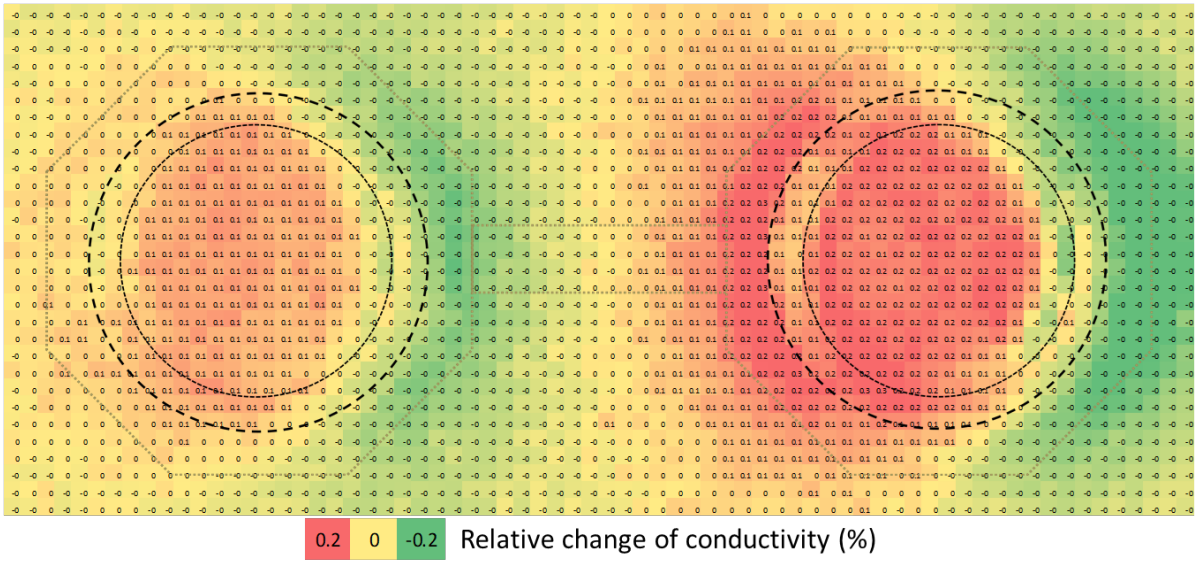
Another method to describe the trend of the bending test is to look at the value at the center part of the plot, in other words, just look at the value change at the horizontal center of the two bumps along the long edge of the sensor array, which is the direction that the bending stress is applied. We can first look at the average of each of these conductivity and the plot is shown in figure 4.13. We can see that the conductivity has a transfer point and the trend shows a difference, which can indicate that the dominant part of stress distribution changed between these two regions. One hypothesis can be because of the full crack at the edge bump, which can decrease the number of bumps that undergo bending stress. We can consider analyzing these two regions differently.

The change of the conductive curve along the two bumps in small bending displacement is shown in figure 4.14, the location of these two bumps can refer to figure 3.5. From the arrow in figure 4.14 we can see with the increase of bending displacement, the stress distribution pattern at the center part of the bumps shifts to one side. Moreover, we can see the difference in stress change level between these two bumps, right bump, the one near the edge of the PCB, shows more stress change, and conductivity discontinuity is also seen at the edge of the bumps. This stress distribution discontinuity can be an indication of the initiation of a crack.

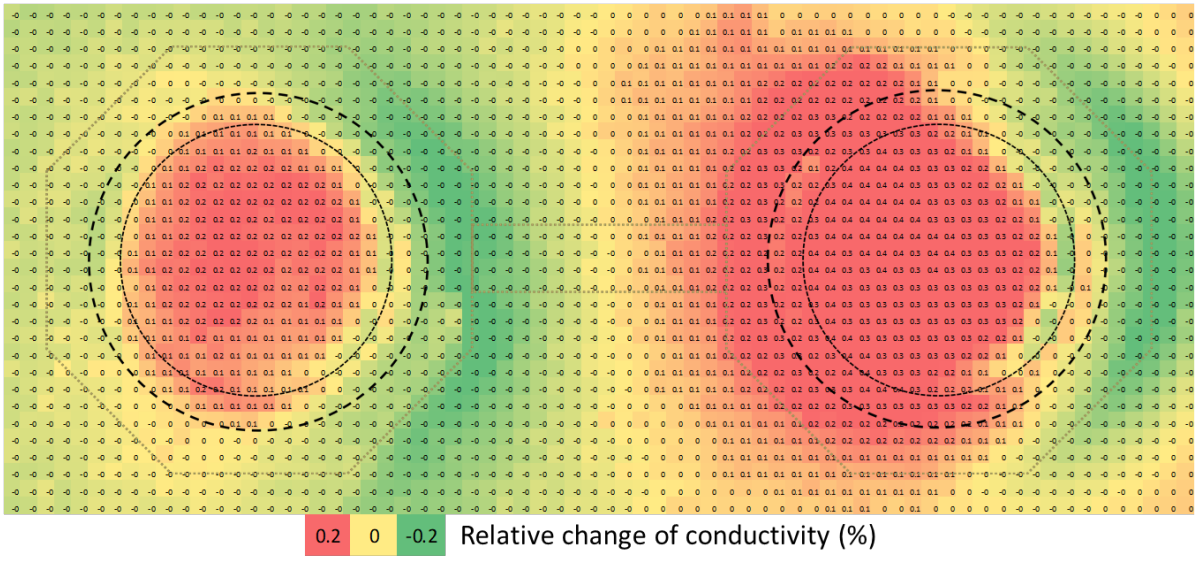
If we continue to increase the bending displacement on the same PCB, the trend will no longer follow the trend described in figure 4.12. Figure 4.15 shows three results after we gave higher bending displacement to the PCB. We can see from the figure 4.15a on the edge between the solder joint and the left edge of PCB (left side of right bump in figure 4.15a), there is a small crescent area, this area didn't observed in figure 4.11, it's believed that this area is caused by the fact that the solder joint on the edge of the PCB already cracked and the stretch stress to the solder joint become dominate. In addition, from the figure 4.15c we can see with the continued increase of the bending stress, the left bump also shows the crescent. Then we can get the conclusion: when we do the bending test on the PCB, the stress first occurs on the



(a) Stress distribution pattern change after 0.5mm bending



(b) Stress distribution pattern change after 1mm bending



(c) Stress distribution pattern change after 2mm bending

Figure 4.11: The piezoresistive measurement results in small bending compare to no bending state

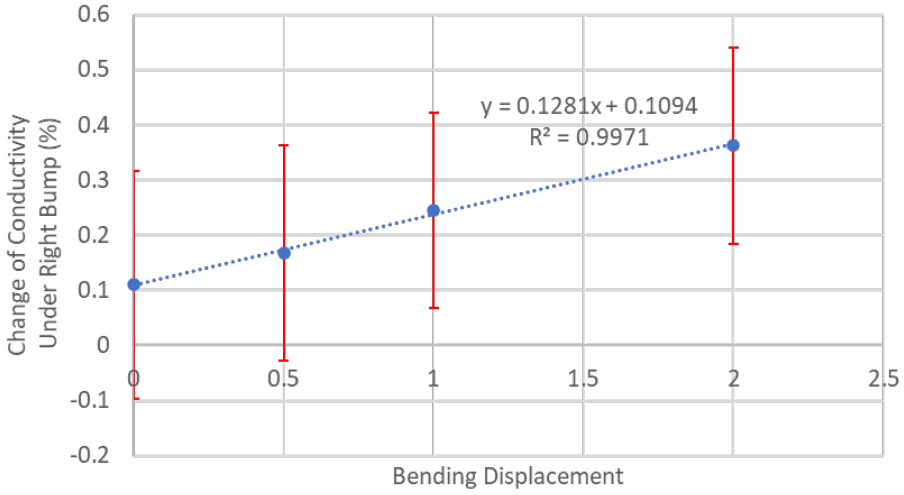


Figure 4.12: The Average Change of Conductivity under the right bump in small bending displacement

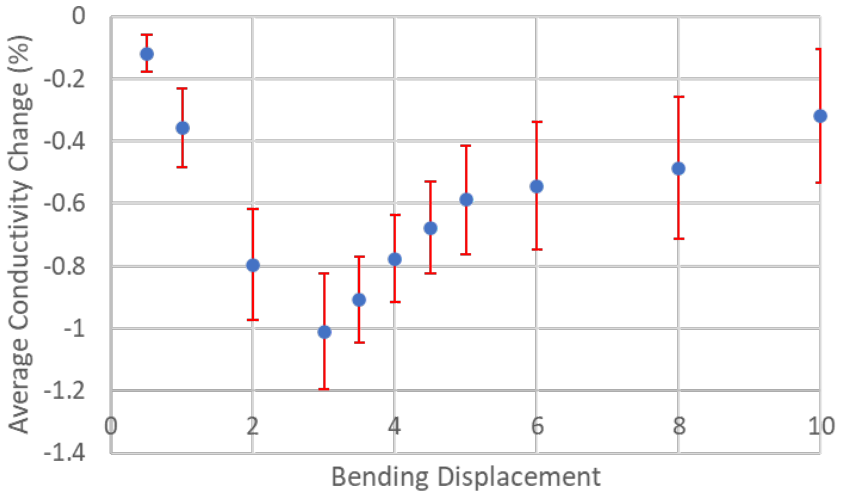


Figure 4.13: The average change of conductivity change pattern at the bumps center of the differential stress distribution pattern in bend test

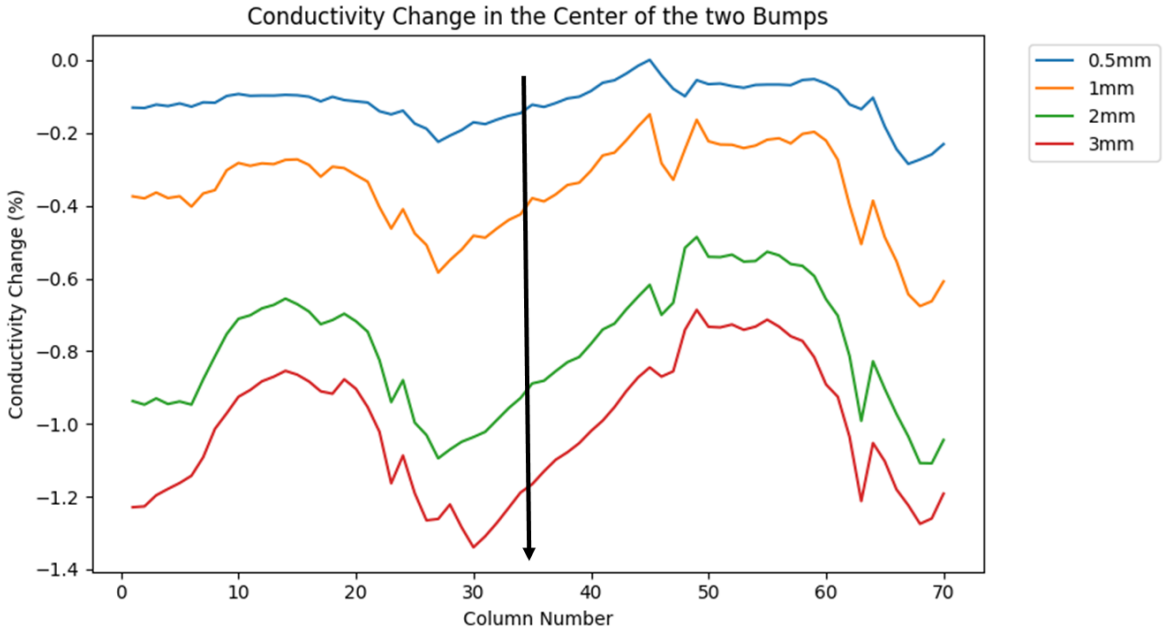


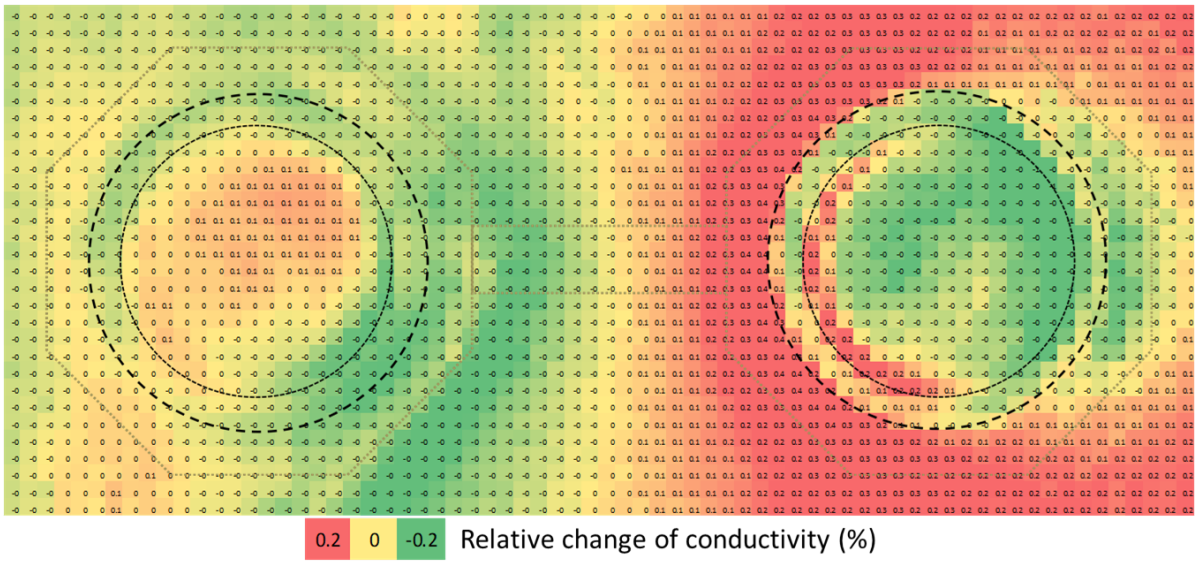
Figure 4.14: The change of conductivity change value at the rows 15 and 16 of the differential stress distribution pattern in small bending, the arrow shows the direction of increased bending stress

solder joints near the edge of the PCB, with continued increase in the bending stress, the edge solder joint first shows a crack and stretch propagate into the solder joints at inner side. With the continued increase in the bending stress, the stretching force of the PCB continues to go toward the center of the die, and because of the superposition of the bent of the die due to unbalance of solder joint stretch stress and the solder joint stretch, the crescent start to appear.

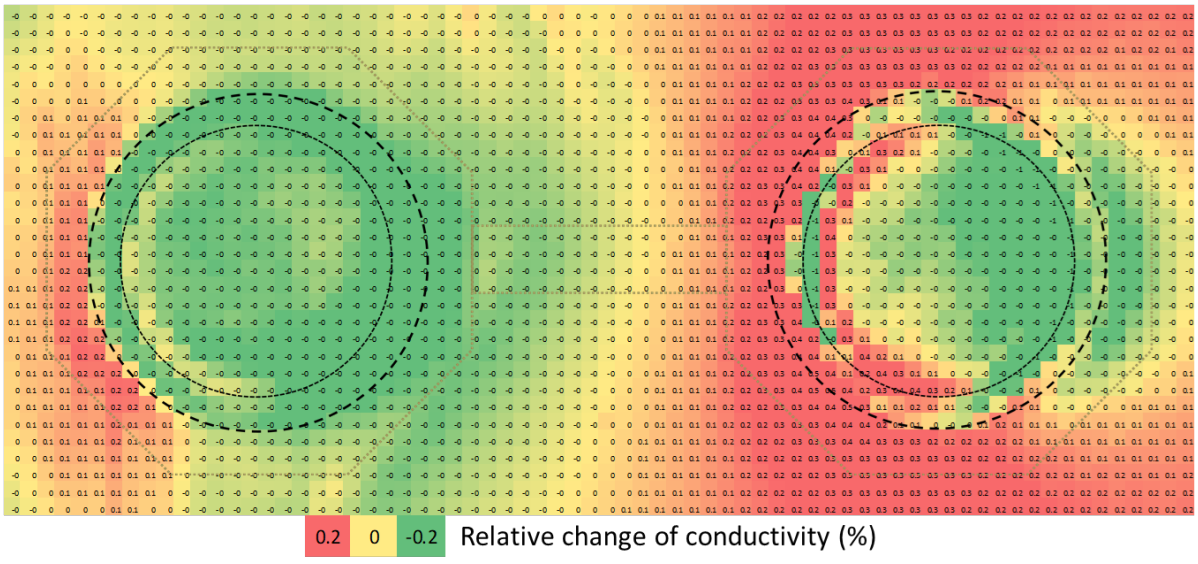
When increasing the bending displacement on the PCB, the behavior deviates from that depicted in figure 4.12. The subsequent figure 4.15 displays three outcomes after subjecting the PCB to elevated bending displacements. Notably, there's a small crescent region at the left edge of the solder joint. This region, absent in figure 4.11, is likely due to the crack of the solder joints near the edge and the stretch stress to bend the die transferred to the solder joint we are monitoring. The figure 4.15c also reveals that with further increased bending stress, a similar crescent appears on the right bump. In summary, during a PCB bending test, stress initially manifests in the whole region of solder joints. As bending stress escalates, the edge solder joints crack and stress propagation moves inwards. With further stress, the solder joint that undergoes most of the stretching force proceeds toward the die's center. This induces a crescent formation.

We can also plot the change of conductivity at the horizontal center side of the solder joint, as shown in figure 4.16 we can see the spark around columns 48 and 23 which is the reflection of the crescent and shows the mutation of the stress distribution. The area around column 48 even shows violent fluctuations, that's can be an indication of the initialization of the right solder joint starting to crack. If we look at the left bump, we can somehow see the area around column 23 shows a similar change trend, which can tell us the same crack process and initial crack will start to develop if we can continue to increase the bending displacement.

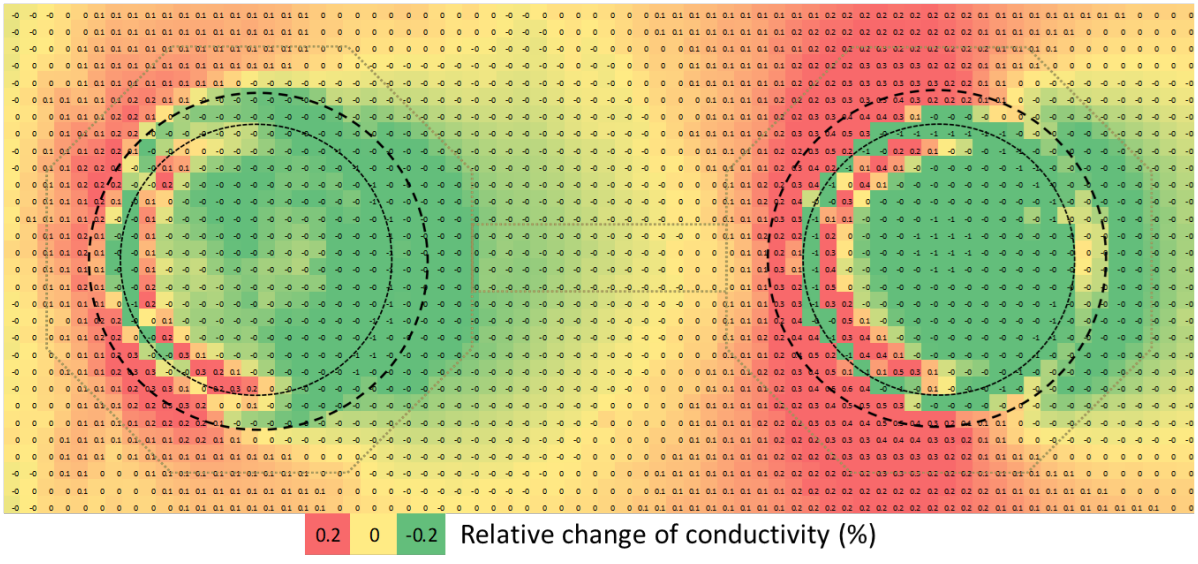
In the cross-sectional analysis of the PCB post a 10mm bend, as illustrated in the respective figure 4.17, cracks are evident in the solder joints at the PCB's edge, and with the location goes inside the die, a lower amount of damage was observed. These cracks are likely attributable to the elevated bending stress and explain the observed high-stress variations beneath the



(a) Stress distribution pattern change after 4mm bending



(b) Stress distribution pattern change after 5mm bending



(c) Stress distribution pattern change after 10mm bending

Figure 4.15: The piezoresistive measurement results in large bending compare to no bending state

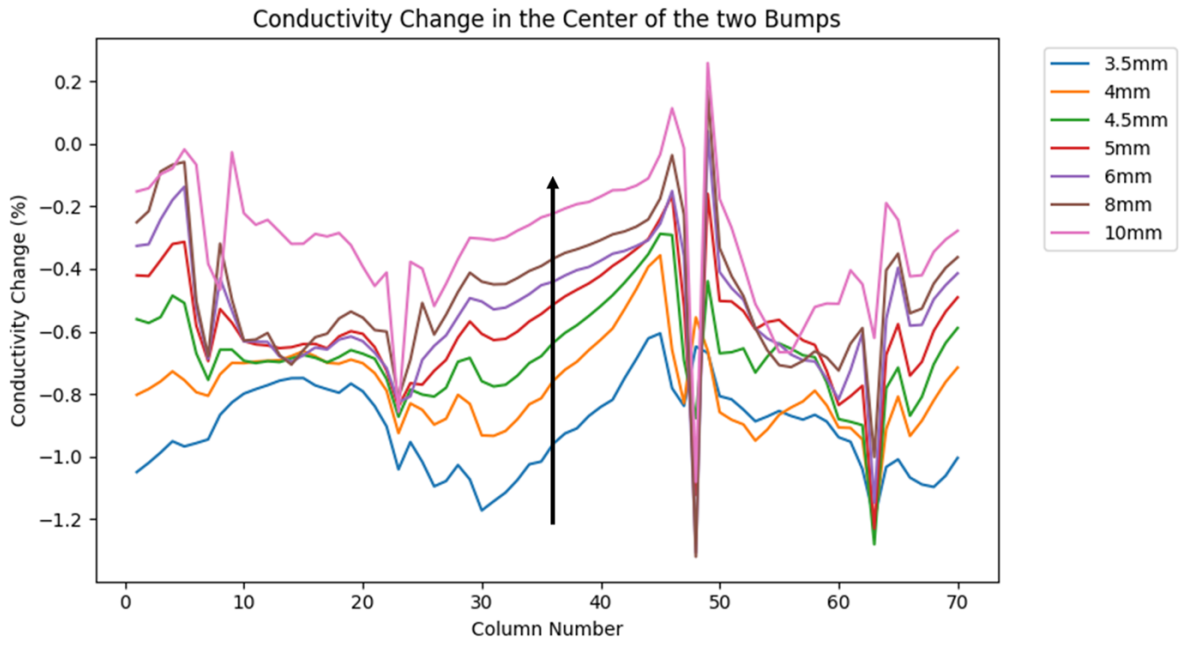


Figure 4.16: The change of conductivity change value at rows 15 and 16 of the differential stress distribution pattern in high bending, the arrow shows the direction of increased bending stress

monitored solder bumps after the solder bumps near the edge cannot hold the stretch stress. A crack initiation point is observed in the left edge of the right bump equipped with piezoresistive sensor cells, which can correlate with the sharp conductivity change shown in figure 4.16 and we can conclude that the sensor is capable to detect solder bump failure near to it and crack initiation under the bumps with sensor cells.

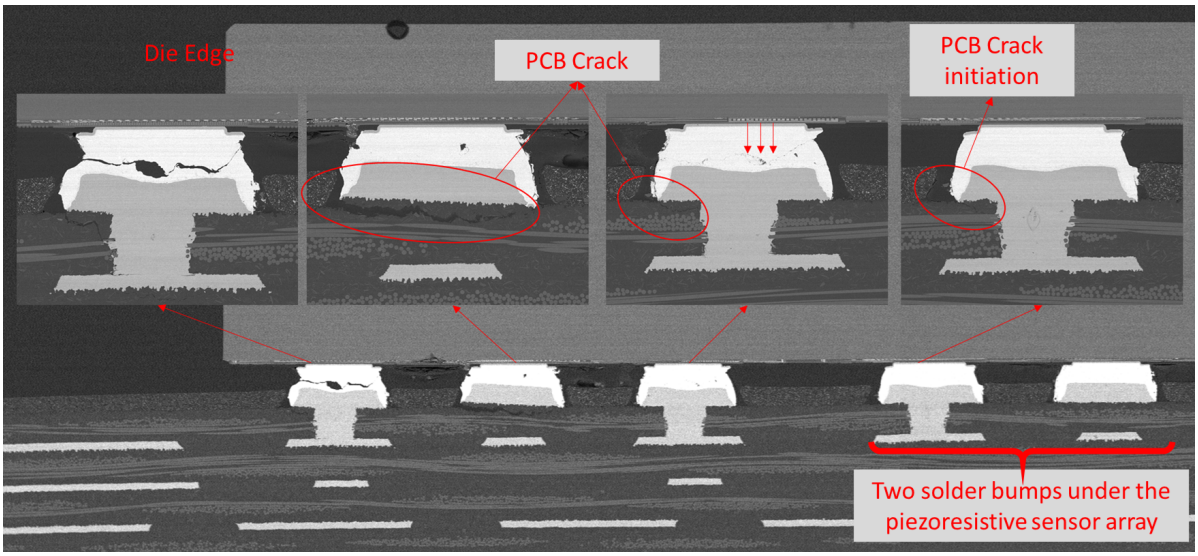


Figure 4.17: The cross-section SEM photo of the piezoresistive sensor WLCAP9 test vehicle after 10mm bend test

4.2.3. Temperature-coupled Bending Test Result

In total four displacements (0mm, 0.5mm, 0.75mm, and 1.1mm) and 11 different temperatures are adopted, but not all displacement and temperature combinations have the test result. The data process procedure is the same as the previous bend test, we subtract the stress distribution pattern from the 0mm bending state at room temperature. The test result is shown in appendix A

From figure A.1 to figure A.3, we can see the increase in temperature under the same 0.5mm bend result. From these plots, we can see the change in stress change pattern in low and high temperatures. It's clear the region under the bumps first recovered from the green shade on the region under the bump, and with temperature increase, the shade become red, which means the stress change in one direction. That's a very clear influence of the mismatch of CTE (Coefficient of Thermal Expansion). At low temperatures, the solder joint can stretch the die toward the center of the die, whereas, at high temperatures, the stretch is in the other direction. The difference on the edge of the die can also be because of the stretch stress change in different temperatures.

Moreover, we can also look at the influence of the superposition of temperature change and bending. In figure A.4, two plots are displayed. Figure A.4a displays the stress distribution shift pattern at 125 °C with 1mm bending test, and figure A.4b shows the sum of zero bending stress pattern shift at 125 °C and 1mm bending test at room temperature. We can see the color in figure A.4a is darker than figure A.4b, which can tell us that the influence on the stress, when we couple the thermal and mechanical test together, can cause more stress combine to do these two types of data separately. That's can give us the impression that doing the temperature-coupled mechanical test is important in reliability tests because, in the real application, the mechanical stress is always coupled with thermo stress, and making the reliability test closer to the environment in the real application can good for the accuracy of the test result.

4.3. Thermal Cycle Test

4.3.1. Test Setup

As introduced in section 4.3, we can use the thermal cycle chamber to do a thermal cycle test. The only thing we need to do is to connect the high-temperature resistance cable and fix the PCB on the fixture inside the chamber. Then the chamber will automatically run with the desired program and start the thermal cycle. We put one QFN test vehicle PCB, two small WLCSP36 piezoresistive sensor PCB and one big WLCSP36 piezoresistive sensor PCB inside the chamber and continue to do in-situ measurements on the electrical response.

4.3.2. QFN Test Vehicle

After we developed the resistance measurement method with the datalogger, we have the capability to continue monitoring the resistance of all 24 solder joints in one PCB. To further understand the relationship between the crack growth and resistance increase and other response during the thermal cycle process, we took the three components out from the chamber by laser cutting separately so we can look at the physical states in different stages of the thermal cycle.

One resistance measurement result from the thermal cycle is shown in figure 4.18, we can clearly see the change in the resistance with different temperatures. In each cycle, the high resistance is the resistance over high temperatures, and the low resistance is the resistance of the solder joint in low temperatures. From figure 4.18 we can also see, with the increased time of the thermal cycle test, the resistance value in high and low temperature also increase. This can be because the crack starts to develop inside the solder joint, the growth of the Intermetallic Compound (IMC) layer, or changes in the microstructure of the solder.

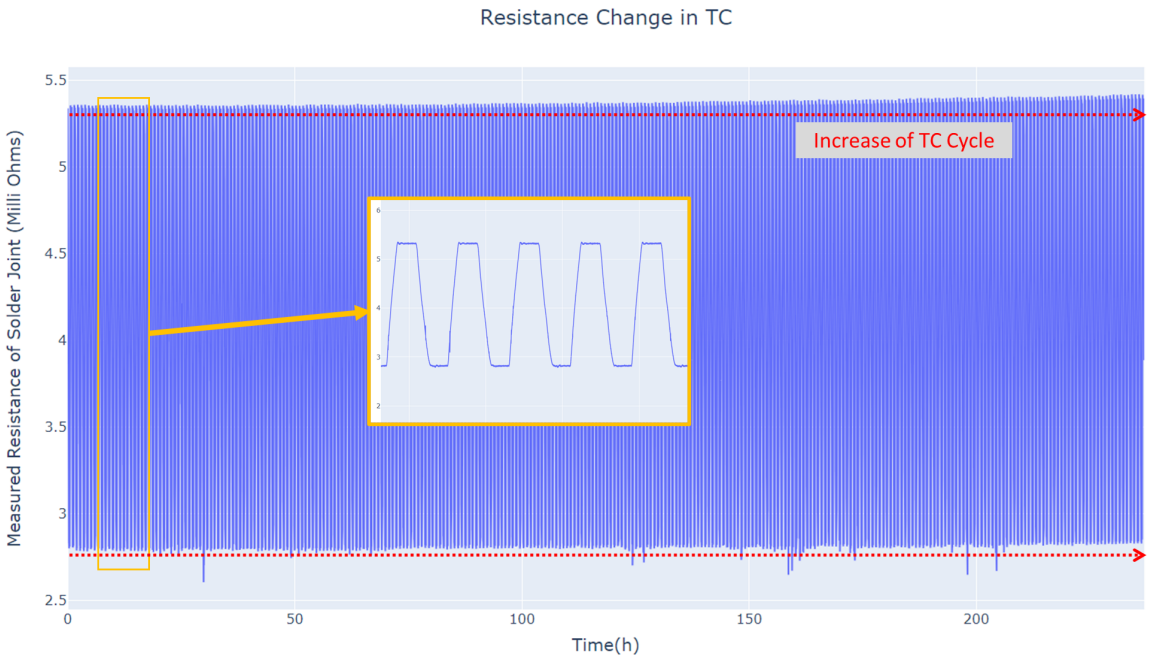
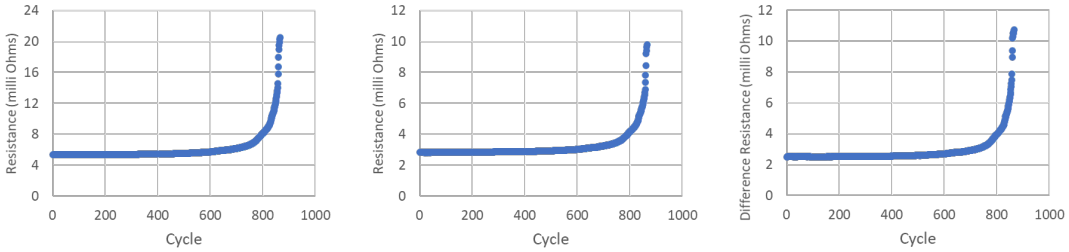


Figure 4.18: An example of the solder joint resistance during the thermal cycle test. The resistance value both influenced by the change in ambient temperature and the degradation of the solder joint

We can look at the whole process of the solder joint during the thermal cycle test. For one solder joint, the resistance change at high temperature, low temperature, and differential of high and low temperature during the thermal cycle test are plotted in figure 4.19. We can see for the last 200 cycles, the resistance rapid increase and the failure analysis also shows full crack results.



(a) The resistance in high temperature with increase of thermal cycle number

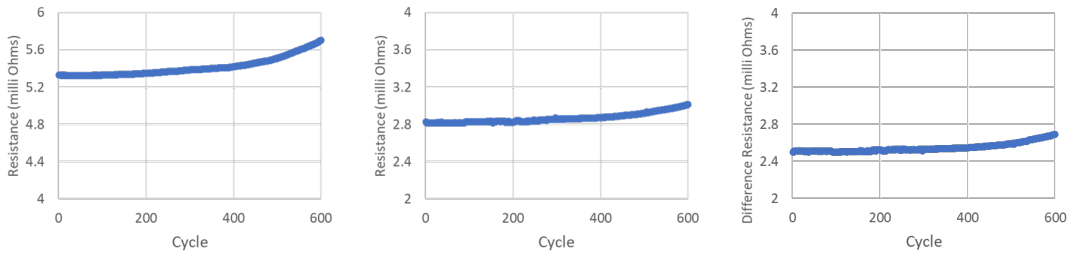
(b) The resistance in low temperature with increase of thermal cycle number

(c) The resistance difference in high and low temperature with increase of thermal cycle number

Figure 4.19: Resistance value change of one solder joint in the thermal cycle test

If we zoom in on the initial 600 cycles of the result shown in figure 4.19, we can find the initial small resistance change of the solder joint, which is shown in figure 4.19. We can see after the thermal cycle test start, the resistance of the solder joint will first stay stable for a while and then start to increase. This stable region can be found in both resistance in high and low temperatures. The initial stable state can be treated as the solder joint didn't show damage, or we can call this region the failure-free region. However, more physical analysis like microstructure analysis is required to give further conclusions on the solder joint state. For the resistance increase region, most of this change can be attributed to the growth of cracks in the solder joints. Several cross-section photos show the crack process shown in figure 4.21, where

we can see the solder crack in the QFN package will initiate from the edge of the package and propagate toward the PCB, then the crack will propagate along the bottom of the package and until the end of the solder area and shows a full open. When the crack grows all the way through the solder joint, a high resistance result will occur, and we can treat that region as a failure. Then it's clear that the resistance change will be very quick at the last several cycles in figure 4.19. The conducting area becomes shorter and shorter, and results in the resistance emotionally increasing.

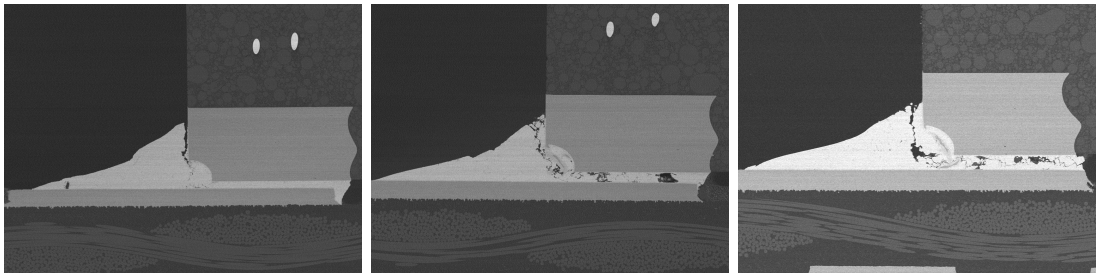


(a) The solder joint resistance change in high temperature for the first 600 cycles

(b) The solder joint resistance change in low temperature for the first 600 cycles

(c) The resistance difference in high and low temperature for the first 600 cycles

Figure 4.20: Resistance value change of one solder joint during initial 600 cycles in TC



(a) Cross-section photo shows the crack initiate of solder crack in TC

(b) Cross-section photo shows the crack propagation in TC

(c) Cross-section photo shows the full crack of solder crack in TC

Figure 4.21: Cross-section photos show the solder crack propagation during the thermal cycle test

If we look again at figure 4.19 and figure 4.20, we can also find the resistance surge at higher temperatures exceeds that at lower temperatures. To validate this, we can graph the resistance difference between high and low temperatures for each cycle, which is plotted in figure 4.19c and figure 4.20c. This data suggests that as the solder joint degrades, the resistance disparity between high and low temperatures expands. This variation in resistance could serve as a physical parameter in modeling solder joint degradation.

4.3.3. Piezoresistive Sensor Test Vehicle

Two small WLCSP36 PCB (PCB1 and PCB2) are used to do the TC test. The implementation of two WLCSP36 piezoresistive sensors inside the thermal cycle chamber produced intriguing results. Notably, one of the smaller WLCSP36 PCBs failed to produce any measurements after 600 thermal cycles. Upon comparing the evolution of the stress distribution patterns across these cycles, a discernible trajectory emerges. This evolution in stress distribution is comprehensively cataloged in appendix B.

After the start of thermal cycling, there are a lot of changes in the stress distribution pattern. As the cycles progress, this alteration not only becomes more pronounced but also encompasses more locations. Figure B.3 illustrates a significant discrepancy: the stress shift at

lower temperatures exceeds that at higher temperatures. This disparity can be ascribed to a couple of plausible explanations.

First, at lower temperatures, the deviation from the reflow temperature is substantial. Consequently, the CTE mismatch stress peaks, exert considerable strain on the solder. Even a limited number of cycles under these conditions can manifest tangible damage.

Secondly, the intrinsic resistance of the sensor cell is susceptible to temperature fluctuations. Therefore, given identical stress levels, the relative shift in conductivity can vary depending on the temperature. This further underscores the intricacies involved in interpreting the results, necessitating careful consideration of both the mechanical and the material properties of the system.

If we obverse all processes of stress change during the whole process. At the outset, evident alterations are noticeable at the die's edge and the lower-right corner of the left solder joint, as depicted in figure B.2. This can be due to the initial few cycles, repeated stretching of the bump leads to crack initiation. Concurrently, the die edge experiences some stress relief as the solder joint becomes more malleable, resulting in reduced conductivity at the die's edge.

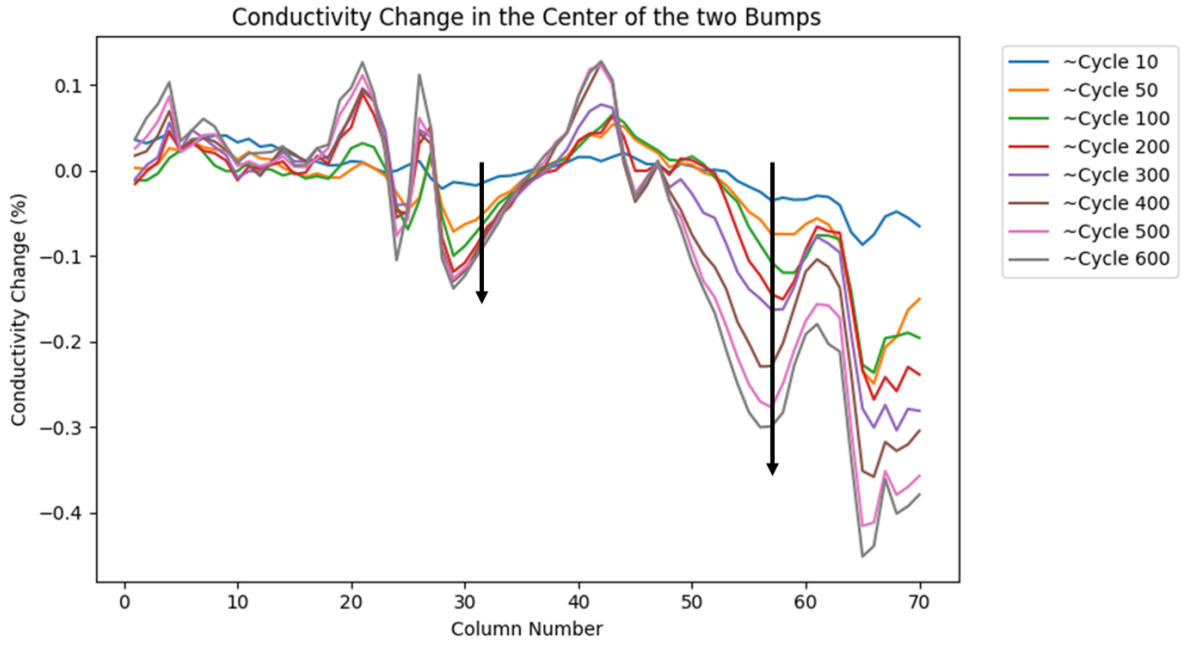
Subsequently, by the 200th cycle (as shown in figure B.4), the color intensity deepens, implying an increased influence on both the solder joint degradation and the die release. This is logically consistent: with an increasing number of thermal cycles, the damage escalates.

By the 300th cycle (presented in figure B.5), the left bump exhibits an inward spread of the red shade. This suggests that damage has penetrated towards the solder joints closer to the center, subsequently affecting the stress profile of the interconnecting regions between solder joints.

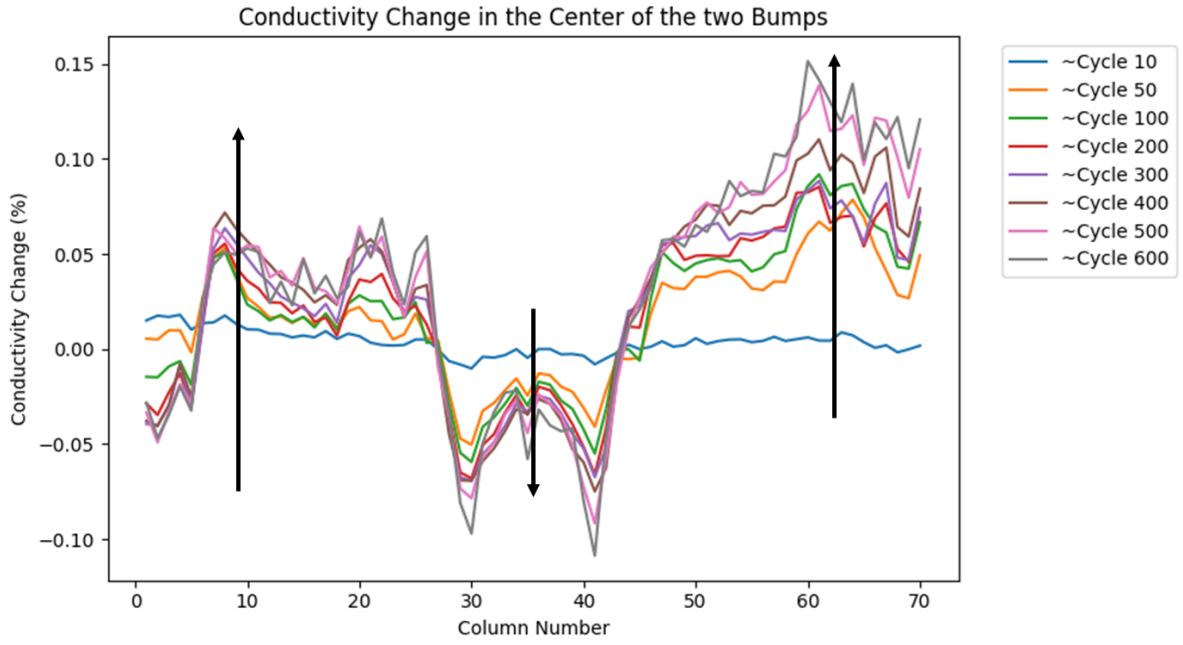
In the concluding 400 cycles, this stress alteration intensifies. Ultimately, nearly all solder joints proximate to the edge of the package exhibit stress changes shift, with stress redistribution on the left-side solder joints. It's also observable that when stress diminishes on one side of a solder joint, it escalates on the opposite side. This behavior hints that the solder joint hasn't cracked completely.

We can also try to decrease the dimension of the dataset to get results into curves. One method is the same as the bend test result. We look at the conductivity change at the center of the two bumps, and the result of the conductivity change at the center of two rows for the result shown in appendix B are plotted in figure 4.22. We can obverse that due to the stress introduced by CTE mismatch is not along the long edge of the PCB, the change direction of the curve in different locations is different. At both temperatures, the edge of the die can suffer more stress compared to the region inside the die. However, the conductivity change values are different and this difference is more in low temperatures, which can be because there is more stress in low temperatures especially in the edge bump because of the CTE mismatch. We can also clearly see the spikes growth in the curve, which can be because of the crack of other solder bumps and cause the redistribution of the stress.

To capture more information and include all cycles during the TC test, we can look at the average conductivity shift of each cycle. Because in the thermal cycle test, the main stress is not coming from the horizontal direction as in the bend test, and we can also obverse from figure 4.22 that the change of the conductivity in the different area along the horizontal center of the sensor can towards different directions. Therefore, we should not use a horizontal line as the direction we extract the average conductivity change. We can notice that the direction of thermal expansion will always be toward the center of the die, so we can look at the conductivity change in the opposite diagonal direction (from F6 to A1 direction in figure 3.6) of the bump. The average conductivity change value of the cells along the opposite diagonal direction is calculated and the plot over cycle number is plotted in figure 4.23, this plot only considers the opposite diagonal of the right bump. We can see from figure 4.23a that the conductivity shows



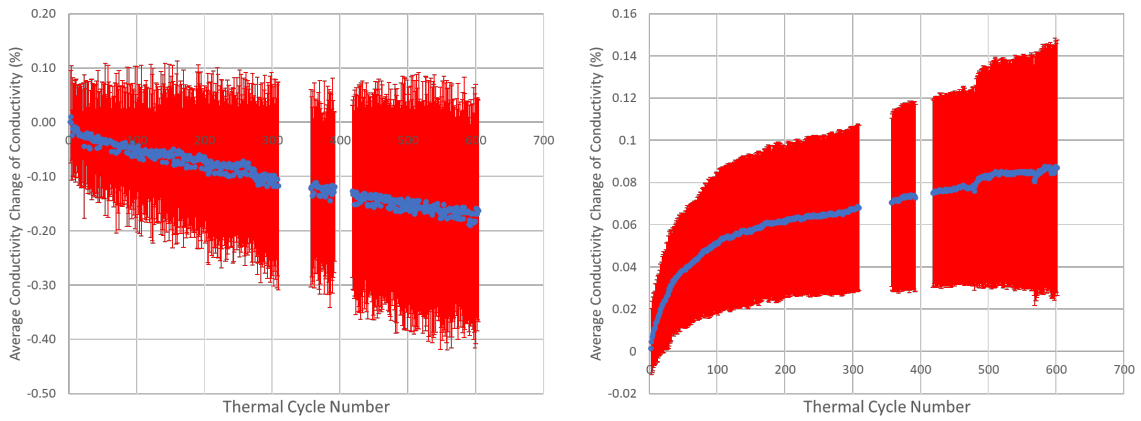
(a) Result for low temperature in thermal cycle test



(b) Result for high temperature in thermal cycle test

Figure 4.22: The change of conductivity change value at rows 15 and 16 of the differential stress distribution pattern during the thermal cycle test, the arrow shows the direction of increased cycle number.

a decrease with the thermal cycle and in figure 4.23b shows an increase in conductivity over time. Notably, the standard deviation of the cells over the opposite diagonal of the bump also increases, these two parameters can be used to reflect the health of the solder joint.



(a) Average Conductivity change in the diagonal of the right bump in low temperature

(b) Average Conductivity change in the diagonal of the right bump in high temperature

Figure 4.23: Average Conductivity change in the diagonal side of the right bump during the thermal cycle

We can also look at the differential of the average value in high and low temperatures and plot them over temperature, to make a comparison, both results from PCB 1 and PCB 2 are plotted together. In figure 4.24 the difference of conductivity change in high and low temperatures are plotted over thermal cycle number. We can see that both the two PCBs can show similar trends, and the increased speed of PCB 2 is lower than PCB1, which can be due to the bump shape being different. In PCB 1, the bump size is smaller and more like a cylinder, but in PCB 2, the bump shape is more like a sphere, which happens in real applications; more pictures of the bump shape can be seen in figure 4.25 and 4.26. In figure 4.24 we can see the result of PCB2 is not as smooth as PCB1, which is because of the noisy measurement data. This noisy result may be due to the position of the PCB inside the chamber being changed to an unstable region (somewhere far from the center) and the instability in temperature can make measurement data not noisy and unstable.

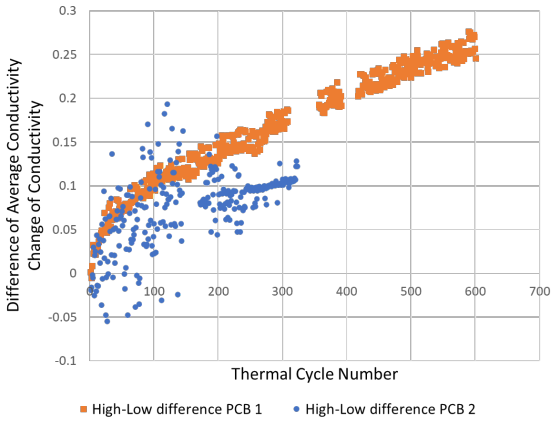
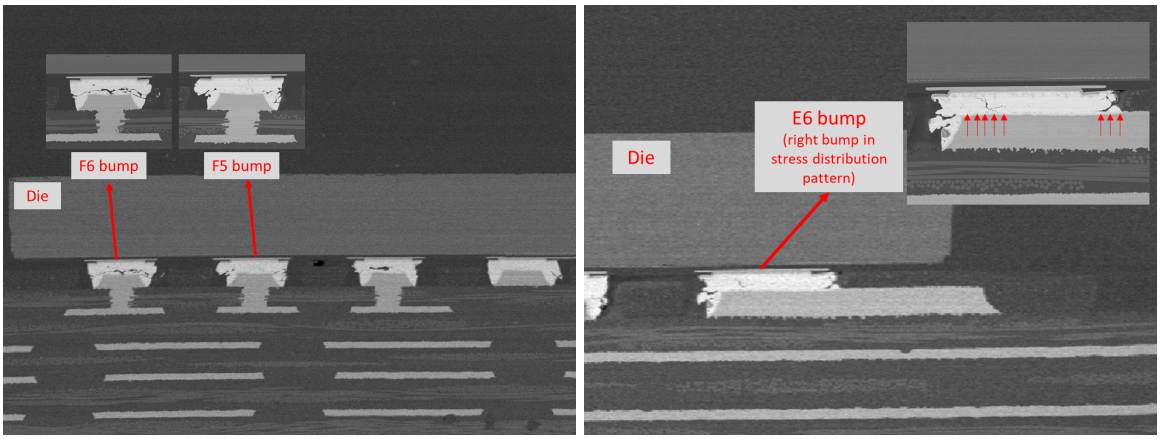


Figure 4.24: The difference of average conductivity of opposite diagonal direction of the right bump over high and low temperatures in PCB 1 and PCB 2

The failure analysis result of the two is shown in figure 4.25 and figure 4.26. We can see that pin F6 in figure 3.6 shows a full crack from figure 4.25a, this is the *VDD* connection of the

sensor, which is the reason the sensor shows a failure in measuring. Moreover, this crack can lead to the unbalance of the other solder joints inside the die, which can be the reason that the right bump edge shows a shift in the pattern. We also see a partial crack in the right bump from figure 4.25b, which can increase the green shade. The combination of these effects can lead to the whole right area showing green. For PCB 2, in figure 4.26, similar crack areas are found, and that can explain the value change trend over the thermal cycle test of PCB2 is also similar to PCB 1.



(a) Cross-section result of row F in WLCSP36 PCB after 600 cycles thermal cycle test

(b) Cross-section result of bump E6 in WLCSP36 PCB after 600 cycles thermal cycle test

Figure 4.25: Cross-section result of WLCSP36 test vehicle after thermal cycle test

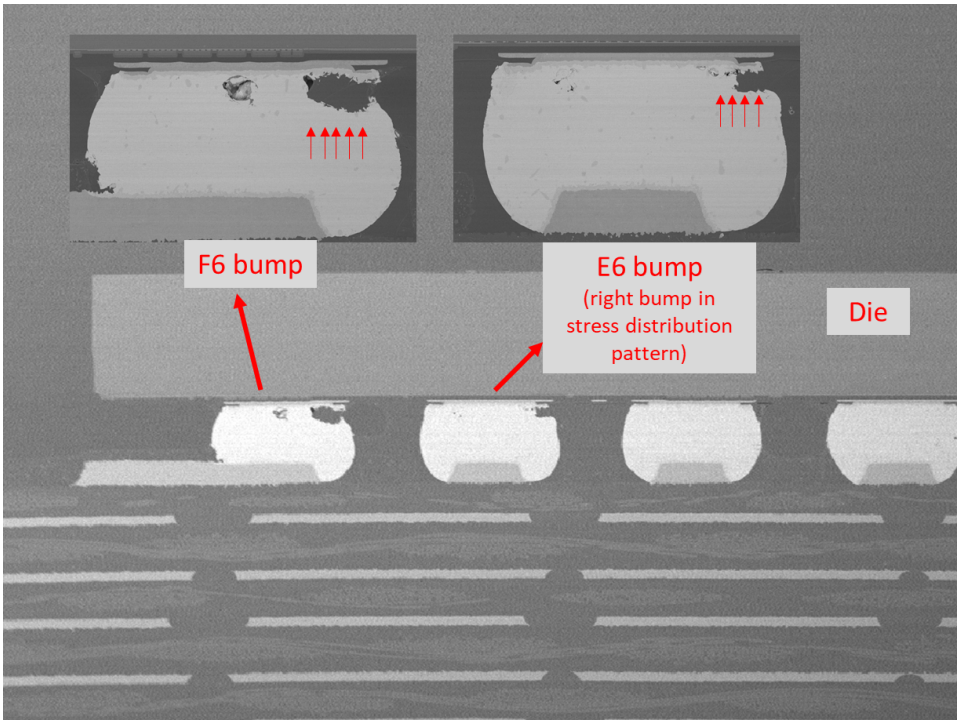


Figure 4.26: Cross-section of PCB 2, which shows partial failure with the bump failed in PCB1

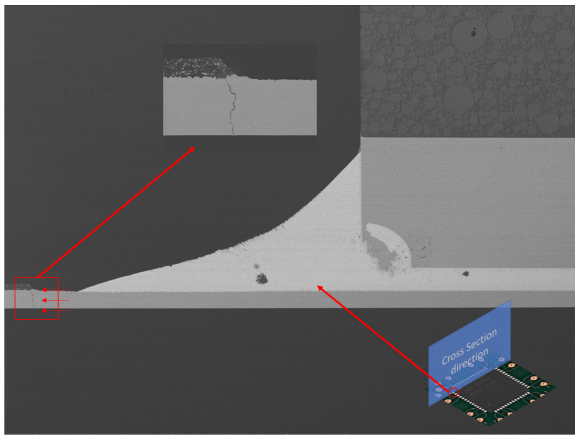
4.4. QFN Test Vehicle Result Statistical Analysis

In this section, some of the cross-section results will be correlated with the electrical measurement result, and try to see the link between them.

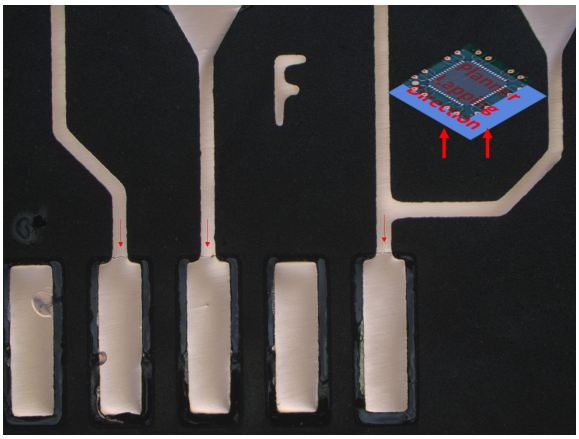
Analyzing the resistance measurement data across all QFN test PCBs provides valuable insights into the critical location of solder joints during vibration tests. A particularly noticeable pattern emerges: a majority of the solder joints that exhibit an open in their resistance measurements are aligned parallel to the long edge of the PCB. This not only underscores the significance of the spatial orientation of solder joints in determining their stress level during vibration tests but also offers an initial indication of critical locations. The position of these solder joints seems to predispose them to increased susceptibility to failure or degradation. In cross-section, as we need to polish part of the solder joints, we will only look at the solder joints along the long edge of the PCB.

Through failure analysis, distinct failure modes were observed in the QFN test vehicles across different reliability tests.

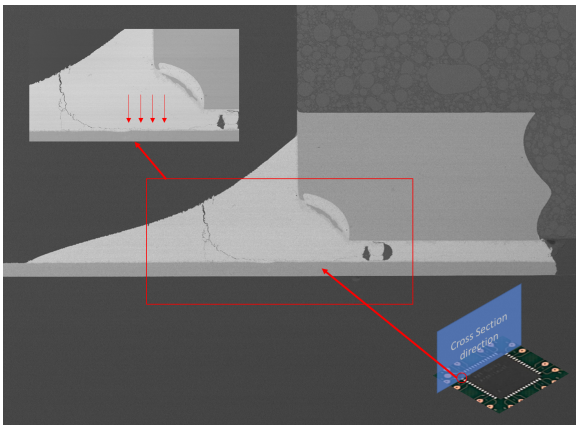
In vibration tests, two principal types of failures emerged. The first mode of failure is associated with the PCB, characterized by fractures on the PCB's copper trace. This can be clearly seen in figures 4.27a and 4.27b.



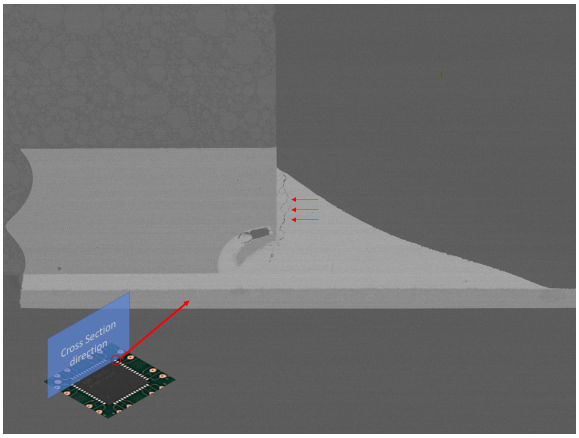
(a) Cross-section result shows PCB crack



(b) Planner lapping result shows PCB crack



(c) Cross-section result shows solder joint crack type 1



(d) Cross-section result shows solder joint crack type 2

Figure 4.27: Some typical failure/degradation results on QFN test vehicle after vibration reliability test

The second mode of failure pertains to cracks within the solder joint itself. Within this category, there are two primary directions of crack propagation.

In the first scenario, as illustrated by figure 4.27c, the crack originates from the sloped section

in the side wettable area of the solder joint. Notably, the crack can then shift its direction and grow parallel to the PCB. This specific kind of solder joint degradation is frequently encountered in these test vehicles.

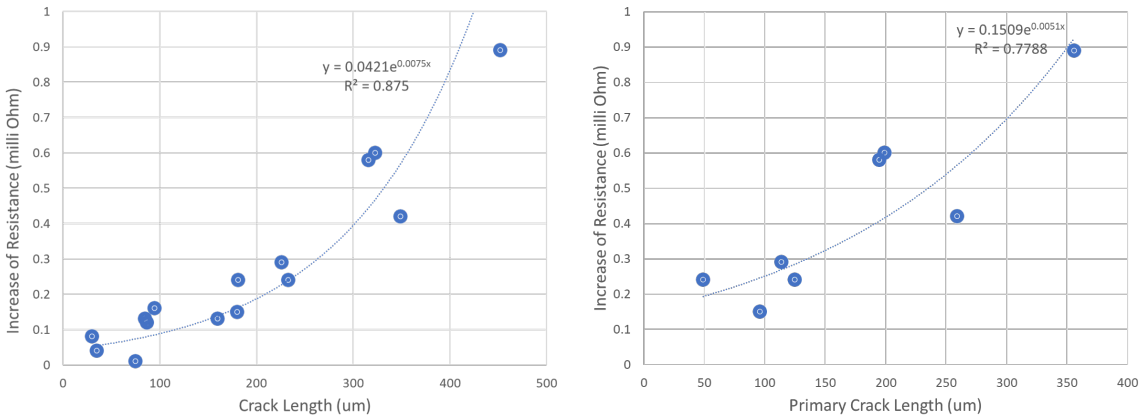
The second type of solder joint crack is depicted in figure 4.27d. Here, the crack commences close to the package wall and advances downward. This particular form of degradation is exclusive to the side A component of the QFN test vehicle. This could potentially be attributed to elevated stress concentrations on the solder joint in that region.

Interestingly, a subset of samples showcased a confluence of both PCB cracks and solder joint cracks, emphasizing the interconnected nature of these failures and the cumulative stresses the system endures during testing.

An interesting observation was made when looking at the cross-sectional images and planar-lapping images: a sudden spike in resistance measurement was invariably associated with a crack in the PCB. Intuitively, if either the sense or force line becomes disconnected, resistance measurement would not be possible, resulting in an infinite reading due to either skyrocketing voltage or plummeting current.

In analyzing the remaining resistance measurements in tandem with cross-sectional images, an effort was made to quantify the extent of the cracks. For the cracks of type 1, as visualized in figure 4.27c, measurements were taken of both the crack length extending towards the PCB's surface and the length of the crack running parallel to the PCB. The aggregate crack length was determined by summing these two measurements.

Figure 4.28a elucidates the correlation between the overall crack length and the rise in resistance measurements. An evident positive relationship exists between crack length and resistance augmentation. An exponential relationship is believed to be a good way for fitting the curve because the resistance increase can first be slow and will be very sharp before the full crack of the solder joint. However, employing an exponential regression method did not yield an optimal fit, possibly due to insufficient sample size.



(a) The relationship between total solder crack length and resistance increase

(b) The relationship between parallel to PCB solder crack length to resistance increase

Figure 4.28: Relationship between the resistance measurement and solder joint crack length

Upon solely considering the crack length that runs parallel to the PCB — which can extend underneath the package — we are presented with figure 4.28b. This figure also mirrors a similar trend between crack length and resistance increment. Comparing these two charts as presented in figure 4.28, it becomes evident that the crack running parallel to the PCB appears to have a pronounced influence on resistance enhancement. This could very well be the principal factor causing solder joint disconnections.

Armed with this regression model, it becomes feasible to anticipate the crack's length based on variations in resistance.

We also use sample simulation to look at the change in resistance with the increase in crack length. The picture that shows the simulation model is shown in figure 4.29. This model is a 2D model, which means we consider the crack is all the way through and that can be a deviation of the real circumstance. The simulation result can show the percent of resistance increase verse crack length. If we consider the initial solder joint resistance as the same value shown in figure 3.8, we can plot the simulated resistance change over the crack length which is shown in figure 4.30. We can see that the trend is similar between the simulation result and measurement result in figure 4.28a, the difference between them could mostly be attributed to the limitation of the 2D simulation methods. The 2D simulation treats the crack homogenous along the width of the solder joints, and the cross-section can only give us a limited number of pictures of the crack distribution along the solder joints, we cannot measure the length of the crack along the short edge of the solder joint.

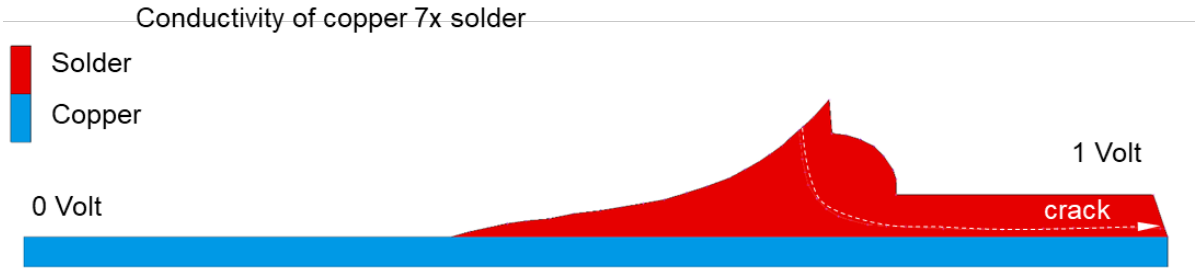


Figure 4.29: Simulation model of the solder crack and resistance increase. A 2D model that considers the crack is all the way through in the cross-section.

The intricacies of solder joint behavior in thermal cycles can be notably divergent from those observed in vibration tests. Notably, solder fracture mechanics in thermal cycles don't align with the mechanical tendencies during vibration analyses. This divergence is especially evident when observing the heterogeneity of solder joint cracks during thermal cycle tests. In the vibration test, due to out-of-plane stress being expected to be more dominant in vibration testing, the crack tends to be homogeneous and distributed on the short edge of the solder joints.

A vivid demonstration of this discrepancy of crack can be observed in figure 4.31. This

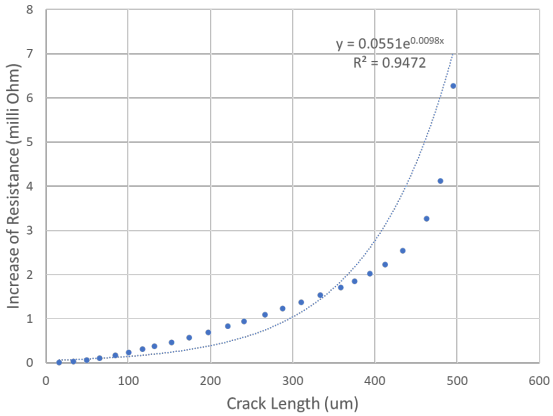
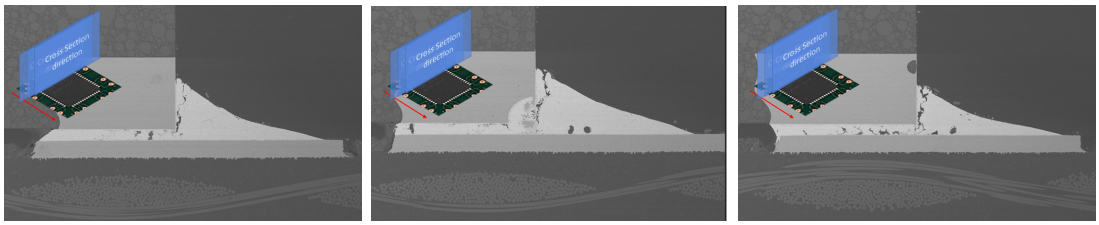


Figure 4.30: Simulation result on resistance change with solder joint crack

figure portrays an asymmetric solder crack distribution on either side of the solder joint's center. Specifically, figure 4.31a reveals minimal cracking, especially when juxtaposed with the more pronounced cracking exhibited in the center of the solder joint shown in figure 4.31b. This discrepancy further escalates when observing figure 4.31c, which showcases even more extensive cracking. Another cross-section photo to demonstrate the difference of solder crack is shown in figure 4.32 [49]. These two cross-section photos are from different directions compared to the direction we normally used. This cross-section is along the short edge of the solder joint, which can see the crack distribution along the short edge of the solder joints and give us a view of how the crack is distributed. In figure 4.32a, we can see the crack always exists along the short edge of the solder joint, however, only part of the solder joint shows the crack in the short edge after the TC test from figure 4.32b, that's can also prove it's risky to use the cross-section photo along the center of the solder joint to estimate the crack area.

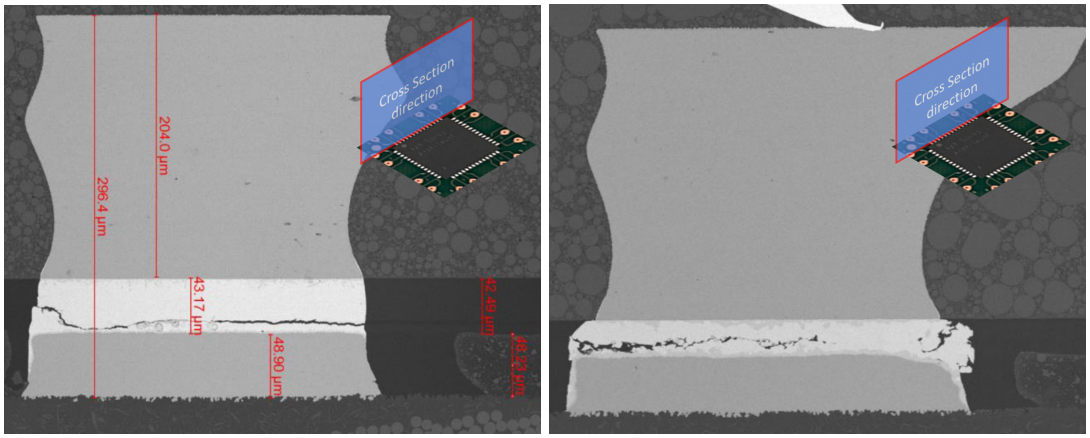


(a) Cross-section picture on the first polish of the solder joint

(b) Cross-section picture on the center position of the solder joint

(c) Cross-section picture on the third polish of the solder joint

Figure 4.31: Cross-section photo after thermal cycle test, three different cross-sections in same solder joints



(a) Cross-section picture along the short edge of the solder joint, after the drop test [49]

(b) Cross-section picture along the short edge of the solder joint, after the TC test [49]

Figure 4.32: Cross-section photo along short edge of solder joints

The implications of such observations are profound. Sole reliance on the cross-section analysis of a solder joint's center doesn't provide an accurate representation of the complete crack area. This makes it difficult to get a similar result as figure 4.28 during thermal cycling. To attain a holistic understanding of the crack area and distribution, more sophisticated methodologies, like 3D X-ray techniques, may need to be employed.

In assessing the failure time of solder joints within the QFN test vehicle, the distribution data provides valuable insight. Board-level reliability tests commonly utilize the Weibull distribution due to their aptitude in depicting an escalating failure rate as time progresses, especially when the shape parameter is greater than 1 — a scenario frequently observed in BLR test outcomes.

The unique attribute of our dataset is its capacity to trace the resistance measurements

throughout the transition from an operational state to failure. This enables not just an examination of the Weibull distribution for failure data but also an evaluation of the degradation distribution over time, giving us the option to discern the duration until the solder joint's resistance augments by intervals of 1%, 5%, 10%, 20%, and 50% (which is also construed as failure). By mapping the distribution of these resistance increasements against time, and subsequently examining the regression data, one can anticipate an increasing trend in the scale factor corresponding to each resistance level.

The analysis primarily focuses on components located on the B side of the test PCB, particularly emphasizing solder joints along the long edge due to their demonstrated vulnerability in our test results.

The graphical representation in figure 4.33 showcases the Weibull plots for resistance increment at 1%, 10%, and failure case. The discernible shift in the scale parameter is evident. Nevertheless, the plots reveal a deviation from a straight line, indicating the failure data does not strictly conform to a singular Weibull distribution, especially when observing a 1% resistance enhancement. Such deviations can be attributed to the varied failure modes observed in figure 4.19. Despite these nuances, the shape parameters across these three curves exhibit consistency. This insight holds potential implications for reducing overall test time by modifying the failure criteria. Moreover, the 90% confidence interval of the scale factor is listed in table 4.3, we can use that to estimate the remaining useful lifetime of the solder joint-PCB interface. For example, after we see resistance increase by 1% in the vibration test, we can calculate for the worse case, the solder joint-PCB interface can still survive for $16.0798 - 10.2609 = 5.8189$ hours (difference between lower value estimation of failure and upper and the value estimation of 1% resistance increase). Therefore, we can say we are 90% confident that the solder joint-PCB interface can still survive for 5.8 hours, then we have a chance to get rid of the failure.

Scale Factor	Estimate Value	90% Lower Value	90% Upper Value
1% resistance increases	8.72240	7.41457	10.2609
10% resistance increases	16.4186	14.1327	19.0743
Failure	19.3092	16.0798	23.1872

Table 4.3: The 90% confidence interval in Weibull scale factors

Further examination extended to the drop test outcomes for the identical package years ago [49], which employed a daisy chain as the failure detection mechanism. A notable observation was the presence of two distinct slopes on the Weibull plot, coupled with two distinguishable failure modes. Intriguingly, the scale factor registered at 2.31, closely mirroring our current results. Such parallels suggest that both drop and vibration tests may manifest similar failure modes.

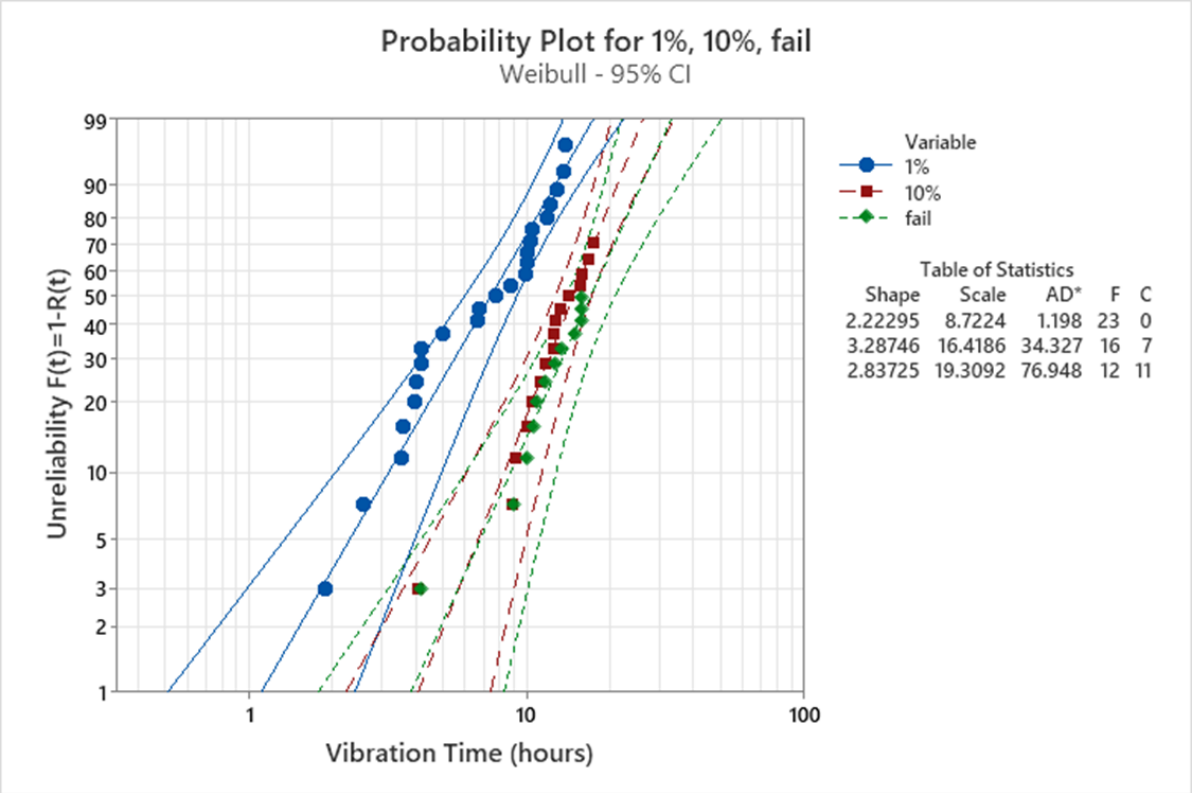


Figure 4.33: Weibull distribution plot for 1% change samples and fail samples

5

Conclusion

This thesis proposed a method developed for monitoring the degradation in the solder joint during board-level vibration test and thermal cycle test. In this chapter, the findings and results are listed, the research limitations are discussed, and recommendations for future work have been made.

5.1. Conclusion

This study aims to develop and assess methods for monitoring and characterizing solder joint degradation during board-level vibration tests and thermal cycle tests. The results have not only validated our methodologies but also provided pivotal insights.

The advanced four-wire resistance measurement technique we developed provided an accurate representation of solder joint resistance. By correlating these measurements with cross-sectional analyses, we were able to distinguish between the primary mechanisms of failure, most notably the PCB copper trace crack and solder joint degradation.

Our resistance measurements offered crucial insights into the location of solder joints that are critical within the board-level vibration test. One key observation was the disparity in solder joint life between side A and side B of the QFN test PCB. This suggested a possibility of extending the component lifespan by ensuring all package pins are soldered. Further, the longevity of solder joints along the PCB's long edge was found to be compromised in the board-level vibration test compared to those on its shorter edge.

A notable deviation was observed in the resonance frequency changing slope during the vibration test when PCB cracks were present. This abnormal trend could serve as an indicator of potential degradation or failure within the PCB or solder joint during the board-level vibration test.

An intriguing observation emerged when comparing PCB #4 and PCB #3, both of which had undergone simultaneous SMT processes. PCB4 exhibited a significantly higher number of PCB copper trace cracks, suggesting the limitations of vibration tests in accurately causing solder joint cracks.

The relationship between resistance increases during board-level reliability tests and solder joint cracks became evident. This correlation enables an initial mapping between resistance parameters and the progression of joint degradation, which can be future used as a parameter to calculate the lifetime of solder joints.

By analyzing solder joint lifetime during vibration tests, we discerned an opportunity to economize on reliability test durations by changing failure criteria. This conclusion is from the Weibull distribution result, a similar shape factor in the Weibull distribution was also

observed in old reports related same package in the board-level drop test. That can tell us the board-level vibration test and board-level drop test can cause similar failure modes and the test results of one could be transferable to the other for the kind of QFN package used in this study.

With the Weibull distribution on the solder joint-PCB interface at different degradation levels, we can conclude the remaining useful lifetime of the solder joint-PCB interface. The scale factor difference between different degradation levels can be transferred into the remaining useful time. This can be a useful technique as we can intervene in the degradation process before the failure happens.

Our exploration into the thermal cycle highlighted the utility of resistance increments as potential markers of degradation. Furthermore, disparities in resistance values between high and low temperatures offered another dimension of understanding the degradation phenomenon.

Our piezoresistive sensor measurement approach showcased flexibility across varied board-level reliability test paradigms. Post validating the sensor's responsiveness to singular stresses in board-level bend tests, its efficacy in detecting stress alterations due to temperature shifts was also confirmed.

The temperature-coupled bend tests brought the chance to compare the critical interplay between mechanical and thermo-mechanical stresses. Their combined influence is significant, inducing higher stress on the test board during BLR tests than when they act individually.

By examining and extracting data from stress change patterns during board-level reliability tests, a visual curve of solder joint degradation was formulated. This condensed data representation holds potential for algorithmic applications such as data-driven methods utilizing machine learning techniques.

In conclusion, our rigorous investigations give additional insights into the solder joint degradation process. These findings would help improve the existing methods used for determining the remaining useful life of solder joints and optimize board-level reliability tests.

5.2. Limitations

The study encountered several limitations that are important to address when considering the findings.

Firstly, our sample size for the thermal cycle test was not expansive, particularly when focusing on the analysis of degradation/failure distribution and the measurement of crack lengths. Future endeavors should consider gathering more results using the established test setup and measurement methods to provide a more robust dataset.

For piezoresistive sensor measurement, it can make worse because of the involvement of the microprocessor in the measurement, not many samples are measured in this project, and because of the difference between the three PCBs in TC tests (different solder bump sizes, different PCB), we cannot provide repeatability and statistical data on the measurement result.

The failure analysis methodology adopted in this project also presents constraints. Due to circumstantial limitations, we predominantly relied on the cross-section method to measure the solder crack lengths. This approach is inherently destructive, which means the investigated specimen must be thrown away. Additionally, it offers merely a two-dimensional perspective of the crack, which is confined to the specific areas chosen for the cross-section. The inclusion of advanced diagnostic tools, such as 3-D X-ray imaging, would undoubtedly enhance the quality of our analysis, particularly when aiming to explore the depth and complexity of the solder crack regions.

Lastly, it is pivotal to acknowledge that our piezoresistive sensors do not offer a direct measurement of stresses, because of the involved calculation and piezoresistive coefficients. This limitation of the piezoresistive sensor make it challenging to discern the directionality of stress changes. Moreover, figuring out the shift of stress from the shifts of the conductivity pattern

can be difficult.

5.3. Future Recommendation

For further recommendation, the first is to design a test PCB, it's recommended to use a more robust design for the PCB, such as adding redundant copper traces or increasing the width of the existing traces. Then we can increase the lifetime of the PCB trace and delay the fracture of the PCB trace.

The second recommendation is utilizing a non-destructive method to look at the solder joint state every 50 or 100 thermal cycles, which could make it easier to link the crack length and the change of resistance.

The third recommendation is to connect in series an ammeter meter to the force ports in the four-wire resistance measurement structure, by precisely measuring the current we can get more accrue resistance measurement results.

For the piezoresistive sensor measurement, it's recommended to perform more reliability tests, especially in the thermal cycle. Checking the repeatability of the readout within the same test condition and sample condition is recommended in the future.

Last but not least, advanced data process methods can be developed based on the method and data developed and collected in this project. Such as anomaly detection and remaining useful life live prediction.

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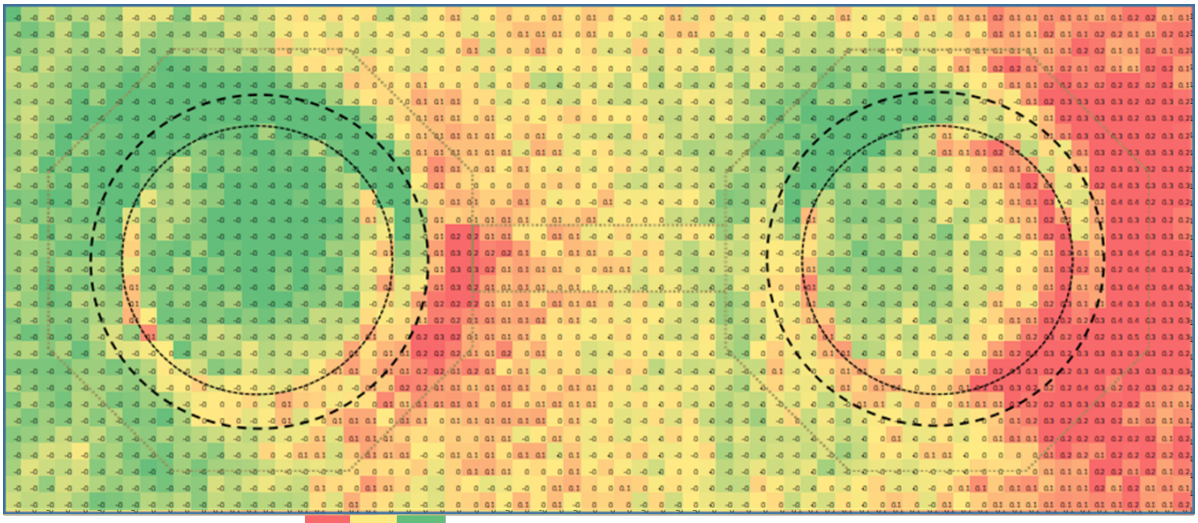
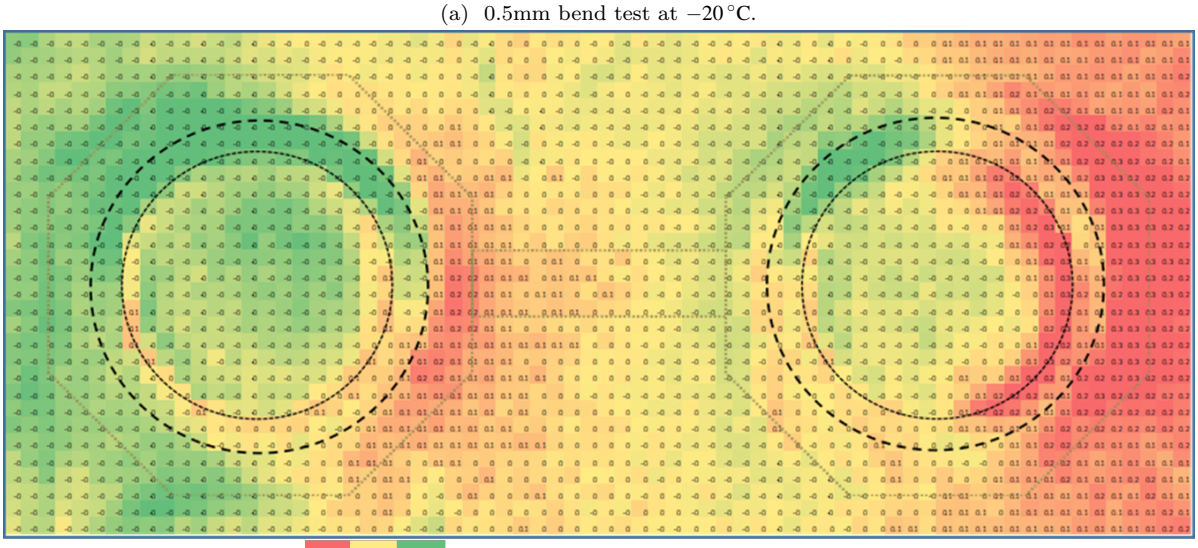
A

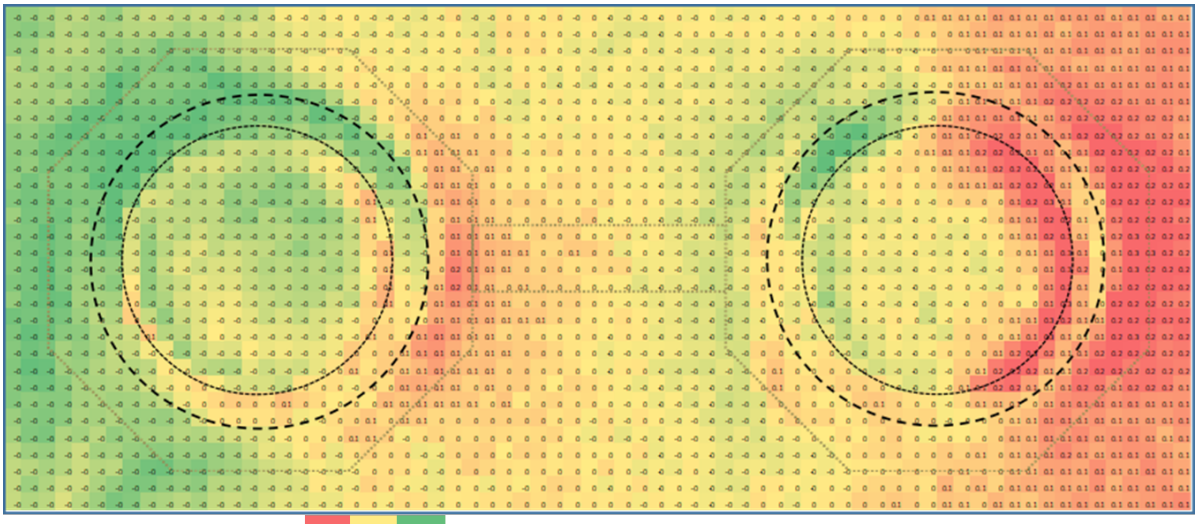
Appendix A: Piezoresistive Sensor Pattern Change in Temperature Coupled Bend Test



(a) 0.5mm bend test at −20 °C.

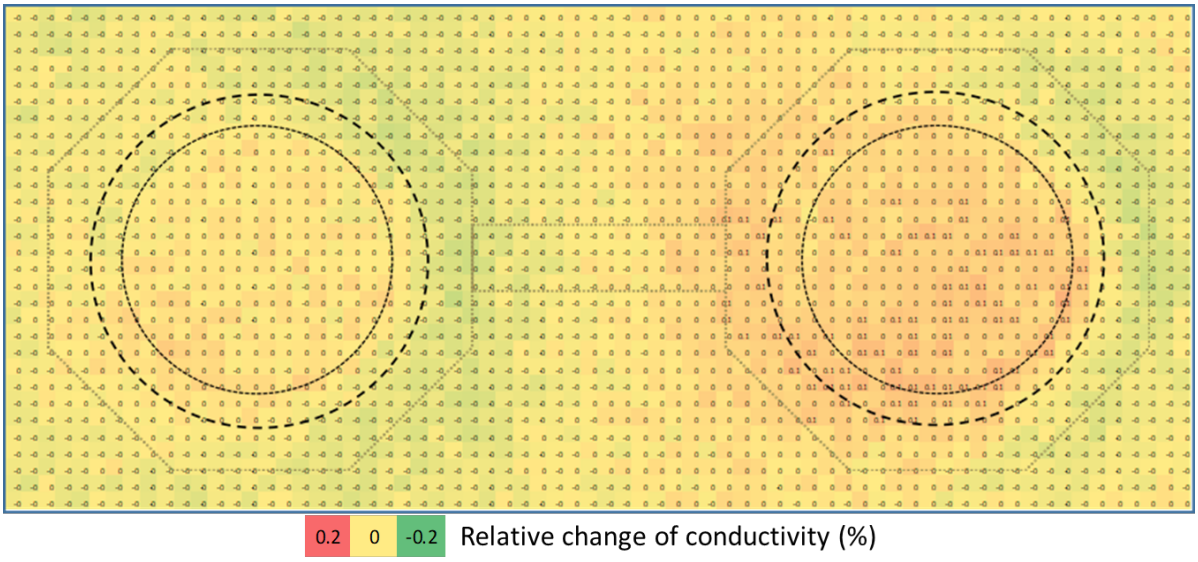


(b) 0.5mm bend test at 0 °C.

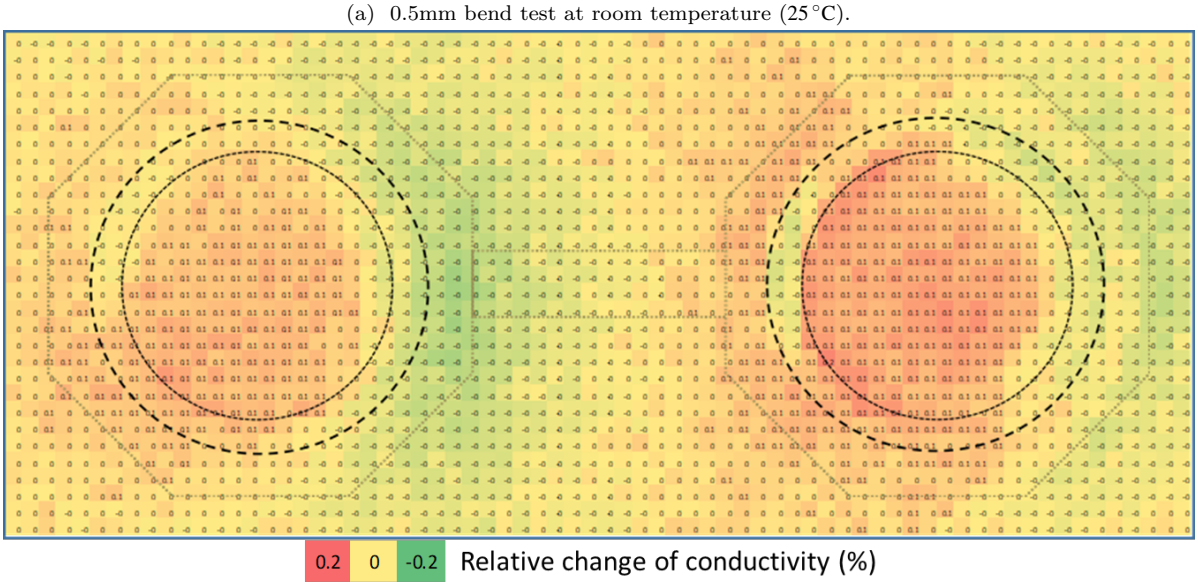


(c) 0.5mm bend test at 10 °C.

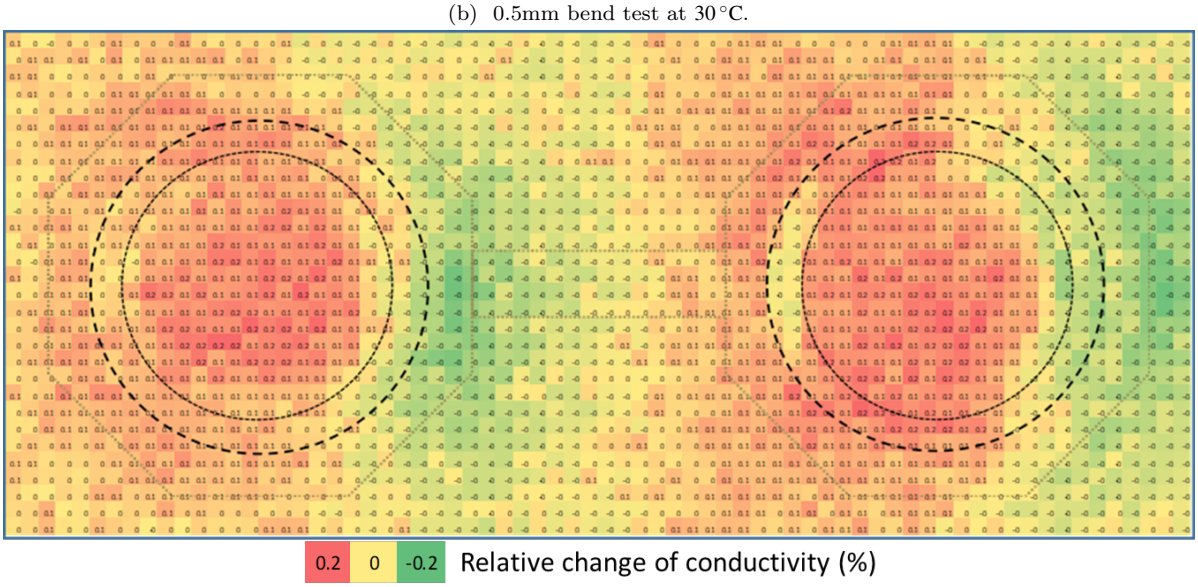
Figure A.1: The piezoresistive sensor measurement result at 0.5mm bend test.



(a) 0.5mm bend test at room temperature (25 °C).

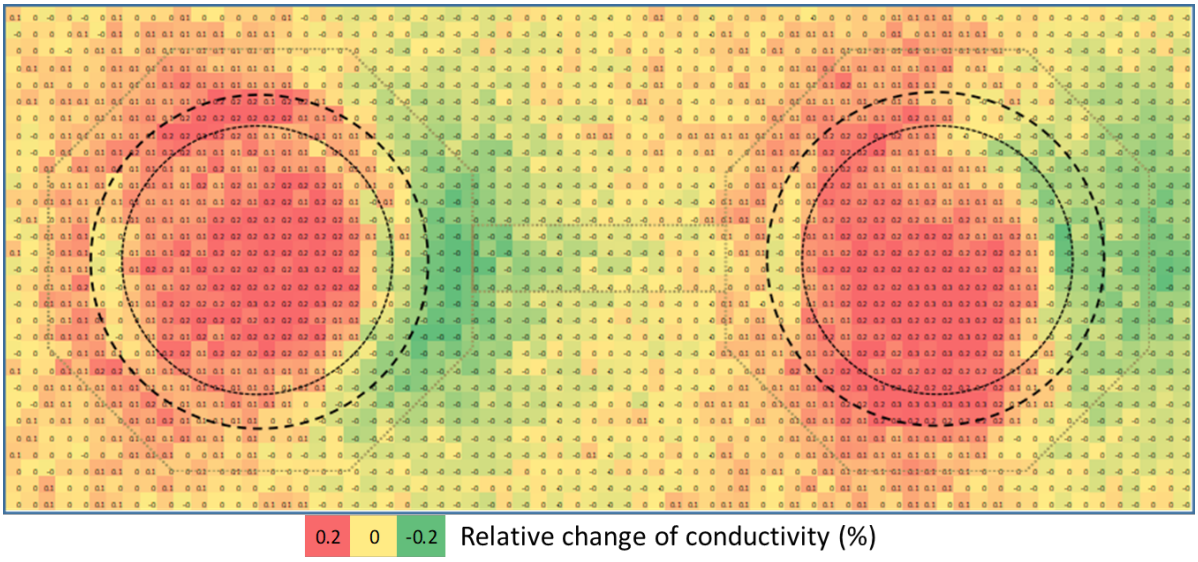


(b) 0.5mm bend test at 30 °C.

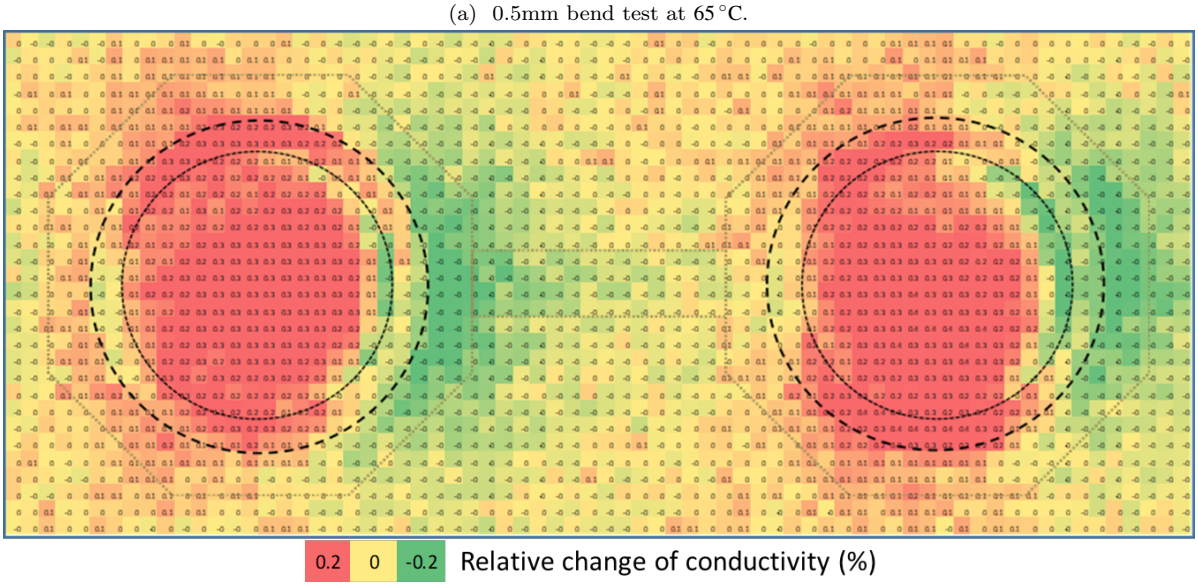


(c) 0.5mm bend test at 45 °C.

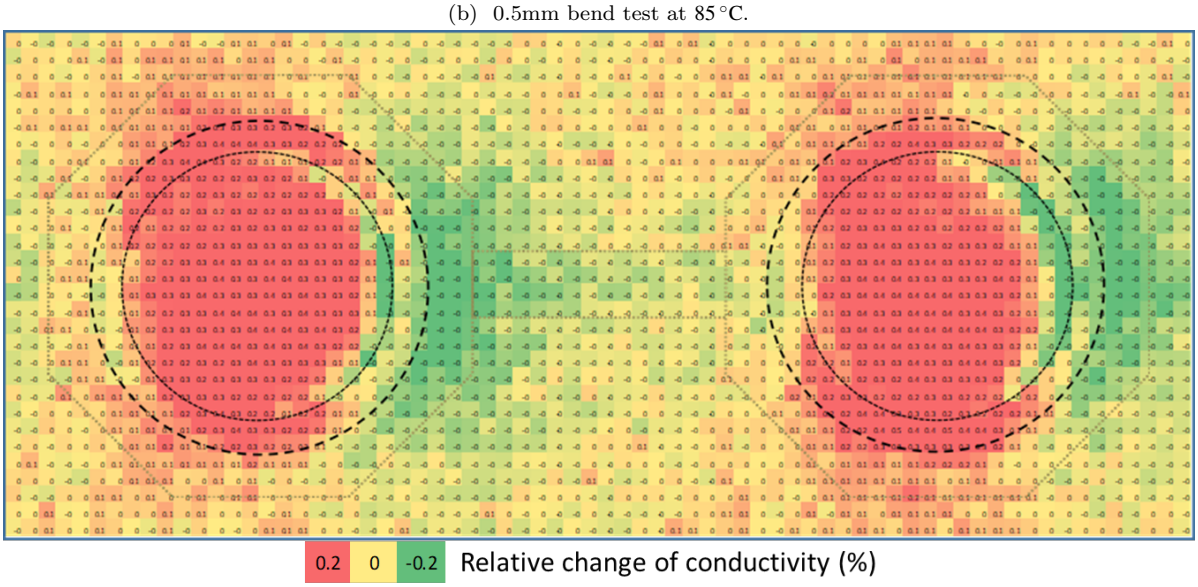
Figure A.2: The piezoresistive sensor measurement result at 0.5mm bend test.



(a) 0.5mm bend test at 65 °C.

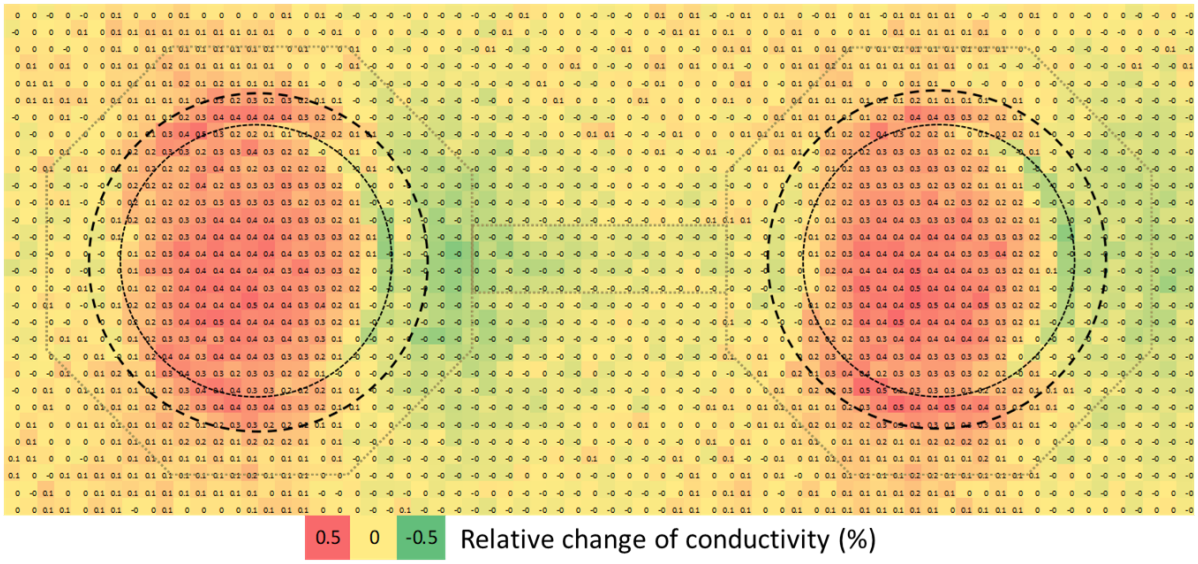


(b) 0.5mm bend test at 85 °C.

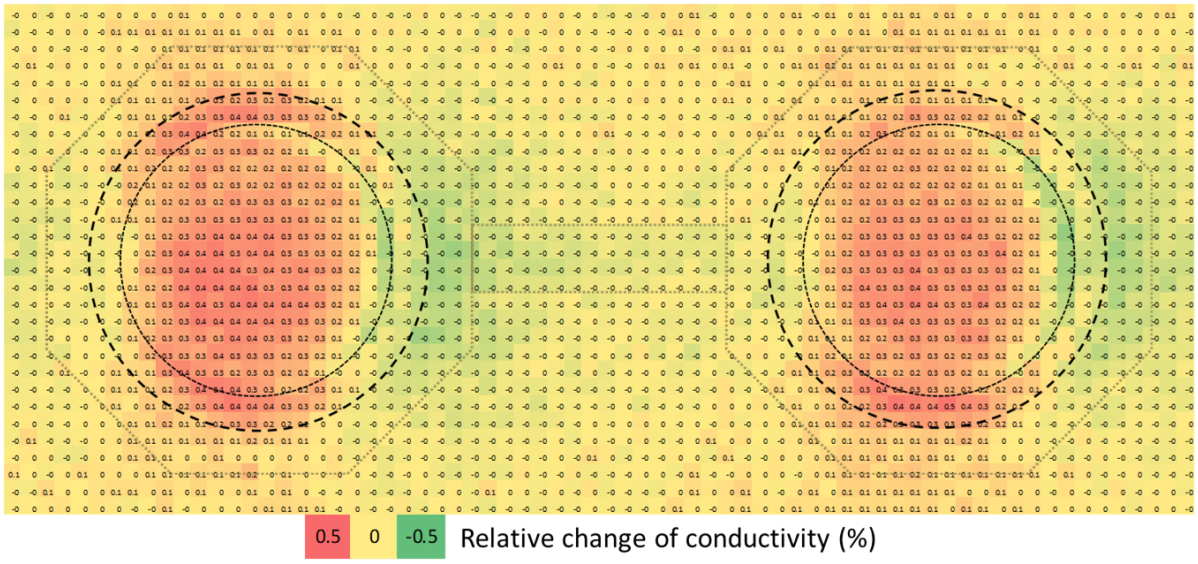


(c) 0.5mm bend test at 105 °C.

Figure A.3: The piezoresistive sensor measurement result at 0.5mm bend test.



(a) 1mm bend test at 125 °C.

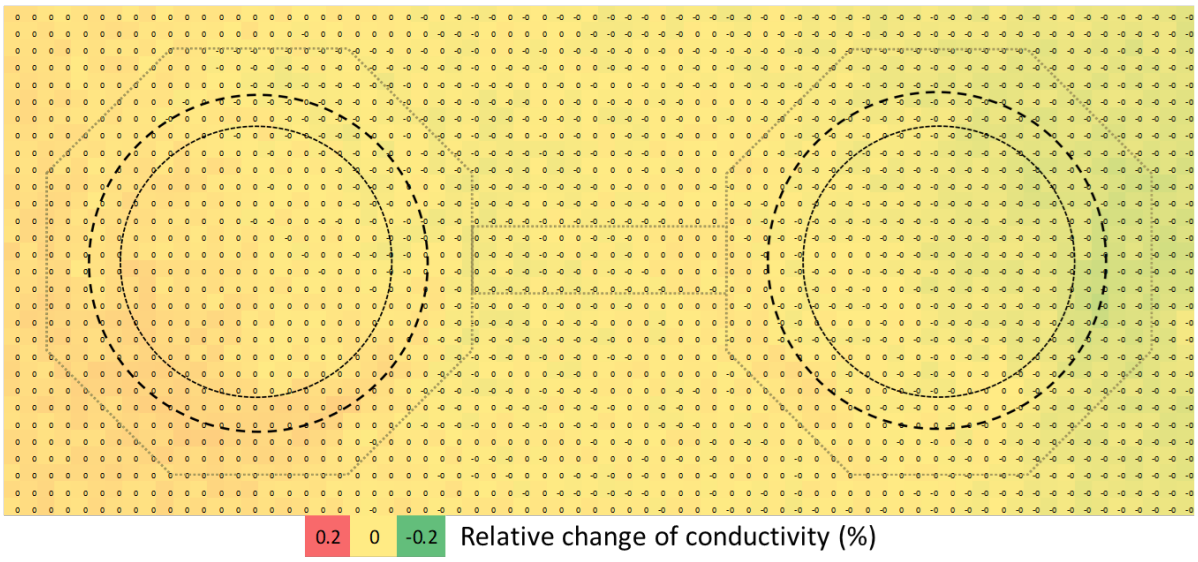


(b) Sum result of 1mm bend test at room temperature and 125 °C without bending.

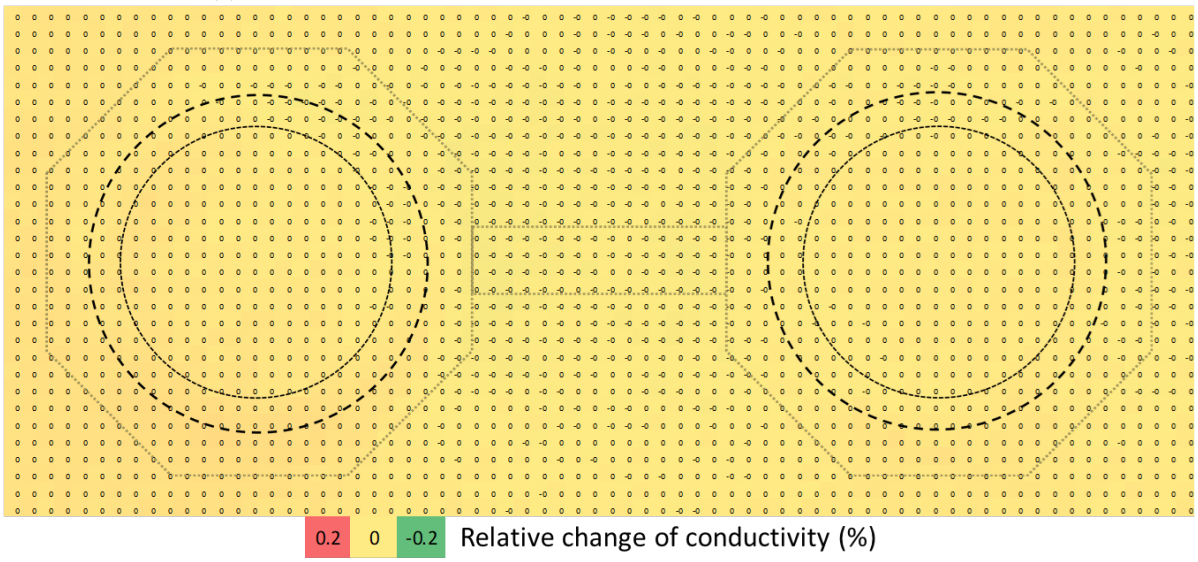
Figure A.4: The piezoresistive sensor measurement result: extra influence on thermo-mechanical coupled reliability test.

B

Appendix B: Piezoresistive Sensor Pattern Change During TC

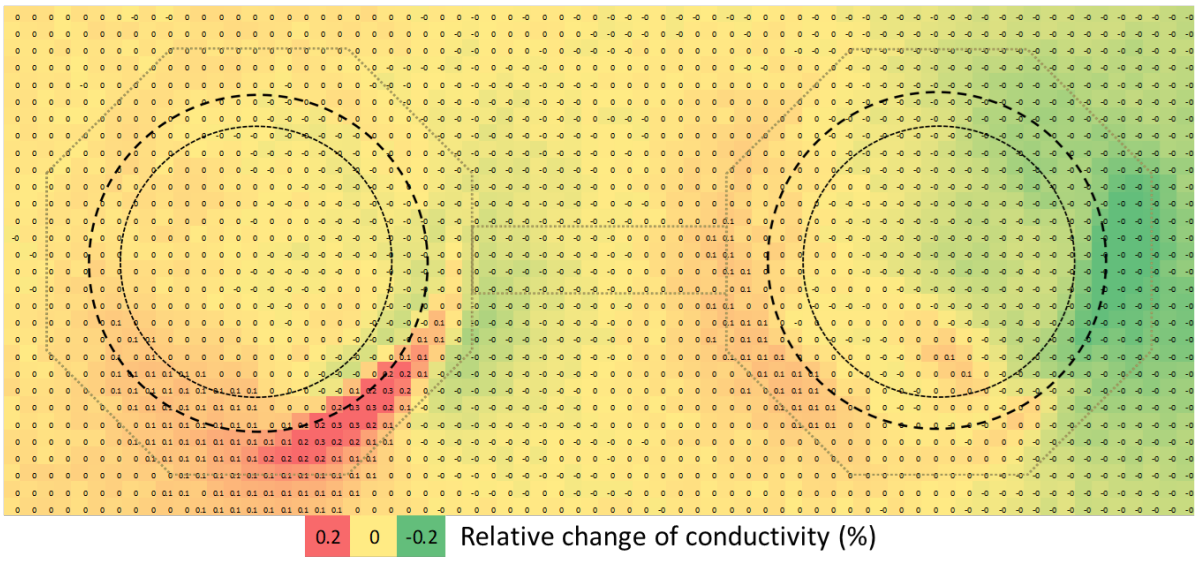


(a) Low-temperature shift of pattern compare to initial low-temperature state.

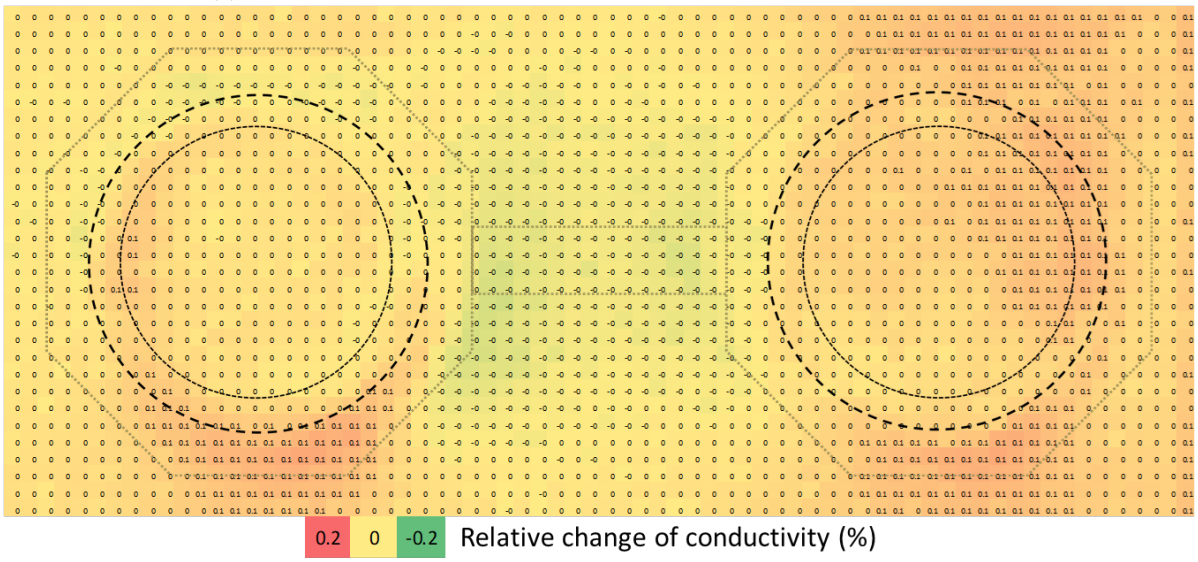


(b) High-temperature shift of pattern compare to initial high-temperature state.

Figure B.1: The piezoresistive sensor measurement result at the initial of in temperature cycle.

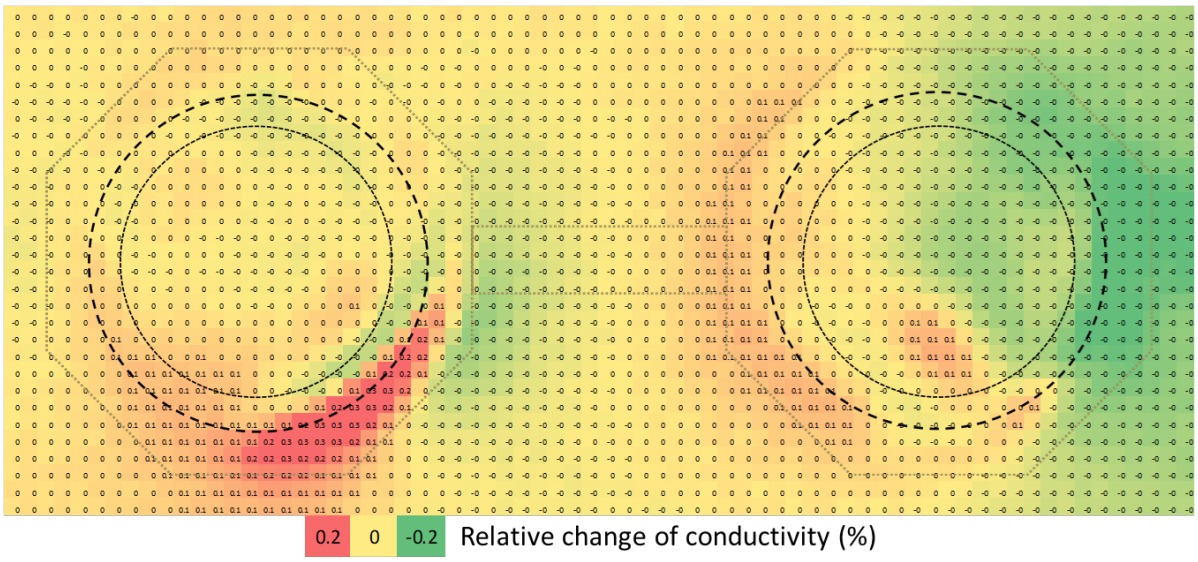


(a) Low-temperature shift of pattern compare to initial low-temperature state.

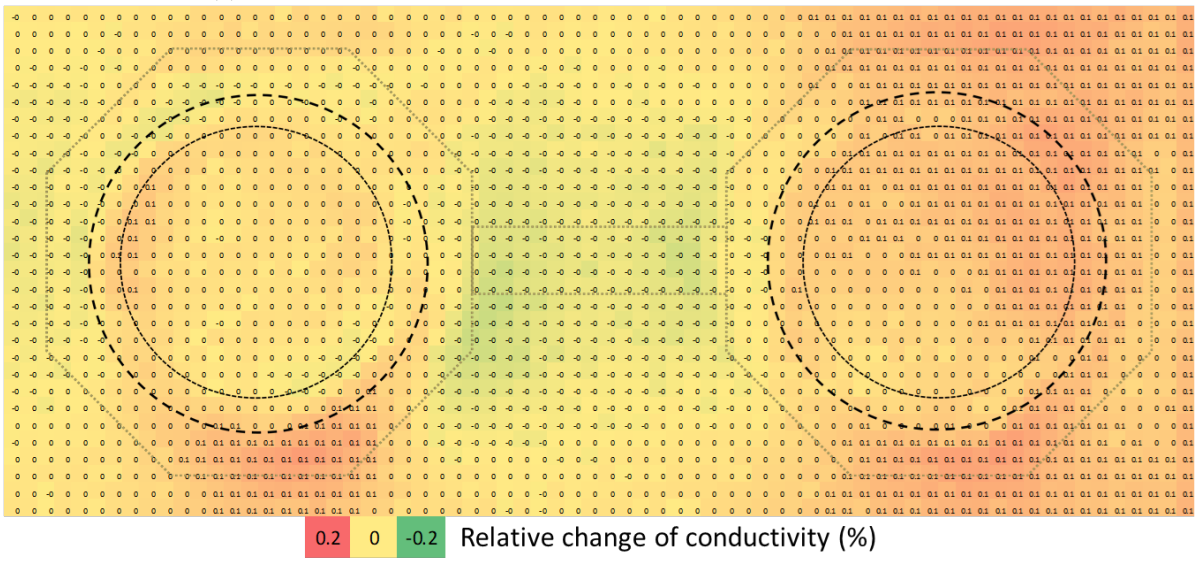


(b) High-temperature shift of pattern compare to initial high-temperature state.

Figure B.2: The piezoresistive sensor measurement result at around cycle 50 in the temperature cycle.

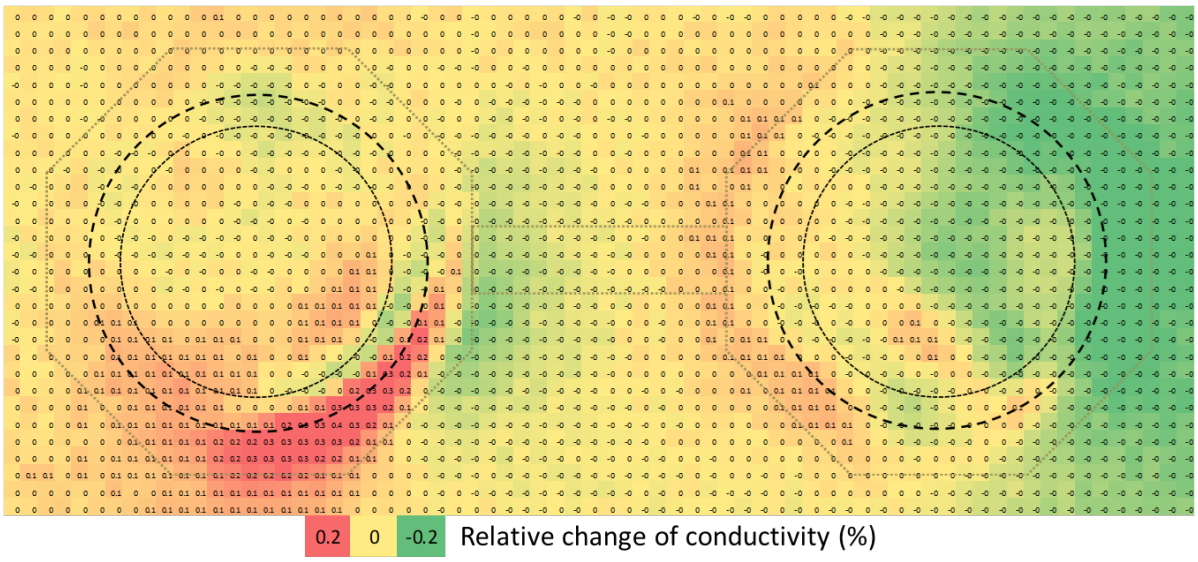


(a) Low-temperature shift of pattern compare to initial low-temperature state.

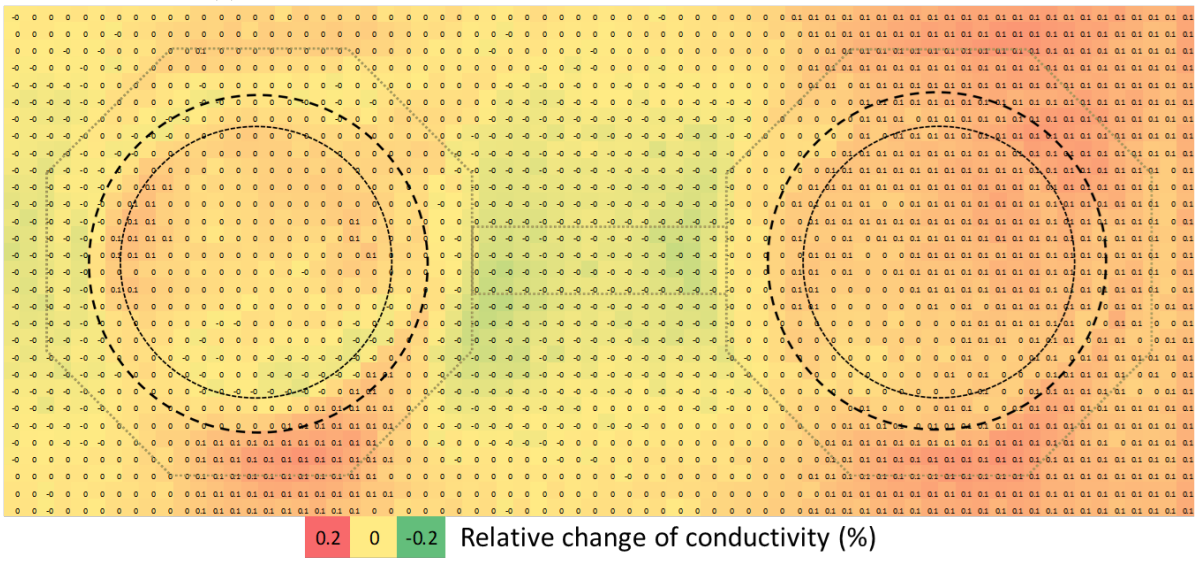


(b) High-temperature shift of pattern compare to initial high-temperature state.

Figure B.3: The piezoresistive sensor measurement result at around cycle 100 in the temperature cycle.

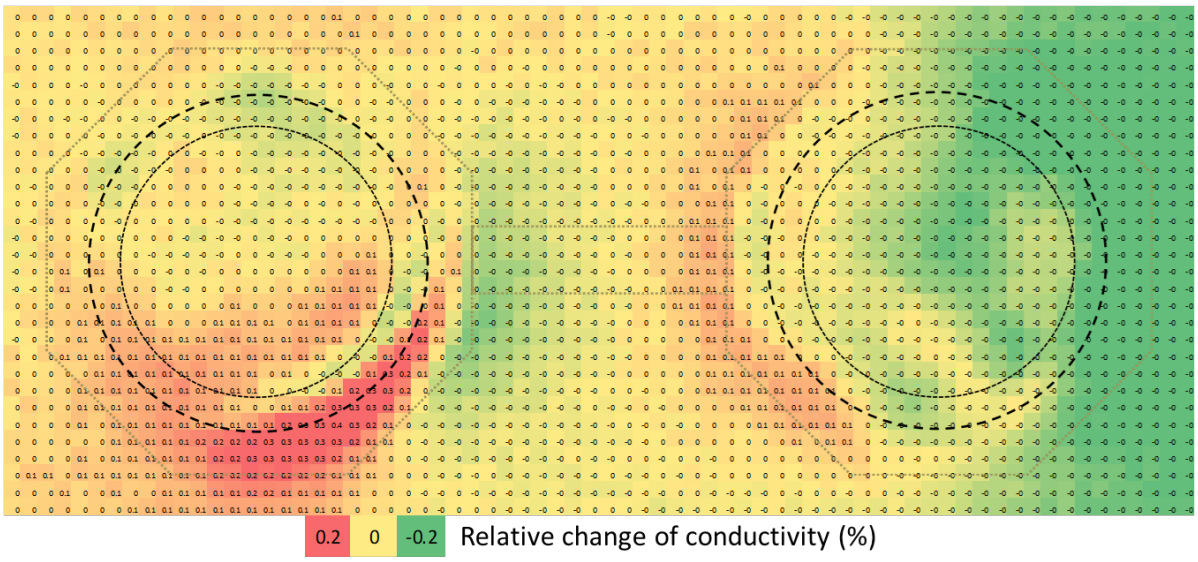


(a) Low-temperature shift of pattern compare to initial low-temperature state.

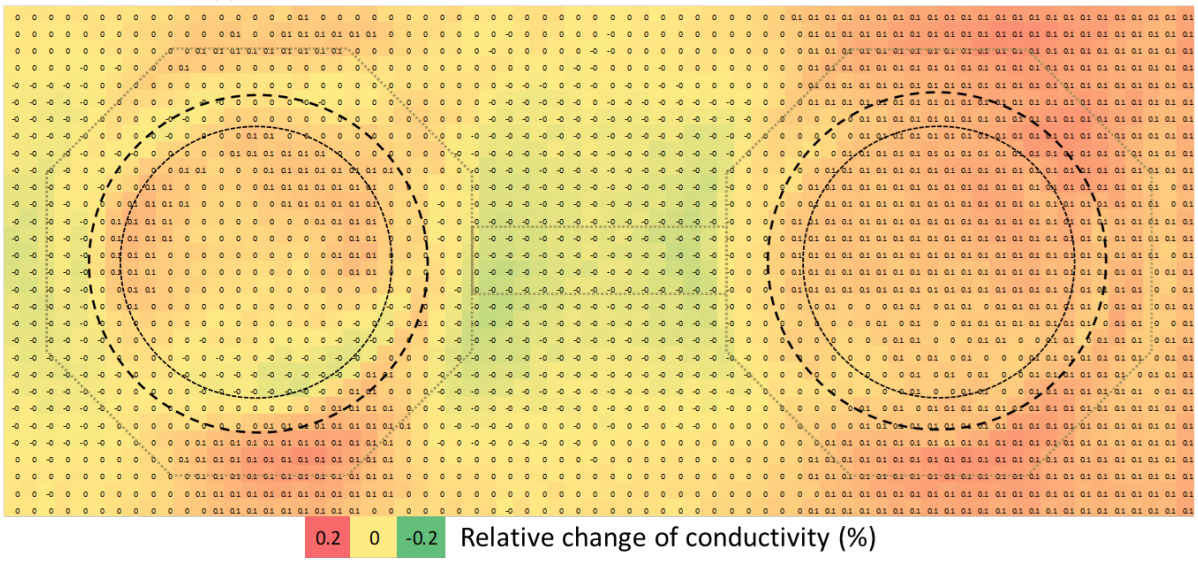


(b) High-temperature shift of pattern compare to initial high-temperature state.

Figure B.4: The piezoresistive sensor measurement result at around cycle 200 in the temperature cycle.

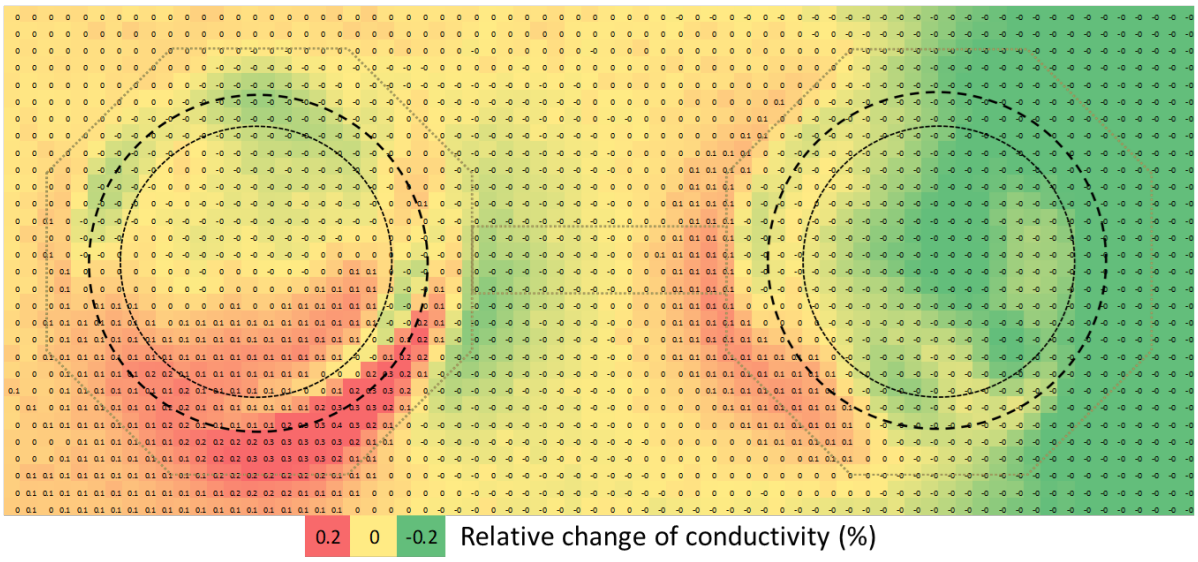


(a) Low-temperature shift of pattern compare to initial low-temperature state.

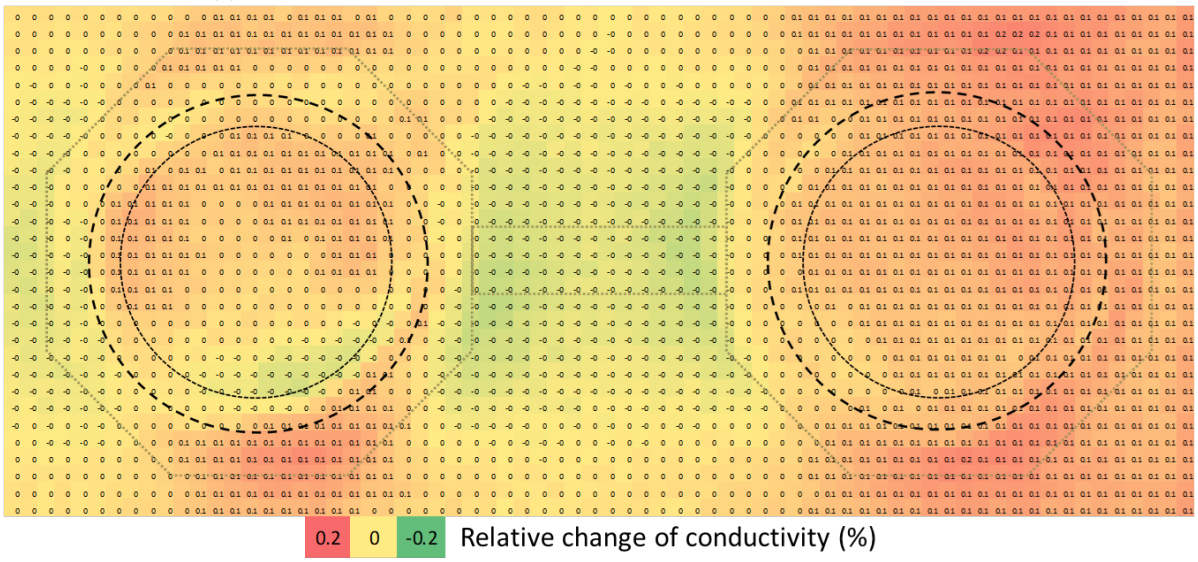


(b) High-temperature shift of pattern compare to initial high-temperature state.

Figure B.5: The piezoresistive sensor measurement result at around cycle 300 in the temperature cycle.

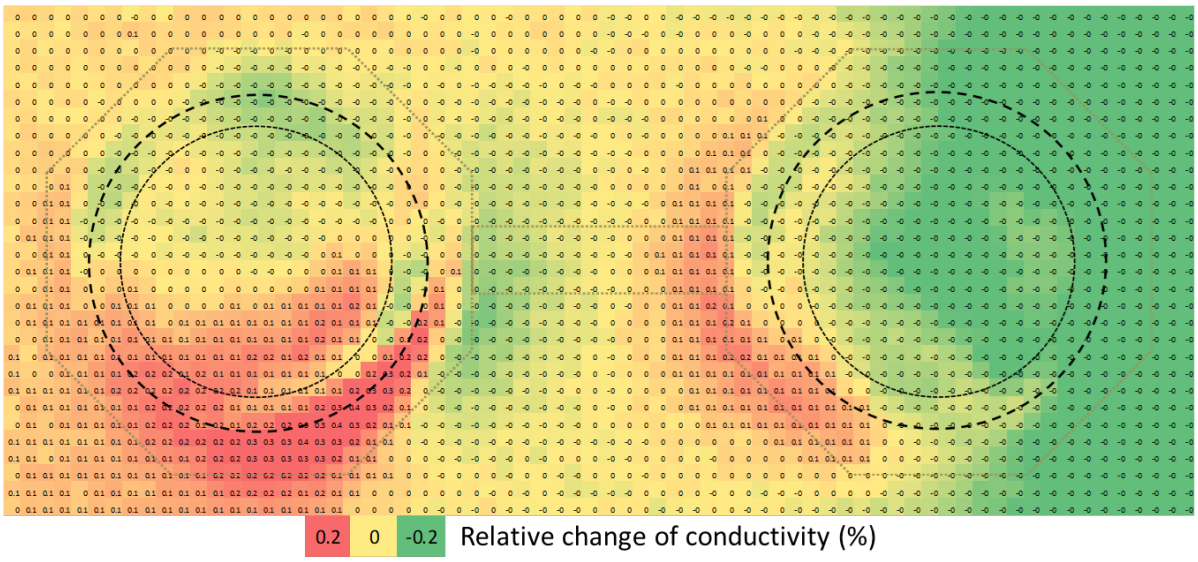


(a) Low-temperature shift of pattern compare to initial low-temperature state.

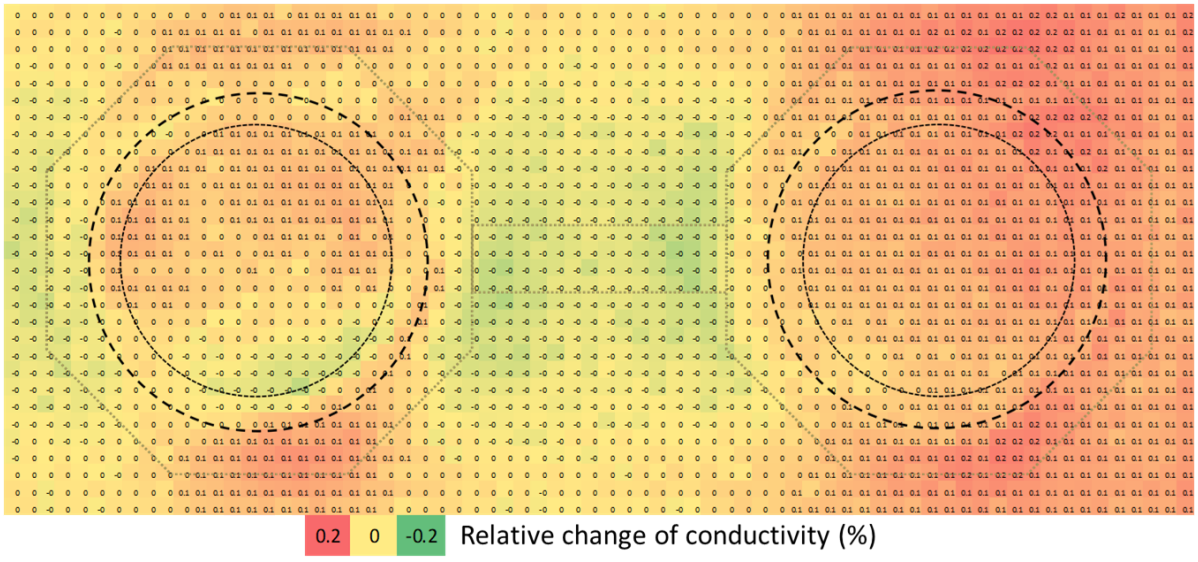


(b) High-temperature shift of pattern compare to initial high-temperature state.

Figure B.6: The piezoresistive sensor measurement result at around cycle 400 in the temperature cycle.

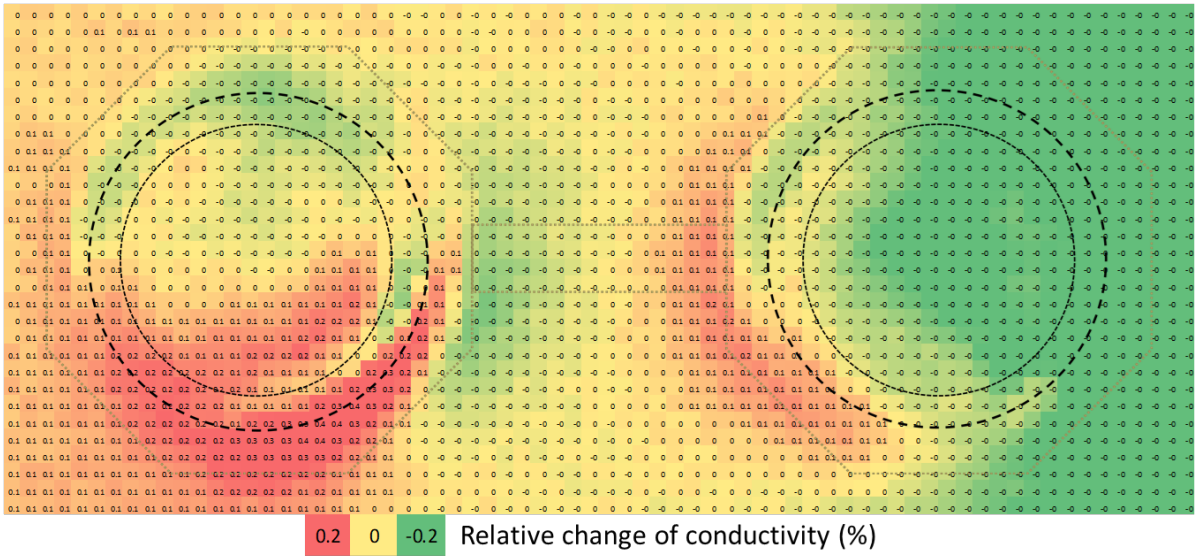


(a) Low-temperature shift of pattern compare to initial low-temperature state.

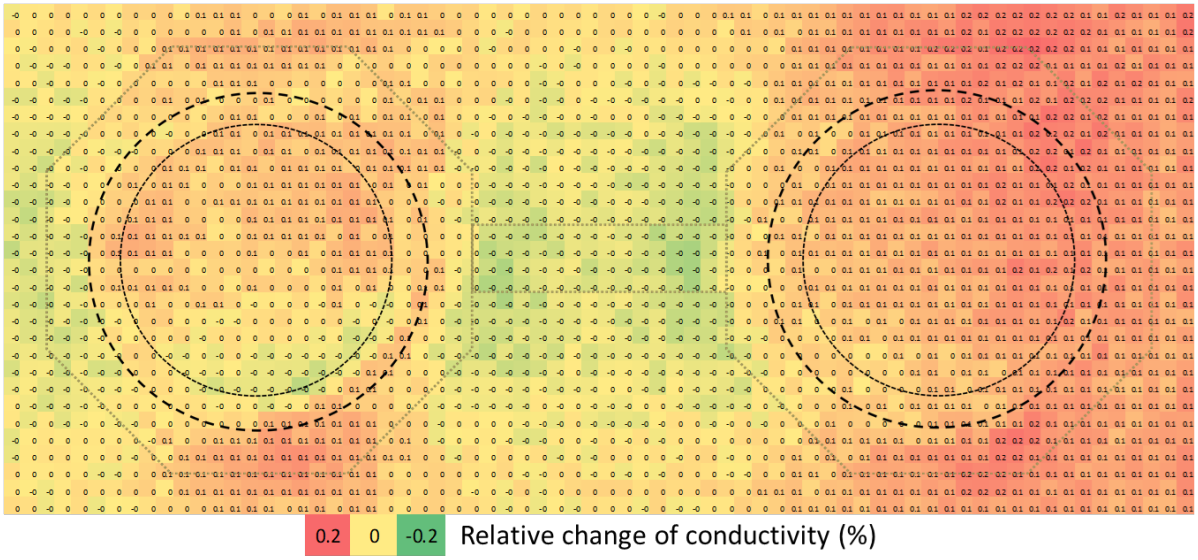


(b) High-temperature shift of pattern compare to initial high-temperature state.

Figure B.7: The piezoresistive sensor measurement result at around cycle 500 in the temperature cycle.



(a) Low-temperature shift of pattern compare to initial low-temperature state.



(b) High-temperature shift of pattern compare to initial high-temperature state.

Figure B.8: The piezoresistive sensor measurement result at around cycle 600 (last cycle before failure) in the temperature cycle.