An Active Power Decoupling Strategy to Reduce the Capacitor Size of a Cascaded H-Bridge Converter in a Solid State Transformer

Yadav, Sachin; Qin, Zian; Bauer, Pavol

DOI
10.1109/PEDG61800.2024.10667459

Publication date
2024

Document Version
Final published version

Published in
Proceedings of the 2024 IEEE 15th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)

2024 IEEE 15th International Symposium on Power Electronics for Distributed Generation Systems (PEDG) | 979-8-3503-6100-1/24/$31.00 ©2024 IEEE | DOI: 10.1109/PEDG61800.2024.10667459

An Active Power Decoupling Strategy to Reduce the Capacitor Size of a Cascaded H-Bridge Converter in a Solid State Transformer

1st Sachin Yadav
DCE&S, ESE
Delft University of Technology
Delft, The Netherlands
S.Yadav-1@tudelft.nl

2rd Zian Qin
DCE&S, ESE
Delft University of Technology
Delft, The Netherlands
Z.Qin-2@tudelft.nl

3th Pavol Bauer
DCE&S, ESE
Delft University of Technology
Delft, The Netherlands
P.Bauer@tudelft.nl

***Index Terms*—Solid-state transformer, System modeling, Active front-end, Cascaded H-Bridge, Dual Active Bridge (DAB), Active power-decoupling circuit**

***Abstract*—This paper presents a control strategy for active power decoupling in a Solid State Transformer (SST) using a cascaded H-bridge (CHB) converter, dual active bridge (DAB) converters, and a high-frequency link (HFL). The strategy balances capacitor voltage and decouples power flow, significantly reducing second harmonic voltage ripple in DC link capacitors and potentially reducing their size.**

I. Introduction

The recent rise in renewables has made it essential to make the distribution grid more robust and flexible. A normal transformer is just not enough for this purpose. Solid State Transformers provide the way forward to mitigate the challenges for a future distribution system by providing additional functionalities like reactive power support and integration of battery energy storage systems (BESS) [1]. Until now, several prototypes of SST have been produced for the distribution grids [2], [3].

This paper introduces a control scheme for an SST with a CHB converter to step down high voltage and maintain DC output voltage. It addresses issues with traditional control methods, where uneven DAB parameters lead to varying submodule voltages. This work also reviews existing literature on active power decoupling methods in SSTs, highlighting their role in reducing capacitor size, a significant component of the converter volume [4]–[6]. Unlike previous studies that use multilevel modular converters as active front-end (AFE) converters, this paper utilizes a CHB converter. This is because an SST application does not require a large common DC link voltage. The research discusses the limitations of conventional decoupled SST control and proposes an alternative power control algorithm to reduce the size of DC link capacitors between CHB and HFL modules.

The structure of the paper is as follows. Section II provides the description of the SST converter model. Section III discusses two control strategies of the SST along with the various potential drawbacks. Section IV provides the simulation results of the proposed control. Finally, section V concludes the paper.

II. Converter Model

The model of an SST is based on the topology illustrated in Fig. 1, utilizing a CHB converter as the AFE to interface with the grid and DAB converters as the HFL for isolation between the MV and LV sides. The SST's more cost-effective Star connection is highlighted.

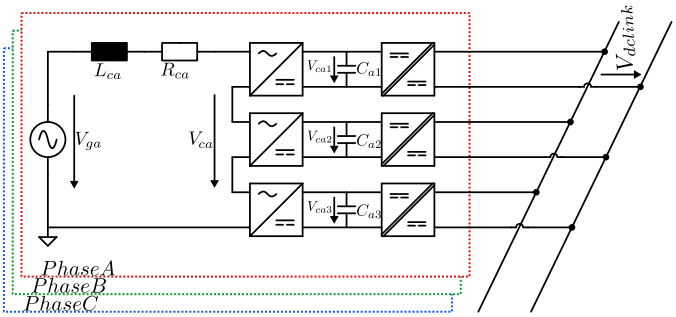

Fig. 1. Schematic of the SST converter upto the LVDC bus.

Focusing on phase A, as shown in Fig. 1, the grid voltage is 11 kV, with three submodules per phase connected through converter filter inductance (L_{cx}, R_{cx}). The DC link capacitors (C_{x1}, C_{x2}, C_{x3}) are situated between the CHB submodules and HFL modules. Details of the topology of the CHB and HFL modules are depicted in Fig. 2, with CHB submodules comprising full-bridge SiC MOSFETs ($S_{chbxy1} - S_{chbxy4}$) and HFL modules consisting of DAB converters with primary ($S_{dabpxy1} - S_{dabpxy4}$) and secondary ($S_{dabsxy1} - S_{dabsxy4}$) switches.

III. Control Strategy

This section presents the mathematical model of the CHB converter, as depicted in the schematic in Fig. 1. The model is based on several assumptions:

- all passive components in the converter phases and the grid are symmetrical,

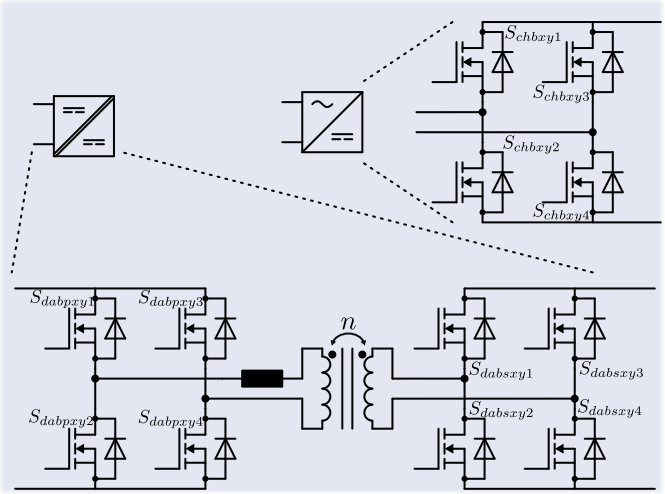

Fig. 2. Topologies of the submodules and high-frequency links.

- the switches are ideal, meaning they have no resistance or losses,
- the voltage across the capacitors is stable and equal across all H-Bridges in all phases, implying that the total voltage in all phase arms is equal, although, in reality, there's always a ripple component in the capacitor voltages which is double the line frequency (2ω), and
- The grid is strong enough that the current injection from the converter doesn't affect the source voltage behind the grid's inductance and resistance.

The whole converter can be treated as a two-level grid-connected converter using these assumptions. The grid currents and voltages are measured from the point of common coupling (PCC), similar to a two-level converter. However, a two-level converter has a single capacitor. Therefore, the control algorithm uses a lumped capacitor voltage to apply the control principles of a two-level converter in a CHB converter. The lumped DC link capacitor voltage is given by [7]

$$V_{dc} = \frac{V_{ca1} + .. + V_{can} + V_{cb1} + ... + V_{ccn}}{\mathrm{n_{bridge}}} \tag{1}$$

where V_{dc} is the lumped capacitor voltage, V_{cxy} is the voltage across capacitor number y in phase x, and $\mathrm{n_{bridge}}$ is the total number of bridges in all the phases of the converter.

A. Control strategy - 1

Several methods exist for implementing current and voltage control in converters, as detailed in various studies [8]–[13]. The main components of the controller include a phase-locked loop (PLL), capacitor voltage controller, current controller, and capacitor voltage balancing controller. The control strategy for the converter is categorized into three main areas, each with its subcategories.

The first category, Lower Level Control, is focused on active and reactive power control, which can alter frequency and voltage. This level adopts a cascaded control method, where the current control algorithm typically has a higher bandwidth than the DC capacitor voltage control algorithm. The bandwidth disparity allows for a cascaded control approach, with the current controller as the inner loop and the DC capacitor voltage controller as the outer loop [14]. This level encompasses two main aspects: Current Control and DC Capacitor Voltage Control, which are elaborated in subsequent sections.

Upper-level control, the second category, balances the capacitor voltages in each phase and each submodule (SM). It includes two approaches: Cluster Control, which manages groups of components, and Individual Control, focusing on single elements.

Lastly, the HFL Control category is dedicated to controlling the Dual Active Bridge (DAB) converters' output voltages, ensuring efficient and stable operation of the overall system.

1) Current control: Kirchhoff's voltage law (KVL) is applied between the PCC and the neutral point of the converter to determine the current flowing through the filter in all three phases. This current also flows through the filter inductor, and its relationship with the voltage across the inductor is expressed as $v_{gx} - v_{cx} = L_c \frac{d}{dt} i_x + R_c i_x$, where v_{gx} is the grid voltage, v_{cx} is the voltage after the filter, and i_x is the phase current.

To simplify, the system is reduced from three to two equations using Clarke's Transformation, which converts the system to the $\alpha\beta$ domain [15]. These $\alpha\beta$ quantities, which are sinusoidal, can be transformed into DC quantities using Park's transform. This converts the stationary frame of reference to a rotating one, resulting in the final equation:

$$\begin{bmatrix} v_{gd} - v_{cd} \\ v_{gq} - v_{cq} \end{bmatrix} = \begin{bmatrix} L_c \frac{d}{dt} + R_c & -\omega L_c \\ \omega L_c & L_c \frac{d}{dt} + R_c \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{2}$$

This equation represents the plant model for the converter's current, depicted in Fig. 3. The reference values are indicated by a $*$ symbol. The model shows that the current controller's direct and quadrature axis terms are coupled, necessitating a PI controller designed for decoupling, which is crucial for independent control of active and reactive power. Decoupling is achieved by feed-forwarding the coupled terms and the grid voltage, which improves disturbance rejection. Thus, the final current controller for the plant is illustrated in Fig. 4, with K_p and K_i representing the proportional and integral coefficients, respectively.

2) DC Link Voltage Control: The dynamics added by DC capacitors in the converter are crucial for voltage control at the PCC. For simplicity, all DC capacitors are modeled as single lumped capacitors, as shown in Fig. 5, where the state of the system is defined by the voltage across this capacitor. The power conservation at the node is given by:

$$p = p_c + p_{dc} \tag{3}$$

The power invariant form for powers in the rotating reference frame is expressed as:

$$\frac{3 v_d i_d}{2} = v_{dc} i_c + v_{dc} i_{dc} \tag{4}$$

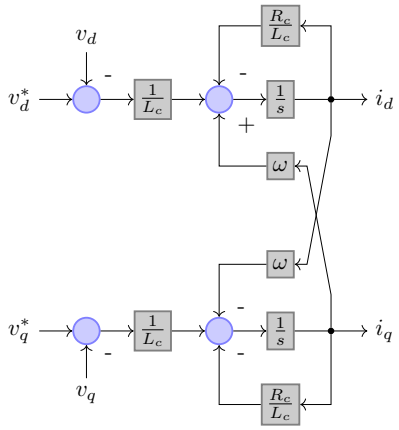

Fig. 3. Converter current plant diagram for the CHB in dq0 coordinates.

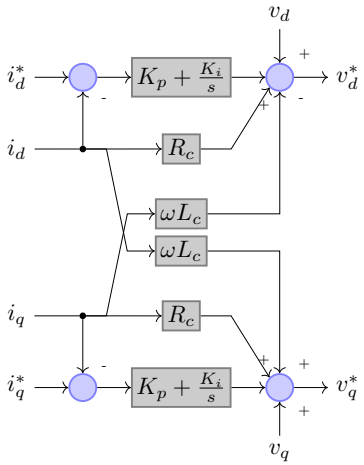

Fig. 4. Current controller in dq0 coordinates.

Rearranging this equation gives the current through the capacitor:

$$i_c = \left(\frac{3v_d i_d}{2v_{dc}} - i_{dc}\right) \tag{5}$$

The relationship between capacitor current and voltage is:

$$i_c = C_{dc}\frac{dv_{dc}}{dt} \tag{6}$$

Combining these equations leads to a non-linear plant model for DC capacitor voltage control, which is linearized using

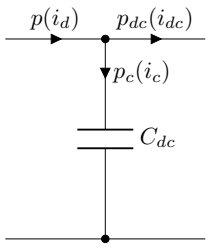

Fig. 5. Current and Power flowing through the DC Capacitor of the converter.

Taylor's expansion at an equilibrium point, denoted by $v_{dc,ref}$:

$$C_{dc}\frac{d\Delta v_{dc}}{dt} = \frac{3v_d}{2v_{dc}^*}\Delta i_d + \frac{3i_d}{2v_{dc}^*}\Delta v_d - \frac{3v_d i_d}{2(v_{dc}^*)^2}\Delta v_{dc} - \Delta i_{dc} \tag{7}$$

Simplifying further, the linearized form for the DC capacitor voltage control plant becomes:

$$C_{dc}\frac{d\Delta v_{dc}}{dt} = \frac{3v_d}{2v_{dc}^*}\Delta i_d \tag{8}$$

Taking the Laplace transform leads to the transfer function for DC capacitor voltage control:

$$\frac{\Delta V_{dc}(s)}{\Delta i_d(s)} = \frac{3v_d}{2V_{dc}^*}\frac{1}{sC_{dc}} \tag{9}$$

A PI controller is then used to control the voltage across the capacitor, as depicted in Fig. 6, where $K_{p,dc}$ and $K_{i,dc}$ are the proportional and integral coefficients of the current controller, and $T_{cc,eq}$ is the equivalent time constant for the DC link capacitors.

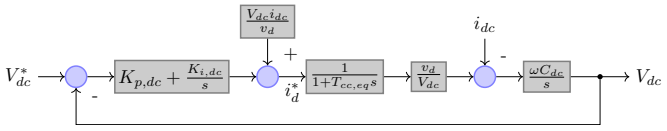

Fig. 6. Control model for the DC Capacitor Voltage Control.

3) Cluster voltage balancing control: In cluster control, to counteract the rise in capacitor voltage proportional to the active power increase, the current is reduced by shortening the activation time of H-Bridge switches. The control algorithm, depicted in Fig. 7, calculates the necessary zero-sequence voltage for the PWM signal by subtracting the average voltage of all capacitors from the phase arm voltages average, then multiplying this difference with current vectors. The coefficient $K_{p,ph}$ determines the magnitude of this voltage, crucial for maintaining voltage balance, especially in unbalanced grid conditions, although it may increase second harmonic distortion in the converter's power. The algorithm thus finely tunes the control process by using the unit current vector $\hat{i}_x$ and proportional coefficient $K_{p,ph}$.

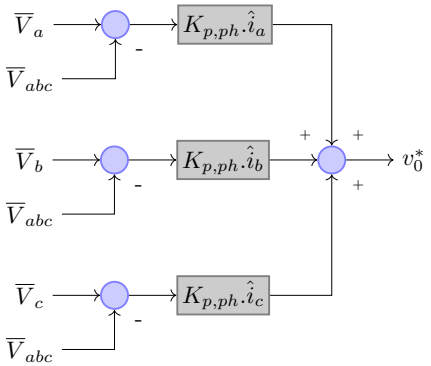

Fig. 7. Algorithm for cluster control.

4) Individual voltage balancing control: This algorithm balances capacitor voltages in a phase leg by adjusting power flow based on the capacitor's charge state. If a capacitor's voltage falls below the reference, the controller increases power to charge it, and vice versa for discharging. The process involves modifying the modulation signal with phase current unit vectors.

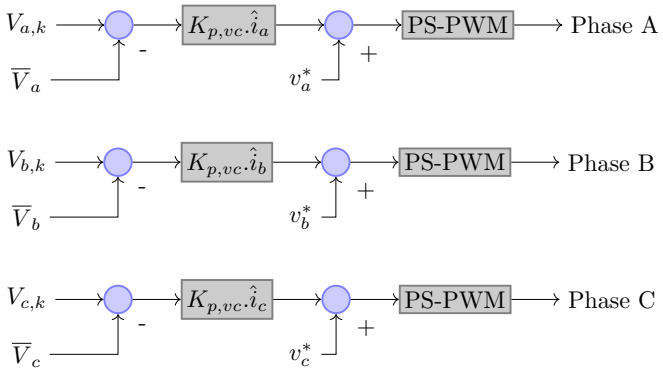

Fig. 8. Algorithm for individual control.

Illustrated in 8, individual capacitor voltage control is achieved by adjusting each capacitor's voltage against the phase leg's average voltage ($\overline{V}_x$), using the phase current unit vector ($\hat{i}_x$). A proportional controller ($K_{p,vc}$) simplifies calculations, although a PI controller could alternatively be used.

B. Control strategy - 2

In this control scheme, the power flowing at the LVDC bus produces the direct current set-point to the CHB rectifier. Hence, DC link voltage (V_{dclink}) is used to generate the active power setpoint for power control. This differs from the original control strategy in that the SM capacitor voltage (V_{cxy}) was used to control the active power flow through the converter. Furthermore, in control strategy 2, the SM capacitor voltages are controlled by the individual HFLs. In the following sections, the main focus is on the balancing strategy of the CHB capacitors, and the voltage and current control of the CHB rectifier are omitted.

To develop a control system, the model of the HFL must be developed. The average model of the DAB around an operating point D is given by [16].

$$\frac{v(s)}{d(s)} = \frac{V_i}{2L_{dabxy}f_{sdab}}(1-2D)Z(s) \tag{10}$$

where $v(s)$ is the voltage variable of the controlled side, $d(s)$ is the laplacian of the duty ratio between the HV and LV side of the DAB, V_i is the fixed or uncontrolled voltage, L_{dabxy} is the leakage inductance of transformer of DAB connected to SM y of phase x, f_{sdab} is the DAB switching frequency, D is the duty ratio at the operating point and $Z(s)$ is the characteristic impedance of the controlled side.

Equation (10) can be expanded as

$$\frac{v(s)}{d(s)} = \frac{V_i}{2L_{dabxy}f_{sdab}}(1-2D)\left(\frac{1}{sC_{dabxy}} + R_{dabxy}\right). \tag{11}$$

where C_{dabxy} and R_{dabxy} are the capacitance and resistance, respectively, at the DAB output. Considering the resistance term as disturbance, the linearized plant can be written as:

$$\frac{v(s)}{d(s)} = \frac{V_i}{2L_{dabxy}f_{sdab}}(1-2D)\frac{1}{sC_{dabxy}} \tag{12}$$

The plant in (12) can be compensated with a PI-R controller as it provides infinite gain at DC and a chosen frequency ω_c. The transfer function for the PI-R controller is given by

$$G_{pir}(s) = K_{p,pir} + \frac{K_{i,pir}}{s} + \frac{K_{r,pir}s}{s^2+\omega_c^2} \tag{13}$$

where, $K_{p,pir}$ is the proportional gain, $K_{i,pir}$ is the integral gain, and $K_{r,pir}$ is the resonant gain of the PIR controller.

TABLE I
PARAMETERS FOR DAB INPUT VOLTAGE CONTROLLER.

Parameter	Value
Capacitance	4100 µF
$K_{p,pir}$	0.4
$K_{i,pir}$	0.0004
$K_{r,pir}$	80

The bode plot for the PIR controller with values given in table I is shown in Fig. 9.

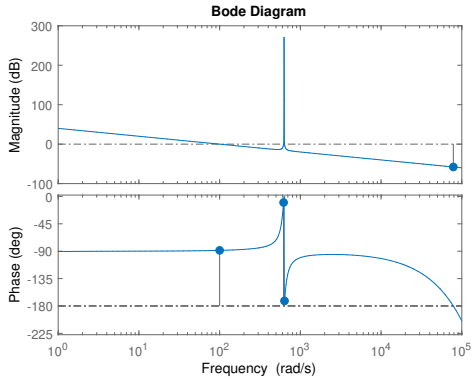

Fig. 9. Bode plot for the open loop transfer function for DAB input voltage control. The plot shows that the system is stable.

IV. RESULTS

In this section, we present simulation results of a CHB and DAB model created in MATLAB Simulink, with each phase containing three submodules for enhanced simulation speed. The switch models were used The converter and grid parameters are detailed in table II.

The control algorithm, implemented in MATLAB, demonstrates the efficacy of our approach. Initially, we applied a balancing control algorithm via the CHB, involving zero

TABLE II
PARAMETERS OF THE GRID AND CONVERTER MODEL

Parameter	Value
Grid RMS voltage	11 kV
Rated power	1000 kV A
L_{cx}	57.8 mH
R_{cx}	2.33 Ω
Number of Submodules	5

sequence component injection for individual capacitor balancing while modeling DABs as current sources. Conventional control results, shown in Fig. 10, reveal significant voltage deviations due to varying HF transformer ratios in the DABs. Our proposed method overcomes this by controlling LVDC voltage through the LV side converter and using DABs for phase-wise capacitor voltage balancing, visible in the second subplot of Fig. 10.

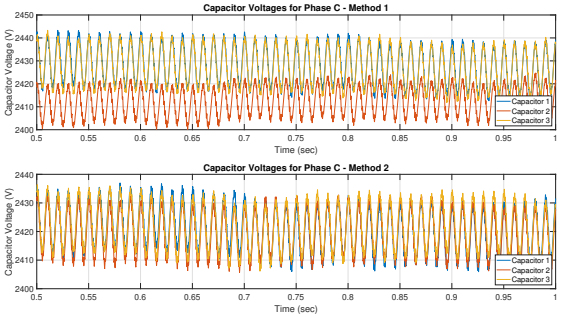

Fig. 10. Comparison of capacitor voltages with conventional control method and proposed method. The difference is due to different load current flows at the DC side.

Additionally, our control strategy enables active power decoupling, reducing the capacitor size needed for the CHB converter. The PI-R controller effectively tracks capacitor voltage, allowing DAB current adjustments to minimize voltage ripple. Simulation results, depicted in Fig. 11, confirm the reduction in capacitor size. The FFT plots in the same figure show that using a 2100 µF capacitor results in a 15 V second harmonic ripple, while a 410 µF capacitor maintains a similar total ripple, albeit with an additional 1000 Hz ripples due to the CHB converter's 500 Hz switching frequency. Thus, our method maintains total ripple levels even with reduced capacitance.

V. CONCLUSION

In conclusion, this paper presents a significant advancement in control strategies for a solid-state transformer's AFE and HFL components. We have thoroughly analyzed the limitations of traditional control methods and introduced a control strategy that effectively addresses these shortcomings. Our proposed approach demonstrates superior performance in balancing submodule capacitor voltages, a critical aspect of efficient transformer operation. Moreover, it introduces an innovative mechanism for active power decoupling from the submodules

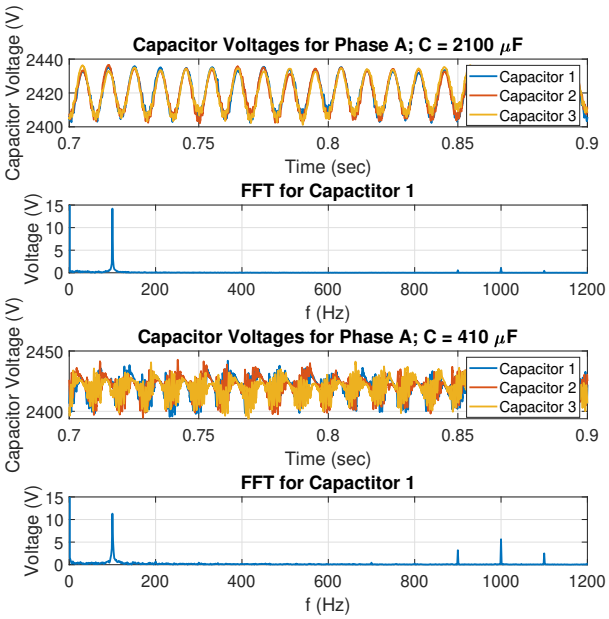

Fig. 11. A comparison of the capacitor voltage ripple using the proposed control method. The corresponding FFT is also shown.

to the LVDC link. This breakthrough enhances the overall system efficiency and paves the way for a substantial reduction in capacitor size. This reduction is not just a marginal improvement but a transformative step in solid-state transformer design, leading to more compact, cost-effective, and reliable systems. The potential impact of these advancements on the field of power electronics and transformer technology is profound, offering a pathway to more sustainable and efficient power distribution solutions.

REFERENCES

[1] Xu She, A. Q. Huang, and R. Burgos, "Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, pp. 186–198, Sept. 2013.

[2] J. E. Huber and J. W. Kolar, "Solid-State Transformers: On the Origins and Evolution of Key Concepts," *IEEE Industrial Electronics Magazine*, vol. 10, pp. 19–28, Sept. 2016.

[3] Y. Jiang, "Modeling of Solid State Transformer for the FREEDM System Demonstration," p. 71.

[4] Z. Kong, X. Huang, Z. Wang, J. Xiong, and K. Zhang, "Active Power Decoupling for Submodules of a Modular Multilevel Converter," *IEEE Transactions on Power Electronics*, vol. 33, pp. 125–136, Jan. 2018.

[5] Y. Liu, W. Zhang, Y. Sun, M. Su, G. Xu, and H. Dan, "Review and Comparison of Control Strategies in Active Power Decoupling," *IEEE Transactions on Power Electronics*, vol. 36, pp. 14436–14455, Dec. 2021.

[6] Z. Bu, J. Teng, X. Sun, Y. Pan, and Y. Pan, "Low-Frequency Voltage Ripples Decoupling With Switched-Capacitor Conversion for an MMC-Based SST," *IEEE Transactions on Industrial Electronics*, vol. 69, pp. 11293–11303, Nov. 2022.

[7] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade pwm statcom with star configuration," *IEEE Transactions on Industry Applications*, vol. 43, no. 4, pp. 1041–1049, 2007.

[8] M. Angulo, P. Lezana, S. Kouro, J. Rodriguez, and B. Wu, "Level-shifted PWM for Cascaded Multilevel Inverters with Even Power Distribution," in *2007 IEEE Power Electronics Specialists Conference*, pp. 2373–2378, June 2007.
[9] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A Survey on Cascaded Multilevel Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2197–2206, July 2010.
[10] H. Akagi, "Multilevel Converters: Fundamental Circuits and Systems," *Proceedings of the IEEE*, vol. 105, pp. 2048–2065, Nov. 2017.
[11] Y. Yu, G. Konstantinou, C. D. Townsend, R. P. Aguilera, and V. G. Agelidis, "Delta-Connected Cascaded H-Bridge Multilevel Converters for Large-Scale Photovoltaic Grid Integration," *IEEE Transactions on Industrial Electronics*, vol. 64, pp. 8877–8886, Nov. 2017.
[12] H. Akagi, "A review of developments in the family of modular multilevel cascade converters," *IEEJ Transactions on Electrical and Electronic Engineering*, vol. 13, pp. 1222–1235, Sept. 2018.
[13] D. Yang, L. Yin, S. Xu, and N. Wu, "Power and Voltage Control for Single-Phase Cascaded H-Bridge Multilevel Converters under Unbalanced Loads," *Energies*, vol. 11, p. 2435, Sept. 2018.
[14] L. Wang, S. Chai, D. Yoo, L. Gan, and K. Ng, *PID and predictive control of electrical drives and power converters using MATLAB/Simulink*. John Wiley & Sons, 2015.
[15] W. Duesterhoeft, M. W. Schulz, and E. Clarke, "Determination of instantaneous currents and voltages by means of alpha, beta, and zero components," *Transactions of the American Institute of Electrical Engineers*, vol. 70, no. 2, pp. 1248–1255, 1951.
[16] H. K. Krishnamurthy and R. Ayyanar, "Building block converter module for universal (ac-dc, dc-ac, dc-dc) fully modular power conversion architecture," in *2007 IEEE Power Electronics Specialists Conference*, pp. 483–489, IEEE, 2007.