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***Abstract*—Estimation of the collapse (V_{col}) and snapback (V_{sb}) voltages of Capacitive Micromachined Ultrasonic Transducers (CMUTs) is usually performed by extracting C-V curves from low frequency impedance measurements at different bias points. However, impedance analysis in several bias conditions is time-consuming, making this technique unsuitable for wafer-level testing. Additionally, prolonged exposure to high electric fields may lead to charge injection and trapping phenomena in the CMUT in-cavity insulation layers. This paper proposes an adjustment to the conventional impedance analysis technique aimed at enhancing estimation accuracy and introduces a novel technique for fast C-V assessment enabling rapid wafer-level characterization. Results from both techniques are compared, demonstrating the validity of the proposed approaches.**

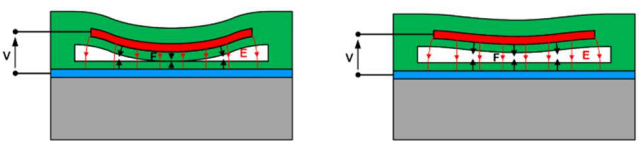
Keywords— Collapse, Snapback, CMUTs, C-V curves, electrical characterization, impedance measurement

I. Introduction

During the characterization of CMUTs, accurately estimating collapse (V_{col}) and snapback (V_{sb}) voltages is important for understanding the device behavior and setting the DC bias voltage for conventional mode or collapse mode [1] operation. When a DC bias voltage (V_{DC}) is applied across the CMUT electrodes, an electrostatic force is generated, pulling the free-moving plate toward the fixed backplate. This movement reduces the distance between the electrodes, leading to an increase in capacitance. As the bias voltage increases, the plate eventually collapses onto the substrate at $V_{DC} = V_{col}$, causing a sharp increase in capacitance. Conversely, when the bias voltage is gradually decreased, the electrostatic force weakens, and the plate detaches from the substrate at $V_{DC} = V_{sb}$ [2]. Fig. 1 schematically diagrams the collapsed and non-collapsed CMUT configuration.

Collapse and snapback voltage estimation is typically done by extracting capacitance-voltage (C-V) curves from low-frequency impedance measurements at various bias points. However, this technique has limitations. In order to have a high resolution on the assessment of V_{col} and V_{sb}, the CMUT electrical impedance should be measured by increasing V_{DC} in small steps when approaching collapse and snapback. Sweeping across multiple bias points may lead to very long measurement times, making this technique not suitable for wafer-level testing of all elements of CMUT arrays. Moreover, during the measurement, the CMUT may be exposed to high electric fields for long times. This prolonged exposure to high fields may induce charge injection and trapping [3] in the in-cavity insulation layers that affect the measured capacitance value, shifting the obtained C-V curve and thereby impairing the accuracy of V_{col} and V_{sb} estimation. Additionally, measuring the CMUT electrical impedance at low frequency, i.e. below resonance, implies driving the device where the displacement response to the applied voltage has non-negligible amplitude and is in phase with the excitation. This condition can cause the stimulus signal to induce premature collapse of the plate, reducing the measurement accuracy and resolution.

This paper proposes an improvement to the conventional technique for the evaluation of V_{col} and V_{sb} based on the C-V curve extraction from impedance analysis, aimed at addressing existing issues and increasing the reliability of the results. Furthermore, this paper introduces a novel fast C-V assessment method, based on dynamic excitation of the CMUT and real-time acquisition of the voltage across the device. In Section II, the proposed improvement for impedance analysis technique and the novel fast C-V assessment method are described in detail. In Section III, results from experiments performed with both techniques are compared. Section IV discusses the validity of the proposed approaches.



$V_{DC} > V_{col}$ (a) $V_{DC} < V_{sb}$ (b)

Fig. 1. Schematic diagram of a collapsed (a) and non-collapsed (b) CMUT

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II. Methodology

A. Improved impedance analysis technique

Electrical impedance analysis was used to obtain the C-V curves of individual elements of a 64-element CMUT array designed for low-frequency medical imaging applications. The CMUT array specifications and complete characterization and benchmarking against other traditional and MEMS-based ultrasonic transducer is available in [4], [5], and [6]. A bias voltage sweep across the ±70 V range was applied in steps of 1 V. To overcome the issues related to premature collapse induced by the stimulus signal, the measurement frequency was set to twice the maximum resonance frequency of the device. Specifically, the resonance frequency of the device at V_{DC} = 0 V is 850 kHz, but it reaches 2 MHz at V_{DC} = 70 V. Hence, the measurement frequency was set at f = 4 MHz. At this frequency, the amplitude of the displacement response to the voltage input is much smaller than it is below the resonance frequency, and in phase opposition with the electrostatic force, thereby mitigating the risk of premature collapse. This enables higher voltage resolution and ensures more accurate results with respect to conventional impedance analysis.

The frequency-dependent electrical impedance, Z_c, was acquired using a HP4194A (Hewlett-Packard Inc., Palo Alto, CA, USA) impedance analyzer at each bias point. The corresponding capacitance is then calculated as

$$C = \frac{1}{2\pi f\, \Im(Z_c)} \tag{1}$$

The capacitance values over the range of applied V_{DC} are then plotted to show the C-V curve. At collapse, the capacitance sharply increases due to the reduced distance between the electrodes; conversely, at snapback, the capacitance decreases abruptly. The resulting collapse and snapback voltages for the CMUT under test are V_{col} = 60 V and V_{sb} = 45 V, respectively.

Increasing the voltage step between bias points gives faster results, but impairs voltage resolution, compromising the accuracy of V_{col} and V_{sb} assessment. Achieving higher resolution requires impedance measurements at multiple bias points with small voltage increments, which significantly increases measurement time and raises the risk of charge trapping. A potential tradeoff between speed and accuracy consists of using a coarse voltage sweep in regions where collapse or snapback doesn't occur, and finer resolution near those critical regions. This approach ensures improved resolution while maintaining a relatively efficient measurement time.

Nevertheless, despite the proposed improvements, the time required to perform impedance measurements at different bias points to assess V_{col} and V_{sb} still makes impedance analysis impractical for wafer-level testing of CMUT arrays, and does not prevent charge trapping from affecting the measurement and stressing the devices.

B. Proposed fast C-V assessment method

To overcome the issues related to long measurement times, a novel fast C-V assessment method is introduced.

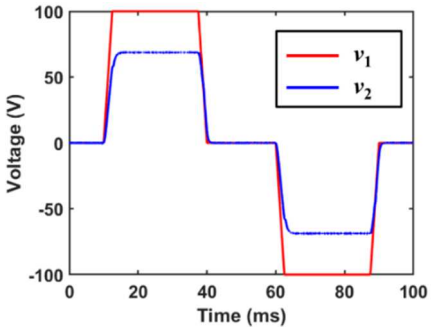

Fig. 2. Applied voltage signal $v_1(t)$ and voltage measured across the CMUT electrodes $v_2(t)$.

In the proposed method, a resistor is placed in series with the CMUT, R_s, and an arbitrary AC trapezoidal bipolar pulse, v_1, is generated and applied using a Keysight B2926A (Keysight Technologies, Santa Rosa, CA, USA) Source Measure Unit. The voltage measured across the CMUT element, v_2, is acquired using a R&S MXO44 (Rohde & Schwarz GmbH & Co., Munich, Germany) oscilloscope. Both applied and measured voltages are shown in Fig. 2. Using these voltages, the current flowing through the resistor is obtained by

$$i_s(t) = \frac{v_1(t) - v_2(t)}{R_s} \tag{2}$$

However, the impedance of the probe used to measure v_2 cannot be neglected, as it is comparable to the electrical input impedance of the CMUT array element. Thus, the equivalent circuit of the measurement setup, shown in Fig. 3, includes a parallel resistor, R_p, that represents the probe impedance.

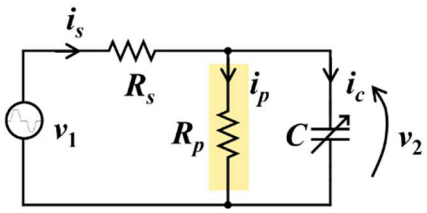

Fig. 3. Equivalent circuit representing the measurement setup. In the schematic, the probe resistance is highlighted in yellow.

Consequently, the current flowing through the probe, i_p, is

$$i_p(t) = \frac{v_2(t)}{R_p} \tag{3}$$

and the current in the CMUT, i_c, can be computed from

$$i_c(t) = i_s(t) - i_p(t) \tag{4}$$

The currents in the series resistor, the probe, and the CMUT, are reported in Fig. 4.

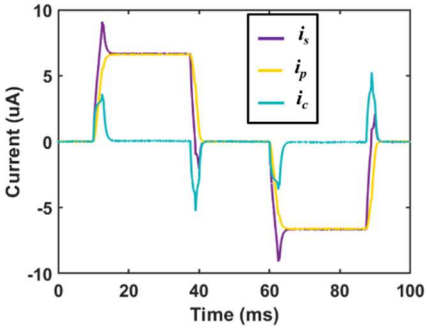

Fig. 4. Current flowing through the series resistor (i_s), probe resistor (i_p), and CMUT under test (i_c).

Following, the charge can be computed as

$$Q(t) = \int i_c(t)\, dt \tag{5}$$

and the capacitance can be obtained from

$$C(t) = \frac{Q(t)}{v_2(t)} \tag{6}$$

Finally, the dependence from time can be removed by plotting the capacitance C against increasing values of v_2, thereby generating the C-V curves. These curves are then used to estimate V_{col} and V_{sb}.

Using this approach, each acquisition provides all the data needed to estimate V_{col} and V_{sb} in approximately one second, including processing time. This significantly reduces the exposure of the device under test to the electric field, minimizing the risk of charge trapping and improving the measurement repeatability. Furthermore, this short measurement time makes this method suitable for wafer-level characterization. This technique also provides high voltage resolution, as the voltage step is limited only by the record length of the oscilloscope employed.

Nevertheless, this method poses some challenges. First, the acquired data must be compensated for the input impedance of the probe. Furthermore, it requires generating an arbitrary waveform, tailored on the characteristics of the specific device under test, because the maximum voltage applied must exceed the collapse voltage value of the CMUT.

III. Results

The two approaches described were used to obtain the C-V curves of a CMUT element, enabling investigation of the collapse and snapback phenomena and assessment of the corresponding voltages. Initially, impedance analysis was carried out by performing a V_{DC} voltage sweep from 0 V to 70 V, and from 70 V to 0 V, followed by a sweep from 0 V to −70 V, and finally from −70 V to 0 V, with a voltage step of 1 V. Positive and negative voltage sweeps were performed to ensure that the net charge applied to the device is zero. The capacitance values of the CMUT under test were then extracted and plotted as a function of the applied bias voltage. The same CMUT element was tested using the proposed fast C-V assessment method. The comparison of results from both techniques is shown in Fig. 5.

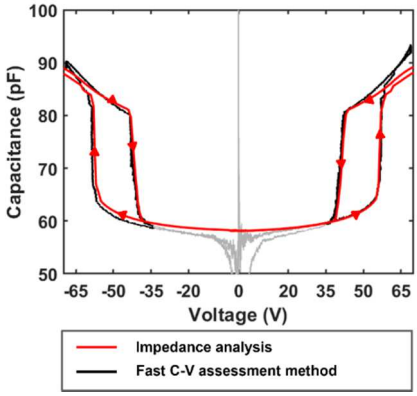

Fig. 5. Comparison of impedance analysis and fast C-V assessment method results.

As can be noticed, the C-V curves shown in Fig. 5 are nearly superimposed, providing the same values of collapse and snapback voltage of the CMUT under test. However, in the fast C-V assessment method, the capacitance values at low voltages are not measured accurately. Additionally, the capacitance curves in the high-field regions are not identical. This indicates that the fast C-V assessment method is not suitable for capacitance measurements across all the voltage range, although it is very effective for estimating collapse and snapback voltages. For what concerns the measurement time, it took 5-7 minutes to acquire data from the improved impedance analysis technique, whereas the measurement time was less than one second for the fast C-V assessment method.

To achieve higher resolution in the transitions to collapse and snapback regions, another set of data was acquired using the improved impedance analysis technique. A V_{DC} unipolar sweep between 35 V and 70 V and back was performed, with voltage increments of 0.1 V. The resulting C-V curve, compared with that from the fast C-V assessment method, is reported in Fig. 6.

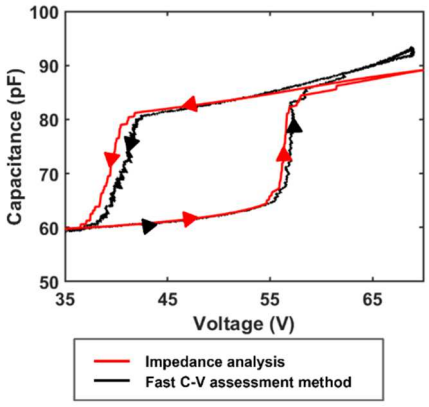

Fig. 6. Comparison of fast C-V assessment results with high-resolution impedance analysis results.

The high-resolution impedance analysis curve in Fig. 6 (red curve) reveals discrete steps in the transitions to collapse and snapback regions, indicating the collapse and snapback of individual cells within the element. The intra-element variability of the collapse and snapback voltages is due to fabrication-related nonuniformity of the cells [7], [8]. Acquiring these high-resolution results took around 40 minutes, therefore the device was exposed to the risk of charge trapping. Indeed, the charging effect is evident from

the comparison with the C-V curves obtained with the fast technique: by observing Fig. 6, it can be noticed that the two curves are slightly shifted, likely because of the accumulation of charges in the in-cavity insulation layers of the CMUT. This phenomenon was not observed during the comparison with the C-V curves obtained from the coarse sweep of V_{DC} shown in Fig. 5.

IV. Conclusions

In this work, two different techniques were applied for the estimation of collapse and snapback voltages of CMUT array elements from C-V curves. To mitigate the risk of inducing premature collapse during conventional low-frequency impedance measurements, we performed impedance analysis at twice the resonance frequency of the CMUT at maximum bias voltage. Additionally, we proposed a novel fast C-V assessment method that prevents charge trapping and reduces the measurement time. Both techniques yield similar collapse and snapback voltage estimates. However, the fast technique cannot be used for capacitance measurements in low bias conditions. While the improved impedance analysis provides deeper insight into the collapse of individual cells across the element, supporting the estimation of intra-element cell nonuniformity, the fast C-V assessment method prevents charge trapping in the in-cavity insulation layers and enables wafer level testing thanks to the lower acquisition time.

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