An Adaptive 2-Mode Bias-Flip Rectifier with Lowered Cold-Startup Voltage Requirement for Multiple Piezoelectric Energy Harvesting

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DOI
10.1109/TPEL.2025.3532856

Publication date
2025

Document Version
Final published version

Published in
IEEE Transactions on Power Electronics

An Adaptive Two-Mode Bias-Flip Rectifier With Lowered Cold-Startup Voltage Requirement for Multiple Piezoelectric Energy Harvesting

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***Abstract*—Various bias-flip rectifiers were proposed to improve the energy extraction performance for piezoelectric energy harvesting (PEH), which requires a power supply. However, no stable power supply is available when the system starts from a cold state. Typically, during the cold state, the system operates as a passive full bridge rectifier (FBR) to build up a stable power supply by charging a capacitor and then switching to the active rectifier after the cold state. Unfortunately, the system cannot start up if the open circuit voltage from a piezoelectric transducer (PT) is lower than the required supply voltage level. As a result, the system would end up with cold startup failure. This article proposes a two-mode bias-flip rectifier, which addresses the startup issue by lowering the required input open circuit voltage from the PT. The proposed design was fabricated in a 180-nm BCD process. Measurement results show that the necessary open-circuit voltage from the PT is lowered by 73% to achieve a successful cold startup, and the proposed system achieves 1182% energy extraction enhancement compared to a passive FBR.**

***Index Terms*—Bias-flip rectifier, cold-startup, open circuit voltage, piezoelectric energy harvesting (PEH), synchronized switch harvesting on inductor (SSHI) rectifier.**

I. Introduction

ENERGY harvesting (EH) has become a promising solution to replace traditional batteries, often bulky and costly for maintenance in Internet-of-Things applications. The EH can scavenge energy from many external sources, e.g., solar, thermal, RF, and kinetic, etc., to power low-energy electronics [1], [2], [3], [4], [5], [6]. Among these energy sources, kinetic energy has the benefits of low cost, low operating frequency, and high power density, which is around 10–500 $\mu \mathrm{W} cm^{-2}$. The kinetic energy is converted to electrical energy through a piezoelectric transducer (PT). A weakly coupled PT vibrating at its resonance frequency can be modeled as an ac current source, I_P, in parallel with an intrinsic capacitor, C_P, and a resistor, R_P, as shown in the left of Fig. 1. Since the output of the PT is ac energy, a rectifier is required to convert the ac into dc energy to power loads [7], [8], [9], [10], [11], [12].

Received 21 June 2024; revised 16 October 2024 and 13 December 2024; accepted 20 January 2025. Date of publication 24 January 2025; date of current version 20 March 2025. Recommended for publication by Associate Editor Michael A. E. A.E. Andersen. *(Corresponding author: Sijun Du.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3532856.

Digital Object Identifier 10.1109/TPEL.2025.3532856

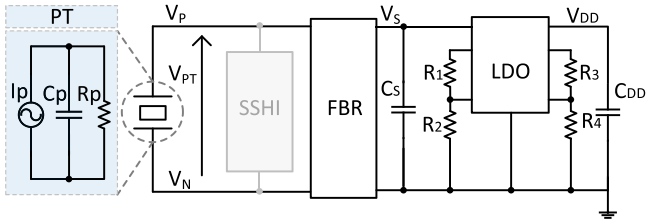

Fig. 1. Conventional cold-startup circuit working as an FBR.

The most straightforward and typical ac–dc rectifier is a full bridge rectifier (FBR) [13]. It employs four passive diodes and does not require any active components while sacrificing the power extraction efficiency. The poor performance of an FBR is caused by the PT voltage flipping moment from positive to negative, or vice versa, at the zero-crossing moment of I_P. And in this process, the FBR has to flip the PT voltage slowly with the charge harvested by the PT itself. The passive diodes' high voltage thresholds also dissipate extra energy. To improve the output power efficiency, some active bias-flip rectifiers were proposed in recent years [13], [14], [15], [16], [17]. An efficient bias-flip rectifier, named synchronized switch harvesting on inductor (SSHI) rectifier, has been verified that it can enhance the output power efficiency largely with the help of using an inductor to flip the PT voltage [18], [19], [20], [21], [22].

An SSHI rectifier requires a stable voltage supply (V_{DD}) to operate and control the active switches. However, there is no available dc voltage supply when the system starts from a cold state, resulting in the system having to operate as a passive FBR to build up a stable dc supply. After the cold state, when the voltage supply is ready, the active rectifier will work normally. However, the input open circuit voltage amplitude (V_{OC}) from the PT can be very low, e.g., 0.5 V, in many applications when the PT is implemented in a low-excitation environment. In this case, the system would never build up a stable voltage supply from the low V_{OC}, and the system cannot start up normally. As a result, the active rectifier will not be engaged. Most prior research works do not give much detail about achieving cold-startup in low V_{OC}, and they employ precharged capacitors to avoid startup issues [23], [24], [25]. Du et al. [26] divides the PT into two regions and utilizes a specific region to effectively increase the V_{OC} by sacrificing some generated power. The authors in [27] proposed a reconfigurable SSHI rectifier with

only one PT, involving four diodes and four capacitors. There are also two modes: 1) mode I and 2) mode II. In mode I, the system works as a voltage multiplier, while in mode II, it works as a typical SSHI with two load capacitors connected in series, reducing the effective output capacitance. The authors in [28] proposed a self-configurable rectifier for an extended operating range of piezoelectric energy harvesting (PEH). However, it only configures an FBR and a voltage doubler, resulting in a limited extension.

Recently multiple PTs energy harvesting techniques have drawn much attention due to their high power density [29], [30], [31]. However, they are not focusing on cold-startup circuit in low excitation. This article investigates an SSHI rectifier with low input open circuit voltage for multiple-PT energy harvesting. The input V_{OC} is 0.5 V and desired power supply is 1.8 V. The system cannot start up normally for a typical FBR circuit with such a low V_{OC}. The proposed bias-flip rectifier has two configurable modes, and 4 PTs are employed as the energy sources. The 4 PTs are configured in series connection, namely, mode I, to address the cold-startup issue for low V_{OC} and build up a high power supply. At the end of mode I, a 1.8-V voltage supply becomes available, ending the cold state. Consequently, the configuration changes to parallel, namely mode II, to achieve higher power tracking and output power efficiency. Compared with other rectifiers [1], [2], [3], the proposed rectifier in our work does not increase the overall cost, as it utilizes the same inductor shared among the input piezoelectric transducers (PTs).

The rest of this article is organized as follows. Section II analyzes the cold startup in traditional and proposed rectifiers. Section III shows the proposed system and circuit implementations, respectively. The measurement results are presented in Section IV. Finally, Section V concludes this article.

II. Proposed Cold-Startup Theoretical Analysis

A. Cold-Startup in Conventional Circuit

In a cold state, there is no available power supply. The active rectifier would operate as an FBR instead until the power supply, V_{DD}, is available. Fig. 1 shows the conventional cold-startup circuit. The PT consists of an ac current source, I_P, in parallel with a capacitor, C_P, and a large resistor, R_P. The V_{PT} is the voltage across PT. In the cold state, the SSHI rectifier is disabled, and only an FBR combined with a low dropout (LDO) regulator can work. The C_S is the storage capacitor, and V_S is the output voltage. The LDO is used to build up a V_{DD} charged by C_{DD} whose energy is derived from the storage capacitor, C_S. In traditional FBR circuits, the maximum V_{DD} can be expressed by

$$V_{DD} = V_{S(MAX)} = V_{OC} - 2V_D \tag{1}$$

where V_D is the voltage drop of the diode. According to (1), the V_{DD} is lower than the open circuit voltage V_{OC}. If V_{OC} is too low to build up a required V_{DD}, the circuit would not start up normally, and the system would end up with startup failure.

The output power of an FBR can be written as [32]

$$P_{FBR} = 4C_P V_S f_P (V_{OC} - V_S - 2V_D). \tag{2}$$

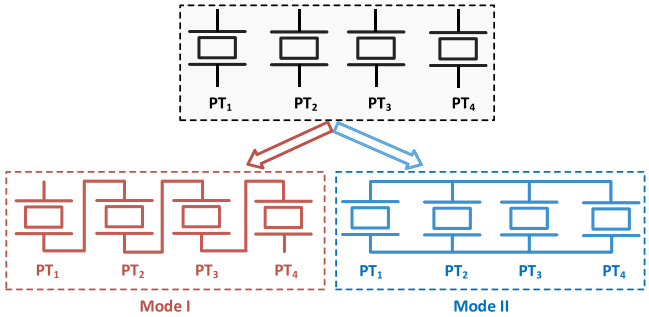

Fig. 2. Multiple energy source inputs of the proposed system for eased cold startup.

When the 4 PTs are connected in parallel as the input, the effective C_P is increased by 4× while the open circuit voltage remains unchanged. Therefore, the output power of a conventional FBR with 4 PTs connected in parallel is expressed by

$$\begin{aligned} P_{FBRP} &= 4 \times 4 \times C_P V_S f_P (V_{OC} - V_S - 2V_D) \\ &= 16 \times C_P V_S f_P (V_{OC} - V_S - 2V_D). \end{aligned} \tag{3}$$

B. Cold-Startup in Proposed Circuit

In the proposed SSHI rectifier, there are four identical PTs employed as the input energy sources [33]. The PTs have the same intrinsic capacitance and resonant frequency. They are implemented on the same vibrating substrate. On the other hand, the four cantilevers are tip-clipped together to avoid off-phase vibration. The proposed 4 PT models, PT_1, PT_2, PT_3, PT_4, are expressed in Fig. 2, each of them representing a typical PT as shown on the left of Fig. 1. During the cold state, the 4 PTs are connected in Mode I, where PTs are connected in series to generate a summed-up input open circuit voltage amplitude, V_{OCE}. The V_{OCE} can be expressed as follows:

$$V_{OCE} = 4 \times V_{OC} \tag{4}$$

where the V_{OC} is the open circuit voltage generated by one PT. Equation (4) shows that the effective open circuit voltage V_{OCE} is theoretically increased by 4×. Considering (1), the required power supply V_{DD} obtained from the new system can be written as

$$V_{DD} = 4 \times V_{OC} - 2 \times V_D. \tag{5}$$

If the desired power supply for the system is 1.8 V, the minimum V_{OC} of each single PT can be lowered to around 0.5 V (V_{OC} = (1.8 + 2 × 0.1)/4V), assuming that the voltage drop, V_D of the diode is roughly 0.1 V. In a conventional circuit, V_{OC}=0.5 V is too low to start up. While in the proposed circuit, the system can build up a 1.8V-V_{DD}, and the active rectifier would normally work after the cold state.

When the 4 PTs are connected in series, the C_P becomes 4× smaller while the V_{OC} increases 4×. According to (2), the output power of an FBR with 4 PTs connected in series is expressed by

$$P_{FBRS} = C_P V_S f_P (4V_{OC} - V_S - 2V_D). \tag{6}$$

C. Better Output Power Tracking Consideration After Cold-Startup

For a typical SSHI rectifier, the output power, P_{SSHI} can be expressed as

$$P_{SSHI} = 2f_P C_P V_S(2V_{OC} - (V_S + 2V_D)(1 - \eta_F)) \quad (7)$$

where f_P is the PT vibration frequency and η_F is the flipping efficiency of the SSHI rectifier.

When there are 4 PTs connected in series, the power expression P_{SSHIS} is written by

$$P_{SSHIS} = 4f_P C_P V_S V_{OC} - \frac{1}{2} f_P C_P V_S (V_S + 2V_D)(1 - \eta_F). \quad (8)$$

When there are 4 PTs connected in parallel, the power expression P_{SSHIP} is written by

$$P_{SSHIP} = 16f_P C_P V_S V_{OC} - 8f_P C_P V_S (V_S + 2V_D)(1 - \eta_F). \quad (9)$$

From (7), it can be found that the maximum power can be achieved by making $V_S = \frac{V_{OC}}{1-\eta_F} - V_D$. The maximum power can be expressed by

$$P_{SSHI(MAX)} = 2C_P f_P \left(\frac{V_{OC}}{1 - \eta_F} - V_D \right)^2 (1 - \eta_F). \quad (10)$$

Equation (10) shows that the maximum power is highly dependent on V_{OC} and flipping efficiency η_F. In the proposed circuit, the system is operated with the initial conditions: V_{OC}=0.5 V, η_F around 80%. When the active SSHI rectifier works normally, the output voltage V_S goes higher, resulting in a lower voltage drop, V_D. As V_D is very small, the maximum power is dominated by V_{OC} and η_F. For the SSHI rectifier with four series connected PTs, by making the optimal voltage $V_{S1} = \frac{4V_{OC}}{1-\eta_F} - V_D$, the maximum output power, $P_{SSHI(MAXS)}$, can be expressed as

$$P_{SSHI(MAXS)} = \frac{1}{2} f_P C_P \left(\frac{4V_{OC}}{1 - \eta_F} - V_D \right)^2 (1 - \eta_F). \quad (11)$$

Assuming $V_D = 0$ when active diodes are employed in the rectifier, (11) can be written as

$$P_{SSHI(MAXS)} \approx 8f_P C_P \left(\frac{V_{OC}}{1 - \eta_F} \right)^2 (1 - \eta_F). \quad (12)$$

When the SSHI rectifier is connected with four parallel-connected PTs, by making the optimal output voltage $V_{S2} = \frac{V_{OC}}{1-\eta_F} - V_D$, the maximum output power, $P_{SSHI(MAXP)}$ is written as

$$P_{SSHI(MAXP)} = 8f_P C_P \left(\frac{V_{OC}}{1 - \eta_F} - V_D \right)^2 (1 - \eta_F). \quad (13)$$

Similarly, (13) can be written as

$$P_{SSHI(MAXP)} \approx 8f_P C_P \left(\frac{V_{OC}}{1 - \eta_F} \right)^2 (1 - \eta_F). \quad (14)$$

Considering (12) and (14), they have the same expression, meaning that the connection configuration does not change the peak rectified output power. However, the maximum values are achieved at different output voltage levels, with $V_{S1} = \frac{4V_{OC}}{1-\eta_F} - V_D$ and $V_{S2} = \frac{V_{OC}}{1-\eta_F} - V_D$ for series and parallel connections, respectively. Assuming that the $V_{OC} = 0.5\,\text{V}$ and $\eta_F = 82\%$, the optimal output voltages for the maximum power in series and parallel connections are $V_{S1} = 11.1\,\text{V}$ and $V_{S2} = 2.78\,\text{V}$, respectively. Considering the device breakdown voltage of on-chip CMOS switches is 5 V, the low V_{S2} in parallel connection is better for higher output power if the system has been started.

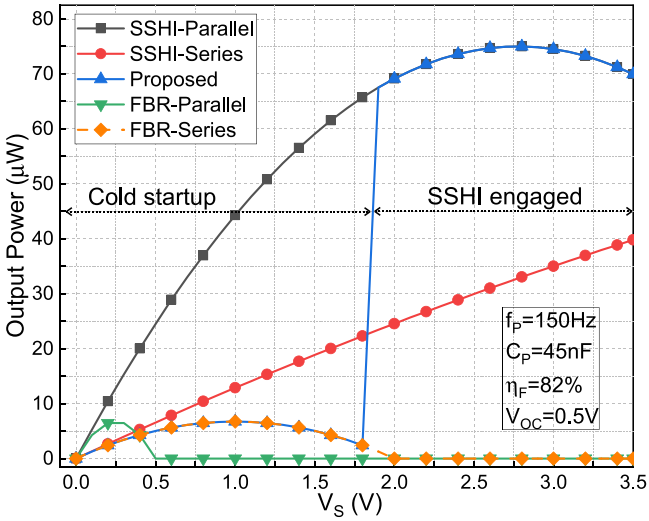

Fig. 3. Simulated output power of the rectifier with series and parallels PTs connection.

Fig. 3 shows the output power for different PT connections: parallel-FBR in (3), series-FBR in (6), series-SSHI in (8), and parallel-SSHI in (9). The figure illustrates that the parallel-connected PT FBR has a smaller output power and cannot establish a stable power supply. While the PT is in an FBR connection, it can build up an up to 2 V voltage. When a 1.8 V voltage is ready, the SSHI rectifier will work. Fig. 3 shows that the PT parallel-connected SSHI rectifier has a higher output than the series-connected SSHI rectifier. Therefore, during the cold state, the PTs are connected in series to build a stable high V_{DD}, namely, mode I. Once the V_{DD} is ready, the PTs are switched to a parallel connection to extract more power, defined as mode II.

III. System Architecture and Circuit Implementation

A. System Architecture

The system architecture is presented in Fig. 4. There are mainly five blocks: A switch control block, a charge-up block, an SSHI rectifier, an FBR and an active diode, an LDO with a load capacitor, C_{DD}, to provide a stable power supply in the cold-state. There are 4 identical PTs, PT_1, PT_2, PT_3, and PT_4 as the inputs. When the system starts from the cold-state with a low input open circuit voltage, these 4 PTs are working in mode I, where the PTs are all connected in series by turning ON S_1 to S_3 and turning OFF S_4 to S_9. This method allows the effectual output open circuit voltage up to 4× higher than a single PT. The S_1 to S_3 are the same as TG_1 as shown on the left of Fig. 4,

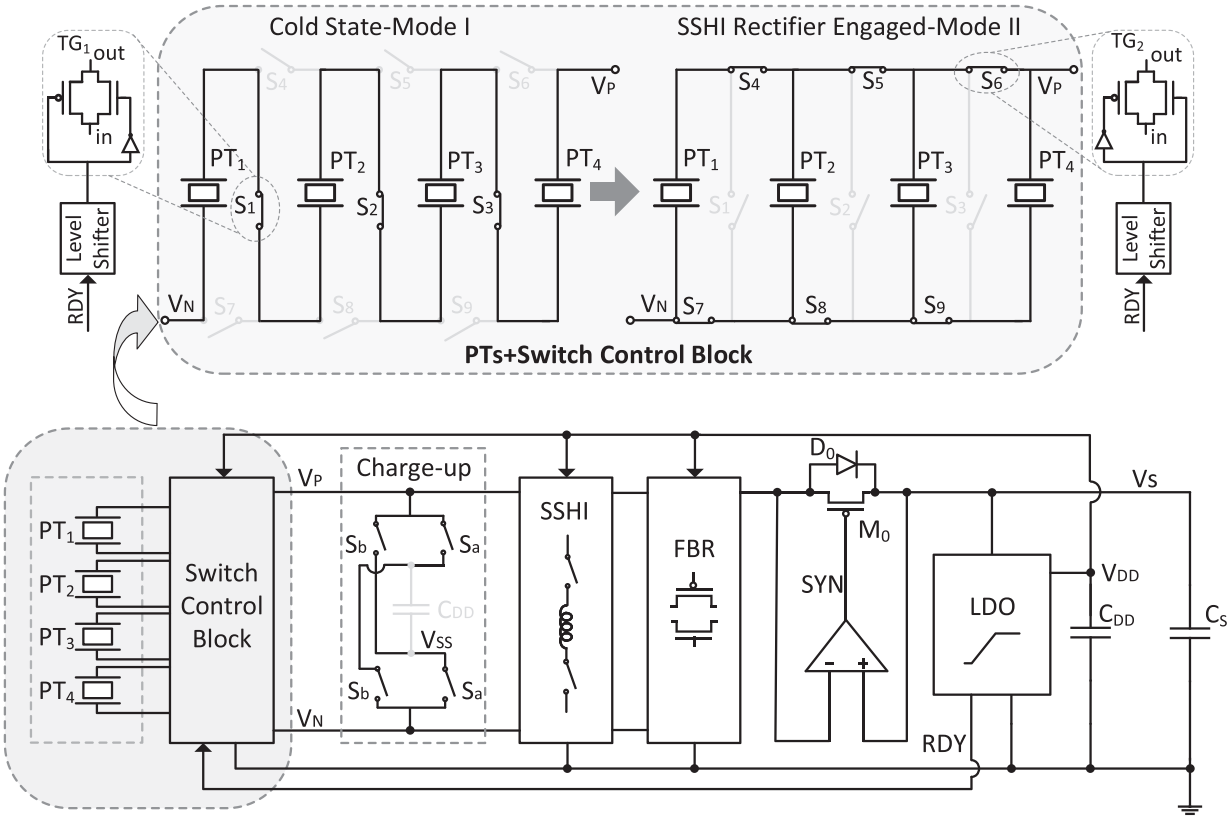

Fig. 4. System architecture of the two-mode switching bias-flip rectifier.

which is turned ON by low input. Meanwhile, the S_4 to S_9 are the same as TG_2, as shown on the right, which is turned ON by high input. When the system starts to harvest energy, a RDY signal is generated from the LDO and used to generate a SYN_C signal to control the switch control block. It follows the output voltage at first and turns to low when the power supply V_{DD} is ready, indicating that the cold state is finished.

When the cold-state is finished, as mentioned in Section II-C, the connection will be switched from series (mode I) to parallels (mode II) to extract higher power. However, when the connection changes from series from parallels, the voltage, V_{PT}, will drop naturally by 4× instantly. Since the single open circuit voltage is only around 0.5 V, it is impossible to charge the dropped V_{PT} to the threshold voltage $V_S + 2V_D$ (around 1.8 V). Thus, a charge-up block is required to help C_P to overcome the threshold voltage after the PTs connection is changed. The charge-up block is implemented by two switches, S_a and S_b, and the load capacitor, C_{DD}, of the LDO as shown in Fig. 4. After the charge-up finishes, the system will operate as an active SSHI rectifier with four paralleled PTs. The circuit implementation details of the system are shown in the following contents.

The FBR includes four cross-connected MOSFETs. The active diode, M_0, is connected to the output storage capacitor, C_S, and can prevent the reverse current out of C_S. The left FBR consists of 4 cross-connected MOSFETs. When the rectified voltage reaches the threshold voltage, the M_0 is ON. Otherwise, it is OFF. The ON-OFF state of the M_0 is controlled by a synchronized signal, SYN, generated from the active diode's comparator.

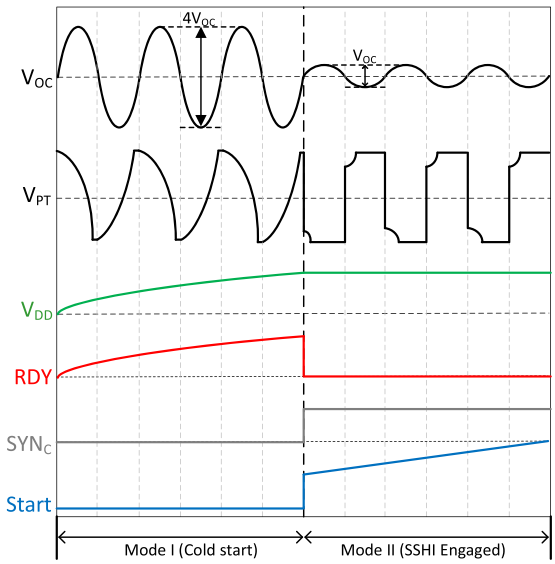

Fig. 5. Key signals during the transition moment of the two modes.

When the system starts from the cold state, the SYN is not high enough to open M_0 since the threshold voltage of M_0 is around 800 mV. In this case, the body diode D_0 is the main door for the current to flow into C_S.

The system signals of V_{OC}, V_{PT}, V_{DD}, RDY, SYN_C, and $Start$ are shown in Fig. 5. In mode I, the four input PTs are connected in series, resulting in 4× V_{OC}, where V_{OC} is the

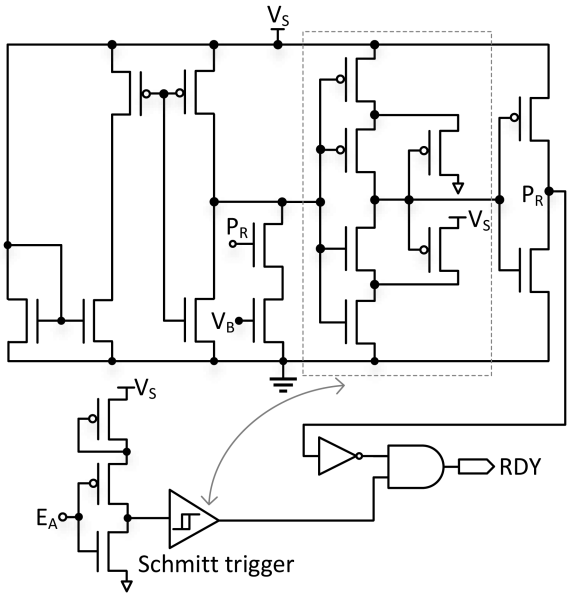

Fig. 6. RDY signal generation from the LDO.

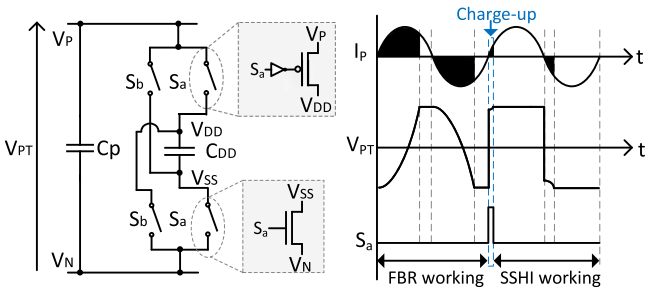

Fig. 7. Charge-up block and associated signals.

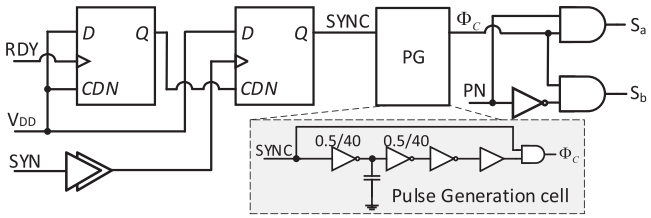

Fig. 8. Switch control signal generation for the charge-up block.

open circuit voltage of one PT. The V_{PT} waveform shows no PT voltage flipping during this period since the circuit operates as an FBR. The power supply V_{DD} is building up, and RDY follows V_{DD} during this period. When the V_{DD} is ready, the RDY turns to low, resulting in a rising edge signal for SYN_C to control the PT switching block. After the level shifters, the SYN_C is levelly shifted to a high level, namely $Start$, to drive the switches directly. The $Start$ signal is kept low during the cold state and changes to the highest voltage to fully turn ON the series-connected PT switches. Then, it turns OFF the parallel-connected PT switches. So, the PT connection changes from mode I to mode II. Then, input effective V_{OC} becomes $1\times$. Afterward, the charge-up block and SSHI rectifier will start working.

B. RDY Signal Generation From LDO

The RDY is used to switch the supply of the bandgap inside the LDO to achieve stable operation and low power for the LDO. Meanwhile, this design also considers it the cold-state indicator. The RDY generation is presented in Fig. 6. The E_A is generated by comparing the output voltage with a reference voltage as introduced in [34]. It has a high voltage equal to $V_S - V_{GS}$, and P_R is low during the cold-state. Therefore, RDY equals V_{DD} during the unconscious state. When the output voltage V_S reaches the required power supply voltage V_{DD}, the E_A changes from high to low, and P_R varies from low to high. Therefore, RDY changes to low, indicating that the cold state has been finished. The Schmitt trigger is used to avoid ringing response during the transition, as shown in Fig. 6.

C. Charge-Up Block

When the connection of the PTs is changed from series to parallels after the cold state, the V_{PT} will drop by $4\times$. Therefore, the charge-up block is used to charge the dropped V_{PT} close to the threshold voltage to start the SSHI rectifier normally. The charge-up block is shown in Fig. 7. Considering two flipping directions, there are two group switches, S_a and S_b. When the connection changes, for the first flipping cycle, if V_{PT} needs to flip from negative to positive, V_P will be connected to V_{DD} while V_N will be connected to the ground V_{SS}. Therefore, S_a is turned ON and vice versa. The upper switch comprises an inverter and a PMOS, while the lower switch is a NMOS. On the right, the corresponding waveform of I_P, V_{PT}, and S_a are presented. Before the cold-state is ended, the system operates as an FBR and a lot of energy is wasted during V_{PT} flipping, as shown in the right black blocks. When the cold-state is ended, the flipping starts at the zero-crossing moment of I_P, and the charge-up block works in the first flipping cycle. It helps V_{PT} charge to the threshold voltage by connecting to V_{DD}. Then, the system would operate as an SSHI rectifier, and the wasted energy is reduced thanks to the inductor for PT voltage flipping.

The control signals generation of the charge-up block is shown in Fig. 8. It includes some digital logic gates and a pulse generation block. Because the charge time is only several tens μs. When the V_{DD} is built up to a preset voltage, the RDY from the LDO will generate a falling edge, which indicates that the cold state is ended. However, the PT connection would not change instantly. When the first PT flipping comes after the cold state ends, the PT connection will change from series to parallels. At the flipping moment, the SYN signal from the comparator of the active diode will generate a rising edge to start the charge-up block. Then, through the pulse generation block in Fig. 8, either S_a or S_b is created for the switching control in Fig. 7. The PN is used to indicate the flipping direction. When the V_{PT} flips from negative to positive, the PN is high, and S_a is created and vice versa. The details of PN generation are given in the following subsection.

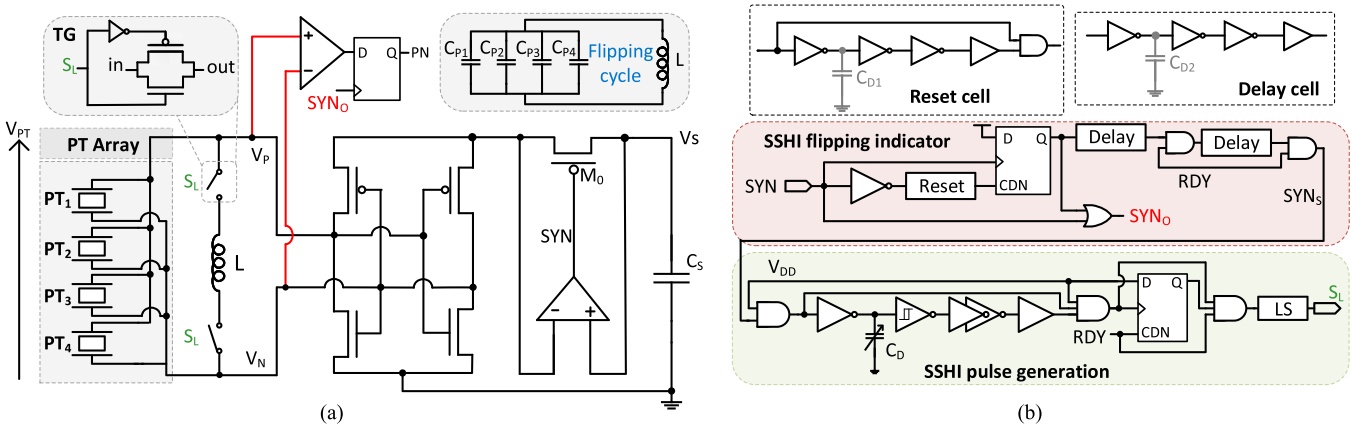

Fig. 9. Implementations of the SSHI rectifier (a) and the corresponding control signals for the switches in the SSHI rectifier (b).

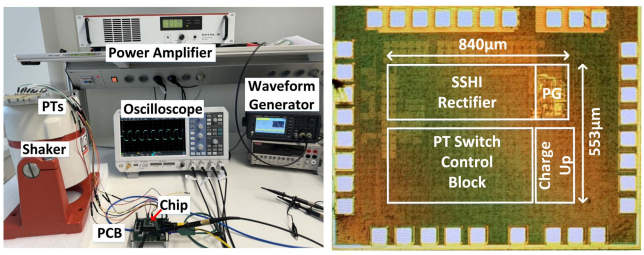

Fig. 10. Measurement setup and chip micrograph.

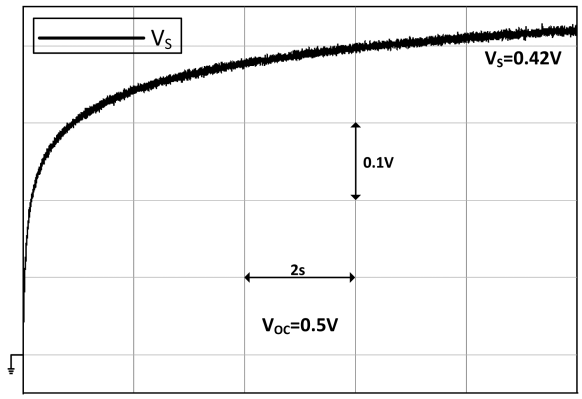

Fig. 11. Rectified output voltage of a conventional startup circuit.

D. Synchronized Switch Harvesting on Inductor Rectifier

After the charge-up, the V_{PT} can build up to the threshold voltage, and the system starts to harvest the energy. The system would operate as an SSHI rectifier. Therefore, for the second flipping time, the PT voltage will be flipped by the SSHI rectifier. The proposed SSHI rectifier is shown in Fig. 9(a). There are four paralleled PTs as the input with the same intrinsic capacitor, C_P, and resonant frequency, f_P. Since the 4 PTs are clipped on the same substrate, they have the same vibrating frequency. Therefore, they will share one standard SSHI rectifier at the same time. When it is time to flip the PT voltage, the switch controlled by S_L will be turned ON. The PN, indicating the flipping direction of PT voltage, is obtained by comparing the voltage of V_P and V_N and triggered by the rising edge of SYN_O. The SYN_O is the effective synchronized signal from SYN, as shown on the right. It is generated after the charge-up block is ended. The switch control of S_L is also presented on the right where C_D, C_{D1}, and C_{D2} are the adjustable capacitor which can be tuned according to the required period in each cell.

IV. Measurement Results

A. Measurement Setup and Die Micrograph

The experimental setup is shown in Fig. 10. The inputs are four commercial PTs (S234-H5FR-1803XB) with resonant frequency 150 Hz and intrinsic capacitance 45 nF. The chip was fabricated in a 180-nm BCD process, and the die micrograph is shown on the right of Fig. 10 with an active area of $0.47\,\text{mm}^2$. The active area is dominated by four main blocks: An SSHI rectifier, a pulse generation block, a PT switch control block, and a charge-up block.

B. Cold-Startup Verification

Fig. 11 shows the rectified output voltage of a typical cold-start circuit working as an FBR. The input open circuit voltage is around 0.5 V. The result shows that the maximum output voltage V_S of typical design is charged to 0.42 V, which is slightly lower than the open circuit voltage 0.5 V due to voltage drop across the diodes. Therefore, the maximum voltage supply generated from the typical cold-start circuit can only go to 0.42 V, which is too low to start the whole system.

C. Power Supply Building up and Charge-Up Moment

Fig. 12 shows the proposed bias-flip rectifier's output voltage and built-up power supply voltage. The input open circuit voltage amplitude is around $V_{OC} = 0.5\text{V}$. The top figure shows that the V_S can be built up from 0 to 1.8 V during the cold-start period. Correspondingly, the power supply V_{DD} is also built up from 0 to 1.8 V. When the V_{DD} attains 1.8 V, this indicates that the cold state (mode I) has been finished. Then the system changes to the SSHI-engaged phase (mode II), the V_{DD} keeps in 1.8 V while

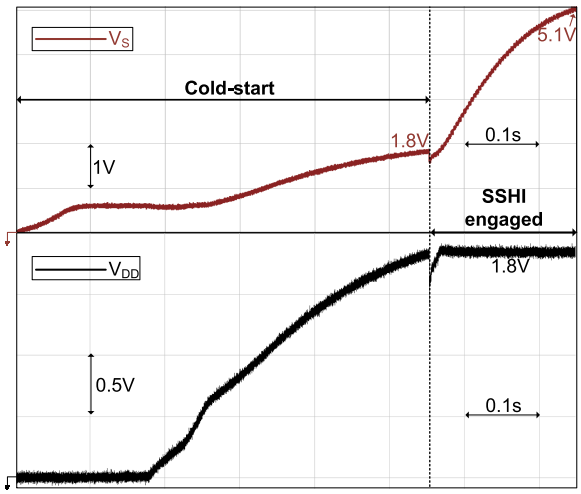

Fig. 12. Measured rectified output power and built-up power supply of proposed bias-flip rectifier.

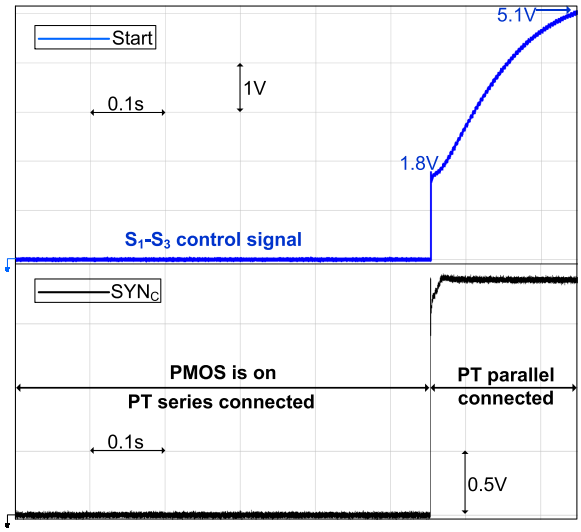

Fig. 13. Series connected control signal and SYN_C signal.

the V_S goes up to 5.1 V. When the system switches from mode I to mode II, the V_{DD} slightly drops because the charge-up block is engaged. A small amount of energy in the C_{DD} is used to charge the C_P since the effective output voltage amplitude from the 4 PTs decreases significantly due to the parallel connection, which is insufficient to sustain the SSHI operation after the SSHI rectification is engaged.

Fig. 13 top shows the switching control signal of the $Start$ signal. It is the gate-driving signal of the PT switches. During the cold state, the $Start$ signal is kept low so that the switches of S_1–S_3 are turned ON to connect the PTs in series. As a result, the effective open-circuit voltage V_{OC} can be roughly 4× higher than the open-circuit voltage of a single PT. After the cold-state, the V_{DD} keeps at around 1.8 V. Then, the $Start$ signal starts to follow the output voltage level to fully turn OFF the switches, S_1–S_3, so the PT connection is changed into a parallel connection. The bottom of Fig. 13 shows the SYN_C signal, which is used to generate the top $Start$ signal as indicated in Fig. 4.

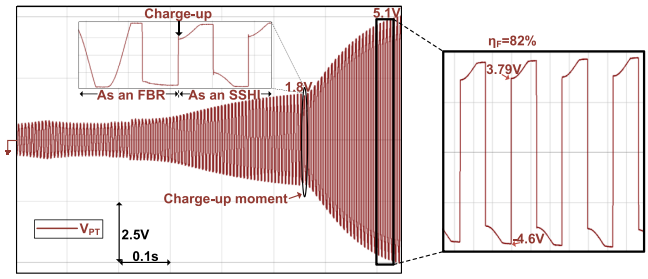

Fig. 14. Measured PT voltage of the proposed rectifier.

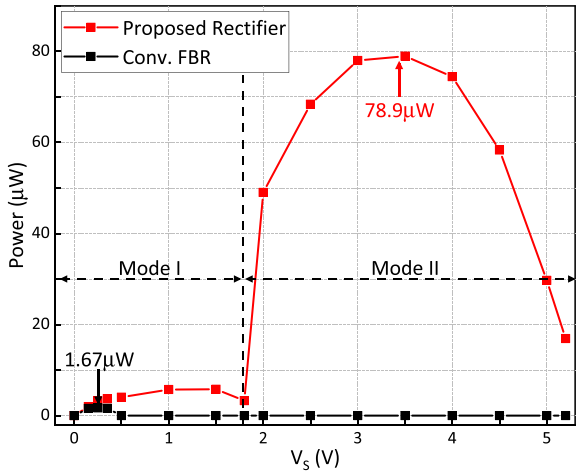

Fig. 15. Measured output power versus the output voltage of the proposed rectifier.

D. Performance Analysis of the Proposed Design

Fig. 14 shows the waveform of PT voltage, V_{PT}. The zoomed-in phase is shown on the top when the system changes from an FBR to an SSHI rectifier. After the cold state, the first bias-flip operation is triggered by the charge-up block; then, the SSHI rectifier performs the rest of the bias-flips autonomously. The PT voltage can be up to 5.1 V finally, which corresponds to the maximum rectified voltage in Fig. 12. The right zoomed-in figure shows the maximum flipping efficiency of the proposed circuit. The voltage is flipped from −4.6 to 3.79 V, indicating an 82% flipping efficiency.

Fig. 15 shows the output power of the proposed two-mode bias-flip rectifier and the conventional FBR versus the output voltage V_S. The conventional FBR rectifier has only 1.67 μW with only one PT. In contrast, the proposed bias-flip rectifier can output 78.9 μW in mode II, indicating an up to 1180% power enhancement.

Table I shows the comparison table between the proposed work and the prior art. This design was fabricated in a 180-nm BCD process rather than discrete components verification. The input open circuit voltage (V_{OC}) is low to 0.5 V. Thanks to the proposed two-mode bias-flip rectifier, the active method can overcome the cold state, and the ratio of V_{OC}/V_{DD} can be lowered to 0.27. Among these works, the proposed two-mode rectifier has the highest flipping efficiency (82%) and power enhancement (1180%).

TABLE I
PERFORMANCE COMPARISON WITH PREVIOUS WORK

	TPE'19 [26]	TPE'21 [35]	TPE'21 [19]	TIE'22 [22]	TPE'22 [36]	TPE'22 [37]	**This work**
Technology (nm)	180	N/R	N/R	N/R	N/R	N/R	180
Technique	SSHI	SSDCI	SSHI	SSHI	FBR/VD	SSHI	**SSHI**
PT Number	1	1	2	3	1	4	**4**
C_P (nF)	4.5	100	41	100	N/R	170*	**45**
Frequency (Hz)	219	22	19	30*	153	77.5	**150**
Inductor	Yes	Yes	Yes	Yes	No	Yes	**Yes**
V_{OC} (V)	2/4.2	N/R	5.8/5.2	5.8	0.4-15	3.9-5.8	**0.5**
Chip Area (mm^2)	0.2	Discrete	Discrete	Discrete	Discrete	Discrete	**0.47**
Flipping Efficiency	30%*	No	50%*	52.8%	No	66%*	**82%(Max)**
Cold Startup?	Yes	Yes	N/R	Yes	Yes	N/R	**Yes**
Startup Technique	Passive	Passive	Passive	Passive	Passive	N/R	**Active**
System Mode	2	2	1	1	2	1	**2**
V_{OC}/V_{DD}	2.8	N/R	N/R	N/R	N/R	N/R	**0.27**
P_{IC}/P_{FBR}	N/R	300%	370%	485%	100%	322%	**1180%**

*: Estimated value. N/R: Not reported.

V. CONCLUSION

This article proposes a two-mode bias-flip rectifier utilizing multiple PTs as inputs to address the cold startup issue caused by low input open circuit voltage. When the system starts from a cold state, the 4 PTs are connected in series to generate a fourfold increase in effective open circuit voltage, referred to as Mode I. During this mode, a 1.8 V V_{DD} is established with the aid of the series-connected PTs. Once the cold state concludes, the circuit automatically reconfigures from series to parallel, transitioning to Mode II, and SSHI rectifier begins to operate to extract more power. Measurement results indicate that the proposed circuit successfully builds a 1.8 V V_{DD} power supply with only a 0.5 V input open circuit voltage. This demonstrates that the proposed circuit can reduce the required input open circuit voltage by approximately 3.6×.

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