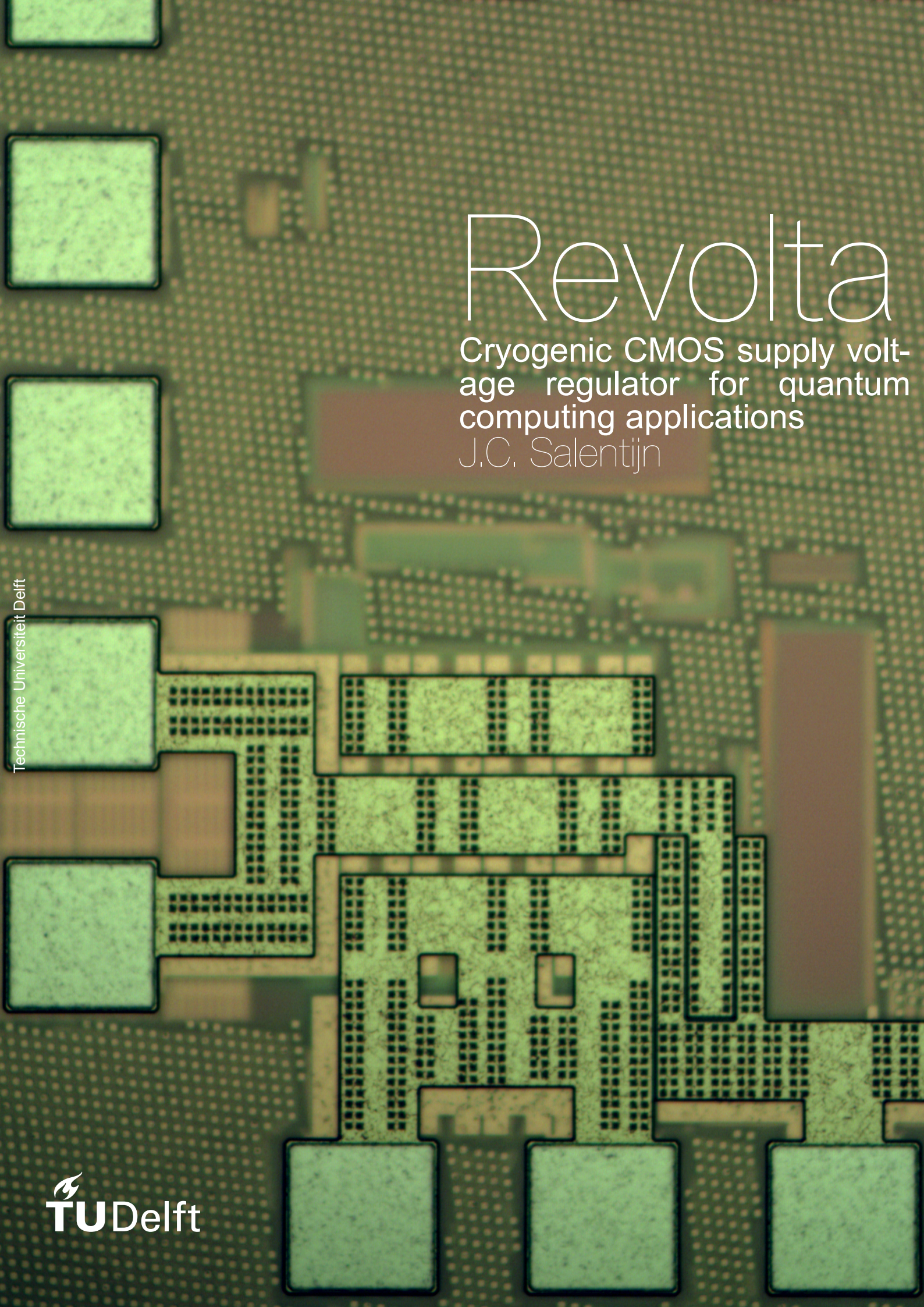

Revolta

Cryogenic CMOS supply voltage regulator for quantum computing applications

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TU Delft

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by

J.C. Salentijn

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Abstract

Quantum computers are able to deal with large problems, like molecular modelling, financial prediction and cryptography. A classical controller is used to control the qubits of the quantum computer. A proposed controller, operating at $4\ K$, needs a clean voltage supply in order to function well. The long interconnects between the room temperature power supplies and the $4\ K$ classical controller are not loss-less and do have parasitic capacitance and inductance. Low drop-out (LDO) voltage regulators are able to clean this dirty supply voltage and produce a stable, regulated voltage. Therefore, a cryogenic $40\ nm$ CMOS LDO voltage is designed. This regulated is designed with room temperature models and optimized for operating at $4\ K$. The specification are competitive to other LDO voltage regulators.

Acknowledgement

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And finally, last but by no means least, also too my wife Loïs. Thank you for always being my biggest supporter and number one fan. The support was definitely worthy of having your name on the chip.

Thank you all.

J.C. Salentijn
Delft, November 2018

Contents

1 Introduction

1.1. Quantum Computing

Today's classical computers are the best and cheapest solutions to solve common tasks. However, large problems, such as molecular modelling, financial prediction and cryptography cannot be addressed to a classical computer, because of the limited speed [1]. Quantum computers are able to deal with those large problems. The qubits, the building blocks of the quantum computer, can exist in a superposition state of $|1\rangle$ and $|0\rangle$. Classical logic is based on bits that can assume only two values, $'1'$ and $'0'$. The superposition in a qubit results in doubled computing power per each added qubit compared to classical computers. Quantum computers with 100 qubits can perform computational operations which classical computers can not do [2]. Nevertheless, a classical controller is needed to read-out these qubits.

1.2. Cryogenic Electronics

State-of-the-art qubits operate at very low temperature, close to the absolute zero. A dilution refrigerator, like the one in figure 1.1, is used to cool down to these extreme low temperatures. This refrigerator consist of several stages, each at a different temperature. The lowest stage is at the mK range, where the qubits are located. The next stage is at a higher temperature $(1 - 10K)$ and so on. The limited power budget of each stage is a major disadvantage. This is the reason why current classical controllers are placed at room temperature. The electronics needed for this classical controller consumes quite some power. However, the long interconnects are a limiting factor in scaling quantum computers to a large number of qubits, since several interconnects are used to control and read out each qubit. Therefore, a proposed classical controller close to the qubits could solve this interconnect problem [3]. Moreover, a fully CMOS controller is preferred, since CMOS offers Very Large Scale Integration (VLSI), but it must operate at cryogenic temperatures. However, CMOS transistors operate differently at $4K$ with respect to room temperature.

Figure 1.1: Dilution refrigerator, Oxford Instruments

1.3. The need of an LDO

The proposed classical controller operating at $4K$ needs a clean supply voltage. However, power supplies are still placed at room temperature. The long interconnects between the room temperature power supplies and the $4K$ classical controller are not loss-less and do have parasitic capacitance and inductance. Thus, it causes ripples and drops on the supply voltage. Voltage regulators are able to clean this dirty supply voltage and produce a stable, regulated voltage. Several active methods

are used to clean supply voltage, like switching regulators, linear regulators or a combination of both [4]. Although the efficiency of switching regulators is high, these regulators are more complex and the output ripple and noise are also higher compared to linear regulators. Low drop-out (LDO) voltage regulators are linear regulators which can achieve a very low output noise and low ripple. Therefore, room temperature LDOs have been cooled down in order to prove if these LDOs can operate at $4K$. The results are disappointing, none of the LDOs are stable at $4K$. While discrete LDOs show surprisingly better results [5]. However, discrete LDOs occupy more space with respect to integrated LDOs. Therefore, the objective of this thesis is to design an integrated LDO which can be placed close to the classical controller and which can operate at $4K$.

1.4. Objective

The main objective is to design an LDO voltage regulator which will operate at $4K$. To ease testing, the LDO should also operate at room temperature.

1.5. Specifications

The specification for the LDO design are listed in table 1.1. Chapter 3 contains a more detailed list of specifications and their rationale.

Table 1.1: List of specifications

Specification	**Symbol**	**Value**
Process		TSMC40
Output voltage	V_{out}	$1.1\ V$
Output current	I_{out}	$0 - 50\ mA$
Load regulation	$\Delta V_{out}/\Delta I_{out}$	$20\ mV/A$
Line regulation	$\Delta V_{out}/\Delta V_{in}$	$2\ mV/V$
PSRR	$\Delta V_{out}/\Delta V_{in}$	$-54\ dB$
Efficiency	η_{pwr}	95%

1.6. Thesis outline

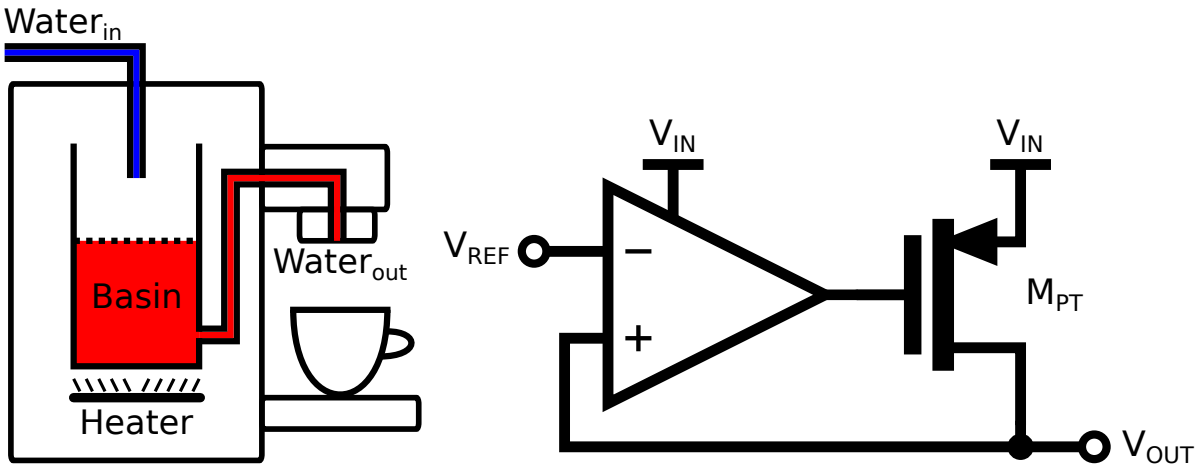
Chapter 2 describes the principle of an LDO and the differences between analog and digital LDOs. Moreover, it describes the performance and the design trade-offs. This chapter ends with examples of advanced LDO structures and a state-of-the-art overview. The specifications are given in chapter 3. This chapter also describes the behaviour of CMOS transistors at $4K$. Chapter 4 describes the design process of the cryogenic LDO. It describes the design of the LDO circuit, biasing, and test structures. This chapter ends with simulation results and layout of the test chip. The measurement results are documented in chapter 5, including the design of the PCB and the measurement setup. Finally, chapter 6 contains the conclusion and recommendations for future work.

2

Low drop-out Voltage Regulator

2.1. Principle of an LDO

Imagine the water heating system of a coffee machine, like in figure 2.1a. There is a large water basin, filled via a water inlet. The water level of the basin is fixed. This means when warm water is flowing out of the basin, cold water will be added to the basin. A heater regulates the water temperature to a set value. Therefore, when warm water is flowing out of the basin, the temperature of the water in the basin will drop, because at the same time cold water is added. Consequently, the heater is turned on and will heat the water to the set value.



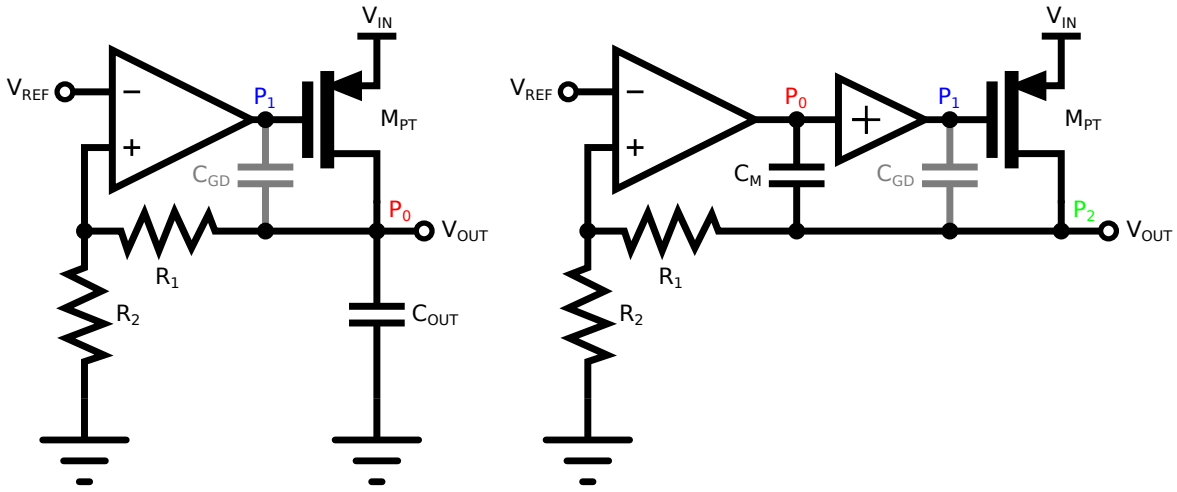
(a) Coffee machine

(b) Basic LDO circuit

Figure 2.1: The analogy between a coffee machine and a LDO circuit

The water heating system of a coffee machine resembles the working principle of a low drop-out (LDO) voltage regulator circuit (figure 2.1b). The coffee machine regulates the temperature of the outcoming water. While the LDO regulates the output voltage V_{out}. A basic LDO circuit consist of a pass device (M_{PT}) and a driver which drives the pass device. The two components are supplied by a voltage V_{in}, which is analogues to the temperature of the incoming water of the coffee machine. Consequently V_{in} and V_{out} are different potentials, which is also the case in the coffee machine system, since the temperature of the in- and outcoming water are not the same. The driver controls the current flowing in the pass device. It compares the output voltage to a reference voltage V_{ref} and produces an error signal when needed. The same happens in the coffee machine; it compares the water temperature to the set value and drives the heater when needed. Thus, a LDO circuit will ensure a steady output voltage V_{out} when the load current changes. Nowadays, there are analog and digital LDOs on the market. The decision between those two types depends on the application [6].

2.1.1. Basic analog LDO structure



(a) Dominant pole structure (b) C-free structure

Figure 2.2: Basic LDO structures

There are mainly two types of analog LDO architectures. One of these structures is a dominant pole structure, like in figure 2.2a. This structures is characterized by its large output capacitance C_{OUT}. C_{OUT} is located at the output of the LDO in order to regulate the output voltage, it solves the sudden load current changes. This circuit has two main poles, the dominant pole P_0 located at the output of the LDO and a non-dominant pole P_1 located at the gate of the pass device. Usually, the pass device is large, so the gate to drain capacitance is large as well. This capacitance acts like a Miller capacitance, which splits the poles. However, the output impedance of the driver is large. Consequently, both poles are located close to the origin. Therefore, the bandwidth of a dominant pole structure is small. The other structure is a C-free LDO structure, shown in figure 2.2b. A buffer stage is inserted to overcome the large output impedance problem. The buffer lowers the output impedance of the driver and moves the pole to higher frequencies. The large output capacitor is replaced by a Miller capacitance C_m, which sets the bandwidth of the circuit and regulates the output voltage. Moreover, the dominant pole is now located at the output of the first stage. This Nested Miller compensation structure has three main poles. The poles of this architecture are located further away from the unity gain frequency compared to a dominant pole architecture. Hence, the bandwidth of a C-free structure is larger.

The difference between the in- and output voltage is called the drop-out voltage. Usually this voltage is around $V_{drop} = 300\ mV$ [7]. The output current flows through the pass device M_{PT}, and causes power loss of $P_{loss} = V_{drop} I_{out}$. Therefore, in therms of power efficiency, a low drop-out voltage is preferred.

Pass Device

The type of pass device depends on the LDO's application. Figure 2.3 shows the most commonly used pass device structures. Single NMOS or NPN (figure 2.3a and c) are nice since the mobility is higher compared to single PMOS or PNP devices. The advantage of the higher mobility results in a lower aspect ratio and thus in a lower gate to source (base to emitter) capacitance. However, the required drop-out voltage for the NMOS and NPN are $V_{drop} = V_{gs} + V_{ds}$ and $V_{drop} = V_{be} + V_{ce}$ respectively. Single PMOS and PNP devices suffers from lower mobility and therefore, the gate to drain (base to collector) capacitance is larger. Moreover, this capacitance is amplified by the Miller effect since it operates in a common source (emitter) stage. However the required drop-out voltages are $V_{drop} = V_{ds}$ and $V_{drop} = V_{ce}$ respectively, which are much lower compared to the drop-out voltages of single NMOS or NPN devices. The BJT devices (figure 2.3c and d) suffer from a large base current, which can be improved by a Darlington pair, like in figure 2.3f. However, it requires a higher drop-out voltage. Besides, BJT devices do not operate well at $4K$, due to freeze-out in the base [1]. All single device suffers from low gain. This could be improved by cascoding, like in figure 2.3e. Again, the required drop-out voltage is higher with respect to single devices. Consequently, a single PMOS transistor is the best solution in order to achieve a low drop-out voltage.

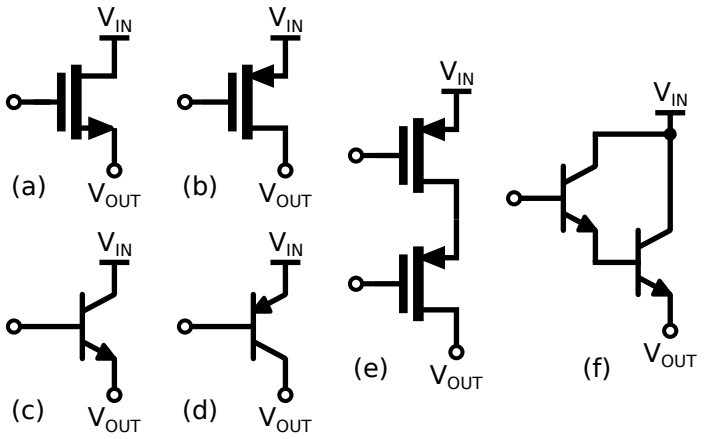


Figure 2.3: Analog pass devices (a) NMOS, (b) PMOS, (c) NPN, (d) PNP, (e) cascoded PMOS, (f) NPN Darlington pair

Driver
The driver is the motor of the LDO. It has to ensure not only the right biasing voltage for the pass device, but also it has to provide gain and bandwidth to ensure good performance. In most prior work, this driver is just a simple amplifier like a Folded Cascode or Telescopic amplifier. Other techniques like adaptive biasing or Dynamic Frequency Compensation (DFC) could be applied in order the increase the bandwidth or improve the stability of the circuit.

2.1.2. Basic digital LDO structure

Nowadays, there is a strong need for low power electronics operating at low supply voltages. Compared to analog LDOs, digital LDO can operate at much lower supply voltages. Figure 2.4 shows a simple digital LDO structure. Similarly to the analog LDOs, it consists of a pass device and driver. The pass device is an array of small mosfets, which are driven by the controller. A comparator compares the output voltage to the reference voltage and produces an error signal to the controller. This controller fully turns on or off the mosfets depending on the load conditions. Therefore the on-resistance of the pass devices changes. Compared to analog LDOs, the pass device can be smaller since the transistor are fully turned on or off and thus the digital LDO can be faster. Nevertheless, the output voltage is always bouncing between two values in steady state situation. The resolution defines what the difference of these values is. Moreover, the bouncing behaviour introduces spikes in the output voltage. To target low output ripple and noise, there is a preference for analog LDOs.

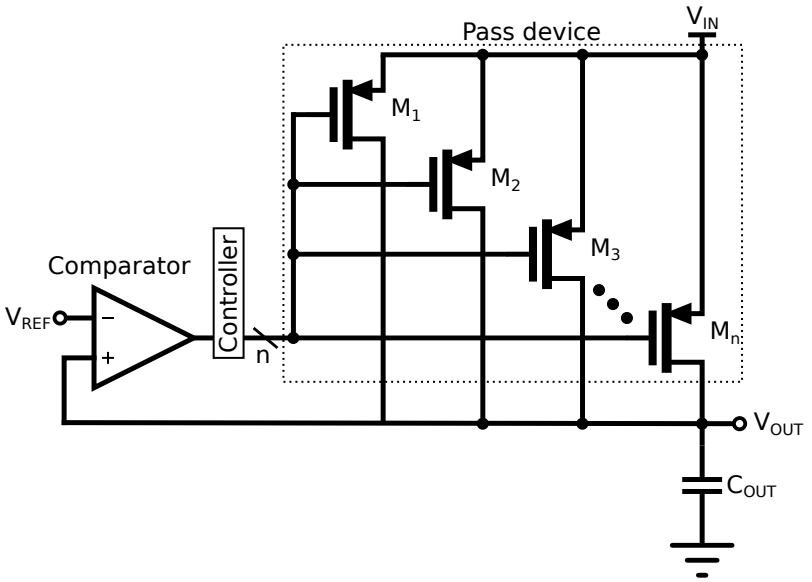


Figure 2.4: Basic digital LDO structure

The sizing of the array of mosfets depends on the implementation of the controller. It is sized uniformly when the controller is just a simple shift register. In this case, each mosfet of the array can deliver the same amount of current. This implementation is simple and effective, but rather slow since the output of the shift register is only 1 bit. This can be improved by sizing the array of mosfets in a binary way. This means that the width of $M3$ is twice the width of $M2$ and four times the width of $M1$ and so on. The controller should be adjusted such that it drives the array in the right way. Most of the time, a digital LDO is a single pole system, since full swing signals push the poles and zeros to high frequencies. Only the output pole should be placed carefully in order to implement a stable circuit. Moreover an external large capacitor is located at the output of the LDO to overcome sudden load current changes.

2.2. Performance

The performance of an LDO is divided into DC- and dynamic performance. DC performance also include line and load regulation and dynamic performance includes stability, transient response and power supply rejection (PSR).

2.2.1. Line regulation

The ratio between the output voltage variation due to a DC input voltage variation and the input voltage variation is called the line regulation. In other words, line regulation measures the variation of the output voltage due to a variation of input voltage. It is defined as

$$\text{Line regulation} = \frac{\Delta V_{out}}{\Delta V_{in}} \tag{2.1}$$

For an analog LDO, the line regulation is Li.Re. $= g_m r_o / L_o$, where g_m and r_o are the transconductance and output impedance of the pass device and L_o is the loop gain. The calculation can be find in appendix A. Therefore, a high loop gain will result in better line regulation performance. Figure 2.5 shows the output voltage versus the input voltage of a typical LDO. The output voltage is set to a desired value. When the input voltage increases, the dropout voltage increases too. Before point A, the loop gain of the LDO is too bad to regulate the LDO well. After point A, the output voltage is well regulated and it is the desired region of operation.

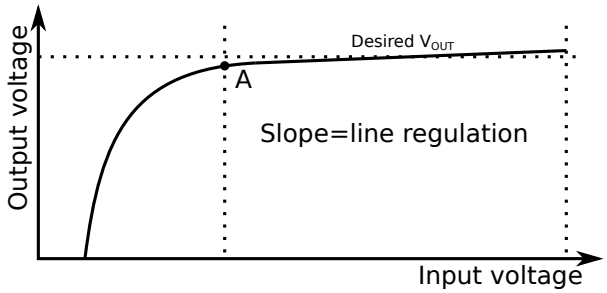


Figure 2.5: V_{out} versus V_{in}

2.2.2. Load regulation

The ratio between the output variation due to an output current variation is called the load regulation. In other words, load regulation measures the variation of the output voltage due to a variation of output current. It is defined as

$$\text{Load regulation} = \frac{\Delta V_{out}}{\Delta I_{out}} \tag{2.2}$$

For an analog LDO, the load regulation is Lo.Re. $= -r_o/(1 + L_o)$ [8]. Where again r_o is the output impedance of the pass device and L_o is the loop gain. Therefore, a high loop gain will also result in better load regulation performance. Figure 2.6 shows the output voltage versus the output current for a typical LDO. When the output current increases, the output voltage decreases. Before point A, the output voltage is well regulated due to good loop gain. However after point A, the loop gain is too bad to regulate the output voltage and the output voltage starts to drop.

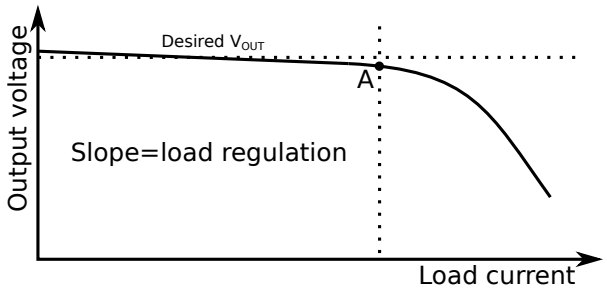


Figure 2.6: V_{out} versus I_{out}

2.2.3. Efficiency

The ratio between the in- and output power is defined as the power efficiency. The input power is the product of the input voltage and current. This input current is the summation of the currents I_{out} and I_q, where I_{out} is the load current and I_q is the quiescent current, the current consumption of the LDO. Moreover the output power is defined as the product the output voltage and current.

$$\eta_{LDO} = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}(I_q + I_{out})} \tag{2.3}$$

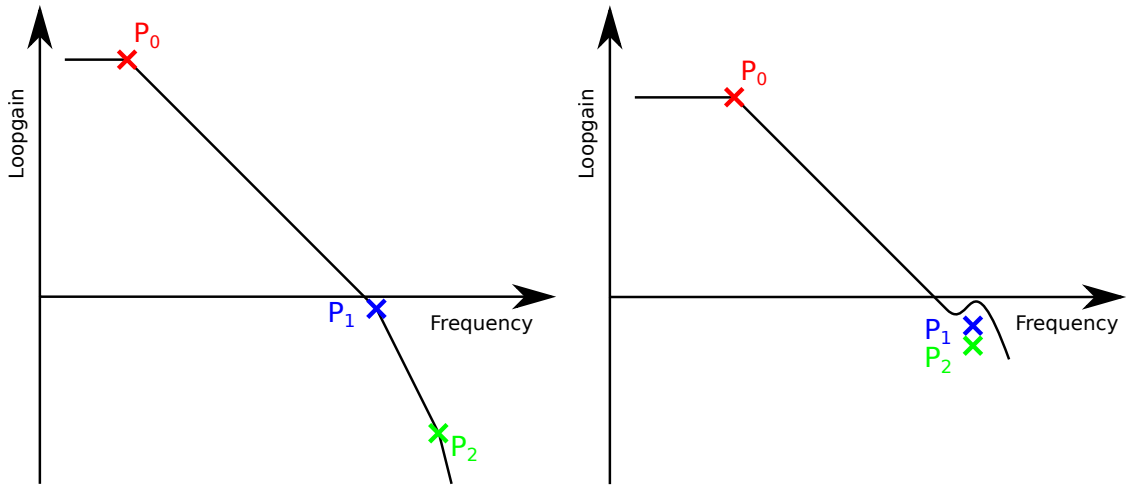
Where V_{out} is the output voltage. The difference between the in- and output voltage is the so called drop-out voltage V_{drop}. In order to make a power efficient LDO, this drop-out voltage has to be as low as possible, since the current efficiency is usually close to 1. However, lowering the drop-out voltage results also in disadvantages. It results in a lower output impedance and therefore a lower power supply rejection ratio (PSRR).

2.2.4. Maximize the output current

It is also important to know what the load will be, since it determines the maximum output current of the LDO. Moreover, the aspect ratio of the pass device depends on the maximum output current. The relationship between the the output current and drop-out voltage is

$$V_{drop} = I_{out}R_{on} \tag{2.4}$$

Where R_{on} is the on resistance of the the pass device which is defined as $R_{on} = V_{ds}/I_{ds}$. Therefore, there is a trade-off between efficiency, maximum output current and stability. A low dropout voltage and large output current is desired. This results in a low on-resistance of the pass device. However, the stabilization of such pass device becomes complex, since the aspect ratio is large.



(a) $I_{out} = high$ (b) $I_{out} = low$

Figure 2.7: Transfer curve for different load conditions

2.2.5. Stability

An LDO circuit must be stable for the specified load current range. Therefore each pole and zero should be placed carefully. Especially, a multistage architecture is much more difficult to stabilize. For example, the poles of the multistage architecture of figure 2.2b are shown, for two different load conditions, in figures 2.7a and 2.7b. The unity gain frequency $UGF = g_{m1}/C_m$ is set via the dominant pole P_0, where g_{m1} is the tranconductance of the first stage. The non-dominant poles P_1 and P_2 are located far from the UGF in order to have enough phase and gain margin. Figure 2.7a shows that the non-dominant poles P_1 and P_2 are split well via the capacitance C_{gd}, it acts like a Miller capacitance. Nevertheless, the second non-dominant pole P_2 heavily depends on the transconductance of the pass device. Thus, low output current conditions move the pole P_2 to lower frequencies until it crosses non-dominant pole P_1. The poles run in each other and become complex and causes ringing during settling. Therefore, a minimum load current is needed in order to ensure enough splitting of the non-dominant poles. Further decreasing the load current could cause instability since the non-dominant poles moves to the right half plane. However, increasing the minimum current will lower the power efficiency of the LDO.

2.2.6. Transient response

Sudden load changes can causes serious undesired voltage spikes at the output. These voltage spikes can influence the performance of the load circuitry. It is useful to know where the spikes comes from and how to improve the dynamic behaviour. Figure 2.8 shows a step response of a typical LDO. The current step goes from $I = I_{min}$ to $I = I_{max}$ in a certain rise time. The voltage will drop, because the LDO cannot respond infinitely fast to this current step. The voltage drops until a certain point and then starts to recover to the original value. The time between the start of the step and the start of the recovery is the so called response time. The response time is inversely proportional to the system bandwidth. Moreover, the amplitude of the spike is proportional to the response time and inversely proportional to the output capacitance of the LDO

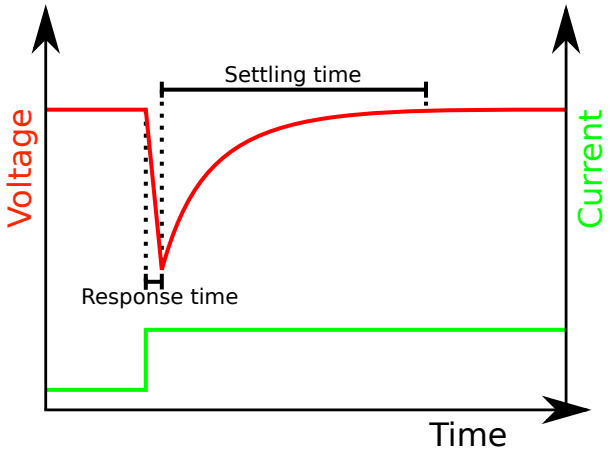


Figure 2.8: Step response

$$\Delta V_{tr} \propto \frac{\Delta I_{out}}{C_{OUT}} \Delta t_r \tag{2.5}$$

Where ΔI_{out} is the change in current, C_{out} the output capacitance and t_r the response time of the LDO. The output capacitor can deliver thus transient current in order to reduce the amplitude of the spike. Nevertheless, a large output capacitor will result a in small bandwidth. Consequently, a small bandwidth will result is a small settling time, since the settling time is inversely proportional to the bandwidth of the system.

2.2.7. Power supply rejection ratio

The power supply rejection ratio (PSRR) tells how much ripple from the input voltage will flow to the output of the LDO. It is defined as [9]

$$PSRR(dB) = 20log\left(\frac{\Delta V_{out}}{\Delta V_{in}}\right) \tag{2.6}$$

For an analog LDO, the PSRR is defined as $PSRR = A_{VO}/A_V$. Where A_V is the loop gain and A_{VO} the gain from input to output. Increasing the loop gain is one method to improve the PSRR.

2.2.8. Area

Chip area is expensive. The chip area depends heavily on the maximum current of the LDO, since the aspect ratio of the pass device is proportional to the maximum current. A minimum length of the pass

device is then preferred, since it minimizes the area for a given aspect ratio. However, increasing the length of the pass device should give a better PSRR, since the output impedance improves.

2.3. Trade-offs

At this time, there are thousands of LDOs on the market, each with different specifications. It is thus important to make sure what the LDO's application will be. Some LDOs are fast, others are power efficient and so on. There is trade-off between efficiency, maximum output current, settling time, power supply rejection ratio and area. A relative high drop-out voltage gives the advantage of a high output current and high PSRR and low area. However, the consequence is a lower efficiency with respect to a relative low drop-out voltage. As stated before, a minimum length for the power device is preferred. However, increasing this length could improve the PSRR, because of the improved output impedance. Nevertheless, the area will increase and the bandwidth will decrease, which results in a larger settling time.

2.4. Advanced analog LDO structures

Many techniques could be applied to improve the performance of an LDO. Two of these techniques are adaptive biasing and dynamic frequency compensation (DFC). Adaptive biasing is used to improve the bandwidth and slew rate. DFC is also used to improve to bandwidth.

2.4.1. Adaptive biasing

Figure 2.9 shows a three stage C-free LDO optimized with adaptive biasing. The error amplifier is biased with a nominal bias current I_{BIAS}. For high output currents, the second non-dominant pole is far away from the unity gain frequency. At high output currents, the current mirror starts to conduct current and an extra biasing current I_{AB} is applied to the error amplifier. Therefore the transconductances of both stages are increased and the dominant pole and the first non-dominant pole are moved to higher frequencies. Thus, the bandwidth is increased. A larger bandwidth results in a smaller response and settling time. Thus, this LDO with adaptive biasing is faster at higher output currents compared to the same LDO without adaptive biasing. The efficiency, even at low output currents, is still maintained. On the other hand, the higher biasing current also improves the slewing, since the gate to drain capacitor of the pass device is charged faster.

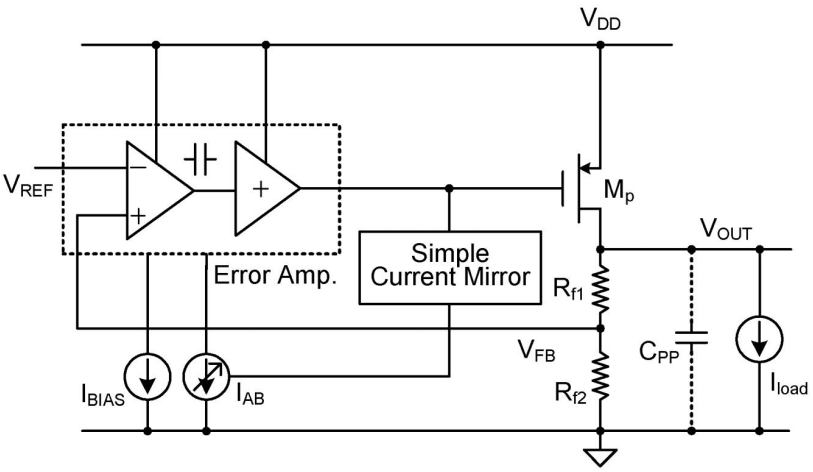


Figure 2.9: Adaptive biasing technique [10]

2.4.2. Dynamic frequency compensation

One of the problems of a C-free LDO is the minimum pole splitting at low output currents. The two non-dominant poles are complex and located at low frequencies. Instability issues are the results of these low frequency complex poles. DFC is used to split those poles in order to improve the stability at low output currents. Moreover, an extra zero is inserted and will cancel one of the non-dominant poles, resulting in an improved bandwidth. This improved structure is shown in figure 2.10. It consist of a three stage LDO optimized with DFC amplifier and two Miller capacitors C_{m1} and C_{m2}. Capacitor C_{F1} inserts a zero inside the bandwidth to cancel one of the non-dominant poles. The negative gain of the DFC block splits the non-dominant poles sufficiently.

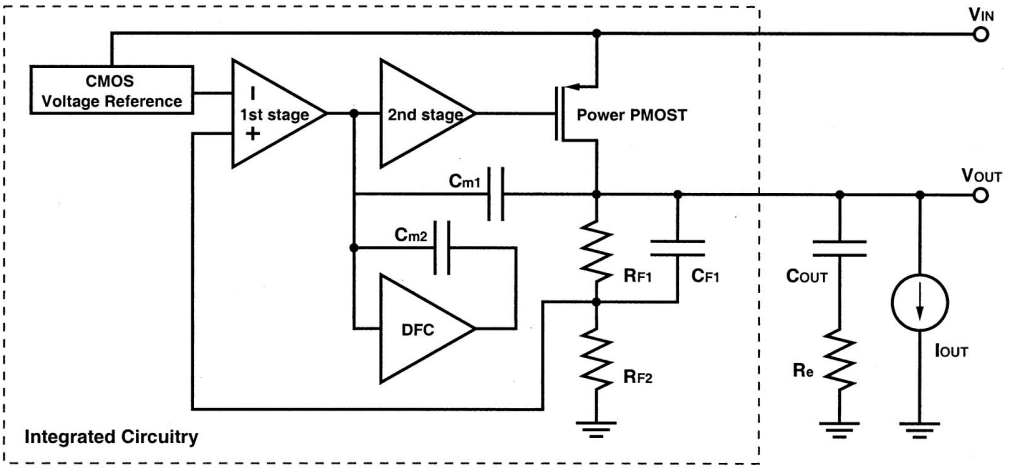


Figure 2.10: Dynamic frequency compensation [11]

2.4.3. Negative capacitance circuit (NCC)

A structure like in figure 2.11 improves the PSRR of an LDO circuit. This two stage C-free structure contains an NCC-block, frecuency compensation (FC) and a voltage damper (VD). A NCC block generates a negative capacitance which is located parallel to the gate to drain capacitor of the pass device. Therefore, the gate to drain capacitance is reduced due to the parallel negative capacitance. Hence, any signal variation on the V_{DD} node is also present at the gate of the pass device, since there is an AC short between V_{DD} and the gate of the pass device. In other words, the gate voltage follows the small signal voltage at V_{DD} perfectly, the PSRR is improved. The NCC block consists of a Miller capacitance and a non-inverting amplifier with feedback resistors. The feedback resistors are digitally trimmed in order to optimize the Miller capacitance for different load conditions, since the value of the gate to drain capacitance depends on the load current. The voltage damper senses voltage ripples and speeds up the settling. The frequency compensation ensures stability. All those extra blocks improves the dynamic behaviour, but require power.

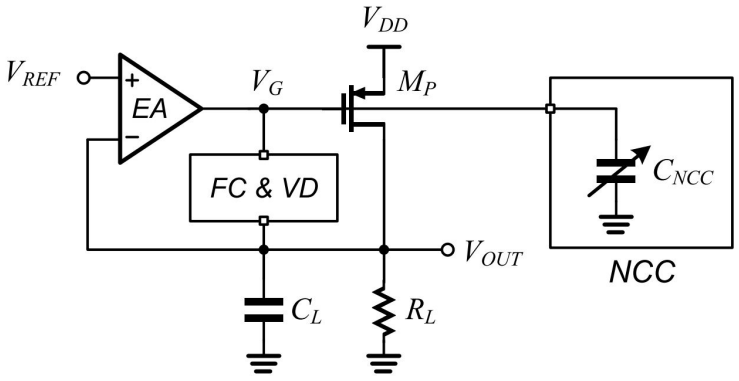


Figure 2.11: Negative capacitor circuit [12]

2.4.4. Multiple-loop design

Single loop LDO architectures are usually slow, since the bandwidth of the high gain drivers are small. The over- and undershoot of these architectures is usually larger, since the response time is relatively high. Multiple-loop design are able to improve the over-, undershoot and noise performance. Figure 2.12 shows a multiple-loop LDO design. The first loop consists of the error amplifier (Opamp), buffer and pass device M_N with feedback network. This loop maintains the output voltage. The second loop (highlighted in blue) basically introduces adaptive biasing to increase the bandwidth. This loop generates a sensing current I_{sen} which is proportional to the output current. The sensing current will be used to track the non-dominant pole. Capacitor C_z and resistor R_z introduce a zero to cancel the non-dominant pole. The third loop (highlighted in orange) senses voltage ripples and speeds up the settling by adding currents to the slowest nodes in order to improve the slewing. Again, all those loops improve the dynamic behaviour, however but require power.

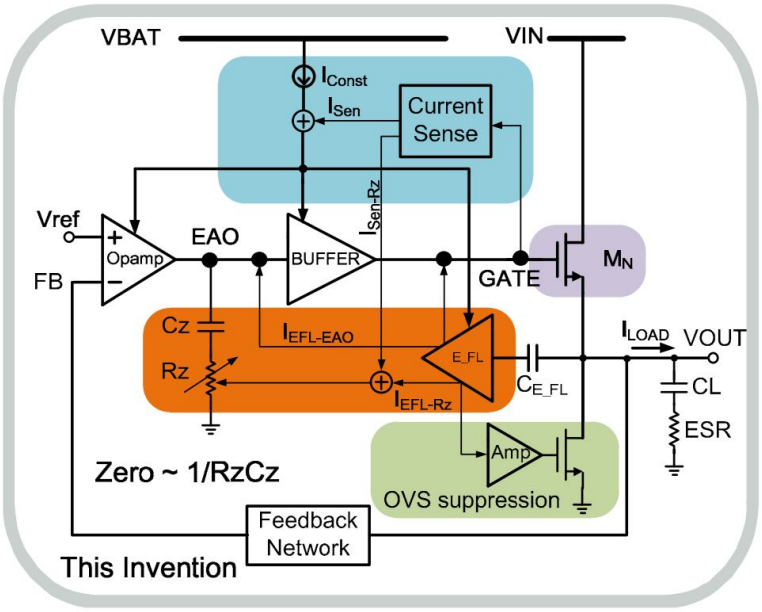


Figure 2.12: Multiple-loop design [13]

2.5. State-of-the-art

Nowadays, there are thousands of LDOs on the market, each with different performances. Table 2.1 shows an overview of state-of-the-art LDO regulators of the last years. All LDOs from this table are relatively new, are designed in a relatively small technology node and operate at room temperature. Papers [13], [14] and [15] do have high efficiency since the drop-out voltage and current consumption are low. The maximum bandwidth of the LDOs heavily depends on the process, the maximum output current, the quiescent current and the maximum output capacitance.

Table 2.1: State-of-the-art LDO voltage regulators (* DP = Dominant pole)

	[14]	[15]	[16]	[12]	[13]
Year	2015	2015	2016	2017	2017
CMOS Process	$180\ nm$	$65\ nm$	$180\ nm$	$180\ nm$	$130\ nm$
Area	-	-	$0.079\ mm^2$	$0.033\ mm^2$	$0.1825\ mm^2$
Type	C-free	C-free	C-free	C-free	DP*
Maximum output current	$50\ mA$	$100\ mA$	$10\ mA$	$100\ mA$	$300\ mA$
Drop-out voltage	$120\ mV$	$100\ mV$	$200\ mV$	$200\ mV$	$29.7\ mV$
Line regulation	$1.66\ mV/V$	$1.8\ mV/V$	$0.58\ mV/V$	-	$0.44\ mV/V$
Load regulation	$2.16\ mV/A$	$21\ mV/A$	$21\ mV/A$	-	$6\ mV/A$
Quiescent current	$4.4\ \mu A$	$3.89\ \mu A$	$142\ \mu A$	$71-101\ \mu A$	$14-120\ \mu A$
Bandwidth	-	$70\ kHz$	$20\ MHz$	-	$60\ kHz$

3

Specifications

The specifications are based in the state-of-the-art performances, the process and requirements based on the cryogenic application. Both DC and AC specifications will be discussed. The chapter ends with measurements of TSMC40 transistors at room temperature and $4\ K$ as well.

3.1. Output voltage/current

The LDO will be designed in a $40\ nm$ CMOS process from TSMC, which has a nominal supply voltage of $V_{DD} = 1.1\ V$. Consequently, the output voltage of this LDO is set to $1.1\ V$, since it will supply other circuits designed in this process.

$$V_{out} = 1.1\ V$$

To get an idea of the power consumption of other TSMC40 circuits, some other designs are checked. Some of these designs are the transmitters which will be used for qubit control. One transmitter consists of a DAC, some filters, a mixer, a LO driver and an output driver. The power consumption of one transmitter is about $36\ mW$ of power, which corresponds to $32\ mA$ of current. If this LDO will be used to power up this transmitter, the maximum current should be at least $32\ mA$. To be on the safe side, the maximum output current is set to $50\ mA$.

$$I_{max} = 50\ mA$$

Moreover, the LDO should operate well even without a load connected to the output of the LDO. Thus, the minimum load current is set to zero.

3.2. Output capacitance

The output capacitance of a LDO is limited, because the stability could be affected. Hence the capacitance at the V_{DD} node of the load circuit should be low enough to ensure a stable LDO circuit. The load circuits are modeled as a parallel RC network, like in figure 3.1. In order to find the values for R and C, and thus the maximum output capacitance of the LDO, transient simulations are done with a basic load circuit. As a test load circuit, we will consider a digital circuit.

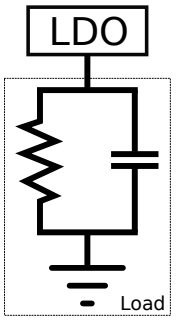


Figure 3.1: Load model

3.2.1. Load capacitance

Usually this capacitance of the digital circuits is higher compared to an analog circuits, because of the higher gate density. Therefore, the capacitance at the V_{DD} node of minimum size inverters is simulated. The setup is illustrated in figure 3.2. The input and output of the devices under test (DUT) are buffered with the same minimum size inverters, to simulate realistic loading. The layout of this circuit is made with standard inverter cells, provided by TSMC. The area of these inverters is $2.1168 \mu m^2$

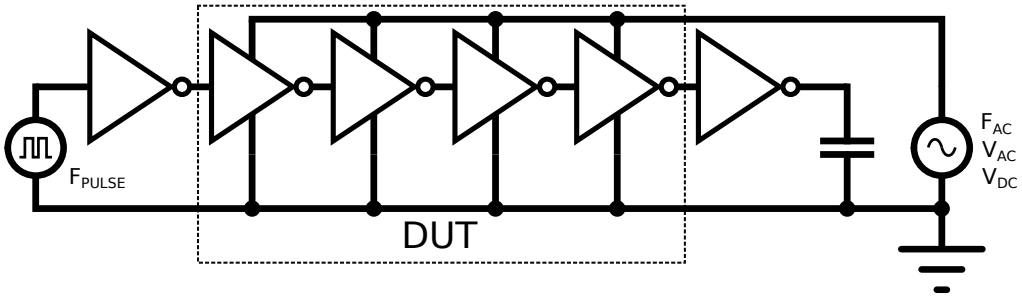
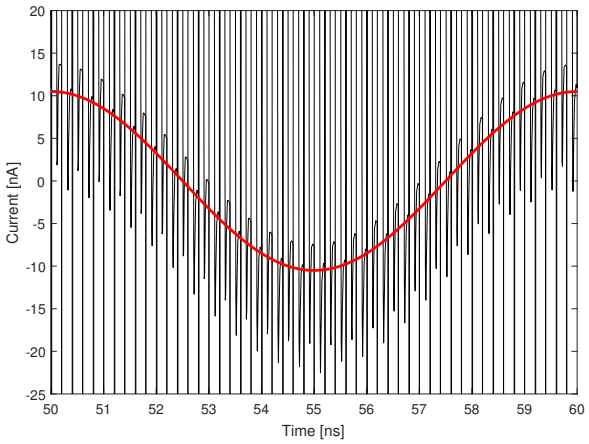


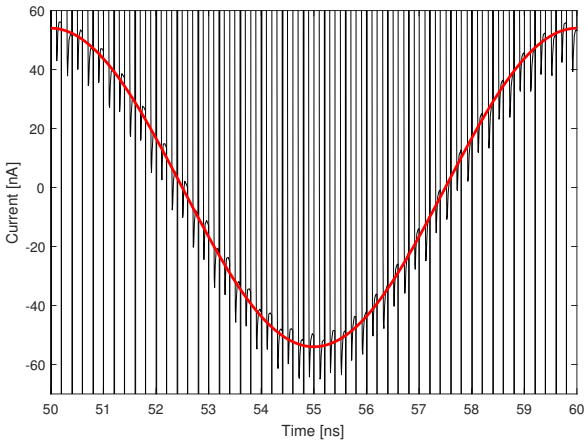
Figure 3.2: Set-up inverters transient simulations

An AC source with an operating frequency F_{AC}, amplitude V_{AC} and a dc value V_{DC} is connected to the V_{DD} node, in order to find the AC current through the capacitance. A pulse source with an operating frequency F_{PULSE} is connected to the inverting chain. Figures 3.3a and 3.3b show two plots with different settings of the sources. The figures show a sinusoidal signal with spikes from the switching behaviour. The corresponding voltage current relation of the capacitance is: $I = CVF$. Consequently, the capacitance calculated from the results from figure 3.3a is

$$C_{INV} = \frac{I}{2\pi VF} = \frac{54.5n}{2\pi \cdot 50m \cdot 100M} = 1.72\ fF \tag{3.1}$$



(a) Transient result, $F_{AC} = 100MHz$, $V_{AC} = 10mV$, $V_{DC} = 1.1V$ and $F_{PULSE} = 2.5GHz$



(b) Transient result, $F_{AC} = 100MHz$, $V_{AC} = 50mV$, $V_{DC} = 1.1V$ and $F_{PULSE} = 2.5GHz$

Figure 3.3

The rest of the simulations shows similar results. Hence the capacitance per unit area is $C_{VDD}/A = 813\ aF/\mu m^2$. Figure 3.3b shows the results with a doubled frequency F_{AC}. The current consumption is doubled which is also stated in equation 3.1. The operating frequency of the inverters does not influence these results.

3.2.2. Load resistance

The resistance of the inverters is also simulated in order to find the static and dynamic current consumption. A DC source with value $V_{DC} = 1.1\ V$ is connected to the V_{DD} node, like in figure 3.2. The operating frequency of the transistors is swept from $F_{PULSE} = 100\ MHz$ to $5\ GHz$, since the load circuits will operate in this frequency range. The resistance versus the operating frequency is illustrated in figure 3.4. The corresponding voltage current relation of the resistance is: $I = V/R$.

The results show that the current consumption increases when the frequency increases. The current consumption of the inverters, operating at $2.5\ GHz$, averaged over time is $11.3\ \mu A$. Therefore

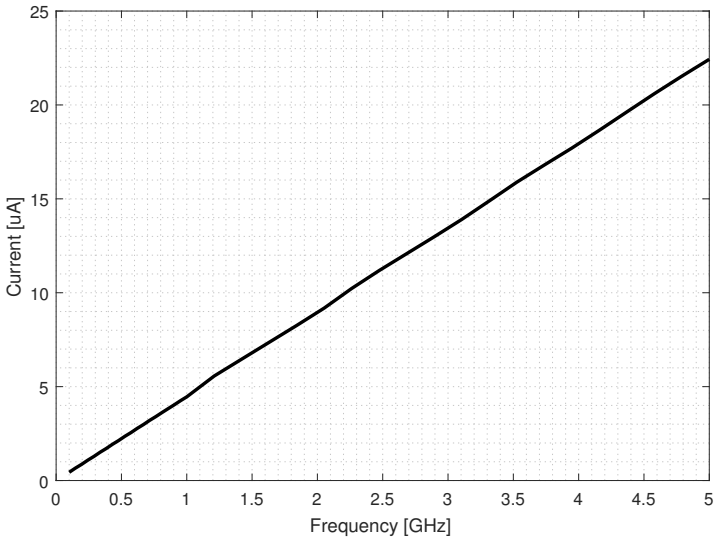


Figure 3.4: Current consumption versus frequency

$R_{INV} = 97.3\ k\Omega$. Coming back to the transmitter load, the operating frequency of the transmitters is $F_{clk} = 2.5\ GHz$ and the supply voltage is $V_{DD} = 1.1\ V$. At the end, the current consumption for a digital chip operating at $F_{clk} = 2.5\ GHz$ per unit area is $I_{VDD}/A = 5.33\ \mu A/\mu m^2$ with a activity factor of $\alpha = 1$. For example, a chip with a current consumption of $I_{max} = 50\ mA$ has an area of $9380\ \mu m^2$. The corresponding capacitance at the V_{DD} node is $C_{VDD} = 7.6\ pF$. To be on safe side, the LDO has to drive a capacitive load of at least $10\ pF$.

$$C_{out} = 0 - 10\ pF$$

3.3. Line regulation

The shift in V_{out} due to the line voltage shift from $1.15\ V$ to $1.20\ V$ is set to $0.2\ mV$. This will lead to a line regulation of $4\ mV/V$. The average line regulation is about $2\ mV/V$ [14], [15]. The output voltage is more sensitive to the input voltage when the drop-out voltage is low. Therefore, the specification on the line regulation is somewhat relaxed.

$$\frac{\Delta V_{out}}{\Delta V_{in}} = 4\ mV/V$$

3.4. Load regulation

The shift in V_{out} due to the load current shift from $0\ mA$ to $50\ mA$ is set to $1\ mV$. This would be enough to ensure operation of sensitive analog circuits. This will lead to a load regulation of $20\ mV/A$, which is in line with state-of-the-art design, as shown in chapter 2 [16] [17].

$$\frac{\Delta V_{out}}{\Delta I_{out}} = 20\ mV/A$$

3.5. Power supply rejection ratio

The line regulation is actually the power supply rejection ratio at DC. The overall line regulation is set to $4\ mV/V$, which is equal to $4\ mV/V \equiv -48.0\ dB$. Therefore the PSRR at DC is set to

$$PSRR = -48.0\ dB$$

3.6. Transient behaviour

The response time and open loop bandwidth defines transient behaviour of the system. A regular power supply regulates the voltage within 10% of the nominal supply voltage. This means that the amplitude of the spikes generated by this LDO should be lower than $V_a = 110\ mV$. Moreover, the bandwidth of the system should be higher than $BW_{ol} > 1MHz$, based on the specified maximum output current, output capacitance and power consumption.

3.7. Integrated noise

The noise coming from the circuit is divided into thermal and flicker noise. Since there are no accurate models of CMOS transistors at $4\ K$, it is difficult to define the noise specifications. Still the line and load regulations should be measurable. Therefore, the integrated noise in a bandwidth from $1\ Hz$ to $1\ GHz$ should be lower than $1\ mV_{rms}$.

$$V_{n,int} < 1mV_{rms}$$

3.8. Efficiency

A high power efficiency is desired since there is limited power budget at $4\ K$. Therefore, the aim is to design a LDO with an efficiency higher than 95%. Compared to the literature study, this number is rather high. Only a few LDO's will reach this specification.

$$\eta_{PWR} > 95\%$$

3.9. Area

The area of the chip including padring is set to $1\ mm^2$.

$$Area = 1\ mm^2$$

3.10. Specification summary

Table 3.1: List of specifications

Specification	Symbol	Value
1. Technology		TSMC40
2. Output voltage	V_{out}	$1.1\ V$
3. Output current	I_{out}	$0 - 50\ mA$
4. Output capacitance	C_{out}	$0 - 10\ pF$
5. Load regulation	$\Delta V_{out}/\Delta I_{out}$	$20\ mV/A$
6. Line regulation	$\Delta V_{out}/\Delta V_{in}$	$4\ mV/V$
7. PSRR	$\Delta V_{out}/\Delta V_{in}$	$-48\ dB$
8. Open loop bandwidth	BW_{ol}	$> 1MHz$
9. Integrated Noise ($BW = 1\ GHz$)	$V_{n,rms}$	$1\ mV_{rms}$
10. Efficiency	η_{pwr}	95%
11. Area	A	$1\ mm^2$

3.11. CMOS at 4K

The TSMC40 process offers three types of NMOS/PMOS transistors, each which a different substrate doping concentration. Therefore, a low threshold (LVT) transistor has a higher substrate doping concentration compared to a standard threshold (SVT) transistor. On the other hand, a high threshold (HVT) transistor has a lower substrate doping concentration compared to a SVT transistor. Nevertheless, the threshold voltage of these three devices will increase at $4\ K$ compared to room temperature. In addition, the mobility increases at $4\ K$ either [18].

3.11.1. Threshold voltage and mobility increase

The thermal energy in silicon is much lower at $4\ K$ compared to room temperature. Because of that, not all dopants are ionized, which results in a lower carrier concentration. Figure 3.5 shows the ionized impurity density versus temperature for three different doping levels. The impurity density at room temperature is $N_{D+}/N_D = 0.8$ for a doping concentration of $N_D = 10^{18}\ cm^3$, which is often assumed to be $N_{D+}/N_D = 1.0$. However, at $4K$ is the impurity density close to $N_{D+}/N_D = 0$. This means that an higher gate voltage is needed to create an inversion layer between source and drain of a mosfet. In other words, the threshold voltage increases. On the other hand, the mobility in silicon increases due to the reduction of phonon scattering. Therefore, the drain current can increase in triode and saturation region.

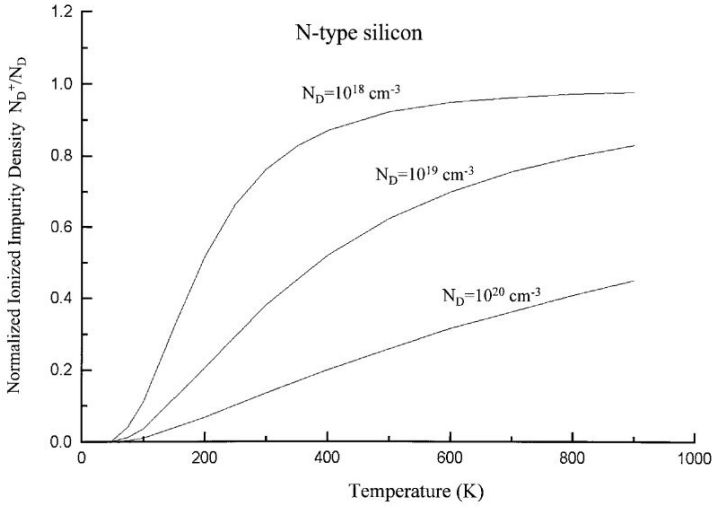


Figure 3.5: Normalized ionized impurity density versus temperature [19]

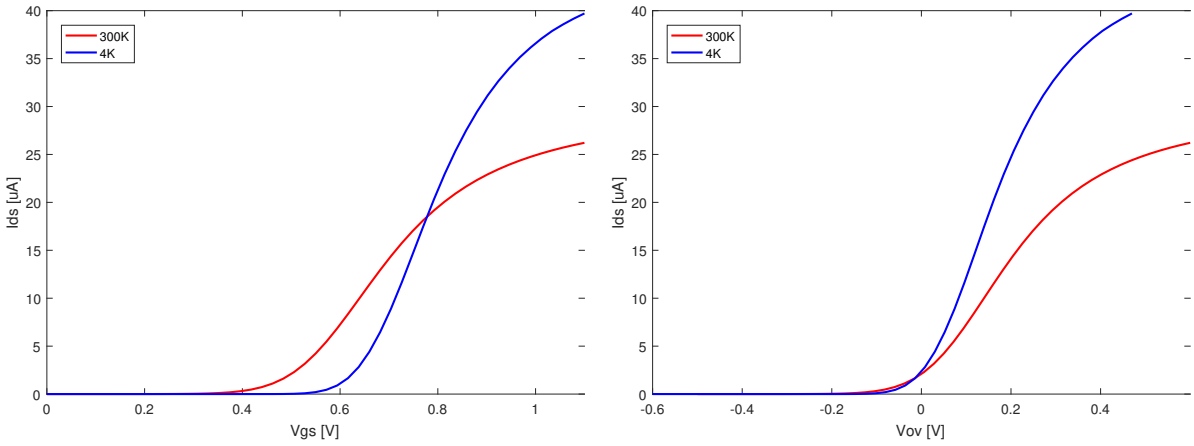
3.11.2. Measurements

Unfortunately, there are no accurate TSMC40 transistor models operating at $4\ K$. However, 4 transistor structures (SS, SL, LS, LL) are measured at room temperature and $4\ K$. The corresponding aspect ratio are listed in table 3.2. The drain current of those structures are measured while the V_{ds} an V_{gs} are swept. This data gives a prediction of the threshold voltage and mobility shifts. The I_d versus V_{gs} and V_{ov} with a fixed V_{ds} for a LS structure are plotted in figures 3.6a and 3.6b. The corresponding threshold voltage shift is $\Delta V_{th,n} = 130\ mV$ and the mobility is increased by a factor 1.7. The mobility increase in defined as the ratio of the currents at room temperature and $4\ K$ at a fixed overdrive voltage. This data will be used for the design of the pass device.

Table 3.2: List of specifications

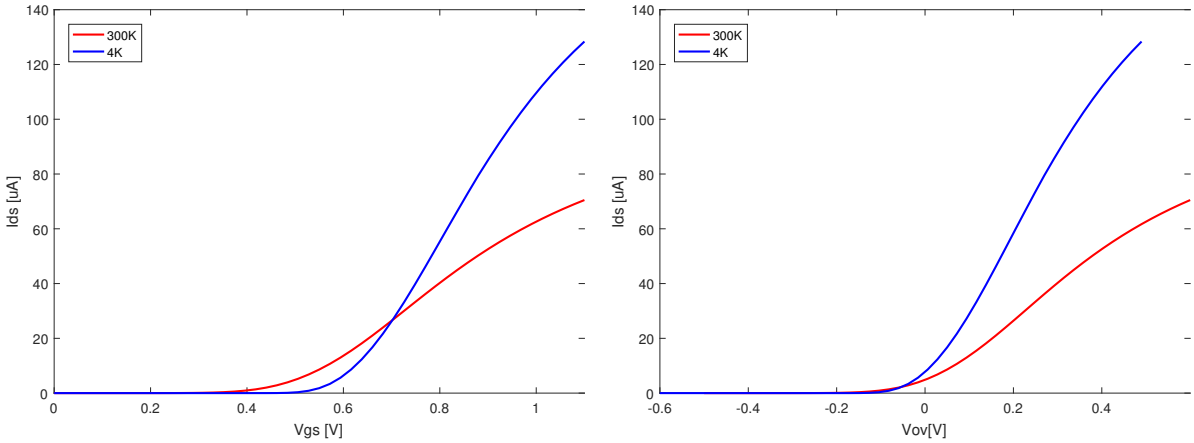
Structure	Aspect ratio
SS	$0.12\ \mu m/0.04\ \mu m$
SL	$0.12\ \mu m/0.4\ \mu m$
LS	$1.2\ \mu m/0.04\ \mu m$
LL	$1.2\ \mu m/0.4\ \mu m$

The I_d versus V_{gs} and V_{ov} with a fixed V_{ds} for a LL structure are plotted in figures 3.7a and 3.7b. The corresponding threshold voltage shift is $\Delta V_{th,n} = 110\ mV$ and the mobility is increased by a factor 2.1. This data will be used for the design of the first and second stage.



(a) I_{ds} vs. V_{gs}, $V_{ds} = 50\ mV$ and $W/L = 1.2\ \mu/0.04\ \mu m$ (b) I_{ds} vs. V_{ov}, $V_{ds} = 50\ mV$ and $W/L = 1.2\ \mu/0.04\ \mu m$

Figure 3.6



(a) I_{ds} vs. V_{gs}, $V_{ds} = 200\ mV$ and $W/L = 1.2\ \mu/0.4\ \mu m$ (b) I_{ds} vs. V_{ov}, $V_{ds} = 200\ mV$ and $W/L = 1.2\ \mu/0.4\ \mu m$

Figure 3.7

4

Design Process

This chapter starts with the choice of the architecture. The advantages and disadvantages of different typologies will be discussed and the design specification will be given. The next section goes about the design of the chosen architecture, it includes a pole-zero analysis, the design of all stage and simulation results. This chapter ends with the layout of the LDO circuit.

4.1. Specifications

The specification are shown in table 4.1. A description of each specification is given in chapter 3.

Table 4.1: List of specifications

Specification	**Symbol**	**Value**
1. Technology		TSMC40
2. Output voltage	V_{out}	$1.1\ V$
3. Output current	I_{out}	$0 - 50\ mA$
4. Output capacitance	C_{out}	$0 - 10\ pF$
5. Load regulation	$\Delta V_{out}/\Delta I_{out}$	$20\ mV/A$
6. Line regulation	$\Delta V_{out}/\Delta V_{in}$	$4\ mV/V$
7. PSRR	$\Delta V_{out}/\Delta V_{in}$	$-48\ dB$
8. Open loop bandwidth	BW_{ol}	$> 1MHz$
9. Integrated Noise ($BW = 1\ GHz$)	$V_{n,rms}$	$1\ mV_{rms}$
10. Efficiency	η_{pwr}	95%
11. Area	A	$1\ mm^2$

4.2. Architecture choice

The main difference between a dominant pole and a C-free structure is the use of the large external capacitor. A dominant pole structure uses a large external capacitor to regulate the output voltage. This capacitor limits the bandwidth and the LDO is therefore relatively slow. The bandwidth in a C-free structure is usually larger. It is limited by the smaller Miller capacitor and the LDO is therefore faster with respect to dominant pole structures. The output voltage is thus regulated via the fast loop of the LDO. Also digital LDOs usually use a large external output capacitor to regulate the output voltage.

Some discrete LDOs have been proved to operate at $4\ K$ [5]. However, fully on-chip cryogenic CMOS LDO's have not been published yet. The challenge is to design a fully on-chip LDO which operates at room temperature and $4\ K$, since CMOS transistors operate differently at those two temperatures [20]. This on-chip LDO can be placed close to other CMOS circuits to provide a stable and regulated voltage. Therefore, a C-free architecture is chosen, because dominant pole structures need a large off-chip capacitance. Although, off-chip capacitors are not so expensive, they may limit the reliability,

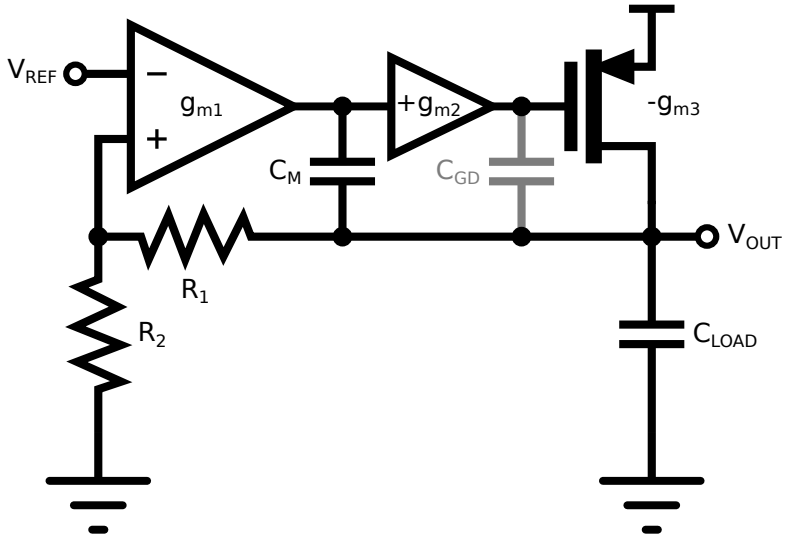


Figure 4.1: C-free architecture

the size and the level of integration of the quantum computer controller and hence it it's scalability.

However, choosing for the C-free architecture also gives issues in terms of stability, over- and undershoot. A load transient is difficult to suppress because there is no large capacitor. A large unity gain frequency can easily solve this problem, because this decreases the response time of the system. Usually a multistage driver can provide this large bandwidth, but it requires good pole and zero placement. Non-dominant poles should be placed far away from the unity gain frequency in order to get sufficient phase margin. Nevertheless, a multistage nested Miller architecture like figure 4.1 is chosen, because it does not require a large external capacitor and it is already proven that this structure works at room temperature [21].

4.3. Design of the architecture

Basically, the chosen architecture is a three stage amplifier with nested Miller compensation. The third stage is the pass device of the LDO and the first and second stage is the driver, which drives the pass device. The design procedure of the pass device is described in section 4.4. The design of the third stage is important, because it determines many of the system choices. It is therefore useful to start with the design of the third stage. Many internal specifications, such as gain and bandwidth, will follow from the third stage design.

4.3.1. Poles and zeros

This architecture in open loop has three main poles, 1 dominant pole, ω_{P0}, and 2 non-dominant ones, ω_{P1} and ω_{P2}. It is a challenge to place these pole such that the circuit is stable. This means that the two left half plane non-dominant poles should be placed far enough from the unity gain frequency. First, the location of all three poles has to be known. The unity gain frequency is defined as the product of the loop gain (A_0) and the dominant pole (ω_{P0}):

$$\omega_{UGF} = A_0 \cdot \omega_{P0} = g_{m1} r_{o1} g_{m2} r_{o2} g_{m3} r_{o3} \cdot \frac{1}{r_{o1} C_m (g_{m2} r_{o2} g_{m3} r_{o3} + 1)} \approx \frac{g_{m1}}{C_m} \tag{4.1}$$

where g_m and r_o are the transconductance and output impedance of each stage and C_m the Miller capacitance. The equation hold if $g_{m2} r_{o2} g_{m3} r_{o3} >> 1$. The first non-dominant pole, located at the output of the second stage is computed as:

$$\begin{aligned} P_{non1} &= \frac{g_{m2} r_{o2} g_{m3} r_{o3}}{r_{o2}[C_{gd}(g_{m3} r_{o3} + 1) + C_2]} \approx \frac{g_{m2}}{C_{gd}} \\ & C_{gd}(g_{m3} r_{o3} + 1) >> C_2 \\ & g_{m3} r_{o3} >> 1 \end{aligned} \tag{4.2}$$

where C_{gd} is the gate to drain capacitance of the pass device and C_2 is the output capacitance of the second stage. The second non dominant pole, located at the output of the LDO is computed as:

$$P_{non2} = \frac{g_{m3} C_{gd}}{C_2 C_3} \tag{4.3}$$

where C_3 the output capacitance of the LDO is. The calculation of the second non dominant pole is done in Matlab, the script is documented in appendix B. From equation 4.2 and 4.3, it is clearly visible that the gate to drain capacitance of the pass device acts like a Miller capacitance, it splits the poles.

To achieve a stable circuit, a phase margin of $60°$ is often required [21]. Also this requirement avoids ringing and speeds up the settling. This means that all poles are at least separated by a factor 2. Thus:

$$P_{non2} = 2P_{non1} = 4\omega_{UGF} \Rightarrow \frac{g_{m3} C_{gd}}{C_2 C_3} = 2\frac{g_{m2}}{C_{gd}} = 4\frac{g_{m1}}{C_m} \tag{4.4}$$

Another requirement is that right half plane zeros are located far away from the unity gain frequency. The location can be calculated when an AC short is applied to the output of the LDO. The most important zero is located at

$$Z_1 = \frac{g_{m3}}{C_{gd}} \tag{4.5}$$

This means that g_{m3} should be at least two times larger than g_{m2} in order to get enough phase margin.

4.3.2. Root locus

The design of the LDO would be a lot easier when the transconductances and capacitors do not change for different load conditions. However, it is not the case, because g_{m3}, C_{gd}, C_2 and C_3 are load depended. When the load current increases, g_{m3} will increase substantially and the two non dominant poles will move away from each other. On the other hand, when g_{m3} becomes small, the pole will run into each other and become complex, which deteriorates the stability of the system. The root locus is illustrated in figure 4.2. This figure describes the root locus under different load conditions. Under heavy of medium load conditions the non-dominant poles are well split. Under light load condition, the poles run in each other and become complex. Under ultra-light conditions the complex poles move to the right half plane, this occurs when g_{m3} is smaller than g_{m2}. This circuit is unstable and will not settle well. Therefore, the minimum biasing current through the pass device should generate enough transconductance.

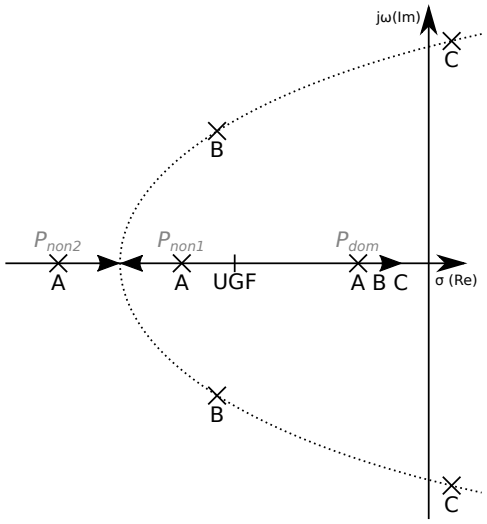


Figure 4.2: Pole plane, A: Heavy/medium load, B: Light load, C: Ultra-light load

4.3.3. Sizing of the loop

Since the locations of the poles are known, the transconductances and output impedances can now be translated into realistic values. As mentioned before, the focus is on designing the first and second stage, because the design of the pass device is fixed. From this design, the exact locating of the second non-dominant pole is known. For the minimum load current, this pole is at $P_{non2} \approx 8.0\ MHz$. The pole limits the maximum achievable bandwidth. However, this pole will move to higher frequencies if the bias current

for the pass device is increased.

The Miller capacitance should be a well defined, since it determines the bandwidth. If this capacitor is too small, the parasitic capacitance do play a roll. If this capacitor is too large, it is a waste of area and power. From equation 4.4 it is clearly visible if $C_m = C_{gd}$ that $g_{m2} = 2g_{m1}$. This means that transconductance of the second stage is twice the transconductance of the first stage when the Miller capacitance is chosen the same as the gate to drain capacitance of the pass device. To achieve a 95% efficiency, the total maximum quiescent current is about $100\ \mu A$. From section 4.4 we see that the third stage already uses $30\ \mu A$ of current, so there is $70\ \mu A$ left. The maximum gain bandwidth of the system depends on the available transconductance, which depends on the power consumption. Therefore, it is wise to maximize the bandwidth taking in account the limited power budget. With this power budget it for sure possible to achieve a transconductance for the first stage of $g_{m1} = 100\ \mu S$. Because for a fixed overdrive voltage of $V_{ov} = 200\ mV$, the transconductance divided by the current can be $g_m/I_d = 10$. Consequently, the transconductance of the second stage $g_{m2} = 2g_{m1} = 200\ \mu S$. In order to maximize the gain bandwidth, the transconductances may be increased, if the efficiency is still higher than 95%.

In order to find the gain of the driver, the load and line regulation of the system are simulated. The used circuit is illustrated in figure 4.3, an ideal amplifier and the designed pass device. Increasing the voltage gain of the amplifier will lead to a better load and line regulation. To meet specifications 5 and 6 in table 4.1, the gain of the amplifier has to be larger than $66\ dB$. This will lead to the following equation

$$g_{m1}r_{o1}g_{m2}r_{o2} = 66dB \equiv 2000 \tag{4.6}$$

Usually in a multistage amplifier design the first stage has high gain in order to keep the noise at the output low. Telescopic, Folded Cascode and Pseudo differential amplifiers can easily have $40-50\ dB$ of gain, without gain boosting technique. This means that the output impedance of the first stage is about $r_{o1} = 1.8M\ \Omega$. The gain of the non-inverting second stage can easily be about $20\ dB$, consequently $r_{o2} = 50\ k\Omega$.

4.4. Pass device

Since pass devices come in different configurations, it is useful to find out what the advantages and disadvantages are. An NMOS pass device is easier to stabilize, but requires a gate voltages higher than the source voltage. The gate voltage may exceed the input voltage for a low drop-out voltage. On the other hand, a PMOS pass device is more difficult to stabilize, but requires a gate voltage lower than the source voltage. Most LDO circuits are built with a PMOS pass device, because the required gate voltage is between V_{in} and GND, and a level shifter is not required. So in therms of simplicity, a PMOS pass device is chosen.

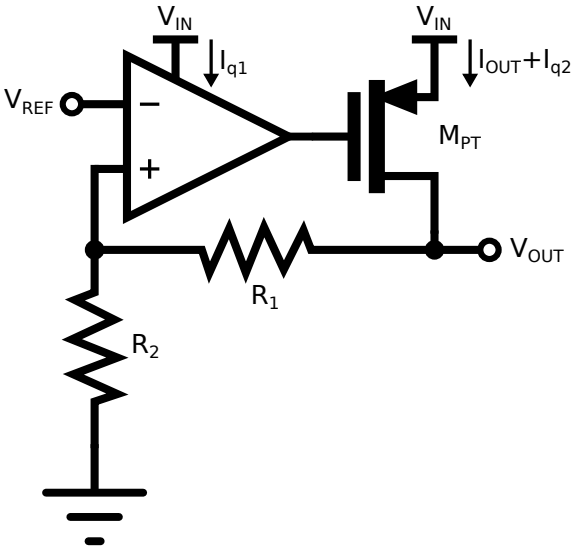


Figure 4.3: Current flows in a LDO

4.4.1. Efficiency

The efficiency of the LDO is mostly determined by the on resistance of the pass device and the quiescent current of the LDO. The on resistance of a transistor is defined as $R_{on} = \partial V_{ds}/\partial I_{ds}$, where V_{ds} and I_{ds} are the drain source voltage and the drain source current, respectively. The efficiency of the LDO is defined as

$$\eta_{LDO} = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}(I_q + I_{out})} \tag{4.7}$$

Where V_{out} and I_{out} are the output voltage and current and I_q is the quiescent current, like in figure 4.3. The output voltage is fixed to $1.1V$, the V_{dd} of the TSMC40 process. Since I_{ds} is the output current of the LDO, only V_{in} can be decreased to increase the efficiency of the LDO. When the input voltage is set to $V_{in} = 1.15\ V$, the V_{ds} of the pass device is only $50\ mV$ and the voltage efficiency is $95,7\%$. A lower on-resistance has drawbacks unfortunately, for example a lower PSRR. This drawback can be overcome by increasing the loop gain of the circuit.

4.4.2. Transistor types

The TSMC40 process offers three types of PMOS transistors, the low threshold voltage (LVT), standard threshold voltage (SVT) and the high threshold voltage (HVT) transistors, due to the different substrate doping concentrations [22]. Since the pass device has to conduct the output current, the type of transistor and sizing of the pass device are important. First, the voltage swing on the gate has to be known. In this stage of design, there is an assumption made about the design of the output stage of the driver. The most minimalistic output stage will probably look like illustrated in figure 4.4, an NMOS transistor (M_{N1}) cascoded with a PMOS transistor (M_{P1}). This output stage ensures a high swing and therefore the aspect ratio of the pass device can be designed smaller.

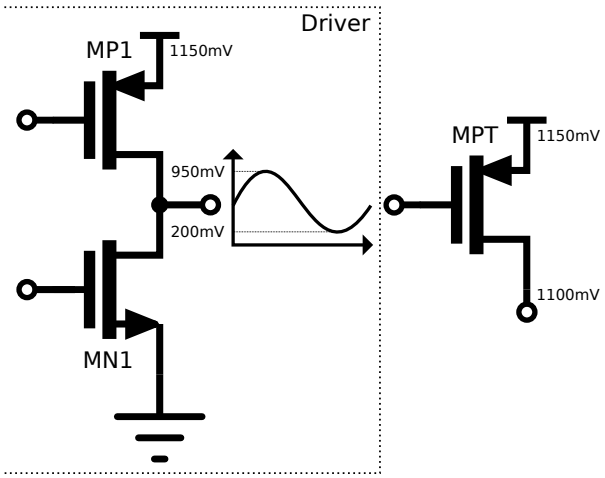


Figure 4.4: Output stage of the driver and pass device MPT

To keep both transistors M_{N1} and M_{P1} in saturation, a V_{ds} of $200\ mV$ is required for those transistors. Therefore, the voltage swing on the gate of the pass device is ranging between $200\ mV$ and $950\ mV$ and the maximum gate source voltage of the pass device is therefore $950\ mV$. Since the V_{ds} of the pass device is set to $50\ mV$, the pass device will operate in the triode region, when the maximum gate source voltage is applied. For a PMOS transistor in triode region, the drain source current is defined as [23]

$$I_{ds} = \mu_p C_{ox} \frac{W}{L}\left((V_{gs} - V_{th,p})V_{ds} - \frac{V_{ds}^2}{2}\right) \tag{4.8}$$

The drain source current heavily depends on the aspect ratio and the threshold voltage of the device. To keep the area of the LDO as small as possible, it is wise to set the length of the device to minimum, i.e. $40\ nm$. In order to find the total width of the pass device, a small simulation is done with the three types of the device. Each type is simulated in the same conditions; $V_{ds} = 50\ mV$, $V_{gs} = 950\ mV$ and $I_{ds} = 55\ mA$. Table 4.2 shows the simulated threshold voltages and the corresponding aspect ratio for the different types of transistor. In this table, it is clearly visible that the required aspect ratio increases when the threshold voltage increases. Again, in order the keep the area of the LDO as small as possible, it is wise to choose for a LVT transistor. Moreover a smaller device has less gate capacitance, with helps to stabilize the loop gain. Nevertheless, a LVT transistor has more leakage current compared to a SVT or HVT transistor.

Table 4.2: Size and threshold voltage of different types of PMOS transistors, $V_{ds} = 50\ mV$, $I_{ds} = 55\ mA$, $V_{gs} = 950\ mV$ and $T = 300\ K$

Types	$\mathbf{V_{th,p}}$	Aspect Ratio (W/L)
LVT	$565\ mV$	45000
SVT	$615\ mV$	54000
HVT	$745\ mV$	90300

At this moment, there are no models for the TSMC40 transistors operating at $4K$, so it is useful to overdesign the pass device. From figures 3.6a and 3.6b, it is stated that the threshold voltage increases with $130\ mV$ when the transistor is cooled down to $4\ K$. It is necessary to compensate for this behaviour, because an increase in the threshold voltage will lead to a decrease in maximum output current. At this

stage of the design, an LVT transistor with an aspect ratio of an HVT transistor (90300) will be used, to compensate for the threshold voltage increase. From the figures, it is also stated that the mobility increases with 2.1 times. The mobility increase works as an advantage, because it will increase the maximum output current when the same gate source voltage is applied.

4.4.3. Biasing

Nevertheless there is leakage current, the minimum biasing current of the pass device. This current will flow through a resistor pair like in figure 4.5. This resistor pair is also needed to scale the reference voltage. When the minimum overdrive voltage of $200\ mV$ is applied, the pass device is in sub-threshold region and the leakage current is $26\ \mu A$. Consequently, $R_1 + R_2 < V_{out}/I_{leak} = 42.3\ k\Omega$. The corresponding minimum transconductance is $g_{m3} = 577\ \mu S$, which is larger than the required $400\ \mu S$. Besides current biasing, the resistor pair also fixes the output voltage, by scaling the reference voltage. This voltage is defined as

$$V_{out} = \frac{R_1 + R_2}{R_2} V_{ref} \tag{4.9}$$

The value of the reference voltage depends on the design of the driver and the available bandgap references. In section 4.5 the reference voltage is set to $300\ mV$. Consequently, R_1 is set to $30.71\ k\Omega$ and R_2 is set to $11.52\ k\Omega$. It is stated that the leakage current at $4K$ will decrease compared to room temperature, so this pass device is still functional at $4\ K$ [24].

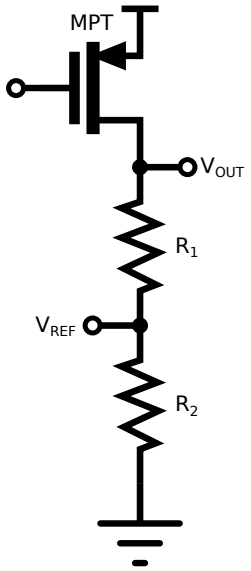


Figure 4.5: Pass device MPT with feedback resistors

4.5. Driver

The pass device is driven by an amplifier which has good gain and bandwidth properties. The driver for this application consists of two stages to ensure high gain and a large voltage swing at the output. Usually, the first stage of an amplifier has high gain to ensure high noise performance. However the second stage acts like a buffer, it ensures high output voltage swing.

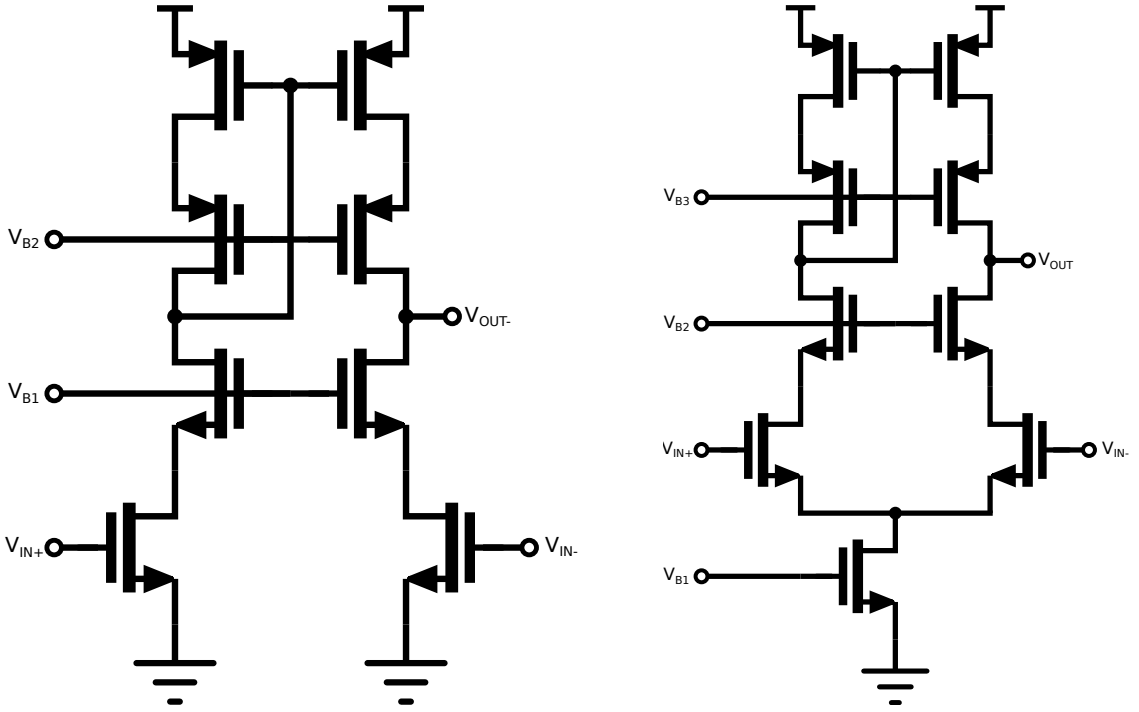
4.5.1. First stage

A high gain driver stage improves the line and load regulation of the system. Usually in the multistage amplifier design, the first stage is designed with respect to noise [25]. Therefore, the gain in the first stage is high and the gain in the other stages are lower. Otherwise the noise at the output of the first stage will be amplified too much. The gain in this stage is about $A_0 = 40 - 50\ dB$, with a transconductance of $g_{m1} = 100\ \mu S$ and a current consumption of $I_{pwr} = 30\ \mu A$. The three most common amplifier topologies are Telescopic, Folded cascode and pseudo differential. All topologies have good gain capabilities [26], but some are not suitable for this LDO application.

Headroom

One of the simplest amplifiers is a Pseudo-differential amplifier consisting of two single ended amplifiers, like in figure 4.6a. This amplifier combines good gain capability, low power, high speed with high voltage output swing. Furthermore, it is easy to design and the biasing is not too complex. However this topology has a poor common mode rejection. A telescopic amplifier, figure 4.6b, has even better gain capabilities, because of the extra cascode. It is a low power, high speed and fully differential topology. Nevertheless, it has a lower voltage output swing because of the same extra cascode. Another commonly used amplifier is a Folded Cascode, like in figure 4.7a. This has the advantage of a higher voltage output swing, compared to a telescopic topology. However, the power consumption is twice as high compared to the Pseudo-differential and Telescopic amplifiers and there is a second pole located at $g_m/2C_{gs}$ which is due to the folding node.

One of the criteria for the first stage amplifier is the voltage headroom at the output. The headroom for these three amplifiers is $V_{GS} + 2 \cdot V_{DS}$ for the Pseudo-differential and Folded Cascode amplifiers, and



(a) Pseudo-differential amplifier architecture

(b) Telescopic amplifier architecture

Figure 4.6

$V_{GS} + 3 \cdot V_{DS}$ for the Telescopic amplifier. The V_{DD} for this LDO circuit is set to $1.15V$. A useful V_{GS} for this process at room temperature is about $500mV$ with a V_{DS} of $200mV$. The behaviour of CMOS transistor in saturation at $4K$ shows an increase of threshold voltage of $110mV$. From this data, it is obvious that one V_{GS} and three V_{DS} does not fit in one V_{DD}. Increasing the supply voltage is a solution, but lifetime of the transistors due to reliability and the overall efficiency will decrease.

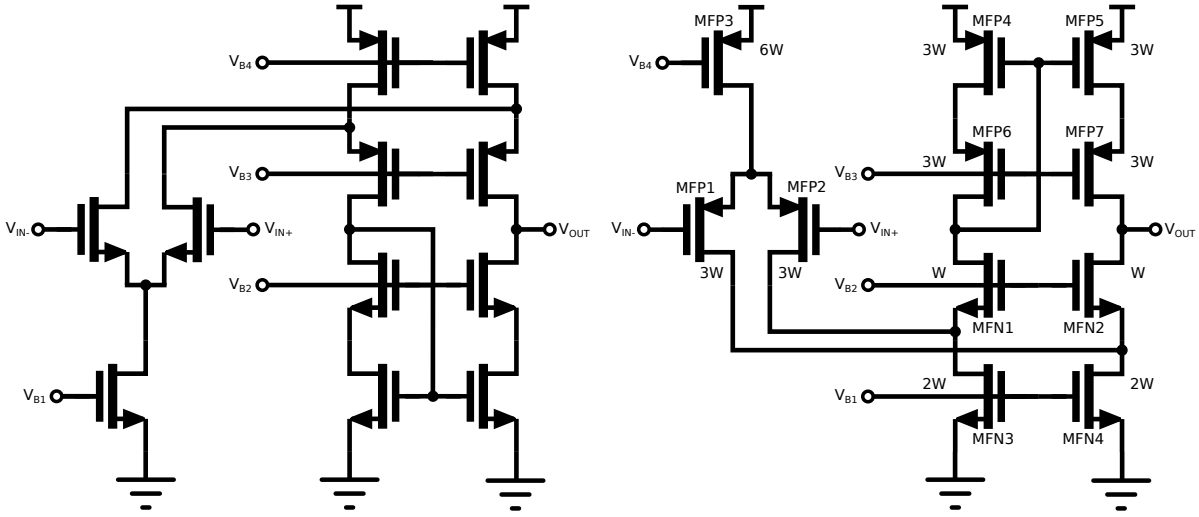
Common mode voltage

The reference voltage is connected to the negative input of the first stage amplifier. This voltage is basically fixed in a LDO design. However, this LDO application will operate at room temperature and at $4K$. The biasing voltages at these two temperatures are different. However, the transconductance of this stage has to be roughly the same. Therefore it is useful if this reference voltage is tuneable without changing the biasing currents through the amplifier. Therefore, a Pseudo-diffential amplifier is not suitable, because the common mode rejection ratio too poor [27]. At the end a Folded Cascode is the most suitable amplifier for this LDO application.

Folded Cascode Design

The Folded Cascode amplifier comes in two different versions, a NMOS and a PMOS input transistor based. The decision between those two versions could be made based on the available reference. The reference voltage comes from a bandgap reference circuit, which has an output voltage of about $500mV$, operating at $4K$ [28]. Scaling down this voltage is easier because it does not require active components, compared to scaling up the bandgap voltage. Based on the reference voltage, there is a preference to use a PMOS input transistor. The disadvantage is that the second pole is closer to the unity gain frequency, since the gate to source capacitances are higher.

The first step to design this Folded Cascode is to apply relative aspect ratios to the transistors. The length of all transistor is the same and the ratio of the width of PMOS compared to NMOS is set to $3:1$, with respect to the reference transistor $MFN1$. The differences in mobility is compensated with this ratio of widths. The current through the input transistors is at the same as the current through the two output branches, this means $W_{MFP1} = W_{MFP2} = W_{MFP4} = W_{MFP5}$. The circuit with the relative aspect ratios



(a) NMOS based Folded Cascode architecture (b) PMOS based Folded Cascode architecture

Figure 4.7

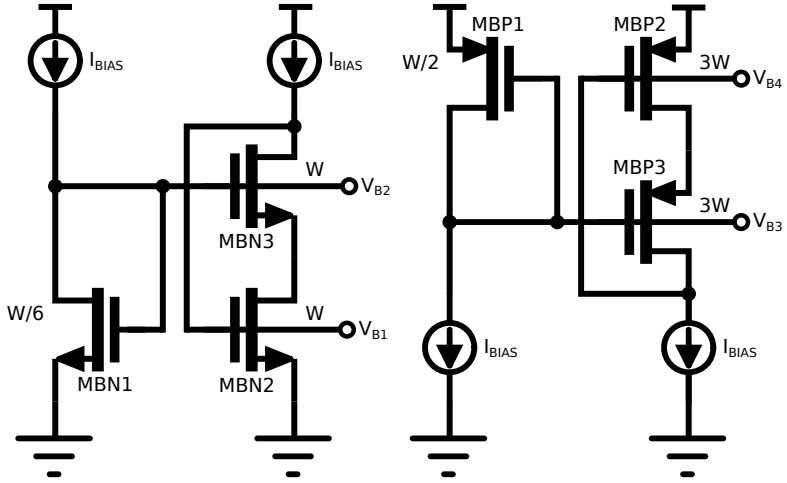


Figure 4.8: Biasing circuit for Folded Cascode amplifier

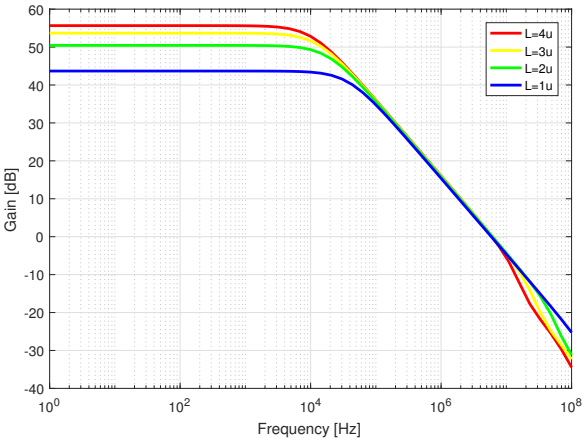
is shown in figure 4.7b. The biasing circuit which will be used to bias the Folded Cascode is shown in figure 4.8. The ratio of the width of $MBN1$ compared to $MBN2$ is set to 1:6. Under this condition is $V_{B2} = V_{gs,MBN3} + V_{ds,MBN2}$ and the biasing currents I_{BIAS} are the same. The gain of this stage depends on the transconductance and the output impedance. The output impedance is defined as

$$\begin{aligned} &R_{OUT} = g_{m,MFN2} r_{o,MFN2} r_{o,MFN4} // g_{m,MFP7} r_{o,MFP7} r_{o,MFP5} \propto \frac{1}{\lambda I_d} \\ &g_{m,MFN2} r_{o,MFN2} >> 1 \\ &g_{m,MFN2} r_{o,MFN2} r_{o,MFN4} >> r_{o,MFN4} \end{aligned} \tag{4.10}$$

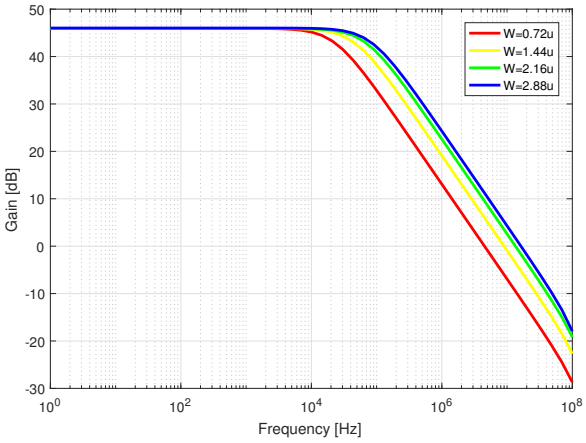
Where λ is the channel length modulation factor [29]. The tranconductance of transistor $MFP1$ is defined as

$$g_{m,MFP1} = \frac{2I_d}{V_{gs} - V_{th,p}} \propto I_d \tag{4.11}$$

assuming it is in strong inversion. Therefore the small signal gain of the Folded Cascode is defined as the product of the transconductance and the output impedance



(a) Small signal gain of the first stage, loaded with a $1pF$ capacitor



(b) Small signal gain of the first stage, loaded with a $1pF$ capacitor

Figure 4.9

$$A_0 = g_{m,MFP1} R_{OUT} \propto \frac{1}{\lambda} \propto L \tag{4.12}$$

Increasing the channel length will result in an increase of the small signal gain, for a fixed aspect ratio and thus a fixed overdrive voltage. Nevertheless, the second pole of the folded cascode moves to lower frequencies because of the larger gate to source capacitance. This is clearly visible in figure 4.9a. A channel length of $L = 1.2\mu m$ is already sufficient for a small signal gain of $A_0 = 45dB$, which meets the requirements. Although an increase of the bias current will not result in an increase of the gain, but the bandwidth does. Therefore width and the biasing current are increased to ensure the transconductance of this stage is $g_{m1} = 100\mu S$. A width of $W = 2.16u$ for the reference transistor is already sufficient. The corresponding current consumption excluding to biasing is $I_{pwr} = 30.1\mu A$.

The reference voltage in the previous simulations is set to $V_{REF} = 450mV$ to ensure that $V_{ds,MFP3} > 200mV$. This holds operating at room temperature. At $4K$ the threshold voltage in increased with $130mV$. To compensate for that behaviour, the reference voltage is set to $300mV$. This change will not influence to previous room temperature simulations.

4.5.2. Second stage

This buffer stage ensures a high voltage swing at the output of the driver, since the output swing of the first stage is only $350mV$. Another requirement is the non-inverting property, otherwise the circuit is unstable. At least, the transconductance has to be $200\mu S$, the output impedance $50k\Omega$ and the current consumption around $40\mu A$. The simplest non-inverting amplifier is shown in figures 4.10, it consist of two inverting branches. It is proven that this architecture is useful and effective [30] [31] [32].

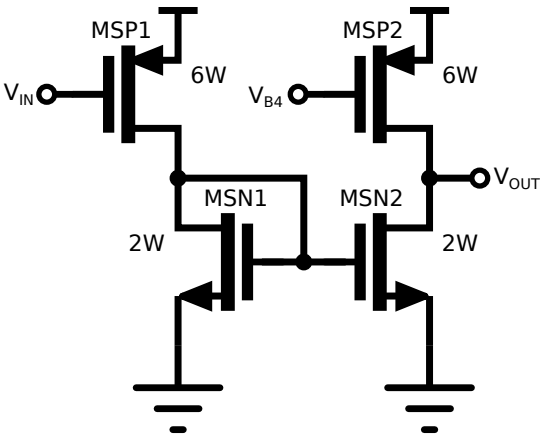
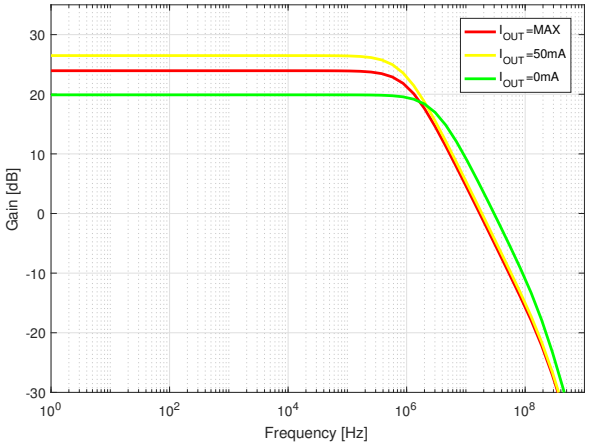
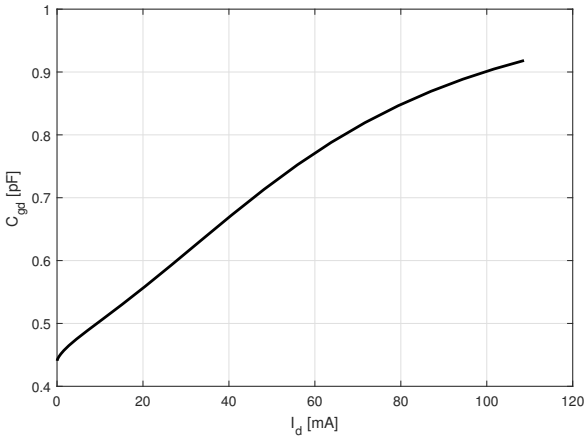


Figure 4.10: Non-inverting architecture

For matching purposes with the first stage, the length of all transistors of the second stage is set to $L = 1.2\mu m$. However, the transconductance of this stage has to be twice as high of the first stage. Therefore the width of transistor $MSN1$ is twice the width of reference transistor $MFN1$. The small signal gain of this stage is defined as



(a) Small signal gain of the second stage, loaded with the pass device



(b) Gate drain capacitance versus the drain current of the pass device

Figure 4.11

$$A_0 = \frac{g_{m,MSP1} g_{m,MSN2}}{g_{m,MSN1}} r_{o,MSN2} // r_{o,MSP2}$$
$$1/r_{o,MSP1} + 1/r_{o,MSN1} >> g_{m,MSN1} \tag{4.13}$$

This stage consist of two poles, where the second pole is defined as

$$\omega_{p2} = \frac{g_{m,MSN1}}{2C_{gs,MSN1}} \tag{4.14}$$

The width of transistor $MSN2$ is kept the same as transistor $MSN1$ for matching purposes. Moreover, an increase of the width of transistor $MSN2$ would result in a second pole which is closer to the unity gain frequency. Therefore, the current in those two braches are the same. The transfer curve for different load conditions is plotted in figure 4.11a. The current consumption for this stage is about $37.8\mu A$ with a corresponding transconductance of $200\mu S$.

4.6. Miller compensation

The Miller capacitance ensures sufficient pole splitting and therefore a stable circuit. In section 4.3.3 the Miller capacitance is assumed to be the same as the gate to drain capacitance of the pass device. However this gate to drain capacitance changes for different load conditions, as plotted in figure 4.11b. Holes are attracted to the gate when the gate to source voltage increases and the channel becomes conducting. Hence, the gate to drain capacitance becomes larger. To be on the safe side, the nominal Miller capacitance is set to $1.75pF$. It is about twice the gate to drain capacitance of the pass device, therefore the bandwidth is two times less. Unfortunately it is uncertain how the poles and zeros of the LDO system will move when the circuit is cooled down from room temperature to $4K$. Therefore, an extra Miller capacitance DAC will be added parallel to the nominal Miller capacitance in order to control the bandwidth of the system. A CDAC with PMOS switches will be used, since the output voltage of the LDO system is a stable $1.1V$.

The binary CDAC has a resolution of $250fF$ and the total Miller capacitance is $17.5pF$, ten times the nominal value. Nevertheless, the capacitor in series with a switch creates a zero due to the on-resistance of the switch. The location of this zero created by a capacitor and a transistor in triode region is defined as

$$\omega_z = \frac{1}{R_{on,MCPn} C_n} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th}) C_n} \tag{4.15}$$

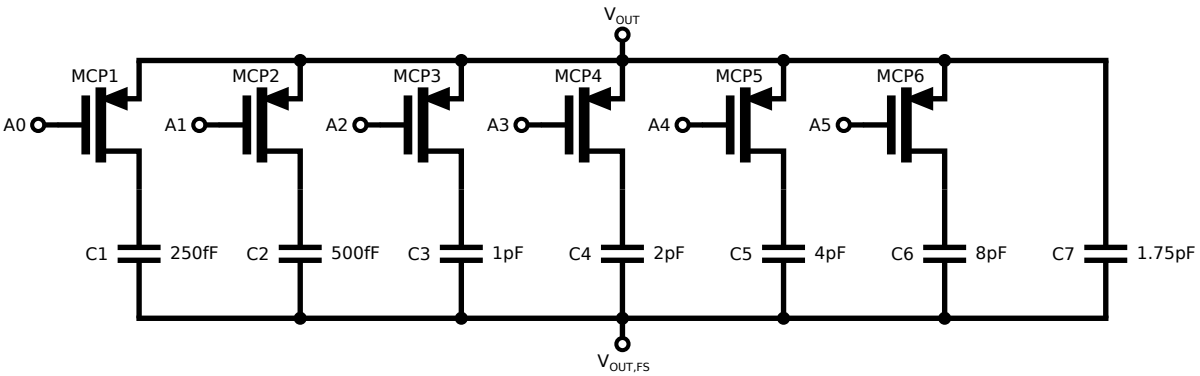


Figure 4.12: Miller capacitor DAC parallel to nominal Miller capacitance C7

Therefore, the switch transistors have to be wide enough in order to lower the on resistance. Increasing the length from minimum to $L = 100\ nm$ will result in a lower on-resistance because the threshold voltage drops substantively, due to the reverse short channel effect (RSCE) [33]. The width of each transistor scales with the value of the capacitor for easy layout purposes. In other words, the ratio between the width of $MCPn$ transistor to the value of C_n capacitor is kept the same. Moreover, the introduced zeros are at the same frequency. The location is far away from the unity gain frequency.

Table 4.3: Aspect ratios used for the Miller DAC

Transistor	Aspect ratio
MCP1	$1.6\ \mu m/0.1\ \mu m$
MCP2	$3.2\ \mu m/0.1\ \mu m$
MCP3	$6.4\ \mu m/0.1\ \mu m$
MCP4	$12.8\ \mu m/0.1\ \mu m$
MCP5	$25.6\ \mu m/0.1\ \mu m$
MCP6	$51.2\ \mu m/0.1\ \mu m$

4.7. Biasing

The blocks of the LDO system need a bias current. The first and second stage are biased with a current, but also the pass device will be biased with an extra current, in order to push the second non-dominant pole to higher frequencies. Most of the time, the biasing current is mirrored from a constant transconductance circuit. Since the room temperature models are pretty accurate, a fixed current could be applied. However, it is uncertain what exactly will happen with the biasing currents at $4K$ and with spread in the resistance in the constant gm circuit. Hence, the current DACs will be added in order to control the biasing currents and transconductances of all stages.

4.7.1. Constant gm cell

A constant transconductance circuit provides a constant g_m over temperature [27] [34], which is useful in this application. A PMOS based constant g_m circuit, like in figure 4.13, is more suitable than an NMOS based, since the g_m of the PMOS input transistors of the first and second stage have to be matched.

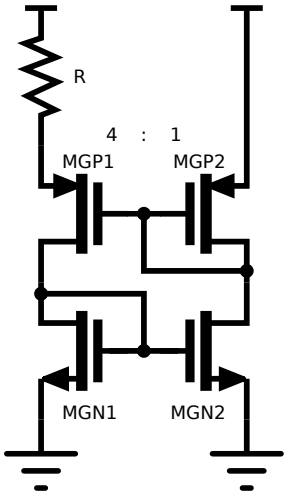


Figure 4.13: Constant g_m circuit

The current in both branches is equal and is defined as

$$I_{MGP2} = \frac{2}{\beta_{MGP2} R^2} \tag{4.16}$$

Where β_{MGP2} is the current factor for transistor $MGP2$. The transconductance of a transistor in saturation region is defined as $g_m = \sqrt{2\beta I}$. Therefore the transconductance of this circuit only depends on the resistance

$$g_{m,MGP2} = \frac{2}{R} \tag{4.17}$$

The transconductances of the first and second stage are $100\ \mu S$ and $200\ \mu S$ respectively. Hence, the resistance is set to $20\ k\Omega$ as a starting point. The current in both branches has to match, therefore the threshold voltages of the transistors have to match. Hence, it is wisely to use large devices. Larger devices match better according to Pelgroms law [35]

$$\sigma_{Vth} \propto 1/\sqrt{WL} \tag{4.18}$$

In order to have 1% matching between the currents, the devices should have a length of $L = 4\ \mu m$. The biasing current is set to $8\ \mu A$, since the biasing current of the first stage is the same. The aspect ratios of the transistors are given in table 4.4.

Table 4.4: Aspect ratios of the constant gm circuit

Transistor	Aspect ratio
MGP1	$23.04\ \mu m/4\ \mu m$
MGP2	$5.76\ \mu m/4\ \mu m$
MGP3	$0.12\ \mu m/4\ \mu m$
MGP4	$5.76\ \mu m/4\ \mu m$
MGP5	$5.76\ \mu m/4\ \mu m$
MGP6	$5.76\ \mu m/0.1\ \mu m$
MGP7	$5.76\ \mu m/0.1\ \mu m$
MGP8	$5.76\ \mu m/4\ \mu m$
MGN1	$1.92\ \mu m/4\ \mu m$
MGN2	$1.92\ \mu m/4\ \mu m$
MGN3	$1.92\ \mu m/0.1\ \mu m$
MGN4	$1.92\ \mu m/0.1\ \mu m$

Nevertheless, this circuit needs a start-up circuit, since there are two stable solutions of this circuit. One of the stable solutions is when the current is zero. Therefore the start-up circuit should enable the 4 transistors conducting current. There are multiple solutions to implement a start-up circuit, depending on the requirements. One of these requirements is the off-current. For this application, the off-current should be lower than a nano ampere. Just a simple diode connected PMOS transistor can be placed between the gates of transistors $MGP1$ and $MGN1$, like in figure 4.14. When the supply is turned on, the diode starts to conducted current, because the gate source voltage is $V_{gs} = V_{dd}$. When the circuit is settled, the diode is in sub-threshold region and will conduct only $I_{leak} = 0.22\ pA$. The leakage of the diode will be smaller at $4\ K$, because the gate to source voltage will be more negative. The start-up time is decreased from $50\ \mu s$ to $2.5\ \mu s$, an improvement of factor 20. This improvement helps starting up the constant transconductance circuit even when the leakage current is small.

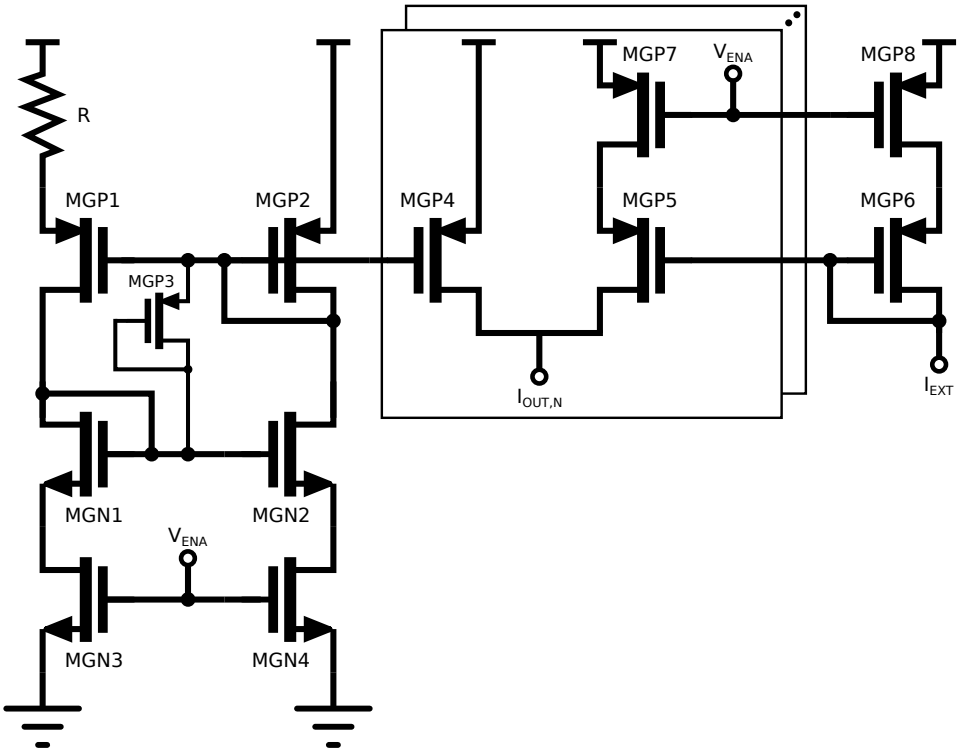


Figure 4.14: Constant g_m circuit, including start-up and external biasing

There is a chance that the constant transconductance circuit will not work at $4K$. For example, the circuit will not start up because of the low leakage current. Therefore back-up biasing circuit is needed, otherwise the whole chip will not work. A single diode connected PMOS transistor will be placed on chip to replace the biasing circuit. The PMOS transistor $MGP6$ will generate a constant V_{gs} which will be used for biasing the current DACs. An enable signal will either enable the constant transconductance

circuit, via switches $MGN3$ and $MGN4$, or the diode connected transistor via switches $MGP7$ and $MGP8$. This is illustrated in figure 4.14. The switches are placed in both branches for matching purposes.

4.7.2. Current DAC

Since there is spread in the resistance, there is spread in transconductance as well. One of the solutions to overcome the spread is to increase the dimensions of the resistor, however area is limited. Since there are no accurate models for CMOS transistors at $4K$, it is wise to come up with a different solution. Also, the spread at $4K$ could be even larger, since the n-poly resistance variation from $300\ K$ at $4\ K$ is 10% [24]. Therefore a current DAC is designed. First, the spread in g_{m1} and g_{m2} has to be known. This is simulated in the 5 different corners. The results show that there is 40% spread in both stages at room temperature. At $4K$, the resistance drops and therefore the total spread is estimated at 44%.

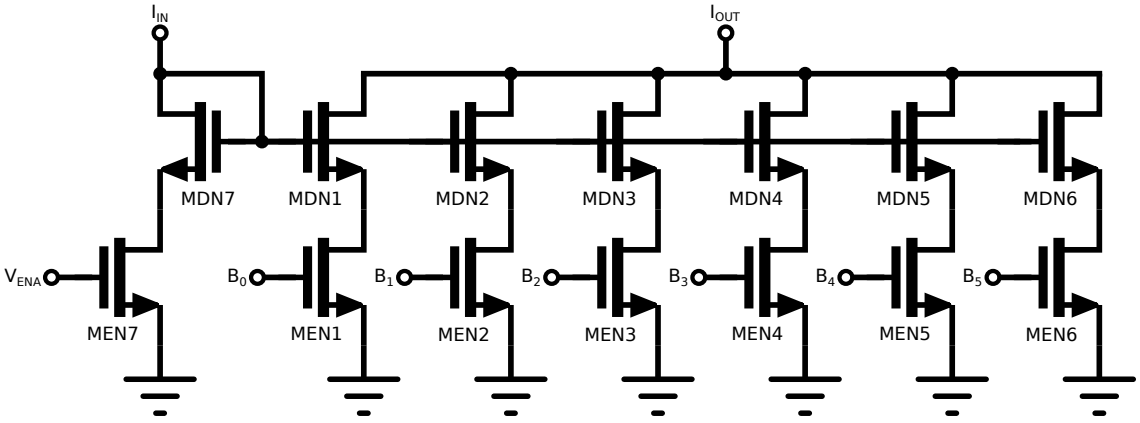


Figure 4.15: Current DAC

The nominal bias current for the first stage is set to $8\mu A$. To overcome the spread, the nominal bias current has to be doubled at least. A resolution of $0.5\mu A$ is already enough to control the transconductance of the first stage. The aspect ratio of the switches are equal to the ones which are used in the constant transconductance circuit. Moreover, this IDAC can be used to bias the second stage and third stage as well. The aspect ratios of the IDAC are placed in table 4.5.

Table 4.5: Aspect ratios of the Current DAC

Transistor	Aspect ratio
MDN1,2,...6	$n \cdot 0.12\mu m/4\mu m$
MEN1,2,...6	$n \cdot 0.12\mu m/0.1\mu m$
MDN7	$1.92\mu m/4\mu m$
MEN7	$1.92\mu m/0.1\mu m$

4.8. Full circuit

Figure 4.16 shows the total circuit including the current and Miller DACs. For testing purposes, the Miller DAC is also used at the output of the LDO. The performance of the LDO can now be measured under different load conditions. The same current DAC is used to bias the first stage and second stage. The same current DAC is also used in the third stage, in order to move the second non-dominant to higher frequencies. The bias current which comes from the IDAC of the second stage is mirrored with a factor 2, since the bias current is twice the nominal current. Moreover, it is useful to control the V_{gs} of the cascoded and non-cascoded transistors of the first stage. In order to do this, three current DACs are needed. The pass device will be biased by the regular current DAC. All control signals from the current DACs, as well as from the Miller capacitance DACs, will be controlled by a Serial Peripheral Interface.

The performance of the total circuit can now be simulated. The following simulations will be executed:

- Load regulation
- Line regulation
- PSRR + noise
- Transient response

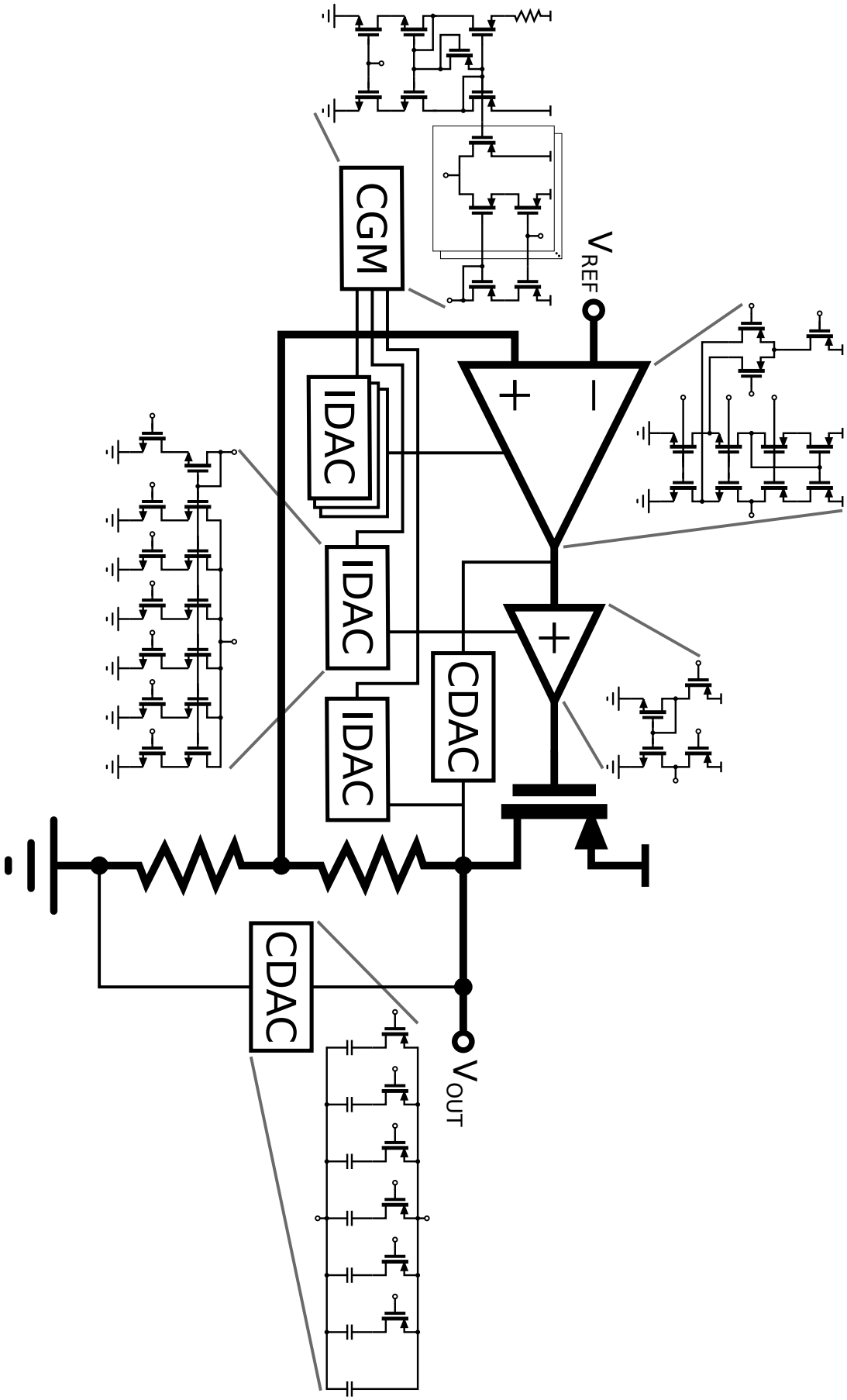


Figure 4.16: Total circuit

4.8.1. Load regulation

The maximum output current of the LDO is set to $50mA$. The maximum shift in output voltage due to the change in output current is $1mV$, consequently $\Delta V_{out}/\Delta I_{out} = 20mV/A$. However, the power transistor is overdesigned with a factor 2. This means that the maximum output current at room temperature is $100mA$. The total shift in output voltage is illustrated in figure 4.17. The overall load regulation from this figure is $\Delta V_{out}/\Delta I_{out} = 8.82mV/A$, which meets specification 5.

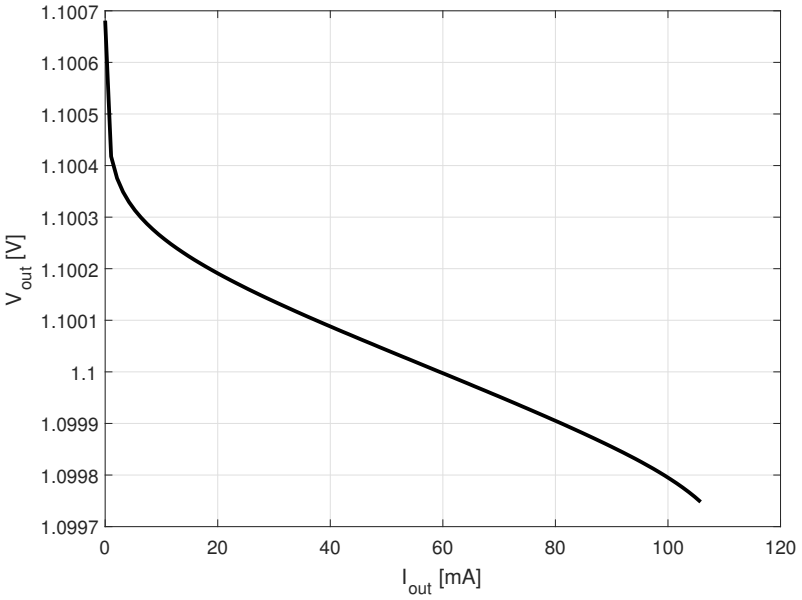


Figure 4.17: V_{out} vs. I_{out}

4.8.2. Line regulation

The line regulation is set to $\Delta V_{out}/\Delta V_{in} = 2mV/V$. The supply voltage for the process is actually $1.1V$. It is possible to increase the supply voltage, but at a certain point the core will break, however this is not visible in figure 4.18. The simulated overall regulation is $\Delta V_{out}/\Delta V_{in} = 1.1mV/V$, which meets specification 6.

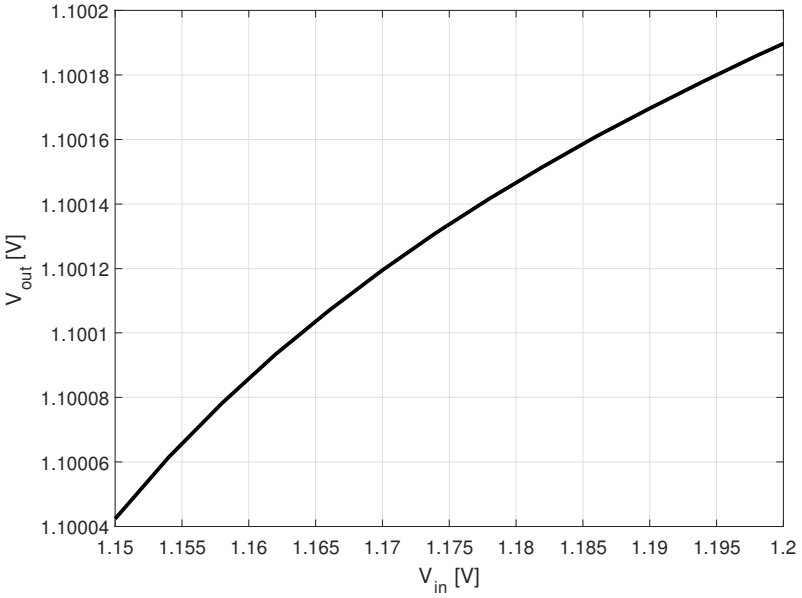


Figure 4.18: V_{out} vs. V_{in}, $I_{out} = 50mA$

4.8.3. PSRR

The PSRR is simulated for different output currents, the results are illustrated in figure 4.19. An small AC signal is applied to the input voltage V_{in} of the LDO. The load capacitance in these simulation is $C_{load} = 10\ pF$. The PSRR strongly depends on the gain of the error amplifier and the output impedance of the pass device. A higher gain results in a better PSRR and vice versa. For $I_{out} = 0mA$ the pass device is in sub-threshold region, however for $I_{out} = 25mA$ and $I_{out} = 50mA$ the device is in triode region. Hence, the PSRR decreases.

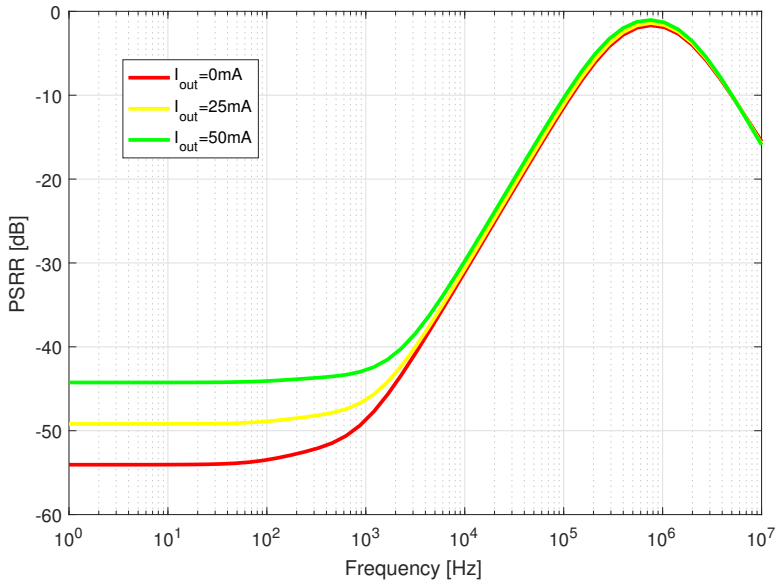


Figure 4.19: PSRR vs. frequency, simulated with $1\mu F$ decoupling capacitance at V_{in}

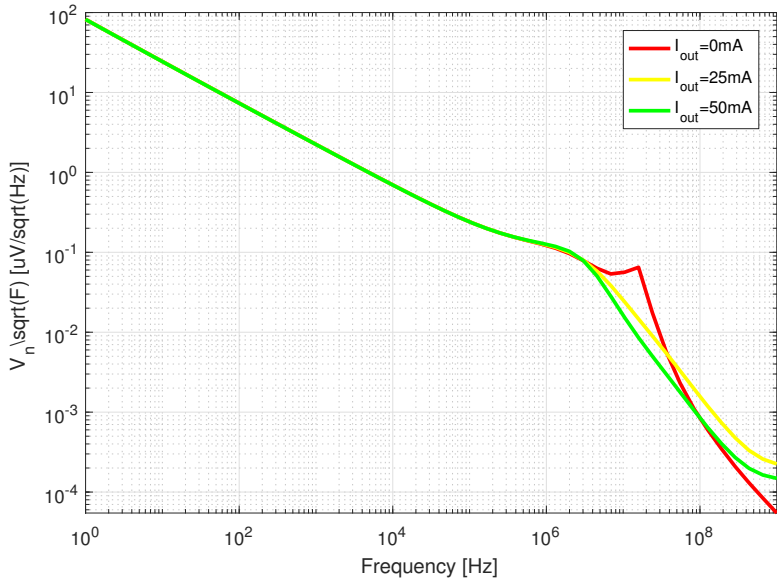


Figure 4.20: V_n vs. frequency, $C_{out} = 10\ pF$

4.8.4. Noise

The noise coming from the circuit should be low enough in order to be able to measure the DC performance. The main noise source are the flicker noise and the thermal. The amount of Flicker noise of a transistor is inverse proportional to the area of the transistor. The integrated output noise over a

bandwidth from $1Hz$ to $1GHz$ therefore should be lower than $V_{n,rms} = 1mV_{rms}$. Noise from frequencies does not count much to the integrated noise, since the Flicker noise is the dominant noise source.
The output noise spectrum for three different output currents is illustrated in figure 4.20. The main noise source is the Flicker noise coming from the NMOS cascode transistors of the first stage $MFN1$ and $MFN2$. These transistors are the smallest transistors of the first stage and the noise is directly amplified by the second and third stage. The simulated integrated noise, for a NPLC of 1 and $I_{out} = 50\ mA$, is $0.29\ mV_{rms}$. The peak in the noise spectrum density, for $I_{out} = 0\ mA$, comes from the low phase margin at that particular frequency. The closed loop bandwidth amplifies this noise at those frequencies [36].

4.8.5. Open loop response

One way to check the stability is via the bode plots, as shown is figure 4.21. The unity gain frequency is $2MHz$ with a minimum phase margin of $72°$. This phase margin is larger than required $60°$, because the Miller capacitance is overdesigned by a factor 2. The complex poles are visible for $I_{out} = 0mA$, for which the phase shifts $180°$ at $15.8MHz$. Therefore, the gain margin is only $GM = 11.3dB$, which is on the low side. However, the LDO will not operate is this region often. The poles will cause ringing during transient simulation. For $I_{out} = 25mA$ and $I_{out} = 50mA$, the poles are split well and the gain margin is larger than $GM = 33.3dB$, which is large enough.

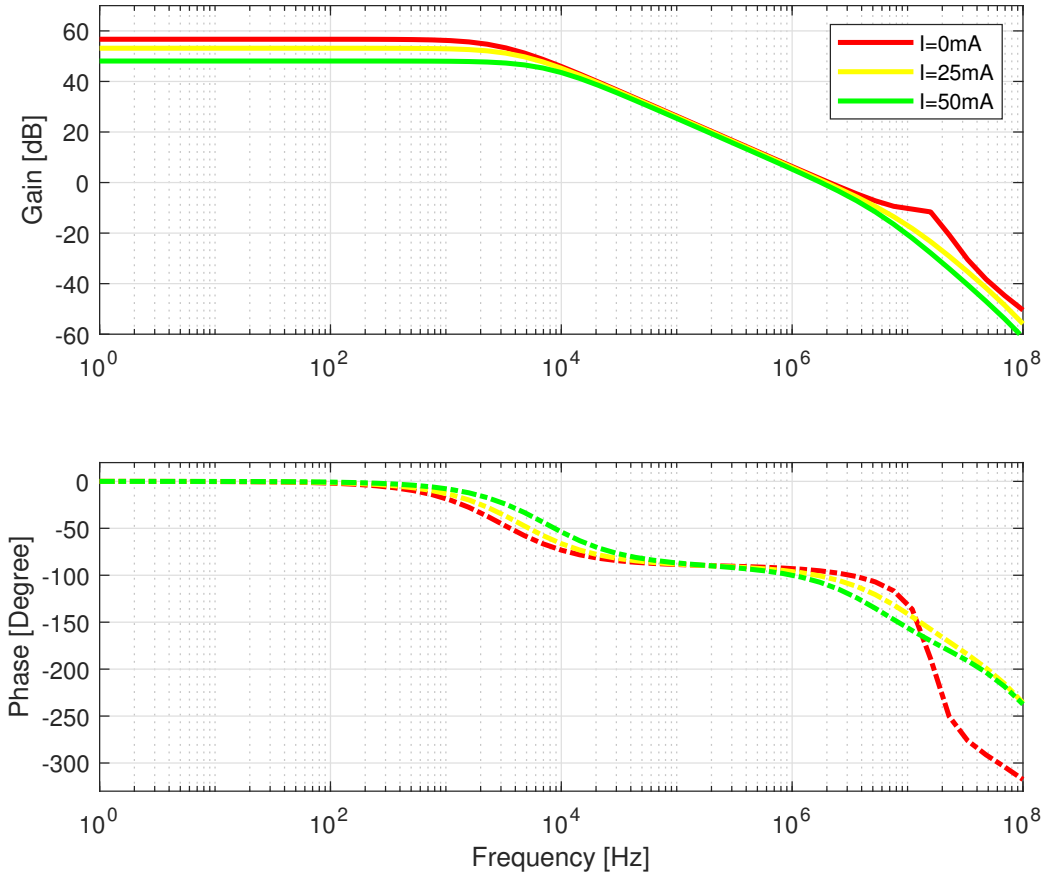
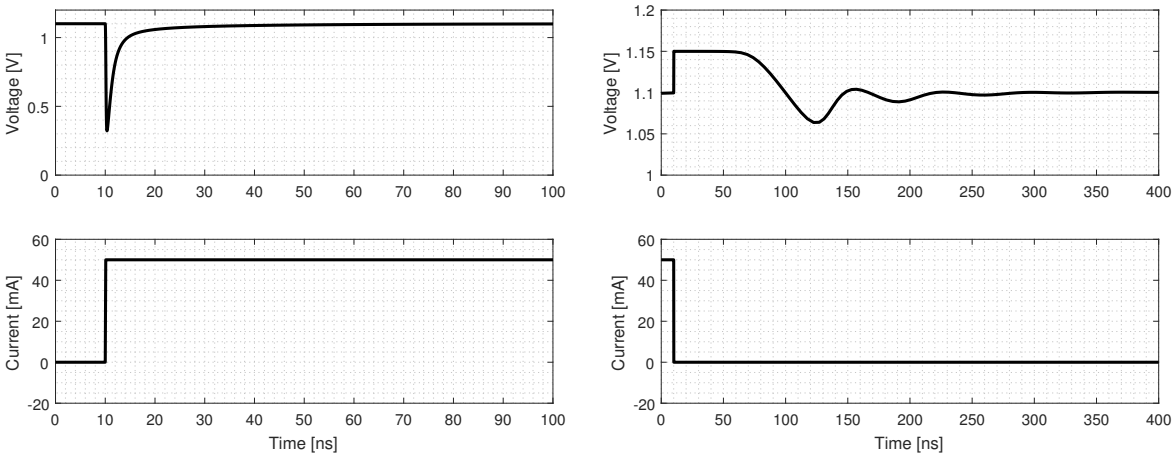


Figure 4.21: Bode plots for different output currents, loaded with $10pF$ capacitance

4.8.6. Transient response

Another way to check the stability is via the transient response. A fast LDO will show spikes with smaller amplitudes and a stable LDO will show a nice settling. The transient simulations are done in steps of $5\ mA$, each with an up- and down going step. At the end the full $50\ mA$ step is executed. The results are

illustrated in appendix C.1. Results of the full current step are shown in figures 4.22a and 4.22b. The circuit is loaded with a capacitive load of $10\ pF$ and the rise and fall time of the current is $t_r = 100\ ps$. Moreover, the sources are ideal and the effect of bond wires is not simulated. The 99% settling time is $t_s = 32.6\ ns$ and $t_s = 182.6\ ns$ respectively. This fast settling time is quite remarkable since the bandwidth is only $F_{-3dB} = 2.96\ k$. The settling time should be in the order of tens of microseconds. According to figure 4.22a, the response time of the LDO is $t_r = 361\ ps$.



(a) Full up-going step

(b) Full down-going step

Figure 4.22

4.9. Test structures

The LDO circuit will be measured in a tank filled with liquid helium Therefore cables of $3m$ will be connected to the chip in order to read out the circuit. All the DC measurements can be done without any buffers. However, the results from the transient simulations show some high frequency behavior. Therefore it is useful the design a on chip 50Ω buffer to drive the long 50Ω cable. The transient measurements can be done in two ways. The current steps can be placed on chip, or at room temperature. Since long interconnects are connected to the chip, it is not reasonable to place the current steps at room temperature, it will cause huge voltage spikes. Therefore, on chip current steps will be designed.

4.9.1. 50Ω Buffer

A 50Ω buffer is used to drive the long cables. One of the most simple, but effective buffers, is shown in figure 4.23. A single NMOS transistor driven by a controllable current source is already suitable for this application. The designed current DAC can be used to control the transconductance of the transistor. The current coming from this DAC is mirrored two times, with a total current gain of $250x$. Hence, the nominal current of the buffer is $I_{d,buf} = 2mA$. In order to get an output impedance of $Z_{out} = 50\Omega$, the transconductance should be $g_{m,MUN1} = 20mS$. The range of the current DAC satisfies the spread in the transconductance of transistor $MUN1$. The transfer curve is shown in figure 4.24, the buffer is loaded with $C_{out} = 10pF$. The resulting bandwidth is defined as

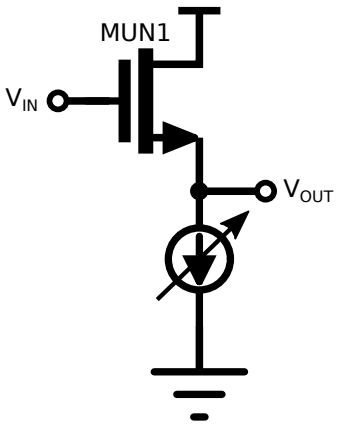


Figure 4.23: Buffer circuit

$$f_{-3dB} = \frac{g_{m,MUN1}}{2\pi C_{out}} = 318.3MHz \tag{4.19}$$

The buffer is perhaps too slow to let the voltage spikes through, however the amplitude of the spikes is not important. The goal is to visualize the settling behavior of the circuit. Another drawback of this buffer is the gain of $A_0 = 0.93$. Usually, the gain of a buffer stage is

close to 1. However, it is no problem for this application. Though the gain of the buffer can easily be calculated via one simple measurement. A small low frequency AC signal will be applied at the input of the LDO. The gain of the buffer is then the ratio between the amplitude of the output of the LDO and the output of the buffer.

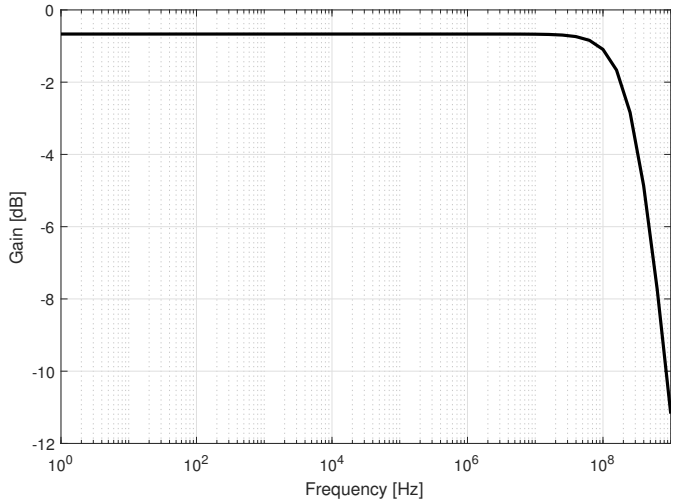


Figure 4.24: Transfer curve of the buffer

4.9.2. Current steps

On chip current steps will be designed in order test the transient behavior of the LDO circuit. Ten current steps with each an output current of $I_{out} = 5mA$ give the opportunity to test the circuit on different current levels. The rise and fall time should be in the range of $t_{r,s} = 100ps$, faster than the response time of the LDO. A digital control network will enable and disable the steps.

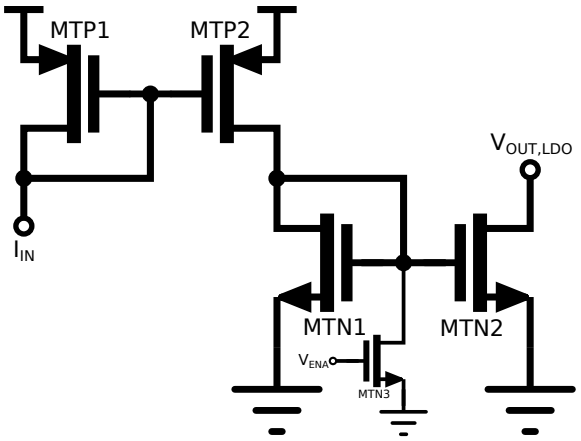


Figure 4.25: Step circuit

The design of a current step is not straight forward. There is a trade-off between speed, maximum current, leakage current and area. First, a current source has to be connected to the output of the LDO. This current source is NMOS transistor $MTN2$, it is sized such that it can handle $5mA$ of current. The input current I_{in} comes from the already designed current DAC and is mirrored two times. The total current factor is $500x$. It is challenging to keep the rise and fall times as small as possible, preferably a 1 or 2 pole settling. Switching at the gate of transistor $MTN2$ gives the opportunity to turn the transistor fully on and off.

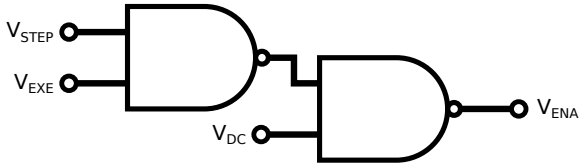


Figure 4.26: Digital control network

The leakage current is therefore low, only $191nA$ per current step. The rise and fall time are in the order of tens of picoseconds either, which is good enough. The area of the switch is quite small, therefore the overall area of the current step is small too. A digital control network, which consist of 2 NAND gates like in figure 4.26 controls the enable signal of the ten current steps. If V_{STEP} is high $('1')$, the selected step is enabled. After a short time, when

V_{EXE} goes from high to low ($'0'$), a step from $I = 0mA$ to $I = 5mA$ is executed. On the other hand when V_{EXE} goes from low to high, a step from $I = 5mA$ to $I = 0mA$ is executed. V_{DC} should be high under these conditions. It is a bit different when a step will be executed from $5mA$ to $10mA$, two steps blocks are needed. For block 1, V_{STEP} and V_{DC} should be high, it is not sensitive for V_{EXE}. For block 2, V_{STEP} should be high and V_{DC} should be low. A step from $5mA$ to $10mA$ will now be executed when V_{EXE} goes from high to low. This is stated in the truth table 4.6.

Table 4.6: Truth table of digital control network

V_{STEP}	V_{DC}	V_{EXE}	V_{ENA}	Mode
0	0	0	1	OFF
0	0	1	1	OFF
0	1	0	0	DC
0	1	1	0	DC
1	0	0	1	OFF
1	0	1	1	OFF
1	1	0	0	STEP
1	1	1	1	STEP

4.10. Serial Peripheral Interface

In total, there are 8 current DACs, 2 capacitive DACs, 21 steps signals and 1 enable signal for the constant transconductance cell which will be controlled by a 7 bit Serial Peripheral Interface (SPI). This means that 90 out of the available 128 outputs of the SPI are in use. Each DAC is connected to a separate register and the 21 step signals are divided over four registers, the step execution signal is connected to a separate register. A UART communication protocol is loaded on a FPGA in order to communicate with the SPI via Matlab.

4.11. Layout

The total area of the core LDO circuit, without any test structure or SPI, is $A_{LDO} = 0.0313mm^2$. The routing of the pass device is the biggest challenge, since the drain source current is $I_{ds} = 50mA$. Therefore, most of the area is occupied by the pass device.

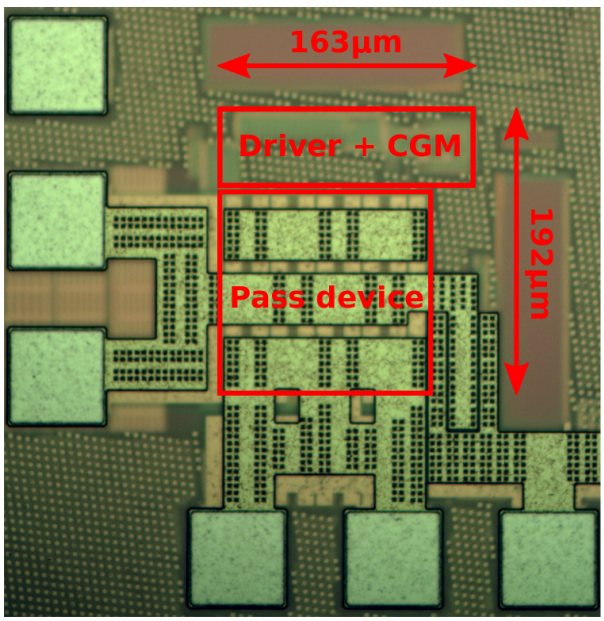


Figure 4.27: Microscopic photo of the LDO

5

Measurements

The performance of the designed LDO will be measured at $4\ K$ and room temperature as well. A dipstick with the device under test goes into a dewar with liquid helium ($4.2\ K$). A PCB will be designed in order to connect the bonded chip, via the dipstick, to the measurement equipment.

5.1. Printed circuit board

The chip is bonded in LCC32 package and the LCC32 socket will be placed on the PCB. Two socket strips connects the PCB to the dipstick. All digital and analog supplies will be decoupled with $C_{Vdd} = 100\ nF$. The separate supply for the power device is decoupled with four parallel capacitors with the a maximum value of $C_{Vdd,PT} = 200\ \mu F$, since the large output current is provided by this supply. 2-way pin headers are placed at V_{out} in order to disconnect the long interconnects from the chip during AC measurements. A $3.1\ mm$ hole is drilled in order to mount the PCB on the dipstick. Besides, one PCB without any decoupling will be fabricated in order to test the stability of the LDO circuit. Figure 5.1 shows the PCB with full decoupling.

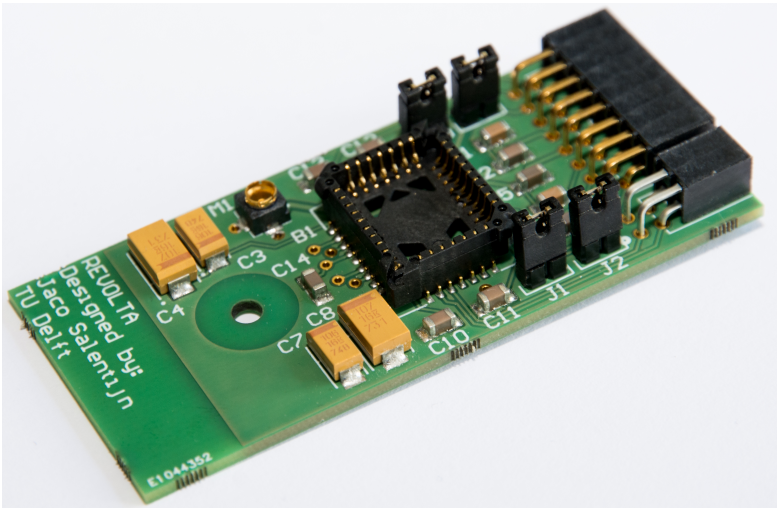


Figure 5.1: Printed circuit board with full decoupling

5.2. Measurement setup

The measurement setup consists of the PCB with chip, the dipstick with the helium dewar and measurement equipment, like in figure 5.2. The measurement equipment consists of supplies, a multimeter, a oscilloscope and network analyzer. The multimeter will be used for DC measurements and the oscilloscope and network analyzer for AC measurements. The PCB with full decoupling will be used for DC measurements and both PCBs, with and without decoupling, will be used for AC measurements.

5.2.1. Supplies

Below, a list of the needed supply voltages. Two HMC8043 sources will be used instead of a power supply PCB, since it is easier to increase the supply voltage for line regulation measurements. Moreover, it is useful to know how much current is flowing through each channel of the supplies. A Keithley 2636B SMU in remote mode will be used to supply the pass device in order to compensate for the long interconnects resistance.

- $2.50\ V$ Digital IO/Line drivers
- $1.10\ V$ Digital core
- $1.15\ V$ Analog core
- $0.30\ V$ Reference
- $5.00\ V$ Optocouplers
- $3.30\ V$ Optocouplers

5.2.2. Other equipment

A Keithley 2002 multimeter will be used to measure the output voltage of the LDO. This high-end multimeter is not only able to measure DC voltages, but it can also average the measured voltage. A Rigol DS4034 oscilloscope will be used to measure the transient response when the current steps are activated. A Stanford Research SR7700 spectrum analyzer will be used to measure the noise spectrum.

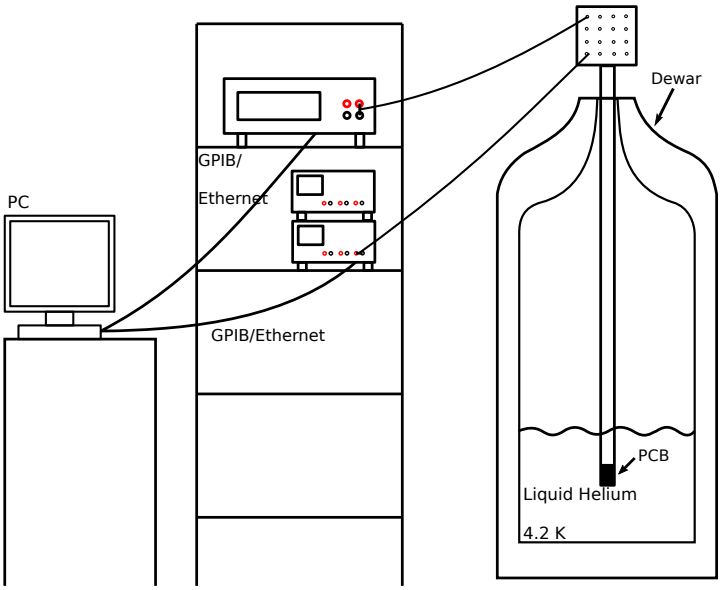


Figure 5.2: Measurement setup [28]

5.3. DC measurements

The supplies and the multimeter will be used for DC measurements, which are the line- and load regulation and power consumption. The PCB with full decoupling will be used for these measurements.

5.3.1. Line regulation

The line regulation is simulated for a range of $V_{in} = 1.15V$ till $V_{in} = 1.20V$. However, voltages above $V_{in} = 1.2V$ could seriously damage the core of the chip. Therefore, the line regulation is also measured for a range of $V_{in} = 1.15V$ till $V_{in} = 1.20V$. The output voltage variation due to the input voltage shift is specified to be lower than $\Delta V_{out} < 0.2mV$. Figure 5.3 shows the measured line regulation for room

temperature and $4K$, for an output current of $I_{out} = 50mA$. The output voltage variation for room temperature and $4K$ are $\Delta V_{out,RT} = 0.33\ mV$ which corresponds to a line regulation of Li.Re. $= 6.6\ mV/V$. This value is 1.65 times larger as simulated, which could caused by a lower gain in the first and second stage. Besides that, the output of the LDO was noisy, and therefore less easy to measure. The noise of the reference voltage source (HMC8043) was large and affected the measurement. Luckily, the digital filtering and of the multimeter solved this issue.

The measured voltage variation at $4\ K$ is $\Delta V_{out,4K} = 0.42\ mV$, which corresponds to a line regulation of Li.Re. $= 8.4\ mV/V$. Probably, the gain of the first and/or the second stage is lower at $4\ K$ with respect to room temperature. The simulated gain of the first and second stage is $A_{fs+ss} = 61.9\ dB$. The recalculated gain form the measurements are $A_{fs+ss} = 54.9\ dB$ and $A_{fs+ss} = 52.8\ dB$ for room temperature and $4\ K$ respectively. This means that the gain for the first and second stage at $4\ K$ is decreased with $2.1\ dB$.

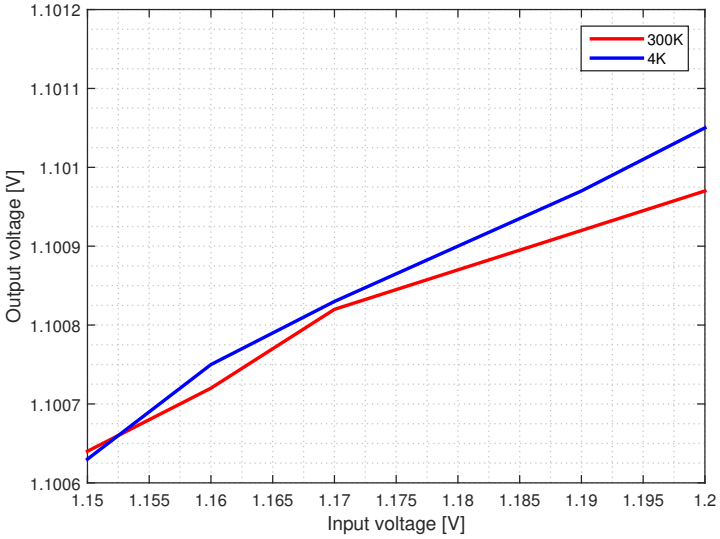


Figure 5.3: Measured line regulation at room temperature and $4K$

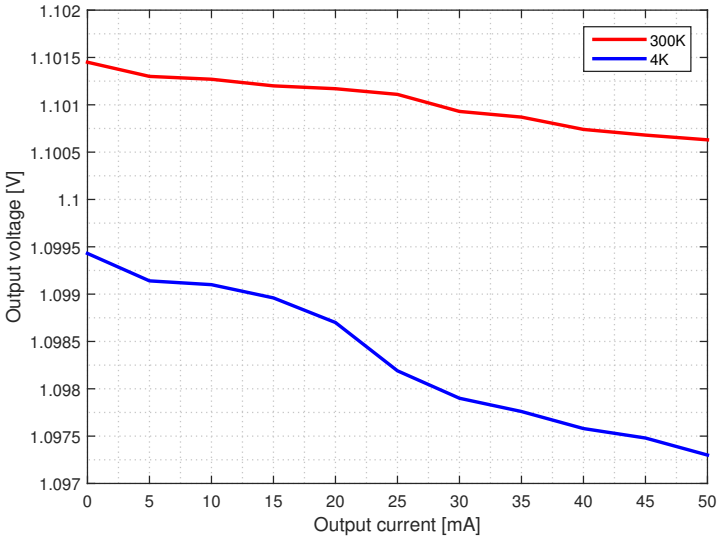


Figure 5.4: Measured load regulation at room temperature and $4K$

5.3.2. Load regulation

The minimum and maximum output current of this LDO is set to $I_{out,min} = 0mA$ and $I_{out,max} = 50mA$ respectively. The allowed output voltage variation due to the load current shift is set to $\Delta V_{out} < 1mV$. Figure 5.4 shows the measured load regulation for room temperature and $4K$, for nominal supply of $V_{in} = 1.15V$. The output voltage variation for room temperature and $4K$ are $\Delta V_{out,RT} = 0.82mV$ which corresponds to a load regulation of Li.Re. $= 16.4\ mV/A$. This value is 1.85 times larger as simulated, probably caused by the same lower gain of the first and second stage. The measured voltage variation at $4\ K$ is $\Delta V_{out,4K} = 2.1\ mV$, which corresponds to a line regulation of Li.Re. $= 42\ mV/A$. Probably, the gain of the first and/or the second stage is lower at $4\ K$ with respect to room temperature. Moreover, the transconductance of the third stage could be lower at $4\ K$ with respect to room temperature.

5.3.3. Power consumption

The power consumption of the LDO circuit is divided into two part. The first part is the driver, which includes the first stage, second stage, constant transconductance circuit and biasing. The constant transconductance circuit provides the biasing currents for the first and second stage. Therefore, it is useful to measure this current over the temperature range from $4\ K$ to room temperature in order to know what will happen with this biasing current. Figure 5.5 shows the measured constant transconductance current over the temperature range. This current is at $4\ K$ 3.3 times lower with respect to room temperature because of the increased mobility and the increased N-poly resistor value. The simulated current is $I_{cgm} = 8.4\ \mu A$. The difference between the measured and simulated value is because of the resistor spread. The difference is current could result in a lower transconductance of the first and second stage, which also affects the bandwidth of the system.

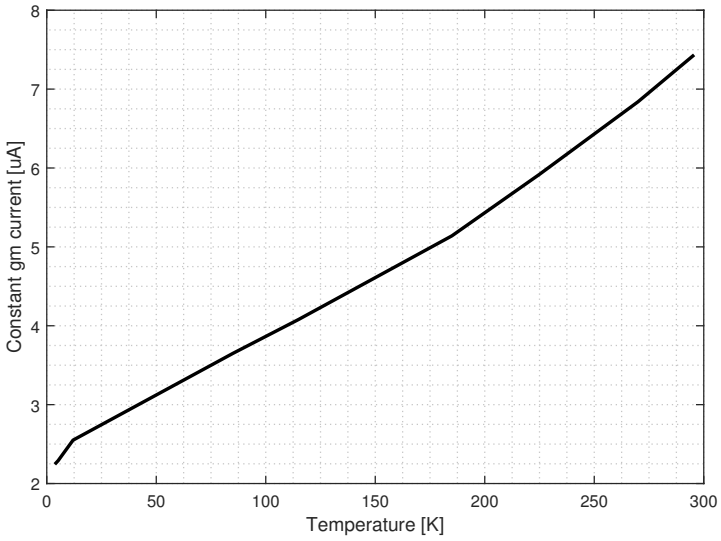


Figure 5.5: Measured constant gm output versus temperature

The second part is the pass device, which is biased with a minimum leakage current. The power consumption of the pass device and the driver are listed in table 5.1. The simulated power consumption resembles the measured power consumption at room temperature. However, there is a major difference between the power consumption at $4\ K$ with respect to room temperature, because of the decreased current from the constant transconductance circuit. The current DACs and extra branches increase the power consumption with about $60\ \mu A$ at room temperature and $26\ \mu A$ at $4\ K$. Consequently, the power consumption at $4\ K$ is $85.0\ \mu A$, lower than the specified $100\ \mu A$.

5.4. AC measurements

The AC measurements includes the PSRR and transient behaviour. The PCB without any decoupling is used for these measurements. However, the output showed a oscillation which has a frequency of $F_{osc} = 1.9MHz$. Therefore, a $C_{Vdd} = 1\ \mu F$ is soldered on the PCB in order to suppress the oscillation.

Table 5.1: Power consumption for $I_{out} = 50mA$

Temperature	I_{driver}	I_{pt}	I_{total}
300 K Sim.	183.2 μA	26.1 μA	209.3 μA
295 K Meas.	181.0 μA	27.8 μA	208.8 μA
4 K Meas.	85.9 μA	25.1 μA	111.0 μA

5.4.1. Power supply rejection ratio

The easiest way to measure the PSRR at DC is to measure the line regulation, the slope is PSRR at DC. The line regulation at room temperature is measured for different load conditions. Figure 5.6 shows the results. The line regulation improves for lower output current, since the loop gain increases.

Table 5.2: Power supply rejection ratio

Output current	Line regulation	PSRR ($0\ Hz$)
$I_{out} = 0\ mA$	3.4 mV/V	49.4 dB
$I_{out} = 25mA$	4.8 mV/V	46.4 dB
$I_{out} = 50mA$ (RT)	6.6 mV/V	43.6 dB
$I_{out} = 50mA$ (4 K)	8.4 mV/V	41.5 dB

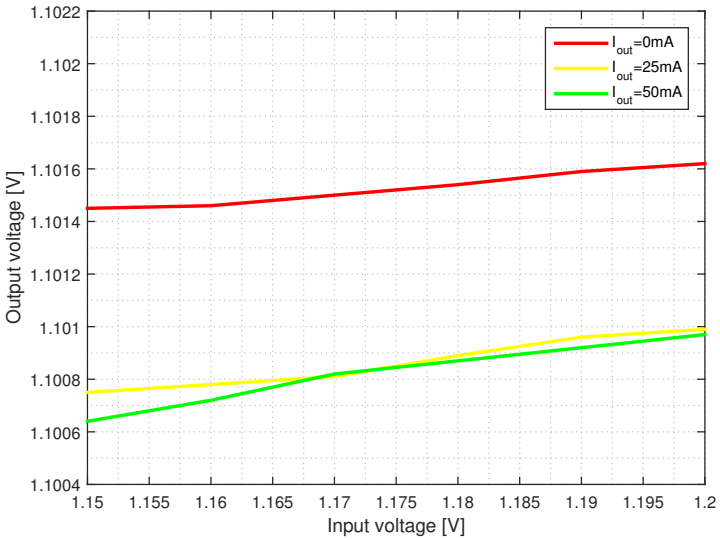


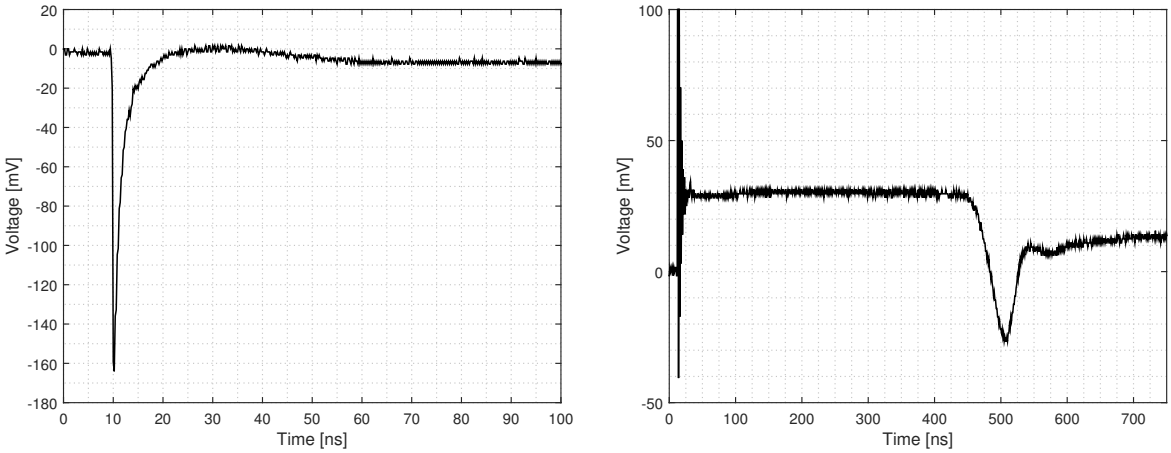
Figure 5.6: Measured line regulation at room temperature for different load conditions

5.4.2. Transient behaviour

The on-chip current are used to measure the settling behaviour of the LDO circuit. The on-chip buffer is used to drive the 50Ω interconnect. This buffer is biased with a current of $2mA$ in order to create a transconductance of $20mS$. The output impedance of the buffer is therefore $R_{out} = 1/g_m = 1/20m = 50\Omega$. An AC coupled scope measures the transients behaviour.

Figures 5.7a and 5.7b show the full current step response, measured at room temperature. From these plots, we see can extract the load regulation. This voltage variation is defined as $\Delta V = V_{t=\infty} - V_{t=0}$. This variation is rather large, since the V_{dd} of the pass device is not compensated for the long interconnects. In other words, the V_{dd} of the pass device decreases when the load current increases. Besides the load regulation, the amplitude of the spike is important. The measured amplitude is much lower than the simulated amplitudes. This is caused by the limited bandwidth of the buffer. In other words, the buffer is not fast enough. The amplitude of these spikes are not important, since we are only interest in the settling behaviour and time.

The extracted settling time of figure 5.7a is about $t_s = 50ns$, which is slightly higher than simulated. This could be caused by the difference in output capacitor or difference in transconductance of the first stage. The capacitance of the bond pads, package, and PCB are added to this output capacitance and can not be neglected. Therefore, the settling time is higher and the figure shows a underdamped settling behaviour. The extracted settling time of figure 5.7b is about $t_s = 700ns$, which is much higher than simulated. At $t = 50ns$, the output voltage of the LDO is $V_{out} = 1.15$, which is the supply voltage. In other words, the output is clipped to the supply voltage. At this time, there is no phase margin left. At $t = 450ns$, the LDO starts to settle. The time that the LDO is clipped is much longer than simulated since the output capacitance is higher than simulated.



(a) Full up-going step

(b) Full down-going step

Figure 5.7

The transient response at different output current levels are shown in appendix C.2.

5.5. Summary

Table 5.3 shows the measurement results. Most of the specifications shows no large differences between RT and $4\ K$, except for the load regulation.

Table 5.3: Performance for RT and $4\ K$

Specification	**RT**	**4 K**
Output voltage	$1.1\ V$	$1.1\ V$
Output current	$0 - 50\ mA$	$0 - 50\ mA$
Output capacitance	$0 - 10\ pF$	$0 - 10\ pF$
Load regulation	$16.4\ mV/A$	$42\ mV/A$
Line regulation ($I_{out} = 50\ mA$)	$6.6\ mV/V$	$8.4\ mV/V$
PSRR ($I_{out} = 50\ mA$)	$43.6\ dB$	$41.5\ dB$
Efficiency	95.3%	95.4%

6

Conclusion and Future works

6.1. Conclusion

The proposed classical controller operating at $4K$ needs a clean supply voltage. Voltage regulators are able to clean dirty supply voltage and produce a stable, regulated voltage. Low drop-out voltage regulators can achieve a very low output noise and low ripple. There are thousands of LDOs on the market, each which different specifications. Many of these regulators are not stable at $4\ K$. These regulators can be divided into analog and digital LDOs. Digital LDOs can operate at much lower supply voltages, which could results into a better power efficiency. Moreover, digital are usually faster since the aspect ratio of the pass device is smaller with respect to analog LDOs. However, the output impedance of such pass device is usually smaller compared to analog one, which results is a worse PSRR. Moreover, the output voltage of a digital is always bouncing between values in steady state situation. This bouncing behaviour introduces spikes in the output voltage. The output voltage is usually regulated with a large external capacitor.

Analog LDOs can be divided into dominant pole structures and C-free structures. A large external capacitance regulates the output voltage of a dominant pole structure. The capacitor provides the faster changing current. C-free structures do not require any external capacitor, the voltage is regulated by the Miller capacitance. The bandwidth is usually higher and therefore the response time is much lower with respect to dominant pole structures. Analog LDO are usually ripple free and the output noise is lower with repsect to digital LDOs. Moreover, the output imepdance of the pass device is larger which results in a better PSRR.

There are several design trade-offs for analog LDOs, like efficiency, maximum output current, stability and area. LDOs with a high output current are complex to stabilize and occupies more area compared to LDO with less output current. The efficiency of LDOs depends mainly on ratio of in- and output voltage. Advanced techniques could be applied in order to increase PSRR, speed or stability. Negative capacitor circuits are able to increase the PSRR for high frequencies, multiple-loop are usually faster and controls the settling behaviour.

The measurements and simulation of the LDO show some differences, especially the line- and load regulation. Fist of all, the load and line regulation were difficult to measure, due to the relatively high output noise of the reference source. Second of all, the measured current from the transconductance circuit differs from simulation. This could result in a lower transconductance of the first and second stage and thus a lower bandwidth. Also, the overall loop gain could be affected. And finally, the power consumption at $4\ K$ is much lower with respect to room temperature, since the mobility is increased. At the end, the LDO is functional at room temperature and $4\ K$.

6.2. Future work

To complete the measurements, a few activities can be done. These activities are based on replacing measurment equipment and small updates in the design of the LDO circuit.

- The line and regulation can be improved. The reference voltage source must be replaced by a source with very low output noise to improve the measurability. Also, the lag of loop gain must be understood.
- The transient simulation at $4\ K$ shows if the LDO settles after performing a load current step.
- The noise performance at room temperature and $4\ K$ can be measured.
- The PSRR at higher frequencies must be measured in to order to know what the performance is at higher frequencies.
- The LDO can be tested with realistic load circuits, analog and digital ones.

Some recommendation for a new LDO design:

- First of all, the start-up circuit of the constant transconductance circuit must also operate at $4\ K$, which is now not the case. Therefore it is more difficult to measure all the performance of the LDO. The aspect ratio of the start-up diode is designed badly. The increased threshold voltage results in a lower leakage current, and therefore the diode is not powerful enough to start up to circuit.
- The noise performance can be increased by using larger devices, especially for the transistors in the first stage.
- The bandwidth and settling could be improved by adding extra loops or applying DFC.
- The SMU configured in remote mode is necessary to compensate for the interconnect resistance. At the moment, in this mode the circuit is not stable.

A

Calculations

A.1. Line regulation

The line regulation is divided into two parts. The first part is the variation in output voltage due to the input voltage. Because of that, the reference voltage will also change. Therefore, the second part the variation due the variation in reference voltage.

$$\begin{aligned}\text{Line regulation} &= \frac{\Delta V_{out}}{\Delta V_{in}} \\ &= \left(\frac{\Delta V_{out}}{\Delta V_{in}}\right)_{LDO} + \left(\frac{\mathrm{A}}{1+\mathrm{A}\beta}\right)\left(\frac{\Delta V_{ref}}{\Delta V_{in}}\right) \\ &\approx \frac{g_m r_o}{1+\mathrm{A}\beta} + \left(\frac{\mathrm{A}}{1+\mathrm{A}\beta}\right)\left(\frac{\Delta V_{ref}}{\Delta V_{in}}\right) \\ &\approx \frac{g_m r_o}{1+L_o} + \frac{1}{\beta}\left(\frac{\Delta V_{ref}}{\Delta V_{in}}\right) \\ &\approx \frac{g_m r_o}{L_o} + \frac{1}{\beta}\left(\frac{\Delta V_{ref}}{\Delta V_{in}}\right)\end{aligned} \tag{A.1}$$

Where L_o is the loop gain, A is the gain from input to output, β is the feedback factor, g_m and r_o are the transconductance and the output impedance of the pass device. In this equation there is an assumption that the gain of the driver is high.

B

Matlab code

B.1. Third pole extraction

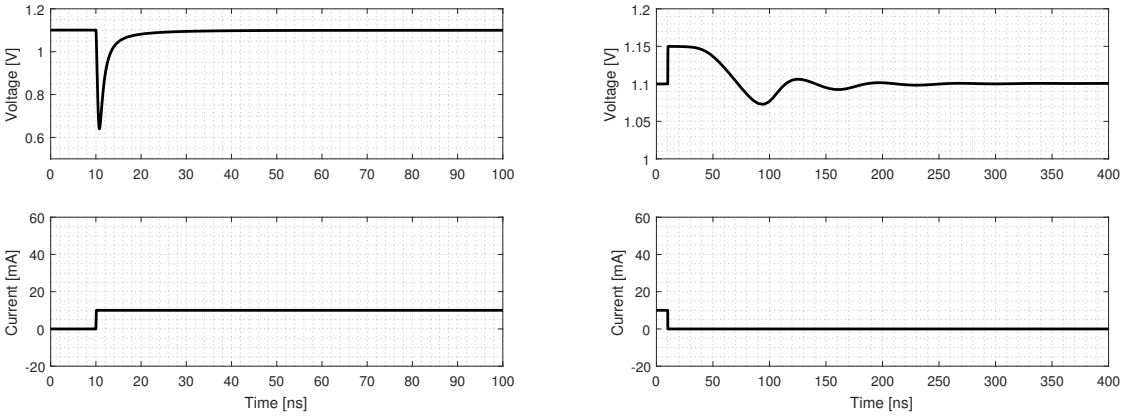
```
% Symbolic calculation of third pole in Nested Miller architecture

clear all
close all

syms s vin v1 vout gm2 gm3 ro2 ro3 C2 Cgd Cb i1 i2 i3 i4 i5 i6 i7

i1 = gm2 * vin;
i2 = v1 / ro2;
i3 = v1 * s * C2;
i4 = (v1 - vout) * s * Cgd;

eq1 = i1 == i2 + i3 + i4;   % KCL for node v1
v1 = solve(eq1, v1);

i5 = gm3 * v1;
i6 = vout / ro3;
i7 = vout * s * Cb;
i4 = (v1 - vout) * s * Cgd;

eq2 = i4 == i5 + i6 + i7;
vout = solve(eq2, vout);    % KCL for node vout
H = collect(vout/vin);      % Tranfer function
[N, D] = numden(H);

eq3 = D == 0;               % Poles at D = 0
s = solve(eq3, s);
s = simplify(s)
```

C

Plots

C.1. Simulated transient responses

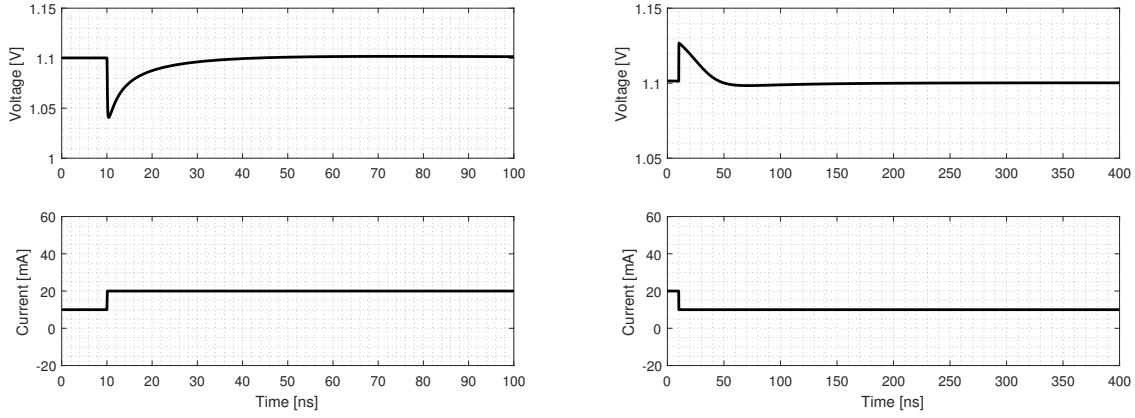
Be aware of the different X- and Y-axis.



(a) $0mA - 10mA$ up-going step

(b) $10mA - 0mA$ down-going step

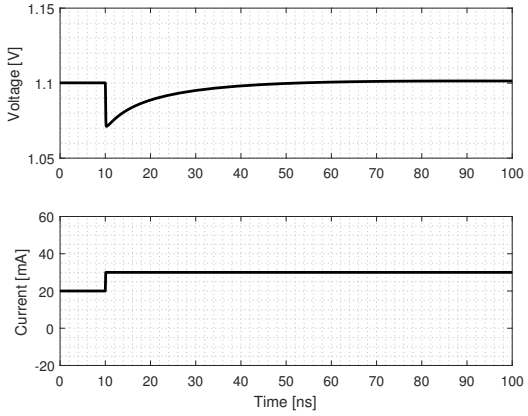
Figure C.1



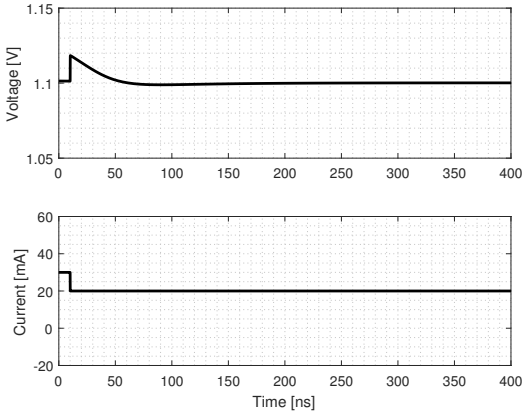
(a) $10mA - 20mA$ up-going step

(b) $20mA - 10mA$ down-going step

Figure C.2

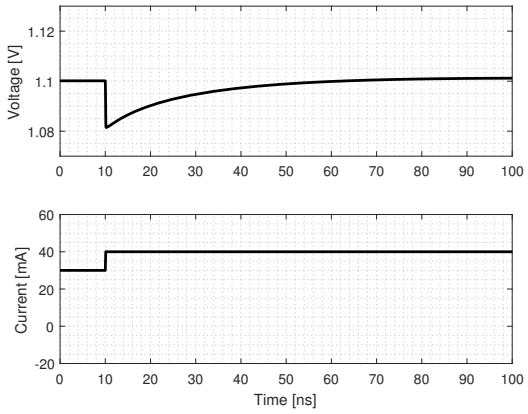


(a) $20mA - 30mA$ up-going step

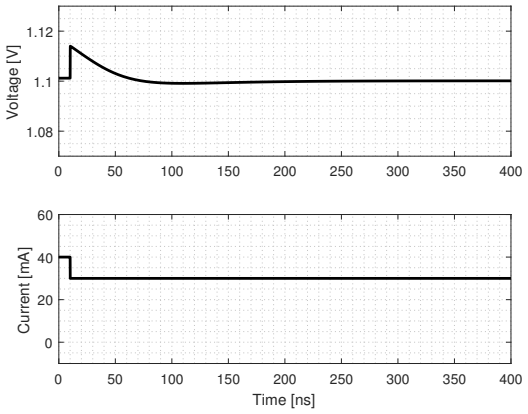


(b) $30mA - 20mA$ down-going step

Figure C.3

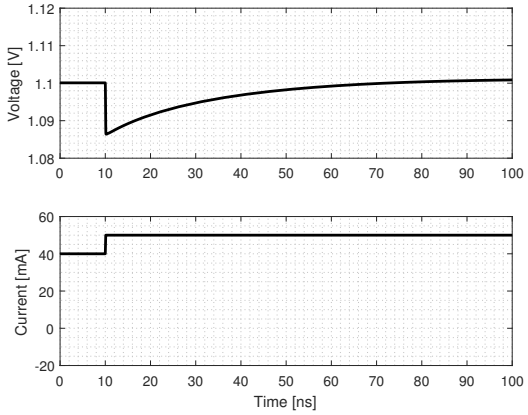


(a) $30mA - 40mA$ up-going step

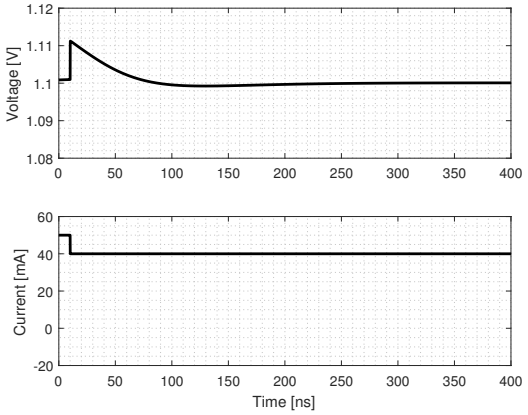


(b) $40mA - 30mA$ down-going step

Figure C.4



(a) $40mA - 50mA$ up-going step

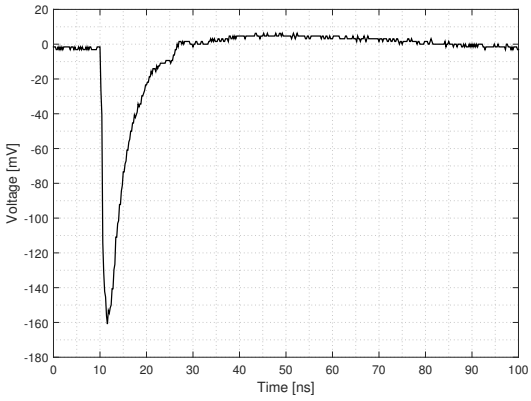


(b) $50mA - 40mA$ down-going step

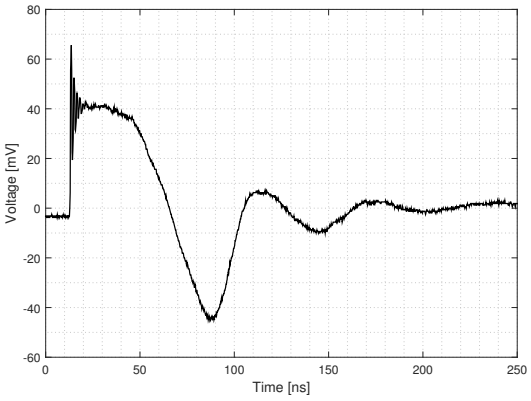
Figure C.5

C.2. Measured RT transient responses

Be aware of the different X- and Y-axis.

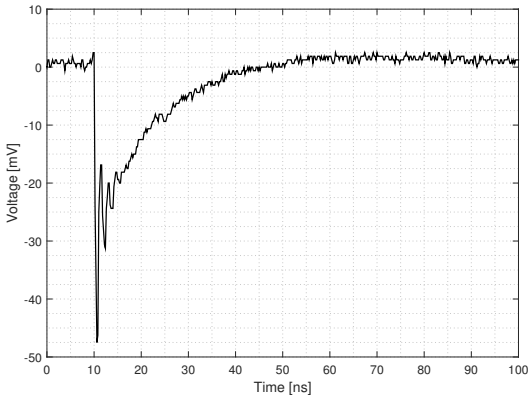


(a) $0mA - 10mA$ up-going step

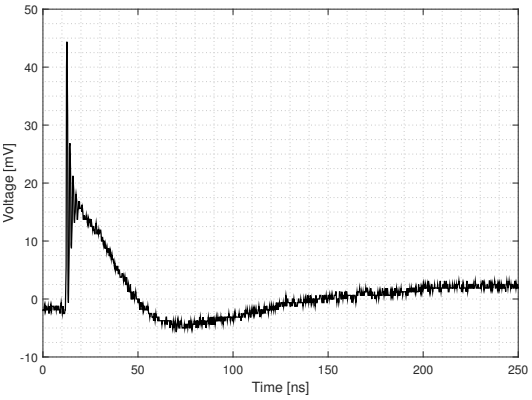


(b) $10mA - 0mA$ down-going step

Figure C.6

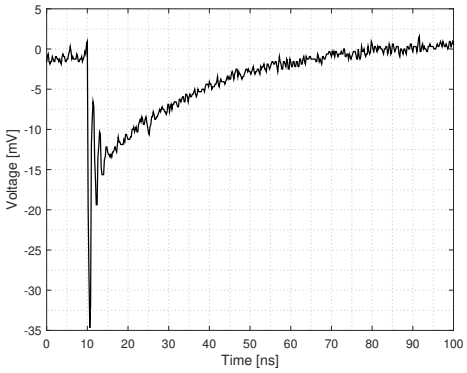


(a) $10mA - 20mA$ up-going step

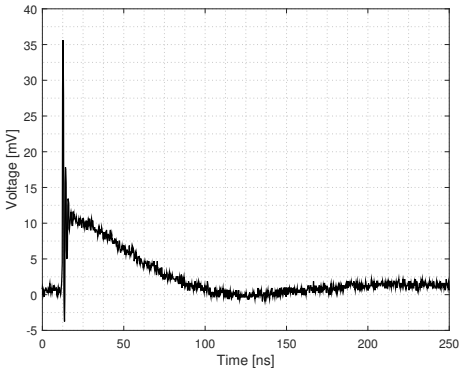


(b) $20mA - 10mA$ down-going step

Figure C.7

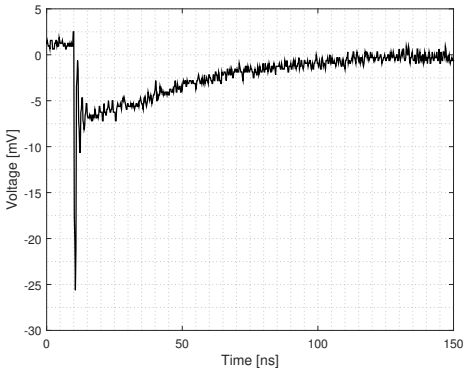


(a) $20mA - 30mA$ up-going step

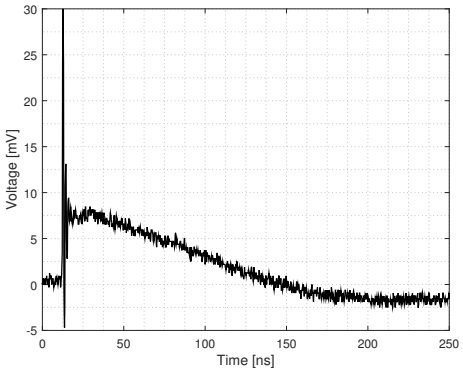


(b) $30mA - 20mA$ down-going step

Figure C.8

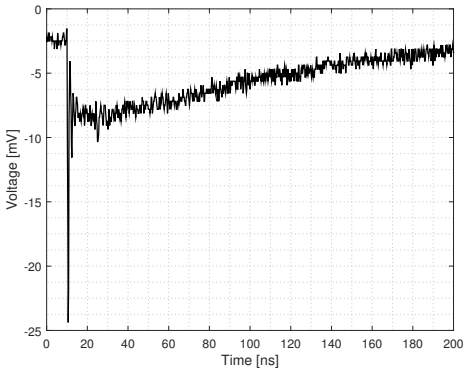


(a) $30mA - 40mA$ up-going step

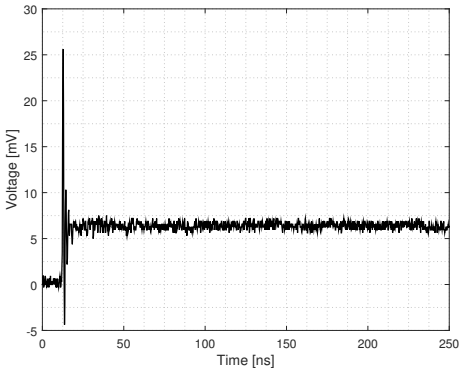


(b) $40mA - 30mA$ down-going step

Figure C.9



(a) $40mA - 50mA$ up-going step



(b) $50mA - 40mA$ down-going step

Figure C.10

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