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A Novel Partial Carrier Stored and Hole Path IGBT for Ultralow Turn-Off Loss and On-State Voltage With High EMI Noise Controllability

Shaogang Wang¹, Chunjian Tan^{1,2}, Liming Wang¹, Houcai Luo¹, Guoqi Zhang², Xianping Chen^{1,2}

¹College of Opto-electronic Engineering, Chongqing University, Chongqing 400044, China.

²Electronic Components, Technology and Materials, Delft University of Technology, Delft 2628 CD, The Netherlands.

Email: xianpingchen@cqu.edu.cn

Abstract

A partial carrier stored and hole path floating dummy shield trench IGBT (PCS-FD-IGBT) is proposed and investigated by simulation. Under E_{off} of $8\text{mJ}/\text{cm}^2$, the $V_{\text{CE(sat)}}$ of 1200V class PCS-FD-IGBT is 1.223V, which is 11.1% and 2.2% less than CON-FD-IGBT and HP-FD-IGBT. Besides, the EMI noise of PCS-FD-IGBT is suppressed at a lower level (dV/dt is below $80\text{kV}/\mu\text{s}$). Moreover, the PCS-FD-IGBT improves the gate drive controllability to easily adapt the larger range of system inductance.

(Keywords: IGBT, partial carrier layer, hole path, turn-off loss, on-state voltage, EMI noise)

Introduction

The performance of IGBTs has almost reached the limit of Si material [1]. Therefore, breaking the limit of the silicon and improving the performance of IGBTs has become a focus for research. So far, many efforts have been devoted to innovate the structure and technology of Si IGBTs in order to further improve its low on-state voltage and excellent switching performance, such as the Trench Gate structure [2], Field Stop technology [3], Carrier Stored technology [4] and Super Junction structure [5]. In recent years, IGBTs have been widely used in the high-speed switching field such as for electric vehicles (EV) which require the switch speed to reach a high frequency (6kHz-12kHz) [6]. In high frequency applications, the electromagnetic interference (EMI) noise and gate drive controllability issues have become as important as the trade-off relationship between on-state voltage ($V_{\text{CE(sat)}}$) and turn-off loss (E_{off}). As we know, for a further increase of the switching performance, it is necessary to reduce the Miller capacitance. Accordingly, the shield gate concept was proposed [7]. As expected, the floating dummy shield trench structure brings with it a low Miller capacitance, but it also produces the EMI noise during the turn-on operation. To solve this problem, the hole path was proposed and optimized the Miller capacitance [8]. Nevertheless, it deteriorates the trade-off relationship between $V_{\text{CE(sat)}}$ and E_{off} , which cannot be ignored.

In this letter, we proposed a novel IGBT combined with partial carrier stored and hole path structures based on the floating dummy shield trench structure for a 1200V high-speed switching application.

Results and Discussion

Fig. 1(a)-(c) show the structures of conventional /hole path floating dummy shield trench IGBT (CON-/HP-FD-IGBT) and PCS-FD-IGBT, respectively. In our study, simulations are calculated by using TCAD, The carrier lifetime is set to $1\mu\text{s}$.

The carrier stored structure has an inherited defect, which degrades blocking capacity when the carrier stored layer is set at a higher concentration [9]. Therefore, we calculate the relationship between breakdown voltage and carrier stored doping concentration. As shown in Fig. 2, the total carrier stored layer structure decreases sharply when the doping concentration is higher than $3\times 10^{17}\text{ cm}^{-3}$, while the breakdown voltage of partial carrier stored layer structure is maintained at 1414 V until the doping concentration is higher than $1\times 10^{18}\text{ cm}^{-3}$. This proves that the partial carrier layer has a reliable ability to resist breakdown compared with the total carrier stored layer structure.

It reported that the dV/dt at more than $80\text{ kV}/\mu\text{s}$ will be more likely to cause EMI noise from a common circuit [10]. To investigate the effects of capacitance on EMI noise (recovery dV/dt) during the turn-on operation (see Fig. 3(b)), we calculate the input capacitance (C_{ies}) and reverse transfer capacitance (C_{res} , Miller capacitance) of three structures with different doping concentrations, as shown in Fig. 3(a). The C_{ies} of PCS-FD-IGBT is $16.103\text{ nF}/\text{cm}^2$ which is 7.8% and 7.2% lower than that of CON-FD-IGBT and HP-FD-IGBT (17.468 and $17.335\text{ nF}/\text{cm}^2$) respectively, as shown in the orange dashed box. On the contrary, the C_{res} of PCS-FD-IGBT ($0.249\text{ nF}/\text{cm}^2$) shows the 10.2% and 1.2% higher in comparison to that of CON-FD-IGBT and HP-FD-IGBT (0.226 and $0.246\text{ nF}/\text{cm}^2$) respectively. Corresponding to this, we find that the turn-on recovery dV/dt of the PCS-FD-IGBT is $80\text{ kV}/\mu\text{s}$, which is 52.7% and 8.2% lower than that of CON-FD-IGBT and HP-FD-IGBT (169.1

kV/ μ s and 87.1kV/ μ s), respectively. Consequently, we can find that the proposed structure effectively suppresses the EMI noise by optimizing the Miller capacitance.

The gate drive controllability is required to ensure that the larger range of system inductance can be easily adapted by an adjusting gate drive part with low energy loss. To ensure this, we calculate the relationship between the gate resistance (R_g) and turn-off loss (E_{off}) of three different structures under the same $V_{CE(sat)}$ in the inductive load circuit. As shown in Fig. 4, it is visible that the E_{off} of PCS-FD-IGBT is 4.252 mJ/cm², which is 32.2% and 9.6% lower than that of CON-FD-IGBT and HP-FD-IGBT under the lower gate resistance ($R_g = 5\Omega$). This illustrates that PCS-FD-IGBT has lower turn-off dissipation within the high-speed switching state. Meanwhile, it is easy to see that the slope of fit curve of the partial carrier stored structure is at 0.286, which is higher than that of conventional and hole path structures (0.235 and 0.247), respectively. These results indubitably prove that the partial carrier stored layer structure has excellent gate drive controllability.

Fig. 5(a) shows the turn-off waves, turn-off delay times (t_d) and turn-off fall times (t_f) of three structures. As was explained above, the hole path structure sacrifices a certain degree of IE effect in exchange for the improved capacitance characteristic and fast turn-off speed. Therefore, the HP-FD-IGBT exhibits the $t_{d(off)}$ of 126ns and t_f of 142ns which is faster than that of CON-FD-IGBT and PCS-FD-IGBT. In Fig. 5(b), the relationship between the E_{off} and $V_{CE(sat)}$ of the CON-FD-IGBT, HP-FD-IGBT and PCS-FD-IGBT calculations are attained by varying the peak P-collector doping concentration. The $V_{CE(sat)}$ of the PCS-FD-IGBT is 1.223V, which is 2.2% and 11.1% lower than that of CON-FD-IGBT and HP-FD-IGBT (1.251V and 1.375V, $E_{off} = 8\text{mJ/cm}^2$).

Conclusion

A novel partial carrier stored and hole path IGBT has been proposed and studied through simulations. By introducing the partial carrier stored and hole path structures, the PCS-FD-IGBT obtains a lower EMI noise and improves the gate drive controllability. Finally, the PCS-FD-IGBT balances the relationship among the turn-off time (T_{off}), turn-off energy loss (E_{off}) and on-state drop voltage

($V_{CE(sat)}$) to achieve a better overall E_{off} - $V_{CE(sat)}$ relationship compared with the CON-FD-IGBT and HP-FD-IGBT.

Acknowledgments

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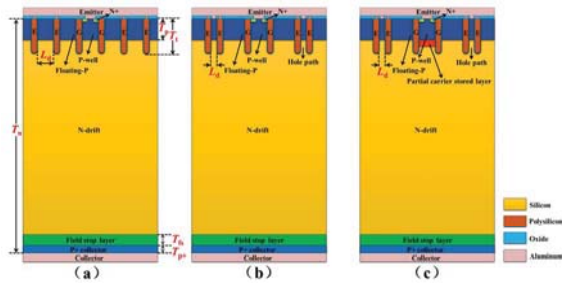


Fig. 1. Schematic cross section of cell structure of (a) CON-FD-IGBT, (b) HP-FD-IGBT and (c) PCS-FD-IGBT.

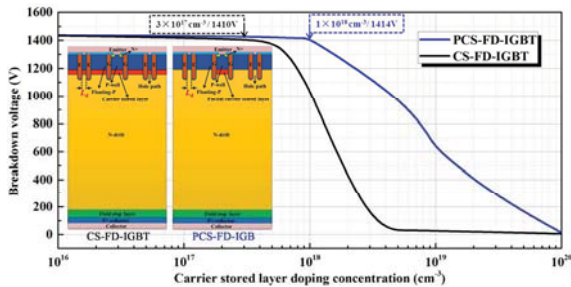


Fig. 2 The relationship between breakdown voltage and carrier stored layer doping concentration of the total carrier layer and partial carrier layer floating dummy shield trench IGBTs ($T = 300\text{K}$).

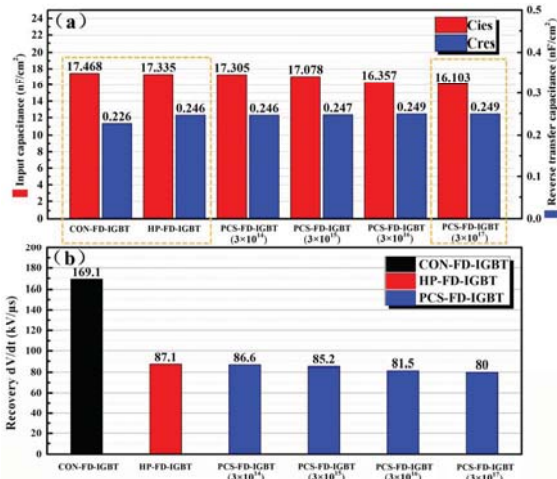


Fig. 3 (a) The input capacitance (C_{ies}) and reverse transfer capacitance (C_{res}) ($V_{CE} = 10\text{V}$ and $T = 300\text{K}$); (b) the turn-on recovery dV/dt (at 100% J_C and $T = 300\text{K}$) of the CON-FD-IGBT, HP-FD-IGBT and PCS-IGBT with different carrier doping concentrations.

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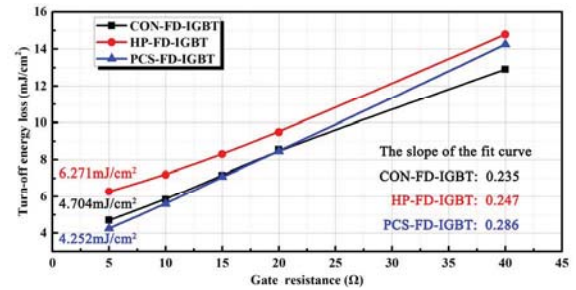


Fig. 4 The relationship between the gate resistance (R_g) and turn-off energy loss of CON-FD-IGBT, HP-FD-IGBT and PCS-FD-IGBT (under the same $V_{CE(sat)}$ and $T = 300\text{K}$.)

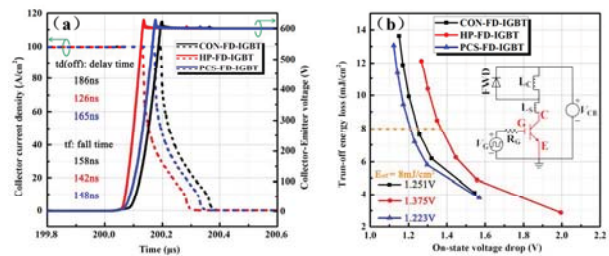


Fig. 5 (a) Turn-off waves, turn-off delay times and turn-off fall times of three different IGBTs under inductive load; (b) The relationship between the turn-off energy loss (E_{off}) and the On-state voltage drop ($V_{CE(sat)}$). The inset shows the simulation inductive load circuit with $V_{CE} = 600\text{V}$, $R_G = 5\Omega$, $L_C = 3\text{mH}$, $L_S = 10\text{nH}$, and $T = 300\text{K}$.