Design for Reliability of Wafer Level MEMS packaging

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door Jeroen Johannes Maria ZAAL

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Dit proefschrift is goedgekeurd door de promotor:
Prof.dr. G.Q. Zhang

Copromotor: Dr.ir. W.D van Driel

Samenstelling promotiecommissie:

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1. Introduction

After the groundbreaking research of Jack Kilby and Robert Noyce on the first semiconductors the world has seen an unrivalled penetration of this technology into virtually any part of society. In 2009 the semiconductor industry sold products with a total value of 226 billion US dollar [1]. As an illustration of the ingression of semiconductors into our live: in 2005 the number of transistors produced per human being on this earth was roughly 90 million, estimations are that this has increased to 1 billion in 2010 [1]. The main enablers of the semiconductor rush are the decreasing feature size and the constantly decreasing costs of semiconductors. The decreasing costs of semiconductors in general are caused by the smaller feature size, the higher yield and larger production volumes. This has made products containing semiconductors cheaper in production thus reaching a larger market. The smaller feature size enables more computing power in the same volume creating new markets and growing application areas.

The increasing number of appliances using semiconductor components is also driving the fast growth of the market. Semiconductor technology is widely used to integrate or miniaturize electronic components. The trend of miniaturization of electronic components also demands the miniaturization and integration of non-electrical functions to allow for large decreases in size, weight and possibly cost.

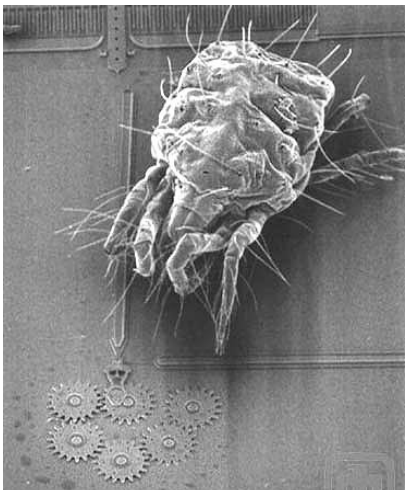


Figure 1 - A mite sitting on a MEMS structure

Soon after the first semiconductors were developed the first Micro Electrical Mechanical Systems (MEMS) were also created. In the 1960's and 1970's experiments with MEMS were done in lab environments [2]. MEMS technology can be used to miniaturize non-electrical components. This enables further system shrinkage and increased function density.

1.1 The world of MEMS

With the growing knowledge of the processes associated with semiconductor fabrication the complexity of MEMS has also grown. The first Micro Electrical Mechanical Systems (MEMS) were designed using the then newly discovered piezoresistive effect. A MEMS strain gauge using the piezoresistive effect would have a much higher sensitivity than the available metal film strain gauges. This first design clearly depicts the difference in function between 'regular chips' with an electrical functionality and MEMS with an electrical (electrical measurement signal) and non-electrical function (measurement of mechanical deformation).

One of the first large volume applications of MEMS was the air pressure sensor installed by Ford in the mid 1970's [2]. Another early application of MEMS is the accelerometer used in car airbags. In 1979 Roylance et al. already published a process to batch-fabricate these sensors [3]. In the 1980's IBM showed that MEMS were necessary to achieve the required printing precision of ink jet printers. This mass volume application of MEMS made ink jet printing a main stream technology [4-6].

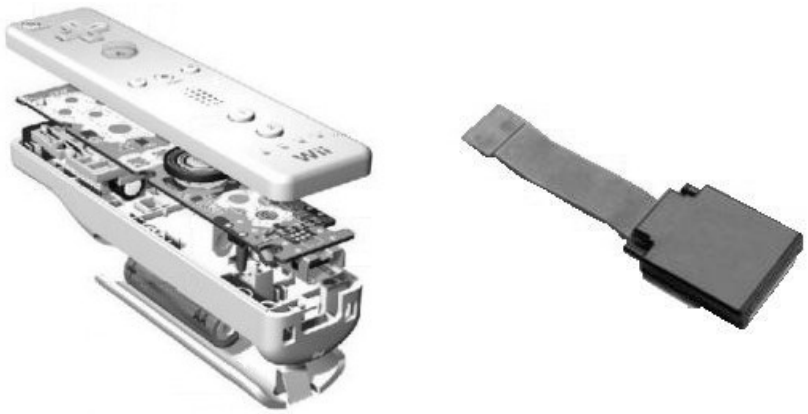


Figure 2 – Two MEMS applications (a Wii controller containing an accelerometer and a printer head with a micro pump)

Today's MEMS can be far more sophisticated and complex than the early MEMS due to the growing capabilities of the IC manufacturing processes and the multidisciplinary research in this field. Examples in everyday live are the MEMS accelerometers used in car airbags and the gyroscopes in the Wii

gaming system. The miniaturized gyroscopes allow all electronics, as depicted in Figure 2, to fit into a remote control sized controller.

Many mechanically oriented MEMS incorporate cavities to allow parts to vibrate or move. In such a cavity one for example places a small mass when building an accelerometer. The movement of this mass due to shocks can be measured thus giving an indication of the acceleration. Other moving parts can include: cantilevers, membranes and resonators. Cantilevers can be used in switching applications [7] or data storage applications. Membranes find applications in microfluidics and microphone applications. Finally, resonators [8] can be used as sensors for temperature [9], gas [10], particles [11], motion [12], pressure and in many other applications such as oscillators [13, 14] or several medical tasks [15].

MEMS come in a wide variety of shapes and sizes. Resonators for example are designed in simple shapes such as clamped-clamped beams [9, 13] and the clamped-free beams [11, 16]. Other variations include plates [13], free-free beams [13], dome-shaped resonators [16], suspended masses [9], tuning forks [7] and several other shapes [13, 14]. Figure 3 depicts several schematic resonator designs.

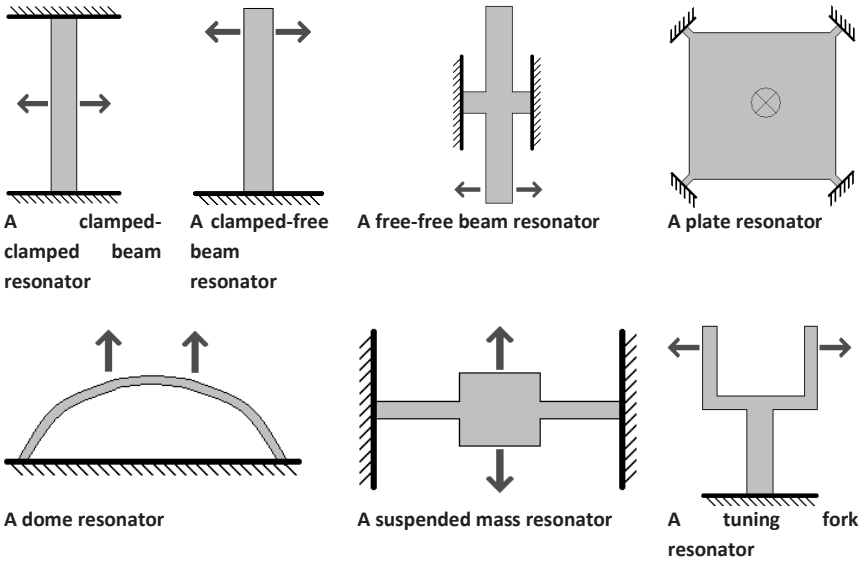


Figure 3 several schematic resonator designs

Other groups of MEMS are optical MEMS or MOEMS and the fluidic MEMS. Optical MEMS can for example function as an optical wave-splitter, wave guide [17], fibre coupler or scanning mirror [18, 19]. Fluidic MEMS have many application areas with examples such as micropumps [20], valves [21], micromixers [22] and lab-on-a-chip applications [23-26].

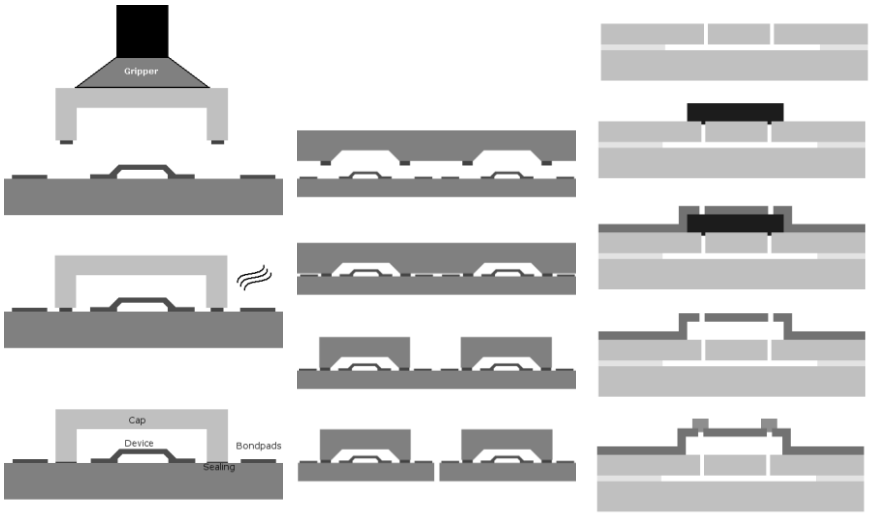
1.2 Types of WLTFP MEMS packages

This research focuses on the group of mechanical MEMS with cavities. In order to form a cavity several wafer level packaging options are available.

a) The solution inspired on traditional manufacturing and assembly would be the assembly of a single cap onto a single MEMS device. This cap would then be glued or soldered to form a (hermetic) seal protecting the die. This process is illustrated in Figure 4a. The main drawback of individual assembly of caps is the loss of the batch advantage typically associated with semiconductor manufacturing processes where all the dies on a wafer are processed at the same time. It also requires an assembly unit and by transporting the naked MEMS out of the wafer fabrication plant the MEMS might become contaminated.

b) Wafer to wafer bonding is a second option available to create a cavity. The wafer to wafer bonding process uses a secondary wafer with cavities etched into it. The cavities on this wafer are aligned with the MEMS devices and the two wafers are bonded together. After bonding the two wafers, they need to be diced to obtain the individual products [27].

c) The Wafer Level Thin Film Packages (WLTFP's) are a third group of packages suitable to encapsulate a bare MEMS device. The cap is fabricated using the lithographic techniques common in the semiconductor industry. One of the advantages of this packaging method is the low risk of contamination since the MEMS is sealed in the cleanroom. Other advantages are the batch creation of the packages and the small feature sizes that can be accomplished by means of semiconductor technology. A drawback is the fragile nature of the WLTFP's.



a) Local assembly of cap on top of a MEMS device **b) Wafer to wafer bonding** **c) Fabrication of a Wafer Level Thin Film Package**

Figure 4 – Three encapsulation methods for MEMS

The small feature sizes of a WLTFP compared to the other two techniques make it very attractive for extreme miniaturization. With a very flat WLTFP one can create silicon oscillators that are flatter than quartz crystals. This is beneficial in applications that demand very thin parts such as security cards, smart paper and electronics embedded in fabric for clothing.

1.3 Objectives and approach

The main objectives of this thesis are:

1. Investigate the failure modes and mechanisms of WLTFP's during assembly processes.
2. Provide guidelines to MEMS designers in doing a first time right WLTFP design.

A combined experimental and numerical approach is used to reach these objectives. From an experimental point of view, the high risk assembly processes are indentified by investigating a large set of WLTFP's. From a numerical pint of view, numerical techniques are developed in order to calculate the stress and deformation levels on the WLTFP during the assembly processes. In more details, this thesis addresses the following topics:

- The elastic properties of (very) thin films are investigated since the miniature scale of the WLTFP might affect the mechanical properties of the used materials.

- The assembly flow for MEMS dies in plastic encapsulations is investigated and a ranking of the most hazardous assembly steps is made.

- The most critical assembly processes are investigated in more detail. Finite Element models exploring stress on the WLTFP during these processes are created. The processes are ranked based on the stresses found.

- The tape removal step in the wafer grinding process is investigated and the delamination process is modeled.

- A set of WLTFP's is designed, manufactured and tested. The failure rates of the 4-axes design set provides MEMS designers rules towards designing a robust WLTFP.

1.4 Outline of the thesis

Chapter 2 will explain the production processes typically associated with Wafer Level Thin Film Packages and the assembly process flow needed to produce a plastic encapsulated product. Chapter 3 will explain the need for co-design of the WLTFP together with the functional MEMS part. Chapter 4 will discuss the work done on the mechanics of (ultra) thin films, failure modes during the assembly of WLTFP's and the resulting challenges. Chapter 5 will discuss numerical models developed for WLTFP assembly. In chapter 6 the more detailed investigation regarding the wafer grinding process is discussed and chapter 7 discusses the development of guidelines for MEMS designers. Chapter 8 will discuss the results and list some recommendations.

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2. Production and processing of WLTFP MEMS

A WLTFP generally consists of the functional parts depicted in Figure 1. A sacrificial layer is used during production to create the thin film cap above the MEMS device. A number of plugs are used to seal the cavity (hermetically) and an optional scratch protection or reinforcement layer is used to protect the seal and strengthen the cap.

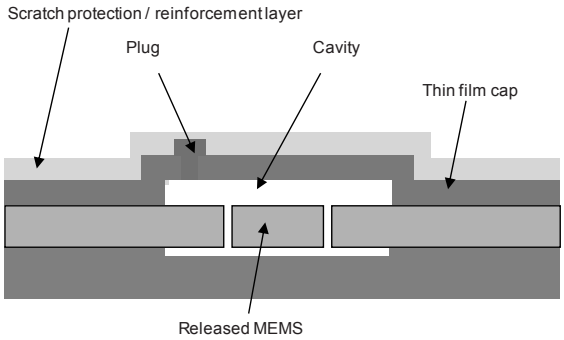

Figure 1 – A schematical representation of a WLTFP structure

This chapter summarizes the main wafer level processes used for production and the assembly of WLTFP's in a plastic package. The reader is referred to references [1-3] for further details.

2.1 Wafer level processing

In this paragraph a number of commonly used processes are described as they are used in many WLTFP production flows.

Doping, implantation and diffusion

Silicon as a semiconductor material is not conductive under 'normal' circumstances; introducing elements into the silicon lattice can make it electrically conductive locally. In general, elevated temperatures will increase the diffusion rate of substances. Therefore furnaces or local heat sources such as lasers are used a lot to diffuse components into the silicon.

Doping can be done by feeding the component into an oven using a gas flow and the component then diffuses into the silicon. The process is limited to suitable volatile components.

The implantation process also introduces a component into the silicon lattice but is using a different mechanism. The component is ionized and then accelerated using an electrical field, all under high vacuum. The resulting particle beam forces the ions into the silicon lattice. The density and depth can be controlled by the voltage and current. The silicon is usually annealed afterwards to release some stress that exists in the lattice due to the components that were forced into the base material.

Patterns

To create a useful structure instead of a stack of materials one needs patterns. Patterning is usually done using a photosensitive material. This material is spun onto a wafer providing a thin and equal layer on the wafer. This photosensitive material can then be changed locally using a light or an electron beam. When using light a wafer stepper uses a reticle and a stack of lenses projects an image of the pattern onto the photosensitive layer. This process is schematically depicted in Figure 2. In this process the feature size is limited by the wavelength of the used light source. This explains the evolution of wafer stepper light sources towards and into the UV domain. When using an electron beam instead of light a beam of electrons is used to modify the mask layer, this implies that every line has to be printed individually while the wafer stepper transfers the reticle image to the wafer in one exposure. This drawback can be reduced by using multiple beams [4]. The advantage is in the absence of the reticle, which needs to be made for every layer and is quite costly. This makes the electron beam method more flexible and suitable for small series.

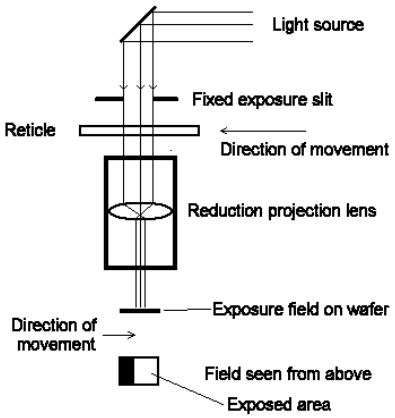

Figure 2 – Transfer of the reticle image onto the wafer

When the modification of the mask layer is finished an etchant is used to remove either the unchanged or the changed part of the layer providing a layer containing trenches suitable for deposition of a new layer in a specific pattern.

Deposition

Several deposition techniques are available, examples are sputtering and chemical vapor deposition (CVD).

In the sputtering process a solid target, made from the material that needs to be deposited, is bombarded by electrons breaking of particles from the target. These particles tend to deposit on all surfaces hence any wafer placed in the sputter chamber will have a thin layer of this material. The bombarding mechanism is sometimes also used as an etching method. Due to the high speed of the particles in the beam it serves as a very anisotropic etching process.

In chemical vapor deposition (CVD) a wafer is exposed to a precursor that decomposes or reacts with the substrate surface leaving behind the desired deposit. By-products and leftovers are transported out of the reaction chamber by a flowing gas. Commonly used is the Low Pressure CVD (LPCVD) where subatmospheric pressures are used to reduce unwanted gas reactions and improve the deposition quality. Plasma Enhanced CVD (PECVD) is used when lower temperatures in manufacturing are necessary. The plasma formed using either a DC current or microwave excitation improves the reactions of the precursors. Figure 3 schematically depicts the PECVD process setup.

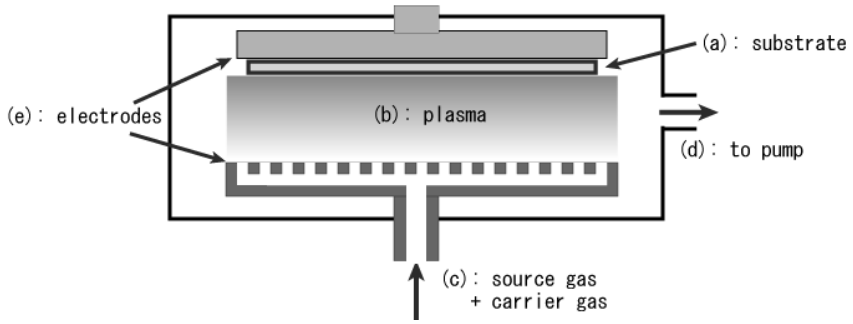

Figure 3 – A PECVD process setup

Etching

Etching is used to remove unwanted material from the wafer or deposited layers. Etching processes can be divided in isotropic and anisotropic groups. Isotropic etching removes an equal amount of material in each direction while anisotropic etching removes different amounts of materials in different directions. Key characteristics of the etching process are selectivity (which materials are attacked), etching rate(s) and/or isotropy. This is schematically explained in Figure 4.

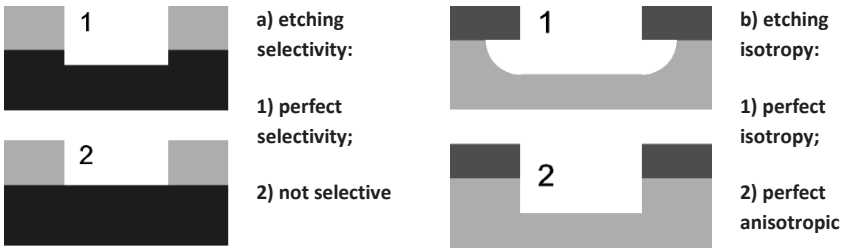

Figure 4 - Etching selectivity and isotropy

Process flows

In real products the processes from the previous section are repeated many times to create the final product. Figure 5 provides an example production flow of a WLTFP used to encapsulate a beam like structure that could be used as a resonator. First a sacrificial layer is deposited on top of the wafer. Then a hole is etched in this sacrificial layer allowing the third layer, made of silicon nitride to contact the wafer. The fourth step is to create an etching hole in the silicon nitride layer and to remove the sacrificial layer. Finally another layer of silicon nitride is deposited to seal the etching holes and reinforce the first silicon nitride layer.

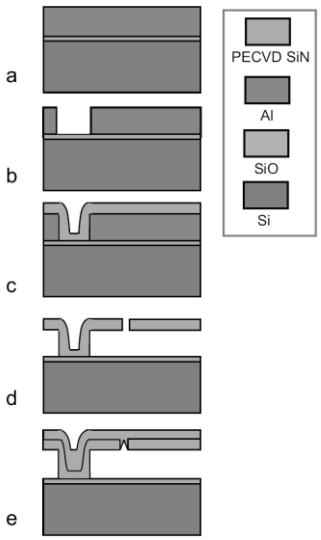

Figure 5 – Fabrication process; a) Sacrificial layer deposition. b) Trench etching defining columns. c) Capping layer deposition. d) Etching of the access holes and sacrificial etching. e) Sealing layer deposition

Many wafer level thin film package process flows have been developed and are under development for usage in many different applications with specific demands regarding, cavity pressure, size, hermiticity and allowable temperatures. Examples of process flows can be found in references [5-12].

2.2 Assembly of WLTFP MEMS

After production, assembly is the next step for the resonator. As mentioned in chapter 1 this research focuses on packaging resonators in plastic moulded packages. A typical assembly flow for such package types is depicted in Figure 6 [13, 14].

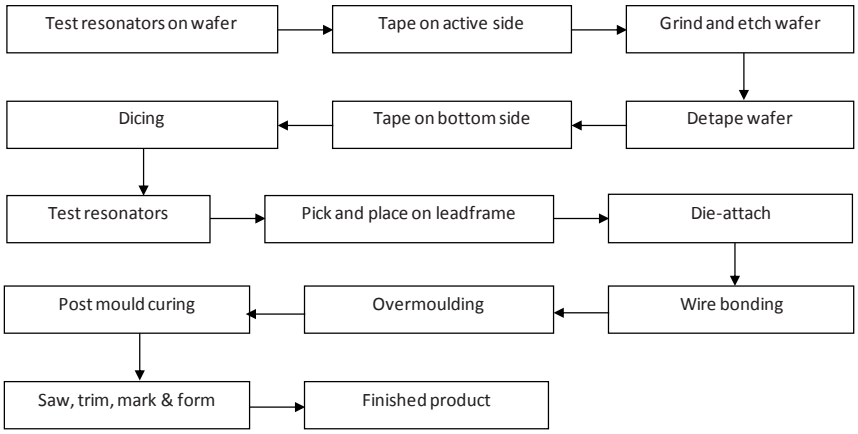

Figure 6 – Assembly flow diagram of a plastic overmoulded package

Each step in the assembly process imposes different types of mechanical loading on the WLTFP. Loading mechanisms that occur during these steps are discussed in the following subsections.

Wafer thinning

Wafer thinning is needed to thin the dies to a thickness that fits into the final package. A typical process starts with the application of a polymer tape to the side of the wafer containing the MEMS. The tape is used to position and secure the wafer to the grinding machine in order to manipulate it during the grinding process. This is depicted in Figure 7.

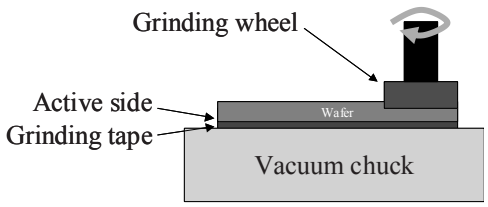

Figure 7 - A schematical depiction of a grinding setup

After the grinding step the wafer undergoes an etching step to increase the strength of the die [15]. The etching step removes the sharp features left by the abrasive particles in the grinding wheel.

Before the wafer can be separated into single dies the tape used in the earlier processes needs to be removed. The polymer tape is either cured to

reduce the adhesive forces and removed or directly removed. The tape removal process is depicted in Figure 8.

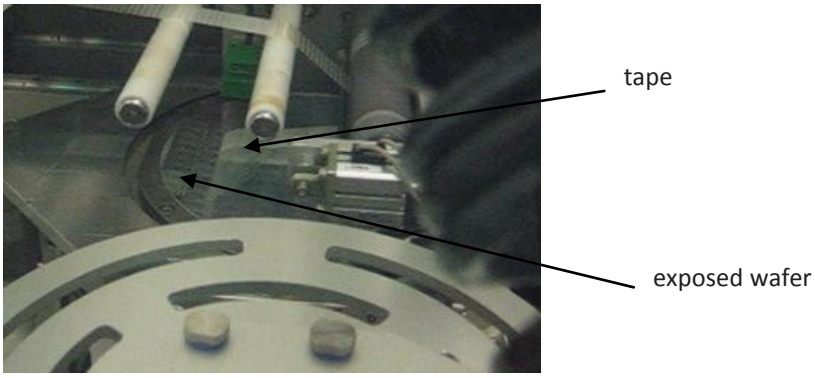

Figure 8 - The tape removal process

Dicing

The thinned wafer is again put on an adhesive foil but now the other way around. The grinded side is stuck to the tape exposing the side of the wafer containing the dies. The foil is used to keep the dies in place once they are singulated.

The most common singulation methods are scribe-and-break, diamond blade dicing, and laser dicing. With the scribe-and-break method cracks are initiated in the desired locations. When stretching the foil the cracks in the wafer progress through the bulk of the material and the dies are separated. Diamond blade dicing uses a thin, for example 40 µm, thick grinding wheel. A water jet is used to cool the wheel and remove the debris. Figure 9 is a schematic representation of the diamond blade dicing process.

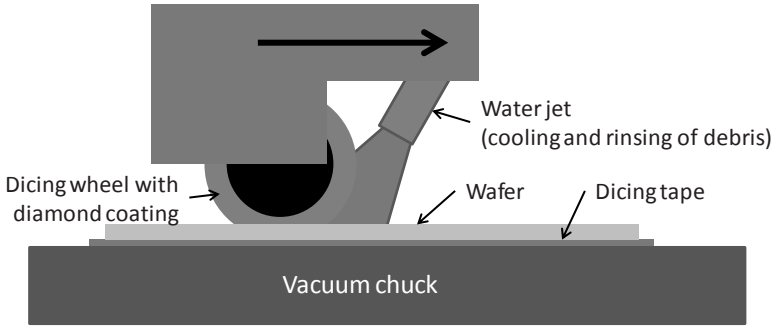

Figure 9 - Side view on a diamond dicing setup

Laser dicing can operate in several ways. One method is full material removal by means of laser ablation. Another method is the initiation of subsurface cracks using one or multiple beams, the wafer can then be broken into pieces [16].

Die attach

The singulated dies are put on a leadframe by means of a pick and place operation. Glue is used to secure the die to the leadframe and is cured after placement of the die. Figure 10 is a schematical depiction of the die attach process.

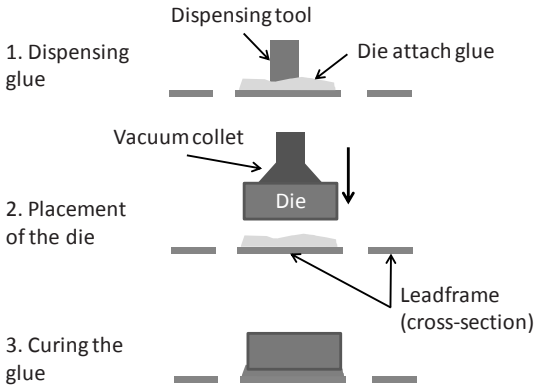

Figure 10 – A schematic depiction of the die attach process

For high power applications the die is sometimes soldered to the leadframe using a gold tin solder. When a flip chip process is used die placement is not necessary since the die will be soldered to the PCB.

Wirebonding

In the wirebonding process the metallic pads on the die are connected to a submount. This submount can be a metallic leadframe or a printed circuit board (PCB). This submount forms a connection between the outside world and the die. The connections between the metallic pads and the submount can be formed by wires or solder balls. Solder balls are used in flip chip technology where the active side of the chip is on the underside. Examples are flip chip ball grid arrays (FCBGA's). Figure 11 schematically depicts a flip chip construction.

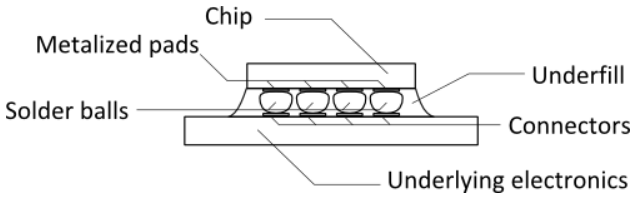

Figure 11 – A flip chip construction

Wire bonds are very common and can also be used to connect two dies in one package. Common materials for wirebonding are gold, copper [17] and aluminum [18]. Wire thicknesses are typically between 15 and several hundreds of micrometers. Figure 13 depicts an electronic product with golden bondwires.

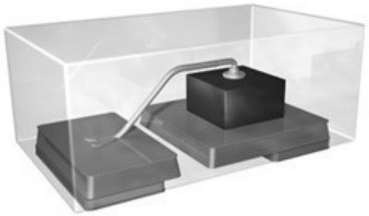

Figure 12 - An ultra thin leadless package with one bondwire (source: NXP)

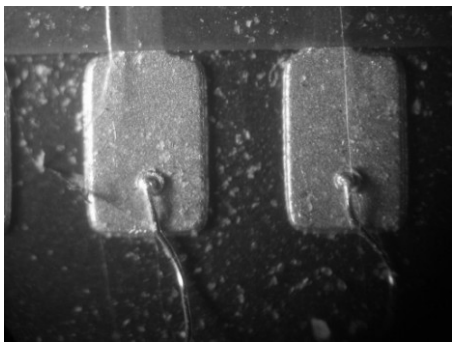

Figure 13 - Two golden bondpads with a ball bond and gold wire

Overmoulding

Once an electrical connection to the outside world has been realized using either wirebonding or a flip chip construction the die needs to be protected. In low cost solutions the die is protected by means of an epoxy moulding compound (EMC). This process is called overmoulding and utilizes an injection moulding setup. The leadframes or PCB's are loaded into a mould that covers the parts that need to stay clean. The free space in the mould is filled with hot EMC forming a plastic part around the chip and wires. An example is depicted in Figure 14.

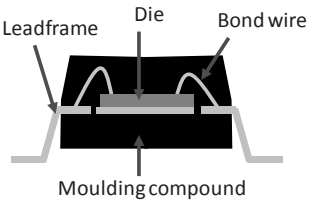

Figure 14 - A cross-section of a completed product

The injection pressure is around 80 bars and the typical plastic temperature is around 175 °C. After this process the overmoulded chips are baked in a oven, the so-called curing step, to change the structure of the EMC by increasing the amount of crosslinks in the polymer. During this process the EMC shrinks imposing a load on the die and leadframe [19].

Saw, trim, mark & form

When the strips are completed the packages need to be separated. The excess lead frame material is cut away. Also a text and/or a brand logo are applied and the leads are bend into the right shape if needed. Leadless packages or BGA's are sawn into separate pieces.

Figure 15 - a product with type number and brand

2.3 Summary

This chapter presented a condensed overview of basic semiconductor manufacturing processes. An overview of the main processes needed to package a (MEMS) die in a plastic package is also presented. Stress evolution during the assembly processes is discussed in chapter 5.

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3. The need for co-design of MEMS

This chapter discusses the need for an adapted development strategy in semiconductor development centers when changing over from the more main stream electronics-only semiconductors to MEMS, Nano Electrical Mechanical Systems (NEMS) or Micro Optical Electrical Mechanical System (MOEMS).

3.1 The need for Co-design

In the design process of a new MEMS device or a new version the process revolves around the intended function and the performance maximization of this function. After the design of the functional component, for example a resonator structure, the performance will be optimized by tweaking the electrical and mechanical design as well as the semiconductor processes used to fabricate this structure. To protect the MEMS a WLTFP is than designed providing a hermetic seal and protecting the device from outside influences. This WLTFP can be tweaked as well to optimize the device performance.

After the final chip design it will enter the back-end flow where an assembly plan is made and a suitable package type is chosen. During this phase prototypes will be fabricated to assess for example yield and device performance.

If the WLTFP is tuned for performance and little to no effort was invested in verifying the mechanical strength of the cavity it is likely problems will arise during assembly. Since performance tuning and cavity strength can require opposite adaptations of the design a first time right design is important [1, 2]. When a design is evaluated with respect to assembly and the yield is low due to mechanical weaknesses in the design this may end in a complete redesign of the device. The device performance and sealing have to be optimized again after a new WLTFP is designed which obviously is a laborious and time consuming task. This process is depicted in Figure 1.

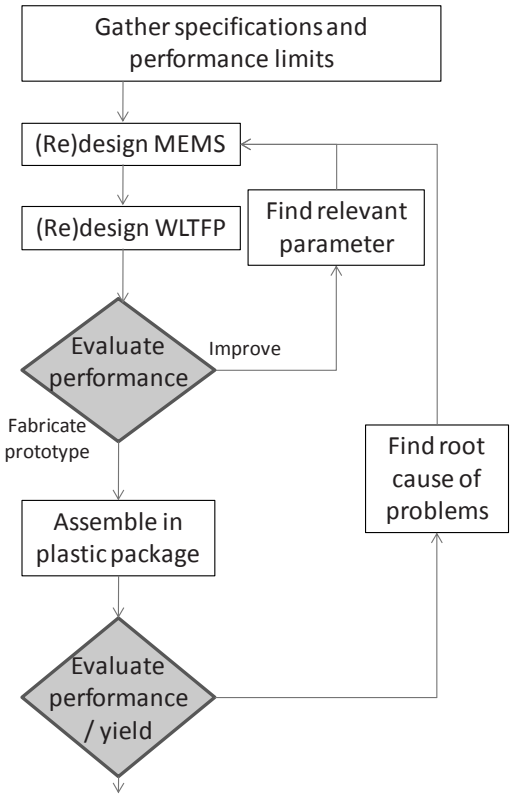

Figure 1 - Design flow of a MEMS WLTFP in a traditional sequential organization

To ensure a shorter time to market, less redesigns and less effort with respect to manufacturability the design of the die and WLTFP should not only be focused towards performance but also to manufacturability. This co-design of both function and package needs inputs from the manufacturing and assembly processes with respect to expected failure rates and preferred geometrical properties.

In the embodiment design phase as described in the book "Engineering Design" by Pahl and Beitz [3] it is important to look for constraints imposed by processes and loads further down the development chain. Pure electronic semiconductor products are less sensitive for some of the loads induced during assembly processes as described in chapter 2. Designing MEMS requires new design guidelines in the die design that account for the fragile nature of the MEMS.

MEMS come in a wide variety and require very different types of packaging in combination with very specific process requirements. For example: when building a structure like a resonator the stiffness of the final structure is determining the resonance frequency. If the curing of the plastic encapsulation deforms the MEMS die the device performance can start to drift. Considering the full manufacturing chain in the development phase will save money and time due to the reduction of prototyping/ramp-up issues.

Gathering the specifications and requirements on the product and processes is essential towards a quick and cost-effective product development cycle. The next paragraph will explain the influence of 'back-end processes' on the 'front-end' and the value of design guidelines.

3.2 Example

To illustrate the influence of the WLTFP and the back-end processes like the assembly a set of numerical simulations are performed. The simulations show the influence of stress on a resonance structure even though the structure was designed to be less susceptible to stress and deformations.

Figure 2 depicts a free-free dogbone shaped resonator and the two anchors it is connected to. The resonator is driven in resonance mode where it extends and contracts in plane. The driving force is applied by means of an electric field.

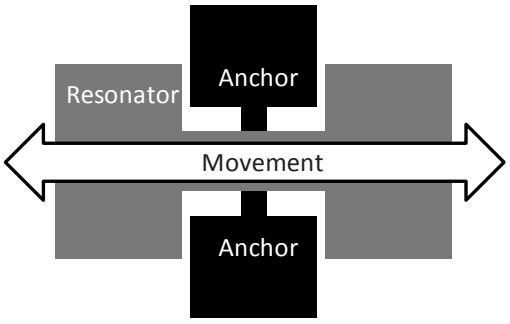

Figure 2 - top view of a 'dogbone' resonator

The finite element model is depicted in Figure 3. The path from the etch hole to the material furthest away is limiting the etching time. The holes and slot are built in to allow for shorter etching time by reducing the etching path length. The arrows indicate the applied boundary conditions, which are fixed

displacements. Along the x and z-axes the displacements are 0, the y-axis has a fixed displacement simulating chip warpage. The resonator is made of silicon (Young's modulus = 169 GPa; poisson ratio = 0.23). The model contains approximately 16000 8-noded 3D elements using the assumed strain formulation.

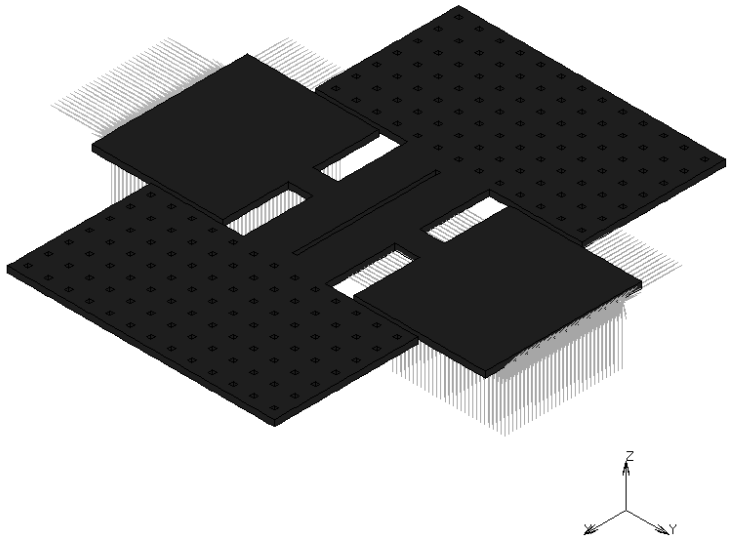

Figure 3 - Resonator model with boundary conditions

The finite element model is used to explore the influence of the surroundings on the resonator performance. The anchors are displaced representing a situation where the MEMS die would be warped due to external forces or stress induced by a thermal mismatch.

The simulations are composed of the following steps:

- A static calculation with anchor displacements to determine the pre stress in the structure
- Modal analysis to find all eigenmodes and associated eigenfrequencies.
- Extraction of the relevant eigenmode(s)

The static calculation consists of a gradual displacement of the anchors to the final position to calculate the pre-stress in the structure. Like a guitar string, that will produce a different frequency when the tension applied to it is

changed, the MEMS resonator frequency will change due to the pretension. Figure 4 and Figure 5 depict the resonator structure after displacement of the anchors. In Figure 4 the anchors were moved towards each other until the slot was completely closed. The color gradients in Figure 4 visualize the out of plane (z-axis) deformations in the structure.

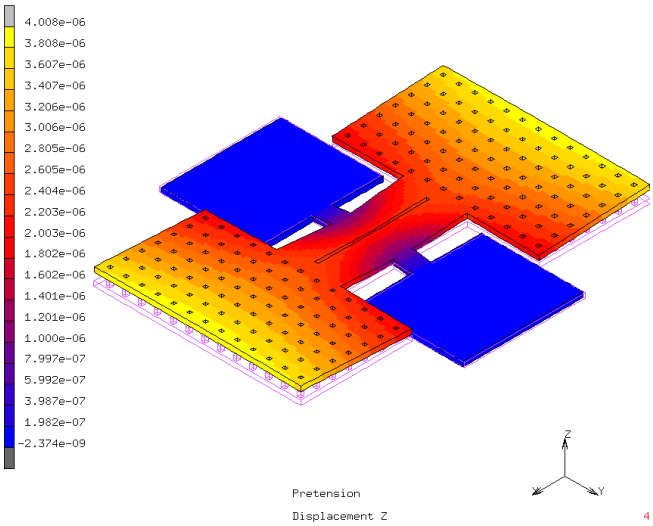

Figure 4 - a deformation plot for a resonator with anchors moving towards each other

In Figure 5 the anchors are pulled apart resulting in the opening of the slot used for etching. The displacements are exaggerated with a factor 10. The color gradients in Figure 5 show the displacements along the movement (y-axis) direction of the anchors.

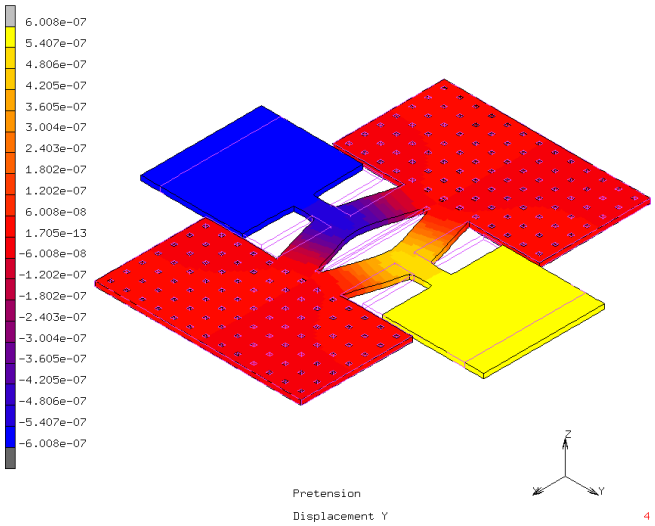

Figure 5 - a (scaled) deformation plot of a resonator with the anchors pulled away

In Figure 6 the change in eigenfrequency as a function of anchor displacement is depicted. When the anchors were pushed inward, towards each other (Figure 4), mixing of both in plane (x/y-direction) and out of plane (z-axis) modes was observed. The eigenfrequency found in the neutral situation is still present at a slightly different frequency but is mixed with an out of plane 'flapping'-mode.

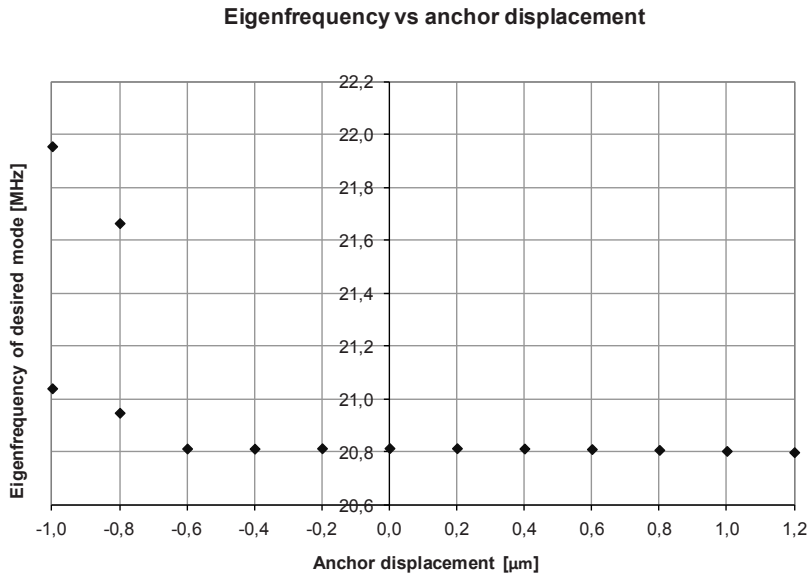

Figure 6 - Anchor displacement versus eigenfrequency (minus sign is movement of the anchors towards each other, plus sign is pulling apart of the anchors)

In Table 1 the results are listed together with the percentual shift of the eigenfrequency with respect to the zero displacement situation.

Table 1 - Eigenfrequency and percentual shift vs. anchor displacement

Displacement [µm]	Eigenfrequentie [MHz]	Difference from neutral
-1,0	21,96	54,9‰
	21,04	10,9‰
-0,8	21,66	40,9‰
	20,95	6,4‰
-0,6	20,81	-0,1‰
-0,4	20,81	-0,1‰
-0,2	20,81	0,0‰
0	20,81	-
0,2	20,81	-0,0‰
0,4	20,81	-0,1‰
0,6	20,81	-0,2‰
0,8	20,81	-0,3‰
1,0	20,80	-0,5‰
1,2	20,80	-0,7‰

When a resonator would be used as a quartz crystal replacement a frequency shift of the magnitudes in Table 1 wouldn't be acceptable. Digital clocks rely on a specified frequency and count pulses to determine the time. A change in resonance frequency due to stress or temperature would speed up or slow down the clock.

Displacements as listed in Table 1 can have two main sources:

- On die CTE mismatch; the on die CTE mismatch is caused by choice and layer thickness of the different materials used in the structure
- Packaging stress; the epoxy moulding compound used to package low cost plastic packages shrinks and can warp the die and leadframe combination. An example is depicted in Figure 7 (deformations amplified 10 times).

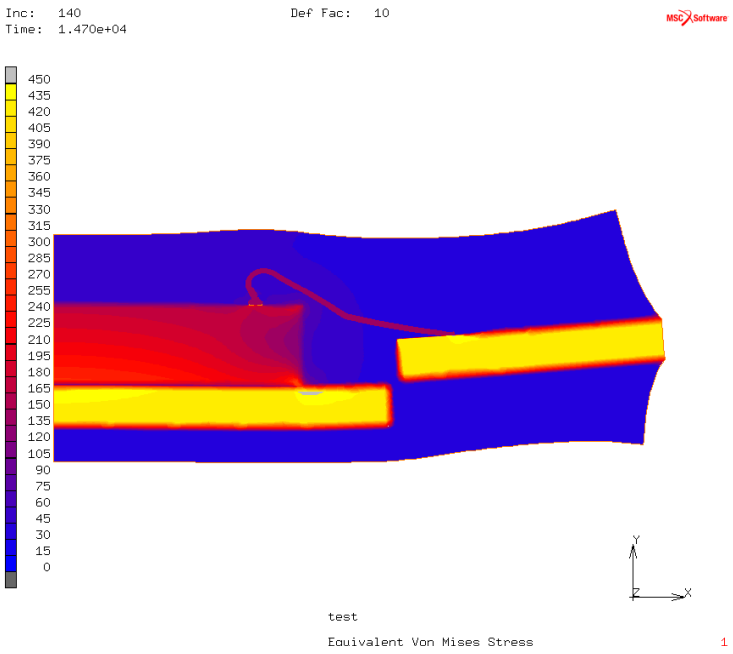

Figure 7 - Package deformations due to shrinking Epoxy Moulding Compounds (EMC)

In Figure 7 a thick die was used, when making very thin packages for integration in flexible substrates, bank cards and such a thinner die is required.

Very thin dies are easier deformable and will therefore bend more under the stresses applied by the leadframe and EMC.

Creating a robust WLTFP design that makes the structure less sensitive to these influences can enhance the functionality and accuracy of the actual device itself and raise the value and applicability of the product.

Chapter 7 will introduce a design of experiments exploring important design choices during the design of the component and the WLTFP.

3.3 Summary

This chapter illustrates and explains the need for co-design of (WLTFP) MEMS. Taking the full production and assembly chain into account during the design phase is critical in reaching a cost effective product development and fast time to market. The example illustrates that for MEMS all interfaces are of vital importance and that the assembly can significantly influence the functionality.

3.4 References

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4. The reliability of WLTFP MEMS

When making reliability predictions numerical methods can be very beneficial. Accurate predictions rely on known good input data, such as materials, geometry and environmental parameters. With the shrinking feature sizes of MEMS and microelectronics it is important to investigate the material properties, accurate material properties are essential for numerical models. Failure analysis also relies on accurate material models. The first section describes an investigation into the mechanics of thin films and the influence of layer thickness. The second paragraph briefly discuses several failures modes that can encounter during the manufacturing of MEMS with freestanding layers. The third section illustrates failures modes during assembly and explains the main stressors.

4.1 The mechanics of thin films[1]

During the manufacturing of MEMS a stack of thin layers is constructed. Depending on the function one needs conductive parts, sealing layers and many other layers such as insulation, diffusion barriers and structural capping layers. The thickness of these layers is usually in the sub millimeter range. Recent studies, both experimental [2-7] and theoretical [4, 8-11], have shown and predicted that mechanical and material properties such as Young's modulus and yield stress become noticeable functions of size on the micro- and nanometer scale. This is also known as the size-effect [12, 13]. Characterization of the material and mechanical response at device level is crucial for reliable and predictable performance of electro-mechanical systems [12, 14-17]. Therefore, great interest exists with respect to the effects of size on the material properties.

Performing accurate nanoscale experiments to determine material properties is not trivial [12, 17-19]. This is shown by the large variation in experimental methods and scatter between measurements found in the literature [20].

[1] Poelma, R.H., Sadeghian, H., Noijen, S.P.M., Zaal, J. J. M., Zhang, G. Q., *A numerical experimental approach for characterizing the elastic properties of thin films: application of nanocantilevers.* Journal of Micromechanics and Microengineering, 2011. **21**(6): p. 065003.

Nano-indentation is a well-established technique for studying the mechanical properties of thin film materials [12, 17, 21, 22]. Nano-indenters equipped with a flat punch tip are employed for studying the mechanical response of small structures, such as nanodots and micropillars [23, 24]. However, nano-indentation can suffer from experimental uncertainties such as tip effect [3, 25], calibration [17, 25], estimation of indenter contact area [3, 17, 25], data interpretation [3, 17, 18] and substrate effects [3, 12, 21]. To avoid the substrate or indentation tip effects, the bulge testing technique [12] or the tensile testing technique can be employed [16, 26]. The bulge test consists of uniformly pressurizing one side of a freestanding membrane and recording the load deflection curve. Haque et al performed in situ nanometer scale tensile tests of a freestanding aluminum film with a MEMS-based experimental setup placed inside a transmission electron microscope [26]. The main advantage of the nano-indentation, bulge testing and tensile testing techniques is that these techniques provide the entire load–displacement (or stress–strain) response of the material. However, bulge and tensile testing of freestanding thin films becomes more challenging or unsuitable at nanoscale due to the increased difficulty in handling, specimen fabrication, deformation detection and force loading [27].

Mechanical resonance is another property that can be used to determine the stiffness of structures in non-contact mode [36]. It involves exciting the cantilevers into vibration at specific resonance frequencies. The resonance frequency depends on geometry, stiffness and the density of the cantilever. The oscillations can be induced by applying an ac voltage between the cantilever and the substrate [28]. Additionally, resonance frequencies can be acquired from the cantilever thermal noise spectra [29]. This measurement technique can easily be extended to bilayer cantilever systems. However, the difficulty remains in distinguishing between the frequency variations caused by the added mass of the thin film and the frequency variations caused by the variation in bending stiffness [30, 31]. Consequently, decoupling of stiffness and resonating mass is needed before the thin film Young's modulus can be determined from the resonance frequency of bilayer cantilevers.

Variations in experimental results and difficulties in experimental methods make accurately determining nanoscale properties a challenge. There are numerous materials in microsystems technology that have not yet been fully characterized on the nanometer scale. Furthermore, a complete fundamental

explanation for experimentally observed size-effects is still lacking. No simulations are yet available that can account for all the small-scale effects. Consequently, a substantial gap between the computational prediction and experimental observation of the size-dependent Young's modulus of both metallic and semiconductor materials still exists [12, 13, 20].

Using the electrostatic pull-in instability (EPI) [5] of a MEMS structure one can determine the elastic properties of homogeneous thin films deposited on this structure. This approach is a highly accurate method for characterizing the size-dependent silicon Young's modulus down to 40 nm thickness [5]. It is mainly due to the well-known sharp instability point that allows for accurate measurements of the pull-in voltage V_{PI} of electrostatic actuated cantilevers [32]. Therefore the combination of accurate V_{PI} measurements, consistent structural design and calibrated models, can provide an accurate extraction of the thin film Young's modulus. As a case study and to provide new information, the copper Young's modulus is explored at the nanoscale (10–50 nm).

Fabrication and geometry characterization

Single crystal silicon cantilevers were fabricated on bonded (1 0 0) silicon on insulator (SOI) wafers with smart cut, see [5, 19] for details. The device layer is 340 nm thick low boron doped silicon on a 1.019 μm thick buried oxide (BOX) layer on a 525 μm thick silicon handle layer. The effect of doping on the elastic properties of silicon is well documented in [33]. The contribution of the impurities to the elastic constants appears to be small and is therefore ignored [33]. The device layer was patterned using photo lithography and afterward plasma etched. The buried oxide layer was sacrificially etched in hydrofluoric acid (HF 40%) to make the cantilevers free standing. The sacrificial etching resulted in a typical anchor point and undercut at the base of the cantilevers, as shown in Figure 1.

The effects of undercut and anchor point on the mechanical response of cantilevers are investigated in [34, 35]. The effects of undercut can be included into the cantilever effective length by adding a correction length of the undercut L_{uc} to the original cantilever length [34, 35]. The added length depends on the cantilever width, the etch time and the etch rate. Therefore, the cantilevers of similar width that were processed in a similar way, will have the same undercut. The cantilever correction lengths of the undercut were

measured by optical microscopy and by scanning electron microscopy from the cross-sections in previous work [5].

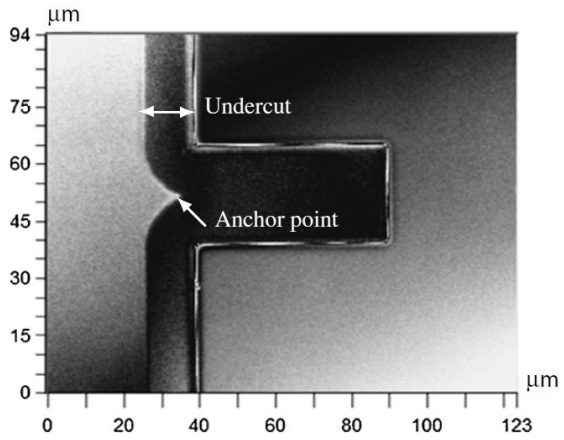


Figure 1 - White light interferometric measurement of a 50 µm long, 25 µm wide and 340 nm thick silicon cantilever. The cantilever is slightly transparent and therefore diffusion of light occurs making the undercut visible.

The length L of the fabricated cantilevers varies from 10 to 80 µm. The width b varies from 8 to 25 µm and the thickness t_{Si} is 340 nm. The thickness was measured by ellipsometry [45]. Paddle cantilevers were also fabricated. The width of the neck of the paddle cantilevers is 8 µm and the paddle itself is 16 µm×16 µm. Figure 2 shows the paddle cantilevers under the optical microscope; the dark shadows are the two probe needles.

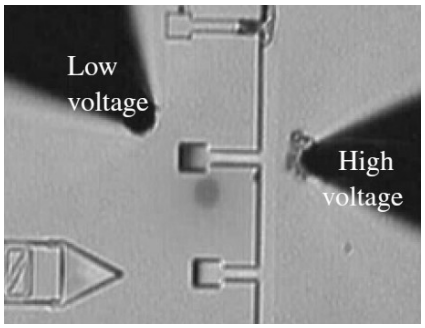


Figure 2 - Paddle Optical microscope picture of a 340 nm thick silicon paddle cantilever with a 50 nm thick copper film.

The material properties of the 340 nm thick single crystal silicon cantilevers are well defined [5, 19]. copper films of 10 and 50 nm thickness were deposited with physical vapor deposition (PVD) using a Leybold Heraeus Z550. Prior to copper deposition, the chamber was evacuated to a base pressure of 1×10^{-6} mbar to avoid ambient contamination. The copper deposition rate was about 0.1A° s^{-1} and the thickness of the film was measured during deposition using a resonant piezoelectric crystal and confirmed with WLI. The thin films were tested in the as-received condition and the average grain size of copper sputtered films is assumed to be below 140 nm [36]. Atomic force microscopy (AFM) measurement of the 340 nm thick silicon device layer revealed a smooth surface with a root mean square (RMS) roughness of 0.095 nm [5]. The RMS surface roughness of the 50 nm copper film was about 1.3 nm and the RMS surface roughness of the 10 nm film was about 0.9 nm.

White light interferometric measurements were performed with a Wyko NT3300 optical profiler. White light interferometric measurements were used to acquire the cantilever geometry and pre-bending before and after copper deposition. In Figure 3, a reconstructed 2D image from a WLI measurement of a cantilever after copper deposition is shown.

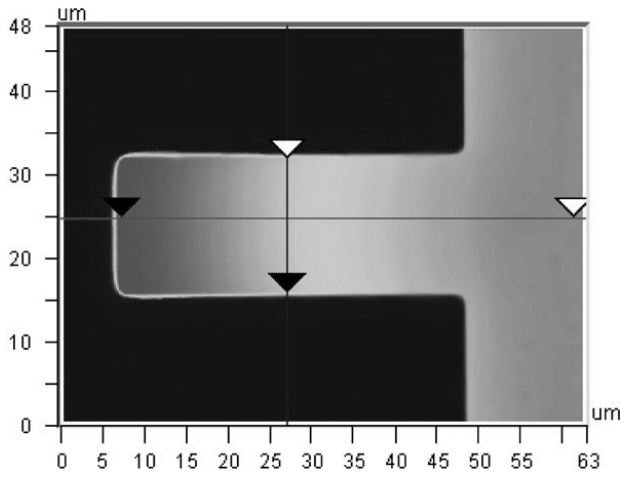
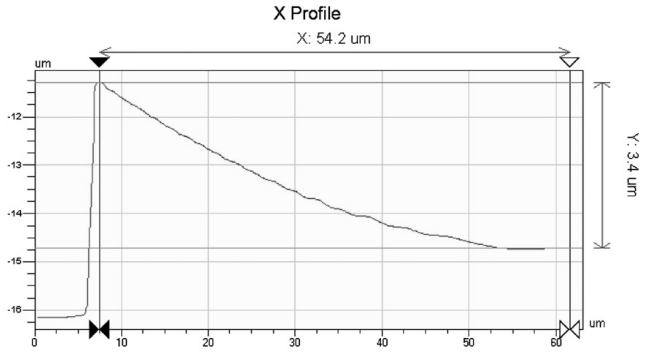


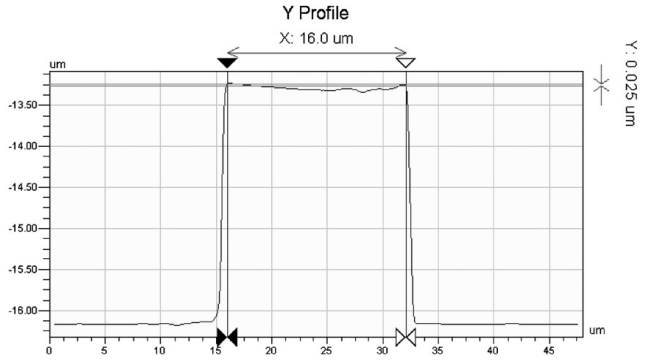
Figure 3 - WLI measurement showing the top view of a 340 nm

The red profile line in Figure 3 measures the out of plane distance of the cantilever along the length, as shown in Figure 4. The color map in Figure 3

and profile measurements in Figure 4 clearly indicate that the cantilever is bent upward after copper deposition.



a) A profile scan along the protruding direction



b) A profile scan along the width

Figure 4 - Profile scan of the pre-bending of the cantilever in Figure 3

Figure 5 shows the out of plane cantilever profiles for several different cantilever lengths, before and after copper deposition. The profile scans in Figure 5 reveal that the cantilever curvature seems slightly dependent on the cantilever length but strongly dependent on the copper film thickness. The curvatures are extracted by least squares fitting a circle to the measurement data, as described elsewhere [37].

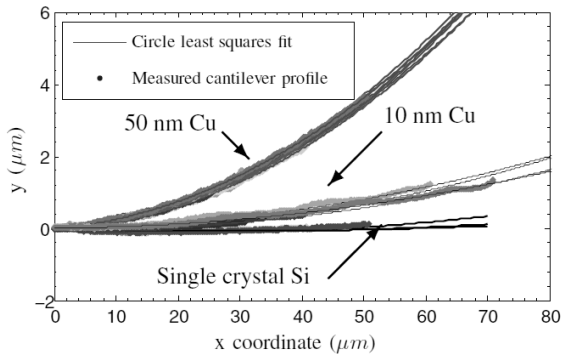


Figure 5 - Profile scans of single crystal silicon cantilevers and bilayer copper/silicon cantilevers of different lengths. Each profile scan consists of 736 data points and is least square (LSQ) fitted to a part of a circle.

The radii of curvature ρ of 20, 30 and 40 µm long cantilevers after 50 nm copper deposition are 383.8 µm, 413.0 µm and 449.7 µm, respectively. The curvatures for other cantilever configurations are given in Table 3 and Table 4. The cantilever pre-bending measured by WLI is used in both the analytical and finite element model to improve the accuracy.

Experimental setup

An experiment is used to obtain the V_{PI}-values that are used to calculate the thin layer properties. Figure 6 shows a schematic illustration of the experiment.

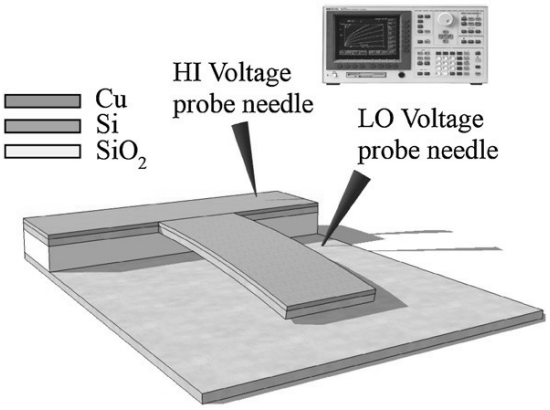


Figure 6 - Schematic illustration of the experimental setup showing a bent freestanding bilayer Si/Cu cantilever separated by an electrically insulating SiO2 layer from the silicon substrate. Two probe needles are used to apply a voltage V, one probe connects to the substrate, while the other connects to the device layer.

The pull-in instability point is determined by applying a voltage between the cantilever and the substrate and slowly increasing the voltage until the system shifts from a stable to an unstable equilibrium. The voltage that corresponds to the sharp instability point is called the pull-in voltage V_{PI} [5, 32]. Here, the force generated by the bending of the cantilever becomes smaller than the electrostatic force generated by the potential difference and a small disturbance will make the cantilever snap toward the substrate. This instantaneous collapse is called the electrostatic pull-in instability of the cantilever and is observed under an optical microscope as shown in Figure 7.

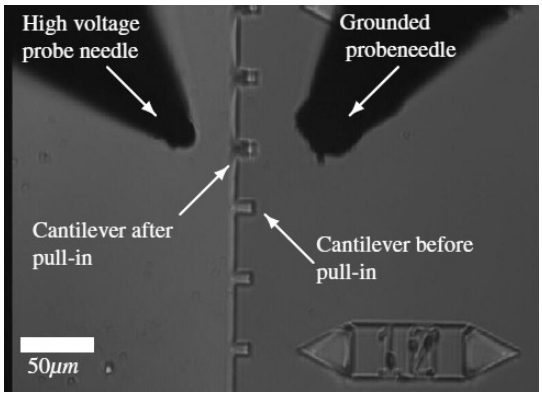


Figure 7- Optical image showing the pull-in of the top three rectangular cantilevers observed by the darker color. The bottom three are still freestanding due to their shorter length which corresponds to a higher V_{PI}. From bottom to top the cantilever length increases by 1 μm per cantilever. The discoloration of the cantilevers from light to dark is instantaneous when V_{PI} is reached.

Electrostatic pull-in instability is also confirmed by measuring the current I with a parameter analyzer as was indicated in Figure 6. When pull-in occurs, the cantilever short-circuits with the substrate and a sudden rise in current is measured.

The electrostatic attraction is generated by the applied potential difference and acts as a distributed load along the length of the cantilever. The electrostatic pressure is a highly nonlinear function of the applied voltage V and the gap between the cantilever and the substrate [37, 38]. Therefore, it is important to take into account the initial cantilever deflection because it strongly affects the pull-in voltage.

The electrostatic pull-in experiments were performed with a Cascade Microtech probe station in combination with a Hewlett Packard HP4156B semiconductor parameter analyzer to apply a controllable voltage to the freestanding cantilevers. A V–I measurement is shown in Figure 8.

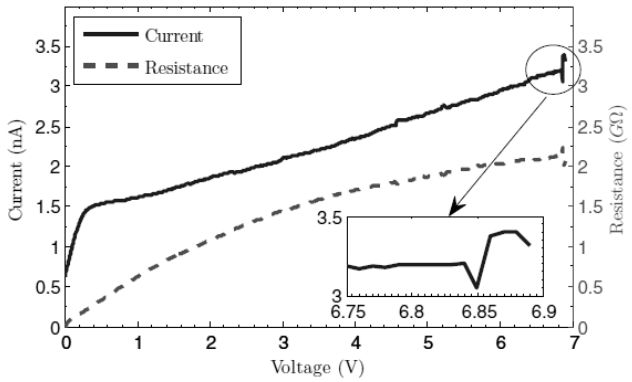


Figure 8 – V–I measurement. Pull-in instability is indicated by the small vertical peak in the measured current and resistance.

At 6.85 V, a sharp vertical disturbance in the measured current versus applied voltage is seen. At this point, short circuit between the cantilever and the substrate occurred. If the voltage is increased slowly, short circuit almost immediately occurs after V_{PI} is reached. The electrostatic pull-in voltages of several single-crystal silicon cantilevers and bilayer copper/silicon cantilevers with 10 and 50 nm thick copper films were measured. The results are summarized in Table 3 and Table 4 on page 18. In the modeling section, an electro-mechanical model is used to extract the Young's moduli of the thin copper films from the measured pull-in voltages.

Modeling the experiment

A schematic illustration of the electrostatic actuated bilayer cantilever model is shown in figure 9. Its electro-mechanical behavior can be described by Equation 1.

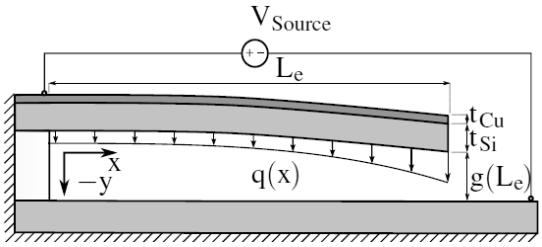


Figure 9 - Schematic side view of a bilayer system where the cantilever bends due to the electrostatic attraction q(x). The parameters t_{Cu}, t_{Si}, L_e, $g(L_e)$ and V_{Source} indicate the copper film thickness, silicon cantilever thickness, cantilever effective length, gap between the tip and the substrate and the applied voltage, respectively.

$$\tilde{E}\,\tilde{I}\frac{\partial^4 w}{\partial x^4} = q(x) \qquad \textbf{Equation 1}$$

In Equation 1 $\tilde{E}$ denotes the effective modulus, $\tilde{I}$ is the second moment of area, *w(x)* is the deflection of the cantilever and *q(x)* is the electrostatic attraction per unit length of the cantilever towards the substrate. Plane-strain conditions are assumed for wide beams (b ≥ 5t); hence, the effective modulus is given by Equation 2.

$$\tilde{E} = \frac{E}{1-\upsilon^2} \qquad \textbf{Equation 2}$$

In Equation 2, v and E denote the Poisson ratio and Young's modulus [32, 38]. In both the analytical and numerical models, the cantilever effective length is used. The cantilever effective length is expressed as $L_e = L+L_{uc}$, where L is the original cantilever length and L_{uc} is the correction length of the undercut. The correction length of the undercut can be calculated from the pull-in voltage measurement of the single crystal silicon cantilevers (without thin film), which have known geometric dimensions and known material properties.

The electrostatic attraction per unit length *q(x)* is derived from parallel plate capacitor theory [38] and modified with a first-order fringing field correction, in order to improve the accuracy for narrow beams [39]. Equation 3 then expresses the electrostatic attraction.

$$q(x) = \frac{-\varepsilon_0 \varepsilon b V^2}{2(g_0 + w(x))^2}\left(1 + 0.65\frac{g_0 + w(x)}{b}\right) \qquad \textbf{Equation 3}$$

V is the applied voltage, the other parameters used and their respective values are listed in Table 1.

Table 1 - Material and geometric parameters used for the pull-in simulation of cantilevers

Parameter	Description	Value
$\mathbf{E_{(1\,1\,0)}}$	Si Young's modulus	170 GPa
N	Si Poisson ratio	0.28
L	Cantilever length	8-50 µm

B	Cantilever thickness	340 nm
$\mathbf{t_{Si}}$	Device thickness	340 nm
$\mathbf{t_{SiO2}}$	BOX thickness	1019 nm
$\mathbf{g_0}$	Initial gap	1019 nm
$\boldsymbol{\varepsilon_0}$	Electric permittivity vacuum	8.8542 x 10^{-12} F m^{-1}
$\boldsymbol{\varepsilon_r}$	Relative permittivity air	1

It is shown in [5, 38] that by inclusion of Equation 3 in Equation 1 an unstable equilibrium is reached if $V \geq V_{PI}$.

Analytical approximation

The closed form for estimating the pull-in instability voltage VPI of curved cantilevers was derived in [40] and is given by equation (3). A small mathematical error was found in equation (43) in [40]; here the correct form is given in Equation 4.

$$V_{Pi} = \sqrt{\frac{\tilde{E}\tilde{I}}{\varepsilon_r \varepsilon_0 b} \times \frac{2\int_0^L \left(\phi''\right)^2 dx}{2\int_0^L \frac{\phi^2}{G^3} dx + 6C\int_0^L \frac{\phi^3}{G^4} dx + 12C^2 \int_0^L \frac{\phi^4}{G^5} dx}} \qquad \textbf{Equation 4}$$

The first natural cantilever mode shape ϕ (x) was used as the assumed deflection shape because it satisfies the boundary conditions and homogeneous part of the governing equation of a dynamic system [40]. G(x, ρ) describes the initial gap between a curved cantilever with radius ρ and the substrate. The coefficient C contains the integral terms that are constants defined by the geometrical parameters. They are given in [40]. Equation 4 is easily modified to account for a bilayer cantilever by substitution of the equation of effective bending rigidity as denoted in Equation 5.

$$\tilde{E}\tilde{I} = E_{Cu} I_{Cu} + E_{Si} I_{Si} \qquad \textbf{Equation 5}$$

In Equation 5 I_{Cu} and I_{Si} are the second moments of area of copper and silicon with respect to the neutral axis, derived by the parallel axis theorem. E_{Cu} and E_{Si} are the corresponding Young's moduli. One of the limitations of Equation 4 is that it does not account for variations in the measured deflection shape. Despite these limitations Equation 4 still provides valuable insights into

the parameter sensitivity of the pull-in voltage and the extracted thin film Young's modulus. In addition, the analytical equation allows a numerical model to find a faster solution by using it as an initial estimate.

Using the earlier mentioned curvature measurements the copper thin film stress can be extracted. The curvature of the cantilevers is caused by the thermal mismatch between the silicon and copper resulting in residual stresses after processing [41, 42]. Therefore, thermal stresses can be accounted for by incorporating the initial measured curvature of the cantilever into an elasticity model. Let us consider a strain mismatch $\Delta\varepsilon_0$ between the thin copper film and the silicon cantilever before any mechanical relaxation occurs. In the thin film approximation ($t_{film}/t_{substrate} \leq 0.01$ for an error < 5%) [43], the average stress in the copper film can be calculated using Equation 6.

$$\sigma_{Cu} \approx E_{Cu}\Delta\varepsilon_0 \qquad \textbf{Equation 6}$$

The curvature K of the cantilever is related to the strain mismatch $\Delta\varepsilon_0$ of the bilayer system according to [43] and can be expressed as denoted in Equation 7.

$$K \approx \frac{1}{\rho} \approx \frac{6E_{Cu}t_{Cu}}{E_{Si}t_{Si}^2}\Delta\varepsilon_0 \qquad \textbf{Equation 7}$$

Introducing Equation 7 in Equation 5 results in Stoney's equation for thin film stress [44].

$$\sigma_{Cu} \approx \frac{E_{Si}t_{Si}^2}{6t_{Cu}}K \qquad \textbf{Equation 8}$$

The thickness ratio $\delta = t_{Cu} / t_{Si}$ of the fabricated bilayer copper/silicon cantilevers exceeds 1%. Therefore, the thin film approximation is no longer accurate and a correction factor $1/(1 + \delta)$ is multiplied with Stoney's equation [43]. This correction factor reduces the error of Equation 8 to less than 3% for thickness ratios as high as 3:10 [43]. In addition, knowledge of the thin film Young's modulus is not required. The extracted copper film stresses from the measured curvatures are plotted in Figure 10 against the cantilever lengths.

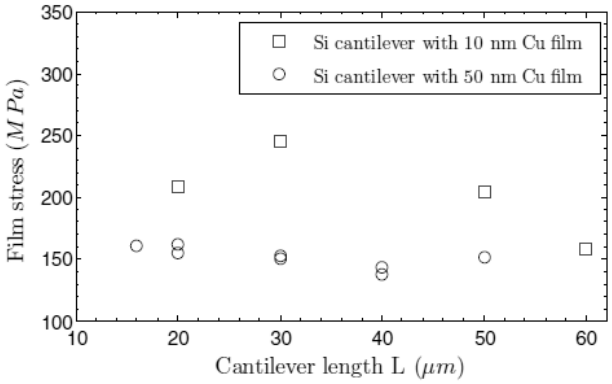


Figure 10 - Copper film stress versus the cantilever length for 50 and 10 nm thick copper films.

Figure 10 shows that the stress inside the 10 nm thick copper film is higher than in the 50 nm thick copper film. This agrees well with Stoney's equation where the thin film stress is inversely proportional to the film thickness, see Equation 8. Even though the cantilever curvature K is also dependent on the film thickness (it increases for increased film thickness, see Figure 5), its contribution was less.

Numerical approach

The electrostatic pull-in experiment was simulated using a 2D electro-mechanical coupled finite element model, which represents the geometry of the bilayer cantilever. A schematic illustration of the model geometry is shown in Figure 9. This model accounts for the highly nonlinear coupling between the mechanical and the electrical fields, the initial cantilever curvature and the variation in the film thickness.

The cantilever geometry was discretized using a sufficient number of eight node quadrilateral finite elements. Mesh refinement showed that the pull-in voltage converged within 0.5% with meshes finer than 140 elements. All cantilever meshes were based upon the measured profiles. In figure 11, a finite element mesh of a bilayer system, with a constant silicon cantilever thickness of t_{Si} = 340 nm and a varying copper film thickness of t_{Cu} = 50 nm, is shown.

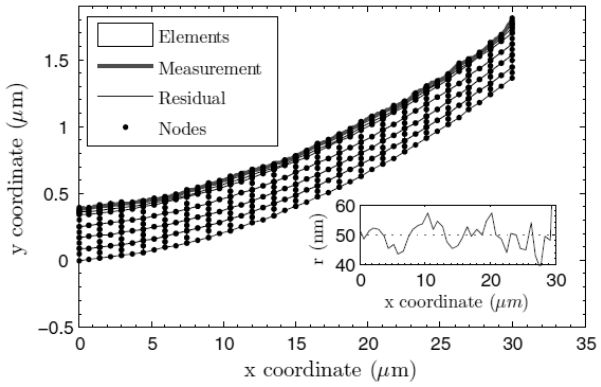


Figure 11 - Side view of the FE mesh of the bilayer cantilever based upon the measured profile; the residual (inset figure) shows the variation of the copper film thickness.

The variation in the copper film thickness was determined from the residual between the measured profile and its quadratic least-squares fit, see the inset in Figure 11. This assumption can be made because the roughness of the silicon cantilever samples was less than 0.1 nm, and was smoother when compared to the copper film roughness. Cubic spline interpolation was used to find the profile measurement values that correspond to the nodal x coordinates.

Plane strain elasticity was assumed for the simulation of bilayer cantilever pull-in. Furthermore, large deformation and a combined incremental iterative Newton Raphson (NR) scheme with logarithmically spaced voltage increments and a tolerance of 10^{-6} are used. Small voltage increments ΔV near V_{PI} are needed because the NR scheme only converges for stable equilibrium points. The pull-in voltage VPI of the model is determined by looking at the onset of numerical instability. When the applied voltage V approaches V_{PI}, the incremental stiffness of the cantilever system goes to zero and the system becomes unstable. The stiffness is defined as the slope between the applied voltage and tip displacement $w(L_e)$; the instability point is defined by Equation 9.

$$\frac{\partial V}{\partial w(L_e)} = 0 \qquad \textbf{Equation 9}$$

The pull-in voltage of the numerical model is regarded as the maximum voltage for which a converged solution exists. In figure 12, the tip

displacement versus applied voltage and the onset of numerical instability are shown and compared to the analytical approximation of V_{PI} (indicated by the straight vertical lines).

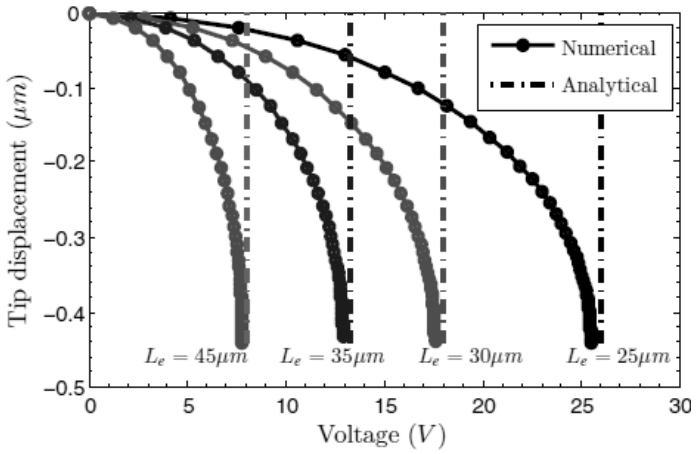


Figure 12 - Tip displacements of several initially straight cantilevers of different lengths versus the applied voltage. L_e is the cantilever effective length which takes into account the cantilever correction length of the undercut. The markers indicate converged solutions of the EM coupled FE model. These results are from the same cantilever configurations used inFigure 13.

It is shown that the voltage increments become very small near the instability point and that good agreement is found between the analytical and numerical models. In Figure 13, the numerical model is validated by comparing with the analytical approximation of equation (3), and pull-in voltage measurements taken from the literature [5].

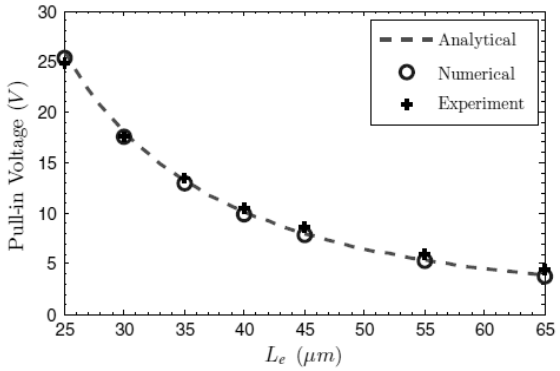


Figure 13 - Validation of the FE model with analytical theory and experimental results [5]. The single crystal silicon cantilevers of different lengths all have thicknesses of t_{Si} = 340 nm and widths of b = 8µm. The silicon (1 1 0) Young's modulus E = 170 GPa and Poisson ratio v = 0.28.

Figure 13 depicts the predicted and measured pull-in voltages V_{PI} of straight single crystal silicon cantilevers versus the cantilever length. Figure 13 shows good agreement between the analytical, numerical and experimental results for straight silicon cantilevers. For longer cantilevers, the measured pull-in voltage is slightly underestimated by both models for the given parameters. However, both model predictions remain in good agreement (<10%) with each other. Equation 4 is insufficiently accurate for curved and tilted cantilevers with a varying film thickness and possible large deformation. Therefore, a numerical approach was used for extracting the Young's modulus from the bilayer copper/silicon system. The copper film Young's modulus was extracted from the measured pull-in voltage by adjusting the copper film Young's modulus in the model until the pull-in voltage prediction matched the measured pull-in voltage. The results are discussed in the following section.

Results and discussion

A set of silicon cantilevers was measured and the corresponding Young's modulus was measured, the results are listed in Table 2.

Table 3 lists the measurement results for the ordinary cantilevers and Table 4 lists the results for the padded cantilevers. V_{PI} is the pull-in voltage; b is the width and L the length of the cantilever. L_{UC} is the length of the undercut and E is the extracted Young's modulus.

Table 2 - Measured V_{PI} and extracted Young's modulus *E* (110) Si cantilevers; t_{Si} = 57 nm

V_{PI}	b (μm)	L (μm)	L_{uc} (μm)	E (GPa)
7.78	8	10	5	98.8
6.85	8	11	5	103.5
6.78	8	12	5	105.5
5.65	8	13	5	103.4
5.10	8	14	5	100.0
Median				103.4
Relative standard deviation				± 2.7%

Table 3 - Measured V_{PI} and extracted copper Young's modulus E_{Cu} of bilayer cantilevers: t_{Si} = 340 nm and t_{Cu} = 10 nm

V_{PI}	b (μm)	L (μm)	L_{uc} (μm)	ρ(μm)	E (GPa)
7.84	20	60	9.5	2185.9	240
11.82	20	50	9.5	1688.0	1180
17.21	20	30	9.5	1410.6	1110
21.66	20	20	9.5	1658.6	265
5.95	25	50	4.0	-	880
9.14	25	40	4.0	-	815
Median				1736	748
Relative standard deviation				± 19%	± 54%

Table 4 - Measured V_{PI} and extracted copper Young's modulus E_{Cu} of bilayer cantilevers: t_{Si} = 340 nm and t_{Cu} = 50 nm

V_{PI}	b (μm)	L (μm)	L_{uc} (μm)	ρ(μm)	E (GPa)
30.80	16	40	10.8	449.7	90
36.10	16	30	10.8	413.0	65
47.48	16	20	10.8	383.8	120
26.16	8-16	50	10.2	409.4	95
26.36	8-16	40	10.2	431.5	115
28.66	8-16	30	10.2	406.7	100
39.44	8-16	20	10.2	398.5	120
55.30	8-16	16	10.2	385.4	105
Median				410	103
Relative standard deviation				± 5.4%	± 18%

Table 2 shows that the variation in silicon Young's modulus for different cantilever lengths is small (<3%). No significant curvature was observed, see

Figure 5. This proves that the Young's modulus can be extracted accurately from single crystal silicon cantilevers.

Table 3 shows a large variation of Young's moduli for different cantilever lengths (±54%); the radii of curvature measurements show a lower variation.

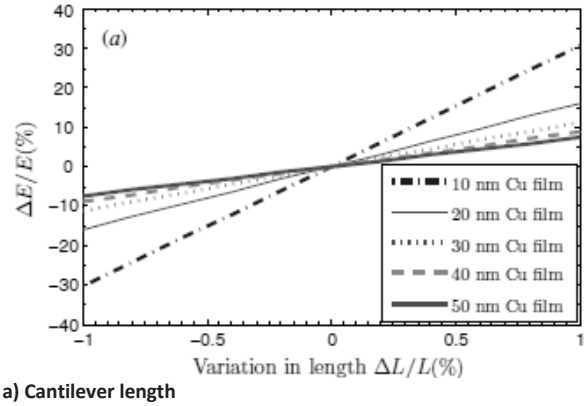
Table 4 shows that the variation of Young's modulus for a 50 nm thick copper film with in-plane dimensions is small compared to the 10 nm copper films of Table 3. In addition, the cantilever curvature measurements show that the measurement is consistent without much variation (±5.4%).

To address the variations in the extracted thin film Young's modulus a sensitivity analysis is performed. Equation 4 was used for the evaluation of the sensitivity of the thin film Young's modulus to uncertainties in dimensional parameters and voltage measurements. To evaluate the effects of uncertainties, small variations of ±1% are considered for the following dimensionless parameters: variation in the cantilever length $|\Delta L/L|$, variation in the film thickness $|\Delta t_{Cu}/t_{Cu}|$, variation in the curvature $|\Delta\rho/\rho|$ and variation in the voltage measurement $|\Delta V/V|$. The sensitivity analysis was performed for the reference cantilever configuration: t_{Si} = 340 nm, L = 30 µm and ρ = 400 µm. The copper film thicknesses are 10–50 nm. Figure 14 shows the sensitivity of the extracted thin film Young's modulus to variations in dimensional and measurement parameters.

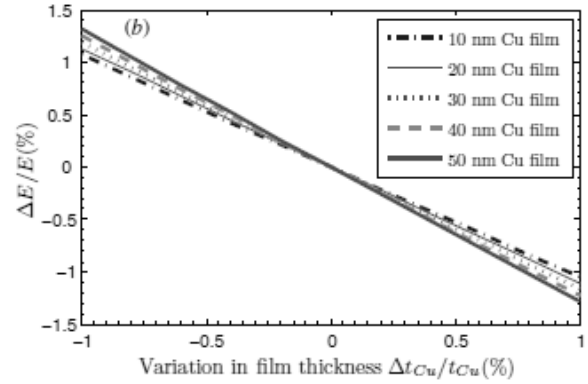
Equation 10 gives a linearized approximation of the cumulative error of the thin film Young's modulus for small variations in dimensional and measurement parameters. In the equation α, β, γ and δ are the sensitivity coefficients.

$$\Delta E/E = \alpha\,|\Delta L/L| + \beta\,|\Delta t_{Cu}/t_{Cu}| + \gamma\,|\Delta\rho/\rho| + \delta\,|\Delta V/V| \qquad \textbf{Equation 10}$$

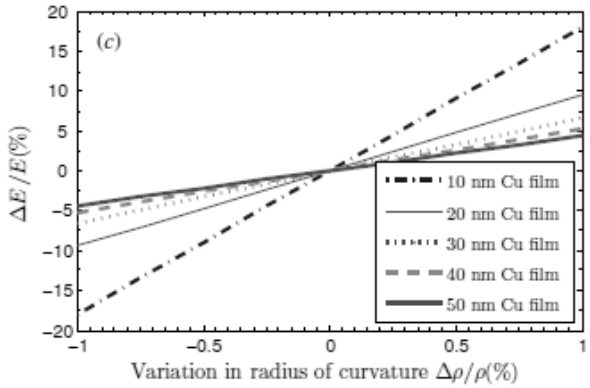
Figure 15 gives the sensitivity coefficients for increasing film to cantilever thickness ratios.



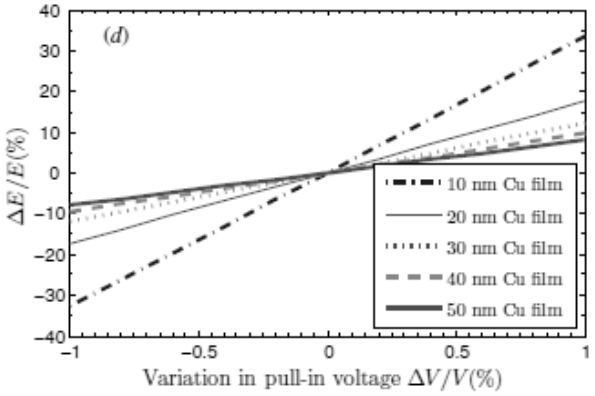
a) Cantilever length



b) copper film thickness



c) cantilever radius of curvature



d) voltage measurements

Figure 14 - Sensitivity of the extracted thin film Young's modulus to variations

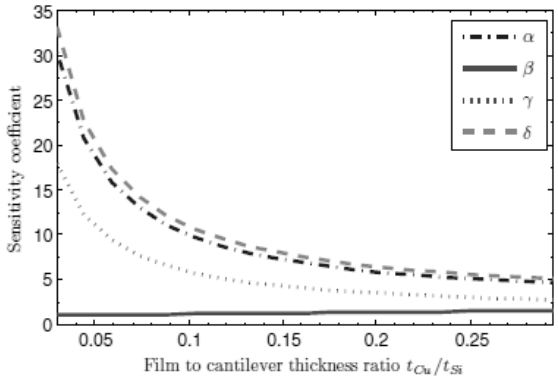


Figure 15 - The sensitivity coefficients for different film to cantilever thickness ratios. The cumulative error is defined by Equation 10

The error in the extracted thin film Young's modulus is very sensitive to measurement errors in the cantilever length, as shown in Figure 14a. Therefore, the length deviation introduced by the photo lithography process is used to examine the possible error in thin film Young's modulus. The length deviation ΔL due to processing inaccuracies is about 200–500 nm, which is roughly equal to ±1% of the cantilever length. This results in a possible thin film Young's modulus error of 30% and 7%, for the 10 and 50 nm films respectively. Therefore, it is also crucial to determine the correction length of the undercut accurately, since it can introduce a large systematical error in the extracted thin film Young's modulus when the film to cantilever thickness ratio

t_{Cu}/t_{Si} is low. Figure 14b shows the variation in the extracted thin film Young's modulus to measurement errors in the film thickness. The resolution of the resonant piezoelectric crystal that is used for the measurement of the film thickness during deposition is about 0.1 nm. This results in a possible thin film Young's modulus error of roughly 1% and 0.3%, for the 10 and 50 nm films, respectively. The cantilever radius of curvature determines the initial gap between the cantilever and the substrate and therefore the pull-in voltage. Figure 14c shows the sensitivity of the extracted thin film Young's modulus to the variation in the radius of curvature measurement. A measurement error of ±1% in the radius of curvature is assumed, which results in a thin film Young's modulus measurement error of 18% and 5% for the 10 and 50 nm films, respectively. Finally the influence of the pull-in voltage measurement error on the extracted thin film Young's modulus is shown in Figure 14d. The applied voltage is ramped up by 10 mV each step. Therefore, the accuracy of the pull-in voltage measurements is about ±10 mV, which results in a thin film Young's modulus measurement error of 0.8% and 0.2% for the 10 and 50 nm films, respectively. The total error in the extracted thin film Young's modulus is estimated at 50% and 13% for the 10 and the 50 nm thick copper films, respectively, which agrees well with the relative standard deviations of the measurements.

The experimental results in Table 3, for the ultra thin copper films of 10 nm thickness, were in a very sensitive regime where geometrical and measurement uncertainties might have played a significant role in the high relative standard deviation, as shown in Figure 15. Furthermore, it is clear that the sensitivity of this experimental method, to uncertainties or possible systematic errors, can easily be improved by increasing the film to cantilever thickness ratio t_{Cu}/t_{Si}.

Conclusions

The experiments show that EPI in combination with WLI can be used for characterization of the copper film Young's modulus and stress, in the 10–50 nm nanometer range. The method can be extended for characterizing other homogeneous thin film materials. The method is fast, practical, robust and requires a basic measurement setup such as a probe station, voltage source and a method to determine the cantilever initial curvature. It is furthermore concluded that:

- The copper Young's modulus increases from 103 ± 18% to 748 ± 54% GPa for a reduced film thickness of 50 and 10 nm, respectively. Even though large variations are present, it can be concluded that the effective copper Young's modulus is size dependent.
- The parameter sensitivity analysis shows that accurately determining the cantilever effective length, applied voltage and the initial gap between the curved cantilever and substrate is crucial. These parameters have a considerable influence on the extracted thin film effective Young's modulus for low film to cantilever thickness ratios t_{Cu}/t_{Si}. The measurement is least sensitive to variations in the film thickness.
- The effective Young's modulus and film stress can be determined more precisely when the film to cantilever thickness ratio t_{Cu}/t_{Si} increases.
- For the single crystalline silicon cantilevers of 57 nm thickness, a Young's modulus of 103.4 ± 2.7% GPa was measured, which closely matches the result 100 ± 10.8% GPa from [5]. This also confirms a size dependent silicon Young's modulus but more importantly shows the accurate reproducibility of the experiment. For bilayer cantilevers the reproducibility can be improved by increasing the film to cantilever thickness ratio.

As shown in [45], the size-effect becomes most dominant for layer thicknesses below a micrometer. This is important during Finite Element Analysis when one wants to simulate the (thermo-)mechanic response.

The presented measurement method for thin films can also be applied to other materials that can be deposited on the cantilevers, for example aluminum, a common material in MEMS manufacturing. In this study copper was chosen since a lot of literature is available for comparison of the results.

4.2 Failures modes during WLTFP production

This paragraph focuses on failures induced by the wafer fabrication processes introduced in section 2.1. During the production of WLTFP MEMS a number of problems can be encountered. Besides the standard issues in semiconductor manufacturing such as contamination and uneven layer thicknesses a number of issues can arise that jeopardize the WLTFP.

Like the actual MEMS device, the WLTFP is vulnerable to stiction as a result of for example etchant evaporation. The capillary forces of the decreasing fluid mass of etchant can pull the WLTFP layers downwards towards the device during drying [46]. Figure 16 depicts the pull down process leading to stiction.

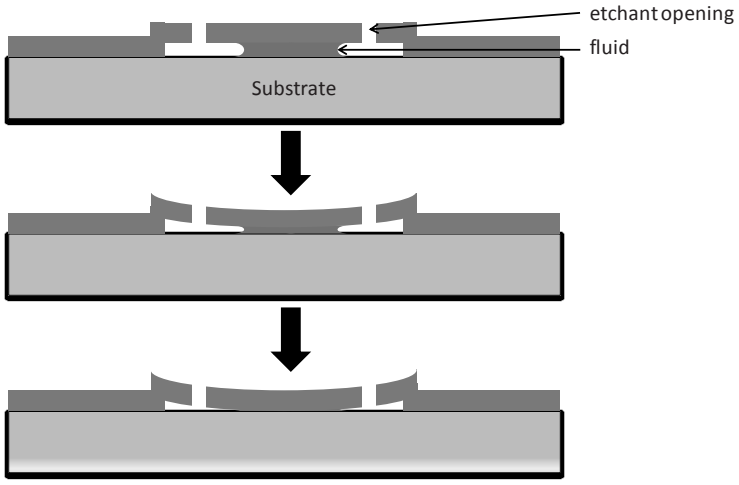


Figure 16 - Pull down of a WLTFP due to capillary forces during drying of the etchant

Another failure mode of WLTFP's, outgassing of the capping layers during lifetime, can be controlled by changing process settings. Li et al investigated the gas composition and determined that gas can come out of the investigated silicon nitride capping layer [47]. The gas in the cavity reduces the quality factor of the resonator effectively rendering it broken.

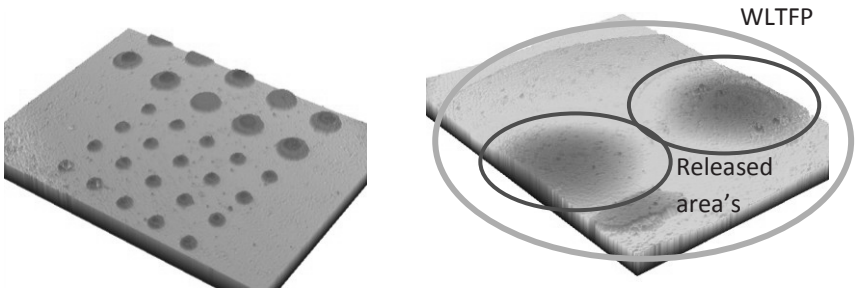
Handling of the wafer during production can also can issues due to the extremely fragile nature of the WLTFP's in production. The glassy nature of the WLTFP and the lack of support of this layer makes it prone to cracking due to contact with other objects or to excessive stress caused by for example a thermal expansion mismatch.

Finally the sealing process, for example sputtering of metals or deposition of silicon nitride can contaminate the cavity. The cavity pressure is equal to the process pressure imposing very strict limits on the process in order to get a good quality factor.

Further wafer level processing of the finalized WLTFP can be problematic when the sealing layer (for example aluminum) can easily melt at common process temperatures. Also outgassing can be accelerated at high temperatures. The temperature window after sealing the cavities will limit the choice in processes.

4.3 Failure modes during assembly

This paragraph focuses on failures induced by the assembly processes introduced in section 2.2. Failures induced during the creation of the wafer level thin film package such as stiction caused by the capillary forces of an etchant will not be investigated. In this study we focus on failure modes due to assembly processes. Some wafer fabrication processes however cannot be neglected in the evaluation of risks for the assembly processes. Everything that is influencing the stress-state of the thin film package can cause failure or weaken negative effects of the assembly processes. It is therefore important to estimate and control the stress-state of the cap. Scans were made on wafer level thin film packages containing no MEMS devices using a white light interferometer system, results are depicted in Figure 17.



a) several circular WLTFPs **b) partially released WLTFP buckling upwards**

Figure 17 - Scans of WLTFP geometry before assembly

From the buckling behavior found in Figure 17b one can deduce that the WLTFP is not stress-free and that this might affect the process yield during assembly. The buckling behavior is caused by the process-induced stress in combination with the thermal mismatch between the wafer and the capping material.

According to Roark the buckling stress of a circular clamped plate can be calculated using Equation 11. [48]

$$\sigma_{buckling} = 1.22 \frac{E}{1-\upsilon^2}\left(\frac{t}{r}\right)^2 \qquad \textbf{Equation 11}$$

In Equation 11 *E* is the Young's modulus, *v* is the poison ratio, *t* the layer thickness and *r* is the radius of the plate. The stress in the plate at room

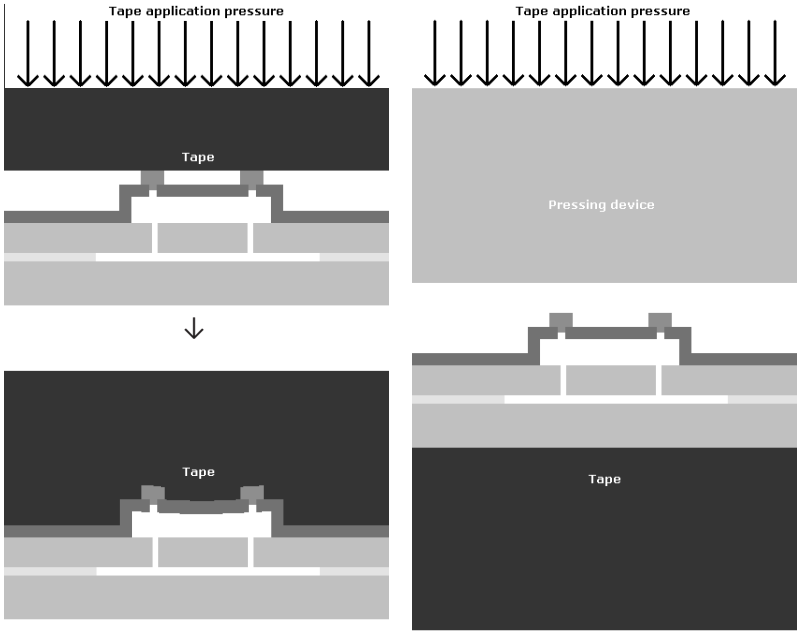
temperature can be calculated using the intrinsic stress in the capping layer in combination with the thermal stress. The thermal stress is caused by the mismatch in coefficient of thermal expansion in combination with the difference between processing temperature and usage or ambient temperature.

$$\sigma_{total} = \sigma_{\mathrm{int}rincsic} + E \cdot \left(\Delta CTE \cdot \Delta T\right) \qquad \textbf{Equation 12}$$

Depending on the stoichiometry of the silane / ammonia mixture compressive stresses of 400 MPa can be measured [49].

Tape (removal) damage

As described in earlier sections a tape is applied to the wafer several times during the entire assembly flow. The tape application process can damage the WLTFP due to the applied pressure needed to create a sufficient adhesive strength. When tape is applied to the WLTFP side of the wafer the tape will land on the WLTFP's sticking out above the surface and the application pressure will then force the tape to contact the remaining wafer surface. If tape is applied to the backside of the wafer one also needs to apply pressure to the wafer. Careful support to the WLTFP side of wafer is needed since the soft tape is on the other side. All objects or surfaces used to support or pressurize the tape will contact the WLTFP's first thereby creating high loads on the cap.

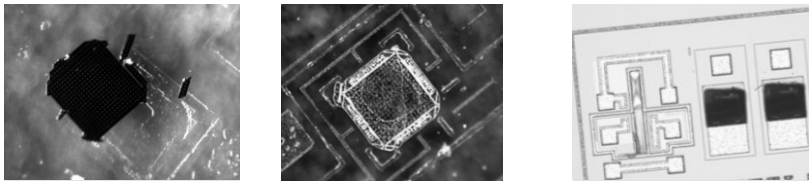


a) tape application to the active side **b) tape application to the back**

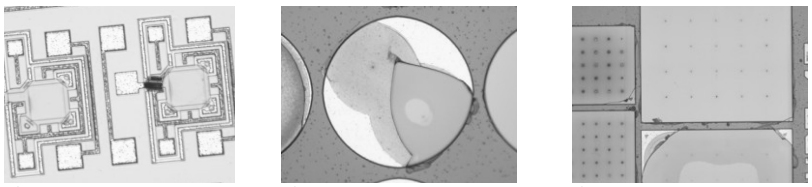
Figure 18 - Tape application to the front and backside of a wafer

Cap loading mechanisms during the tape application process are depicted in Figure 18. The tape removal process on the active side is hazardous since the adhesive forces will apply tensile forces on the WLTFP cap and plugs.

Damage due to backside tape application and damage due to tape application and removal on the active side are depicted in Figure 19.



a) cap sticking on the tape | b) resonator sticking on tape | c) cavity missing a cap



d) cavities missing caps | e) cap broken after dicing | f) missing caps after dicing

Figure 19 - Taping process damage

Dicing damage

The damage observed after the dicing process, depicted in Figure 19e & f, is not induced by the dicing blade since the damage found after dicing is evenly spread over the entire 10x10 mm^2 die.

An overview of a die after dicing is depicted in Figure 20. The WLTFP's in the middle part of the die show similar levels of failure (black spots) as the WLTFP closer to the side of the die. Damage due to the dicing blade itself is very limited as depicted in Figure 21 where little/no chipping can be found.

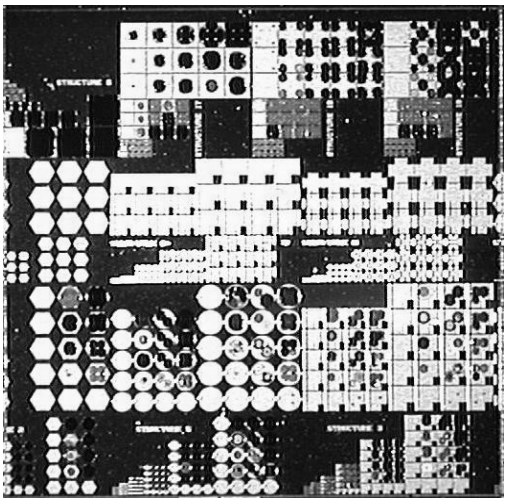


Figure 20 - Die dicing damage

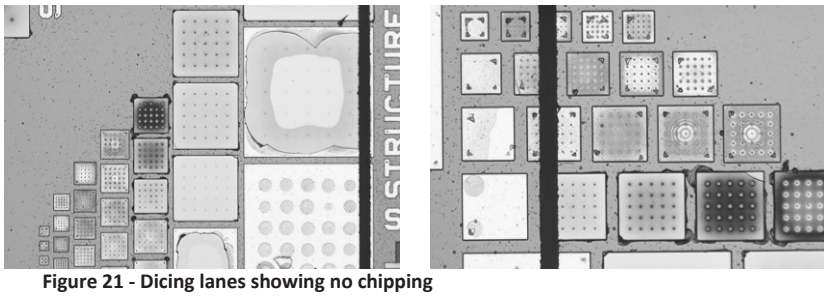


Figure 21 - Dicing lanes showing no chipping

Wire bonding damage

The wire-bonding process has several risks associated with it. The first risk is the excitation of any part of the MEMS or the WLTFP by the wire-bonding frequency. This failure was not observed with the test chips. Since the eigenfrequencies depend on geometry, materials and processing conditions one has to investigate this risk for every layout. This can be done by means of modal analysis using Finite Element software [50].

During failure analysis on WLTFP's that lost hermiticity in production the root cause was determined to be damage by the bond-needle movement as illustrated in Figure 22. Due to the non-flat topography of the WLTFP the bond-needle collided with higher topography and damaged the WLTFP. Careful programming of the bond-needle movement can eliminate this failure relatively easily.

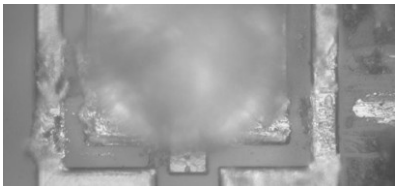


Figure 22 - Damage by the bond-needle

Overmoulding damage

From a mechanical point of view, the protection of the MEMS device should guarantee no contact between the cap and the device during the overmoulding process. In the overmoulding process one uses a relatively high pressure to overflow the epoxy over the die. Due to the imposed pressure, the cap may bend and thereby close the cavity or even crack.

Test results on WLTFP's have shown that they can withstand the pressure [51]. Cracks already present in the WLTFP progressed further but few new cracks were found. Investigation of the ability of the WLTFP to withstand the packaging process is needed to assess the robustness of the WLTFP after

overmoulding. Models can either use a pressure to simulate the moulding pressure or an actual process model.

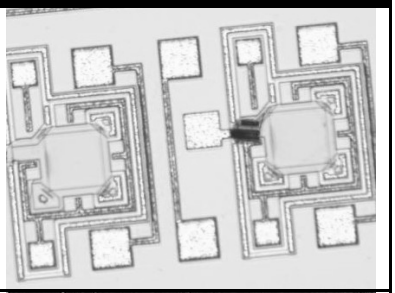
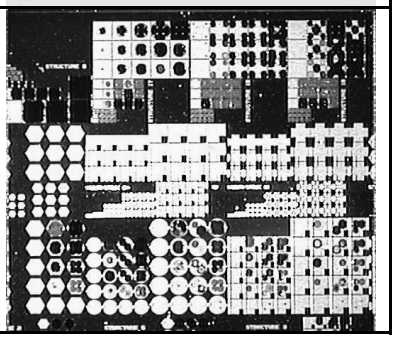
Disadvantages of such models are strong dependence on the correct estimation of the pressure. The actual pressure is strongly dependant on the location of the product in the mould and the process and compound parameters [52].

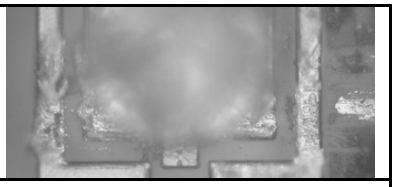
When one wants to investigate the influence of CTE mismatch and curing shrinkage [53, 54] a complete package model is needed since the moulding compound and leadframe/substrate needs to be included [55].

Summary

Most threatening to the WLTFP are processes exerting pressure on it. Tape adhesives as used in the wafer thinning process can exert significant pulling forces on the WLTFP, the brittle nature and small dimension of the capping layers causes the WLTFP to fail easily under these loads. The most common failure modes are summarized in Table 5.

Table 5 - summary of common failure modes during assembly

Assembly step	Failure mode(s)	Example
Wafer thinning	Tape application / removal damage Excessive pressure	
Singulation	Tape application Jet cooling damage	

Wire bonding	Resonance damage Scratching	
Overmoulding	Cracking due to applied pressure	

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5. The process reliability of WLTFP MEMS

This chapter contains several numerical models developed for WLTFP's to estimate the stresses induced during several common assembly processes.

The first paragraph focuses on the wafer grinding process, the second paragraph looks into the pick-and-place process and the third paragraph investigates the overmoulding process. Finally a process ranking based on the severity of loads is presented.

5.1 Introduction

The models in this chapter are made using the finite element analysis (FEA) package MSC Marc Mentat. Stress plots in this chapter show principal stresses unless otherwise indicated. FEA is a powerful tool to explore new designs and design concepts as it does not require physical prototyping.

5.2 Wafer grinding[1]

The wafer grinding process, as earlier described in chapter 2, can be separated into several steps:

1. Tape application: tape is applied to aid in the mounting of the wafer on a vacuum chuck. Since the backside is grinded the tape is applied to the front side where the actual device is located.

2. Grinding: the wafer is secured to the aforementioned vacuum chuck and is grinded to a thickness slightly more than required.

3. Etching: the grinded surface is quite rough, with a lot of microcracks and a relatively high roughness. Etching is used to strengthen wafer.[2]

4. Tape removal: finally the tape is peeled off and the wafer grinding is finished.

[1] Zaal, J.J.M., W.D. van Driel, and G.Q. Zhang, *Challenges in the Assembly and Handling of Thin Film Capped MEMS Devices.* Sensors, 2010. **10**(4): p. 3989-4001.

This paragraph focuses on calculating the loads during tape application and removal process.

Tape application

The tape application process is schematically depicted in Figure 1.

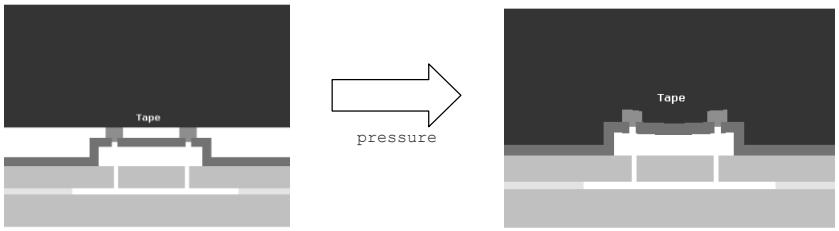


Figure 1 - Tape application to the front side of a wafer

A 2D Finite Element (FE) simulation is performed to calculate the stresses in the WLTFP during tape application. Table 1 list the material parameters used in the simulation. The material properties for silicon nitride, silicon and aluminum are taken from literature while the base foil parameters were obtained by tensile testing. The properties of the acrylic glue are estimated.

Table 1 - material properties used in the tape application model

Material	Young's modulus	Poisson ratio	Material model type
Base foil of grinding tape	50 MPa	0.3	Elastic
Acrylic glue	20 MPa	0.3	Elastic-plastic
Silicon nitride	190 GPa	0.2	Elastic
Aluminum	60 GPa	0.3	Elastic-plastic
Silicon	169 GPa	0.23	Elastic

The geometry used for the simulation is depicted in Figure 2. The model contains 33700 elements with mixed usage of 3-noded and 4-noded elements. The model uses a plane strain assumption as the "thickness" (the Z axis of the picture) is not small compared to the other dimensions. The elements use the assumed strain formulation. To prevent the tape from deforming sideways a boundary condition is use on the side nodes to prevent them from moving in the horizontal direction. This boundary condition acts as a symmetry condition as usually there would be another WLTFP next to the one that is modeled. This

next WLTFP would balance the forces causing the tape to bulge to the side and would thus result in a zero displacement of the side nodes in this simulation.

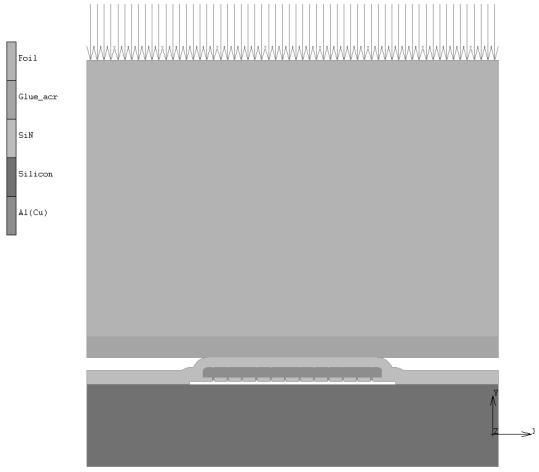
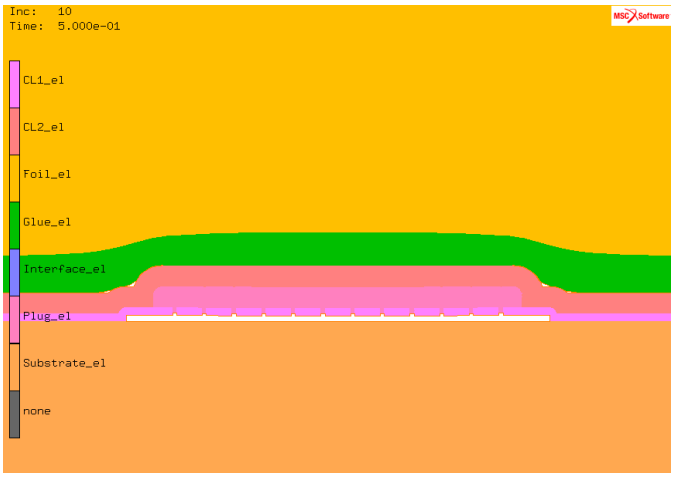


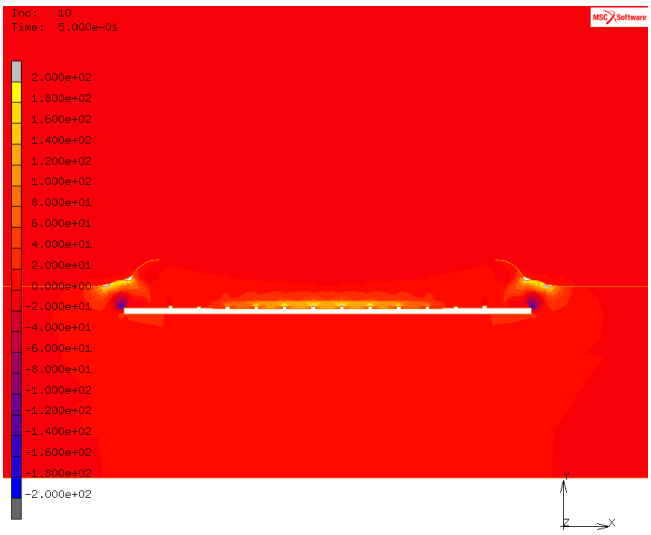
Figure 2 - Tape application geometry

The application of the tape is done by means of a gradually increasing edge load that is applied on the top side of the tape. The edge load represents the location where a lamination tool is usually pressed down on the tape. At the bottom side a boundary condition is applied that prevents the model from moving in the Y direction.

The resulting deformations and stress levels of a WLTFP during tape application be found in Figure 3. The yellow layer in Figure 3(a) is the base film of the tape and the green layer is the glue. The glue is forced around the WLTFP by the applied pressure but the glue does not have full contact everywhere. Contact algorithms are used to mimic the embedding of the WLTFP in the glue. The contact method uses a division into different contact bodies, in this case one body consists of the base foil and the glue and the other body consists of the WLTFP. During each calculation step the distance between all nodes and curves is checked and if there is contact the chosen contact condition is applied. The possible conditions are: glue (once contacted surfaces stick to each other) or touching (the two bodies can separate or slide). In this model the glue condition is used.



a) tape application deformation plot



b) stress distribution during tape application

Figure 3 - Tape application simulation results

Figure 3(b) depicts the maximum principal stress corresponding with this loading mechanism. The edges and the center of the cavity are loaded due to the bending in the freestanding WLTFP layers. The maximum principal stress due to the application of the tape is 180 MPa with a WLTFP span of 100 µm.

The calculated deformation of the WLTFP under the tape application load is depicted in Figure 4. A maximum deflection of 0,2 µm is found in the centre of the freestanding WLTFP layer.

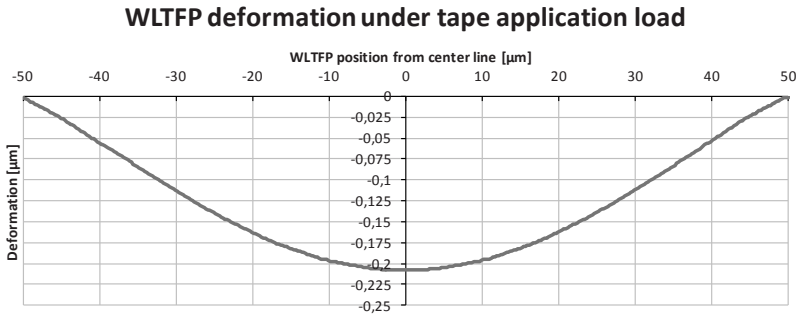


Figure 4 - WLTFP deformation shape under tape application load

A cross section of a WLTFP embedded in the glue found in experiments is depicted in Figure 5. It clearly matches the calculated deformations.

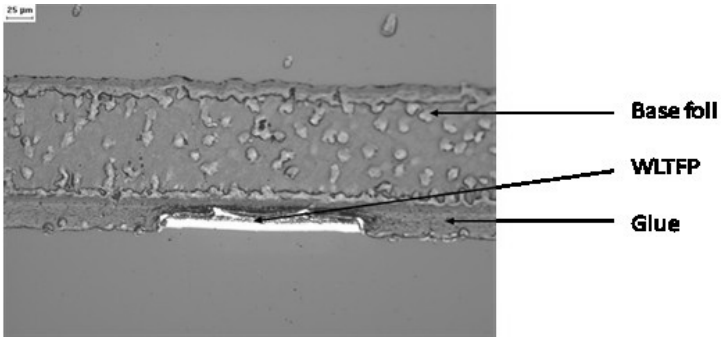


Figure 5 - cross-section of a WLTFP embedded in glue

Tape removal

The tape removal process from the active side is hazardous in the sense that the release of the glue will apply tensile forces on the WLTFP caps and seals. Damage to WLTFP's due to tape application and removal are depicted in section 4.3. As a reminder, a typical damage pattern is depicted in Figure 6.

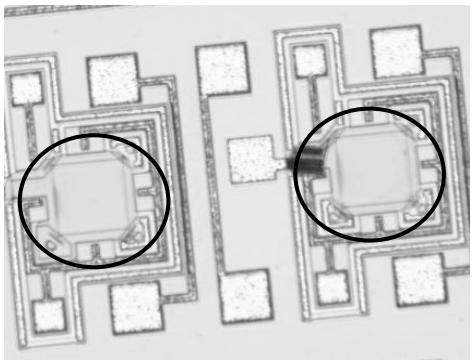


Figure 6 – Two resonators without a WLTFP after wafer thinning foil removal

The wafer in section 4.3 did not undergo any grinding process between tape application and removal. This means all damage is caused by forces of either applying the tape or removing the tape.

Simulation of the tape removal process can identify the regions of the WLTFP that experience the highest stress concentrations. To simulate the tape removal process, a model using the cohesive zones technique [3] is derived from the geometry of the tape application model. The material properties are the same as listed in Table 1.

The geometry depicted in Figure 7 is a 2D representation of a 100 µm wide cavity with a matrix of plugs sealing the cavity. The symmetry boundary condition is kept at the left side of the detaping model. A new boundary condition (replacing the edge load used for applying the tape) is introduced to peel the tape off. This boundary condition uses a vertical displacement that is gradually applied to the tape resulting in the tape being peeled of the wafer. Again the underside of the wafer is constrained in such a way that movement in the vertical direction is not possible.

The stress distribution in Figure 8 shows that the stress concentrations are found in the region near the corners of the WLTFP and the middle part of the

freestanding layer. The maximum principal stress is around 200 MPa for this specific type of tape and cavity combination.

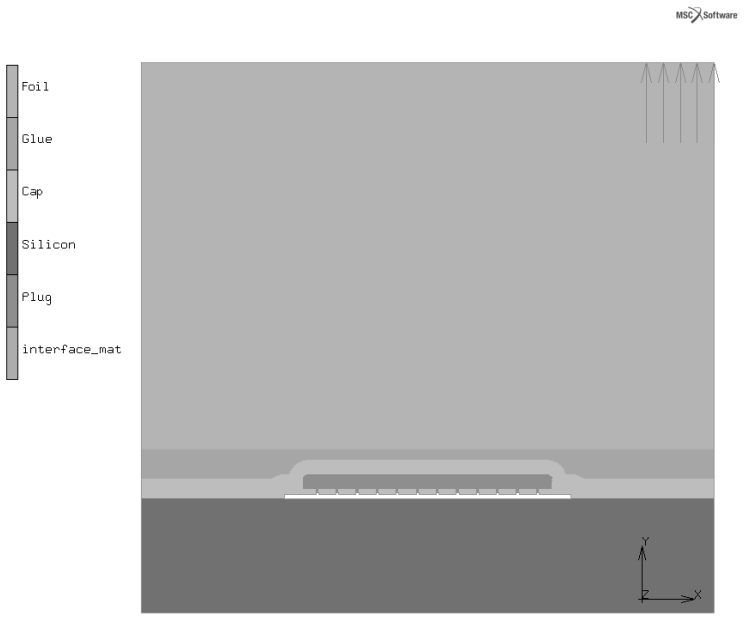


Figure 7 - Tape removal model

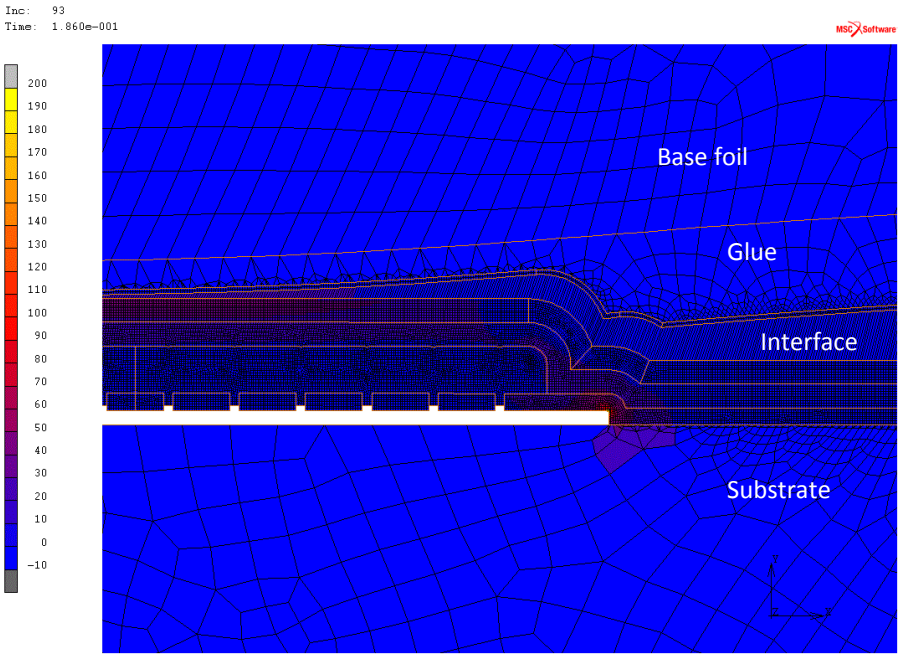


Figure 8 - Principal stresses in MPa caused by tape removal

A 3D model of the tape removal simulation is made to see if the model can predict the failure shape found after grinding tape removal. This model consists of half the cavity to limit the amount of elements. On one side a symmetry condition is created while on the other side a “fixed” condition is applied on the silicon nitride layers to represent the side of cavity where the silicon nitride layer is again in contact with the substrate. The model consists of an extruded 2D view with the etching holes in the capping layer added along the extrusion line. The full 3D geometry is depicted in Figure 9. The model consists of 75000 8-noded 3D elements with assumed strain formulation. 2200 elements cohesive zones elements are used to simulate the glue attachment of the tape to the wafer. The cohesive elements have an energy release rate of 0,02 J/mm and a maximum traction of 1 µm. The cavity side is fixed by means of boundary conditions instead of a physical model of the side of the cavity to ensure the calculations can still be solved in a reasonable CPU time. Figure 10 depicts the cavity. The centerline has a symmetry condition applied to it while the side of the cavity should have a physical connection between the substrate and the freestanding capping layer. To reduce the number of elements a boundary condition was used.

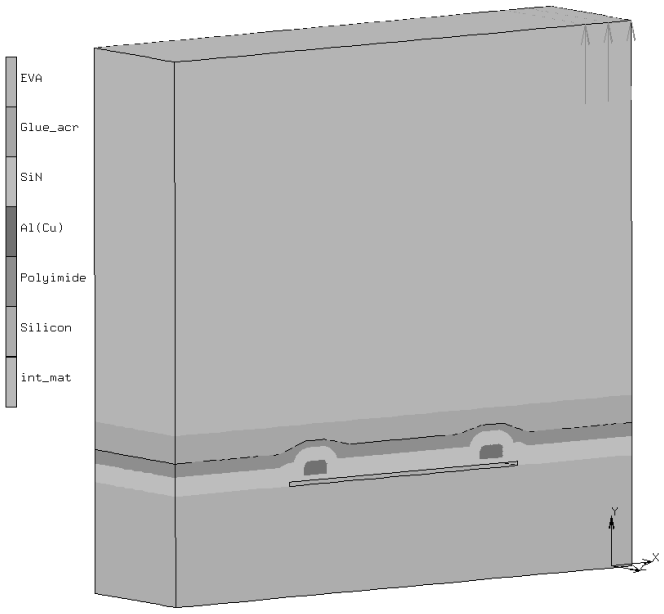


Figure 9 - 3D model (with planarization)

Figure 10 depicts the model as seen from the bottom (silicon substrate side). The small dots are the etching holes used to remove the sacrificial layer during production. A notable difference with the earlier simulations is the different etch hole distribution. The placement of the etch holes on the side results in a longer etching time but at the same time reduces the risk of sealant deposition on the device.

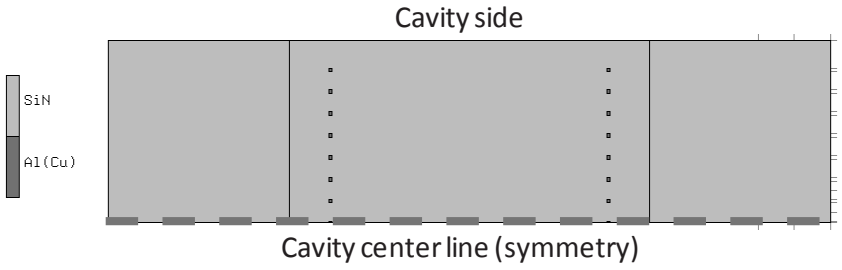


Figure 10 - Bottom view of the half model of the WLTFP cavity

Failure of the WLTFP's in the experiments is seen along the cavity edges. The corners however are mostly remaining while the center is gone after

detaping. In Figure 11 the left and lower right cavity illustrate this phenomenon.

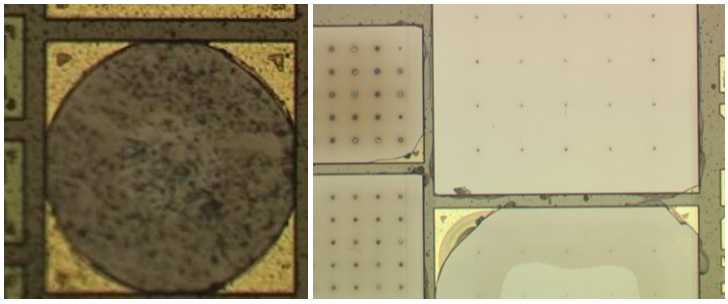


Figure 11 - Failed WLTFP's after tape removal

During the detaping simulation in 3D the delamination process is not progressing smoothly. When the glue releases from the side of the cavity the sudden deformation causes an unstable crack propagation towards the next vertical obstruction, which is the next row of plugs sealing the cavity.

In the 3D model, depicted in Figure 12, the stress pattern is showing similarities with the failed WLTFP above.

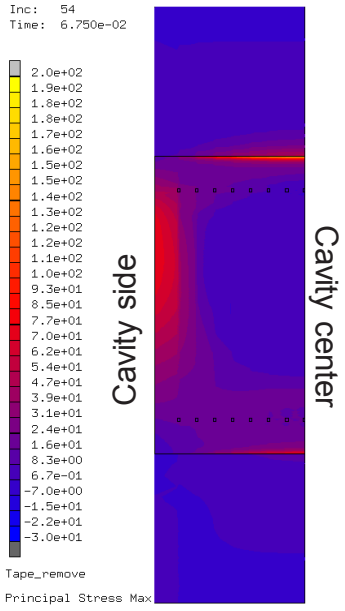


Figure 12 - Bottom view of the 3D model during detaping

This shows the relevance of making a 3D model since a 2D model cannot predict this.

5.3 Pick and place

During the placement of the die on the leadframe, the die needs to be removed from the tape by means of a pick and place operation. The same holds for a flip-chip application. The cavity can be damaged by the gripper when it is touched. On the contrary the vacuum used to hold the chip will not damage low pressure cavities since the differential pressure only decreases due to the very low cavity pressure. The pick and place force is in the order of 1N [4], this corresponds to a 1MPa suction force on the chip when a vacuum collet is used with a 1 mm2 internal cross-section. These forces are not significant in comparison to other process induced stresses.

5.4 Overmoulding

The WLTFP should protect the MEMS device and there should be no contact between the cap and the device during the overmoulding process. In the overmoulding process pressures of 60–90 bar are used to liquidize the epoxy and overflow the die. Due to the imposed pressure, the cap may bend and thereby close the cavity or even crack. The pressure acting on a WLTFP is not equal for each WLTFP in the mould due to the viscous nature of the epoxy moulding compound. Pressure is needed to flow the epoxy to each corner of the mould. The flow front should, by default, be at atmospheric pressure, meaning that a WLTFP just behind the flow front experiences a low pressure. The injection pressure is the pressure measured in the plunger of the moulding machine. The real experienced pressure by the WLTFP is thus a function of location in the mould [5]. WLTFP's closer to the runner will experience a higher pressure than WLTFP's far away from the runner. When the filling of the cavity is completed, pressure will rise everywhere due to the lack of empty space to fill. However, due to curing the pressure on the WLTFP will not be equal to the injection pressure since the EMC is curing rapidly and reinforcing the cavity. This is caused by the high mould temperature which affects the curing kinetics.

After moulding the curing shrinkage of the EMC [6] can load the WLTFP. The curing shrinkage can be 1 to 2 percent in each direction.

Simulations of a moulding process should thus include curing kinetics and cure shrinkage in combination with a flow analysis when an accurate estimation of the moulding process loads is needed. An easier approximation can be made by applying the injector pressure to the model. However, this is an overestimation and the cavity should thus be more robust to survive simulation than needed in reality. Figure 13 depicts such a model. The model is a modified version from the models earlier described using the same materials and geometry. A pressure of 8 MPa is added as representation of an 80 bar moulding pressure.

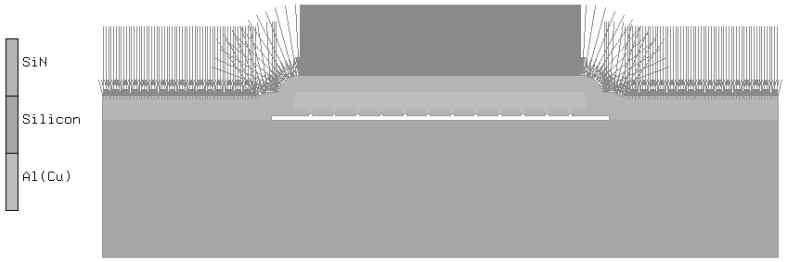


Figure 13 - Model of the WLTFP under moulding pressure (represented by the arrows)

The maximum stresses found are in the order of 250 MPa. The high stress regions are located near the edge of the cavity, which is a bending point, and on the underside of the cavity near the centre. A stress map is depicted in Figure 14.

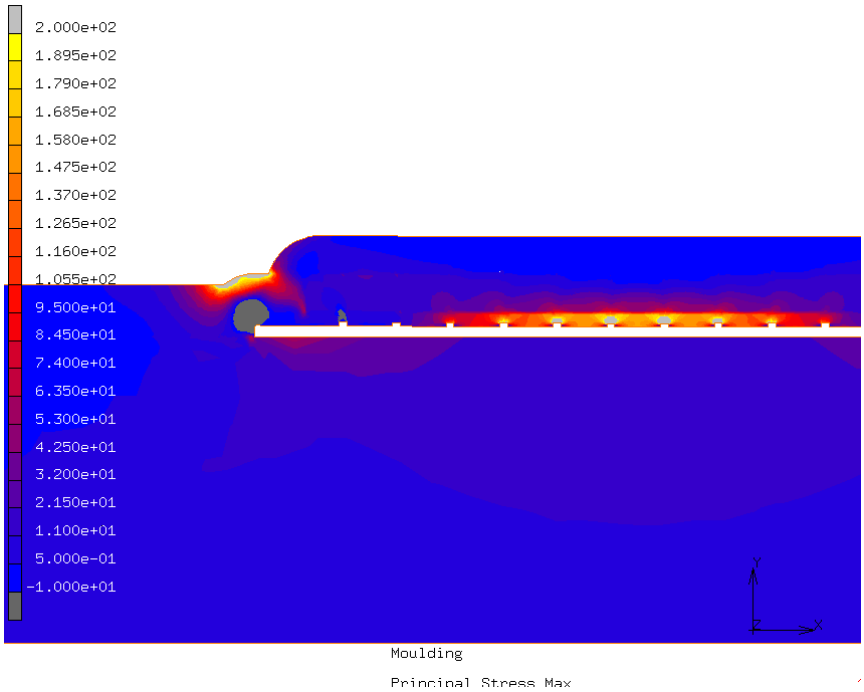


Figure 14 - The maximum principal stress in the WLTFP due to an 80 bar moulding pressure

5.5 Conclusions

Based on experimental observations combined with calculated stress levels, see Figure 15, a ranking of the most hazardous assembly processes for WLTFP's can be made, being:

1. Wafer thinning. The most hazardous is the wafer thinning process due to the direct contact with the grinding tape and the process pressure used.

2. Dicing. Dicing is a hazardous process due to the application to the tape and the risk of debris and subsequent cleaning damage.

3. Overmoulding. The moulding process is less dangerous than the previous two processes but can cause problems in yield due to the different loading levels throughout the mould.

A robust and accurate WLTFP design should consider assembly loads and try to avoid stress concentrations after wafer processing. These stress

concentrations can be caused by, for example, CTE (Coefficient of Thermal Expansion) mismatches or poor geometric design.

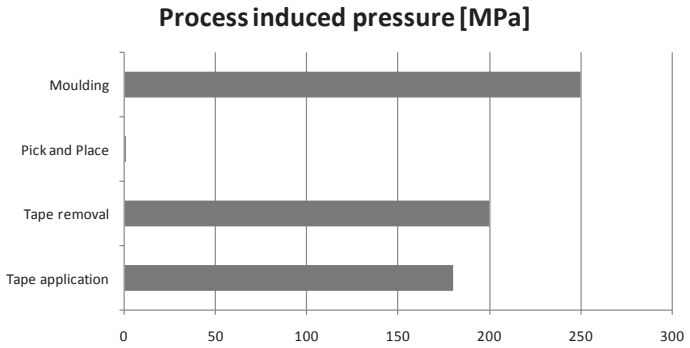


Figure 15 - Process induced pressures on the WLTFP

5.6 References

1. Zaal, J.J.M., W.D. van Driel, and G.Q. Zhang, *Challenges in the Assembly and Handling of Thin Film Capped MEMS Devices.* Sensors, 2010. **10**(4): p. 3989-4001.
2. Wu, J.D., C.Y. Huang, and C.C. Liao, *Fracture strength characterization and failure analysis of silicon dies.* Microelectronics Reliability, 2003. **43**(2): p. 269-277.
3. Zhang, G.Q., W.D. van Driel, and X.J. Fan, *Mechanics of Microelectronics*. Solid mechanics and its application, ed. G.M.L. Gladwell. Vol. 141. 2006, Dordrecht: Springer. 563.
4. *Internal Report Sumo*. 2009, NXP Semiconductors: Nijmegen.
5. Roellig, M., et al. *Modeling, simulation and calibration of the chip encapsulation molding process*. in *Thermal, Mechanical and Multi-Physics simulation and Experiments in Microelectronics and Microsystems, 2009. EuroSimE 2009. 10th International Conference on*. 2009.
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6. Interface characterization

When one wants to optimize the WLTFP for assembly processes as tape application and tape removal FEA is a powerfull tool. Chapter 5 described several FE models used for analysis of WLTFP during assembly processes. The parameters for these models are essential in exploring the sensitivities of the chosen process parameters and during optimization of process settings. The cohesive zone elements used are one of the essential parts in the detaping simulations. The first paragraph will review the theory of cohesive zone elements as implemented in Marc Mentat, the used simulation software. [1] The second paragraph will describe the measurements performed in this research on the used wafer thinning foil.

6.1 Introduction to cohesive zones[1]

Marc Mentat has several types of cohesive zone elements. Element types 186 to 193 are usable for simulating a delamination process. The cohesive elements used in chapter 5 have zero thickness and consist of two planes that are initially coinciding. As a result of applied stresses (both normal and shear) the element undergoes a reversible deformation followed by an irreversible damage process. This process uses a damage parameter ranging from 0 (no damage) to 1 (fully damage).

The effective traction t is a function of the effective opening displacement v and is characterized by the aforementioned initial reversible response followed by an irreversible response as soon as the critical effective opening displacement v_c has been reached.

Marc Mentat has three build in types of traction models. These functions are a bilinear, an exponential and a linear-exponential function. Figure 1 depicts the effective opening displacement - traction graphs for each of the three models.

[1] Submitted to the International Journal of Fracture

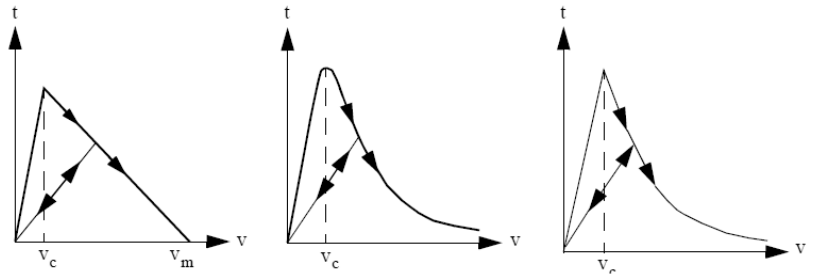


Figure 1 - a bilinear model (left); an exponential model (middle) and a linear-exponential model (right) [1]

The associated traction formulas can be found in Equation 1 to Equation 3.

$$\left.\begin{array}{ll} \text{For } 0 \le v \le v_c & \dfrac{2G_c}{v_m}\dfrac{v}{v_c} \\ \text{For } v_c \le v \le v_m & t = \dfrac{2G_c}{v_m}\left(\dfrac{v_m - v}{v_m - v_c}\right) \\ \text{For } v > v_m & t = 0 \end{array}\right\} \quad \text{Equation 1}$$

$$t = G_c \frac{v}{v_c^2} e^{-v/v_c} \quad \text{Equation 2}$$

$$\left.\begin{array}{ll} \text{For } 0 \le v \le v_c & t = \dfrac{2qG_c}{v_c(q+2)}\dfrac{v}{v_c} \\ \text{For } v > v_c & t = \dfrac{2qG_c}{v_c(q+2)} e^{q\left(1 - v/v_c\right)} \end{array}\right\} \quad \text{Equation 3}$$

G_c is the energy release rate also known as cohesive energy, v_m is the maximum effective opening displacement and q is the decay factor.

In the models presented in chapter 5 an exponential model is used. This model requires two parameters, being: G_c and the maximum effective traction. The maximum effective opening displacement is given in Equation 4.

$$v_c = \frac{G_c}{e \cdot t_c}$$ Equation 4

The next paragraph describes the experiments used to characterize the grinding foil used in the wafer thinning process.

6.2 Interface material characterization

When making an FE model one needs the material parameters of the relevant materials. In the modeling of a delamination process some properties of the adhesive release are needed. The next paragraph describes the measurement setup used to characterize the grinding foil used to thin a wafer.

Experimental setup

A 6" wafer covered with silicon nitride is placed on grinding tape and grinded down to 250 µm. After this step the wafer and the tape are cut by a diamond blade into strips of 15 mm wide and 100 mm long as depicted in the diagram in Figure 2.

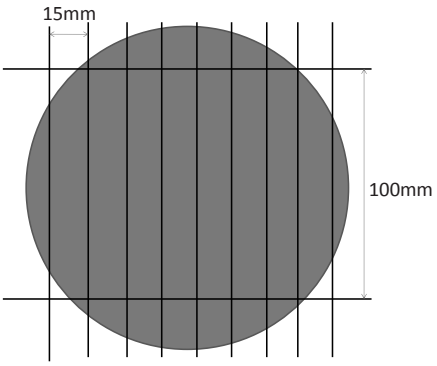


Figure 2 – sample dicing diagram

The strips are fixed on a metal base and the tape is then peeled off using a Zwicki 1120 universal testing machine in combination with a Hottinger Baldwin Messtechnik 5N load cell. The load cell is connected to the tape by means of a clamp and pulling rod allowing for small movements to the sides. A schematic picture of the setup is depicted in Figure 3. This method was earlier used by van der Sluis et al. [2]

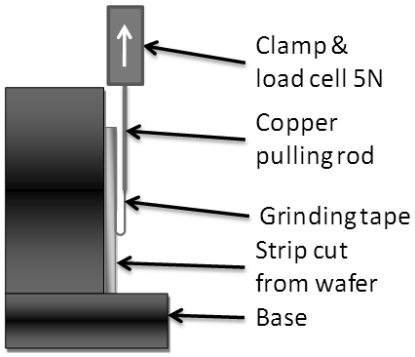


Figure 3 – peeling setup

The setup is used at a pulling rate of 400 mm/min and a preload of 0.1 N as trigger for the start of the detaping process. Figure 4 depicts the real life setup with the sample in place behind the copper pulling rod.

Figure 4 - setup as used

After the start of the test the stage with the load cell is moving slowly until the preload is reached. After this step the preset speed is applied. At the beginning of the force/displacement graph a ramp is visible caused by the fact that the slack needs to be pulled out of the loop in the tape. An example force displacement graph is depicted in Figure 5.

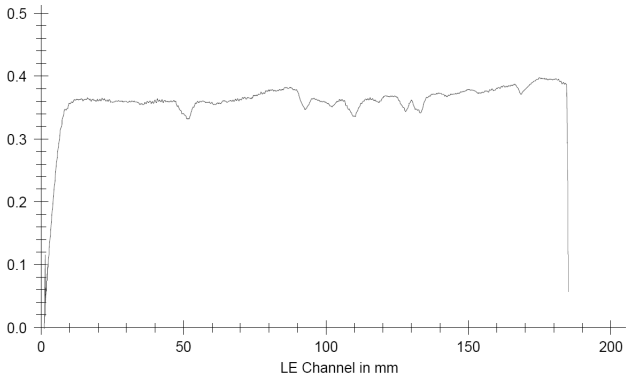


Figure 5 – a force [N] displacement [mm] graph

The small dents in the force-displacement diagram are related to small air bubbles caught under the tape during tape application.

Besides the force another interesting measure is the deformation shape of the tape under the pulling force. The diameter of u-shape in the foil depends on the stiffness of the tape, the pulling force and the traction parameter of the cohesive zones model. [2] Figure 6 schematically depicts the tape removal process and the mentioned diameter *d*.

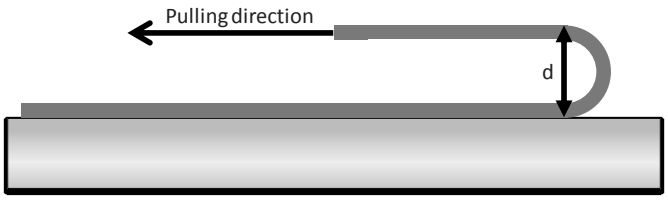
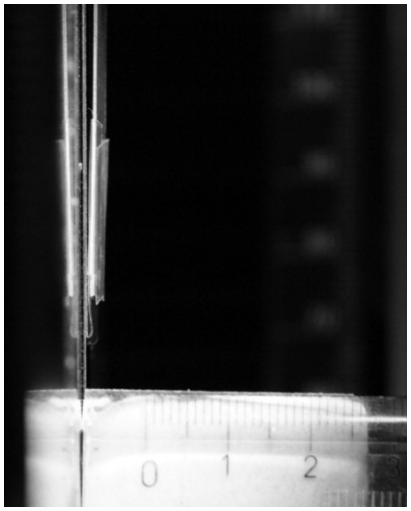


Figure 6 - schematic pulling process

The diameter is measured by taking pictures of the delamination process. By including a scale in the picture the diameter *d* can be measured. The taken pictures have a pixel size equivalent to 27 µm in real life. Figure 7 depicts four consecutive moments in a tape peeling experiment.

1



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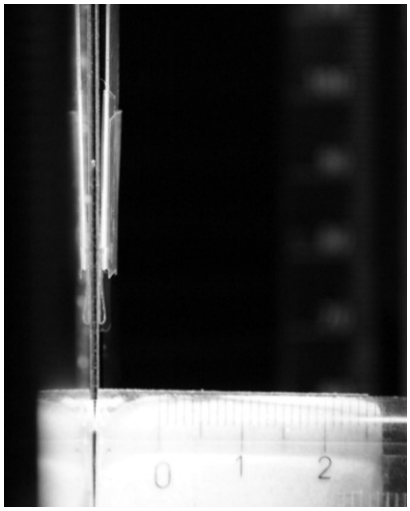

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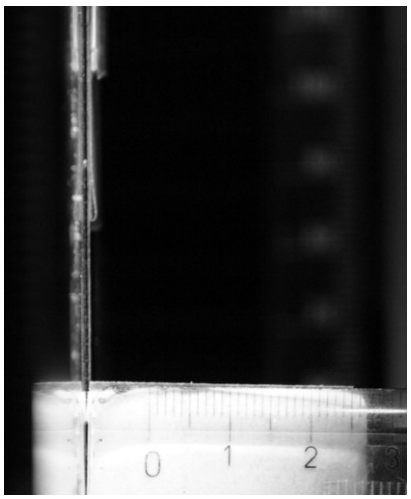

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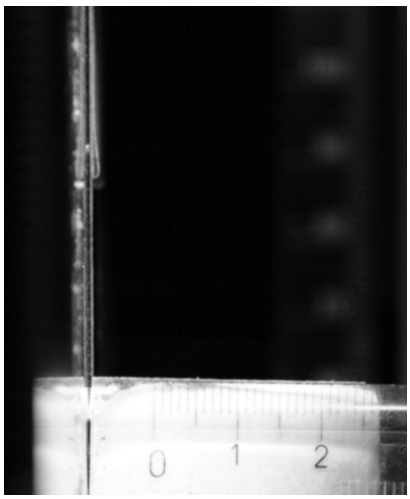

Figure 7 - the grinding foil during 4 stages of the peeling process

The curvature of the tape is measured several times during the peeling process to monitor if the curvature is constant.

Results

To extract the energy release rate from the experiment Equation 1 [3] is used. G is the energy release rate in J/mm, F is the force in N and w is the sample width in mm. θ is the angle between the silicon nitride and the tape.

$$G = \frac{F}{w}\left(1 - \cos(\theta)\right) \qquad \text{Equation 5}$$

All conducted experiments on the earlier described samples yield forces of 1.00 N with a standard deviation of 0.03 N. See Table 1.

Table 1 – tape peeling overview

Measurement	F [N]
1	1,01
2	1,02
3	1,04
4	1,01
5	0,98
6	1,02
7	0,98
8	0,99
9	0,96
10	0,96
11	1,00
12	0,97
13	0,96
14	1,04
Mean	1,00
Standard deviation	0,03

The measured diameters from the photos taken from the measurements are listed in Table 2. The curvatures were measured using the number of pixels for the u curve and the value of an individual pixel.

Table 2 – tape curvature measurements

Sample	Curvature on photo [mm]						Avg
	1	2	3	4	5	6	
1	0,946	0,918	0,918	0,944	0,944		0,934
2	0,935	0,909	0,938	0,907	0,935	0,935	0,926
3	0,779	0,781	0,833	0,885	0,888		0,833
4	0,883	0,93	0,907				0,907
5	0,93	0,956	0,959				0,948
6	0,959	1,01	0,933	0,93			0,958
7	0,938	0,911	0,938				0,929
8	0,984	1,062	1,062				1,036
9	1,011	1,008	0,914				0,978
10	0,931	0,931	0,981	0,981	0,984		0,962
11	0,934	0,932	0,959				0,941
12	1,081	1,005	1,005	1,005	0,95	0,926	0,995
13	1,046	1,032	0,997	1,024	1,051	1,054	1,040
	1,081	1,024	1,048				
						Average	0,958

Combining Equation 5 with the sample width of 15 mm and an estimated peeling angle of 160° yields the energy release rate. All results are listed in Table 1.

Table 3 – Energy release rates

Measurement	G [J/mm]
1	0,130
2	0,132
3	0,134
4	0,131
5	0,127
6	0,132
7	0,127

8	0,128
9	0,124
10	0,124
11	0,129
12	0,125
13	0,124
14	0,134
Mean	0,129
Standard deviation	0,004

6.3 Comparison of experiment to FEM

A FE model is created to investigate the traction value by fitting by the measured curvature to the model curvature during peel off.[4] Figure 8 depicts a 2D FE model that is used for such an analysis. It consists of a SiN layer where the tape is glued to by means of cohesive zone elements. The pulling rod is represented by a piece of copper that is fixed to the tape.

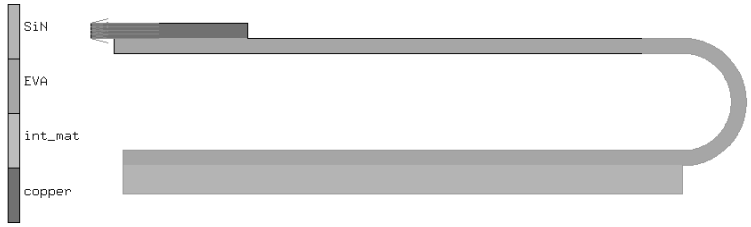

Figure 8 - tape peeling FE model

All material properties of the materials used in the FE model are listed in Table 4.

Table 4 – material properties used in the peeling model

Material	Young's modulus	Poisson ratio	Material model type
Base foil of grinding tape	50 MPa	0.3	Elastic
Silicon nitride	190 GPa	0.2	Elastic
Copper	105 GPa	0.33	Elastic

The tape pulling speed from the experiment is used in the model and is applied through a fixed displacement boundary condition that is linearly increasing with a rate equal to the pulling speed. The properties of the cohesive elements are: G_c =0,13 and t_c=0,01.

Initial results can be found in Figure 9. The color map refers to the displacements, with yellow being large displacements and blue being no displacement at all.

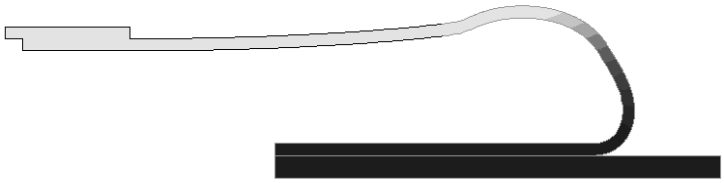

Figure 9 – deformed model during tape peeling (no displacement amplification)

The results from Figure 9 approximate the experiment but a fundamental problem with the simulation is clearly visible. The bended tape present in the initial model is not straightened out by the pulling forces. To solve this mismatch with the experiment a different model is created using a two stage approach.

1. Pre-bending by use of a rigid body
2. Peeling

The pre-bending simulation setup is depicted in Figure 10. The circle in the lower right is a rigid body used to deform the tape until it lands on the upper strip. This strip is used to make sure the direction of the pulling rod is in the pulling direction. After the pre-bending stage the earlier described peeling process is executed.

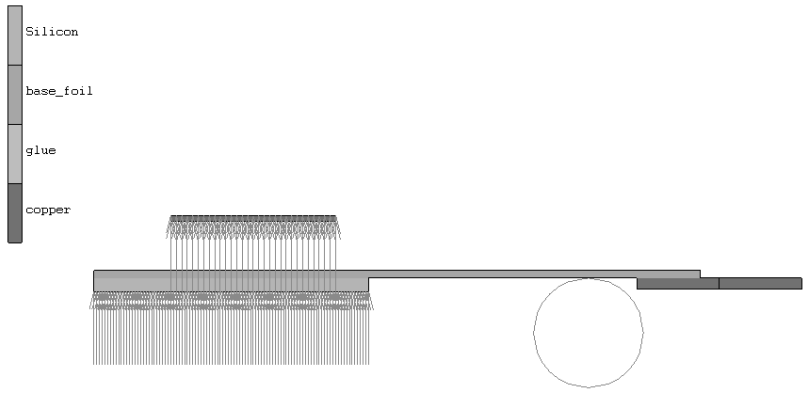

Figure 10 – the pre-bending model; the colors relate to materials

Figure 11 depicts the deformations during the prebending phase. The used colors relate to the different contact bodies.

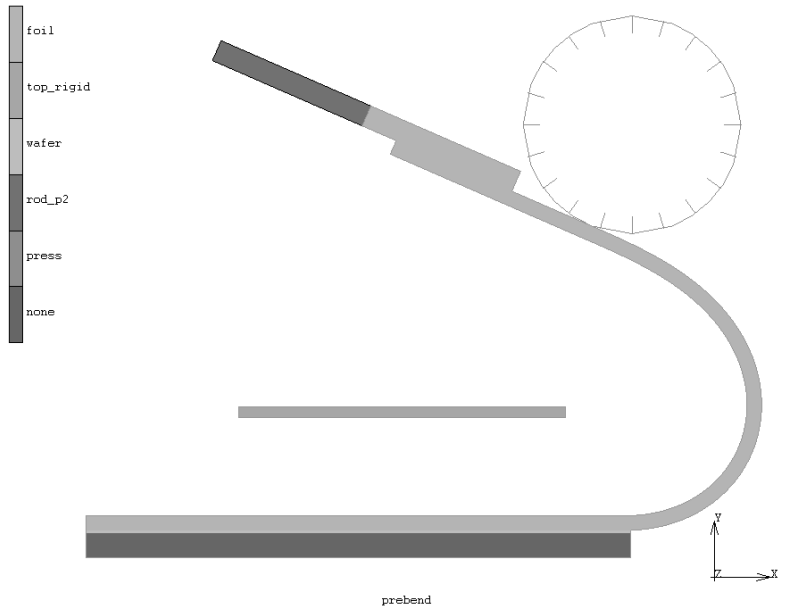

Figure 11 – the model during prebending; the colors relate to the used contact bodies

Figure 12 is a deformation plot during the peel off phase.

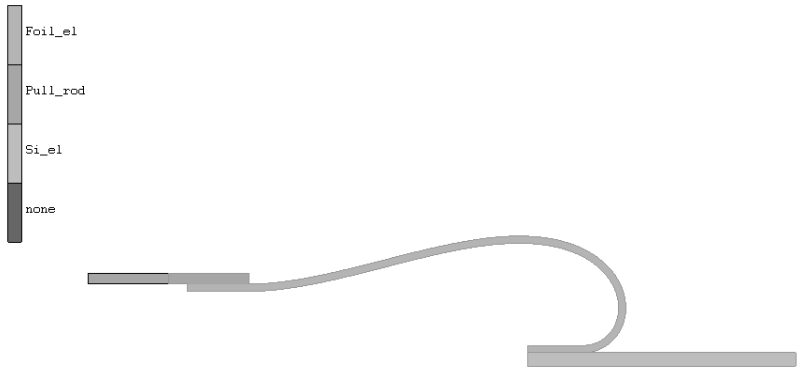

Figure 12 – deformation during the peel-off phase

The cumulative reactive forces during peel off are depicted in Figure 13. The shape of the graph is similar to the earlier presented experimental force-displacement graphs.

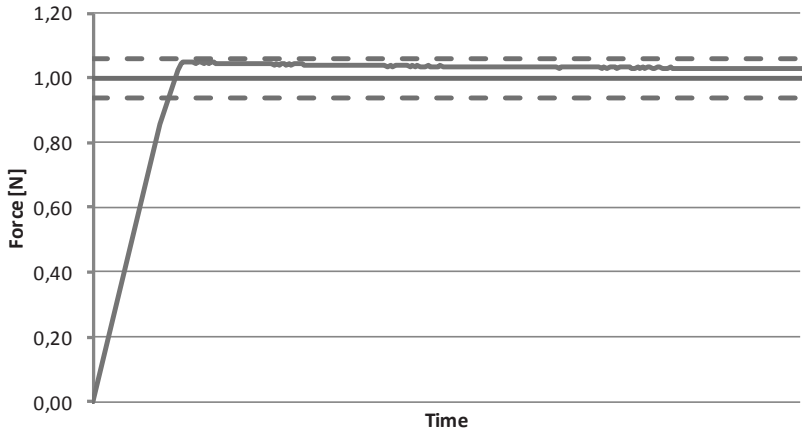

Figure 13 – Pulling forces during the tape pull from FEA and from the experiment (including ± 2 σ lines)

The pull off force diagram in Figure 13 shows that the peel off process can be simulated using a cohesive zones modeling approach. Using cohesive zones it is possible to explore design variations and to optimize the tape peel off process using different tape properties.

6.4 Tape process optimization

When looking for an optimized wafer thinning process a trade off has to be made in properties. The most dominant properties are:

- Tape adhesion force: the tape adhesion force directly influences the forces encountered during tape peel off
- Tape thickness: a thicker tape (with sufficient softness) will reduce stress during the tape application
- Glue layer thickness: a soft thick glue layer, for example a gel like pressure sensitive acrylic, will protect the WLTFP during application of the tape
- Tape stiffness: if a very stiff tape is peeled the radius of curvature (as measured in this chapter and listed in Table 2) will change influence the shape of the region of tape releasing from the wafer.

The easiest way to reduce the stress on the cap during peel off is to reduce the adhesive force of the grinding foil. This can be done by taking a type of tape that is does not stick well or by taking a UV curable tape. When using a UV curable tape the adhesive is cured using UV light and is easier removed afterwards.

The choice of foil also influences the load on the WLTFP during tape application and wafer thinning. If the tape is very soft it will easily form around the WLTFP and distribute the stress over the entire wafer. A stiffer tape will land on the WLTFP's first and will only touch the wafer itself after a lot of pressure is exerted on it.

6.5 Conclusions

The experiments in this chapter in combination with the foil simulations allow for characterization of the adhesive properties of the foil. The adhesive properties can then be used in the simulations to explore the stress patterns of the designed product before it is actually manufactured.

6.6 References

1. Software, M., *Marc 2010 Volume A: Theory and User Information* 2011.

2. Sluis, O.v.d., et al., *Stretching-induced interconnect delamination in stretchable electronic circuits.* Journal of Physics D: Applied Physics, 2011. **44**(3): p. 034008.
3. Thouless, M.D. and H.M. Jensen, *Elastic Fracture Mechanics of the Peel-Test Geometry.* The Journal of Adhesion, 1992. **38**(3): p. 185 - 197.
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7. Product optimization

In this chapter a four variable design of experiments is performed. The goal of this DOE is to derive design boundaries such that the WLTFP can successfully be assembled in a plastic encapsulated package. WLTFP's are fabricated with the following variations:

1. Different spans
2. Different corner radiuses
3. WLTFP thickness
4. Supported and unsupported WLTFP's

The first paragraph will present a listing of all chosen variations, the lithographic mask and the fabrication process. The assembly process and inspection method is also specified. In the second paragraph the results of each assembly process are presented. The third paragraph specifies some guidelines with respect to assembly and the choice of WLTFP. Followed by the fourth paragraph that summarizes the experimental results and list the conclusions and recommendations.

7.1 Introduction

In order to investigate the sensitivities in WLTFP design a DOE is performed focusing on failure during assembly. The failure rates will show the most critical parameters in designing a WLTFP.

7.2 Experiment[1]

The parameters of the WLTFP DOE are chosen to be: span, corner rounding radius, cap thickness and with/without supporting pillar. The design variables are depicted in Figure 1.

All chosen values for the design variables are listed in Table 1.

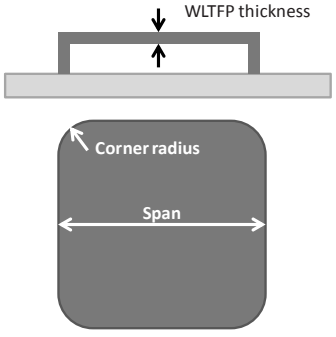

Figure 1 - design variables

1 Submitted to Microelectronic Reliability, Elsevier

Table 1 – WLTFP design variable variations

Parameter	Minimum / maximum	Step size
Span	20 / 200 µm	20 µm
Corner radius	10 / 100 µm	10 µm
WLTFP thickness	1 / 7 µm	2 µm

All caps are produced with and without supporting pillar in the center (circular shape and 5 µm diameter). The lithographic mask of the DOE block is depicted in Figure 2. The block is produced 36 times on a 4" wafer. Each block contains the chosen 130 variations each replicated 36 times on a wafer. The block is produced in 4 different thicknesses resulting in 18720 samples for evaluation.

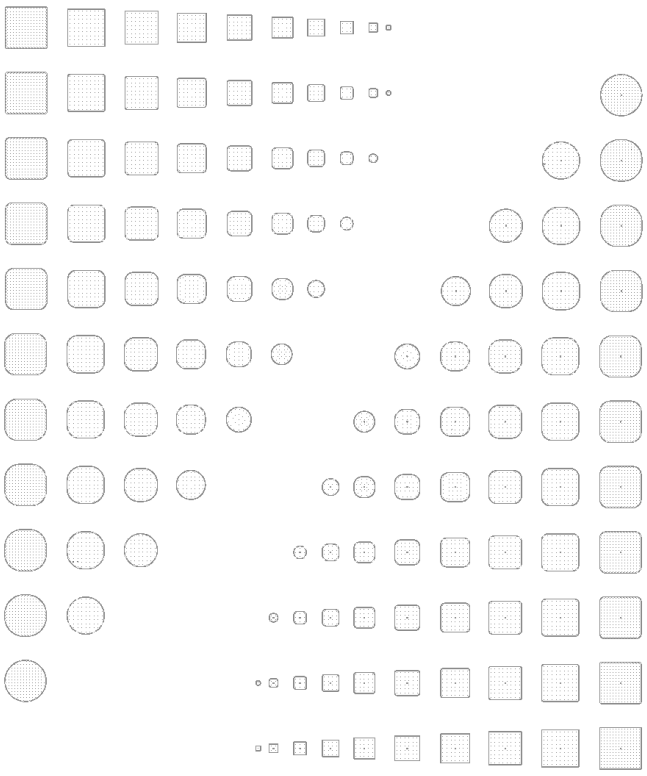

Figure 2 – WLTFP DOE mask; left the WLTFP's without a supporting pillar, right the ones with a supporting pillar

The first fabrication step for the WLTFP's is deposition of a 500 nm SiN by means of Plasma Enhanced Chemical Vapor Deposition (PECVD). This step is

followed by the sputtering of a 2.5 μm aluminum sacrificial layer. After patterning this layer a PECVD SiN layer was deposited and patterned to allow for etching of the sacrificial layer. The aluminum layer is removed by means of a KOH etchant and the cavities are sealed by means of another PECVD SiN layer. Due to the nature of the deposition process the pillars are not completely filled but are comparable to hollow cylinders. The fabrication process is schematically depicted in Figure 3.

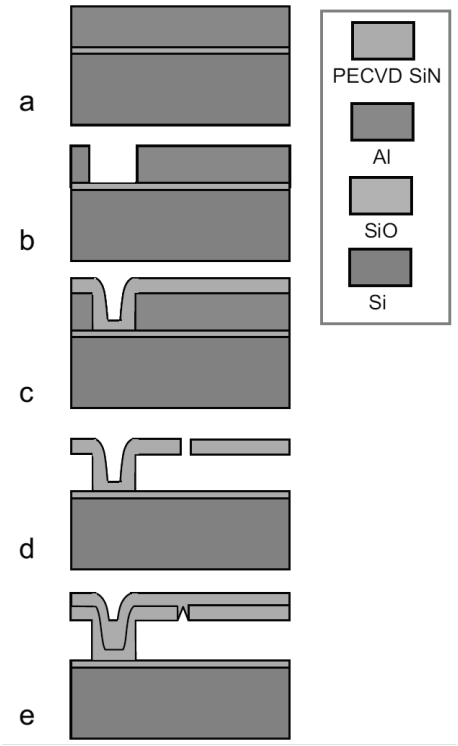

Figure 3 – Fabrication process; a) Sacrificial layer deposition. b) Trench etching defining columns. c) Capping layer deposition. d) Etching of the access holes and sacrificial etching. e) Sealing layer deposition [1]

Figure 4 depicts part of a fabricated block of WLTFP's. In the vertical direction the corner radius is increasing while in the horizontal direction the span is decreasing.

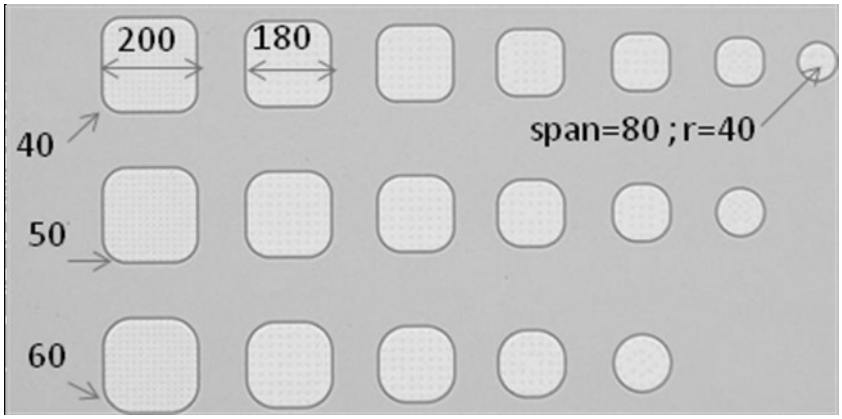

Figure 4 – part of a fabricated block of WLTFP's

A scanning electron microscope (SEM) picture of a cross sectioned cavity and pillar is depicted in Figure 5.

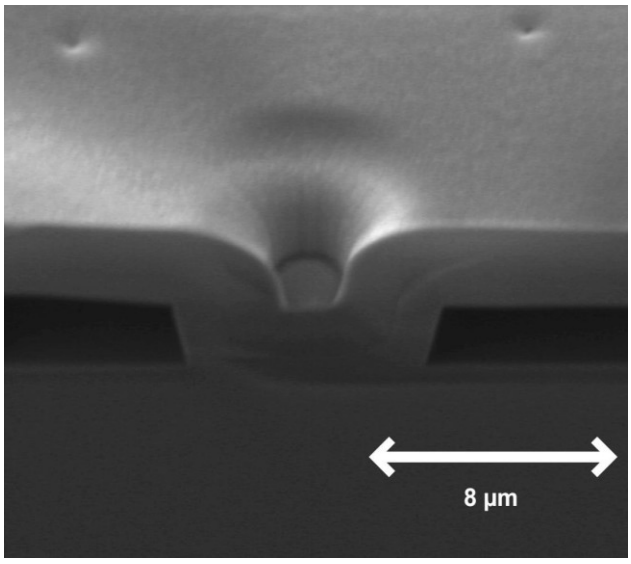

Figure 5 – a cross-sectioned WLTFP pillar with the cavity on both sides

Before the wafers are thinned all WLTFP's are inspected. Besides some dust particles only a few cavities showed some minimal damage.

After inspection the wafers are thinned using the Furukawa SP-594M-130 wafer thinning foil. This foil adheres to the side of the wafer containing the

MEMS and is used to secure the wafer to the vacuum chuck during wafer thinning. The process of wafer thinning is described in section 2.2.

The WLTFP's are inspected through the complete assembly process at various moments. The optical inspection moments and the sample size are summarized in Table 2.

Table 2 – WLTFP inspection scheme

Inspection moment	Number of inspected WLTFP's
After wafer fabrication	18720
After wafer thinning	18720
After dicing	780
After die-attach	780
After overmoulding and decapsulation	780

The last stages of production are not processed and inspected using all samples due to the lead time of the production for that amount of samples. Also some of the samples were damaged so badly that they had very little surviving WLTFP's.

The dicing is done using a 40 µm diamond dicing blade on a standard dicing tape with a standard cleaning method. The die-attach process is also using a standard epoxy die-attach glue with a normal curing process. The dies are mounted on a QFP100 package leadframe with an extra large die pad. The QFP100 was chosen because it can accommodate a 10x10 mm^2 die. The overmoulding was done with a widely used commercial epoxy moulding compound. A transfer moulding process is used with an 80 bar plunger pressure and an injection temperature of 180 °C. After moulding the samples are cured in an atmospheric oven for four hours at 180 °C. The epoxy moulding compound is removed by means of heated 100% sulfuric acid. After the compound is dissolved the fillers are rinsed away.

7.3 Results

A WLTFP showing a defect during inspection, for example one or multiple cracks, is always considered failed since the hermiticity is compromised. This method yields a binary status: failed or intact. By summarizing all binary values per specific DOE point failure fractions are calculated. Each design point in the DOE is present 36 times. The results are divided into sections according to the

production steps. After wafer fabrication no completely broken WLTFP's were found and therefore the first results below are from the inspection after the wafer thinning.

Wafer thinning

The results from inspection after the wafer thinning step are displayed in four graphs. Each graph holds the results for a certain cap thickness. Figure 6 contains the results from the 1 µm WLTFP's, Figure 7 from the 3 µm WLTFP's, Figure 8 from the 5 µm WLTFP's and Figure 9 from the 7 µm thick WLTFP's. Both the designs with and without supporting pillars are included in this graph.

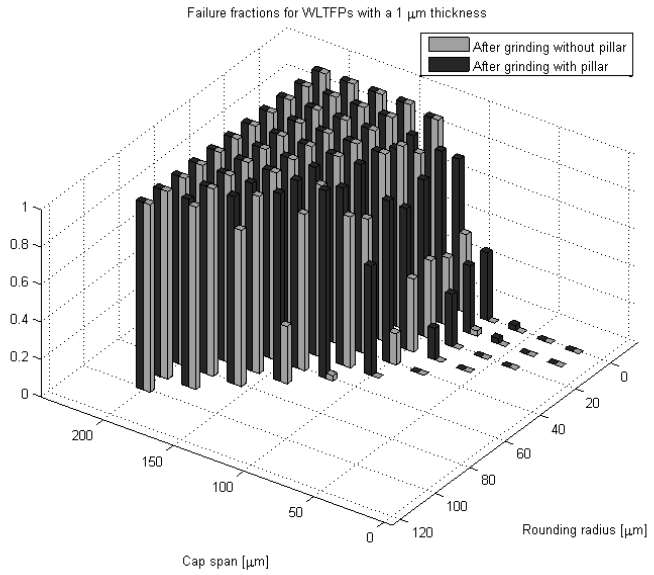

Figure 6 – 1 µm WLTFP thickness failure fractions

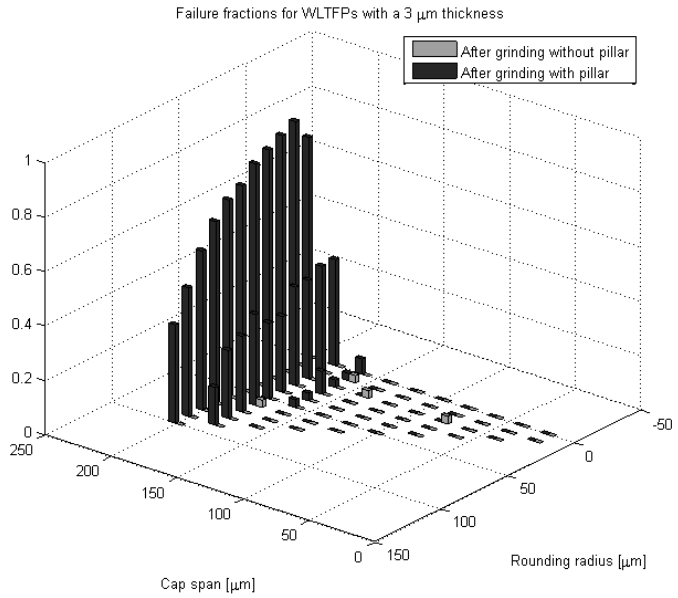

Figure 7 – 3 μm WLTFP thickness failure fractions

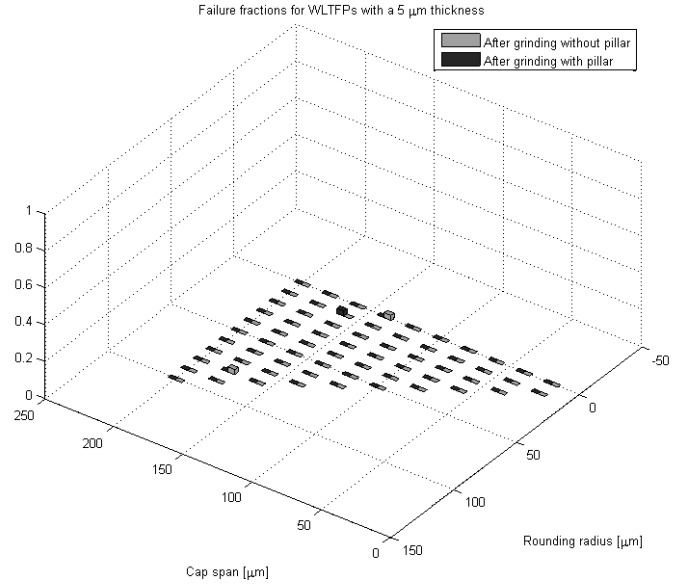

Figure 8 – 5 μm WLTFP thickness failure fractions

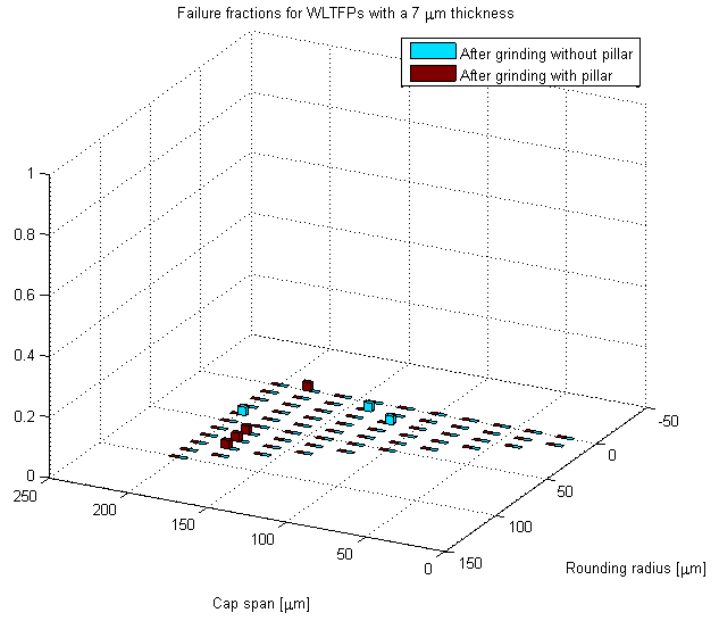

Figure 9 – 7 µm WLTFP thickness failure fractions

Several trends are visible in Figure 6 to Figure 9. A larger span requires a thicker cap layer, this is clearly visible in Figure 6 and Figure 7. Figure 10 also illustrates this.

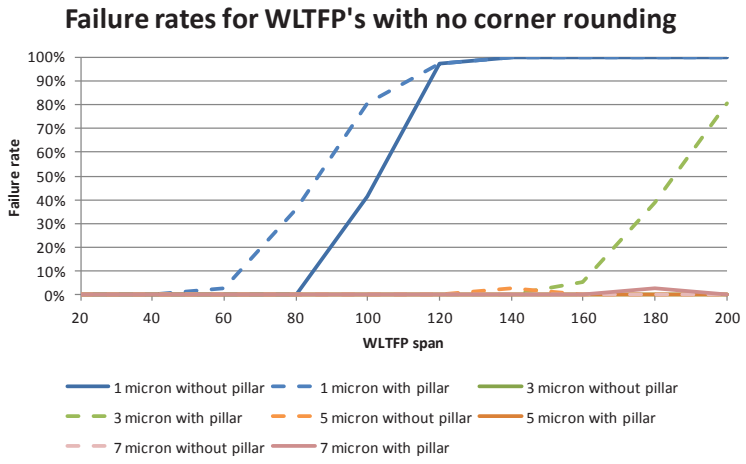

Figure 10 – failure rates for WLTFP's with no corner rounding

A rounded cap is more likely to survive assembly process than a square shaped cap when a supporting pillar is used; this is clearly visible in Figure 7. Figure 11 also depicts this trend in the *3 micron with pillar graph*, with an increasing roundness (corner radius)/(span/2) the failure rates go down.

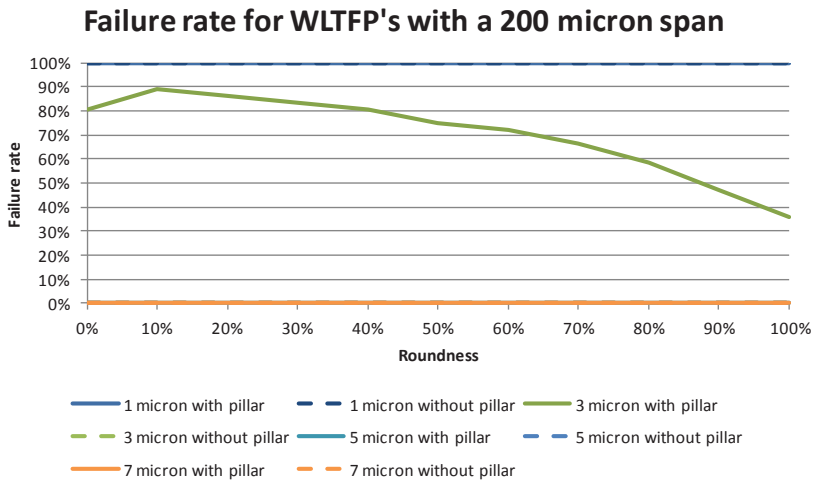

Figure 11 – failure rates for WLTFP's with a 200 micron span with increasing roundness

From Figure 8 and Figure 9 it is clearly visible that both the WLTFP's with and without pillars are not affected by the earlier described wafer thinning process. The presence of pillars can be negative; in Figure 7 it is clearly visible that the presence of pillars affected the survival rates of the WLTFP's in a negative way. The common failure in WLTFP's with a supporting pillar Is a crack around the center pillar. These cracks usually connect the pillar with the etching holes. An example is depicted in Figure 12. The negative effects of a pillar on the WLTFP designs in this experiment are also visible in Figure 7. With increasing roundness the negative effects of the supporting pillar are decreasing.

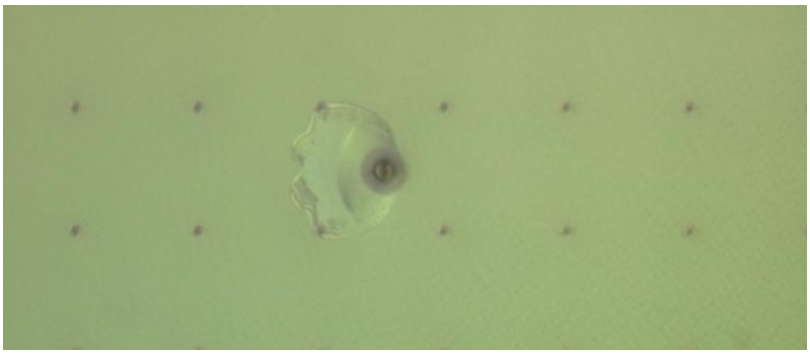

Figure 12 – cracking around the support pillar

The cause for the cracks around the pillars can be found in the thermal mismatch. The WLTFP's without a pillar can bulge upwards in a semi dome shape. The pillar is restricting the upwards movements shaping the top layer in a more donut like form. The higher radius of curvature of the plate in combination with the brittle nature of the Silicon Nitride layer results in cracking and chipping around the pillar.

A FEA is set up to show the differences in stress distributions encountered in the WLTFP. 2 axisymmetric simulations are created of a WLTFP with a 180 µm span and 3 µm thickness. The models are depicted in Figure 13.

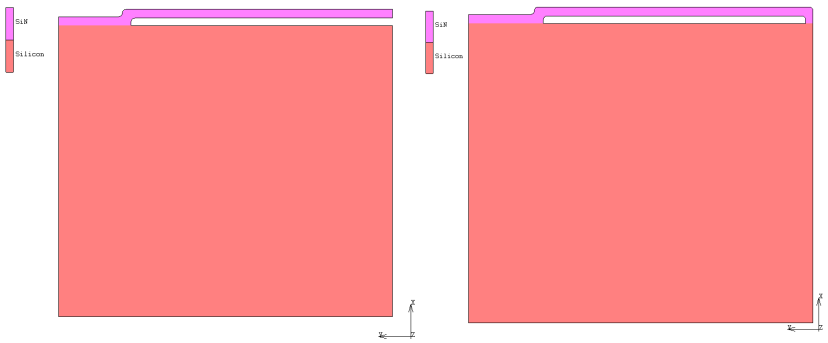

Figure 13 – a WLTFP as seen from the side without pillar (left) and a WLTFP with pillar (right)

The models contain 3640 and 4180 axisymmetric elements (3 and 4-noded elements). The materials used are listed in Table 3.

Table 3 – material parameters

Material	Young's modulus	Poisson ratio	Coefficient of thermal expansion	Material model type
Silicon nitride	190 GPa	0.2	2 ppm/K	Elastic
Silicon	169 GPa	0.23	Table driven: 1 @ -100 °C 1.75 @ -50 °C 2.75 @ 0 °C 3.1 @ 100 °C 3.35 @ 150 °C 3.5 @ 200 °C 3.65 @ 250 °C 3.75 @ 300 °C 4 @ 500 °C	Elastic

An initial stress of 200 MPa is entered in the silicon nitride layer. The model is then cooled from 450 °C to 25 °C. Plots with the maximum principle stress and deformations (amplified) can be found in Figure 14 and Figure 15.

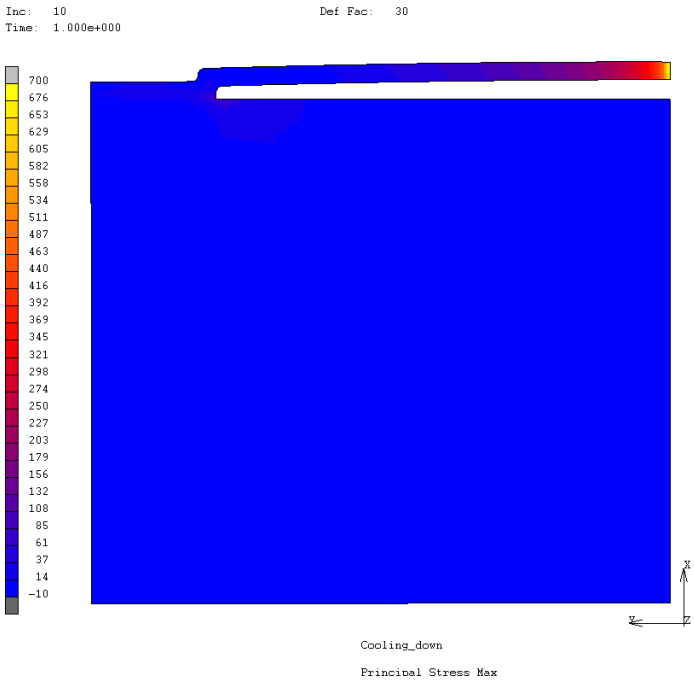

Figure 14 – the WLTFP without pillar

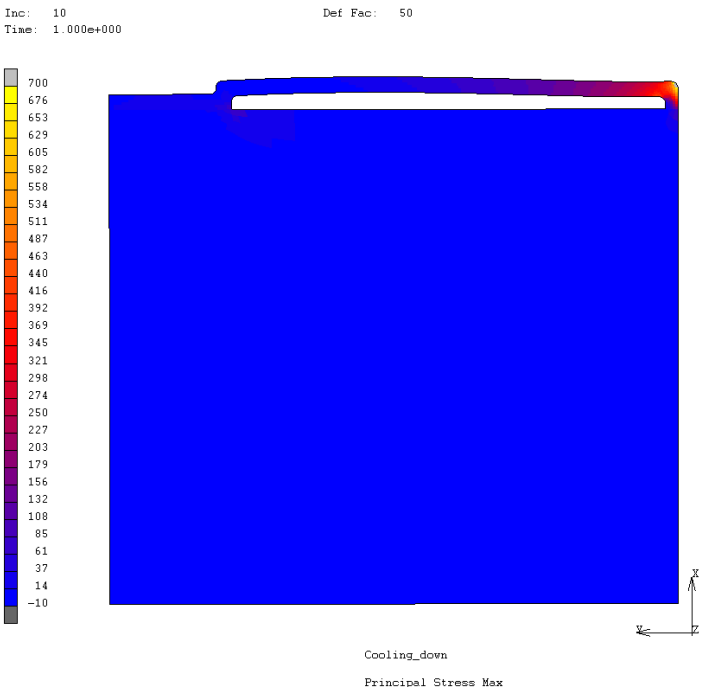

Figure 15 – the WLTFP with central pillar

The donut like shape is clearly visible in Figure 15 where the side and pillar are at the initial location while the free standing part has bulged upwards.

The bulging effect is depicted in

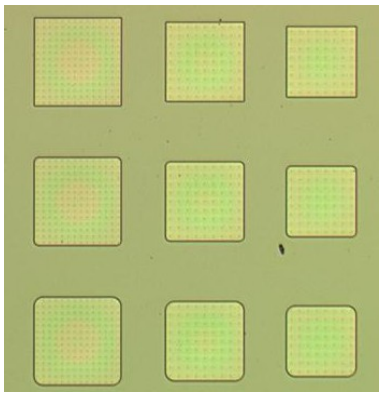

Figure 16 where color rings due to the height differences are visible on WLTFP's without pillar.

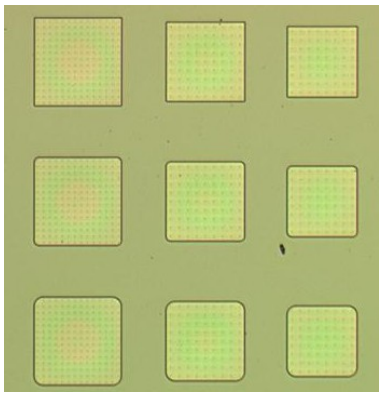

Figure 16 – newton rings on WLTFP's due to bulging

If a WLTFP cracks under the tape application pressure, the process pressure or the peeling force it is also possible that the entire freestanding part is removed.

Based on the failure fractions it is decided not to continue with the 1 and 3 µm samples. The only set of samples that is used for the next steps is the 5 µm as it is the 'weakest' still intact set.

Dicing

Six blocks of samples from the 5 µm WLTFP batch were diced after the wafer thinning inspection. Due to mishandling in the dicing tape application process most WLTFPs with a span larger than 100 µm were broken. Figure 17 shows some WLTFP's that failed during the dicing process due to mishandling.

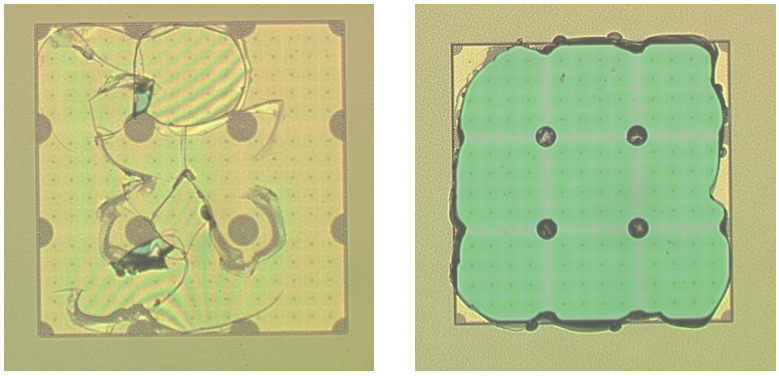

Figure 17 – WLTFP's damaged during the dicing process

The cause of this mishandling is the method of applying the dicing tape in the test environment. This process is schematically depicted in Figure 18.

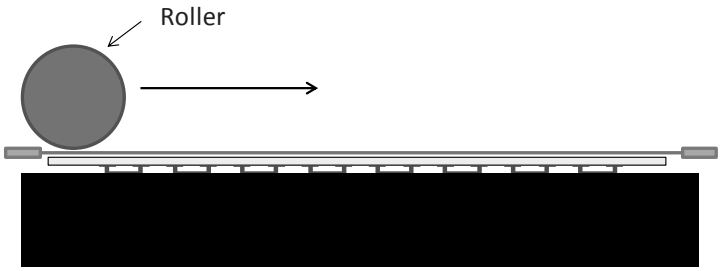

Figure 18 – test environment tape application process

In industrial dicing processes the tape application can also be done in different ways that do less harm to the structures on the wafer. Such a process is depicted in Figure 19.

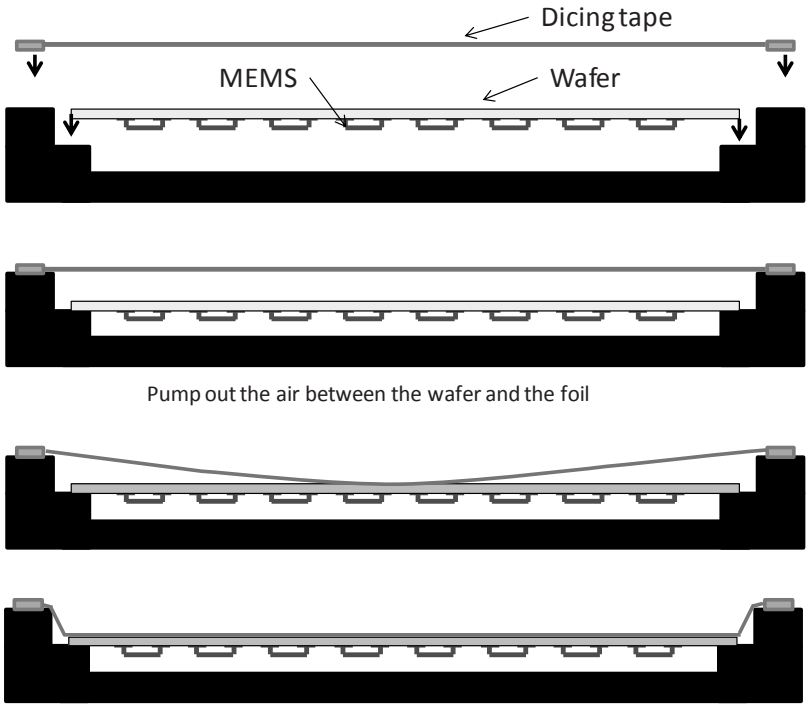

Figure 19 – tape application by means of vacuum; contactless on the active side

Considering the loading pattern in the industrial process depicted in Figure 19 this should do no harm to the WLTFP's. A vacuum on the WLTFP shouldn't

lead to problems such as bursting open since the inside is already at a low pressure.

Although damage was found it is considered to be irrelevant as in mass production a more subtile system is used to apply the tape to the wafer.

Die attach

All WLTFP's were also put through the process of die-attach and overmolding. Figure 20 depicts a strip of QFP100 packages with a mounted WLTFP die.

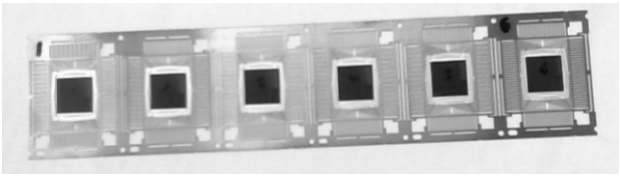

Figure 20 – dies attached to a QFP 100 leadframe strip

When inspected after the die-attach process there were no additional damaged WLTFP's. This supports the earlier conclusion that die attach will not destroy the WLTFP's.

Overmoulding

The overmoulded samples are depicted in Figure 21.

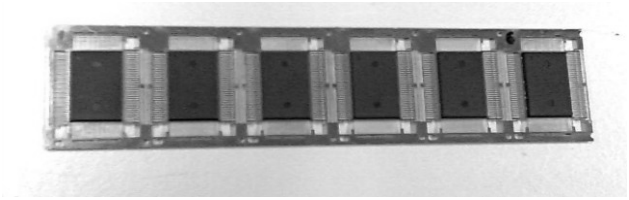

Figure 21 – Overmoulded strip with QFP100 packages

After overmoulding and post mould curing the EMC on top of the die is removed by means of 100% sulfuric acid. The WLTFP's are again inspected and no extra failures were found.

WLTFP's damaged in earlier assembly steps show some additional damage after moulding. Cracks that were initiated in the WLTFP's are aggravated by the moulding process or the post curing step. [1]

7.4 Comparison to Finite Element Analysis

The afore presented results supports the conclusions in chapter 5 concerning the most hazardous assembly processes. Both tape application and tape removal were ranked high and were expected to have a significant influence on the yield during wafer thinning. The experimental results support this conclusion. The overmoulding process was also ranked very high based on the FEA results but, as mentioned in chapter 5, was overestimating the stress significantly due to method of loading. The pressure acting on a WLTFP is not equal for each WLTFP in the mould due to the viscous nature of the epoxy moulding compound. Pressure is needed to flow the epoxy to each corner of the mould. The flow front should, by default, be at atmospheric pressure, meaning that a WLTFP just behind the flow front experiences a low pressure. The injection pressure is the pressure measured in the plunger of the moulding machine. The real experienced pressure by the WLTFP is thus a function of location in the mould [2]. WLTFP's closer to the runner will experience a higher pressure than WLTFP's far away from the runner. When the filling of the cavity is completed, pressure will rise everywhere due to the lack of empty space to fill. However, due to curing the pressure on the WLTFP will not be equal to the injection pressure since the EMC is curing rapidly and reinforcing the cavity. This is caused by the high mould temperature which affects the curing kinetics. The experimental results support the earlier conclusions based on literature leaving the two wafer thinning processes as most critical.

7.5 Design guidelines

From the graphs in Figure 6 to Figure 9 the following design guidelines for square and rounded WLTFP's made of PECVD SiN can be distilled:

- WLTFP packages below with a span of 60 µm or less can be fabricated with thicknesses of 1 µm and above
- WLTFP packages with a span between 60 and 200 µm can be fabricated using WLTFP's with a thickness of 3 µm or more

- Pillars with small radiuses of a few micrometer (as used in this design of experiments) are not beneficial for WLTFP's with a span below 200 µm

- Increasing the corner radius will reduce the likelihood of failure, as illustrated by Figure 7

A graphical representation depicting the save and unsave design points as a function span and thickness is presented in Figure 22. Changing the rounding radius can help as illustrated by Figure 7 in the orange regions. The area outside of the dotted lines is an extrapolation of the experimental results using a FEM stress estimation. The model used to investigate the crack formation around the pillars from section 7.3 is used for this analysis. The span of the 5, 7 and 9 µm is changed such that stress levels found in the orange regions from the table are similar to the stress levels found in the experimentally proven cases.

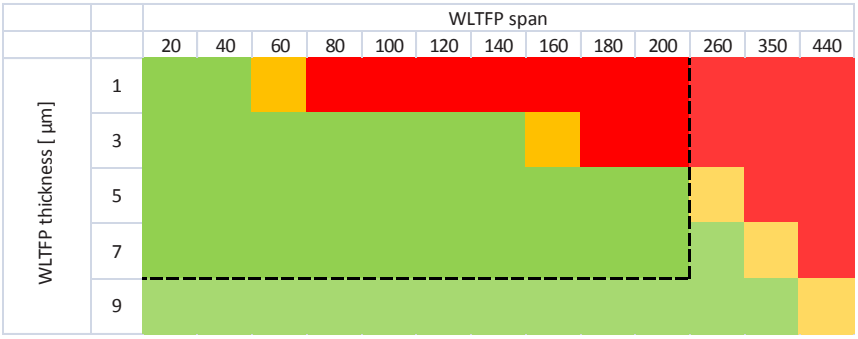

Figure 22 – save and unsave designpoints (save=green; potential hazard=orange; red=unsave)

7.6 Conclusions

The thickness variations in the DOE were not optimal as supported by Figure 8 and Figure 9. Very little damaged WLTFP's were found in these designs. Future experiments could refine and add information to the domain below 5 µm which, from a manufacturing perspective, is interesting since less deposition time is necessary than when using a thick WLTFP layer. Another interesting exploration for future experiments is a variation of pillar diameter since the experiments in [1] show lower stress levels for larger diameter pillars.

Wafer thinning of WLTFP's up to 200 µm can be done with little damage if a WLTFP thickness of 3 µm or more is used. Up to 100 µm WLTFP span one can also use 1 µm thick WLTFP's.

Due to mishandling in the dicing stage no conclusions can be drawn for the WLTFP's larger than 100 µm with respect to the dicing, die-attach and overmoulding process. The WLTFP's smaller than 100 µm did not show failures under dicing, die-attach and overmoulding stresses.

A successful DOE has been performed. The insights yielded can be used by WLTFP designers to design a robust enough WLTFP.

7.7 References

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2. Roellig, M., et al. *Modeling, simulation and calibration of the chip encapsulation molding process*. in *Thermal, Mechanical and Multi-Physics simulation and Experiments in Microelectronics and Microsystems, 2009. EuroSimE 2009. 10th International Conference on*. 2009.

8. Conclusions and recommendations

8.1 Conclusions

The objective of this thesis is to aid MEMS designers in doing a first time right design for Wafer Level Thin Film Packages (WLTFP). To reach this goal a combined experimental and numerical method is used to investigate the WLTFP behavior under the loads encountered during manufacturing, assembly and qualification conditions.

Chapter 2 presented a condensed overview of basic semiconductor manufacturing processes used in WLTFP production. An overview of the main processes needed to package a (MEMS) die in a plastic package is also presented.

In chapter 3 the need for co-design is discussed. Taking the full production and assembly chain into account during the design phase is critical in reaching a cost effective first time right product development and fast time to market. This requires multi-physics and multi-process knowledge. The example illustrates that for MEMS all interfaces are of vital importance and that the assembly can significantly influence the functionality. Contrary to semiconductor products that have a pure electrical function the performance of MEMS is strongly dependant on stresses, temperature and possibly other environmental conditions. This requires a holistic approach in the design phase where both the wafer fabrication and assembly should be taken into account.

Chapter 4 discusses the behavior of thin film materials and the failure modes observed in experiments. An MEMS based material testing method using Electrostatic Pull In (EPI) is evaluated. The experiments show that EPI in combination with WLI can be used for characterization of the copper film Young's modulus and stress, in the 10–50 nm nanometer range. The method can be extended for characterizing other homogeneous thin film materials. The method is fast, practical, robust and requires a basic measurement setup such as a probe station, voltage source and a method to determine the cantilever initial curvature. It is furthermore concluded that the effective copper Young's modulus is size dependent in the 10 to 50 nm range. For single crystalline silicon cantilevers a Young's modulus was measured, which closely

matches the result from Sadeghian et al [1]. This result demonstrates the accurate reproducibility of the experiment.

From experimental observations it can be derived that the root cause of the most threatening processes to the WLTFP is pressure on the WLTFP. Tape adhesives as used in the wafer thinning process can exert significant pulling forces on the WLTFP. The brittle nature and small dimension of the capping layers causes the WLTFP to fail easily under these loads. Based on these experimental observations combined with calculated stress levels from chapter 5 a ranking of the most hazardous assembly processes for WLTFP's can be made, being:

1. Wafer thinning. The most hazardous is the wafer thinning process due to the direct contact with the grinding tape and the process pressure used.

2. Dicing. Dicing is a hazardous process due to the application to the tape and the risk of debris and subsequent cleaning damage. The cut quality also determines the chance of fracture of the entire chip.

3. Overmoulding. The moulding process is less dangerous than the previous two processes but can cause problems in yield due to the different loading levels throughout the mould.

A robust and accurate WLTFP design should consider assembly loads and try to avoid stress concentrations after wafer processing. These stress concentrations can be caused by, for example, CTE (Coefficient of Thermal Expansion) mismatches or poor geometric design.

A further investigation of the foil application and removal in the wafer thinning process are performed in chapter 6. The experiments in this chapter in combination with the foil simulations allow for characterization of the adhesive properties of the foil. The adhesive properties can then be used in the simulations to explore the stress patterns of the designed product before it is actually manufactured.

In chapter 7 a DOE is set up, manufactured and put through assembly steps. Each WLTFP was inspected after the manufacturing steps and detailed information is gathered regarding the most hazardous assembly processes. The results indicate that the thickness values in the DOE were not optimally

spread as two settings did not show any failure. Wafer thinning of WLTFP's up to 200 µm can be done with little damage if a WLTFP thickness of 3 µm or more is used. Up to 100 µm wide WLTFP's one can also use 1 µm thick WLTFP's. Due to mishandling in the dicing stage no conclusions can be drawn for the WLTFP's that are larger than 100 µm with respect to the dicing, die-attach and overmoulding process. The WLTFP's smaller than 100 µm did not show failures under dicing, die-attach and overmoulding stresses. A successful DOE has been performed. The insights yielded can be used by WLTFP designers to design a robust WLTFP. A more detailed overview of feasible and infeasible designs can be found in chapter 7.

The overall conclusion is that the product in chapter 7 and the tool in chapter 4 to 6 provide a helping hand to MEMS designers interested in integrating a WLTFP.

8.2 Recommendations

The recommendations can be split into three parts. The first part concerns extensions of the work done in this thesis. Further investigations into the integration of MEMS die design and package development in combination with optimization methods can improve the design processes. The designspace in chapter 7 and assembly process modeling from chapters 5 and 6 are a starting point in this integration. Future experiments based on the DOE in chapter 7 could refine and add information to the domain below 5 µm which, from a manufacturing perspective, is interesting since less deposition time is necessary than when using a thick WLTFP layer. Another interesting exploration for future experiments is a variation of pillar diameter as explained in chapter 7.

The second recommendation concerns the organizational split made in many semiconductor companies. A split between chip design and package development can be problematic when designing a MEMS. In chapter 3 the need for co-development of packages and MEMS dies was explained. Integrating the two parts of the product design can result in more optimal solutions, to avoid sub optimization. Integrating the design can also help in integrating the functions of the MEMS die and package eventually resulting in either simpler or more robust designs.

The third part concerns the education programs commonly followed by semiconductor designers. In many educational institutions there is a classical split between mechanics, chemistry, physics and electronics. Although many good initiatives are employed to integrate the domains, which is necessary for MEMS designers, a closer relation between, for example the educational programs of Mechanical Engineering and Electrical Engineering, can aid in training better designers. Multidisciplinary departments specifically focusing on semiconductor design, such as DIMES, are a good example of this.

8.3 References

1. Sadeghian, H., et al., *Characterizing size-dependent effective elastic modulus of silicon nanocantilevers using electrostatic pull-in instability.* Appl. Phys. Lett., 2009. **94**(22): p. 221903.

Summary

The world has seen an unrivalled spread of semiconductor technology into virtually any part of society. The main enablers of this semiconductor rush are the decreasing feature size and the constantly decreasing costs of semiconductors. The decreasing costs of semiconductors in general are caused by the smaller feature size, the higher yield and larger production volumes. This has made products containing semiconductors cheaper in production thus reaching a larger market. The smaller feature size enables more computing power in the same volume creating new markets and growing application areas. The increasing number of appliances using semiconductor components is also driving the fast growth of the market. The trend of miniaturization of electronic components also demands the miniaturization and integration of non-electrical functions to allow for large decreases in size, weight and possibly cost. Soon after the first semiconductors were developed the first Micro Electrical Mechanical Systems (MEMS) were also created. In the 1960's and 1970's experiments with MEMS were done in lab environments. MEMS technology can be used to miniaturize non-electrical components thus enabling further system shrinkage and increased function density.

The technologies, experiments and numerical simulations in this thesis provide MEMS designers with a design guideline in the creation process of new Wafer Level Thin Film Package (WLTFP) products as well as an overview of the most likely failure modes and high risk processes in the assembly. WLTFP's are a miniature batch-process and wafer scale encapsulation method for MEMS that need space to move or hold a certain amount of gas.

In the first chapters an overview of the most important processing steps in the production of WLTFP's and the subsequent assembly steps needed to form a plastic encapsulated package is presented. Most common assembly steps included: wafer thinning, chip singulation, die-attach, wire bonding, overmoulding and saw, trim, mark & form. Wafer thinning is necessary to thin the chip to such a thickness that it will fit into the desired package. Chip singulation or dicing is commonly done by a diamond blade saw and makes separates the wafer into individual chips. Die-attach is the placement of the chip onto the carrier, for example a lead frame, by means of a glue. After die-attach connection the IO of the chip to the carrier can be done by wire-bonding. After wire-bonding the package is overflowed by epoxy moulding

compound to protect the chip inside from the environment. After finishing the package and marking it one has a complete product.

In the creation process of a new MEMS product the design team is faced with a multi-scale, multi-physics and multi-timescale challenge. Nanometer dimensions can impact a millimeter size product and hours of operation can change a MEMS that performs microsecond measurements. To address this challenge an integrated design process is needed that covers the chip and wafer design as well as the package and all of the intermediate processes. An example of the influences from the package on the chip is calculated and shown in chapter three.

In chapter four the properties of thin layers are investigated. In this investigation copper thin film are deposited on freestanding micro cantilevers. The samples are analyzed with white light interferometry to obtain the initial geometry properties and cantilever warpage. Using electrostatic pull-in to pull down the cantilever to the substrate the pull-in voltage is obtained. The stiffness of the two layer system can be derived from the pull-in voltage. Copper film thicknesses of 10 and 50 nanometer are measured and a size-dependant stiffness is proven.

During the assembly of a WLTFP several failure modes are found. In the wafer thinning process the application of wafer thinning tape to the active side of the wafer can easily break many WLTFP's. This can happen during the application or for example the removal of the tape. The placement of the wafer on dicing foil is also a potential risk as it leaves the MEMS exposed to the water jet of the dicing machine. Wire-bonding can be hazardous to MEMS sensitive to resonance, this risk can relatively easy be mitigated by calculation of eigenmodes and eigenfrequencies. The overmoulding process and the associated process pressure can be hazardous to for example membranes or large WLTFP's due to the static pressure on the cavity.

The numerical simulations developed in chapter five provide a toolbox to check for weak spots in the design and investigate changes by virtual prototyping instead of physical prototyping. The simulations also include wafer foil application and removal simulation. The use of cohesive zones allows for a detailed investigation of the loads on the WLTFP.

In chapter six the interface properties of the wafer thinning foil are investigated by means of a peeling experiment combined with numerical simulations. The characterization method yields interface properties that serve as input for afore mentioned numerical simulations.

The Design of Experiments presented in chapter seven investigates the influence four major design choices on the likelihood of survival during assembly. The span of the WLTFP, the corner rounding radius, cap thickness and presence of a pillar are investigated. After all 18720 samples were evaluated a design guidelines was derived.

The design guideline in combination with the numerical simulations provides the MEMS design community with tools during the chip-design stage. This aids to the integrated approach of designing new MEMS and reduces the time to market and number of design iterations needed.

Samenvatting

De wereld heeft een ongekende verspreiding van halfgeleiders meegemaakt in vrijwel ieder deel van de maatschappij. De factoren die deze enorme verspreiding van halfgeleiders mogelijk maken zijn de afnemende grootte en de dalende kosten. De kosten nemen af door de hoge opbrengsten en door de efficiëntie van fabricageprocessen en de groeiende batchgrootte. Ook hier draagt de afnemende grootte aan bij. Als gevolg hiervan zijn producten die gebaseerd zijn op halfgeleiders ook goedkoper geworden in productie en bereiken deze producten daarom op hun beurt weer een grotere markt. De toenemende rekenkracht in een gelijkblijvend volume creëert nieuwe markten en applicatiegebieden. Het toenemend aantal halfgeleidertoepassingen op zijn beurt veroorzaakt ook een groei in de markt. De miniaturisatietrend heeft ook tot gevolg dat verdere integratie van niet elektrische functionaliteit nodig is om grote afnamen in gewicht, afmetingen en kosten te realiseren. Kort na de ontwikkeling van de eerste halfgeleiders ontstonden ook de eerste Micro Elektrische Mechanische Systemen (MEMS). In de jaren ‘60 en ’70 werden in laboratoria experimenten gedaan met MEMS. MEMS technologie kan gebruikt worden om niet elektrische functionaliteit te integreren en zo de toename van functionaliteit te realiseren en het totaalproduct te verkleinen.

Dit proefschrift behandelt een specifiek type MEMS: Waferschaal Dunne Film Verpakkingen (WDFV). WDFV’s zijn in batch geproduceerde miniatuur verpakkingen voor MEMS die een holle ruimte vereisen voor bewegende onderdelen of voor het vasthouden van een bepaald gas. De in dit proefschrift besproken technieken, experimenten en numerieke analyses geven MEMS ontwerpers een ontwerprichtlijn. Ook wordt een overzicht van de meest waarschijnlijke faalmodi en risicovolle processen tijdens de assemblage gegeven.

In de eerste hoofdstukken wordt een overzicht van de belangrijkste stappen in de productie van WDFV’s gegeven en de daarop volgende assemblagestappen tot een plastic omhuld product. De meest gebruikelijke assemblagestappen zijn: waferverdunning, chip scheiding, chip plaatsing, draadbonden, spuitgieten en zagen, bijwerken, markeren en vormen. Waferverdunning is een proces waarbij de chip dunner geslepen wordt tot een zodanige dikte dat hij in een (plastic) omhulsel past. Chip scheiding gebeurt vaak met behulp van een diamantzaag of lasersnijder waarmee de wafer in

individuele chips wordt gedeeld. Chip plaatsing is het proces waarbij de chip geplaatst wordt op een drager, bijvoorbeeld een koperframe, met behulp van een lijm. Na het plaatsen van de chip kunnen de elektrische verbindingen van de chip door middel van het draadbondproces verbonden worden met de pootjes of contactvlakken die aan de buitenkant van het omhulsel komen te zitten. Na draadbonden wordt de chip met een spuitgietproces omhuld met plastic. Na het losknippen, het vormen van de pootjes en het markeren van het product is het product gereed.

In het ontwerpproces van een nieuw MEMS product staat het ontwerpteam voor een multischaal, multifysica en multi-tijdsschaal uitdaging. Afmetingen van nanometers kunnen invloed hebben op een millimeters groot product en vele uren van gebruik kunnen een MEMS systeem dat microseconde lange metingen doet beïnvloeden. Om deze uitdaging aan te gaan is een geïntegreerde aanpak nodig waarbij zowel de chip, de wafer en de verpakking ontwikkeld worden als alle tussenliggende processen. Een voorbeeld van de invloeden van de verpakking op de chip wordt geïllustreerd in hoofdstuk drie.

In hoofdstuk vier worden de eigenschappen van dunne lagen onderzocht. In dit onderzoek worden koperen filmlagen aangebracht op vrijhangende microbalken. De microbalken worden geanalyseerd met Wit Licht Interferometrie (WLI) om de initiële vervorming te bepalen. Met behulp van elektrostatische aantrekkingskracht wordt het pull-in voltage bepaald. De stijfheid van het tweelaagssysteem kan vervolgens worden afgeleid uit het pull-in voltage. Koperfilms met een dikte van 10 en 50 nanometer zijn gemeten en een dikteafhankelijke stijfheid is daarbij bewezen.

Gedurende de assemblage van een WDFV kunnen verschillende faalmodi worden aangetroffen. In het waferverdunningsproces wordt een plakfolie aangebracht op de zijde van de wafer die de structuren bevat. Het aanbrengen en verwijderen van dit plakfolie kan de structuren beschadigen. Het scheiden van de wafer in individuele chips kan schade opleveren omdat de MEMS onderworpen wordt aan de waterstraal van de zaagmachine. Draadbonden kan schade veroorzaken in de fragiele MEMS door resonantie van de structuur, veroorzaakt door de bondfrequentie. Dit probleem kan worden opgelost door een resonantiefrequentieanalyse gevolgd door eventuele aanpassingen van het proces of het ontwerp. Het spuitgietproces en de bijbehorende

procesdruk kan schadelijk zijn voor membramen en grote WDFV's vanwege de grote druk op de dunne vrijstaande lagen.

De in hoofdstuk vijf ontwikkelde numerieke analyses vormen een gereedschapset waarmee ontwerpen kunnen worden geëvalueerd en wijzigingen vooraf kunnen worden onderzocht zonder fysieke realisatie van de prototypes. De analyses bevatten ook simulaties voor het aanbrengen en verwijderen van de plakfolie nodig voor het slijpen van de wafer. Het gebruik van 'cohesive zones' maakt een gedetailleerd onderzoek van de belastingen op de WDFV mogelijk.

In hoofdstuk zes worden de eigenschappen van het contact tussen de wafer en het plakfolie onderzocht met behulp van een experiment en numerieke analyse. Deze karakteriseringsmethode levert de contacteigenschappen op die nodig zijn voor de eerder genoemde numerieke analyses.

Het experimenteel ontwerp uit hoofdstuk zeven onderzoekt de invloed van vier grote ontwerpparameters op de waarschijnlijkheid dat de WDFV alle assemblageprocessen overleeft. De overspanning, hoekradius, laagdikte en aanwezigheid van een steunpilaar worden onderzocht. Alle 18720 WDFV's worden onderzocht en een ontwerprichtlijn is beschreven.

De ontwerprichtlijn in combinatie met de numerieke analyses die in dit proefschrift ontwikkeld zijn vormen voor de ontwerpteams van MEMS een gereedschapset voor het ontwikkelen hiervan. Dit helpt bij het realiseren van de benodigde integrale aanpak bij het ontwerpen van MEMS en reduceert het aantal benodigde iteraties in het ontwerpproces. Dit resulteert in een efficiënter, goedkoper en verkort ontwikkelingsproces.

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Curriculum Vitae

Jeroen Zaal was born in Heemstede, the Netherlands, on March 5, 1985. From 1996 to 2002 he attended Atheneum College Hageveld in Heemstede. In 2002 he started his bachelor education in Mechanical Engineering and received his Masters degree with honours in October 2007 from the faculty of 3mE, part of the Delft University of Technology.

From October 2007 to January 2011 he was employed as PhD student by the Delft University of Technology working on this research as part of the Dutch innovation project MEMSLand. During this time he worked mainly at the office location of MEMSLand-partners NXP Semiconductors in Nijmegen and was supervised by Dr.Ir. W.D. van Driel and Prof Dr. G.Q. Zhang.

Since January 2011 he joined Philips Lighting in the LED Platform Development group part of the business line Light Sources & Electronics as reliability engineer. His current work involves failure analysis and root cause analysis of LED products and the prediction of expected lifetimes for new products.