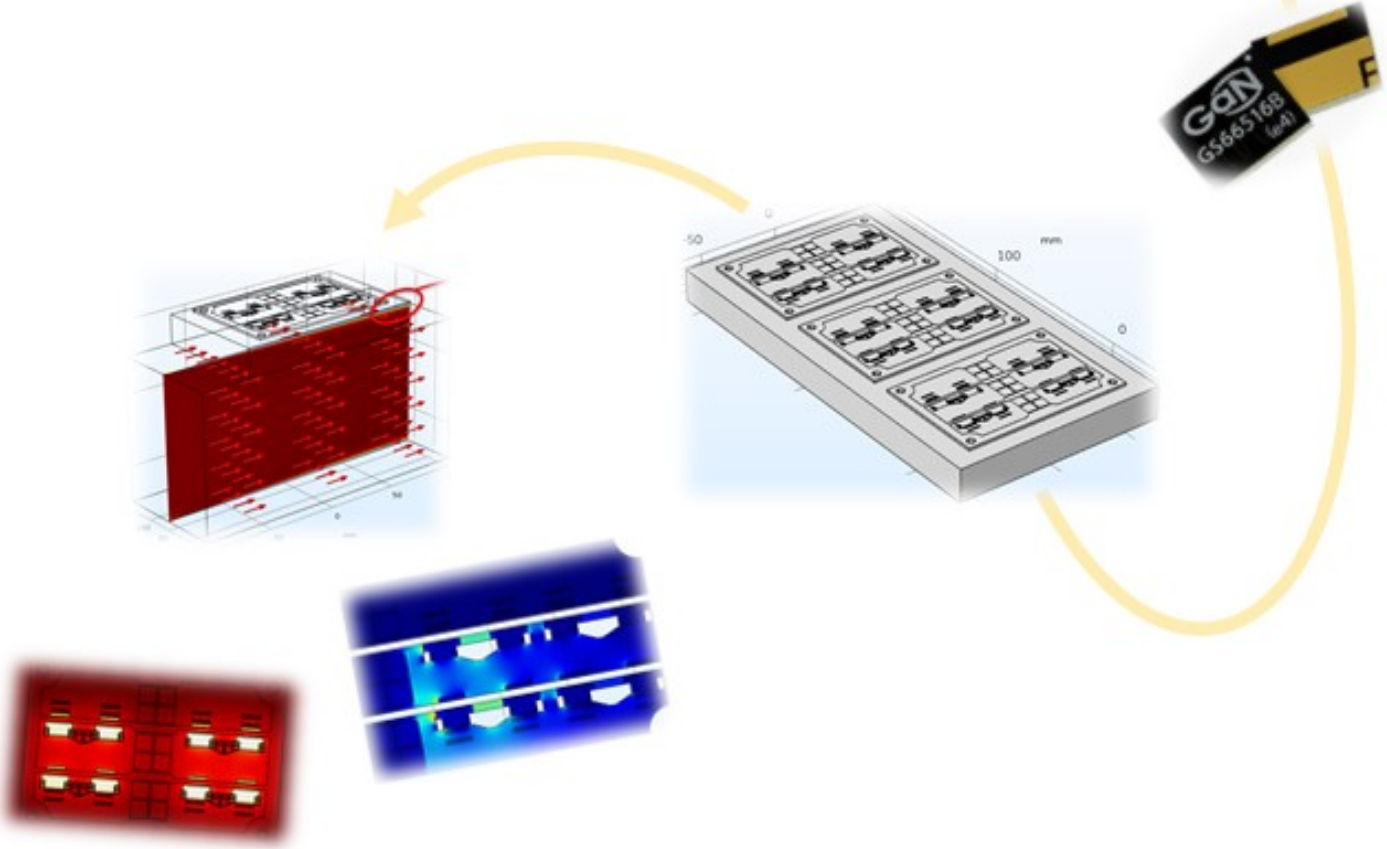
Modelling and design of a GaN based motor drive for the Nuna solar car

Lu Wang

Technische Universiteit Delft



TU Delft Delft University of Technology

Challenge the future

Modelling and design of a GaN based motor drive for the Nuna solar car

by

Lu Wang

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Supervisor:	Prof. dr. ir. Pavol Bauer,	TU Delft
Daily supervisor:	Dr. ir. Zian Qin,	TU Delft
	Dr. Jianning Dong,	TU Delft
Thesis committee:	Prof. dr. ir. Pavol Bauer,	TU Delft
	Dr. ir. Zian Qin,	TU Delft
	Dr. Jianning Dong,	TU Delft
	Dr. ir. Jose Rueda Torres,	TU Delft

TU Delft Delft University of Technology

Abstract

In recent years, electrical vehicle (EV) starts showing its unique advantages that the conventional combustion vehicles do not have. Together with the increasing interests on EV, the motor drive with higher efficiency and lighter weight also becomes more attractive. To reduce the time and cost for the development, the project is aiming for the modelling of the motor drive, with which the voltage and current stress, power loss, thermal and electromagnetic performance can all be evaluated.

In the meanwhile, the Nuon Solar Team is also interested in designing a new motor drive with a higher efficiency and less weight. A promising solution is to apply the wide band gap (WBG) components including gallium nitride (GaN) and silicon carbide (SiC) in the motor drive. Thus, the characteristics of the WBG components especially the GaN MOSFET is investigated as well to clarify the feasibility of applying the WBG components to the application.

In overview, a systematic approach for the design of a GaN-based 4-parallel MOSFET motor drive is presented. The development of the motor drive is divided into 3 parts that are the 1-D modelling, hardware design and 3-D modelling. 1-D or 2-D model is sufficient to simulate the voltage and current stress, power loss, and highly simplified thermal and the electromagnetic performance. Only by using 3-D model the thermal and electromagnetic distribution can be thoroughly studied.

As the beginning, the load profile analysis is done to clarify the design requirements. Based on the requirements, several design candidates are proposed. Then, the 1-D modelling on the control system, power loss and thermal performance are done for each design candidates respectively. Built on the modelling and load profile, the efficiency and temperature of the motor drive in the competition WSC are predicted for each design candidates respectively. Among all the design candidates, the one with the highest efficiency and acceptable maximum junction temperature is selected. Based on the selection, the hardware design proceeds. Among all the hardware design, the layout design of the power stage is most important because it is used as the geometric shape in the 3-D modelling. Three different types of layout of the power stage are proposed.

To make the simulation closer to the reality, in the 3-D modelling, the thermal performance is coupled with the electromagnetic performance and the computational fluid dynamic (CFD). Through the 3-D electromagnetic modelling, the current distribution on the power stage with a certain layout is simulated. Based on the output result, the heat transfer is coupled with the CFD to analyze the heat transfer coefficient on the surface that has the forced convective cooling. Built on the output result, the stationary and time dependent heat transfer study are carried out to evaluate the temperature distribution when the car is cruising and the maximum junction temperature occurring when the large surge current comes. Finally, according to the simulated multi-physical performances, one of the three types of power stages is selected for the PCB construction.

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My gratitude also goes out to the Nuon Solar Team. The team members are very kind and willing to offer help to me.

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Lu Wang
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1 Introduction

1.1. Background

1.1.1. General background

In recent years, with the development of the battery technology as well as the worldwide increasing demands on environmental protection, electrical vehicle (EV) starts showing its unique advantages that the conventional combustion vehicles do not have. Together with the increasing interests on EV, the motor drive with higher efficiency and lighter weight also becomes more attractive. Nevertheless, compared with a single nice design of a motor drive, the methods leading to the nice design is of more concern because it is reproducible for the other design based on the different applications. Therefore, this thesis project seeks to establish a method on how to make the design of a motor drive better directed at the users' requirements.

1.1.2. Cooperation with Nuon solar team

In the meanwhile, Nuon solar team is also interested in designing a new motor drive for the possible changes in the coming future. Annually, the team competes with the other teams in the World Solar Challenge (WSC) which is a racing marathon (e.g. 3000km for the WSC 2017[3]) among solar cars. During the competition, solar energy is the only energy source except the small initially stored energy in the battery. The goal of the team is to arrive at the end point as fast as possible.

Therefore, the team needs the efficiency of the whole power-train to be as high as possible, which releases the pressure on the size of the PV panel and thereby the size and weight of the solar car. A simplified structure of the power-train of the Nuna solar car is shown in the figure 1.1. As it is shown, the motor drive transmits energy from the power source (Li-ion battery) to the brushless direct current motor (BLDCM). The efficiency of the motor drive has significant impact on the efficiency of the power-train. Besides, reducing the power loss produced by the motor drive also decreases the requirements on the cooling of the motor drive, which means smaller and lighter heatsink is needed.

Currently, the team uses a commercial motor drive (WaveSculptor 22 Motor Drive). However, as this one is not dedicated to the needs of the team, there is a room for improving the efficiency and reducing the weight of the motor drive by making the design directed at the desires. Nevertheless, because of the efficiency of the existing motor drive is already very high (roughly 98%), a risky design has to be considered to further increase the efficiency. A promising solution is to apply the wide band gap (WBG) components including gallium nitride (GaN) and silicon carbide (SiC) in the motor drive.

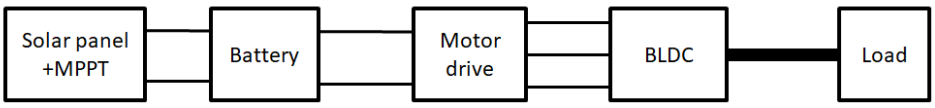


Figure 1.1: The simplified power train of the Nuna solar car

1.2. Research objectives

Macroscopically speaking, the thesis is the first step of a bigger project which tries to develop a design tool for motor drive. Therefore, it is aiming for the modelling of the motor drive, with which the voltage and current stress, power loss, thermal and electromagnetic performance can all be evaluated.

1-D or 2-D model is sufficient to simulate the voltage and current stress, power loss, and highly simplified thermal and the electromagnetic performance. Only by using 3-D model the thermal and electromagnetic distribution can be thoroughly studied.

In summary, the research objectives of this thesis project are:

1. 1-D modelling including control system model, 1-D thermal model and power loss model of the motor drive.
2. The characteristic study of the novel semiconductor (GaN) MOSFET used in such an application.
3. 3-D multi-physics modelling that couples thermal performance with the electromagnetic performance and computational fluid dynamics (CFD).

1.3. Overview on the investigation approach

A design flow chart 1.2 shows the overview of the approach throughout this master thesis project. In overview, the investigation approach comprises three paralleling paths starting with certain specifications which are labeled with red blocks and giving their outputs that are labeled with green blocks. Although the three paths are depicted in parallel, they have logical sequence which is set forth below.

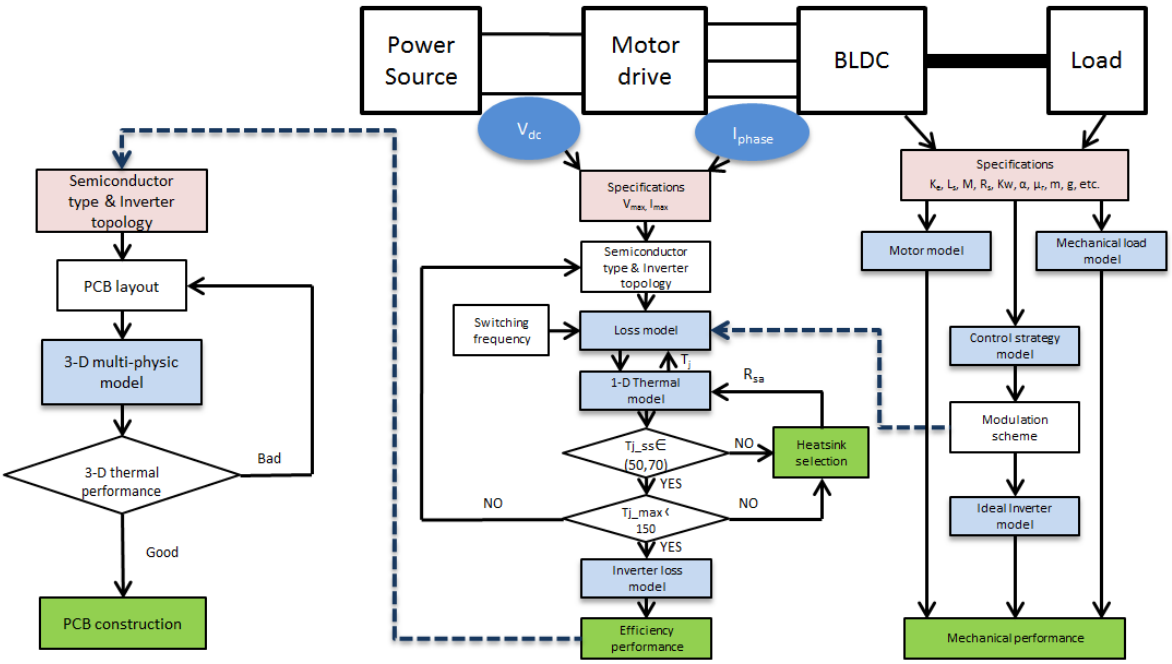


Figure 1.2: Design flow chart of the project

In order to make a design of a motor drive, the first step is clarifying the requirements and specifications. Afterwards, the control strategy and the modulation method are decided because they give the switching pulse pattern and the phase current which determines the power loss of the motor drive.

For the next step, several promising transistor candidates and inverter topologies are proposed based on the load profile. Then, 1-D models are constructed because they avoid struggling in some unnecessary details and save the simulation time. At the end of this stage, an efficiency and maximum junction temperature evaluation on the different design candidates are done. Based on the evaluation result, the feasible design candidate with the highest efficiency is selected.

Then, the hardware design is done based on the chosen candidate. Afterwards, the layout of the PCB is designed and used for the 3-D modelling, in which the cooling system is also included. In the

simulation using 3-D models, studies on the multi-physics including electromagnetic field, heat transfer and CFD are coupled. Based on the 3-D models, the current distribution, the thermal distribution and the maximum junction temperature resulting from the large surge current are evaluated. The performance of the motor drive with three types of layout are compared. A relative better layout is selected for the hardware construction.

1.4. Project contribution

The thesis project has contribution in the field of the modelling and design of the motor drive based on GaN MOSFET. In details, the contributions are:

1. A method for the efficiency and junction temperature analysis of a design of motor drive is developed. The method uses 1-D models to estimate the junction temperature of the MOSFETs to check the feasibility of the design for a certain application. Based on that, a 1-D model without small time step is used to estimate the efficiency of a certain design of motor drive in a time scale of one day.
2. The layout of the power converter is designed. The power converter uses 4-parallel MOSFETs in one position and the design tries to make the temperature and current more evenly distributed. Besides, it also tries to minimize the value of the parasitic inductance of PCB trace to increase the reliability of the motor drive using high switching frequency.
3. A method for the multi-physical (i.e. thermal and electromagnetic) analysis on the performance of the power stage of the motor drive is developed. The method analyzes the current distribution on the power stage with a certain layout under the influence of the induced electromagnetic field. Based on the output result, the heat transfer is coupled with the CFD to analyze the heat transfer coefficient on the surface that has the forced convective cooling. Built on the output result, the stationary and time dependent heat transfer study are carried out to evaluate the temperature distribution when the car is cruising and the maximum junction temperature occurring when the large surge current comes.
4. Based on the output result of the multi-physical simulation, the temperature and current distribution on the power stage with three types of layout are compared. The influence of the symmetry of the layout of the power stage on the even distribution of the temperature and current is evaluated.

1.5. Structure of the work

The thesis consists of the following five part:

1. Chapter 1 introduces the background, the research objectives, the overview on the investigation approach and the contributions of the thesis project.
2. Chapter 2 presents the load profile analysis and the 1-D modelling of the motor drive. Built on the implemented models, efficiency and feasibility analysis on several design candidates are done and their performance are compared. The switching frequency, the control strategy, the type of the transistor and the topology of the inverter is decided at the end of this step.
3. Chapter 3 presents the hardware design of the motor drive based on the results presented in the chapter 2. The control circuit is not included as a commercial product is decided to be used. The other parts are designed based on the characteristics of the used commercial product. The designs of the sensing circuit, protection circuit only involve schematic design without PCB layout design. Only the PCB layout of the power stage and the gate driver are designed.
4. Chapter 4 presents the multi-physical 3-D modeling and the evaluation based on the implemented models. The current distribution on the three types of power stage are compared firstly. Given the current distribution, the power loss of the 4-parallel MOSFETs is known. A simulation that couples the CFD with the heat transfer is carried out to estimate the heat transfer coefficient. Finally, built on the output result, a stationary and a time-dependent heat transfer study are carried out to evaluate the temperature distribution, MOSFET temperature at the cruising speed and the maximum junction temperature in the large surge current condition.

5. Chapter 5 summarizes the work and draws the conclusions based on the output results of every stage.

2

1-D modelling & evaluation

The modelling is crucial for understanding the insight which in return contributes to a good design in reality. Besides, compared with prototyping, modelling normally saves time and cost. Because of these advantages, modelling is the first step in this design.

In this chapter, the 1-D modelling of the motor drive is discussed. In overview, the content includes:

- the concrete design requirements derived from the load profile analysis.
- the modelling of the control system involving the models of the BLDCM and the mechanical load.
- the power loss modelling of the MOSFETs and the inverter.
- the 1-D thermal modelling of the motor drive.
- the thermal aspect evaluation of all the design candidates based on the modelling.
- the efficiency prediction of all the design candidates based on the modelling.

2.1. The specifications of the design

At the beginning of the design, it is very necessary to make the needs from the Nuon solar team clear. As this motor drive is designed for the racing car Nuna which is used for the WSC. Therefore, the recorded data in the WSC 2017 is used to do load profile analysis to clarify the specifications of the design.

2.1.1. Overview on the constraints in the design

From the hardware design point of view, the very general constraints on the motor drive design can be concluded as the maximum voltage rating and the maximum current rating. The requirements on the two need to be specified to properly select the transistors and the topology of the motor drive. Assuming a typical motor drive (inverter) typology in the figure 2.1 is used, the maximum DC bus voltage is the maximum voltage on the six transistors. As for the maximum current through the transistors, it equals the maximum phase current.

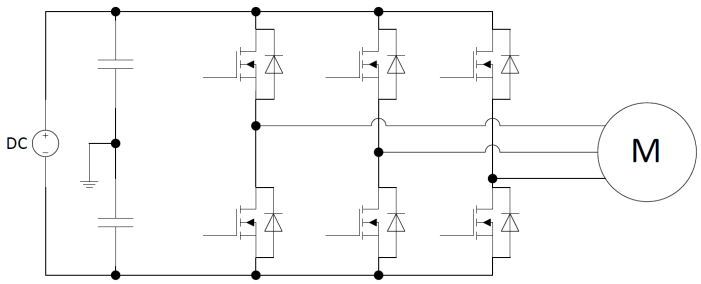


Figure 2.1: A typical motor drive typology

2.1.2. Load profile analysis

From the discussion above, it is clear that the necessary information to be know is the DC bus voltage and the maximum phase current.

During the WSC 2017, Nuon solar team recorded the operation status of the Nuna 9 which is the racing car in that year. The recorded data includes the DC bus voltage, the DC bus current, the amplitude of the phase current of the motor, the speed of the Nuna 9 and the time at which this data is recorded. Given with this data source, the load profile analysis is done. In the table 2.1 some general information that indicates the working status of the motor drive is shown. The more detailed plotting of this data is shown in the appendix A.

Table 2.1: The load profile analysis results: general information

Maximum phase current (A)	DC bus voltage (V)	Cruising speed (km/h)	Phase current(RMS) at the cruising speed (A)	Power rating at the cruising speed (W)
117	147-126	80-90	10-20	800-900

Besides, for the maximum junction temperature evaluation, the length of the period during which the maximum current lasts is also necessary.

In the table 2.2, the different levels of the amplitude of the phase current in the 5 days together with their lasting time are listed. Based on the table 2.2, a statistic of the duration time of the phase current with different levels is shown in the figure 2.2. As it is shown, over 98% of the total time, the car runs with a phase current lower than 50A. Therefore, because of the small portion of time occupied by the high current, the maximum continuous time of the high current is of more value compared with the total time. Thus, the maximum continuous time of these high current is also listed.

According to the statistic, although the maximum current through the transistor is 117A, the duration of this extreme case is rather short. It is not necessary to make the motor drive operate with this current condition. The validation of this statement will be discussed in the section 2.2 where a simulation is done to check if a current as small as 60A is enough to satisfy the acceleration requirement. Nevertheless, from ensuring the performance of the motor drive meet the needs point of view, this extreme current condition is still considered as the maximum current rating of the motor drive to be designed. In summary, the maximum voltage rating is 150V and the maximum current rating is 120A.

Table 2.2: Statistic of the duration time of different levels of the phase current (amplitude)

Phase current (amplitude) level (A)	Total time (s)	Phase current (amplitude) level (A)	Maximum continuous time (s)
0-10	37077.37	>0	-
10-20	74456.65	>10	-
20-30	13456.06	>20	-
30-40	3872.75	>30	-
40-50	1651.71	>40	-
50-60	925.00	>50	51.17
60-70	524.85	>60	50.34
70-80	293.96	>70	39.60
80-90	270.11	>80	34.50
90-100	194.68	>90	19.47
100-110	56.07	>100	9.58
110-117	14.76	>110	4.79

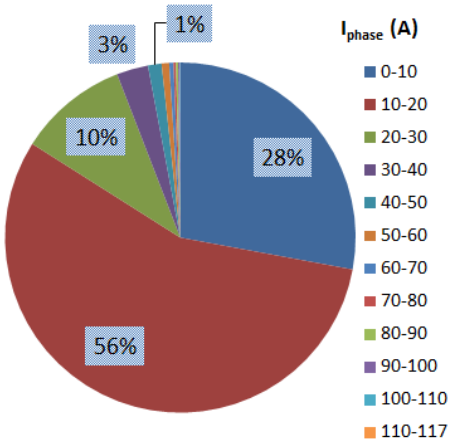


Figure 2.2: Statistic of the duration time of different levels of the phase current (amplitude)

2.1.3. Selection of the transistors and inverter topology

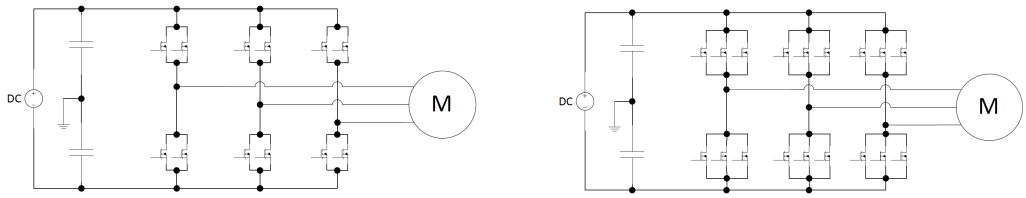
After clarifying the voltage and current stress of the motor drive to be designed, the commercial transistors that meet the stress requirements can be selected. As mentioned previously, in order to further increase the efficiency, which currently is about 98%, of the motor drive the novel semiconductors are considered. However, as the maximum current rating of the existing commercial GaN and SiC MOSFET is still at low level. Therefore, the choice of the feasible candidate is rather limited. As the result, one GaN MOSFET and three SiC MOSFETs that barely meet the maximum current rating requirement are chosen and listed in the table 2.3[4–8]. Except the novel semiconductors, one conventional Si MOSFET is also chosen for the comparison. As it is shown, the maximum current rating of all the candidates are all smaller than 120A even when the junction temperature is as low as $25°C$. When the junction temperature is as high as $100°C$, the maximum current rating of the MOSFETs will decrease to a lower level. This characteristic worsen the feasibility of these candidates because higher current also means higher power loss and therefore higher junction temperature.

In order to settle this problem, the typical inverter typology has to be modified. A promising solution is paralleling the transistors to get a higher maximum current rating. By doing simple calculation, it is easy to find out that using double parallel MOSFETs can satisfy the maximum current requirement for some transistor candidates. However, for the rest, using triple parallel MOSFETs is necessary. However, by doing this, the total power loss of the motor drive is changed. The influence of paralleling MOSFETs on the efficiency of the motor drive need to be evaluated. The result on the efficiency analysis is discussed in the section 2.5.

Table 2.3: Information on the transistor candidates

Manufacturer	Type	Part No.	$I_{ds,max}(A)$ $(T_j = 25°C)$	$I_{ds,max}(A)$ $(T_j = 100°C)$	$T_{j,max}$ $(°C)$	$V_{ds,max}$ (V)	$R_{ds}(m\Omega)$ (typical)
GaN Systems	GaN	GS66516B	60	47	150	650	25
Rohm	SiC	SCT3022AL	93	65	150	650	22
Cree	SiC	C2M0025120D	90	60	150	1200	25
STMicroelectronics	SiC	SCTWA50N120	65	50	200	1200	52
Infineon	Si	IPT60R028G7	75	47	150	600	24

From hardware design point of view, with the increasing number of the parallel MOSFETs, the design difficulty becomes harder and harder. This results from the critical requirement on the simultaneous switching of all the parallel MOSFETs. Otherwise, the earlier switched MOSFETs would fail on the too much current through them. Therefore, it is very challenging to use too many parallel MOSFETs. Based on this reason, the design is kept simple and only the typologies with two parallel MOSFETs and three parallel MOSFETs, which two are shown in the figure 2.3a and figure 2.3b, are considered.



(a) Double parallel MOSFETs **(b)** Triple parallel MOSFETs

Figure 2.3: The inverter topology candidates

As mentioned above, both the semiconductor and inverter typology candidates are specified.Consequently, there are ten kinds of promising design. For the next step, it is necessary to compare the their performance on the temperature and efficiency to check their feasibility. For both the temperature and efficiency evaluation, a power loss model of the inverter is needed.

To implement an inverter loss model, both the power loss model of the MOSFET and the control system model are needed. Compared with the MOSFET loss model, the control system model is prior because it influences the loss in the system level.

2.2. Control strategy

For the control method of brushless DC motor (BLDCM), or more generally a permanent magnet synchronous machine (PMSM), much has been published discussing the optimized method that reduces the torque ripple and increase the efficiency of the BLDCM. In overview, there are vector based control and scalar based control. Compared with the scalar based control, the vector based control has a better performance on minimizing the torque ripple. Generally, the vector based control can be divided into the direct torque control (DTC)[9] and field oriented control (FOC)[10]. Both of them have relative better performance compared with the scalar based control such as six-step commutation method[11].

However, the referenced [12] compares DTC with FOC and shows that FOC has lower torque ripple and current distortion, even though it has slower dynamic response for torque. Besides, together with the space vector pulse width modulation (SVPWM), it also offers an advantage on the better using of the DC bus voltage, which enables a better speed-torque performance[13]. Therefore, FOC is chosen as the control strategy of the motor drive to be designed.

One more advantage of choosing FOC is that there are some commercial micro control unit (MCU) that has FOC algorithm embedded. For instance, InstaSPIN™ series from Texas Instrument embeds FOC algorithm into the micro-controllers. F28069M is one of the series, which is suitable for the application here. Thus, it is chosen as the MCU for the motor driver. In the chapter 3 where the

hardware design is discussed, the interface is designed based on the interface of the LAUNCHXL-F28069M which is a LaunchPad™ development platform using F28069M as the MCU.

2.2.1. Modelling of the BLDCM

In order to investigate the performance of the control strategy in the simulation, a mathematical model of the motor should be constructed. Thus, the modelling of the motor used for Nuna is set forth in this subsection.

Compared with the other type of motor, the permanent magnet synchronous machine has a lot advantages in the application here. For instance, it has the most efficient drive because of its low loss [14]. Generally, PMSM is divided into two types. The first one is BLDCM which is said to have a trapezoidal back emf. The other one is BLACM whose back emf is sinusoidal. However, in reality both of the ideal cases can hardly be achieved [14].

The motor used on Nuna 9 (the solar racer) is a Mitsuba Y-connection BLDCM, or more accurately, a surface mounted permanent magnet (SPM) motor with 18 pole pairs as shown in the Figure 2.4. For such a SPM motor, the saliency of the rotor can almost be neglected and the inductance on the d-axis (L_d) is almost equivalent to the L_q. Besides, the back EMF of it has a waveform closer to sinusoidal waveform instead of trapezoidal waveform.

(a) Stator

(b) Rotor

Figure 2.4: The motor of the Nuna 9

Based on the mentioned above, the assumptions below are made to simplify the motor model:

1. The rotor material has such high resistance that the current induced in the rotor can be ignored.
2. $L_d = L_q$ and they are constant.
3. The waveform of the back EMF is sinusoidal.

The simplified electrical circuit of such a BLDCM is shown in the figure 2.5. Based on such a circuit model and the assumptions listed above, the mathematical model of the BLDCM [15] is set forth as the equation (2.2,2.3 and 2.1) where:

- R_s: stator winding resistance
- L_s: self inductance of the stator winding
- M: mutual inductance between the different stator winding
- $R_a = R_b = R_c = R_s$
- $L_a = L_b = L_c = L_s - M$
- U_a, U_b and U_c: terminal voltage of the motor
- i_a, i_b and i_c: phase current
- e_a, e_b and e_c: back EMF of each phase respectively
- K_e: back EMF coefficient
- $\lambda_{ra}, \lambda_{rb}$ and λ_{rc}: flux linkage between rotor magnets and stator winding

- T_e: electrical torque
- ω_m: rotor rotating speed
- ω_e: electrical angular speed of the rotor

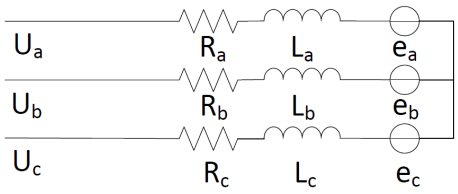


Figure 2.5: The electrical circuit of a BLDC motor

$$e_i(t) = \frac{d}{dt}\lambda_{ri}(\theta) = K_e\omega_m sin(\omega_e t + \phi_i) \quad (i = a, b, c) \tag{2.1}$$

$$\begin{bmatrix} U_a(t) \\ U_b(t) \\ U_c(t) \end{bmatrix} = \begin{bmatrix} R_s & 0 & 0 \\ 0 & R_s & 0 \\ 0 & 0 & R_s \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} L_s - M & 0 & 0 \\ 0 & L_s - M & 0 \\ 0 & 0 & L_s - M \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} + \begin{bmatrix} e_a(t) \\ e_b(t) \\ e_c(t) \end{bmatrix} \tag{2.2}$$

$$T_e(t) = \frac{e_a(t)i_a(t) + e_b(t)i_b(t) + e_c(t)i_c(t)}{\omega_m} \tag{2.3}$$

As we can see for the model of the BLDCM, some important parameters, such as K_e, R_s, L_s and M, are necessary to specify the characteristics of the motor. In order to get an accurate simulation result which is not far away from the real performance, measurements are necessary. However, because of some inconveniences, the measurements are not available. Therefore, a rough estimation based on the recorded competition data is done to approximate these specifications. However, some of the specifications are not possible to be estimated with the given information. In order too complete the simulation, the assumption is used. The resultant specifications of the BLDCM are listed in the table 2.4.

Table 2.4: Specifications of the BLDCM

	Value	Method
R_s	$100m\Omega$	measurement
L_s	$200\mu H$	measurement
M	0	assumption
K_e	0.53	estimation

2.2.2. Modelling of the mechanical load

Except the motor model, the mechanical load model is also needed for the mechanical dynamic performance of the racer. However, as this part of simulation is just used to roughly check whether the extremely high current occurring in the recorded data is necessary or not, a simplified mechanical load model is enough. For a running racer, the driving force is the output force of the motor and the other forces applied on the car consists of the air drag, friction force and gravity force.

In the figure 2.6, the force analysis of the car is depicted, where N is braced force from the ground, F_w is the air drag, F_f is friction force, F_c is the component of gravity force G paralleling the ground and F_{motor} is the output force of the motor. Among all the drags, the air drag and ground friction are the two main force resistance on the car. Formula 2.4[16] set forth the calculation of the air drag where C_d is drag coefficient determined by the shape of the car, ρ is the density of the air and A is the surface area affected. To simplify the calculation, the air density is assumed to be a constant. Thus, the coefficient K_w is used to replace the constant $\frac{1}{2}C_dA\rho$ and the estimation of it is based on the recorded

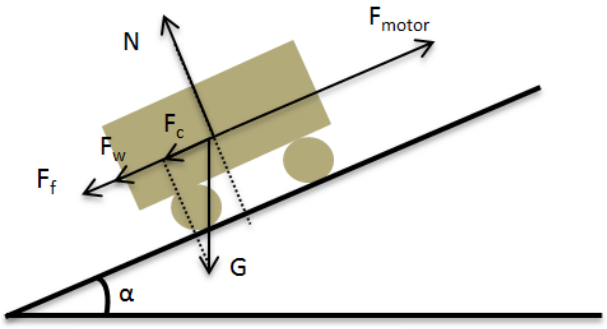


Figure 2.6: Force analysis of the running racer

competition data. As for the ground friction, the formula 2.5 is used to calculate its value, in which μ_r is the coulomb friction coefficient and an empirical value (0.012) [17] is used.

$$F_w = \frac{1}{2} C_d A \rho (v_{vehicle} + v_{wind})^2 = K_w (v_{vehicle} + v_{wind})^2 \tag{2.4}$$

$$F_f = \mu_r mgcos(\alpha) \tag{2.5}$$

As for the F_{motor} and the climbing force F_c, the equation 2.6 and equation 2.7 are used as the model, where R_w is the radius of the wheel, m is the mass of the car. Besides, as the landscape of the competition terrain in the WSC 2017 is quite flat. Thus, the slope angle α is assumed to be zero. In the table 2.5, the specifications used for the mechanical load model is summarized.

$$F_{motor} = \frac{T_e}{R_w} \tag{2.6}$$

$$F_c = mgsin(\alpha) \tag{2.7}$$

Table 2.5: Specifications for the mechanical load modelling

K_w	μ_r	Gravity acceleration g (m/s^2)	m (kg) (driver included)	R_w (mm)	α (°)
0.015	0.012	9.81	220.5	279.2	0

2.2.3. Field Oriented Control (FOC)

The principles of FOC has been introduced in many literature. Basically, it transform the current vector in the a-b-c frame into the d-q-0 frame. In this way, the current vector is split into two orthogonal components (I_d and I_q). The two components are used to control the magnetic field and the torque respectively.

Based on the principles of FOC, a system model is built in PLECS to investigate the mechanical dynamic performance of this control strategy. The block diagram of the model is shown in the figure 2.7.

In this model, the voltage source inverter (VSI) is idealized, which means the rise and fall time of the current through the transistors is zero and their conduction resistances are also neglected.

Another important thing to be mentioned is the structure of the dq PI controller used for the current regulation. Because a VSI is used, the SVPWM is used to directly control the output voltage of the VSI. The current is controlled indirectly by controlling the voltage applied on the motor. The relation between the phase current and the terminal voltage is given in the equation 2.8 and equation 2.9. The two equations are the voltage equation of BLDCM in dq frame transformed from the BLDCM model in the subsection 2.2.1. As we can see, decoupling of the d and q current component, which makes the

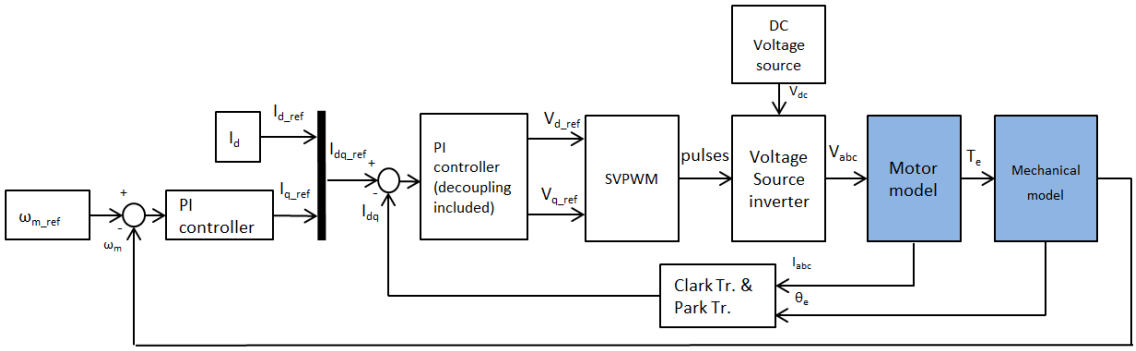


Figure 2.7: Block diagram of FOC

current regulation independent of the rotating speed of the rotor, is necessary to regulate the current by means of voltage manipulation.

$$V_q = R_s i_q + L_q \frac{di_q}{dt} + \omega_e L_d i_d + \omega_e \lambda_m \tag{2.8}$$

$$V_d = R_s i_d + L_d \frac{di_d}{dt} - \omega_e L_q i_q \tag{2.9}$$

In the referenced [18], two different decoupling methods are proposed and compared. Although the proposed methods in [18] are used for the induction machine, they are also applied to the BLDCM. To start with, the figure 2.8 shows the BLDCM model in the rotor frame. Built on this motor model, the block diagrams of the two methods are shown in the figure 2.9a and the figure 2.9b. As we can see, in order to achieve an accurate control, the inductance value and the flux linkage λ_m produced by the rotor magnet are necessary, whereas both of them are not needed in the second method. Therefore, the latter method is preferable.

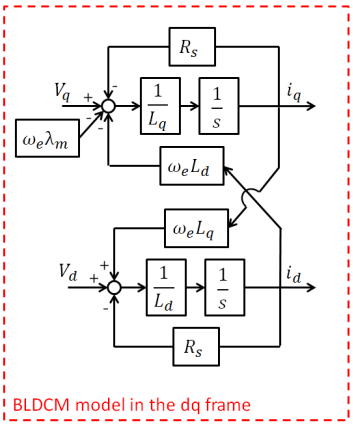
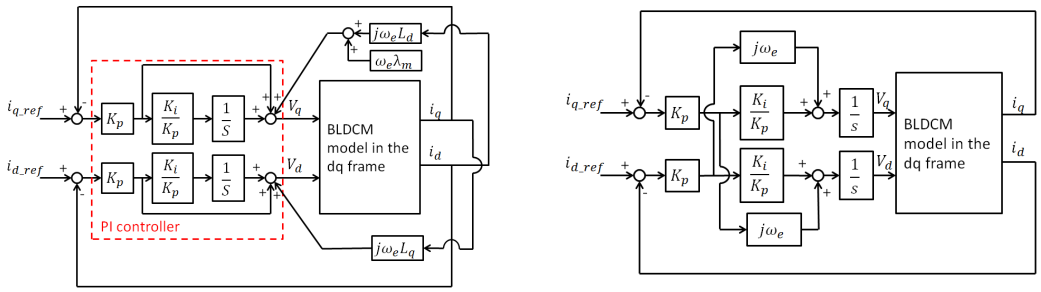


Figure 2.8: BLDCM model in the dq frame

Despite the very obvious advantages of FOC, a tricky thing when using it is the information of the rotor position is necessary. Normally, position encoder is needed to get the rotor position for FOC. However, there are also some sensorless methods [19, 20]. Basically, the sensorless methods make use of a mathematical back EMF observer to estimate the rotor position. This kind of way is effective and accurate when the speed of the rotor is high enough. However, at low speed, it has severe problem because the amplitude of the back EMF is low when the rotating speed is low and the estimation possibly has big error. A general solution for this problem is using a fixed start procedure. For instance, using



(a) Method 1 **(b)** Method 2

Figure 2.9: The method of decoupling the d and q current component

normal six-step commutation method firstly and change to sensorless FOC as long as the speed of the rotor and the amplitude of the back EMF are high enough.

2.2.4. Modulation method

Normally, the field-oriented control is based on SVPWM because of their inherent connection. The current regulator outputs the reference V_d and V_q. After transforming the voltage in the d-q-0 frame to the stator $\alpha - \beta - 0$ frame, the SVPWM modulation can be used to control the voltage follow the reference voltage.

In order to reduce the harmonics, a typical symmetrical 7-segment SVPWM [21] is used. For instance, the switching sequence in the sector iis shown in the figure 2.10

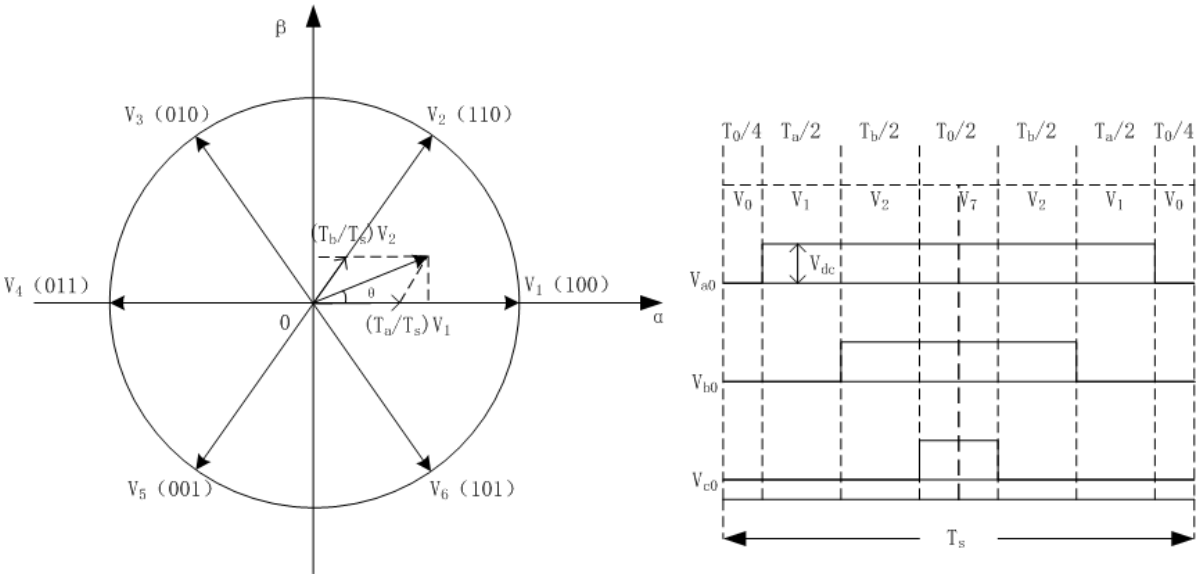


Figure 2.10: The switching sequence of the symmetrical 7-segment SVPWM

As for the switching frequency, a typical value 20kHz that is used for some of commercial motor drives is chosen in the control system modelling. However, in the power loss modelling of the inverter, different switching frequency is selected to compare the influence of the switching frequency on the power loss.

2.3. Motor drive loss modelling

2.3.1. MOSFET loss modelling

As mentioned previously, the power losses of a motor drive is mainly from the power loss of the transistors. With a specified control strategy, the inverter loss model can be implemented after the

modelling of the MOSFET loss.

In overview, the power losses of the MOSFET consist of the conduction loss, switching loss and the loss on the parasitic diode of the MOSFET. The modelling of the conduction loss and the switching loss are discussed respectively.

- Conduction loss modeling:

  Basically, the conduction loss is the Joule loss so it is determined by the current i_{on} flowing through the MOSFET and the on-resistance $R_{ds(on)}$ of the it. Given that the $R_{ds(on)}$ is influenced by both the junction temperature (T_j) and the i_{on}, the conduction loss model is

$$P_{cond} = R_{ds(on)}(i_{on}, T_j) \cdot i_{on}(t)^2 = V_{on}(i_{on}, T_j) i_{on}(t) \tag{2.10}$$

  The value of the voltage drop on the MOSFET during the switch-on status (V_{on}), it varies in terms of the different i_{on} and T_j because of the change of $R_{ds(on)}$. Its value can be found in the datasheet [4–8]. According to the datasheet, a 2-D look-up table of $V_{on}(i_{on}, T_j)$ is implemented in MATLAB and is used for the conduction loss prediction. In the appendix B, the 2-D look-up tables of every kind of MOSFET are shown. Accordingly, it is obvious that under the high i_{on} condition, the conduction loss rises up a lot if the T_j rises up. In the meanwhile, because of the increasing of the power loss, the junction temperature would rise up more. This process proceeds iteratively and might make the MOSFET fail on the junction temperature if it does not converge to certain junction temperature. Such a phenomenon is called thermal runaway. However, for the SiC MOSFETs the thermal runaway problem is relatively less severe than the other two. The GaN MOSFET has the worst thermal runaway problem.

- Switching loss modeling:

  Due to the superposition of I_{ds} and V_{ds} during the switch-on and switch-off interval, there are switching energy losses (E_{on} and E_{off}). Because the energy loss happens in every switching cycle, the switching loss model is

$$P_{sw} = f_s[E_{on}(i_{on}, v_{block}, T_j) + E_{off}(i_{on}, v_{block}, T_j)] \tag{2.11}$$

  ,where v_{block} is the block voltage before or after switching, i_{on} is the conduction current before or after switching and T_j is the junction temperature.

  The power losses of the body diode are neglected because of two reasons. The first one is, the conduction time of the diode is rather short so the conduction loss of the body diode is too small to be counted. The second is the GaN the SiC MOSFET has very small reverse-recovery charge so the reverse-recovery loss of the diode can be ignored. As for the Si MOSFET, though it has significant reverse-recovery loss, the loss is also neglected because the Si MOSFET is only used for the comparison and its switching losses do not have to be calculated precisely.

  Compared with the $R_{ds(on)}$, the accurate estimation of the E_{on} and E_{off} is more difficult. Although in the datasheet the manufacturer offers the measurement data of the E_{on} and E_{off}, the datasheet data is sometimes not sufficient because the measurement is done under a different test condition from the user case. Therefore, in order to get accurate data, measurement is necessary.

  However, the hardware test increases both time and money cost. An alternative way is using SPICE models, which are offered by the manufacturers, to simulate the switching transient and do the virtual measurement. A typical test for the MOSFET is the so called double pulse test (DPT), which is shown in the figure 2.11 where a DPT circuit for the MOSFET GS66516B is shown. The SPICE model of the MOSFET includes the body diode. Hereby, in this test circuit, the additional switch-on energy loss produced by the reverse-recovery charge of the diode is also included. An ideal current source is used to approximate a load with big inductance (motor).

  In the test circuit, all the parasitic inductance of the PCB trace are neglected. The gate driving voltage and gate resistor are selected based on the recommendation from the manufacturers. However, for convenience, among the five transistor candidates, such a switching loss measurement is only done for GS66516B, SCT3022AL and IPT60R028G7. For the other two SiC MOSFET,

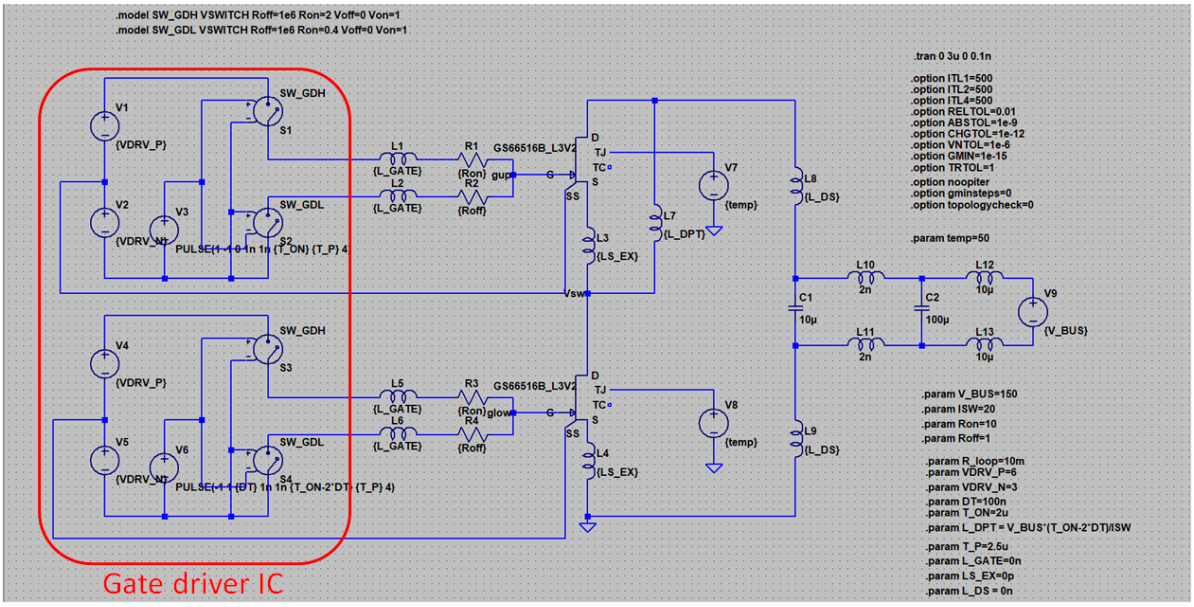


Figure 2.11: DPT circuit with GS66516B

the switching loss is estimated by the datasheet value assuming the switching loss is linearly related to the v_{block} and junction temperature. In the table 2.6, the conditions under which the switching loss is simulated are listed. Based on this estimation method, the $E_{on}(i_{on}, v_{block}, T_j)$ and $E_{off}(i_{on}, v_{block}, T_j)$ are simulated. The resultant 3-D look-up tables of E_{on} and E_{off} are shown in the appendix B.

Table 2.6: Conditions for the switching loss estimation

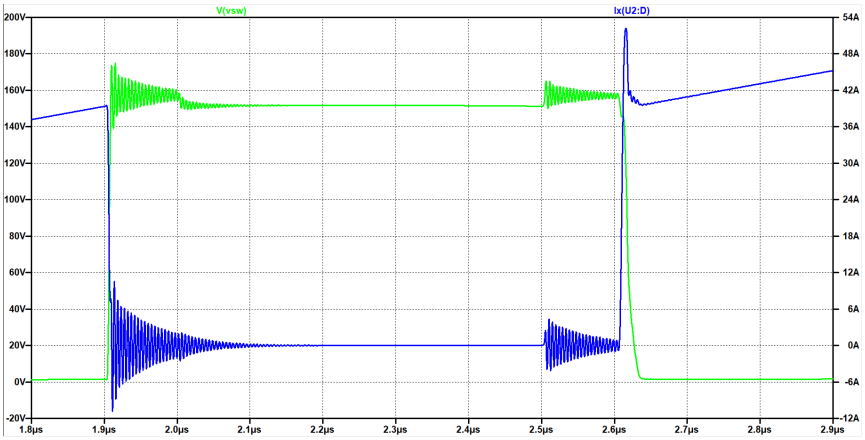
Part No.	Method	$R_{on}/R_{off}(\Omega)$	$V_g(V)$ (sink/source)
IPT60R028G7 (CoolMOS™)	SPICE simulation	10/1	0/18
SCT3022AL(SiC)	SPICE simulation	10/1	0/18
GS66516B(GaN)	SPICE simulation	10/1	-3/6
C2M0025120D(SiC)	datasheet	6.8	-5/20
SCTWA50N120(SiC)	datasheet	2.2	-5/20

As mentioned previously, the GaN and SiC MOSFET have small and even zero reverse-recovery charge (Q_{rr}). But, the Si MOSFET has high reverse-recovery charge stored in the body diode. From the datasheet of the CoolMOS™ IPT60R028G7, it can been found that its switching speed is actually even faster than some SiC MOSFET. In the table 2.7, one of the SiC MOSFETs is chosen and compared with the CoolMOS™ and the GaN MOSFET from the perspectives of the switching speed and the reverse-recovery charge. All the data is from the datasheet [4, 5, 8] where the detailed test condition can be found.

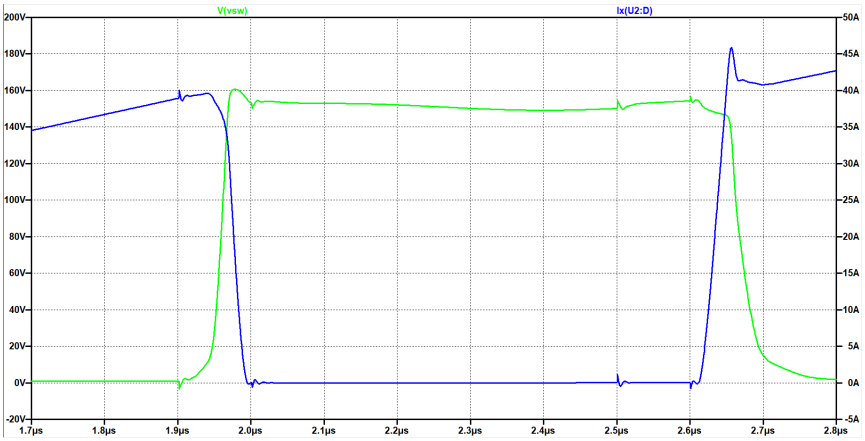
Table 2.7: Comparison between the Si, SiC and GaN on the switching speed and Q_{rr}

Part No.	Test concidtion		Current rise time $t_r(ns)$	Current fall time $t_f(ns)$	$Q_{rr}(nC)$
	$V_{block}(V)$	$I_D(A)$			
IPT60R028G7 (CoolMOS™)	400	58.3	27	5	20000
SCT3022AL(SiC)	300	18	53	35	146
GS66516B(GaN)	400	16	12.4	22	0

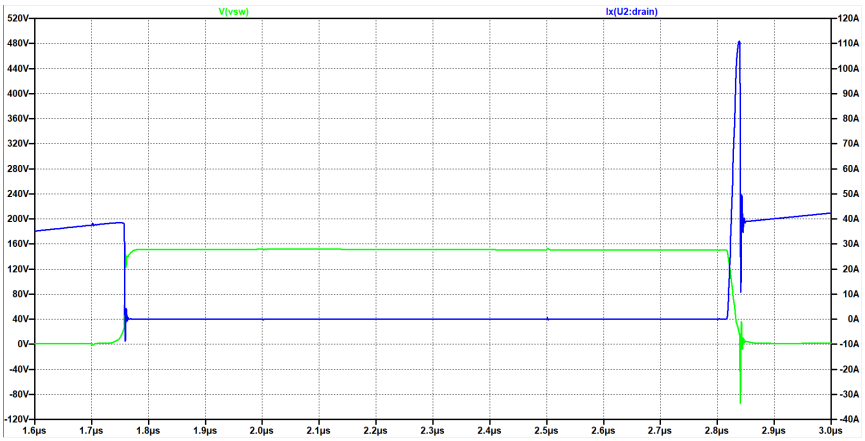
In order to further show how bad impact that the Q_{rr} has on the switching on loss, the switching transient of the three transistors under same v_{block} (150V), i_{on} (40A) and T_j (50°C) is shown in the figure 2.12. In the switching on process, there is an obvious overshoot in the current waveform of the CoolMOS™ where as such an overshoot does not occur in the the current waveform of the GaN and SiC MOSFET. The simulations are done under the same condition that $V_{block} = 150V$, $I_{on} = 40A$ and $T_j = 50°C$.



(a) GaN



(b) SiC



(c) CoolMOS™

Figure 2.12: Waveforms of the voltage V_{ds} (green) and the current I_{ds} (blue) during the simulated switching transient with SPICE model

2.3.2. Detailed inverter loss model

Basically, the inverter loss is the sum of the power losses of all the MOSFETs. Until now, the power loss of a single MOSFET has been modelled. In order to calculate the power loss of every single MOSFET when the motor drive is operating, it is necessary to know the current i_{on} through the MOSFET, the DC bus voltage u_{dc} (equals the block voltage v_{block}), the switching frequency f_s and the junction temperature T_j of the MOSFET. In figure 2.13, all the inputs that will influence the inverter loss are shown. The PWM pulse pattern together with the phase current i_{phase} determines the current i_{on}.

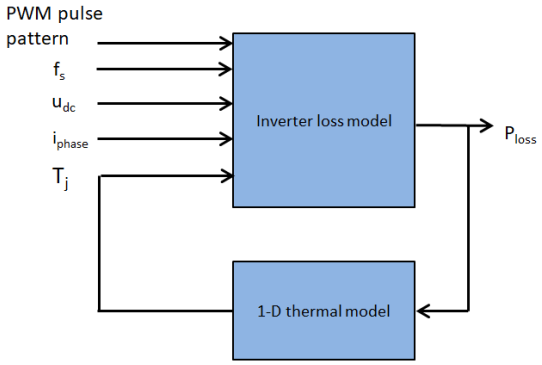


Figure 2.13: The inputs and outputs of the inverter loss model

In order to analyze the switching behaviour of the MOSFETs, a motor drive with the six MOSFETs is used for simplicity. A switching cycle is illustrated in the figure 2.14. The process starts with the upper MOSFET is on while the lower one is off in the figure 2.14a. Next, because of the dead time, the phase current firstly flow through the body diode. Thereby, the block voltage of the lower MOSFET is zero at the switch-on instant. Same process happens during the switch-off of the lower MOSFET.

Therefore, only the upper MOSFET has the switching losses in this switching cycle. When the current is in the opposite direction, only the lower MOSFET has the the switching losses.

Based on the elaboration, if the switching period is T_s and the period of the fundamental wave of the phase current is T_0, the inverter loss model is

$$P_{loss} = N\frac{1}{T_o}\left(\int_0^{T_o}\sum_{i=a,b,c}\left(P_{cond,up,i}(t) + P_{cond,low,i}(t)\right)dt + \sum_{j=1}^{m}\sum_{i=a,b,c}P_{sw,i}(jT_s)T_s\right) \tag{2.12}$$

where N is the number of the paralleling MOSFETs and $m = \frac{T_0}{T_s}$.

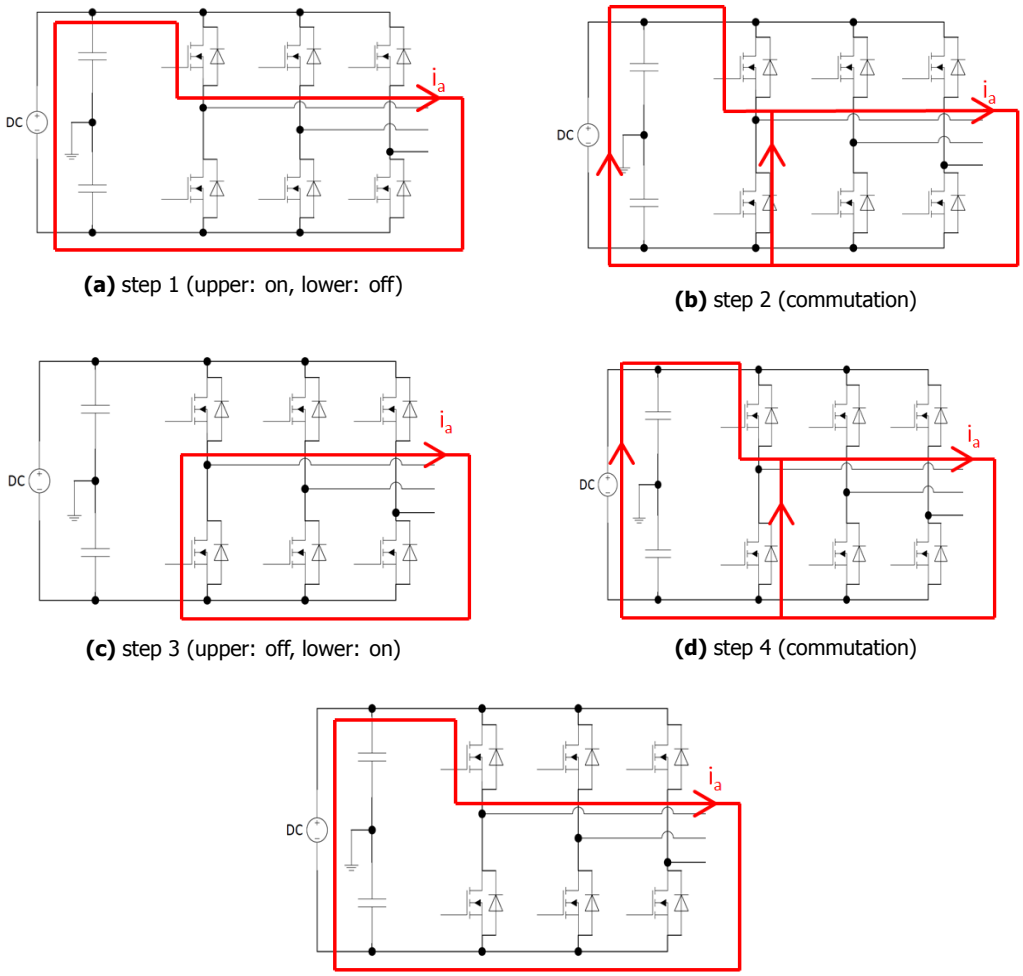
The purpose of modelling the inverter loss is evaluating the efficiency of the motor drive as well as the junction temperature of the MOSFETs during the competition. Therefore, the load profile which has been introduced in the subsection 2.1.2 will be used for the efficiency and junction temperature evaluation.

Apparently, the inverter loss model introduced above need small time steps because of the PWM pulse pattern and the time-dependent T_j. For the efficiency evaluation, a long term (one day) load profile is used to acquire accurate results. Thus, simplification is necessary to decrease the time cost on the simulation. However, for the junction temperature evaluation, the small time step is necessary.

2.3.3. Simplified inverter loss model

The inverter loss model established for the junction temperature can be simplified by removing the need on the PWM pulse pattern. Several assumptions are made to achieve the goal.

- The performance of the current controller is very nice so that the phase current is exactly same as the reference value.
- In one period of the fundamental wave (T_0), the upper MOSFET has the symmetrical behaviour with the lower MOSFET. Therefore, the conduction loss of the two MOSFETs in the same phase leg can be assumed to be same with each other.



(a) step 1 (upper: on, lower: off)

(b) step 2 (commutation)

(c) step 3 (upper: off, lower: on)

(d) step 4 (commutation)

(e) step 5 (upper: on, lower: off)

Figure 2.14: Switching behaviour of the two MOSFETs in one leg in one switching cycle

- The switching period is so short that the current in the period can be assumed to be constant. Thus, the switching loss can be calculated by assuming $i_{on}(t) = i_{phase}(nT_s)$ where n is integral between 1 and T_0/T_s.

Built on the first two assumptions, the instant conduction loss of the MOSFET in one leg can be approximated with

$$P_{cond,up} = P_{cond,low} = \frac{1}{2} R_{ds,on}(i_{phase}, T_{j,average}) \cdot i_{phase}(t)^2, \tag{2.13}$$

where

$$T_{j,average} = \frac{T_{j,up} + T_{j,low}}{2}.$$

Here, the average junction temperature of the upper and lower MOSFET is used. This will not induce big error because the two MOSFETs have symmetrical switching behaviour in one fundamental period.

This junction temperature assumption also used for the switching losses calculation. Thus, with the third assumption, the switching loss can calculated.

With the method introduced above, the need on the PWM pulse pattern is removed. However, the small time step still exists because of the time-dependent T_j. As mentioned previously, for the junction temperature evaluation, it is necessary and it is impossible to remove the small time step. However, for the efficiency evaluation which is based on a time scale of one day, the small time step can be

removed. This results from the racer keeps a very stable cruising status which results in the very stable junction temperature of the MOSFET. Assuming the junction temperature of all the MOSFET are always equal to the temperature $T_{j,cruising}$ at the cruising speed does not bring too big error for the efficiency evaluation but reduce much of the simulation time.

Built on the assumption and a selected switching frequency, a 3-D look-up table for the $P_{loss}(\hat{I_{phase}}, u_{dc}, T_j)$ is established to remove the small time step. This approach is illustrated in the figure 2.15.

Obviously, the only missing input is the switching frequency. Although the switching frequency is crucial for the design of a motor drive, it is not the main concern in this project. For this reason, only two switching frequencies (20kHz and 50kHz) are used and compared. As mentioned previously, 20kHz is use in the control system modelling because it is a very high switching in the motor drive application. As for the 50kHz, it is selected because it is terribly high for such an application and the performance of the GaN and SiC MOSFET switched with such a high frequency is of interest. By comparing the two frequencies, it is of concern what kind of advantages that the GaN and SiC MOSFET has.

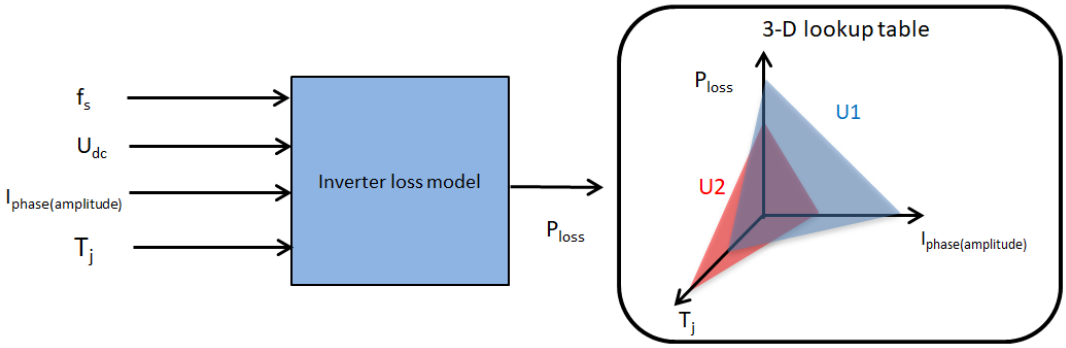


Figure 2.15: The approach for constructing the 3-D look-up table used for the efficiency evaluation

2.4. 1-D thermal modelling

2.4.1. Fundamentals of 1-D thermal modelling

The 1-D thermal model is a kind of thermal circuit in which the thermal parameters is analogized as the electrical parameter. For instance, the power source in thermal circuit is equivalent with a current source in a electrical circuit.

In the 1-D thermal model, the heat transfer in horizontal direction is neglected and only the vertical heat transfer is considered. Besides, the convection and radiation is neglected for the heat transfer in solid. Thus, the thermal model degrades into one dimensional. The drawback of such a thermal modeling, such as it fails in simulating the thermal behaviour in the time order shorter than the thermal constant of the die is discussed in [22].

However, because of the simplicity of the 1-D thermal model, it is widely used. Two different thermal circuit models, the Cauer-model and Foster-model, are introduced in the [23]. The first one has physical relation with the layers in the semiconductor device where as the second one is just an equivalent mathematical model. For the thermal modelling of the layers inside the MOSFET, both models are suitable, because the the manufacturers of the thermal parameters of the semiconductor devices. These parameters result from either the measurements [23] or the detailed thermal analysis with finite difference method (FDM) or finite element method (FEM) [24].

Nevertheless, the manufacturers cannot give the thermal parameters of the layers outside the semiconductor devices. For instance, the thermal resistance and capacitance of the heatsink need to be estimated according to the heatsink selected. Thus, the Cauer-model is selected because of its physical significance of every layers, which makes the thermal modelling easier.

In the figure 2.16, the thermal circuit used for the modelling is shown. The internal thermal resistances as a whole is called junction-to-case thermal resistance ($R_{\theta jc}$). For the external thermal resistances, the case-to-heatsink thermal resistance $R_{\theta cs}$, the heatsink-to-air thermal resistance $R_{\theta sa}$ and the thermal capacitance (the case thermal capacitance $C_{\theta c}$ and the thermal capacitance of the

heatsink $C_{\theta s}$), they vary in terms of the different users' cases. For instance, $R_{\theta cs}$ is influenced by the thermal interface material (TIM) and the air gap between the TIM and the case and the heatsink. For a good thermal performance, the thickness of the air gap should be as small as possible because of the bad thermal conductivity of the air.

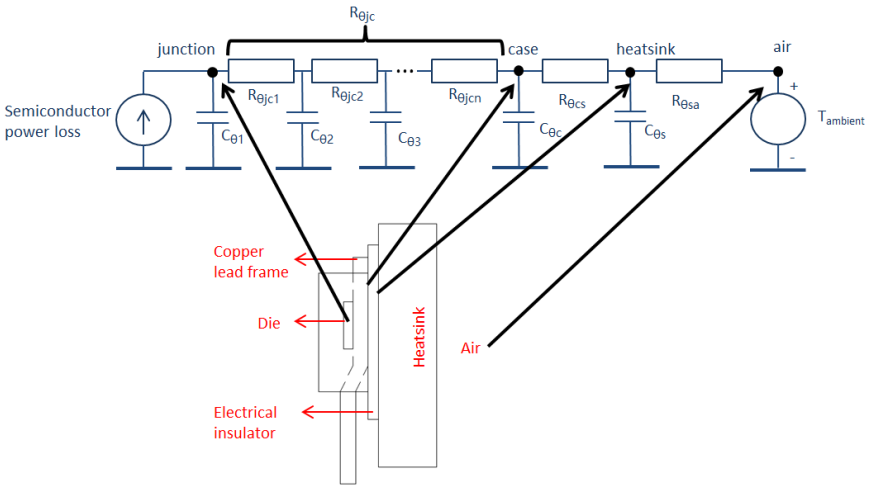


Figure 2.16: Thermal circuit of the 1-D thermal modeling

An analytic estimation method of the thermal resistance is given in the equation 2.14 [25].

$$R_\theta = \frac{x}{Ak} \tag{2.14}$$

where:

- R_θ: the thermal resistance of the material (K/W)
- x: the length of the material (m)
- A: the cross area of the material (m^2)
- k: the thermal conductivity of the material $(W/(K \cdot m))$

The formula for the thermal capacitance $C_\theta(J/K)$ (also called as thermal mass) calculation is given in 2.15[26], in which the $m(kg)$ is the mass of the object and the $c_p(J/kg \cdot K)$ is the specific heat capacity of the material of the object.

$$C_\theta = mc_p \tag{2.15}$$

2.4.2. Thermal parameters in the modelling

In the table 2.8 and the table 2.9, the specific parameters used in the thermal circuit of different transistor candidates are shown. For the internal thermal parameters, some of the manufacturers offer the thermal resistances of the different layers inside the case and the case itself but the others give only an overall junction-to-case thermal resistance. As for the internal thermal capacitance, if it is not given by the manufacturer, it is assumed its internal material consists of only silicon and estimated by formula 2.15. Such a simplification of assuming the internal layers of the transistor are uniform and have the same temperature would result in big error if the current through the transistor is large surge current with short duration time. Nevertheless, because of the lack of information, the model has to be made to roughly approximate the real behaviour. A effective way to ensure such an simplification do not have impact on the feasibility of the design is leaving a safe margin between the simulated peak junction temperature to $150°C$.

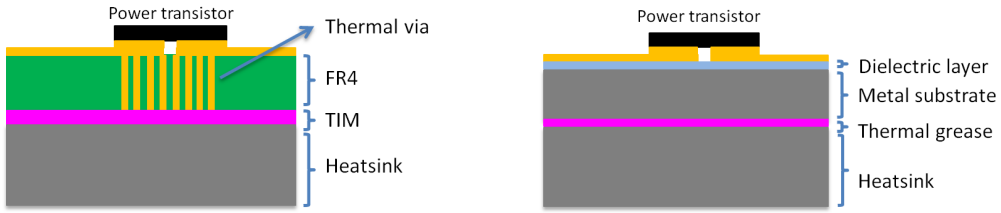
For the external thermal parameters reasonable assumptions are necessary to estimate their value. To start with, the thermal capacitance of the thermal interface material (TIM) $C_{\theta c}$ is estimated by using the formula 2.15 assuming the TIM is the GAP3000S30R from Bergquist™ [27]. For fair comparison,

Table 2.8: Specifications for the thermal circuit of different transistor candidates: Internal thermal parameters

	Thermal resistance (K/W)					Thermal capacitance (J/K)				
	$R_{\theta jc1}$	$R_{\theta jc2}$	$R_{\theta jc3}$	$R_{\theta jc4}$	$R_{\theta jc5}$	$C_{\theta 1}$	$C_{\theta 2}$	$C_{\theta 3}$	$C_{\theta 4}$	$C_{\theta 5}$
GS66516B	6E-3	125E-3	126E-3	13E-3	-	9.03E-5	6.29E-3	1.41E-3	2.14E-3	-
SCT3022AL	4.825E-3	172.5E-3	163.2E-3	-	-	1.403E-3	11.3E-3	60.17E-3	-	-
C2M0025120D	240E-3	-	-	-	-	200E-3	-	-	-	-
SCTWA50N120	10.8E-3	40.5E-3	133E-3	148.5E-3	216E-3	1.1E-3	3.1E-3	14E-3	44.4E-3	296E-3
IPT60R028G7	320E-3	-	-	-	-	200E-3	-	-	-	-

the TIM used for all candidates is assumed to be of same mass therefore same thermal capacitance $(1J/K)$.

The thermal resistance $R_{\theta cs}$ is influenced by the mounting technique, the package size and the characteristics of the TIM. In the reference [28], it gives the empirical value of $R_{\theta cs}$ of some typical packages in which the package TO-247 is included. For the surface mounted device (SMD), it is more complicated because its different mounting method. The case is not directly placed on the heatsink but through the thermal via on the PCB. Because of the bad cooling performance of the conventional design with thermal via. There is also one new PCB technology called insulated metal substrate (IMS) board which changed the structure of the conventional FR4 PCB to achieve better cooling. In the figure 2.17, the vertical structures of the two kinds of PCB are shown. A comparison on the thermal resistance between the FR4 with thermal via and the IMS board is shown in [29]. Because of the good cooling of the IMS board, it is chosen for the SMD to improve their cooling performance. Thus, the $R_{\theta cs}$ for the two SMDs, which two have similar size with each other, is estimated by using the same value given in [29].



(a) FR4 with thermal via

(b) IMS

Figure 2.17: Vertical structure of the PCB together with the cooling system

Table 2.9: Specifications for the thermal circuit of different transistor candidates: External thermal parameters

	Package	$R_{\theta cs}(K/W)$	$C_{\theta c}(J/K)$	$R_{\theta sa}(K/W)$	$C_{\theta s}(J/K)$
GS66516B	SMD	0.8			
SCT3022AL	TO-247	0.3			
C2M0025120D	TO-247	0.3	1	0.6	405.42
SCTWA50N120	TO-247	0.3			
IPT60R028G7	SMD	0.8			

As for the thermal resistance and capacitance of the heatsink, the first one can be known from the datasheet as long as the heatsink is selected. The latter one can be calculated if the mass of the heatsink is known.

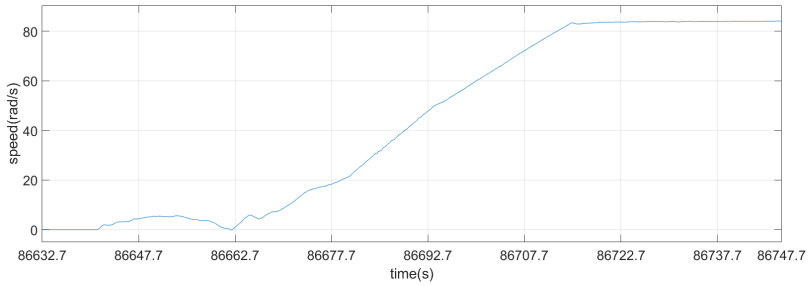
Here, the selection of a heatsink does not need to be optimized because the goal of interests is comparing the performances between the different candidates. Therefore, a heatsink with low enough thermal resistance under natural cooling condition is enough. The size and weight of the heatsink is also taken into account to ensure the chosen heatsink has enough space for the mounting. By referencing the size of the motor drive used on the Nuna 9, the selection of the heatsink is much easier because of the criteria that the chosen heatsink should not be bigger and heavier than the one on the Nuna 9. Finally, the 510-3M from Wakefield-Vette is selected. In the datasheet [30], it shows its sink-to-air thermal resistance $R_{\theta sa}$ is 0.56 K/W, but in the simulation $R_{\theta sa} = 0.6K/W$ is assumed instead.

2.5. Evaluation on the performance of the motor drive

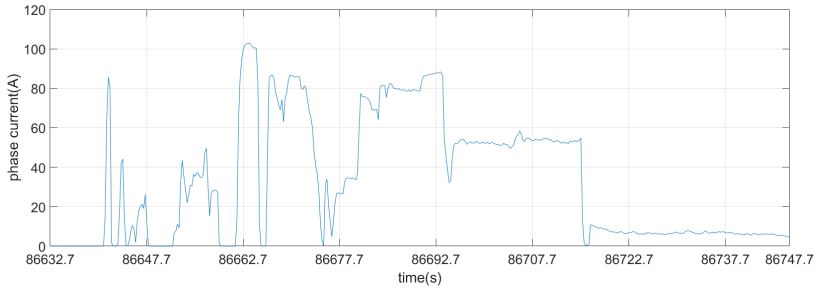
2.5.1. Evaluations on the control strategy

The evaluation is used for checking the feasibility of driving Nuna with a smaller current than the recorded current, especially during the start, overtaking, regenerative breaking and climbing.

After analyzing the given data from the team, it is found that most of the high current ($I_{phase(amplitude)} > 60$) occurs during the start when the racer is driven from $0km/h$ to about $90km/h$. Therefore, this situation is chosen for the evaluation. The real performance of the Nuna 9 in the 2017 WSC is compared with the simulation. A typical acceleration process of the Nuna 9 in the 2017 WSC is shown in the figure 2.18. Comparatively, the results of the simulation, in which the maximum phase current is set as 60A, are shown in the figure 2.19. In the comparison, the speed of the motor in rad/s is used instead of the speed of the car.



(a) Speed

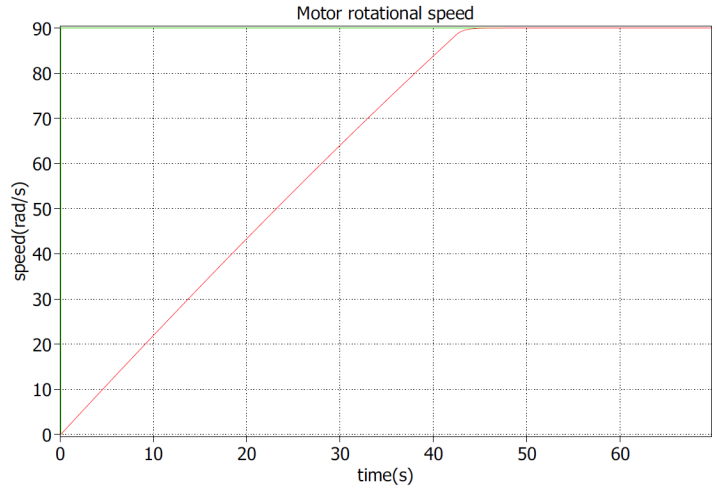


(b) Amplitude of the current

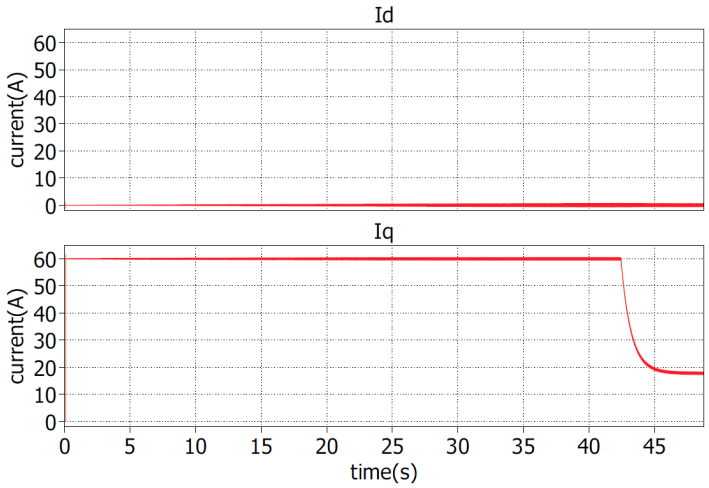
Figure 2.18: Speed and relative current during a typical acceleration process of the Nuna 9 in the 2017 WSC

The figure 2.18a shows the acceleration process of the Nuna 9 last nearly 60 seconds whereas the simulated acceleration process only takes nearly 45 seconds. Obviously, with a phase current whose maximum amplitude is 60A, the acceleration is high enough for the demand. And the high current is actually not necessary. However, for leaving the design a safe margin between the nominal operation and extreme condition, the motor drive is designed to withstand the extreme high current (120A). In this way, it also leaves some space for the team to adapt to the possible changes in the future.

Except the acceleration performance, the control strategy also achieves the desired current regulation. As shown in the figure 2.19b, the I_d is nearly zero while the I_q is the maximum during the acceleration. Although the maximum torque per ampere (MTPA) is not investigated, for such a SPM motor whose $L_d = L_q$, simply control $I_d = 0$ is enough to achieve a high power factor. Therefore, in the simulation I_d is always controlled to zero.



(a) Speed



(b) Waveform of I_d and I_q

Figure 2.19: Simulation results under the condition $I_d = 0$ and $I_{phase,max} = 60A$

2.5.2. Comparison on the conduction loss and switching loss between the GaN, SiC and Si MOSFET

Built on the modelling of the inverter loss, the conduction loss and switching loss of the inverter with the different V_{dc}, I_{phase}, f_s and T_j are evaluated. It is of interests to compare the performance of the GaN, SiC and Si MOSFET to figure out the advantages and disadvantages of the GaN and SiC MOSFET.

For simplicity, only one SiC MOSFET (SCT3022AL) is selected and compared with the GaN MOSFET and CoolMOS™. From the figure 2.20 to the figure 2.22, the conduction loss and switching loss of the motor drive with different kinds of MOSFET, switching frequency and inverter topology are compared. To decrease the complexity of the following explanation, several abbreviations used are listed below.

- 20kHz_d: $f_s = 20kHz$ and dual parallel MOSFET topology
- 20kHz_t: $f_s = 20kHz$ and triple parallel MOSFET topology
- 50kHz_d: $f_s = 50kHz$ and dual parallel MOSFET topology
- 50kHz_t: $f_s = 50kHz$ and triple parallel MOSFET topology

From the information included in the figure 2.20, 2.21 and 2.22, several conclusions can be drawn:

- From the sub-figure a and c in the three figures respectively, it can be found that the conduction loss is independent of the switching frequency and there is thermal runaway problem. However, the SiC MOSFET is the least sensitive to the temperature rising. Besides, adding one more parallel MOSFET can obviously decreases the conduction loss because the conduction resistance is reduced by paralleling MOSFETs.
- From the sub-figure b and d in the three figures respectively, it be observed that although one more parallel MOSFET for each phase is added, the switching loss is still reduced. This results from that the switching loss of the single MOSFET is reduced because of the decreasing of the conduction current of each MOSFET. However, as the gate drive loss is counted, this conclusion is only correct when the gate drive loss is negligible compared with the switching loss. When adding too much parallel MOSFET, the power loss must increase because of too much gate drive loss. Besides, the switching frequency rising from 20kHz to 50kHz brings more switching loss. However, this switching loss increase is much more obvious for the SiC MOSFET and Si MOSFET.
- By comparing the the sub-figure a and b, it can be found that the conduction loss is much higher than the switching loss especially under high current condition for all the three kinds of MOSFET.
- By comparing the three figures, it can be summarized that the GaN MOSFET has the least power loss in the low current condition because of its rather low switching loss. However, when the phase current is higher and higher, the advantage of the SiC MOSFET becomes more and more obvious because the conduction loss is dominant power loss and the SiC MOSFET has relative lower conduction loss.

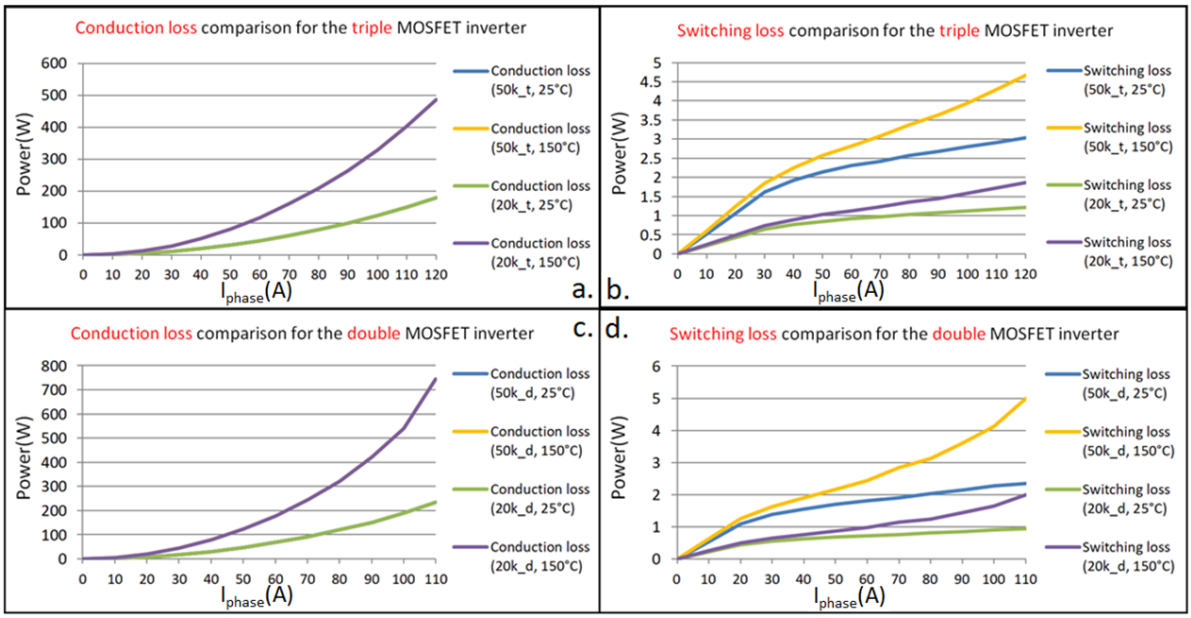


Figure 2.20: The conduction loss and switching loss of the GS66516B MOSFET motor drive with different switching frequency and topology

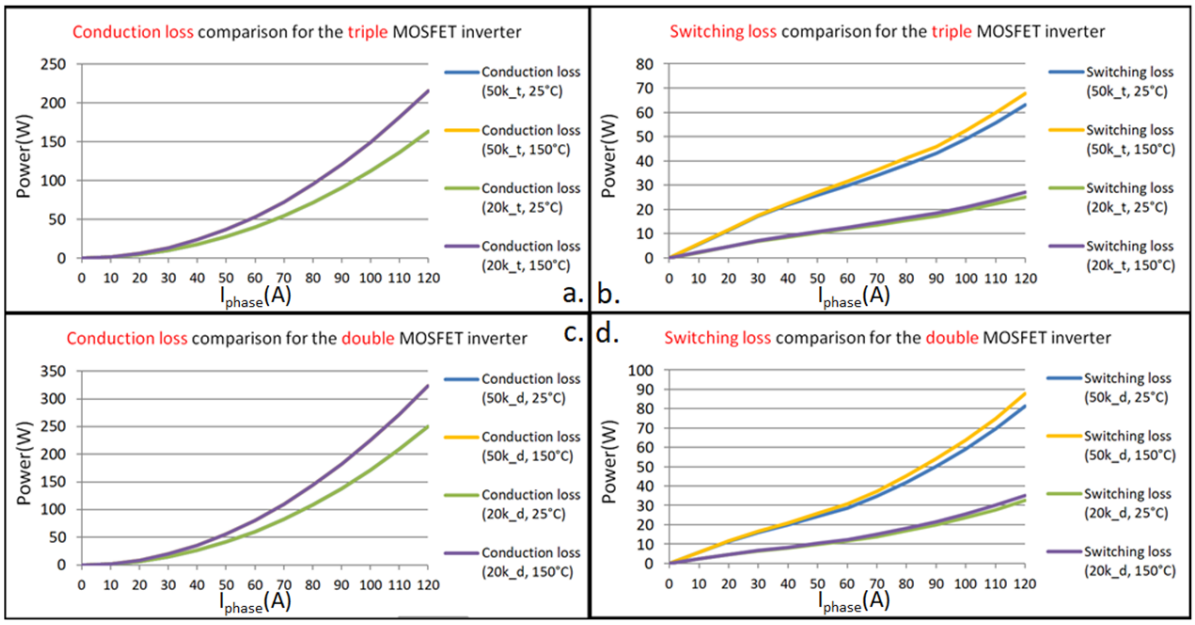


Figure 2.21: The conduction loss and switching loss of the SCT3022AL MOSFET motor drive with different switching frequency and topology

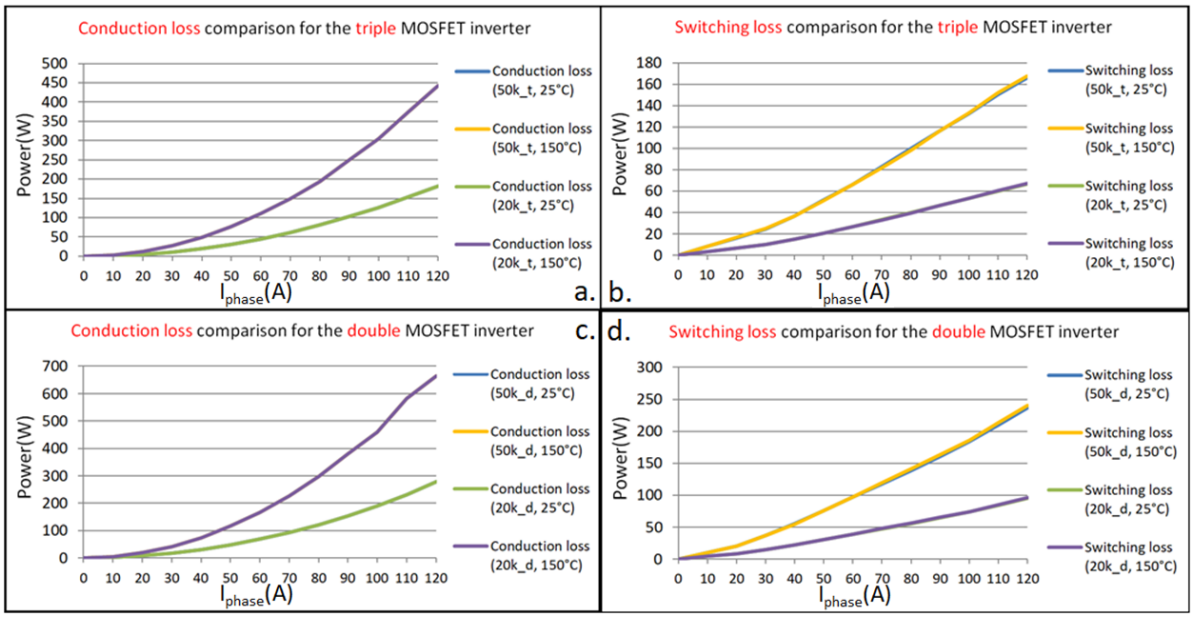


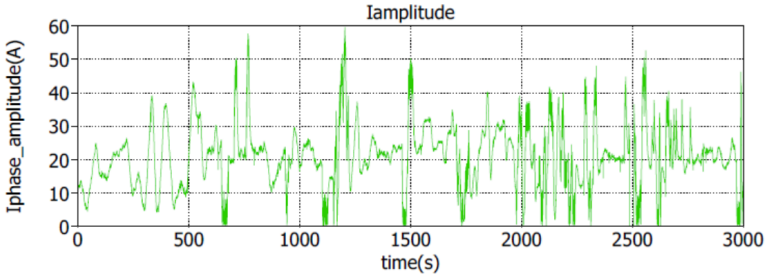
Figure 2.22: The conduction loss and switching loss of the IPT60R028G7 MOSFET motor drive with different switching frequency and topology

2.5.3. Thermal aspect evaluation

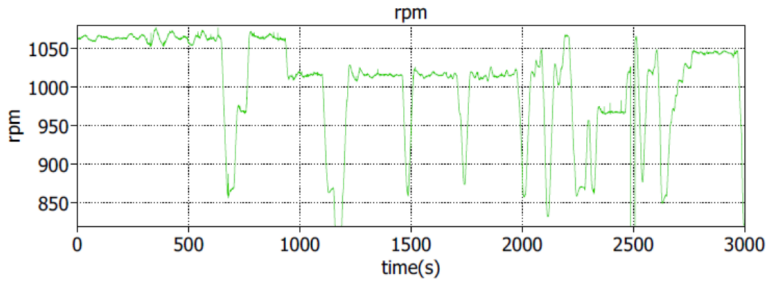
Basically, the thermal aspect evaluation consists of two parts. The first one is the evaluation on the junction temperature $T_{j,cruising}$ at the cruising speed. Assuming the $T_{j,cruising}$ is the initial temperature in the simulation for the maximum junction temperature $T_{j,max}$, the $T_{j,max}$ evaluation proceeds for the check on the feasibility of the design.

To start with, the evaluation on the $T_{j,cruising}$ is introduced. Because of the small time step in the model used for the junction temperature evaluation. The simulation period can not be too long. Hereby, a period of time, during which the speed is almost stable, with a scale of 3000 seconds is chosen for the $T_{j,cruising}$ simulation.

The 3000-second load profile is in the last day of the competition. In that day, the racer cruises at a relative higher speed, which means a higher phase current is used. In this way, a relative higher $T_{j,cruising}$ is gotten and it brings a relative higher $T_{j,max}$ and worse efficiency. The amplitude of the phase current with the corresponding speed information is depicted in the figure 2.23.



(a) $I_{phase}(amplitude)$



(b) speed

Figure 2.23: Load profile used for the $T_{j,cruising}$ simulation

As an example, the $T_{j,cruising}$ simulation of the 20kHz_d motor drive with C2M0025120D is plotted in the figure 2.24. Because of the low initial junction temperature assumed, it takes time to approach the average value. In the case shown in the figure 2.24 $T_{j,cruising}$ is estimated as $54°C$. The results of the $T_{j,cruising}$ simulation for all the candidates are shown in the table 2.10. A statistics plotting based on the data in the table 2.10 is shown in the figure 2.25.

Accordingly, all of the design candidates have a $T_{j,cruising}$ about $50°C$ to $60°C$. And the GaN MOSFET has the lowest $T_{j,cruising}$ because of its lowest power loss while the highest junction temperature is observed in the design 50k_d motor drive using IPT60R028G7. Besides, it can be seen from the statistics that the motor drive using a higher switching frequency has a higher $T_{j,cruising}$ and the motor drive with triple parallel MOSFET has a lower $T_{j,cruising}$ than the one with double parallel MOSFET. These two observations indicates that a lower switching frequency and more parallel MOSFET both help to decrease the power loss of the motor drive.

Table 2.10: $T_{j,cruising}$ simulation results of all the design candidates

	$T_{j,cruising}(°C)$			
	20kHz_d	20kHz_t	50kHz_d	50kHz_t
GS66516B (GaN)	50	46	51	46.8
SCT3022AL (SiC)	52	49.4	60	58
C2M0025120D (SiC)	54	51.6	64	62.5
SCTWA50N120 (SiC)	55.5	52.2	64	61
IPT60R028G7 (Si)	56	51.2	65	61.8

Same as the $T_{j,cruising}$, a 600-second load profile containing the large surge current is used for the $T_{j,max}$ simulation. In the figure 2.26, it shows the plotting of the load profile used for the $T_{j,max}$ simulation. Obviously, during the 600 seconds, the car accelerates and brakes frequently. The suddenly changing of the speed results from the sampling error.

As mentioned previously, the initial junction temperature at the beginning of the 600s simulation is assumed to be the $T_{j,cruising}$. A statistic on the results of the $T_{j,max}$ simulation is shown in the table

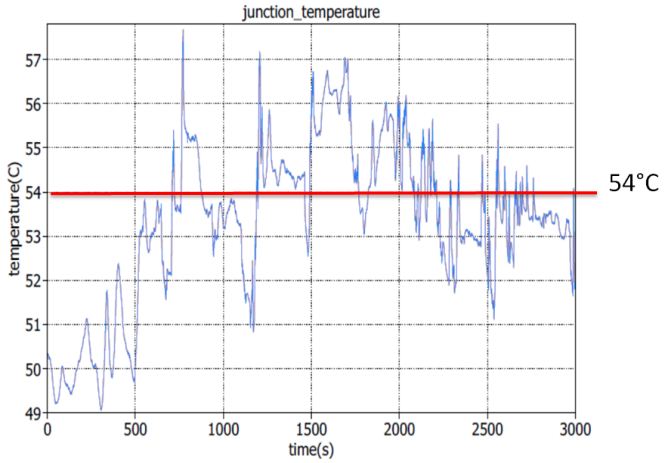


Figure 2.24: The T_j waveform of the 20kHz_d motor drive with the C2M0025120D in the $T_{j,cruising}$ simulation

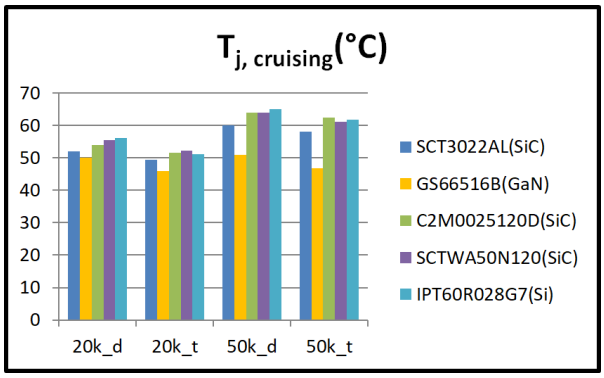
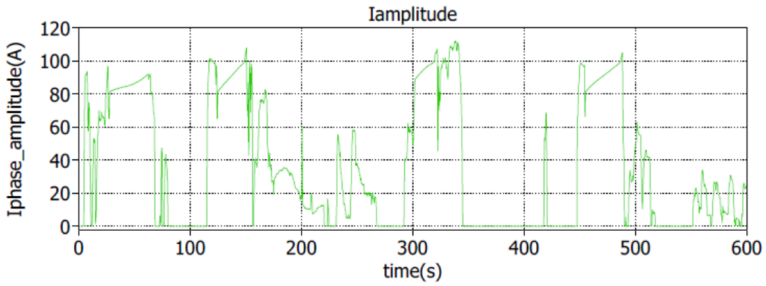
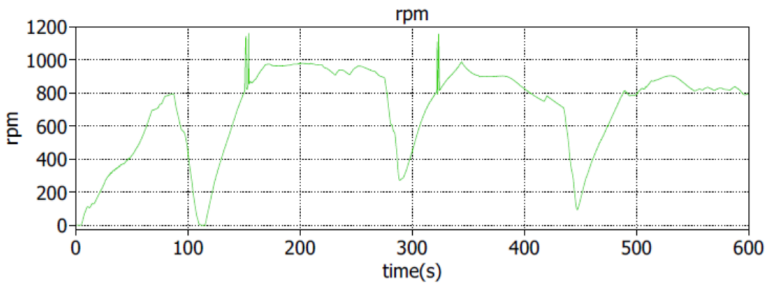


Figure 2.25: Statistics of the $T_{j,cruising}$ for all the design candidates



(a) $I_{phase}(amplitude)$



(b) speed

Figure 2.26: Load profile used for the $T_{j,max}$ simulation

2.11. Similarly, the relevant plotting based on the table 2.11 is shown in the figure 2.28. Accordingly, several design candidates are proved to be unsuitable for the required user's conditions. Especially, the design with double parallel MOSFET is not suitable for most of the MOSFET candidates, but for the one with triple parallel MOSFET nearly all kinds of MOSFET can be used. Besides, it is obvious that the CoolMOS™ can not be switched with a frequency as high as 50kHz where as the SiC and GaN MOSFET can.

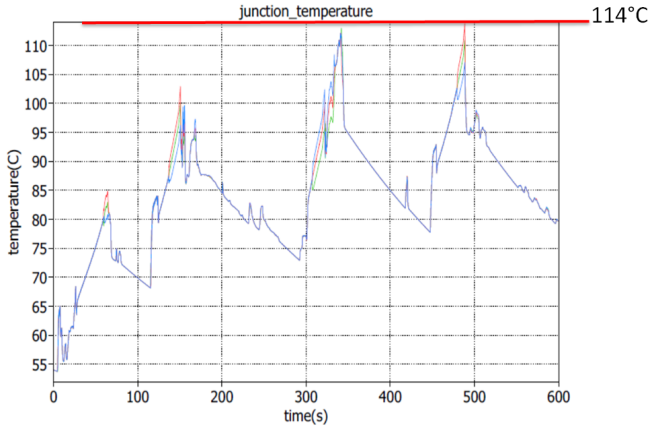


Figure 2.27: The resultant T_j waveform of the 20kHz_d motor drive with the C2M0025120D in the $T_{j,max}$ simulation

Table 2.11: $T_{j,max}$ simulation results of all the design candidates

	$T_{j,max}(^\circ C)$			
	20kHz_d	20kHz_t	50kHz_d	50kHz_t
GS66516B (GaN)	430	99	470	100
SCT3022AL (SiC)	92	72	106	82
C2M0025120D (SiC)	114	83	132	95
SCTWA50N120 (SiC)	132	93	144	104
IPT60R028G7 (Si)	215	111	315	152

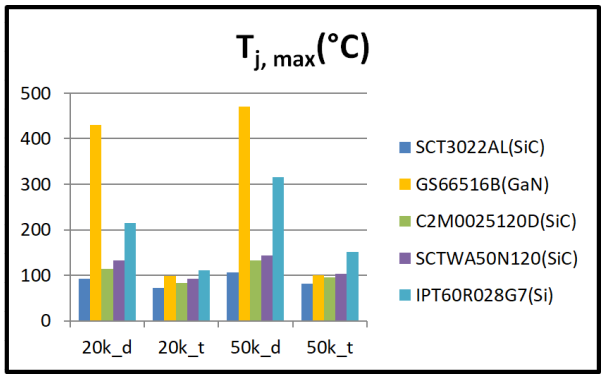
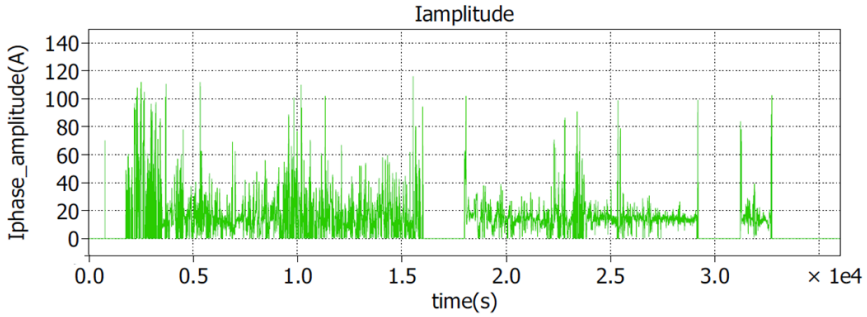


Figure 2.28: Statistics of the $T_{j,max}$ for all the design candidates

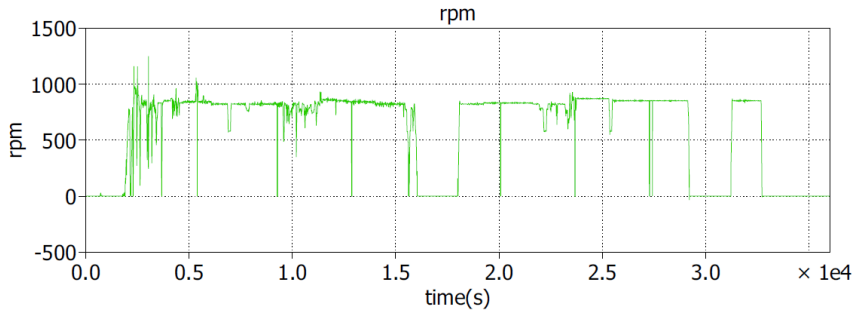
2.5.4. Efficiency evaluation

Based on the simulated $T_{j,cruising}$, the efficiency of the motor drive can be simulated with the simplified inverter loss model without small time step. Fixing the junction temperature at the $T_{j,cruising}$ should not end in big error on the efficiency evaluation because such a evaluation is based on a time scale as long as one day during which the junction temperature is kept around the $T_{j,cruising}$ mostly.

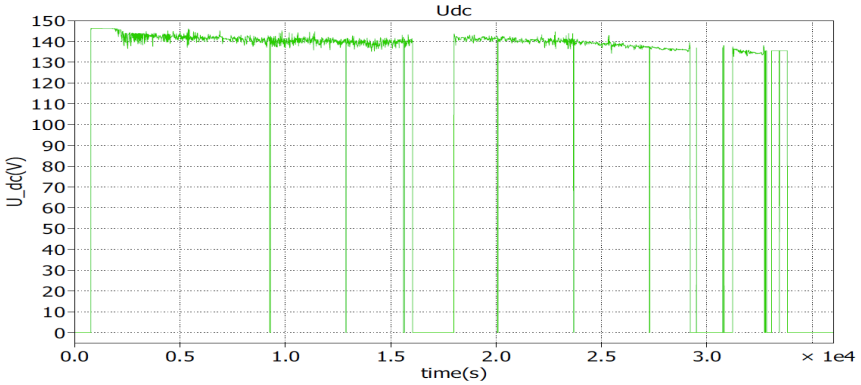
In order to compare the efficiency of the new motor to be designed and the old one that is currently used, a power loss model of the old motor drive is also established based on its datasheet[31]. Furthermore, the load profile in the first day is chosen for the efficiency simulation and the phase current amplitude profile and the DC bus voltage profile are depicted in the figure 2.29. There are some sampling problems so the current, speed and the DC bus voltage suddenly fall to zero at some instants. However, few such instants exist in the whole day so the problem does not bring too much error on the simulation result.



(a) $I_{phase}(amplitude)$



(b) speed



(c) DC bus voltage

Figure 2.29: Load profile used for the efficiency test

As an example, the efficiency simulation result of the 20k_t motor drive with the C2M0025120D is shown in the figure 2.30. A statistic of the efficiency of all the designs that pass the temperature evaluation is shown in the table 2.12 and the relevant statistic plotting is shown in the figure 2.31.

As we can see, the GaN MOSFET has the highest efficiency among all the design candidates. Besides, the triple MOSFET motor drive has generally higher efficiency than the double MOSFET motor drive.

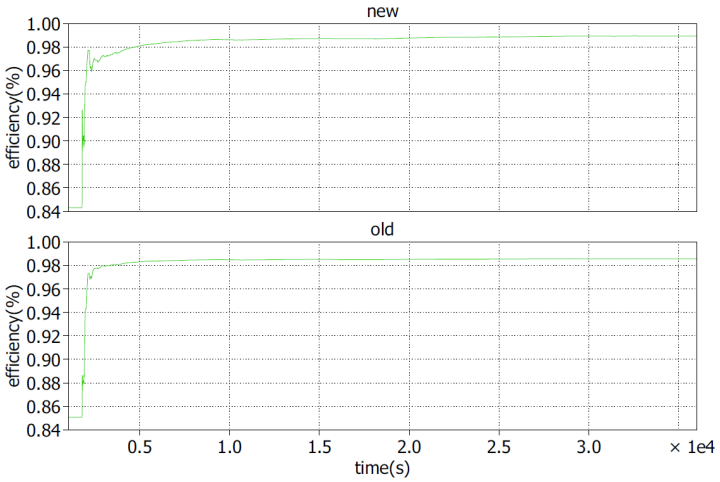


Figure 2.30: The resultant efficiency trend of the 20k_t motor drive with C2M0025120D in the efficiency test

Table 2.12: Efficiency test results of all the design candidates

	efficiency (%)			
	20kHz_d	20kHz_t	50kHz_d	50kHz_t
GS66516B (GaN)	-	99.16	-	99.11
SCT3022AL (SiC)	98.87	99.14	98.37	98.63
C2M0025120D (SiC)	98.53	98.92	97.94	98.28
SCTWA50N120 (SiC)	98.32	98.43	97.8	98.76
IPT60R028G7 (Si)	-	98.62	-	-
Old motor drive	98.56			

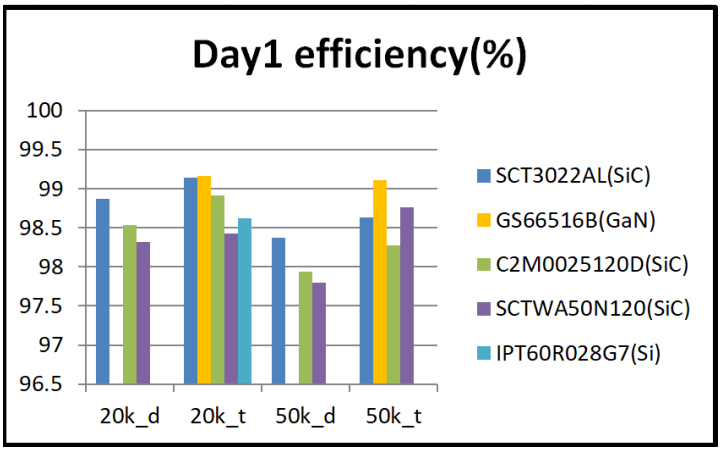


Figure 2.31: Statistics of the efficiency for all the design candidates

2.6. Summary

In this chapter, the 1-D modelling of the control system, the power loss and the thermal performance is introduced. Among all the content presented, the followings are crucial and need to be emphasized.

- The switching loss modelling is difficult to be accurate without measurements. Although the SPICE simulation is used to make the modelling as precise as possible, it still fails to include the gate drive loss and the influence of the parasitic inductance of the PCB trace on the switching loss. The switching loss estimated here is underestimated, which results in a relative high efficiency of the motor drive.
- The 1-D thermal modelling is simple and is suitable for roughly simulating the thermal perfor-

mance of the motor drive. However, the simulation result is not accurate because of the difficulties encountered on the accurate estimation of the thermal resistance and capacitance. Besides, it fails to give information on the temperature distribution on the PCB.

- The high current in the load profile is not necessary. However, this conclusion might not be true because of the wrongly estimation on the motor parameters. To get a more accurate result, measurements on the motor is necessary.
- Among all the design candidates, the motor drive with the triple parallel GaN MOSFET has the highest efficiency and its maximum junction temperature does not exceed $150 \circ C$ in the worst operation condition. Between the 20kHz and 50kHz switching frequency, the latter one is preferable although it has relative lower efficiency. This stems from that the whole efficiency of the power-train probably has a higher efficiency by using 50kHz switching frequency. Using a higher switching frequency decreases the motor drive efficiency but improves the motor efficiency. However, this statement might be wrong and need to be validate by the test with hardware.

Built on the results presented in this chapter, the following proceeds.

- Because of the defects of the 1-D thermal modelling, a more accurate 3-D thermal modelling is used. Before the 3-D modelling, a layout design needs to be finished to get the geometrical shape of the motor drive. Thus, a hardware design is needed for the next step.
- As will be mentioned in the hardware design, because of the difficulties encountered on the symmetrical layout design with triple parallel MOSFET, a 4-parallel MOSFET topology is considered. An efficiency simulation is done to check whether adding one more parallel MOSFET decreases the efficiency or not and the result is shown in the table 2.13. In the table 2.13, the abbreviation 50kHz_q means motor drive with qudra parallel MOSFET and 50kHz switching frequency.

Table 2.13: Efficiency of the 3-parallel MOSFET motor drive and the 4-parallel MOSFET motor drive

	efficiency (%)	
	50kHz_t	50kHz_q
GS66516B (GaN)	99.11	99.35

Although the switching loss is underestimated because of the neglected gate drive loss and influence of the parasitic inductance, the efficiency of the motor drive with 4-parallel MOSFET should not be different from the one using 3-parallel MOSFET too much. It is because the conduction loss is dominant in the application and the simulation result shows that the efficiency difference between the two is not huge. Thus, for the convenience on the hardware design, the design is decided to be a motor drive using GaN MOSFET with a 50kHz switching frequency and 4-parallel MOSFET topology.

3

Hardware design

After determining the general profile of the motor drive, a more detailed hardware design will be introduced in this chapter.

Basically, the design of a motor drive consists of the power stage circuit, gate driver circuit, sensing circuits, protection circuits and control circuits. In the design of this motor drive, only the first four is included because the control circuit is decided to be the platform LAUNCHXL-F28069M from the Texas Instruments Inc. to reduce the workload on the hardware design and leave more time on the 3-D modelling.

In the user's guide [1], the implementation of the sensorless FOC control in the micro-controller TMS320F28069M is introduced. Such a sensorless solution, InstaSPIN-FOC™, contains the so called FAST™ estimator to achieve sensorless FOC. An overview on the parameters related with FAST™ estimator is shown in the figure 3.1

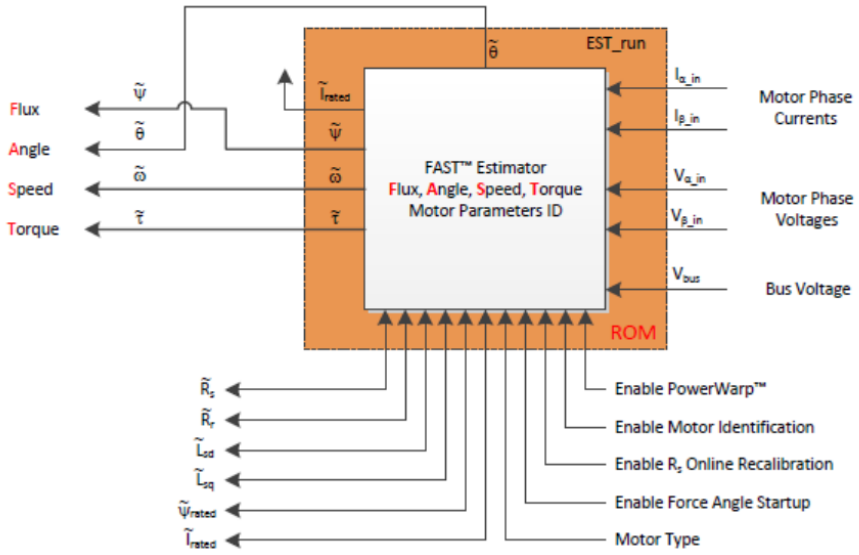


Figure 3.1: Estimating Flux, Angle, Speed, Torque (FAST™ estimator)[1]

Apparently, in order to enable the sensorless FOC, the values of the phase current, the DC bus voltage and the phase voltage are necessary. For the first two, sensing circuit is designed to acquire them. However, the latter one can be reconstructed through the PWM pulses pattern.

The design of the measurement circuits and the protection circuits basically references a similar design [32] from Texas Instrument Inc.. As for the design of the gate driver and the power stage, a similar design [29] from GaN Systems Inc. is referenced as well.

3.1. System layout description

In the table 3.1, the key system specifications are shown. The design includes sensing circuits used for the parameters that are necessary for the control. Besides, the MOSFET protection is also considered, which consists of the overload protection, over-voltage protection, short circuit protection, ground-fault protection and over-temperature protection.

Table 3.1: Key system specifications

Parameters	Specifications
Maximum DC bus voltage	150V
Gate driver supply voltage	Isolated driver: 5V for the input side, 9V for the driver side
MOSFET (GS66516B)	Voltage rating: 650V, Current rating: 60A @ $T_j = 25°C$, 47A @ $T_j = 100°C$
Rated power capacity (@$T_j = 25°C$)	15.6kW
Inverter switching frequency	50kHz
Micro-controller	TMS320F28069M
Motor	3-phase BLDCM
Feedbacks	Phase current, DC bus voltage, MOSFET case temperature
Protections	Overload, over-voltage, short circuit, ground-fault, over-temperature

In the figure 3.2, the block diagram of the design in system level is shown. The power stage is a separate PCB from the other auxiliary circuit for better cooling, which is briefly discussed in the section 2.4.

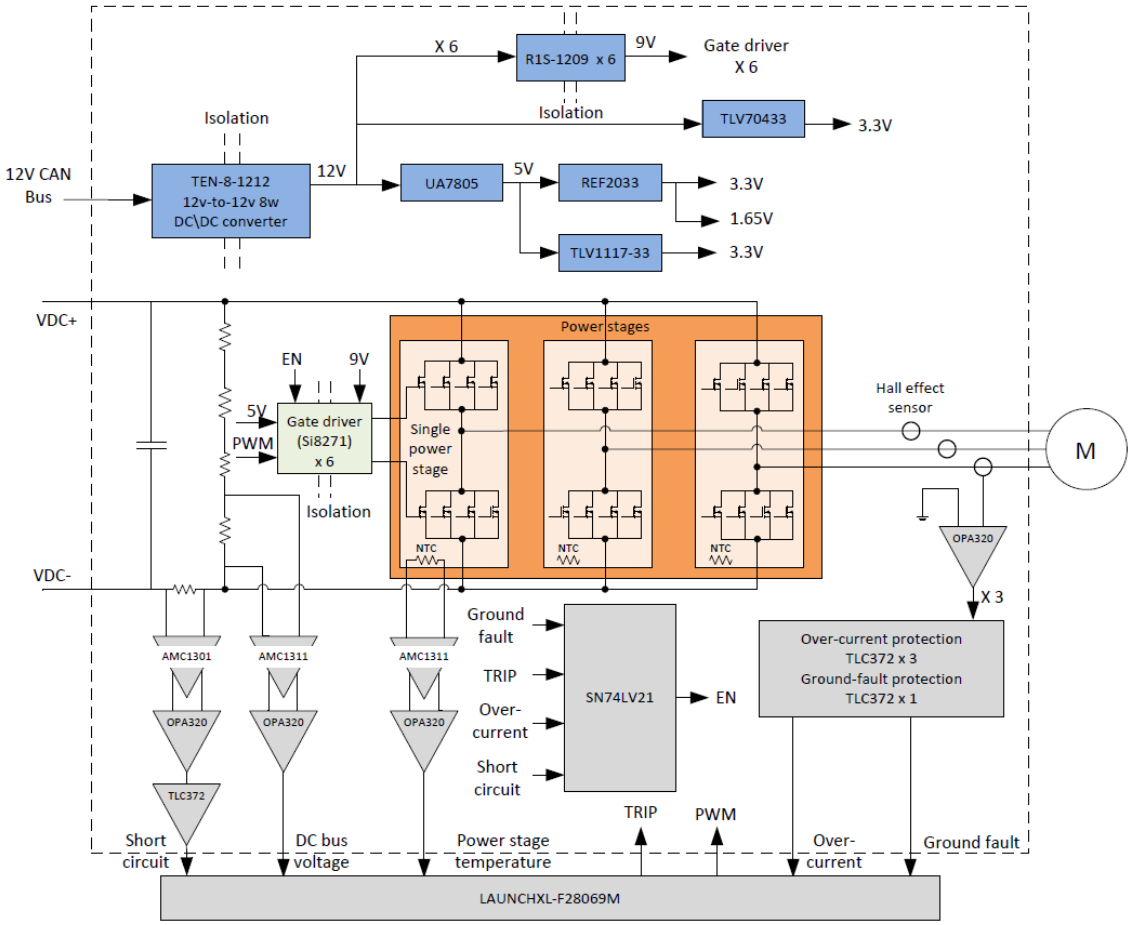


Figure 3.2: System overview of the design

3.2. Sensing circuits design

In overview, the necessary parameters to be sensed for the control are the DC bus voltage and the phase current, which is shown in the figure 3.1. However, for the over-temperature protection, the temperature of the case of the MOSFET is also detected.

3.2.1. DC bus voltage sensing circuit

The sensed DC bus voltage is not only used for the over-voltage and undervoltage protection but also used for the reconstruction of the phase voltage together with PWM pulse pattern.

The schematic of the DC bus voltage sensing circuitry is shown in the figure 3.3. The 150V U_{dc} is scaled down by the resistors in series. In order to achieve high accuracy of the sensed voltage, resistor with a tolerance of ±0.1% is chosen. The precision, isolated amplifier AMC1311B [33] together with an op-amp OPA320 is used to fed the signal to the MCU.

The voltage is scaled down so that the when the $U_{dc} = 150V$, the input voltage of the AMC1311B is 2V which is the maximum input voltage for a linearity performance of the device. A low-pass differential filter (R79, R80 and C39) is added at the input of the AMC1311B for a better noise performance. The cutoff frequency of the low-pass filter is

$$f_c = \frac{1}{2\pi \cdot 2R \cdot C} = \frac{1}{2\pi \cdot 2 * 39 \cdot 0.01 * 10^{-6}} = 204kHz$$

After AMC1311B whose gain is one, the signal is filtered with a differential filter (R81, R82 and C42) with a cutoff frequency 1.7kHz again. Afterwards, because the maximum output of the OPA320 is about 3.3V, which is fed to MCU, the 2V voltage signal need to be amplified. The gain of the OPA320 is designed to be $\frac{15k}{4.7k+4.7k} = 1.6$. Besides, the capacitor C44 and C43 are used to make up filter with a cutoff frequency

$$f_c = \frac{1}{2\pi \cdot 15 * 10^3 \cdot 0.01 * 10^{-6}} = 1.06kHz$$

As we can see latter on, such a differential circuit used in the DC bus voltage sensing circuitry is always used in the whole design because of its much better noise immunity performance than single-end circuit.

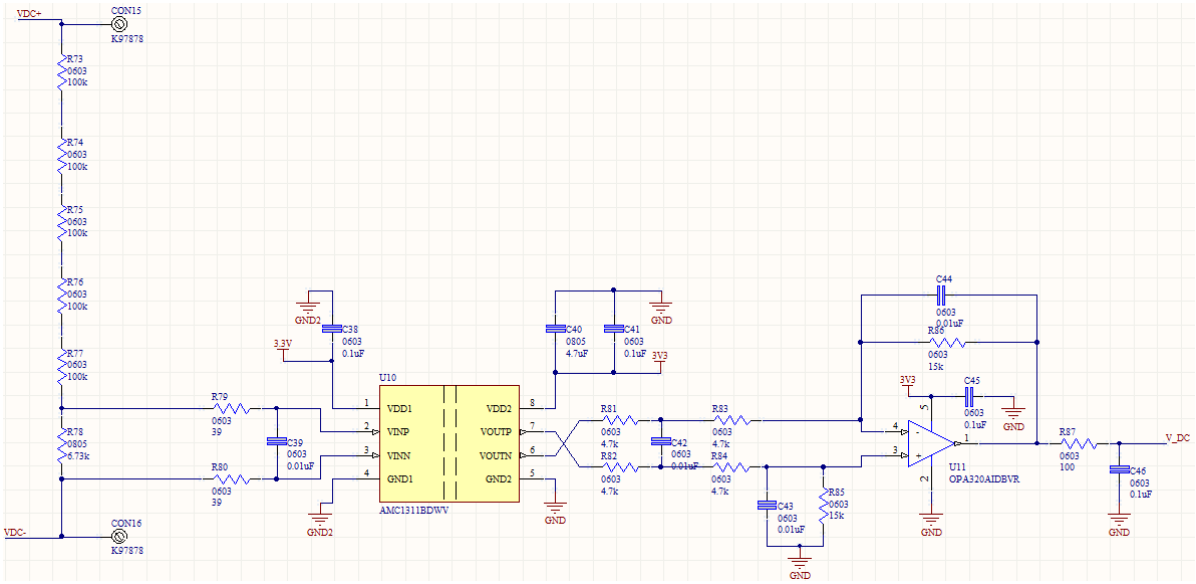


Figure 3.3: Schematic of the DC bus voltage sensing circuit

3.2.2. Phase current sensing circuit

Because of the high current occurs in the accelerating and breaking process, hall effect sensor is used to measure the phase current. The product HC2H200-S from LEM is selected. Although it is an open loop

hall effect sensor, it offers good enough linearity performance. Besides, it has a bandwidth (20kHz) which is much higher than the maximum fundamental frequency 285Hz approached when the car reaches a speed at 100km/h. According to the datasheet [34], the relation between the output voltage of the HC2H200-S and the phase current is:

$$I_p = (V_{out} - \frac{V_c}{2})\frac{1}{G}\frac{5}{V_c}$$

where $G = 0.01$ indicating the sensitivity of hall effect sensor, V_c is the supply voltage 5V and I_p is the phase current.

The maximum and minimum V_{out} is 5V and 0V respectively with an DC offset 2.5V. To feed the V_{out} to the MCU, the signal is attenuated by using R105 and R106, which attenuate the 5V signal to 3.3V. Afterwards, a filter with a cutoff frequency 3.39kHz is used before the signal is fed to the MCU to increase noise immunity.

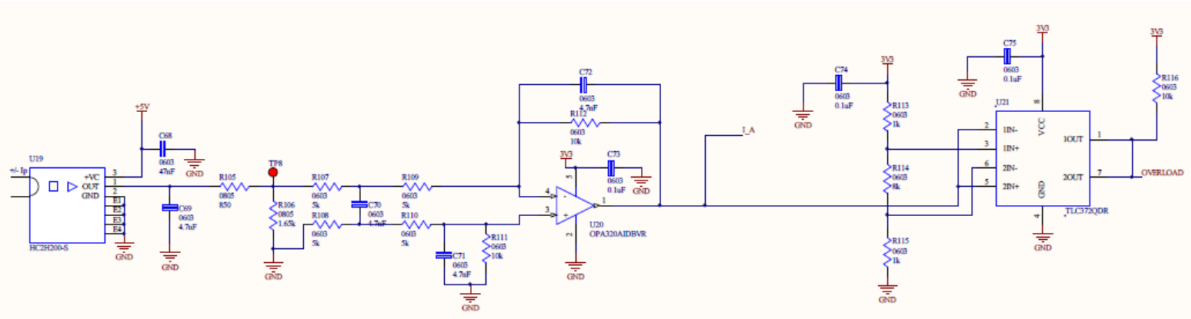


Figure 3.4: Schematic of the phase current sensing circuit

3.2.3. MOSFET case temperature sensing circuit

To measure the temperature of the MOSFET, negative temperature coefficient (NTC) thermistor is used. The B57703M0502A004, whose operating range is between $-25°C$ $125°C$[35], is selected because the junction temperature should be controlled below $150°C$. As the temperature of the case is measured, for safety consideration the case temperature is controlled below $125°C$. Same signal processing circuit is used for the temperature sensing as the one used for DC bus voltage sensing.

To increase the resolution and accuracy of the measurement, the 3.25k resistor with a tolerance of ±0.1% is connected in series with the NTC thermistor so that when the temperature is at $25°C$, the input voltage of the AMC1311B is 2V.

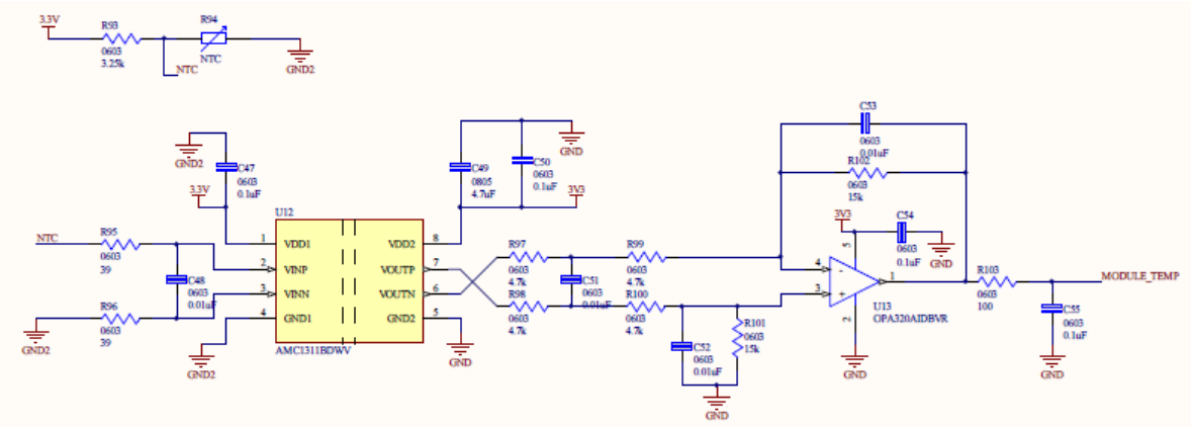


Figure 3.5: Schematic of the MOSFET case temperature sensing circuit

3.3. Protection circuits design

Protection circuit is implemented to ensure the motor drive and the motor operate in safe conditions. Basically, for the safe operation of the motor drive, the current through the MOSFET should never exceed the maximum current rating and the junction temperature of the MOSFET should also be kept below $150°C$. As for the motor, it is necessary to avoid ground fault to protect the motor from being burned.

3.3.1. Over-temperature protection circuit

The temperature of the MOSFET is sensed by the temperature sensing circuitry introduced in the subsection 3.2.3. The sensed analog signal of the temperature is fed to MCU. When is detected temperature is higher than the threshold, the motor drive will be stop from operation to prevent the irreversible damage on the MOSFET. Although the reaction speed is not fast through this way, the thermal capacitance of the MOSFET decreases the requirement on the response speed of the protection circuitry.

3.3.2. Short circuit protection circuit

The short circuit protection is used to avoid a short circuit that results from the simultaneous switch-on of the upper and lower MOSFETs in the same phase leg. Although a dead time is used to prevent such short circuit problem, double safeguard procedure is used to avoid the permanent damage on the MOSFET.

The circuitry is shown in the figure 3.6. As it is shown, a resistor is used to detecting the DC bus current. This resistor R1 is placed after the DC link capacitor because the surge current due to short circuit is mainly from the capacitor.

Nevertheless, because of the high switching frequency of the MOSFET, the di/dt is very high. As it will be shown in the subsection 3.4.5, the DC decoupling capacitor should be placed as close as possible to the MOSFET to reduce the inductance in between. Therefore, except the DC bus capacitor placed just after the DC voltage input, there are DC decoupling capacitors which is placed closer to the power stage. However, the resistor cannot sense the short circuit current from these capacitors which is a defect in the design.

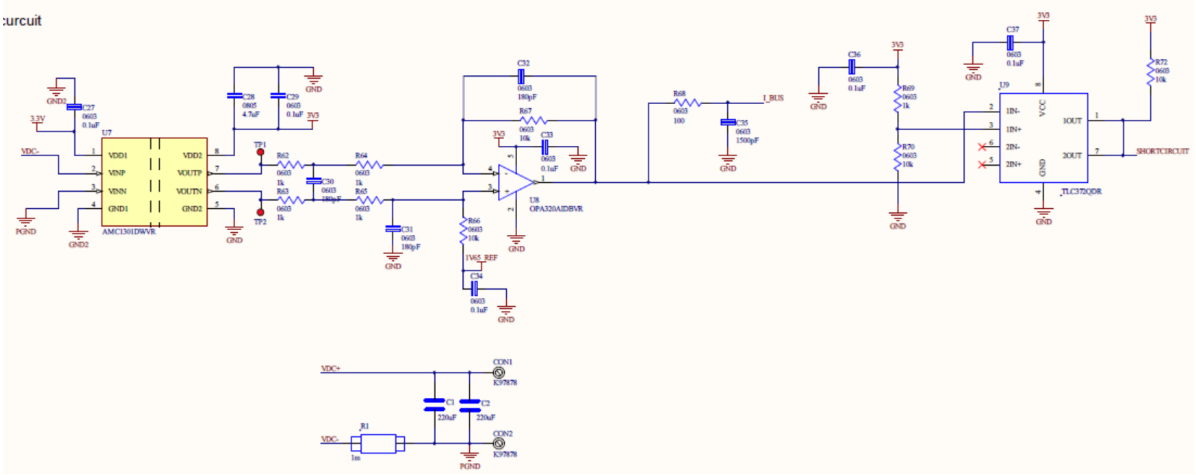


Figure 3.6: Schematic of the short circuit protection circuit

The highest DC bus current occurs when the motor drive operates with the maximum power. Basically, this maximum power appears when both the back EMF and the phase current are high. In another words, a typical scenario is that the car breaks at a high speed. Assuming the maximum speed is 90km/h, a roughly estimation is:

$$I_{dc,max} = \frac{3EI_{phase}}{U_{dc,min}} = \frac{3\times 47.46 \times 120}{2 \times 120} = 72A \tag{3.1}$$

Given the resistor R1 is $1m\Omega$, the maximum voltage on R1 is 72mV. For a higher resolution of the

measured result, AMC1301 whose input range is ±250mV is selected. The gain of AMC1301 fixed at 8.2 [36]. Thus, the output signal of the AMC1301 is amplified 5 times and fed to the MCU. As the AMC1301 has bipolar output, a reference voltage 1.65V is used to change the bipolar signal into uniploar signal. The comparator TLC372QDR [37] is used to change the analog signal into digital signal fed to the MCU directly, which is used to make the protection response faster.

The threshold of the input voltage to the comparator is 3V. Therefore, assuming R70=$10k\Omega$, the resistor used for the threshold setting is

$$R69 = 10000 \times \frac{0.3}{3} = 1k\Omega \tag{3.2}$$

3.3.3. Overload protection circuit

Although the phase current is sensed and fed to the MCU. However, the overload protection is required to have faster reaction speed. Therefore, the comparator TLC372QDR is used to change the analog signal into digital signal fed to the MCU directly. The circuitry is shown in the figure 3.7.

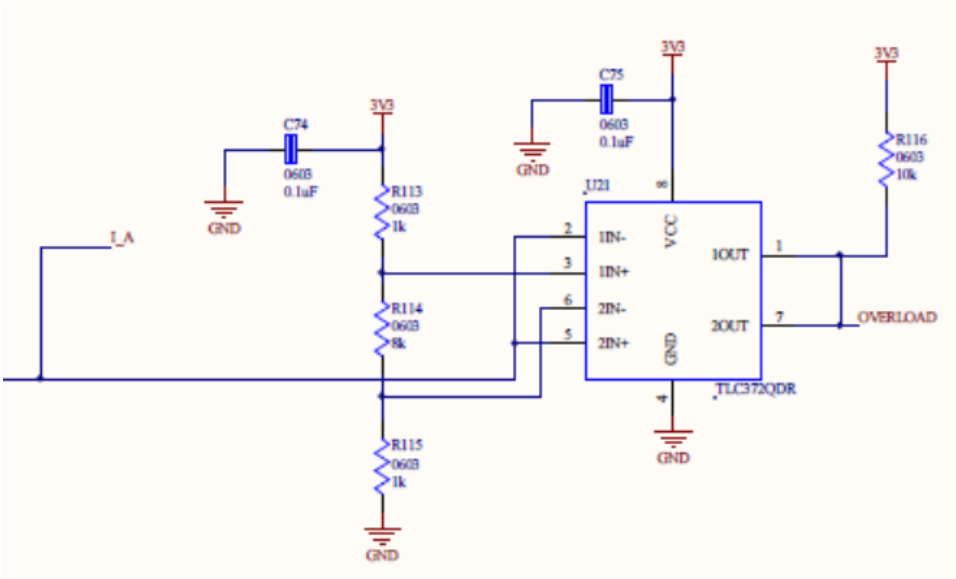


Figure 3.7: Schematic of the overload protection circuit

To guarantee the safe operation of the MOSFET, the phase current can not exceed the maximum rating at the high junction temperature. When $T_j = 100°C$, the $I_{ds,max} = 47$. Thus, the maximum current rating for the motor drive is considered as 180A. Accordingly, the output voltage of the hall effect sensor is 4.3V and 0.7V when $I_{phase} = \pm 180A$ respectively. After attenuation, the input voltage to the comparator has a range of 2.838V-0.462V. Thus, assuming $R114 = 8k\Omega$, the resistors for setting the threshold can be derived with the formula:

$$\frac{3.3}{R_{up} + R_{low} + 8000}(8000 + R_{low}) = 2.838V \tag{3.3}$$

$$\frac{3.3}{R_{up} + R_{low} + 8000}R_{low} = 0.462V \tag{3.4}$$

3.3.4. Ground-fault protection circuit

Theoretically, when the motor operates properly the three-phase current is in balance, which means the sum of the three-phase current is zero. The threshold for ground fault condition 5A is determined by referencing [32]. Accordingly, the higher and lower threshold of the input voltage of the comparator are

$$U_{low} = 2.45\frac{1.65}{2.5} = 1.617V \tag{3.5}$$

$$U_{up} = 2.55\frac{1.65}{2.5} = 1.683V \tag{3.6}$$

The circuitry of the ground-fault is shown in the figure 3.8. The three-phase current is summed by using the $10k\Omega$ resistor. The ground fault signal is sent to the MCU directly as well as used to disable the gate driver.

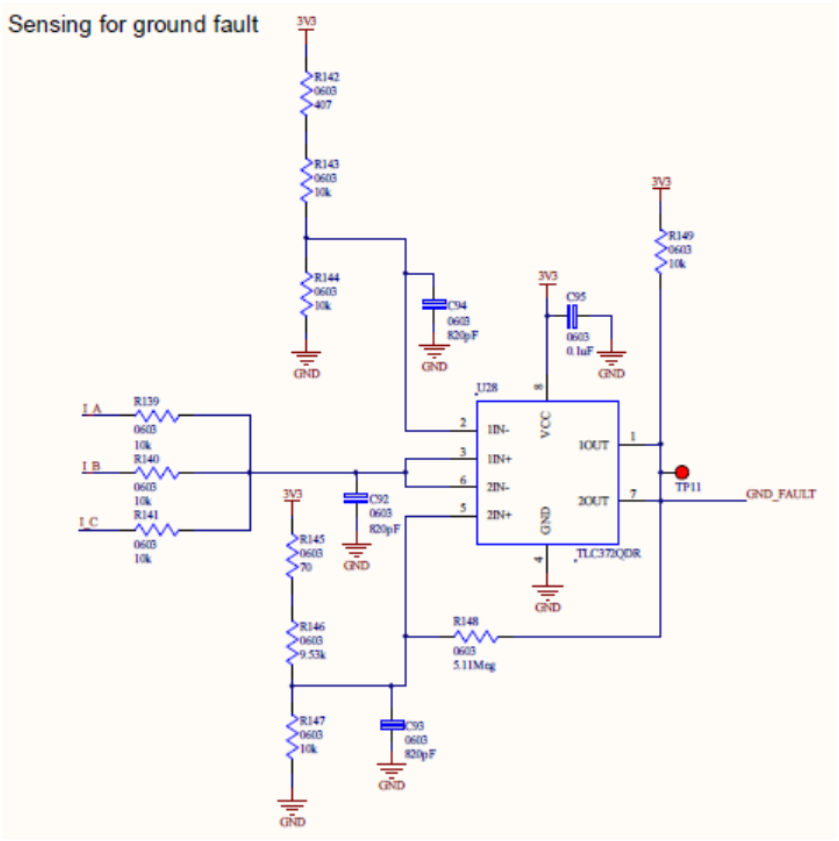


Figure 3.8: Schematic of the ground-fault protection circuit

3.3.5. Gate driver enable circuit

All the digital outputs of the protection circuitry are fed to a logic AND gate SN74LV21ADR [38] whose output is used to enable the gate driver. The circuitry is shown in the figure 3.9.

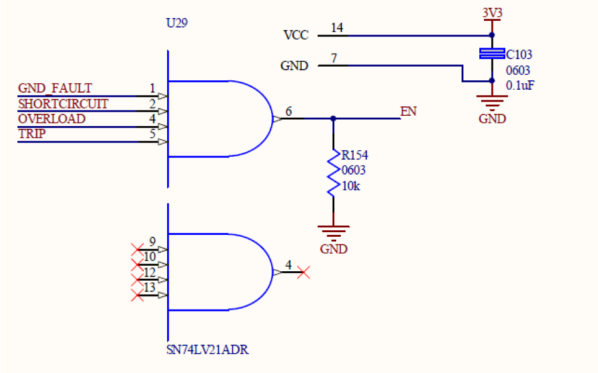


Figure 3.9: Generating enable signal for the gate driver

3.4. Gate driver and power stage design

3.4.1. Overview on the gate driver and power stage design

The gate driver together with the power stage is the most challenging part in the design of this motor drive. Basically, the challenges result from two points. The first one is that due to the high switching frequency the parasitic elements in the PCB circuit and the device itself bring severe problems. The second lies on the balance between the parallel MOSFETs. In details, several key parameters that have impact on the balance performance of the MOSFETs are[39]:

- $R_{ds(on)}$: influence the statistic current sharing between the parallel MOSFETs,
- threshold gate-source voltage $V_{gs(th)}$: influence the switching dynamics of the MOSFETs because the lower the value is the earlier the MOSFET is turned on,
- trans-conductance g_m: influence the current sharing during the switching transient,
- parasitic elements in the gate driver loop and power loop.

The first three are all temperature dependent. Thus, a more evenly distributed temperature helps improve the reliability of the motor drive. Besides, the influence of the parasitic elements on every parallel MOSFET should be controlled same.

In overview, the design should be kept as compact as possible. In the meanwhile, a good symmetrical layout should be used so that the MOSFETs in parallel have balanced performance. In order to achieve this, the design [29] shows a good example on how to fulfill all the requirements. The design use a vertical structure shown in the figure 3.10 which separates the power stage and the gate driver on two different PCB. In this way, both of the requirements of symmetrical and compact layout are satisfied. Therefore, the concept is referenced in design here. Besides, as mentioned previously, because of the excellent cooling performance of the IMS PCB, it is also chosen for this design.

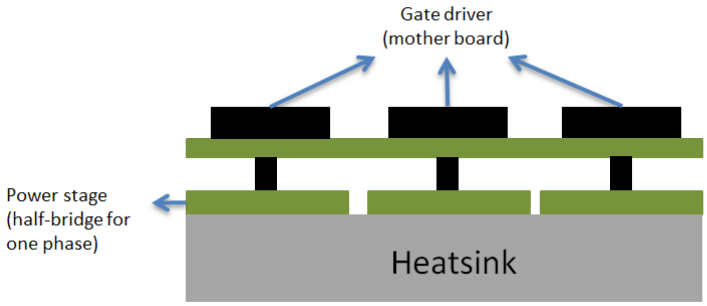


Figure 3.10: Solution using a vertical structure

3.4.2. Parasitic elements identification

Before go into detailed analysis on the influence of the parasitic elements, it is necessary to clarify what kind of parasitic elements are of concern. Basically, the analytic model used here is same as the ones in the referenced [40] and [41].

In the figure 3.11, the analytic model of a half bridge together with the parasitic elements is shown. Because of the large inductance of the motor wingding, the load can be simplified as an ideal current source. Besides, as the switching transient is rather short, the voltage V_{sw} at the phase connection point can be assumed to be constant as well. Further more, as the voltage V_{sw} at the phase connection point is assumed to be constant, the voltage $V_D = V_{dc} - V_{sw}$ is also constant if the DC bus voltage V_{dc} is also assumed to be constant.

For simplicity, the parasitic inductance of the PCB trace can be categorized as three types. The first one, power loop inductance $L_{loop} = L_{d0} + L_{s0} + L_{d1} + L_{s1} + L_{d2} + L_{s2}$, is the parasitic inductance existing only in the power loop. The second is the gate inductance L_g which only exists in the gate driver loop. The final one is the coupling inductance L_{couple} between the gate driver loop and the power loop, which is L_{ss1} and L_{ss2} for the upper and lower MOSFET respectively.

For the following switching analysis, only the high-side MOSFET is discussed for simplicity. The switching transient of the low-side MOSFET can be derived with the same method. Thus, the low-side MOSFET can be simplified as the body diode together with its parasitic capacitance C_f in which the reverse-recovery charge is stored. And the L_{d2}, L_{ss2} and L_{s2} can be combined as one inductance L_{low} because their same influence on the switching behaviour of the upper MOSFET. The simplified model for the following analysis is shown in the figure 3.12. Accordingly, the power loop inductance can be rewritten as $L_{loop} = L_{d0} + L_{s0} + L_{d1} + L_{s1} + L_{low}$.

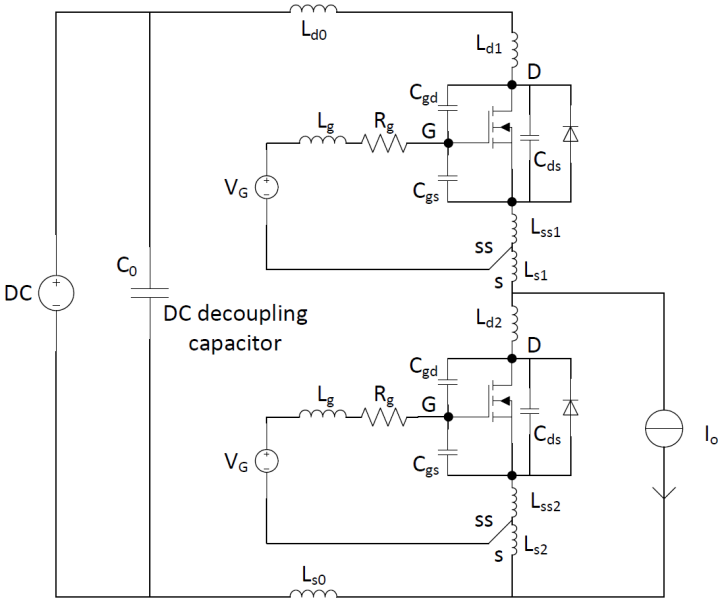


Figure 3.11: Half bridge including parasitic elements

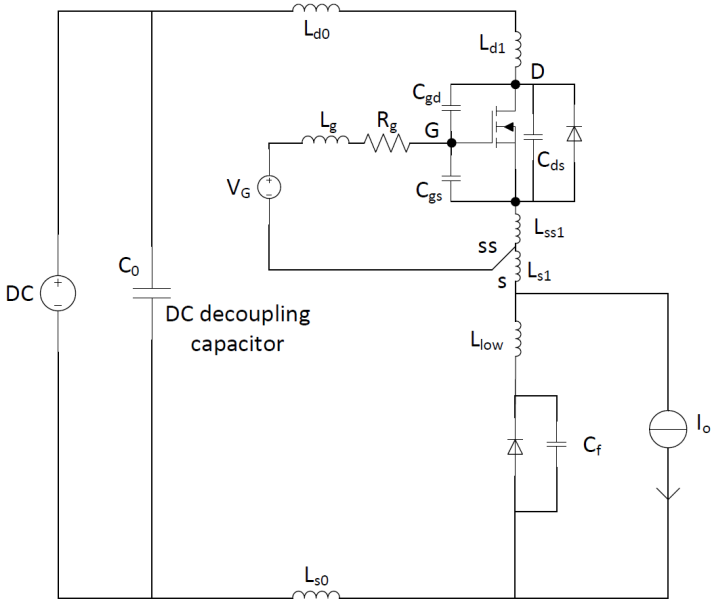


Figure 3.12: Simplified model for the switching analysis

Based on the simplified model, the voltage equation in the gate drive loop is

$$V_G = R_g i_g + V_{gs} + L_{ss1}\frac{di_d}{dt} + (L_{ss1} + L_g)\frac{di_g}{dt} \tag{3.7}$$

where the drain current is i_d and the gate driver sink/source current i_g is

$$i_g = C_{gs}\frac{dV_{gs}}{dt} + C_{gd}\frac{dV_{gd}}{dt} \tag{3.8}$$

The voltage drop on the L_g is neglected because compared with the voltage drop on the gate resistance it is rather low. Besides, the voltage drop on the L_{ss1} induced by di_g/dt is also neglected because di_g/dt is very small compared with di_d/dt.

The voltage equation in the power loop is

$$V_{ds} = V_D - (L_{loop} + L_{ss1})\frac{di_d}{dt} + L_{ss1}\frac{di_g}{dt} \tag{3.9}$$

The voltage balance between the three parasitic capacitance in the MOSFET is

$$V_{ds} = V_{gs} + V_{gd} \tag{3.10}$$

3.4.3. Switching transient analysis

The influence of the parasitic elements on the switching behaviour in each stage of switching process will be discussed separately.

- Turn-on transient analysis:

  An idealized turn-on transient is illustrated in the figure 3.13 ignoring the oscillations induced by resonance. The analysis will proceed stage by stage.

  1. Stage t_0-t_1:

     At the beginning, the output of the gate driver jump from $V_{G(sink)}$ to $V_{G(source)}$ and starts to charge the input capacitance C_{iss}, which equals the sum of C_{gs} and C_{gd}, through the gate driver loop. V_{gs} is built up while there is no obvious change in the waveform of V_{ds} as the di_g/dt and L_{ss1} is low. The MOSFET still stays in cutoff status before the V_{gs} rise up to the threshold voltage V_{th}.

     According to the equation 3.7, the induced voltage on L_g has negative feedback on the rising of V_{gs}. Thus, the different value of the parasitic inductance L_g results in the different delay on the turn-on of the MOSFET.

  2. Stage t_1-t_2:

     The current starts to flow through the channel when V_{gs} reaches V_{th}. The MOSFET starts to conduct current, the drain current rise up in this stage which induces voltage drop on the L_{loop} and L_{ss1}. According to the formula 3.9 and ignoring di_g/dt, the voltage across the MOSFET drops to $V_{ds} = V_D - (L_{loop} + L_{ss1})\frac{di_d}{dt}$.

     Two possible scenarios could happen in this stage. The first one is the MOSFET works in ohmic region if $V_{ds} <= V_{gs} - V_{th}$. Otherwise, the MOSFET works in the saturation region. According to the equation 3.9, the first scenario happens only when the L_{loop} and L_{ss1} are too big.

     Normally, in a good design the two parasitic inductance should be limited under a very low value. Therefore, despite the rapid current change in the switching transient, the voltage drop across the loop inductance is low. So, the second scenario is the normal case. Therefore, the channel current i_{ch} has the following relation with V_{gs}:

     $$i_{ch} = \frac{g_m}{2}(V_{gs} - V_{th}) \tag{3.11}$$

     where g_m is transconductance of the MOSFET. The channel current is the sum of the drain current and the charge or discharge current of the parasitic capacitance, which can be described as

     $$i_{ch} = i_d + C_{gd}\frac{dV_{gd}}{dt} - C_{ds}\frac{dV_{ds}}{dt} = I_o - C_f\frac{dV_{ds}}{dt} + C_{gd}\frac{dV_{gd}}{dt} - C_{ds}\frac{dV_{ds}}{dt} \tag{3.12}$$

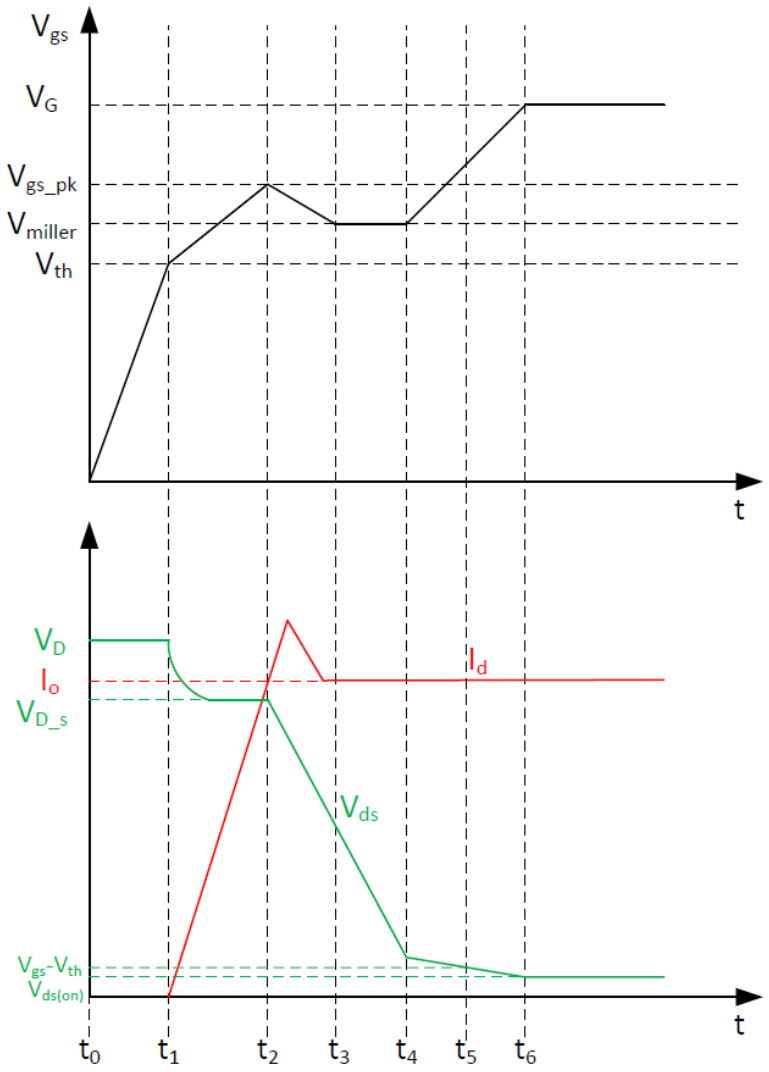


Figure 3.13: Turn-on transient of the upper MOSFET

According to the formula 3.7 and 3.10 and neglecting the small change of the V_{ds} ($dV_{ds}/dt = 0$), the derivative of the V_{gs} can be derived:

$$\frac{dV_{gs}}{dt} = \frac{V_{G(source)} - V_{gs} - L_{ss1}\frac{di_d}{dt}}{R_g(C_{gd} + C_{gs})} \tag{3.13}$$

It is obvious, the induced voltage of the L_{ss1} has a negative feedback on the $\frac{dV_{gs}}{dt}$. V_{gs} rises slower than it does in the first stage. Reducing L_{ss1} helps with decreasing the switch-on loss. Finally, V_{gs} reaches the peak value V_{gs_pk} at the end of the stage where the drain current also reaches the load current I_o.

3. Stage t_2-t_3:
   The freewheeling body diode change into reverse-recovery status in this stage. Therefore, V_{ds} starts to drop. An overshoot in the current waveform can be observed which results from the reverse-recovery charge of the freewheeling diode. Both the parasitic capacitance C_{gd} and C_{ds} start to release charge through the channel of the MOSFET. As V_{ds} drops rapidly, the gate current from the gate driver is not sufficient to release the charge in C_{gd}. Thus, C_{gs} is also discharged to meet the demand which results in a drop of V_{gs}. The resonance induced by the parasitic elements L_g, C_{gs}, L_{loop}, C_{gd} and C_f starts. According to [40], L_{loop}

has dominant influence on the damping of the resonance happening in this stage. To some extend, the larger the L_{loop} is the less the damping is.
However, for the GaN MOSFET, the resonance damps out fast because its reverse-recovery charge is zero.

4. Stage t_3-t_4:
In this stage, the resonance damped out and both i_d and V_{gs} reaches a stable value. For i_d, it equals the load current i_o while V_{gs} stays at the miller plateau V_{miller}. This stage ends when the gate driver is capable to discharge C_{gd} and charge C_{gs} together. Based on the equation 3.7, the voltage drop speed in this stage is:

$$\frac{dV_{ds}}{dt} = \frac{V_{G(source)} - V_{miller}}{R_g C_{gd}} \tag{3.14}$$

5. Stage t_4-t_5:
In this stage, V_{gs} slowly rises up to $V_{G(source)}$. At $t = t_5$ when $V_{ds} = V_{gs} - V_{th}$, the MOSFET goes into ohmic region.
6. Stage t_5-t_6:
At the beginning of this stage, MOSFET goes into ohmic region and $V_{ds(on)} = i_d R_{ds(on)}$. However, as V_{gs} still needs to increase until $V_{gs} = V_{G(source)}$, the $R_{ds(on)}$ keeps decreasing in this stage, which results in a slowly decrease of $V_{ds(on)}$.

- Turn-off transient analysis:

Same as the turn-on transient, the turn-off transient is depicted in the figure 3.14.

1. Stage t_0-t_1:
At the beginning, the output of the gate driver drops from $V_{G(source)}$ to $V_{G(sink)}$. The parasitic capacitance is discharged through the gate drive loop and the voltage equation can be given

$$V_{gs} = V_{G(sink)} - (L_{ss1} + L_g)\frac{di_g}{dt} - R_g i_g \tag{3.15}$$

The current i_g in the gate drive loop cannot have infinite di_g/dt because of the stray inductance in the gate drive loop. Therefore, in this stage i_g still stays in a small value and $R_g i_g$ can be ignored in the equation 3.15. Substituting $i_g = C_{gs}\frac{V_{gs}}{dt} + C_{gd}\frac{V_{gd}}{dt}$ and assuming V_{ds} is constant, the equation 3.15 can be rewritten as

$$V_{gs} = V_{G(sink)} - (C_{gs} + C_{gd})(L_{ss1} + L_g)\frac{d^2V_{gs}}{dt^2} \tag{3.16}$$

The MOSFET still works in ohmic region in this stage. With the decrease of V_{gs}, $R_{ds(on)}$ rise up slowly which results in slow increase of $V_{ds(on)}$.
2. Stage t_1-t_2:
In this stage, C_{gs} is still being discharged through the gate drive loop. However, $R_g i_g$ has dominant impact on V_{gs} where as the impact from $(L_{ss1} + L_g)\frac{di_g}{dt}$ is so small that it can be neglected. The voltage equation in the gate drive loop can be rewritten as

$$V_{gs} = V_{G(sink)} - (C_{gs} + C_{gd})R_g\frac{dV_{gs}}{dt} \tag{3.17}$$

Apparently, the discharge speed is slowed down compared with it in the first stage. $V_{ds(on)}$ keeps rising slightly in this stage. At the end of the stage, MOSFET reaches the boundary condition $V_{ds} = V_{gs} - V_{th}$ and will go into saturation region in the following stage.
3. Stage t_2-t_3:
The discharge of C_{gs} through gate drive loop continues in this stage. However, as MOSFET goes into saturation region, the channel current i_{ch} starts to decrease. Based on equation

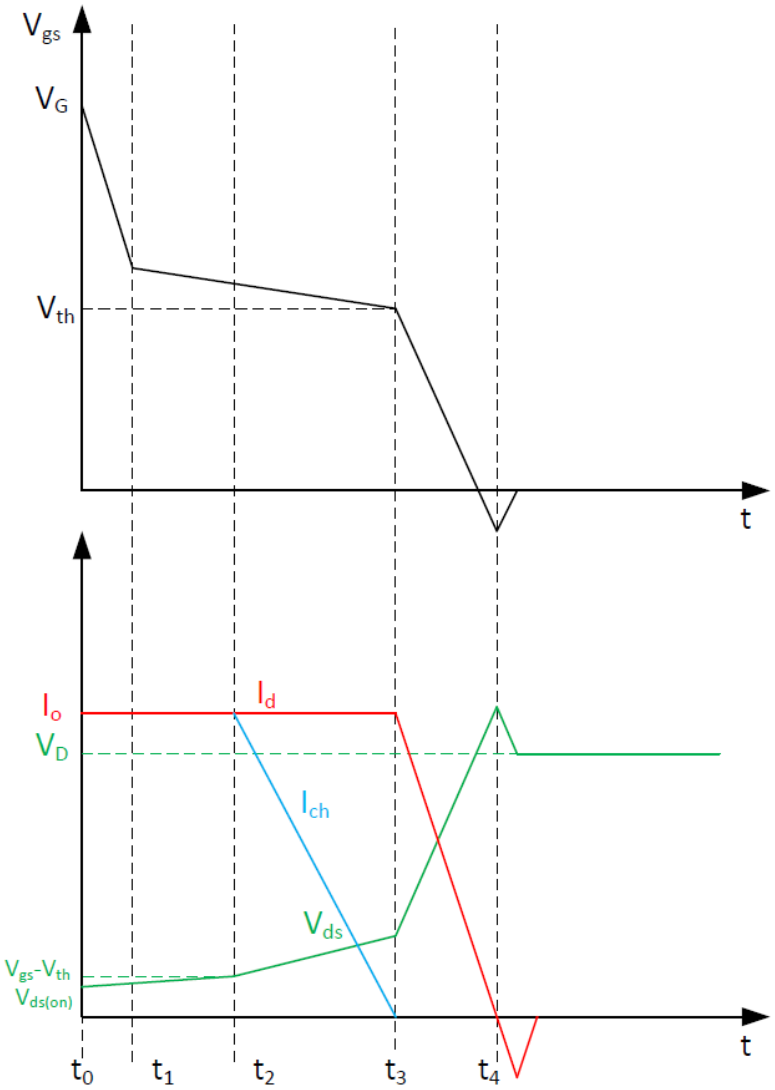


Figure 3.14: Turn-off transient of the upper MOSFET

3.11, 3.12 and the observation that i_d is almost constant in this stage, it can be derived that the unchanged i_d and decreased i_{ch} results in an extra current which charges C_{oss} ($C_{oss} = C_{gd} + C_{ds}$) and makes V_{ds} increase.

According to the equation 3.16, R_g has crucial impact on the duration time of stage 2 and stage 3. A smaller R_g helps to increase the switching speed. However, R_g should not be too small because it helps to prevent the fault turn-on problem during the turn-off, which will be introduced later on.

4. Stage t_3-t_4:

   At the beginning of this stage, V_{gs} reaches the threshold voltage V_{th} and the channel current is cut off. Two resonances starts in this stage. One resonance happens in the gate drive loop and is dominated by L_g, R_g, C_{gs} and L_{ss1}.The other resonance happens in the power loop between the parasitic elements (L_{ss1}, L_{loop}, C_f and C_{ds}). Further more, the two resonances are coupled by C_{gd} and L_{ss1}. However, because of the zero reverse-recovery charge of the GaN MOSFET, the resonance in the power loop is not severe.

   The resonance in the gate drive loop might induced fault turn-on of the MOSFET when the MOSFET has already been turned on. To avoid this, the L_g should be controlled as small as possible. Increasing R_g so that increase the damping of the resonance also helps to prevent this problem. However, it also brings more turn-off loss.

3.4.4. Summary on the influence of the parasitic elements

AS the parasitic capacitance of the MOSFET cannot be controlled once the MOSFET is selected, only the influence of the parasitic inductance will be concluded here.

- L_g: it influence the turn-on delay of the MOSFET. A too big L_g brings more switching loss because it slows down the switching process. Besides, a too big L_g brings fault turn-on problem which might results in the catastrophic short circuit.
- L_{ss1}: it couples the gate drive loop with the power loop. The coupling between the two loop should be reduced as much as possible to reduce the influence of the power loop on the gate drive loop. It has been shown that a too big L_{ss1} increases the switching loss.
- L_{loop}: it slows down the rising and falling speed of the drain current i_d, which results in more switching losses. Besides, a too big L_{loop} might induce lots of problems. For instance, because L_{ss1} is inevitable, the power loop is always coupled with the gate drive loop. Thus, too severe resonance in the power loop might affect the gate drive loop which results in unwanted operation of the MOSFET.

Thus, based on the influence of the parasitic inductance and the requirements mentioned at the beginning of this section, for such a motor drive using 4-parallel GaN MOSFETs which is switched with fast speed, it is crucial that:

- the layout of the gate driver and power stage are perfectly designed so that the parallel MOSFETs are strictly switched simultaneously. Apparently, it requires same L_g for the parallel MOSFETs, which requires the distances between the gate driver and the gate of the MOSFETs are same,
- the distance between the gate and the output of the gate driver is small to decrease the L_g to avoid fault turn-on,
- L_{loop} should be as small as possible to satisfy high switching frequency,
- L_{ss1} should be as small as possible to decrease the coupling between the power loop and the gate driver loop,
- the MOSFETs show equal thermal performance to decrease the imbalanced induced by the junction temperature difference.

3.4.5. Power stage layout

Basically, the layout is highly dependent on the layout of the gate driver. However, the layout design of the power stage is more of concern because it is needed for the 3-D modelling and simulation. Therefore, the layout of the power stage is considered firstly without designing the layout of the gate driver in details.

For convenience, the concept used in the design of the layout of the power stage in [29] is referenced. Basically, the requirements on the layout design can be concluded as:

- minimizing the power loop inductance, which requires minimizing the area of the loop formed by the DC decouple capacitors and one phase leg.
- make the distance between the gate of each MOSFET and the terminals of the gate-driver connector equal and small.

In the figure 3.15, the first layout design, which is called type-one layout for convenience, is shown.

The advantages of this design is obvious:

1. Because the terminals V_{DC+}, V_{DC-} and V_{phase} are placed on the left side of the power stage, there is enough space, which is high lighted with the red rectangular, for the gate driver circuit. Thus, the equal distance between the output of the gate driver and each MOSFET is easier to be achieved.

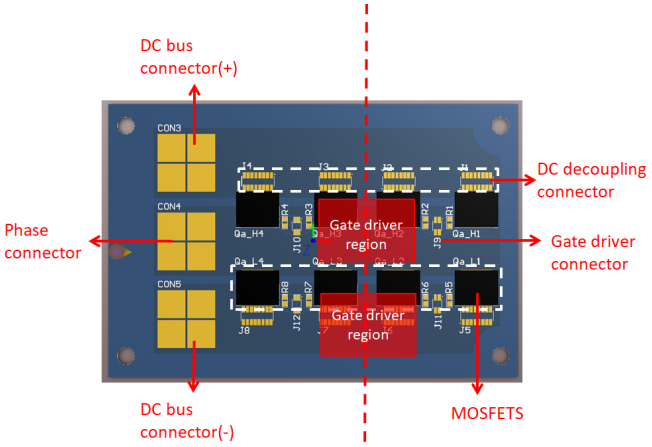


Figure 3.15: Type-one layout of power stage

2. The DC decoupling capacitors are placed just above the power stage and connected with the MOSFET by the connectors J1 - J10. Thus, the area of the loop is nicely controlled to be small which results in a small power loop inductance.

3. The package of the GS66516B uses kelvin source without lead so the coupling between the power loop and gate driver loop is small.

However, the disadvantages of the type-one layout are also obvious.

1. As the terminals are placed on one side, the layout is not perfectly symmetrical. The MOSFETs which are placed closer to the power terminals might share relatively higher current because of the influence of the impedance of the PCB trace.

2. Because of the impedance of the PCB trace, the voltage potential on the source terminals of the parallel MOSFETs is different from each other, which might leads to unequal switching behaviour of the paralleled MOSFETs.

3. It is obvious that among the 4 parallel MOSFETs, the two MOSFETs by the outside have better cooling condition compared with the two by the inside.

Based on these disadvantages, a new layout (type-two) is proposed and shown in the figure 3.16. Apparently, the type-two layout is more symmetrical compared with the type-one. However, the improvement on the even distribution of the current and temperature needs to be evaluated and this part of work is introduced in the next chapter. Apparently, such a layout increases the distance between the gate of the MOSFETs and the output of the gate drivers because the power terminals are placed in the middle occupying the space previously used for the gate driver in the type-one layout.

To place the gate driver closer to the gate and decrease the parasitic gate inductance, the type-three layout is proposed and shown in the figure 3.17. In this layout design, the requirements on symmetry is satisfied and the gate driver loop is also made compact. Besides, the decoupling capacitor is placed on the power stage PCB to further reduce the power loop inductance L_{loop}.

3.4.6. Design of the gate driver circuit

As it is mentioned, the distance between the gate driver and the 4-parallel MOSFET should be same and controlled as small as possible to prevent fault turn-on problem. From increasing the reliability of the design point of view, the design is mainly based on the recommendation from GaN System Inc.. Thus, the design [29] from GaN system, which is a power module using 2-parallel MOSFET in one position, is referenced because it is a good example which fulfills the two requirements. The schematic of the gate driver circuit is shown in the figure 3.18. The sink and source voltage is selected as -3V and 6V respectively. Two connectors J1 and J2 are used to connect the gates of the 4 MOSFETs that are placed on another PCB (power stage).

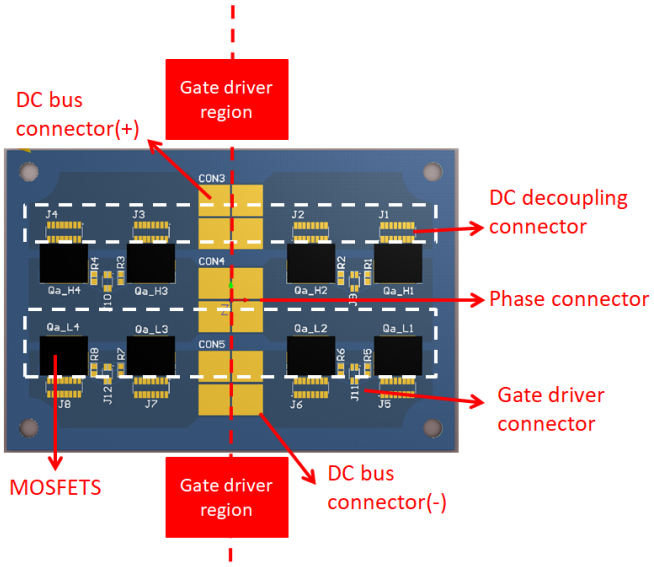


Figure 3.16: Type-two layout of power stage

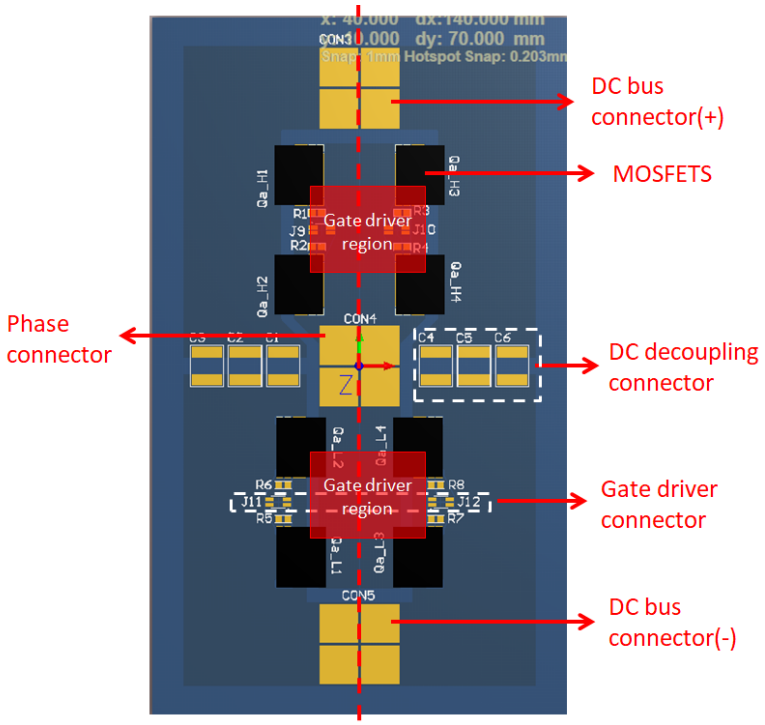


Figure 3.17: Type-three layout of power stage

From the datasheet [42], the power dissipation of the Si8271 used in the application is:

$$P_d = V_{DD1}I_{DD1} + 2I_{DD2}V_{DD2} + fQ_GV_{DD2}\frac{R_p}{R_p + R_{g(on)}} + fQ_GV_{DD2}\frac{R_n}{R_n + R_{g(off)}} + 2fC_{int}V_{DD2}^2 = 126.8mW \tag{3.18}$$

where:

- P_d is the power dissipation (W)
- I_{DD1} is the input-side maximum bias current (10mA)
- I_{DD2} is the driver die maximum bias current (4mA)

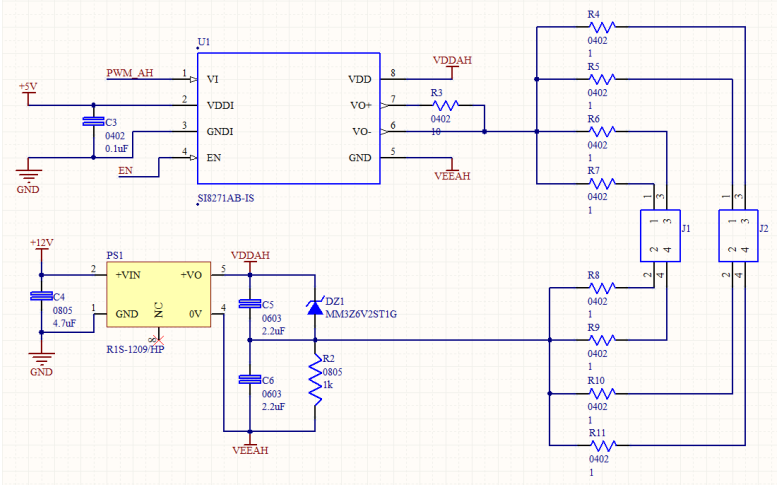


Figure 3.18: Schematic of the gate driver for 4 parallel MOSFET in one position

- C_{int} is the internal parasitic capacitance (370pF)
- V_{DD1} is the input-side V_{DD} supply voltage (5V)
- V_{DD2} is the driver-side supply voltage (9V)
- f is the switching frequency (50kHz)
- Q_G is the gate charge of external MOSFET (4×12.1nC (according to the datasheet [4]))
- $R_{g(on)}$ is the turn-on external gate resistor 12Ω
- $R_{g(off)}$ is the turn-off external gate resistor 2Ω
- R_p is the $R_{DS(on)}$ of the driver pull-up switch: 2.7Ω
- R_n is the $R_{DS(on)}$ of the driver pull-down switch: 1Ω

Based on the calculated power dissipation, the assumed ambient temperature $T_A = 40°C$ and the junction-to-air thermal resistance ($\theta_{ja} = 105K/W$) of Si8271, the maximum junction temperature is

$$T_{jmax} = T_A + P_d\theta_{ja} = 54°C \tag{3.19}$$

The selected power supply R1S-1209/HP is a 12V-to-9V isolated DC/DC converter which can offer maximum 1W power [43]. Therefore, its power capacity is sufficient.

Because the type-three power stage has the most compact layout without sacrificing the symmetry, the gate driver layout is designed based on it. Basically, the design follows the criteria of making the layout as compact as possible. The layout is shown in the figure 3.19.

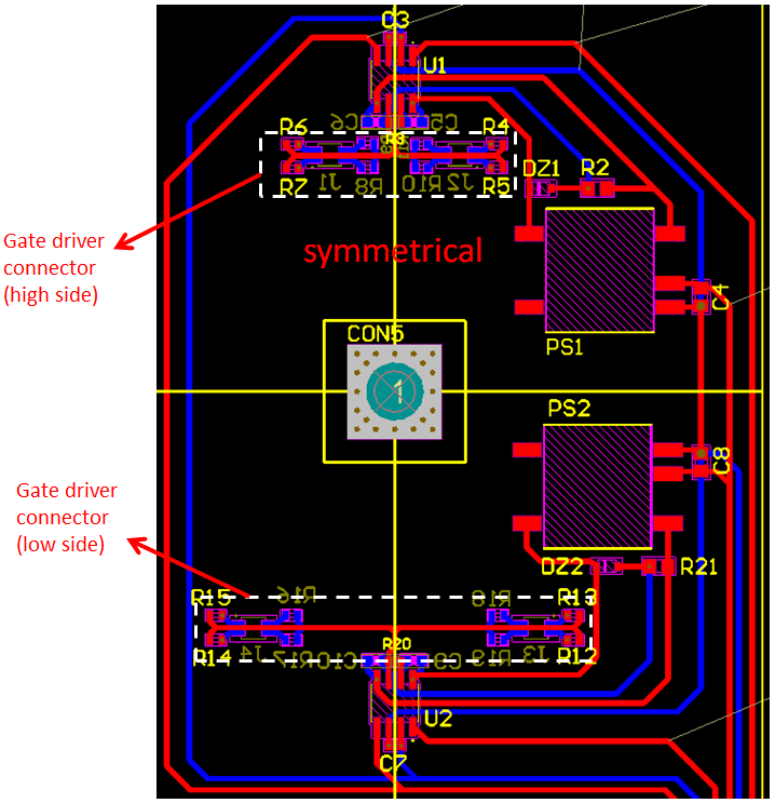


Figure 3.19: Layout of the gate driver for one power stage

3.4.7. Summary

In this chapter, the hardware design of the motor drive is presented. Among all the design, the design of the gate driver circuit and power stage is the most important and challenging part. Among all the content presented, the followings are crucial and need to be emphasized.

- For the design of the motor drive using a high switching frequency, the parasitic inductance in the gate driver and power stage needs to be controlled small to satisfy the high switching speed requirement.
- The balance performance of the parallel MOSFETs in such an application needs to be considered when designing the layout of the gate driver and the power stage. Basically, the required balance consists of the electrical and thermal balance which ensures the parallel MOSFETs are switched simultaneously and have roughly same temperature.
- Built on the last two point, the layout of the gate driver and the power stage should be designed to be compact and symmetrical.

Based on the content presented in this chapter, the 3-D modelling in the next chapter proceeds. With the layout of the three types of power stage, the geometric shape of the three types of power stages can be imported into the 3-D modelling software.

4

3-D modelling & evaluation

As mentioned in the chapter 2, 1-D model has very simple structure which makes it very suitable for a research in general level. However, such a 1-D model is not sufficient on the investigation on the thermal and electromagnetic performance of the motor drive. Therefore, to make up the defects of the 1-D model, 3-D modelling is used to compromise on both the accuracy of the modelling and the time and cost for the development.

Given that the power stage is the part where most of heat is generated, therefore only the 3-D modelling of the power stage are of interest. Basically, the 3-D modelling presented in this chapter are:

- 3-D electromagnetic modelling. The simulation based on it gives the current distribution of the three types power stages.
- 3-D modelling of the computational fluid dynamic (CFD) coupled with the heat transfer. The simulation outputs the heat transfer coefficient on the surface that has the forced convective cooling.
- 3-D stationary heat transfer modelling. The simulation outputs the temperature distribution on the power stage when the car is cruising.
- 3-D time dependent heat transfer modelling. The simulation outputs the temperature distribution on the power stage under the large surge current condition. Besides, it is used for checking the maximum junction temperature of the MOSFETs as well.

4.1. Overview on the 3-D modelling method

In this project, COMSOL Multiphysics® is selected as the simulator for the 3-D simulation. COMSOL Multiphysics® is a very powerful simulator which employs finite element method (FEM) to solve the partial differential equations on different physics. Besides, it shows strong capability on the coupling of multi-physics which is very suitable for the research here where the thermal performance are coupled with the electromagnetic performance and the fluid dynamic.

In the approach of 3-D modelling, the geometry of the object is the first step. After the PCB layout design of the power stage, the geometry of the PCB and the component on the PCB can be imported into COMSOL Multiphysics®. Afterwards, to decrease the difficulties on creating discretisation mesh and the time cost for simulation, the geometry should be modified to fit the studies on the different physics.

Figure 4.1 shows the flow chart of the 3-D modelling method. As it is shown, four different studies are carried out to evaluate the performance of the motor drive from the different perspectives.

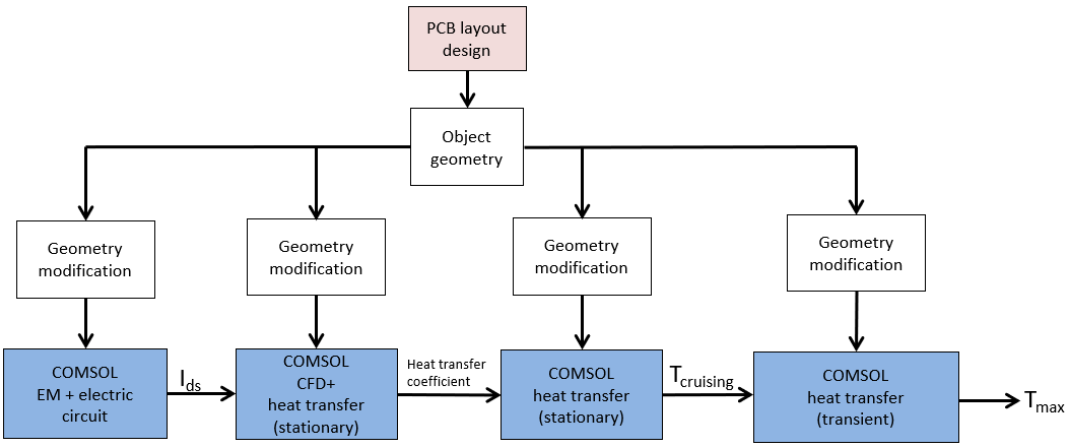


Figure 4.1: Flow chart of the 3-D modelling method

4.2. Geometry construction

The geometry construction introduced here is a general geometry which will be modified for the different physic study in COMSOL.

After the PCB design in Altium Designer, the horizontal geometry of the PCB can be imported into COMSOL by ECAD file. However, this geometry only contains the information of the horizontal layout without the information of the vertical structure of the layers. As mentioned previously, the IMS PCB is selected for this motor drive because of its excellent cooling performance. Therefore, the PCB layers and their thickness is set according the state-of-art of the IMS PCB [44] and the stencil of PCB [45].

Except the PCB geometry, the geometry of the MOSFET is also necessary. However, the inside structure of the GaN MOSFET is rather complicated and there is no open source for the details about it. Thus, only the copper frame is built in COMSOL and it is assumed that the heat source is the copper frame instead of the chip. In the simulation, only the case temperature T_{case} is shown graphically. The estimation of the junction temperature T_j is done by means of 1-D thermal modelling which is offered by the manufacturers. This would not brings too much error as the 1-D thermal model from the manufacturers is a simplification based on their simulation with FEM. According to [46], the result of the simulation using 1-D thermal model is not far away from the one using FEM.

With the known MOSFET geometry and PCB geometry, the MOSFETs can be virtually placed on the PCB. The other components on the power stage are neglected because of their small influence on the thermal and electromagnetic performance. A layer of solder is considered as the junction layer between the bottom of the MOSFET and the top copper layer of the PCB. Normally, there are some air bubbles in the solder which has a huge thermal resistance and has big influence on the thermal performance. Ideally, the geometry of the bubbles should be considered to get a more accurate result. Nevertheless, this kind of small geometry creates so many challenges for COMSOL to make the discretisation mesh. Therefore, the influence of the bubbles are replaced by a thin layer of air to decrease the difficulties on generating mesh.

After the implementation of the geometry of the PCB and the MOSFET. The heatsink can be attached on the bottom side of the PCB through a layer of thermal grease with a thickness of $200\mu m$. Same as the solder layer, the thermal grease layer is a junction layer between the heatsink and the PCB. Therefore, air gap is inevitable. In the implementation of the geometry here, a $10\mu m$ air gap is assumed. Based on the same reason, a $10\mu m$ thick air gap is assumed between the dielectric layer and the aluminum substrate. As for the size of the heatsink, the optimization on it is not included. For simplicity, its length and width is set same as the one used on the old motor drive. As for the thickness of the heatsink, 2cm is decided to get enough thermal capacity. However, the feasibility of such a selection will be evaluated by the simulation on the maximum junction temperature.

As the result, the vertical structure of the implemented geometry in COMSOL is shown in the figure 4.2. In the figure 4.3, an example of the implemented geometry for the type-two power stage is shown. In order to do CFD simulation, the air domain is also constructed. For enough space to do fluid dynamic analysis but not too much computational cost, a 10cm thick air domain is constructed.

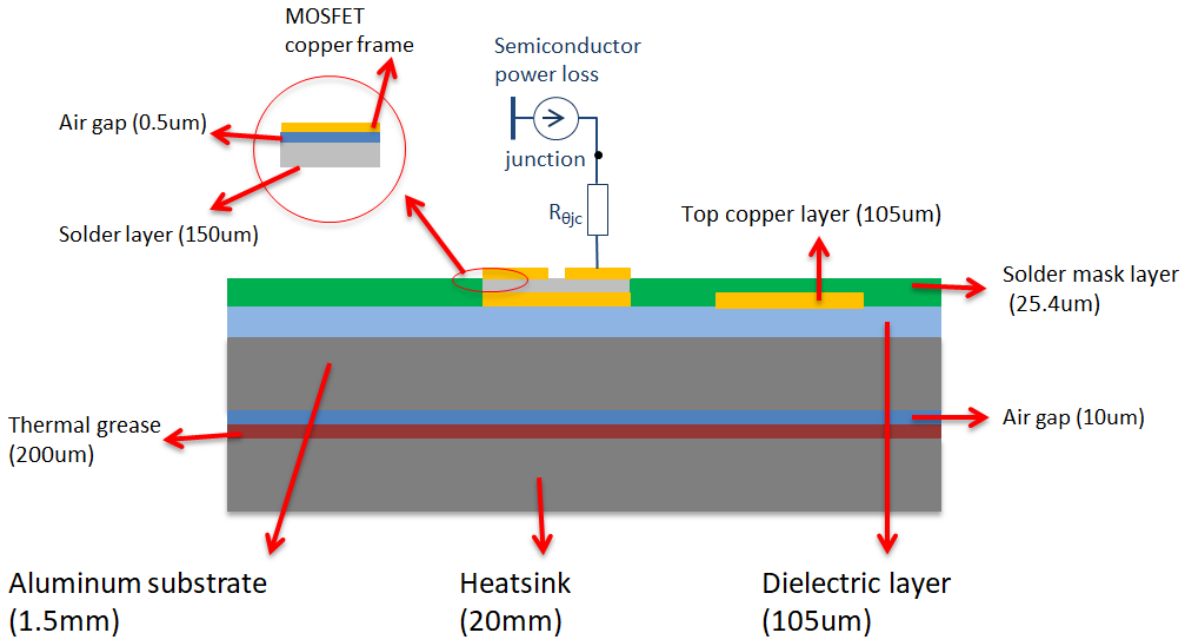


Figure 4.2: Vertical structure of the implemented geometry of power stage for one phase in COMSOL

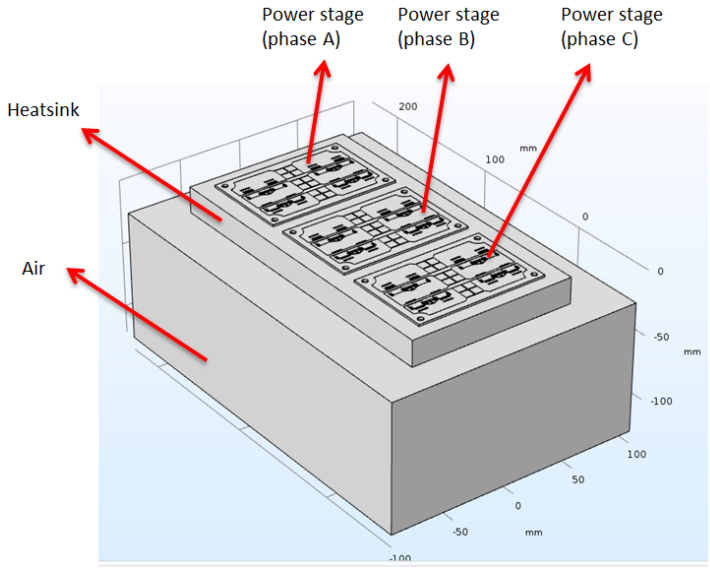


Figure 4.3: Implemented geometry of the power stages with heatsink in COMSOL

As it is shown in the figure 4.2, the thickness of the layers has very wide range from $2\mu m$ to $10cm$. This big difference on size brings a lot of problems. First, the mesh is hard to be constructed and it is even out of the capability of COMSOL to build the mesh within the geometry having objects with so big different size. Besides, according to the COMSOL blog [47], even the mesh is successfully built, there will be big error in the simulation result because of the bad discretisation mesh which stems from the big difference on the size of the objects. Thus, simplification of the geometry based on the different studies on the different physics is crucial.

4.3. Electromagnetic study

Electromagnetic study is carried out to check the imbalanced current distribution due to the layout of the power stage.

The modeling will be introduced first and it is followed by the evaluation on the current distribution in the power stages with three types of layout.

4.3.1. Geometric shape for the electromagnetic study

Based on the geometry implemented for the general use in the section 4.2, some unnecessary parts can be removed in the study here. Actually, the only part of concern is the copper layer where the current flows through. However, to leave enough space to build the electromagnetic field around the copper, the air domain around the circuit is also necessary. Because of the characteristics of IMS PCB on which the copper trace is placed above an aluminum substrate, it can be assumed the bottom side of the copper is electromagnetically isolated. Therefore, only the upper side air domain is is constructed. For sake of enough space for the electromagnetic field, the length, width and height of the air domain is 200mm, 200mm and 1.105mm respectively. The boundary, which is far away from the conductor, of the air domain is assumed to be electromagnetically isolated.

In order to inject current into the conductor, the current input and output port has to be on the electromagnetically isolated boundary. Thus, on the solder pad for the DC+, DC- and phase connectors, a copper conductor with thickness of 1mm is placed to leave the port for the input and output current. Similarly, on the solder pad for the drain and source terminal of MOSFET, a 1mm thick copper conductor is also placed because they are the current input and output terminal of the copper polygon.

The diagram of the geometric shape is shown in the figure 4.4.

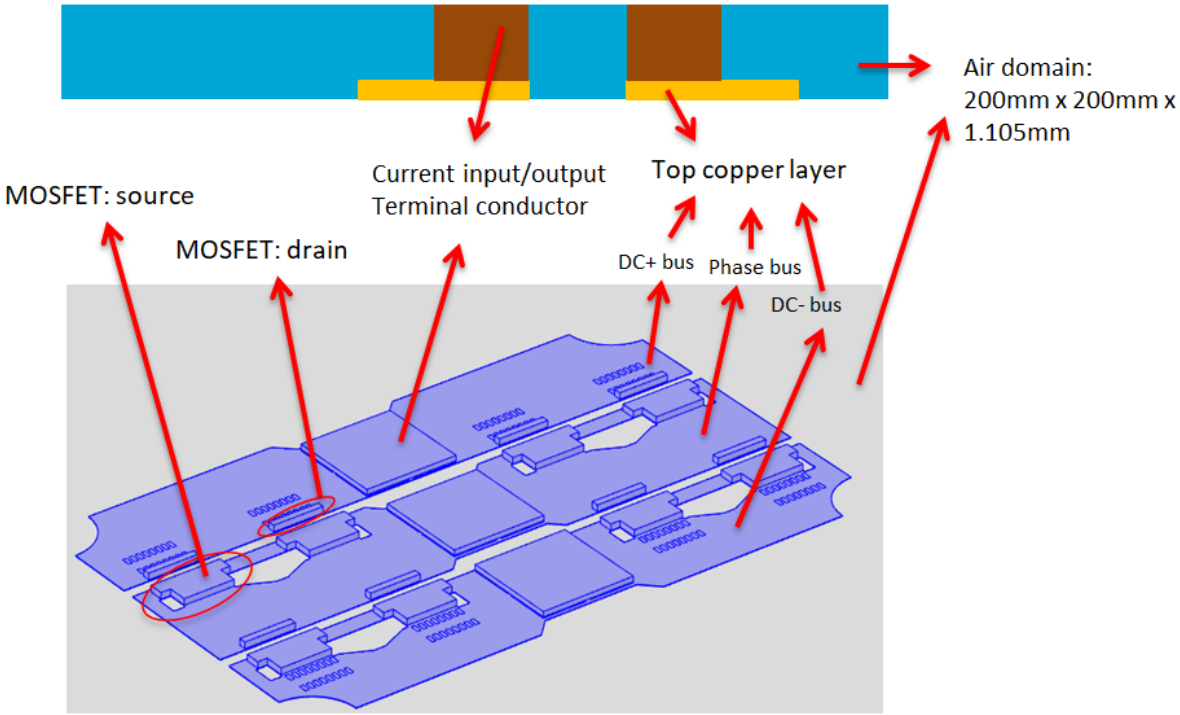


Figure 4.4: Implemented geometry for electromagnetic study

4.3.2. Material properties

For the simulation, the type of the material of the object is necessary to be defined at the beginning. Furthermore, their properties have significant impact on the simulation results.

In the electromagnetic study, only copper and air exist. Their properties that will be used to solve the partial differential equations are listed in the table 4.1

4.3.3. Physics selection for the electromagnetic study

There are two kinds of built-in physics in COMSOL selected for the electromagnetic study. The first one is 'Magnetic and Electric fields (MEF)' which is used to simulate the electromagnetic field inside

Table 4.1: Materials and their properties in electromagnetic study

	Air	Copper
Relative permeability μ_r	1	1
Relative permittivity ϵ_r	1	1
Electrical conductivity σ (S/m)	0	5.998e7

and around the conductor. Once the boundary conditions (magnetic and electric insulation and current input and output on the boundary) are defined, the current distribution in the conductor under the influence of the induced electromagnetic field can be computed by means of FEM.

As the inside material of the semiconductor is very complicated, it is better to exclude the MOSFETs in the filed study. Therefore, the built-in physic 'electrical circuit (CIR)' is used to simplify the semiconductor as a resistor. For simplicity, the MOSFET is simplified as its on resistor $25m\Omega$ when it is switched on and a $1Meg\Omega$ resistor when it is switched off.

In the figure 4.5, the structure of the coupled two simulation is shown, where those highlighted in red exist in the CIR simulation. The labeled nodes are the interfaces between the two simulations. As it is shown, when the upper MOSFETs are turned on, the upper current source has output current and the lower one does not have. In CIR simulation, there is a voltage potential applied at the labeled nodes. The value of the voltage is determined by the output current at the terminal in MEF simulation. In this way, the two kinds of simulations are coupled.

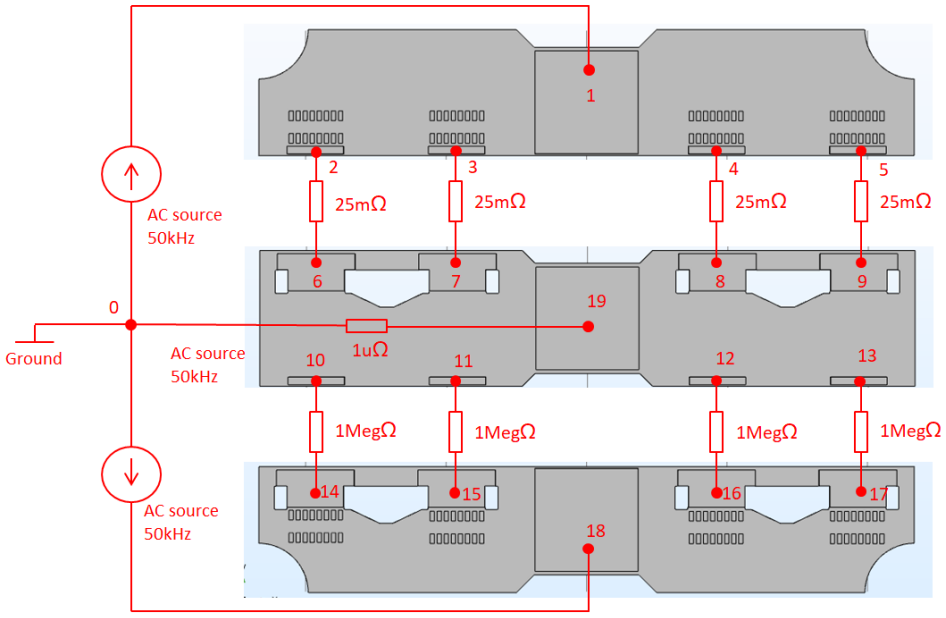


Figure 4.5: The coupled MEF and CIR simulation when the upper MOSFETs are switched on

4.3.4. Current distribution of the two types of layout

After implementing the model of the power stages with the three types of layout, the current distribution in the conductor is simulated. A 20A AC current source with 50kHz, which is the switching frequency, is set as the current source whose current flows through the low side MOSFETs in the simulation.

Basically, what is of concern is the distribution of the current in the conductor and the current sharing ratio between the 4 parallel MOSFETs. With a fixed frequency, the impedance between the nodes (i.e. node 1 and node 2) in the figure 4.5 has a constant value which is independent of the amplitude of the input current. Therefore, the ratio of the current through each MOSFET to the total input current is of concern instead of the current value itself. The amplitude of the output current of the current source does not necessarily need to be 20A.

In the figure 4.6, the current distribution in the type-one power stage is shown. Similarly, the results

belonging to the type-two power stage and the type-three power stage are shown in the figure 4.7 and the figure 4.8. The current through every MOSFET in the three types of power stages is compared in the table 4.2.

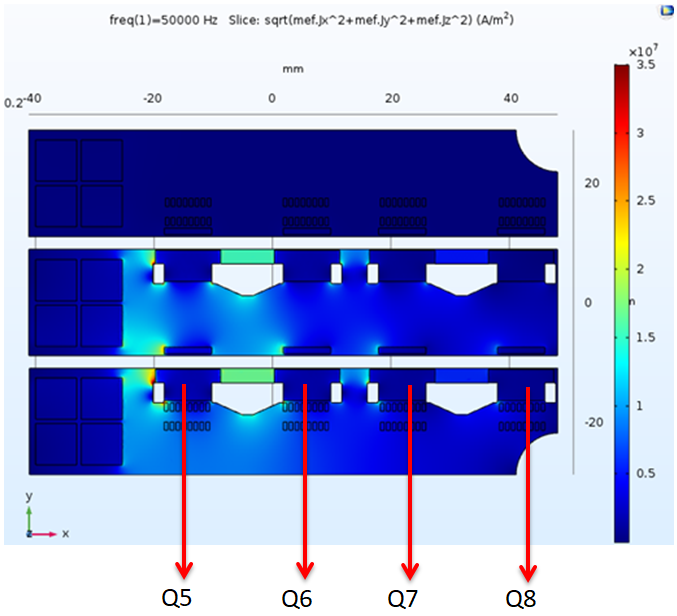


Figure 4.6: Current distribution in the type-one power stage when phase current is 20A

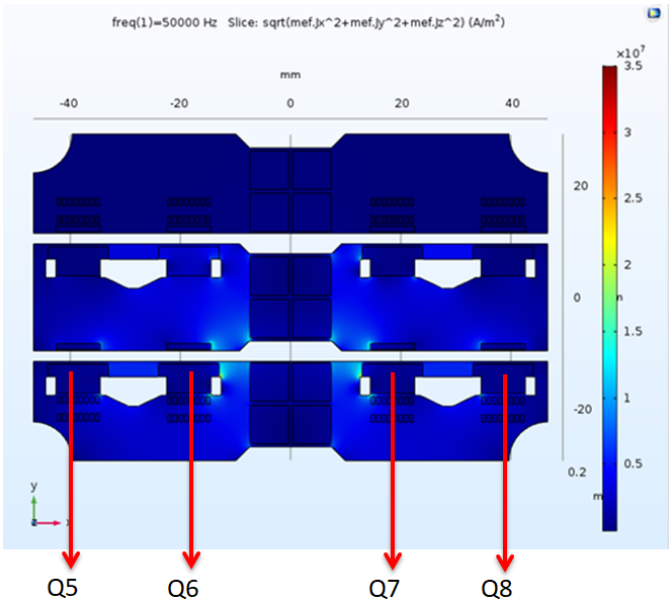


Figure 4.7: Current distribution in the type-two power stage when phase current is 20A

Apparently, the type-two and type-three power stage have a better balance on the current sharing which ensures a more evenly distributed temperature on the power stage. Besides, a more evenly distributed current decreases the difference on voltage potential between the source terminals of the parallel MOSFETs, which decreases the possibility of the asynchronous switching of the parallel MOSFETs. The voltage potential of the source terminals of the parallel MOSFETs in the three types of layout are compared in the table 4.3.

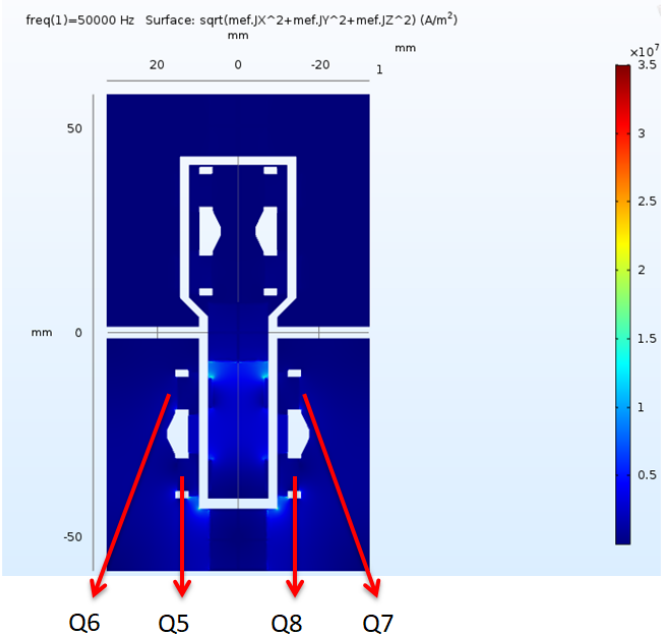


Figure 4.8: Current distribution in the type-three power stage when phase current is 20A

Table 4.2: Current sharing of the 4 parallel MOSFETs in the three types of power stages

	Current (A)			
	Q5	Q6	Q7	Q8
Type 1	5.22	5.01	4.92	4.85
Type 2	4.97	5.03	5.03	4.97
Type 3	5.02	4.98	4.98	5.02

Table 4.3: Voltage potential of the source terminals of the 4 parallel MOSFETs in the three types of power stage

	Source terminal voltage potential (mV)			
	Q5	Q6	Q7	Q8
Type 1	133.04	130.04	128.90	127.88
Type 2	126.15	127.16	127.16	126.14
Type 3	126.96	127.8	127.8	126.96

4.4. Heat transfer and CFD study

In order to evaluate the thermal performance of the motor drive, heat transfer study is necessary. However, as the heat transfer is coupled with the fluid dynamics, a model that couples the heat transfer and CFD is constructed. To reduce computational cost, the simulation that couples the CFD with heat transfer is done only for type-two power stage. The resultant heat transfer coefficient will be used in the heat transfer study for the other types of power stages.

4.4.1. Fundamentals of heat transfer

In overview, there are three kinds of mechanisms, conductivity, convection and radiation, happening in heat transfer [2]. The first two are actually based on the same mechanism that heat as a kind of energy is transferred by molecular motion. The difference between the two is that the first one happens inside a stationary medium such as solid whereas the second one happens at the boundary between a stationary medium and a fluid medium such as water and gas.

Because of the difference, Fourier's law and Newton's law shown in the equation 4.1 and 4.2 are used to describe the heat transfer rate due to conduction and convection respectively.

$$q = -kA\frac{\partial T}{\partial x} \tag{4.1}$$

$$q_c = hA(T_s - T_\infty) \tag{4.2}$$

In the equation 4.1, k is defined as thermal conductivity (in W/mK) and the heat flux q through a surface with an area A along the axis-x can be calculated by k, A and the temperature gradient along axis-x. In the equation 4.2, h is defined as heat transfer coefficient (in W/m^2K). The convective heat flux q_c through a surface with an area A can be calculated by the A, h and the temperature difference between the surface and the ambient at an infinite distance.

As for the last mechanism radiation, it is different from the last two whose happening is based on molecular motion. The radiation transfer energy through electromagnetic wave. Any object has a temperature higher than absolute zero will have radiation heat loss. Heat flux resulting from radiation can be calculated by the equation 4.3 which is called Stefan-Boltzmann law of thermal radiation, where σ is Stefan-Boltzmann constant, A is the area of the surface of interest and T is the temperature of the surface. Based on the equation 4.3, the heat flux emitted from a heating object to the ambient is given in the equation 4.4.

$$q_r = \sigma A T^4 \tag{4.3}$$

$$q_r = \sigma A(T_s^4 - T_\infty^4) \tag{4.4}$$

4.4.2. Motivation of CFD

Apparently, the convective heat transfer is dependent on the cooling condition of the power stage that uses air cooling. As mentioned previously, to increase the reliability of the motor drive, the cooling of the motor drive is designed to be natural air cooling without fans. Besides, to make use of the wind when the racer is running, the bottom side of the heatsink contacts the air outside the car directly while the other sides are inside the car. The placement of the motor drive is shown in the figure 4.9. Thus, it is assumed that the surface of the motor drive inside the car has a natural cooling condition while the bottom side has a forced cooling condition. These cooling condition has crucial impact on the convective heat transfer.

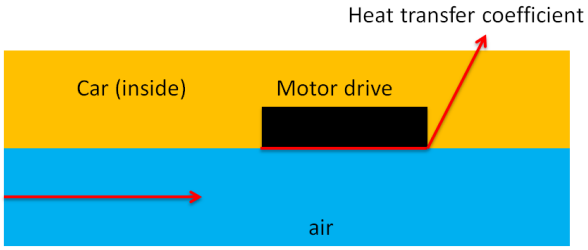


Figure 4.9: Installment position of the motor drive

For the nature cooling inside the car, an imperial value $7W/m^2K$ of the heat transfer coefficient h is enough to estimate the convective heat transfer on the surface inside. However, the heat transfer coefficient of the surface outside the car is highly dependent on the properties especially the speed of the air. Thus, CFD is used to precisely evaluate the heat transfer coefficient h on the surface outside of the car with different wind speed outside the car.

Based on this reason, in the CFD simulation, only type-two power stage is used to evaluate the coefficient h as the heatsink is not changed for the three kinds of power stages with the different layout. The resultant h will be used for the stationary and time dependent heat transfer study.

4.4.3. Fundamentals of fluid dynamics

To select the proper physics study for the CFD model in COMSOL, it is necessary to clarify the relevant basics of fluid dynamics.

Basically, laminar flow and turbulent flow are two kinds of flow, which is determined by the Reynolds number. The difference of the two types of flow is depicted in the figure 4.10. From the velocity of the fluid, it is obvious that the turbulent flow has turbulent eddies while the laminar flow does not have.

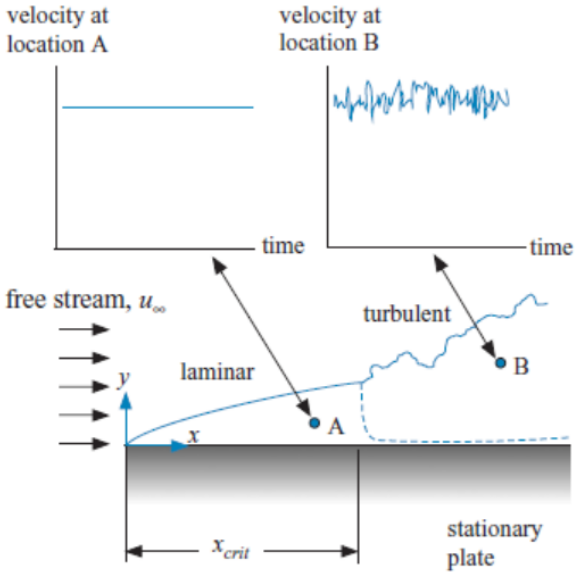


Figure 4.10: Difference between the laminar flow and turbulent flow[2]

The Reynolds number is defined as

$$Re = \frac{uL\rho}{\mu} \tag{4.5}$$

where u is the velocity of the flow at the spot of concern, L is the distance between the spot of interest and the leading edge of the plate, μ is the viscosity of the fluid and ρ is the density of the fluid.

The key parameter, heat transfer coefficient h, varies in terms of the characteristics of the fluid. In [2], the analytic explanation on h is given.

As it is shown in the figure 4.11 [2], the temperature distribution near a plate under the influence of a fluid flow is depicted. The thickness δ_t is defined as thermal boundary layer out of which the fluid temperature is not influenced by the heating surface anymore.

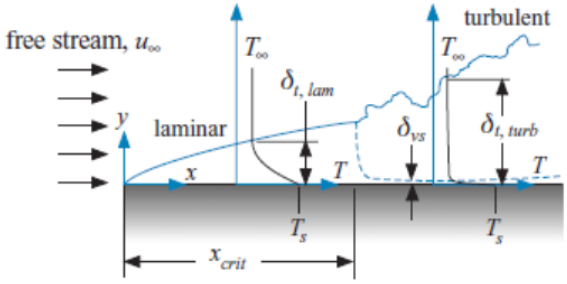


Figure 4.11: Temperature distribution near a plate under the influence of a fluid flow [2]

For the laminar flow, the h can be approximated as

$$h = \frac{k}{\delta_{t,lam}} = \frac{k}{2\sqrt{\alpha t}} \tag{4.6}$$

where k is the thermal conductivity of the fluid material and α is the thermal diffusivity of the material.

However, the approximation on the coefficient h under the influence of the turbulent flow is different. When the laminar flow changes to the turbulent flow, there are two regions near the plate. A thin layer of fluid without turbulent eddies is called viscosity sub-layer and exists near the plate. Above the viscosity sublayer, the fluid starts to have turbulent eddies. As the thermal resistance of the viscosity sublayer is much bigger than the turbulent region [2], the coefficient h is approximated as

$$h = \frac{k}{\delta_{t,vs}} \tag{4.7}$$

where the $\delta_{t,vs}$ is the thickness of the viscosity sublayer.

4.4.4. Geometric shape for the modelling of the CFD coupled with heat transfer

To decrease the computational cost and the difficulties on generating discretisation mesh, the geometric shape used for general use needs to be simplified. As it is shown in the figure 4.12, the big geometric shape is partitioned and the power stages of the three phases are separated.

Because the three phase current is almost same and the heat transfer in the vertical direction is dominant, it can be assumed that the partition surface are thermal insulation boundary and there is a symmetrical behaviour of the fluid at the partition boundary in the air domain.

Built on these assumptions, the domains which are high-lighten in yellow by the two sides are deleted. Only the heat transfer in the power stage in the middle is studied together with the CFD simulation on the air domain just below the heatsink.

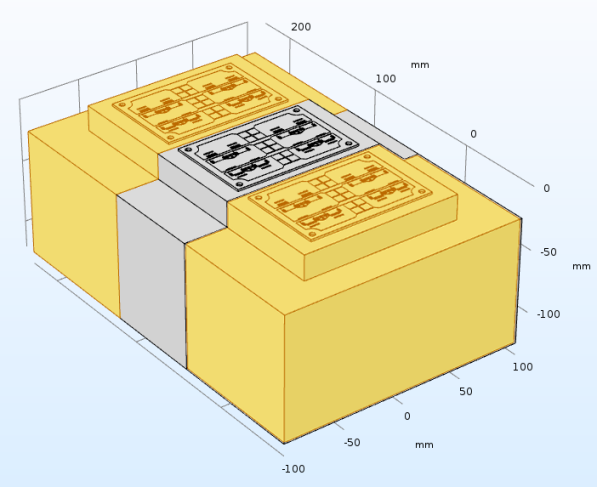


Figure 4.12: Deleted domains (yellow) for the CFD study coupled with heat transfer study

Except from the simplification of the geometric shape by partition, the layers with small thickness are also removed from the geometry. As it is mentioned previously, the big difference on the size of the geometric shape creates many challenges for the mesh construction. Therefore, the thickness of the thin layers on the PCB is ignored. To model heat transfer inside the thin structures, the dedicate function 'thin layer' in the heat transfer physics in COMSOL is used.

4.4.5. Mesh generation considerations

The constructed discretisation mesh is shown in the figure 4.13. Tetrahedral is used for the solid domain where as hexahedral is better for the fluid domain. From the basics of the fluid dynamics, it is known that the behaviour of the fluid flow near the wall is more complicated compared with the fluid flow in the free region. Thus, at the boundary surface between the solid and the fluid, the mesh cells with smaller size are created.

4.4.6. Numerical modelling of the fluid domain

To evaluate the heat transfer coefficient h, a model that couples the heat transfer and CFD is established.

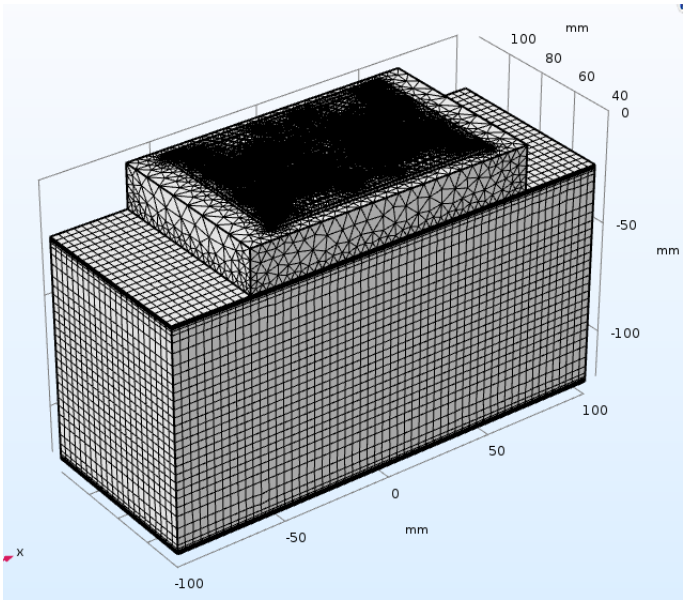


Figure 4.13: Generated mesh for the stationary heat transfer and CFD study

For the fluid dynamic analysis, there are many choices on the physical model settings in COMSOL. The settings are selected according to the goals of the research. With a compromise between the computational cost and accuracy of the simulation results, the fluid dynamic analysis is carried out based on the Reynolds Averaged Navier-Stokes Equations (RANS) assuming the fluid of the flow is weakly compressible. The weakly compressible flow setting makes the density of the fluid pressure dependent but the density will be evaluated at only the reference absolute pressure [48].

As for the turbulence model, the $k-\epsilon$ turbulence model is selected because of its good convergence rate and low memory requirements [49]. In the $k-\epsilon$ turbulence model, wall function which neglects the fluid performance inside the viscosity sublayer and the buffer region between the viscosity sublayer and the turbulent region is used. An analytically computed speed of the flow at the boundary of the wall is used to simulate the influence brought by the ignored two regions [49].

Last but not least, the turbulence model parameters determines the characteristics of the fluid and has crucial impact on the CFD simulation results. In this modelling, the experimental data from [50] is used. In the figure 4.14, the turbulence model parameters used in the modelling are shown.

Turbulence Model Parameters

$C_{\epsilon 1}$	1.44	1
$C_{\epsilon 2}$	1.92	1
C_{μ}	0.09	1
σ_k	0.9	1
σ_{ϵ}	1.3	1
κ_v	0.41	1
B	5.2	1

Figure 4.14: Turbulence model parameters used in the CFD

The boundary conditions are:

- The inlet and outlet boundary of the flow are shown in the figure 4.15.
- The wall boundary condition is shown in the figure 4.16
- The symmetrical boundary condition is shown in the figure 4.17

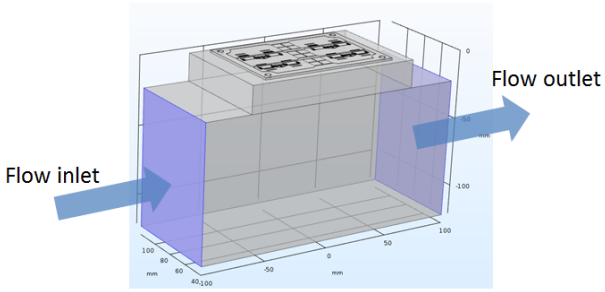


Figure 4.15: Inlet and outlet boundary (blue) of the flow in the CFD study

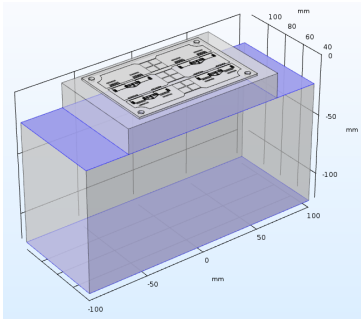


Figure 4.16: Wall boundary condition (blue) in the CFD study

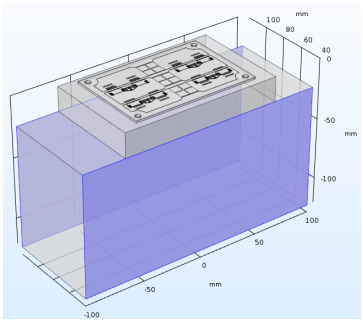


Figure 4.17: Symmetrical boundary condition (blue) in the CFD study

4.4.7. Numerical modeling of the heat transfer

To evaluate the coefficient h with a flow having constant speed, the stationary study is selected. The ambient temperature is set as 40 $^{\circ}C$. After these general settings, the first step is defining the heat source. Obviously, the main heat source is the eight MOSFETs and the PCB trace.

- Power loss of the MOSFETs:

  As mentioned in the chapter 2, a 3-D look-up table of the inverter loss $P_{loss}(i_{phase(amp)}, T_j, v_{dc})$ is implemented. As the switching loss is not terribly influenced by the v_{dc} and the DC bus voltage does not change too much, it can be assumed that the DC voltage bus stays constantly at 150V. Thus, the 3-D look-up table reduces to 2-D look-up table $P_{loss}(i_{phase(amp)}, T_j)$. Based on the inverter loss look-up table, the power loss look-up table of single MOSFET can be derived and it is shown in in the figure 4.18.

  The high side and the low side MOSFET is assumed to have the same power loss because their same behaviour in one fundamental wave period. The power loss on certain MOSFET is

$$P = \frac{1}{2} P_{loss}(i_{phase(amp)} * k, T_j) \tag{4.8}$$

  where k is the ratio between the amplitude of the current through the MOSFET and the amplitude

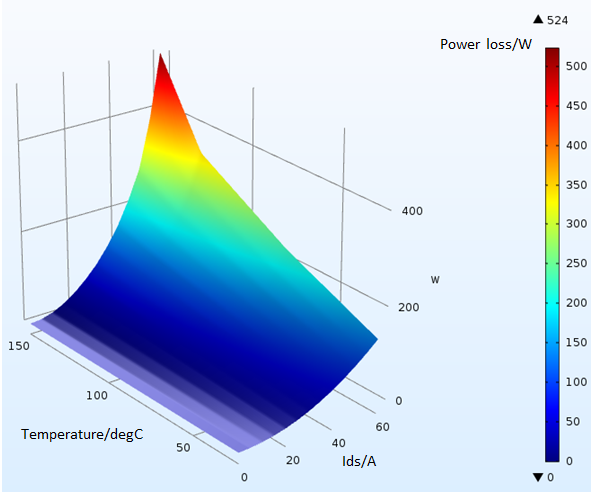


Figure 4.18: The 2-D look-up table of the power loss of single MOSFET

of the phase current. The ratio k is derived from the results of the electromagnetic study in the section 4.3.

The power loss of the MOSFET should be updated in terms of the change of the T_j and $i_{phase(amp)}$. The estimation method of the T_j using 1-D thermal model is introduced in the section 4.2 and is given

$$T_j = T_{case} + R_{jc} * P_{loss}(i_{phase(amp)} * k, T_{case}) \tag{4.9}$$

where R_{jc} is the junction to case thermal resistance. As for the current $i_{phase(amp)}$, it is assumed to be constantly 20A because a stationary study is used.

- Power loss of the PCB trace:

  The power loss of the PCB trace is much less than the loss of the MOSFET. Based on the results of the electromagnetic simulation, the resistance of the PCB trace can be estimated and it is less than $1m\Omega$. Thus, the power loss of the PCB trace is neglected.

The next step is setting the boundary condition. In total, there are five kinds of boundary conditions.

- The thermal insulation boundary condition is presented in the figure 4.19.

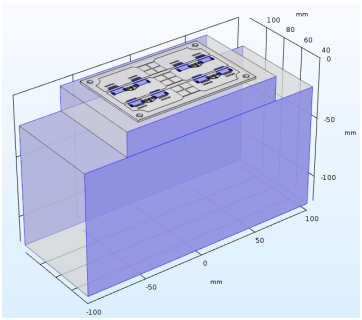


Figure 4.19: The thermal insulation boundary (blue)

- The natural cooling boundary ($h = 7W/(m^2K)$) condition is shown in the figure 4.20.
- The radiation boundary condition is shown in the figure 4.20.
- The temperature boundary condition for the inlet flow and the outflow boundary condition are shown in the figure 4.22

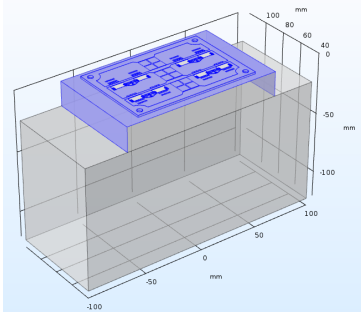


Figure 4.20: The natural cooling boundary (blue)

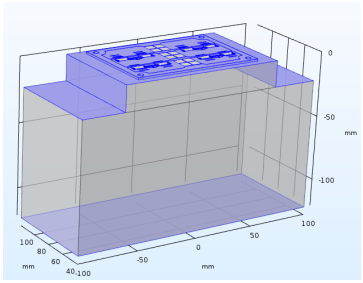


Figure 4.21: The radiation boundary (blue)

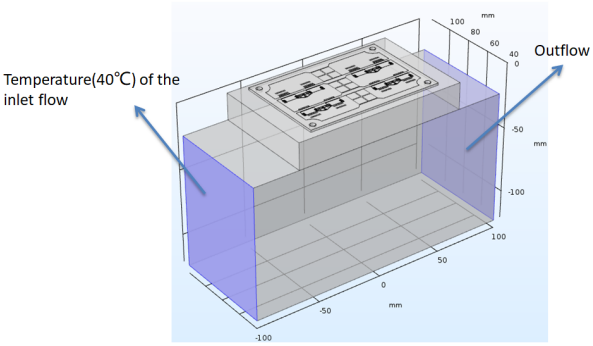


Figure 4.22: The temperature boundary condition for the inlet flow and the outflow boundary condition

- The forced cooling boundary condition does not need to be set, because the heat transfer coefficient at the interface between the bottom side of the heatsink and the fluid is determined by the coupled CFD study.

Besides, as mentioned previously, the function 'thin layer' is used in the heat transfer modelling. In the function node 'thin layer', it is possible to choose the type of the layer. The type 'thermally thick approximation' is used for vertical heat transfer analysis, the type 'thermally thin approximation' is used for horizontal heat transfer analysis and type 'general' is used for the heat transfer in the two directions but requires more memory for the computation. In the modelling here, the 'general' type is selected because the heat transfer in both direction is of interest. The multi-layer function is enabled to set the thickness of the different layers shown in the figure 4.2.

4.4.8. Material properties

The material properties has big influence on the simulation result. The parameter settings of the material are normally based on literature. However, COMSOL offers big convenience because it has many built-in materials. Most of the material parameter settings are based on the built-in materials in COMSOL. However, for the material of the dielectric layer in the IMS PCB, its properties are determined from the literature [44]. Material properties related to the heat transfer study are listed in the table

4.4.

Table 4.4: Materials properties for the heat transfer study

	Heat capacity at constant pressure $C_p(J/(kg \cdot K))$	Thermal conductivity $k(W/(mK))$	Density $\rho(kg/m^3)$	Surface emissivity
Dielectric layer material	440	2.2	7500	-
Copper	385	400	8960	-
Aluminum	900	238	2700	0.9
Solder	150	50	9000	-
Solder mask	1369	1	1900	0.7
Thermal grease	1200	3	2600	-
Air	Cp(T)	k(T)	$\rho(pA)$	0.85

4.4.9. CFD simulation results

The wind speed distribution result of the CFD simulation is shown in the figure 4.23. The flow speed at the inlet boundary is 22m/s. As it is shown, the speed of the flow decreases near the wall, which complies with the theoretical analysis.

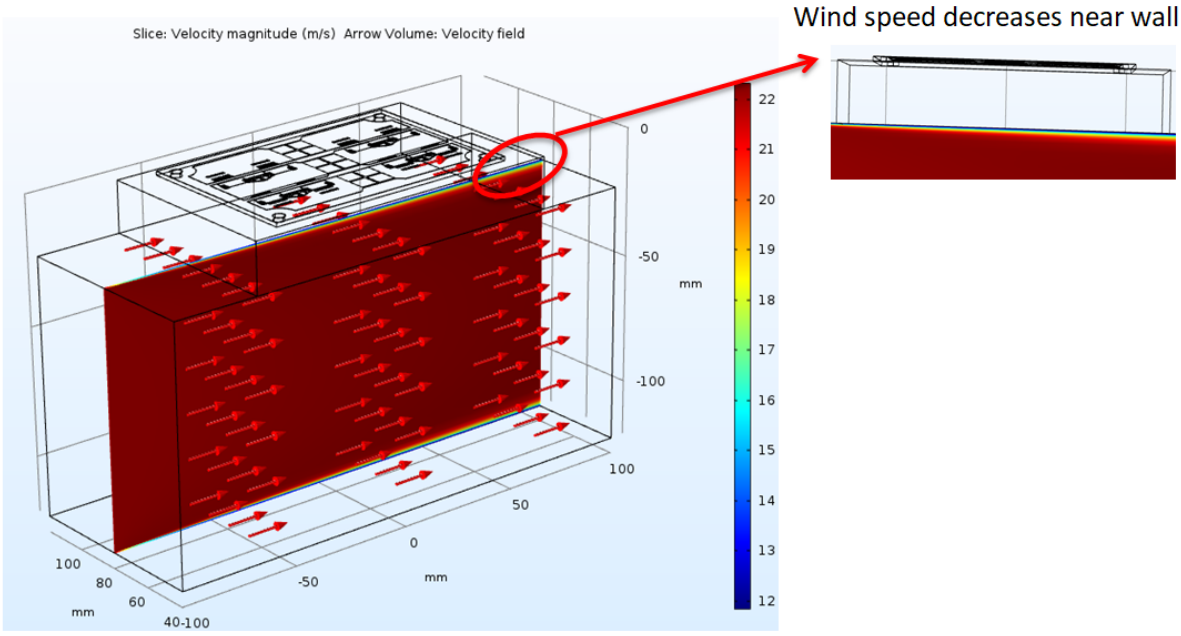


Figure 4.23: Resultant wind speed distribution in the CFD simulation

To evaluate the heat transfer coefficient in the different flow speed condition, the simulations coupling CFD and heat transfer are done in the different flow speed condition. The heat transfer coefficient can be calculated from

$$h = \frac{q_{convective}}{A(T_S - T_\infty)} \tag{4.10}$$

where $q_{convective}$ is the convective heat flux through the boundary of interest, A is the area of the boundary surface, T_s is the averaged temperature of the boundary surface and T_∞ is the temperature of the ambient at an infinite distance. The results of the estimated heat transfer coefficient are listed in the table 4.5.

Table 4.5: Estimated heat transfer coefficient in the different flow speed condition

V (m/s)	0	6	9	12	15	18	22	26	30
$q_{convective}(W)$	-	4.51	4.52	4.45	4.37	4.27	4.16	4.05	3.96
$T_s(^\circ C)$	-	52.44	49.73	48.11	47.02	46.23	45.46	44.89	44.46
Area(m^2)	0.0104								
h $(W/(m^2K))$	7	35	44.66	52.79	59.8	65.95	73.2	79.6	85.42

4.5. Stationary heat transfer study

The stationary heat transfer study is used to estimate the temperature distribution on the power stage when the car is running at the cruising speed. Based the estimated heat transfer coefficient in the CFD simulation, the air domain is excluded from the model for the stationary heat transfer study.

4.5.1. Modelling method

Basically, the modelling is same as the heat transfer modelling introduced in the subsection 4.4.7. The only difference is that the forced cooling boundary condition is manually set. Based on the assumption that the wind speed is zero and the fact that the cruising speed of the car is about $80km/h$, the heat transfer coefficient on the bottom side of the heatsink is assumed to be $73.2W/(m^2K)$.

The amplitude of the phase current is still assumed to be 20A because it is roughly the amplitude of the phase current when the car is cruising.

4.5.2. Simulation results of the stationary heat transfer study

The resultant temperature distribution on the type-one, type-two and type-three power stage are shown in the figure 4.24, figure 4.25 and figure 4.26 respectively.

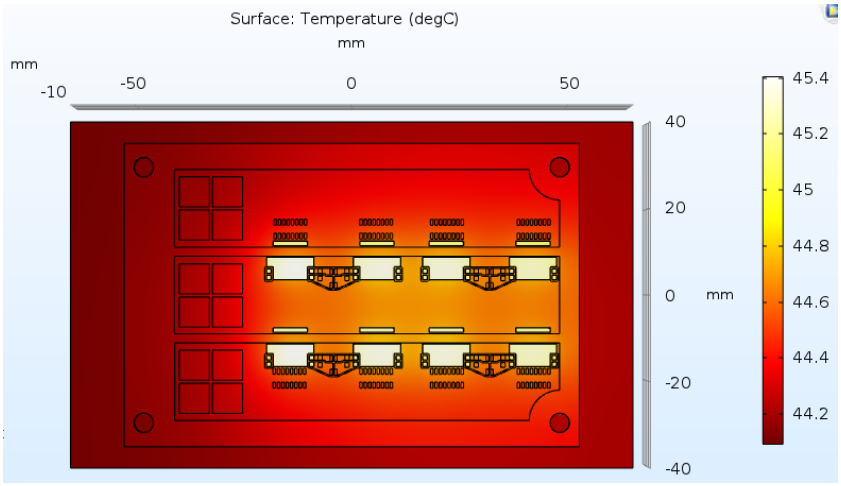


Figure 4.24: Resultant temperature distribution on the motor drive with type-one power stage (overview)

Based on these results, a statistics on the temperature of the 4 parallel high-side MOSFETs are listed in the table 4.6.

Table 4.6: Statistics on the temperature of the 4 parallel high-side MOSFETs

	Temperature$(^\circ C)$			
	Q1	Q2	Q3	Q4
Type 1	45.37	45.34	45.33	45.28
Type 2	44.95	44.94	44.94	44.95
Type 3	45.02	45.07	45.07	45.02

Because the current i_{phase} is low when the car is cruising, the power losses on the MOSFETs are not high, which leads to a low temperature of the MOSFETs. Thus, the imbalanced temperature

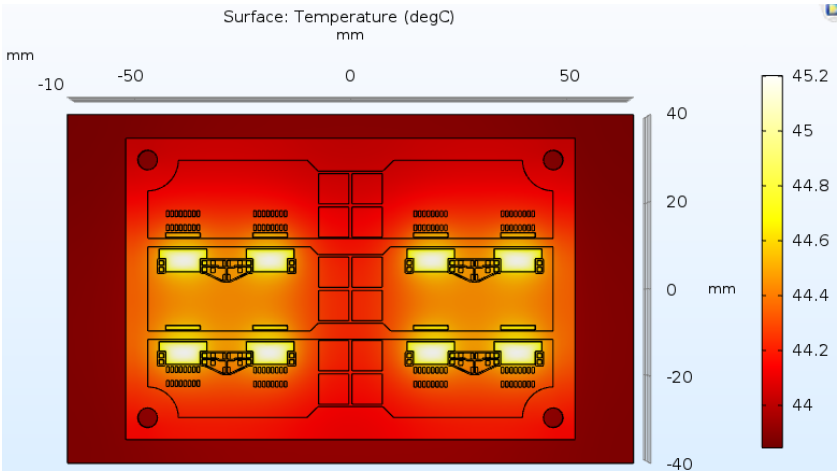


Figure 4.25: Resultant temperature distribution on the type-two power stage (overview)

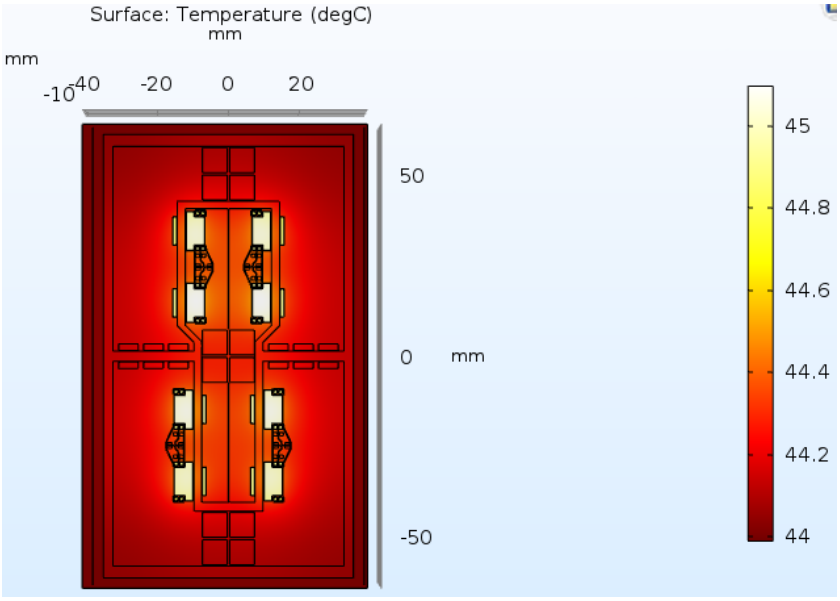


Figure 4.26: Resultant temperature distribution on the type-three power stage (overview)

distribution is not obvious. However, from the small difference on the temperature of the parallel MOSFETs, it can be found that the type-two and type-three power stage has a more evenly distributed temperature. Besides, because the MOSFETs on the type-two power stage are more scattered, the MOSFET temperature is averagely lower and this advantage is more obvious in the time dependent heat transfer study

4.6. Time dependent heat transfer study

The time dependent heat transfer simulation is used to estimate the maximum junction temperature under the large surge current condition occurring in the load profile. Based the estimated heat transfer coefficient in the CFD simulation, the air domain is excluded from the model for the time dependent heat transfer study.

4.6.1. Modelling method

Basically, the modelling is same as the heat transfer modelling introduced in the subsection 4.4.7. However, a time dependent study is applied here instead of the stationary study. Therefore, the inputs that are assumed to be constant in the stationary heat transfer study need to be changed into a

function of time. The inputs and output of the model used for the time dependent heat transfer study are shown in the figure 4.27 in which the $T_{cruising}$ is assumed to be the initial temperature at $t = 0s$, $I_{phase(amp)}(t)$ is used to estimate the power loss on the MOSFETs and $speed(t)$ is used to estimate the heat transfer coefficient on the bottom surface of the heatsink. The wind speed is assumed to be zero, thus the heat transfer coefficient is only related to the speed of the car. A look-up table of the coefficient h(V_{flow}) shown in the figure 4.28 is implemented based on the data in table 4.5.

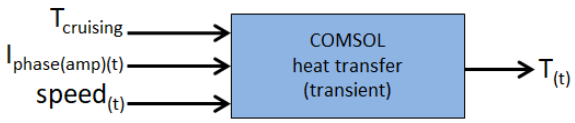


Figure 4.27: Inputs and output of the model used for the time dependent heat transfer study

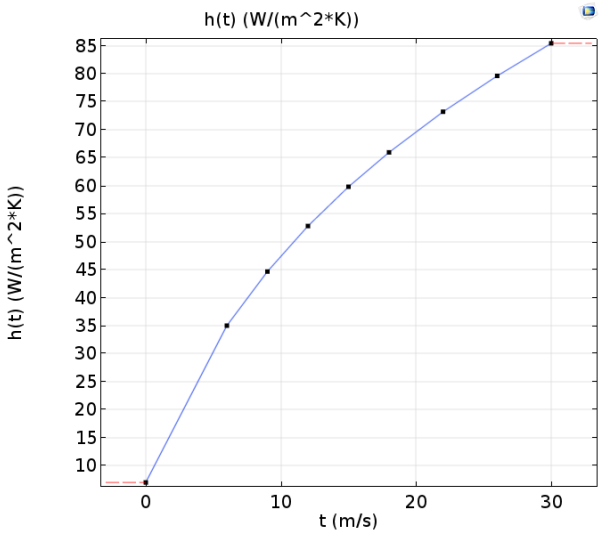


Figure 4.28: Look-up table of the heat transfer coefficient

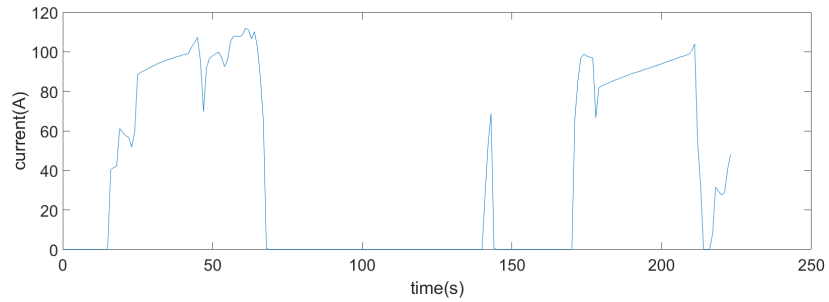
The profile of the $I_{phase(amp)}(t)$ and $speed(t)$ can be acquired from the load profile. In the chapter 2, a same evaluation is done with 1-D thermal model. The load profile used in that evaluation can also be used here. However, the 600-second load profile shown in the figure 2.26b is still too long for the 3-D simulation. To reduce the computational cost, the 223-second load profile between 277s and 500s is used, because from the result of the 1-D model evaluation, the maximum junction temperature occurs in between. The load profile used for the time dependent heat transfer study is shown in the figure 4.29.

4.6.2. Simulation results of the time dependent heat transfer study

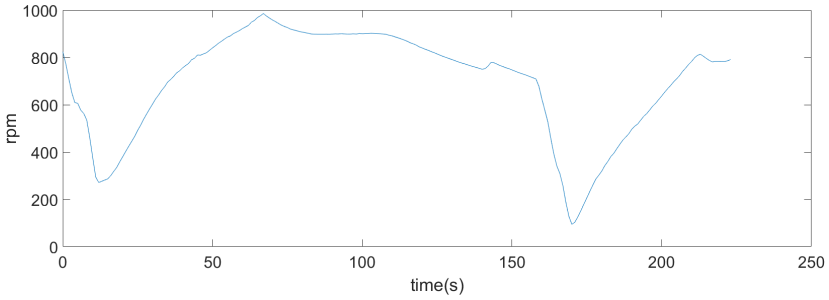
In the figure 4.30, the junction temperature of the 4 parallel MOSFETs on the type-one power stage in the 233-second simulation is shown . Similarly, the figure 4.31 and the figure 4.32 show the temperature of the MOSFET on the type-two and the type-three power stage respectively. Apparently, in the simulation, the maximum junction temperature of the MOSFET on all the three types of power stage does not exceed $150°C$.

However, there some difference on their performance. It can be concluded:

- The type-two power stage has the lowest temperature. The layout makes the MOSFETs more scattered and leaves more space to spread the heat.
- The type-two and type-three power stage have a more evenly distributed temperature.
- In the type-one and type-three, it is obvious the MOSFET by the outside has a relative lower temperature. Same conclusion should also apply to the type-two power stage but it is less



(a) $I_{phase}(amplitude)$



(b) speed

Figure 4.29: Load profile used for the time dependent heat transfer study

obvious because the temperature of the MOSFET is lower compared with the other two types of power stages.

Nevertheless, a big reason that induces the unequal temperature of the parallel MOSFETs is the imbalanced current distribution. In reality, the current distribution is more balanced because the MOSFET has the self-balance characteristic. It means, when the temperature of certain MOSFET rises, its conducting resistance rises as well. As the result, less current flow through it and the its temperature falls. Therefore, the temperature difference induced by the imbalanced current sharing is decreased with such a mechanism. However, it is not considered in the simulation.

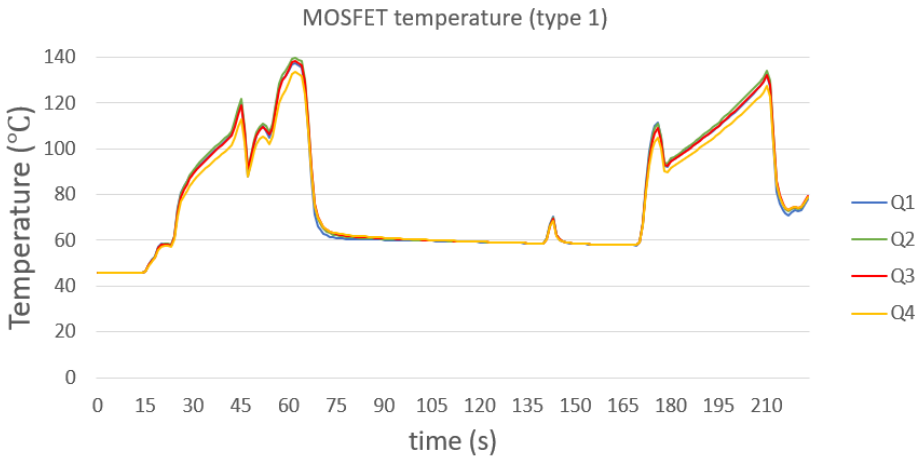


Figure 4.30: MOSFET temperature of the type-one power stage

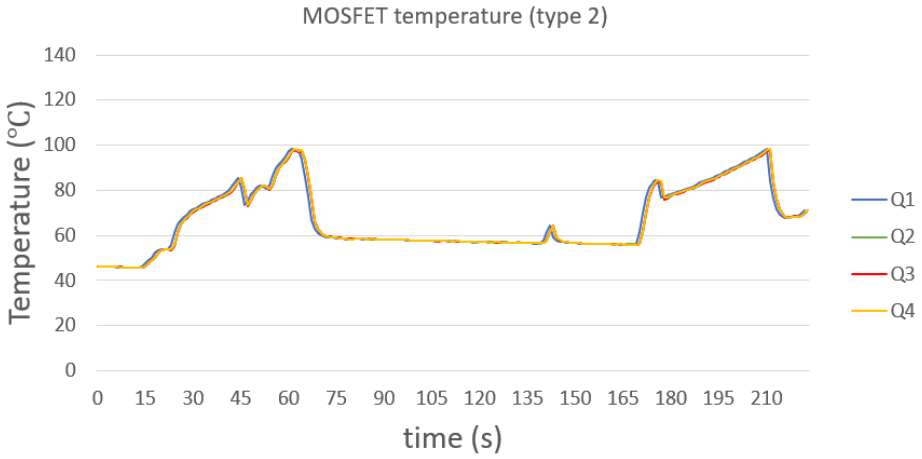


Figure 4.31: MOSFET temperature of the type-two power stage

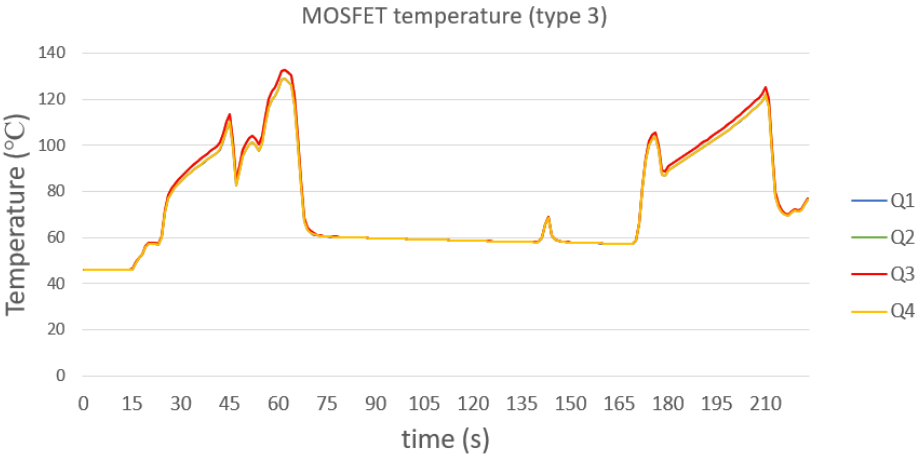


Figure 4.32: MOSFET temperature of the type-three power stage

4.7. Summary

In this chapter, the 3-D electromagnetic modelling, 3-D CFD modelling and 3-D heat transfer modelling of the motor drive are presented. The three kinds of modelling are directly and indirectly coupled in the multi-physic simulation on the performance of the motor drive.

From the modelling, the followings are worth being emphasized:

- In the modelling, the small structures in the geometric shape is replaced by the built-in function 'thin layer' in COMSOL to release the pressure on generating the mesh. Considering this is a dedicated function designed by COMSOL for simulating the physic process inside the small structure, the error brought by such a simplification should be acceptable.
- The thickness of the air gap and the solder layer is highly dependent on how well the components are soldered and how well the thermal grease adhere to the heatsink and the PCB. Apparently, in the modelling a nice manufacturing condition is assumed.
- The boundary condition setting is crucial for making the simulation close to the reality. In the modelling, some boundary conditions are idealized for decreasing the computational cost.

Apparently, to validate the correctness of the modelling, the measurements based on the hardware is necessary. The results from the measurements act as a feedback which helps on improving the accuracy of the modelling. Once the modelling is proved to be accurate enough, the same modelling method can be applied to the other designs and helps decreasing the time and cost for the development.

From the results of the simulation, the followings are worth being emphasized:

- It is obvious that a more symmetrical layout helps with a more evenly distributed temperature and current. The advantages of the symmetrical layout is more obvious under the large surge current condition.
- A trade-off is found between making the layout compact so that the parasitic inductance is small and making the layout more scattered so that the temperature of the MOSFET is lower.
- All the three types of power stages satisfy the requirements on the maximum junction temperature. Considering the requirements on making the parasitic elements small, the type-three power stage should be the best among the three.

5

Conclusion & Future work

5.1. Conclusion

A systematic approach for the design of the GaN-based 4-parallel MOSFET motor drive is presented. This motor drive running at 50kHz with a 150V nominal DC bus voltage. The design is dedicate to the demands of the Nuna in the WSC.

The development of the motor drive is divided into 3 parts that are the 1-D modelling, hardware design and 3-D modelling. The conclusions from each part can be draw as below:

1. From the 1-D modelling and evaluation based on it introduced in the chapter 2, it can be seen that:
    - from the 1-D thermal modelling, it is obvious that such a modelling method is suitable for a rough estimation. However, it is not enough for a thorough research on the thermal aspect.
    - the most important reason of the lower switching loss of the GaN and SiC MOSFET compared with the CoolMOS is not their fast switching speed but their low even zero reverse-recovery charge.
    - for the GaN and SiC MOSFET, the conduction loss is much higher than the switching loss in the high current condition. To some extent, adding the parallel MOSFETs helps increasing the efficiency of the motor drive. However, as the gate driver loss and influence of the parasitic inductance on the switching loss are not considered, the optimized number of the parallel MOSFET is not clear.
    - from the efficiency evaluation, there is a possibility of further increasing the efficiency of the motor drive for the Nuon Solar Team.
2. From the hardware design introduced in the chapter 3, it can be seen that:
    - the parasitic inductance of the PCB trace has impact on the switching loss. Therefore, the switching loss of the MOSFET is not only determined by its own characteristics but also the design of the PCB. Because of this, measurements is the only precise way for precisly estimating the switching loss.
    - the parasitic inductance L_g between the gate driver and the gate has significant impact on the delay on the switch-on of the MOSFET. For a design with parallel MOSFET in one position, it is crucial to control the this value by making a nice symmetrical layout design.
    - for the GaN MOSFET used in this project, it is crucial to make the layout of the gate driver and power stage compact to make the parasitic inductance L_g in the gate drive loop small to prevent the fault turn-on problem.
    - for the GaN MOSFET used in this project, it is crucial to make the layout of the gate driver and power stage compact to make the parasitic inductance L_{loop} in the power loop small to satisfy the high switching frequency.

3. From the 3-D modelling and evaluation in the chapter 4, it can be seen that:
    - the thickness of the air gap and the solder layer is highly dependent on how well the components are soldered and how well the thermal grease adhere to the heatsink and the PCB. After the manufacturing of the motor drive, these parameters should be estimated to refine the 3-D modelling.
    - it is obvious that a more symmetrical layout helps with a more evenly distributed current. The self-balance characteristic of the MOSFET can only decrease the imbalance of the current sharing among the parallel MOSFETs but not totally eliminate it.
    - a more symmetrical layout helps with a more evenly distributed temperature as well. It is more obvious under the large surge current condition, because the thermal runaway characteristic of the GaN MOSFET enlarges the temperature difference.
    - a trade-off is found between making the layout compact so that the parasitic inductance is small and making the layout more scattered so that the temperature of the MOSFET is lower.
    - all the three types of power stages satisfy the requirements on the maximum junction temperature. Considering the requirements on making the parasitic elements small, the type-three power stage should be the best among the three.

5.2. Future work

For the future work, several crucial things are worth to be mentioned.

- First and foremost, the prototype of the power stage and the gate driver can be constructed. It is very important to use the realistic performance as a feedback to refine the modelling.
- After making the prototype, the switching loss of the MOSFET can be measured precisely.
- Doing the temperature test under the small current condition for safety. The test is used to estimate the thickness of the air gap made during the manufacturing.
- According to the air gap thickness, refine the 3-D modelling and do the temperature simulation to check if the design satisfying the maximum junction requirements.
- The heatsink design is not optimized in this project. It mainly results from the uncertainty in the thickness of the air gap. However, with the feedback from the measurements, the optimization on the heatsink can proceed.

A

Load profile plotting

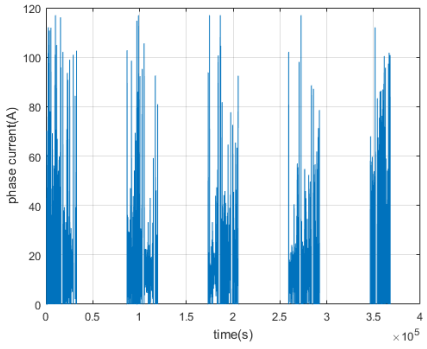


Figure A.1: Amplitude of one phase current of the motor in the 5 days

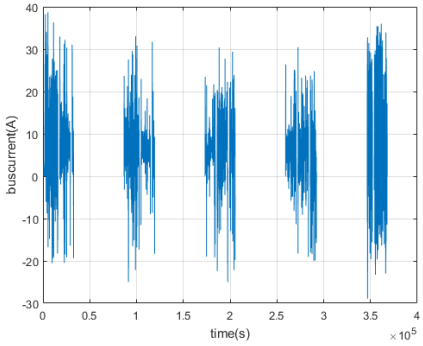


Figure A.2: DC bus current in the 5 days

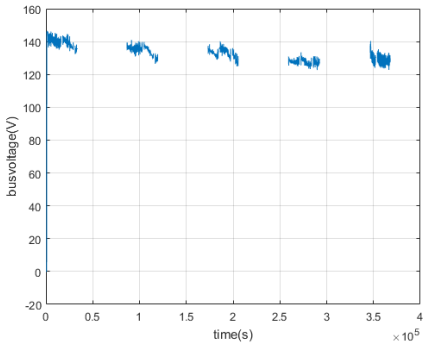


Figure A.3: DC bus voltage in the 5 days

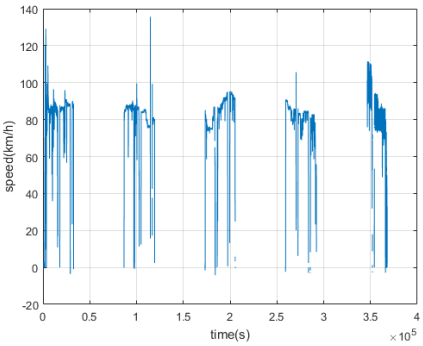
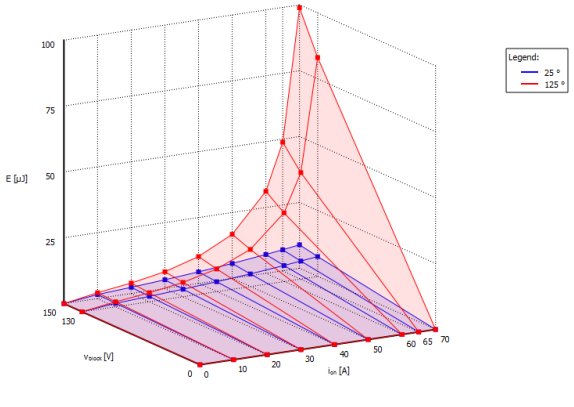


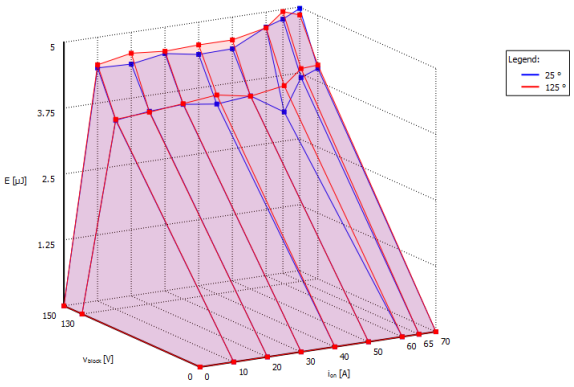
Figure A.4: Speed of Nuna 9 in the 5 days

B

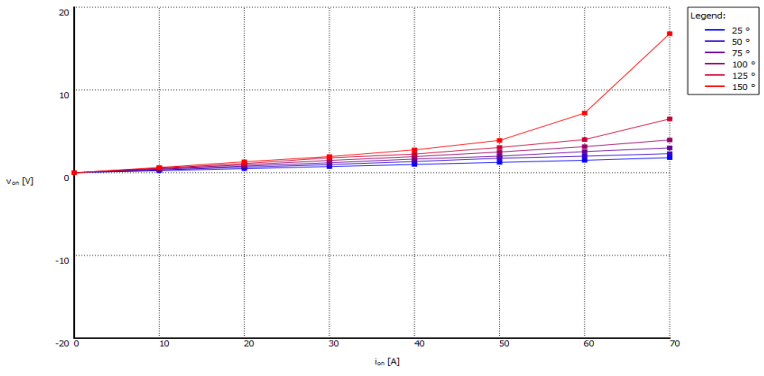
The look-up tables of the conduction and switching loss



(a) Switching on loss (E_{on})

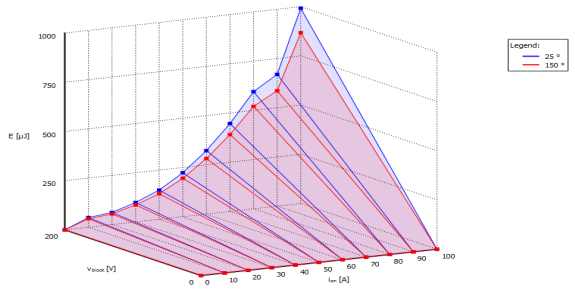


(b) Switching off loss (E_{off})

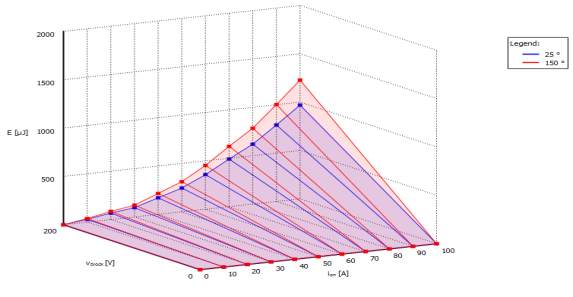


(c) $V_{ds(on)}$ in terms of different I_{ds} and T_j

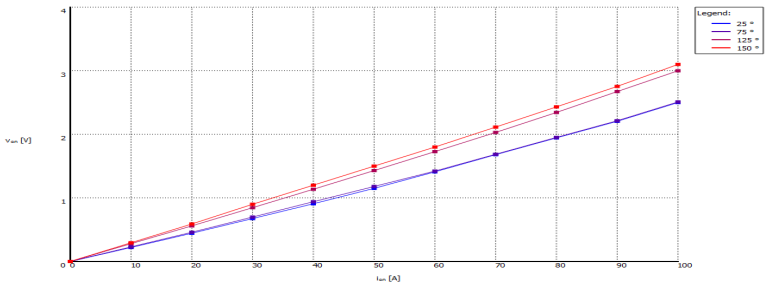
Figure B.1: Conduction loss and switching loss of GS66516B (GaN)



(a) Switching on loss (E_{on})

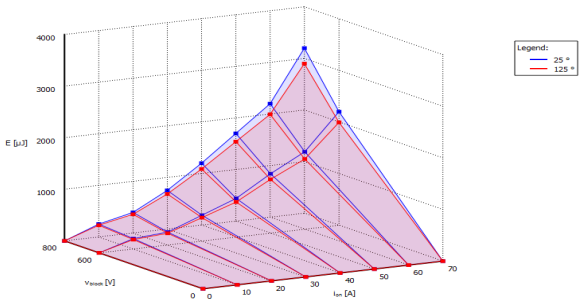


(b) Switching off loss (E_{off})

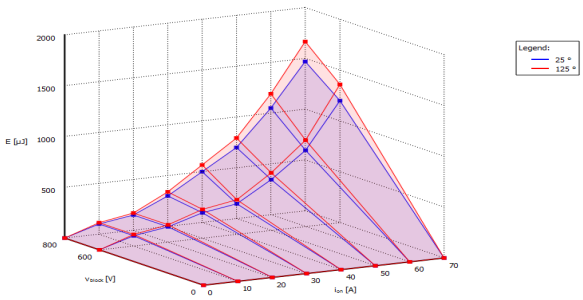


(c) $V_{ds(on)}$ in terms of different I_{ds} and T_j

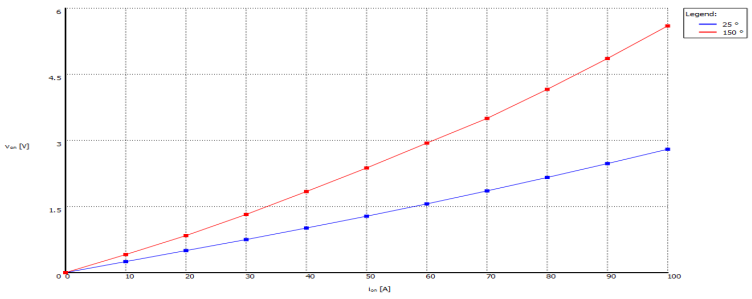
Figure B.2: Conduction loss and switching loss of SCT3022AL (SiC)



(a) Switching on loss (E_{on})

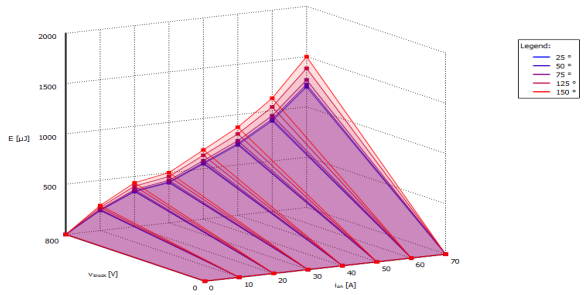


(b) Switching off loss (E_{off})

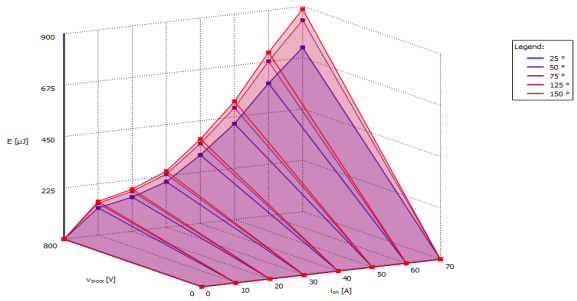


(c) $V_{ds(on)}$ in terms of different I_{ds} and T_j

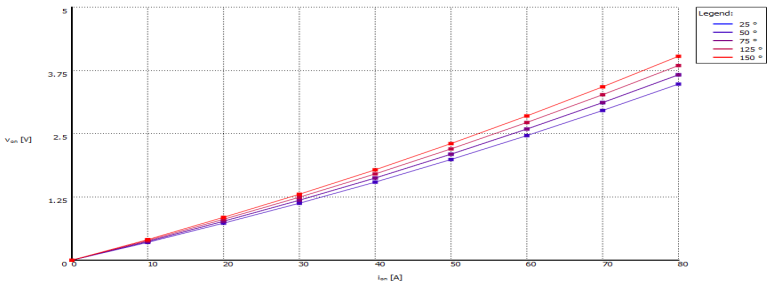
Figure B.3: Conduction loss and switching loss of C2M0025120D (SiC)



(a) Switching on loss (E_{on})

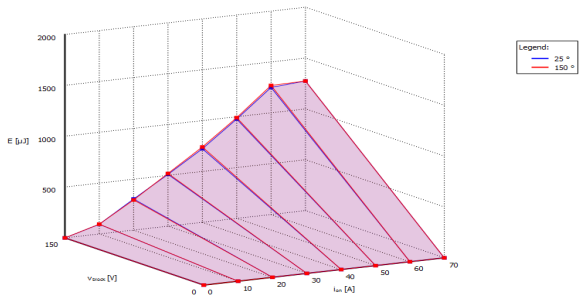


(b) Switching off loss (E_{off})

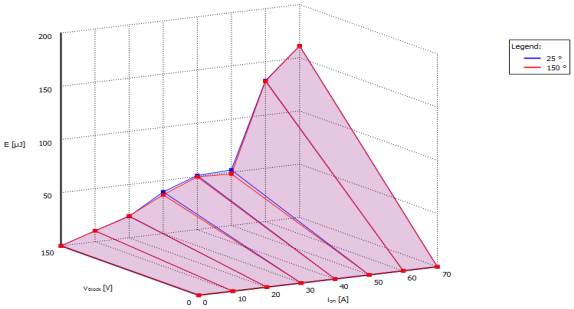


(c) $V_{ds(on)}$ in terms of different I_{ds} and T_j

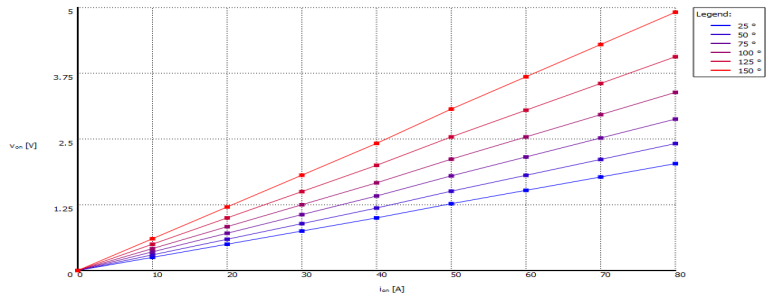
Figure B.4: Conduction loss and switching loss of SCTWA50N120 (SiC)



(a) Switching on loss (E_{on})



(b) Switching off loss (E_{off})



(c) $V_{ds(on)}$ in terms of different I_{ds} and T_j

Figure B.5: Conduction loss and switching loss of IPT60R028G7 (Si)

C

Design of the auxiliary power supply and interface

C.1. Auxiliary power supply

The power used for the ICs are all draw from the 12V CAN bus. In the figure C.1, the overview on the auxiliary power supply system is shown. The 12V CAN bus is isolated from the devices on the motor drive by a 12V-to-12V 8W DC/DC converter. Except from the main isolation, the isolated power supply R1S-1209 is used to isolate the input side from the output side of the isolated gate driver IC Si82171 and the isolated amplifier AMC1301 and AMC1311.

C.1.1. 12V generation

The 12V-to-12V DC/DC converter is needed for isolation. The total power needed by the auxiliary circuit is roughly 3W. Based on this, TEN-8-1212 whose maximum output power is 8W is used to isolated the auxiliary circuit of the motor drive from the CAN bus.

C.1.2. 9V generation

The 9V is used to power the V_{DD2} of the gate driver IC Si8271 (76.5mW). Each gate driver IC has an individual power supply which is placed near the gate driver IC to minimize the gate loop inductance. Because isolation is necessary, the isolated converter R1S-1209 whose maximum power capability is 1W is used.

C.1.3. 5V generation

The 5V is used to power the following devices:

- V_{DD} of the three hall effect sensors HC2H200-S ($3 \times 13.5mA = 40.5mA$)
- V_{DD} of the five differential comparators TLC372 ($5 \times 400\mu A = 2mA$)
- V_{DD1} of the gate driver IC Si8271 ($6 \times 10mA = 60mA$)
- V_{DD} of the voltage references REF2033 ($0.46mA$)
- Input of the linear voltage regulator TLV1117-33 (660mW)

Given the current consumption of the devices, the total power needed can be calculated and roughly equals 1.5W. For the comparators and hall effect sensors, the supply voltage should be stable to operate properly. Therefore, a linear voltage regulator UA7805 whose maximum power capability is 7.5W is selected.

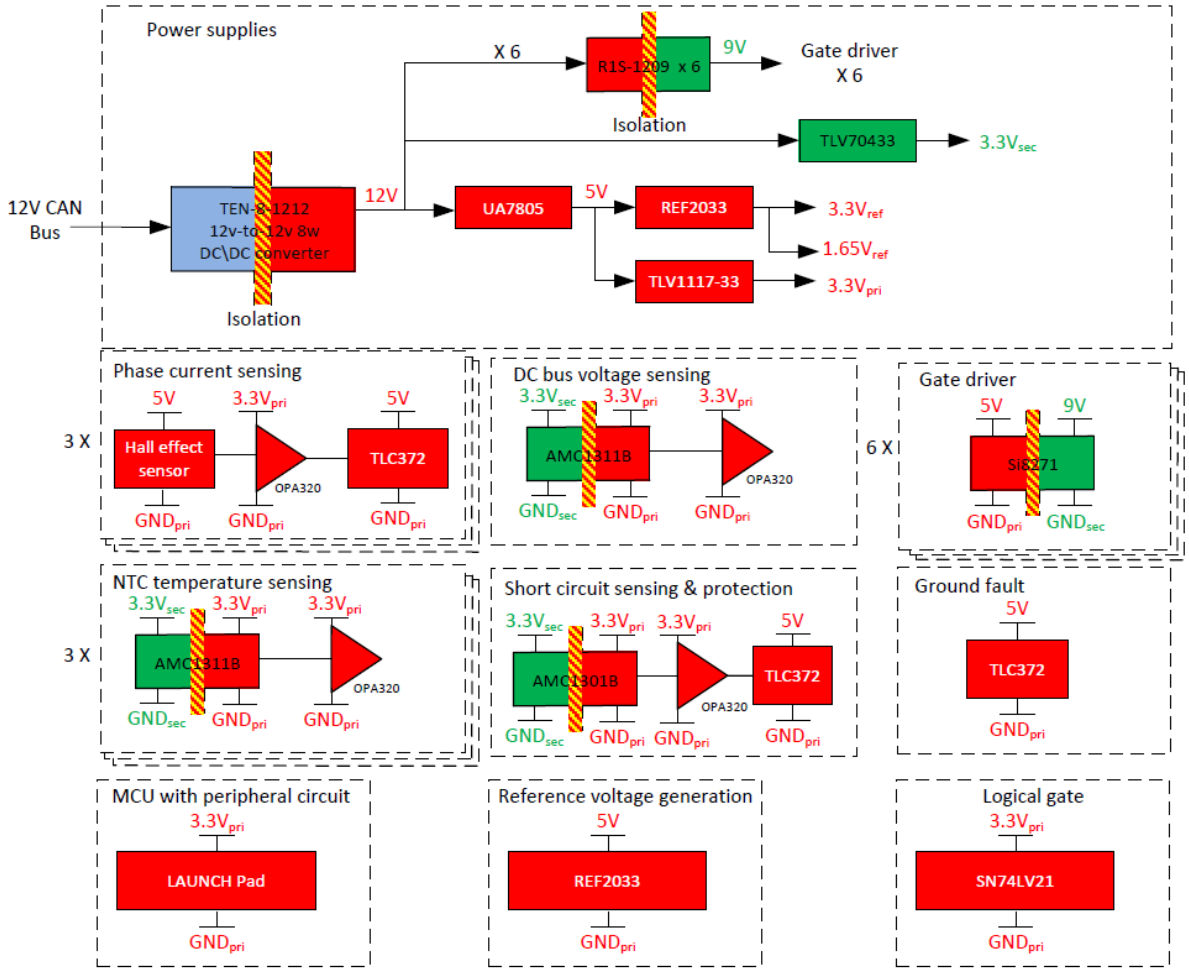


Figure C.1: Overview on the power supply system

C.1.4. $3.3V_{pri}$ generation

The $3.3V_{pri}$ is used to power the following devices:

- V_{DD} of the eight op-amp OPA320Q ($8 \times 1.85mA = 14.8mA$)
- V_{DD} of the AND gate SN74LV21ADR ($20\mu A$)
- V_{DD2} of the four isolated amplifier AMC1311B ($4 \times 7.2mA = 28.8mA$)
- V_{DD2} of the isolated amplifier AMC1301 (5.6mA)
- 3.3V supply for LAUNCHXL-F28069M (150mA)

The total power consumption is about 0.66W. Thus, a linear voltage TL1117-33 whose maximum power capability is 2.64W is chosen.

C.1.5. $3.3V_{sec}$ generation

The $3.3V_{sec}$ is used to power the following devices:

- V_{DD1} of the four isolated amplifier AMC1311B ($4 \times 8.4mA = 33.6mA$)
- V_{DD1} of the isolated amplifier AMC1301 (6.9mA)

The total power consumption is about 150mW. Thus, a linear voltage TLV70433 is selected because of its wide input voltage range and sufficient power capability (0.5W).

C.2. Interface design

Given the pin out information of LAUNCHXL-F28069M [51], the interface designed for LAUNCH Pad is depicted in the figure C.2.

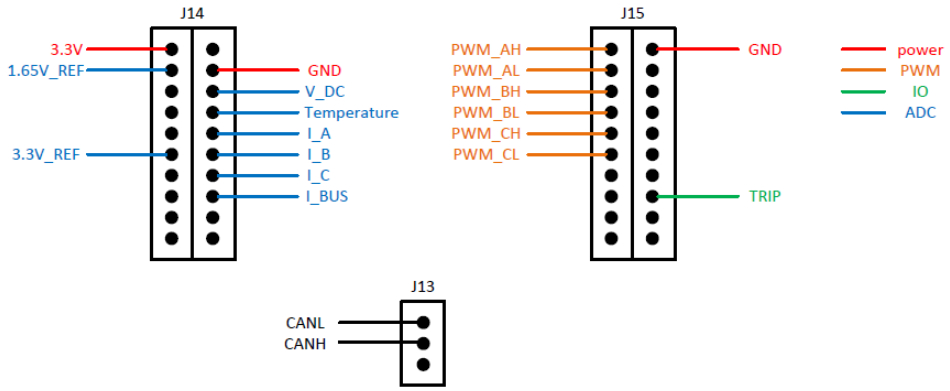


Figure C.2: Interface with the LAUNCHXL-F28069M

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