Thermal-Aware Channel Capacity

Chee, Yeow Meng ; Etzion, Tuvi ; Schouhamer Immink, Kees A.; Nguyen, Tuan Thanh ; Vu, Van Khu ; Weber, Jos H.; Yaakobi, Eitan

DOI
10.1109/ISIT54713.2023.10206738

Publication date
2023

Document Version
Final published version

Published in
2023 IEEE International Symposium on Information Theory, ISIT 2023

Thermal-Aware Channel Capacity

Yeow Meng Chee[*], **Tuvi Etzion**[†], **Kees A. Schouhamer Immink**[‡], **Tuan Thanh Nguyen**[§], **Van Khu Vu**[*], **Jos H. Weber**[¶], and **Eitan Yaakobi**[†]

[*] Department of Industrial Systems Engineering and Management, National University of Singapore, Singapore
[†] Department of Computer Science, Technion — Israel Institute of Technology, Haifa, 3200003 Israel
[‡] Turing Machines Inc., 3016 DK Rotterdam, The Netherlands
[§] Science, Mathematics and Technology Cluster, Singapore University of Technology and Design, Singapore
[¶] Department of Applied Mathematics, Delft University of Technology, 2628 CD Delft, The Netherlands

2023 IEEE International Symposium on Information Theory (ISIT) | 978-1-6654-7554-9/23/$31.00 ©2023 IEEE | DOI: 10.1109/ISIT54713.2023.10206738

***Abstract*—High temperatures in electronic devices have a negative effect on their performance. Various techniques have been proposed and studied to address and combat this thermal challenge. To guarantee that the peak temperature of the devices will be bounded by some maximum temperature, the transmitted signal has to satisfy some constraints.**

With this motivation, we study the constrained channel that only accepts sequences that satisfy prescribed thermal constraints. The main goal in this paper is to compute the capacity of this channel. We provide the exact capacity of the channel with some certain parameters and we also present some bounds on the capacity in various cases.

Finally, we consider the model that multiple wires are available to use and find out the smallest number of wires required to satisfy the thermal constraints.

I. Introduction

High temperatures in electronic components should be avoided as they degrade their performance and lifetime. Various thermal-aware design techniques have been proposed to lower the average dissipation of electronic products by lowering the number of pulses in signal state transitions [1] used, for example, in a parallel on-chip bus [2, 3] or in laser-based recording [4]. Several coding techniques are proposed to combat the challenges of high temperature [5]–[9]. Coding techniques are designed to minimize the average power consumption by using (sets of) constant-weight codes of low weight [10, 11]. Coding schemes that make it possible to directly control the peak temperature of the hottest wires of a parallel bus have been presented recently [3, 11]. In these schemes, it is required to use $n > k$ wires to encode a given k-bit bus. However, no coding technique was provided to detect and control the hottest wires on the chip. To control the temperature of each wire with coding techniques one should start to apply coding technique on a single wire. Coding for serial single-wire buses or electronic components such as laser diodes requires a different coding approach.

Laser diodes have been widely used in optical communications and data storage, both optical and heat assisted magnetic recording [12]. For example, in binary recording channels, a high-power laser diode is used to record (burn) data into an optical disc [13]. In numerous channels, data are recorded or transmitted by switching a laser on and off. As temperature increases, threshold current increases while lasing efficiency decreases, and as a result more drive current is required to turn on the laser diode [14]. In order to reduce the dissipation and extend the life of the electronic component, prior art code design has been guided by minimizing the average number of laser pulses [4].

We study systems where the maximum temperature of the electronic components must be bounded by a given number. It is assumed that the chip temperature rises by t_1 (degrees) after a current 'on' period and that its temperature lowers by t_0, after an 'off' period. The maximum allowed chip temperature is $t_{\max}$ and the base (ambient) temperature is $t_{\min}$ where $t_{\max} > t_{\min}$. Clearly, at most $\lfloor (t_{\max} - t_{\min})/t_1 \rfloor$ consecutive pulses can be applied before the chip reaches its maximum allowed temperature, where the integer function $\lfloor x \rfloor$ maps x to the largest integer less than or equal to x. When the chip is at its base temperature, $t_{\min}$, the temperature cannot decrease further. To guarantee that the temperature stays within desired bounds, we present and analyze coding techniques that encode data into sequences that satisfy some certain constraints. We then focus on the channel that only accepts these sequences.

The rest of the paper is organized as follows. Firstly, we provide some necessary notations and definitions of the thermal-aware channel and codes in Section II. Next, we present numerous results on the capacity of the channel in various cases in Section III. Finally, in Section IV, we study a model where multiple wires are available to the users.

II. Notations and Definitions

We start with a description of the thermal-aware channel model. The general modelling of the component temperature due to electrical activity might be complex and thus we have opted for a simpler model which is amenable for code design and analysis.

It is assumed that the temperature increases by t_1 after a current 'on' period and the temperature decreases by t_0, after an 'off' period. The maximum allowed temperature is $t_{\max}$ while the base temperature is $t_{\min}$. Without loss of generality, we assume that the base temperature is $t_{\min} = 0$. All temperature variables are non-negative real numbers.

Let $\Sigma = \{0, 1\}$, $[[n]] = \{1, 2, \ldots, n\}$, and let the signal be defined by the binary sequence $\boldsymbol{x} = (x_1, \ldots, x_n) \in \Sigma^n$, where a '1' denotes a current 'on' period and a '0' denotes the 'off'

period. Given a sequence $\boldsymbol{x} = (x_1, \ldots, x_n) \in \Sigma^n$, we denote $\boldsymbol{x}[i, j] = (x_i, \ldots, x_j)$ as a substring of $\boldsymbol{x}$ from index i to index j. Given two real positive numbers $t_0, t_1 \in \mathbb{R}$, we define the following *temperature map*, $\Psi_{t_0,t_1} : \Sigma^n \to \mathbb{R}^n$, such that, for each sequence $\boldsymbol{x} = (x_1, \ldots, x_n) \in \Sigma^n$, we obtain

$$\Psi_{t_0,t_1}(\boldsymbol{x}) \triangleq \boldsymbol{s} = (s_1, \ldots, s_n) \in \mathbb{R}^n,$$

where $s_0 = 0$ and for all $i = 0, 1, \ldots, n-1$, $s_{i+1} = s_i + t_1$ if $x_{i+1} = 1$ and $s_{i+1} = \max\{s_i - t_0, 0\}$ if $x_{i+1} = 0$. The sequence $\boldsymbol{s} = \Psi_{t_0,t_1}(\boldsymbol{x})$ is called the (t_0, t_1)-*temperature sequence of* $\boldsymbol{x}$. It is assumed that the temperature of the device at the initial point is the base temperature $s_0 = t_{\min} = 0$, and that the temperature of the device at time i is s_i when $\boldsymbol{x}$ is the transmitted signal.

To guarantee that the device will not be over-heated, the peak temperature of the device must be bounded by $t_{\max}$, that is, $\max_{1 \leqslant i \leqslant n} s_i \leqslant t_{\max}$. In this work, we are interested in sequences that satisfy the above constraint and we consider the channel that only accepts these sequences.

Definition 1 *Let $t_{\max}$, t_0, t_1 be some positive real numbers.*

- *A sequence $\boldsymbol{x} = (x_1, \ldots, x_n) \in \Sigma^n$ is called a $(t_{\max}, t_0, t_1)$-**thermal-aware sequence** if the (t_0, t_1)-temperature sequence of $\boldsymbol{x}$, $\boldsymbol{s} = \Psi_{t_0,t_1}(\boldsymbol{x}) = (s_1, \ldots, s_n)$, satisfies $0 \leqslant s_i \leqslant t_{\max}, \forall 1 \leqslant i \leqslant n$.*
- *The set of all $(t_{\max}, t_0, t_1)$-thermal-aware sequences of length n is called the **maximal** $(t_{\max}, t_0, t_1)$-**thermal-aware code**, and is denoted by $\mathcal{A}(t_{\max}, t_0, t_1, n)$.*
- *The channel that only accepts $(t_{\max}, t_0, t_1)$-thermal-aware sequences is called the $(t_{\max}, t_0, t_1)$-**thermal-aware channel**.*

Given three parameters $t_{\max}, t_0, t_1$, let $k = \frac{t_1}{t_0}$ and $M = \frac{t_{\max}}{t_0}$. We observe that a $(t_{\max}, t_0, t_1)$-thermal-aware sequence is also an $(M, 1, k)$-thermal-aware sequence. For simplicity, if $t_0 = 1$, a $(t_{\max}, t_0, t_1)$-thermal-aware sequence is called an (M, k)-*thermal-aware sequence* and similarly the $(t_{\max}, t_0, t_1)$-thermal-aware channel is referred to as the (M, k)-*thermal-aware channel*. The maximal (M, k)-thermal aware code of length n is denoted by $\mathcal{A}(M, k, n)$.

Example 1 *Let $k = 1$ and $M = 3$. We consider the sequence $\boldsymbol{x} = (1, 1, 0, 1, 0, 0, 0, 1, 1, 1)$ and the $(1, 1)$-temperature sequence of $\boldsymbol{x}$ is $\boldsymbol{s} = (1, 2, 1, 2, 1, 0, 0, 1, 2, 3)$. Since $s_i \leqslant 3$ for all i, the sequence $\boldsymbol{x}$ is called a $(3, 1)$-thermal-aware sequence. Now, we consider the sequence $\boldsymbol{y} = (1, 0, 0, 0, 1, 1, 1, 1, 0, 0)$ and its $(1, 1)$-temperature sequence $\boldsymbol{v} = (1, 0, 0, 0, 1, 2, 3, 4, 3, 2)$. Since $v_8 = 4 > 3 = M$, we see that the sequence $\boldsymbol{y}$ is not a $(3, 1)$-thermal-aware sequence.*

Given M and k, the maximal asymptotic rate of the maximal (M, k)-thermal-aware codes is

$$\mathsf{cap}_{\mathsf{TA}}(M, k) = \limsup_{n \to \infty} \frac{\log |\mathcal{A}(M, k, n)|}{n}.$$

The maximal asymptotic rate $\mathsf{cap}_{\mathsf{TA}}(M, k)$ is also referred as the capacity of the (M, k)-thermal-aware channel. In this work, we are interested in finding the maximal code $\mathcal{A}(M, k, n)$, its size, and the capacity of the (M, k)-thermal-aware channel.

III. The Capacity of the Thermal-Aware Channel

In this section, we aim to compute the capacity of the thermal-aware channel which is also the maximal asymptotic rate of the thermal-aware codes. For $k > M$, it is not possible to store even a single one and hence only the all-zero sequence is an (M, k)-thermal-aware sequence which directly implies that the capacity is zero in this case. Thus, we only focus on the case $k \leqslant M$. We also note that $k \geqslant 1$ is more suitable for practical purpose, however for a comprehensive theoretical study, we investigate in this work both cases of $k \geqslant 1$ and $k < 1$.

We first provide some good bounds on the capacity of this channel in Subsection III-A. These bounds usually hold for some family of infinitely many parameters in various cases, however, they are not tight. Then, in Subsection III-B and Subsection III-C, we present some techniques to compute the capacity of the channel exactly in the case k is an integer and the case that k is a rational number, respectively. In both cases, we provide some numerical results on the capacity of the channel. Furthermore, when $k = 1$, we show an explicit formula of the capacity of the $(M, 1)$-thermal-aware channel. Due to the lack of space, we skip some proofs of our results in this version.

A. General bounds on the capacity

In Subsection III-C, we compute some numerical results on the capacity of the channel in general case when $k = p/q$ is rational. However, when the parameters p, q are large, the computation becomes much more complicated. In this subsection, we provide some mathematical bounds on the capacity in general case.

Theorem 1 *When $1 < k$, it holds that*

$$\mathsf{cap}_{\mathsf{TA}}(M, k) \leqslant H(\alpha)$$

where $\alpha = \frac{1}{1+k}$ and $H(\alpha)$ is the entropy function of α.

Theorem 2 *When $1 > k$, let $\delta = \lfloor \frac{M}{k} \rfloor$, it holds that*

$$\mathsf{cap}_{\mathsf{TA}}(M, k) \geqslant \log(2 \cos \frac{\pi}{\delta + 2}).$$

B. The capacity when k is a positive integer

In this subsection, we focus on computing the capacity of the channel exactly when k is a positive integer. Let $N = \lfloor M \rfloor$, we observe that the maximal (M, k)-thermal-aware code is the maximal (N, k)-thermal-aware code since the temperature of the device is always an integer. We can view this code as a constrained code where the codewords can be generated by all paths in a labelled graph with a set of $N+1$ states. The states set is denoted by $[N] = \{0, 1, \ldots, N\}$,

where every state represents a temperature level. For each $i = 0, \ldots, N-k$, there is an edge from state i to state $i+k$, corresponding to a signal 1 which increases the temperature from i to $i+k$. For each $i = 1, \ldots, N$, there is an edge from state i to state $i-1$, associated with a signal 0 which decreases the temperature from i to $i-1$. There is also a self loop at state 0 for the case of a signal 0 at the minimum temperature. This $(N+1) \times (N+1)$ transition matrix is denoted by $D_{N,k}$ and is formally defined as follows:

$$\begin{aligned} d_{N,k}(0,0) &= 1, \\ d_{N,k}(i,i-1) &= 1,\ i = 1, \ldots, N, \\ d_{N,k}(i,i+k) &= 1,\ i = 0, \ldots, N-k, \\ d_{N,k}(i,j) &= 0,\ \text{otherwise.} \end{aligned} \tag{1}$$

Example 2 *Figure 1 describes the labelled graph when $N = 4, k = 1$ and Figure 2 describes the labelled graph when $N = 4, k = 2$. The transition matrix when $N = 4$ and $k = 1$ is*

$$D_{4,1} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix}. \tag{2}$$

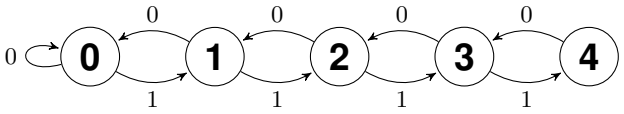

Figure 1. The labelled graph for the (4,1)-thermal-aware channel.

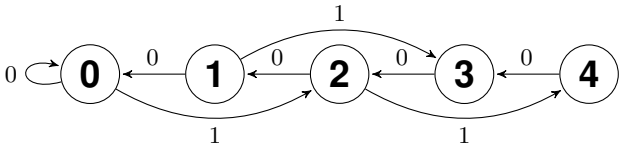

Figure 2. The labelled graph for the (4,2)-thermal-aware channel.

We observe that the (N,k)-thermal-aware channel is actually a constrained channel which can be represented by the above labelled graph. Hence, the capacity of the (N,k)-thermal-aware channel is also the capacity of the constrained channel represented by $D_{N,k}$. Now we turn our attention to the computation of the capacity of this constrained channel. Let

$$\Gamma_{N,k}(z) = \det[zI - D_{N,k}]. \tag{3}$$

The determinant $\Gamma_{N,k}(z)$ is an $(N+1)$-th degree polynomial in z, and is called the *characteristic polynomial* of $D_{N,k}$. Hence, it is well known that, the capacity of the above constrained channel [16] is

$$\mathsf{cap}_{\mathsf{TA}}(N,k) = \log_2 \lambda_{N,k}, \tag{4}$$

where $\lambda_{N,k}$ is the largest real root of the equation

$$\Gamma_{N,k}(z) = 0. \tag{5}$$

In other words, $\lambda_{N,k}$ is the largest real eigenvalue of the matrix $D_{N,k}$. It is possible to compute $\lambda_{N,k}$ in every case and thus find the capacity. Several results are computed and tabulated in Table I.

Next, we are interested in an explicit formula for the channel capacity in the general case. For this end, we investigate the characteristic polynomial $\Gamma_{N,k}(z)$. First, we define a slightly different matrix, namely the $(N+1) \times (N+1)$ integer matrix $E_{N,k}$ with elements $e_{N,k}(i,j) \in \{0,1\}$ by

$$\begin{aligned} e_{N,k}(0,0) &= 0, \\ e_{N,k}(i,j) &= d_{N,k}(i,j),\ \text{otherwise.} \end{aligned} \tag{6}$$

Let

$$\Phi_{N,k}(z) = \det[zI - E_{N,k}] \tag{7}$$

denote the characteristic polynomial of $E_{N,k}$.

We observe that, for the case $k = 1$, $E_{N,k}$ is the transition matrix of the state machine for the well-known RDS codes [17], [19], [20]. In this case, $\Phi_{N,1}(z)$ is often called a *Vieta-Fibonacci-like* polynomial, which is closely related to the well-known Chebyshev polynomial of the second kind [18] and

$$\Phi_{N,1}(2\cos x) = \frac{\sin(N+2)x}{\sin x}.$$

We generalise these results to obtain some interesting properties of $\Phi_{N,k}(z)$ for any k. Define $\Phi_{0,k}(z) = 1, \Phi_{1,k}(z) = z$ and $\Phi_{i,k}(z) = 0$, $i < 0$. The connection between $\Phi_{N,k}(z)$ and $\Gamma_{N,k}(z)$ is derived in the next lemma.

Lemma 1 *It holds that*

$$\Gamma_{N,k}(z) = \Phi_{N,k}(z) - \Phi_{N-1,k}(z).$$

From Lemma 1, we see that $\Phi_{N,k}(z)$ and $\Gamma_{N,k}(z)$ are closely related, and thus, the RDS codes and the thermal-aware codes are closely related. Following the argument in [18], we derive an explicit formula for the characteristic polynomial, as follows,

$$\Phi_{N,k}(z) = \sum_{i=0}^{\lfloor (N+1)/(k+1) \rfloor} (-1)^i \binom{N+1-ki}{i} z^{N+1-i(k+1)}. \tag{8}$$

Using Equation (8) together with Lemma 1, we can find the characteristic polynomials $\Gamma_{N,k}(z)$ and compute the capacity of the channel. For example, when $N = k$, we obtain the following characteristic polynomial

$$\Gamma_{N,N}(z) = z^{N+1} - z^N - 1. \tag{9}$$

The characteristic polynomial (9) is well-studied for a family of run length constrained codes and the capacity of the channel in this case is known [15]. Furthermore, we can find an explicit formula of the capacity of the $(N,1)$-thermal-aware channel as follows.

Theorem 3 *The capacity of $(N,1)$-thermal-aware channel is*

$$\mathsf{cap}_{\mathsf{TA}}(N,1) = \log(2\cos(\frac{\pi}{2N+3})).$$

Proof: From [20], pp. 200–203, the polynomial $\Phi_{N,1}(z)$ can be written as follows.

$$\Phi_{N,1}(2\cos x) = \frac{\sin(N+2)x}{\sin x}, \tag{10}$$

where $z = 2\cos x$. Using Lemma 1 with $k = 1$ and $z = 2\cos x$, we obtain

$$\begin{aligned}\Gamma_{N,1}(2\cos x) =& \Phi_{N+1,1}(2\cos x) - \Phi_{N,1}(2\cos x)\\ =& \frac{\sin(N+2)x}{\sin x} - \frac{\sin(N+1)x}{\sin x}\\ =& \cos(\frac{2N+3}{2}x)\frac{2\sin(x/2)}{\sin x}.\end{aligned}$$

The largest root of $\Gamma_{N,1}(z)$ is $\lambda = 2\cos\frac{\pi}{2N+3}$. Hence, the capacity of $(N,1)$-thermal-aware channel is $\mathsf{cap}_{\mathsf{TA}}(N,1) = \log(2\cos\frac{\pi}{2N+3})$, which concludes the proof. ∎

C. The capacity when k is a positive rational number

We now consider a more general case when k is a positive rational number. Let $k = \frac{p}{q}$, where the two positive integers p, q are co-prime. Let $N = \lfloor qM \rfloor$. Hence, an (M,k)-thermal-aware code is an (N,q,p)-thermal-aware code, where all three parameters N, p, q are integers. Since p and q are two positive integers, it follows that the temperature of the device is an integer from 0 to N. Let $[N]$ be the set of states. We can view the (N,q,p)-thermal-aware channel as a constrained channel and we can build a states machine of the channel. Each state of the machine represents a temperature level. We can build a states machine (the labelled graph) of the channel as follows. The graph $G_{N,q,p}$ has $N+1$ vertices, corresponding to $N+1$ states. For each $i = 0,\ldots,N-p$, there is an edge from vertex i to vertex $i+p$, corresponding to signal 1 and the temperature increases from i to $i+p$. For each $i = q,\ldots,N$, there is an edge from vertex i to vertex $i-q$, corresponding to signal 0 and the temperature decreases from i to $i-q$. And for each $i = 0,\ldots,q-1$, there is an edge from vertex i to vertex 0, corresponding to signal 0 and the temperature decreases to the base temperature. Each (N,q,p)-thermal-aware sequence of length n can be represented as a path of length n from the vertex 0 to any vertex among $N+1$ vertices in the above labelled graph. The number of (N,q,p)-thermal-aware sequences of length n is the number of distinct paths of length n from the vertex 0 to any vertex in the graph. The capacity of the (N,q,p)-thermal-aware channel is the capacity of the constrained channel represented by the above states machine.

We now focus on the transition matrix of the states machine. The $(N+1)\times(N+1)$ transition matrix $D_{N,q,p}$ with binary elements $d_{N,q,p}(i,j) \in \{0,1\}$ is

$$\begin{aligned} d_{N,q,p}(i,0) &= 1,\ i = 0,\ldots,q-1,\\ d_{N,q,p}(i,i-q) &= 1,\ i = q,\ldots,N,\\ d_{N,q,p}(i,i+p) &= 1,\ i = 0,\ldots,N-p,\\ d_{N,q,p}(i,j) &= 0,\ \text{otherwise.}\end{aligned} \tag{11}$$

For example, Figure 3 shows the states machine when $N = 7, p = 3, q = 2$.

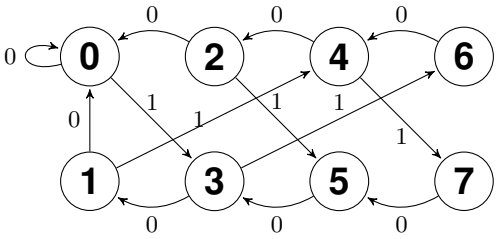

Figure 3. The labelled graph for the (7,2,3)-thermal-aware channel

Since an (N,q,p,n)-thermal-aware sequence is equivalent to a path of length n from the vertex 0 in the above state machine, the maximum size of the (N,q,p,n)-thermal-aware code is the number of distinct paths of length n from the vertex 0 in the above labelled graph. Since the matrix $D_{N,q,p}$ is of size $(N+1)\times(N+1)$, we can compute $D^n_{N,q,p}$ in $O(\log n)$ time, given N, q, p. If the matrix $A_{N,q,p} = D^n_{N,q,p}$, then $a_{i,j}$ is the number of paths of length n from vertex i to vertex j in the graph $G_{N,q,p}$. Hence, the number of paths of length n from vertex 0 to any vertex in the graph $G_{N,q,p}$ is $\sum_{j=1}^{N} a_{0,j}$ which can be computed in $O(1)$ time. Hence, we can count the number of valid sequences in the (N,q,p)-thermal-aware channel in $O(\log n)$ time. We state the result formally as follows.

Theorem 4 *Given M,k,n, there is an algorithm to compute the maximal size of the (M,k,n)-thermal-aware code $|\mathcal{A}(M,k,n)|$ with at most $O(\log n)$ operations.*

In other words, we have a sub-linear algorithm to compute the maximal size of the (M,k,n) thermal-aware code, given M,k. Furthermore, we also can compute the capacity of the thermal-aware channel using the states machine. Apply the well-known Perron-Frobenius theory [23], we know that the matrix $D_{N,q,p}$ has the largest real eigen value $\lambda_{N,q,p}$. Then, we calculate the capacity $\mathsf{cap}_{\mathsf{TA}}(M,k) = \log\lambda_{N,q,p}$. Given M,k, we can compute the capacity $\mathsf{cap}_{\mathsf{TA}}(M,k)$ and tabulate some selected results in Table I. As expected, $\mathsf{cap}_{\mathsf{TA}}(M,k)$ is increasing in M and decreasing in k. Further, note that it follows from Theorem 1 that $\mathsf{cap}_{\mathsf{TA}}(M,k)$ cannot exceed $H(1/(1+k))$ for all M and $k > 1$.

IV. Thermal-Aware Channel with Multiple Wires

In this section, we introduce the thermal-aware channel when multiple wires are available to the user. When the chip reaches its maximum allowed temperature in some of the wires, the pulses can be applied in one of the other available wires. We observe that as the number of wires increases, the information rate can be significantly increased as compared to the single wire case. To minimize the cost and power supply, we are interested in determining the minimum number of wires necessary so that the temperature always stays within the desired boundaries for arbitrary transmitted signals.

TABLE I
CAPACITY $\mathsf{cap}_{TA}(M,k)$ VERSUS k AND M.

M	$k=1/2$	$k=2/3$	$k=1$	$k=4/3$	$k=3/2$	$k=2$	$k=5/2$	$k=3$	$k=7/2$	$k=4$	$k=5$
2	0.969757	0.925323	0.84955	0.679286	0.6509	0.551463	-	-	-	-	
3	0.990431	0.964523	0.91026	0.803641	0.759177	0.64060	0.52934	0.46496	-	-	-
4	0.996655	0.983464	0.94034	0.854675	0.81677	0.72631	0.597003	0.52448	0.45164	0.40569	-
5	0.998774	0.9911	0.95746	0.88822	0.859232	0.76745	0.662721	0.58152	0.498964	0.44894	0.36199
6	0.999541	0.995122	0.96812	0.911378	0.882798	0.79917	0.699842	0.63462	0.544883	0.49034	0.39519
7	0.999826	0.997202	0.97522	0.925765	0.899583	0.82017	0.730043	0.66284	0.588095	0.52910	0.42694
8	0.999934	0.998371	0.98019	0.936103	0.911923	0.83628	0.753438	0.68628	0.613699	0.56500	0.45681
9	0.999975	0.999035	0.98380	0.943895	0.92099	0.84836	0.769528	0.70509	0.635383	0.58535	0.48464
10	0.99999	0.999424	0.98650	0.949854	0.928043	0.85792	0.782481	0.71908	0.653458	0.60285	0.51046

This approach can be applied when we are interested in transmitting information on a set of wires which do not exceed the maximum allowed temperature. One of the motivations to consider multiple wires is to use the coding scheme also to send information of a bus which has m wires to send information words of a larger size.

Given a binary sequence $\boldsymbol{x} = (x_1, x_2, \ldots, x_n) \in \Sigma^n$ and a set $I \subseteq [[n]] = \{1, 2, \ldots, n\}$, the complete-projection of $\boldsymbol{x}$ in I, denoted by $\mathrm{P}_I(\boldsymbol{x})$, is the binary sequence $\boldsymbol{y} = (y_1, y_2, \ldots, y_n)$ where $y_i = x_i$ if $i \in I$, and $y_i = 0$ otherwise. For example, consider $I_1 = \{1, 3, 4, 5\}$, $I_2 = \{2, 6\}$, and $\boldsymbol{x} = (1, 0, 0, 1, 0, 1)$. We then have $\mathrm{P}_{I_1}(\boldsymbol{x}) = (1, 0, 0, 1, 0, 0)$ and $\mathrm{P}_{I_2}(\boldsymbol{x}) = (0, 0, 0, 0, 0, 1)$.

Definition 2 *A binary sequence $\boldsymbol{x} \in \Sigma^n$ is called an $(m; M, k)$-**thermal-aware sequence** or in short an $(m; M, k)$ **sequence**, if there exists a partition of $[[n]]$ into m mutually disjoint subsets $I_1, I_2, \ldots, I_m$, such that $\bigcup_{i \in [[m]]} I_i = [[n]]$ and for all $j \in [[m]]$, the **complete-projection** of $\boldsymbol{x}$ in I_j, $\mathrm{P}_{I_j}(\boldsymbol{x})$, is an (M, k)-thermal-aware sequence. A set of $(m; M, k)$-sequences is called an $(m; M, k)$-thermal-aware code.*

For simplicity, we consider the case when M and k are positive integers. We observe that if $\boldsymbol{x}$ is an $(m; M, k)$-sequence, there exists a coding scheme over m wires, that the electric pulses are applied on the jth wire on those indices $i \in I_j$, and the maximum temperature over each of the m wires is at most M. Given M, k, we aim to determine $\nu(M, k)$, which is the minimum number of wires necessary to transmit every sequence. We define $\nu(M, k)$ as the following value,

$$\min\left\{m : \boldsymbol{x} \text{ is an } (m; M, k)\text{-sequence for all } \boldsymbol{x} \in \{0, 1\}^*\right\}.$$

Example 3 *Consider $M = 2, k = 1$, and $n = 8$. When $\boldsymbol{x}$ is the all-one sequence of length $n = 8$, we observe that it is impossible to transmit $\boldsymbol{x}$ when there is only one wire. On the other hand, with only one additional wire, there is an efficient coding scheme to transmit $\boldsymbol{x}$ through two available wires so that the maximum temperature on each wire is at most $M = 2$. For example, we can partition $[[n]]$ into two parts, $I_1 = \{1, 2, 5, 6\}$ and $I_2 = \{3, 4, 7, 8\}$, and obtain two corresponding complete-projection sequences as*

$$\mathrm{P}_{I_1}(\boldsymbol{x}) = (1, 1, 0, 0, 1, 1, 0, 0),$$
$$\mathrm{P}_{I_2}(\boldsymbol{x}) = (0, 0, 1, 1, 0, 0, 1, 1).$$

We observe that each complete-projection sequence is a $(2, 1)$-thermal-aware sequence, and hence, $\boldsymbol{x}$ is a $(2; 2, 1)$-thermal-aware sequence.

Remark 1 *We observe that, to decode the transmitted signals, it is not necessary to require every $(m; M, k)$-sequence to share the same m partitions of indices $I_1, I_2, \ldots, I_m$. Since $I_{j_1} \cap I_{j_2} = \emptyset$ for all $j_1 \neq j_2$, a transmitted signal $\boldsymbol{x}$ can be decoded uniquely by implying the bitwise OR over all the sequences. For example, when $m = 2$, if $\mathrm{P}_{I_1}(\boldsymbol{x}) = (1, 1, 0, 0, 0, 1)$ and $\mathrm{P}_{I_2}(\boldsymbol{x}) = (0, 0, 0, 1, 1, 0)$ then $\boldsymbol{x} = (1, 1, 0, 0, 0, 1)$ **OR** $(0, 0, 0, 1, 1, 0) = (1, 1, 0, 1, 1, 1)$.*

Theorem 5 *We have $\nu(M, k) = k + 1$ for all $M > k$.*

Proof: We first show that when $m = k + 1$, for all n, every binary sequence $\boldsymbol{x} \in \Sigma^n$ is an $(m; M, k)$-thermal-aware sequence. Indeed, for all $j \in [[k + 1]]$, we consider $I_j = \{t \in [[n]] : t \equiv j \pmod{k+1}\}$. Then $I_{j_1} \cap I_{j_2} = \emptyset$ for all $j_1 \neq j_2$ and $\bigcup_{j \in [[m]]} I_j = [[n]]$. Furthermore, for all $j \in [[k + 1]]$, the complete-projection of $\boldsymbol{x}$ in I_j is $\boldsymbol{y} = (y_1, y_2, \ldots, y_n)$ where $y_i = 0$ for all $i \not\equiv j \pmod{k + 1}$. Since $\boldsymbol{y}$ is an (M, k)-thermal-aware sequence for all $M > k$, $\boldsymbol{x}$ is an $(m; M, k)$-thermal-aware sequence.

Next, we observe that when $m = k$, the all-one sequence of length n is not an $(m; M, k)$-thermal-aware sequence when n is large enough. Hence, $\nu(M, k) = k + 1$ for all $M > k$. ■

V. CONCLUSION

In this work, we have studied a new coding scheme to control the peak temperature of some electronic devices. We first presented new constraints and investigated the channel that only accepts sequences that satisfy these constraints. Next, we provided some lower and upper bounds of the capacity of the channel and compute the exact capacity in various cases. Finally, we have studied the channel when multiple wires are available to use. Due to the lack of space in this version, we will provide all the definitions, detailed proofs, related works, and further analysis in the full version of this work.

REFERENCES

[1] M. R. Stan and W. P. Burleson, "Bus-invert coding for low power I/O," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 3, no. 1, pp. 49–58, 1995.

[2] S. Ramprasad, N. R. Shanbhag, and I. N. Hajj, "Information-theoretic bounds on average signal transition activity VLSI systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 7, no. 3, pp. 359–368, 1999.

[3] Y. M. Chee, T. Etzion, H. M. Kiah, and A. Vardy, "Cooling codes: thermal-management coding for high-performance interconnects," *IEEE Transactions on Information Theory,* vol. 64, no. 4, pp. 3062–3085, 2018.

[4] J. J. Verboom, C. P. M. J. Baggen, C. M. J. Van Uijen, and E. W. Gaal, "Method of and device for recording information, record carrier, and device for reading the recorded information," US patent 4,930,115, May 1990.

[5] P. P. Sotiriadis and A. P. Chandrakasan, "Reducing bus delay in submicron technology using coding," *in Proc. IEEE Asia South Pacific Design Autom. Conf.,* 2001, pp. 109–114.

[6] P. P. Sotiriadis and A. P. Chandrakasan, "A bus energy model for deep submicron technology," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.,* vol. 10, no. 3, pp. 341–350, 2002.

[7] P. P. Sotiriadis and A. P. Chandrakasan, "Bus energy reduction by transition pattern coding using a detailed deep submicrometer bus model," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.,* vol. 50, no. 10, pp. 1280–1295, 2003.

[8] P. P. Sotiriadis, V. Tarokh, and A. P. Chandrakasan, "Energy reduction in VLSI computation modules: An information-theoretic approach," *IEEE Trans. Inf. Theory,* vol. 49, no. 4, pp. 790–808, 2003.

[9] P. P. Sotiriadis, A. Wang, and A. P. Chandrakasan, "Transition pattern coding: An approach to reduce energy in interconnect," *in Proc. ISSCIRC,* 2000, pp. 348–351.

[10] Y. M. Chee, C. J. Colbourn, and A. C. H. Ling, "Optimal memoryless encoding for low power off-chip data buses," *ICCAD 2006: Proceedings of the International Conference on Computer-Aided Design,* 2006, pp. 369–374.

[11] Y. M. Chee, T. Etzion, H. M. Kiah, A. Vardy, and H. Wei, "Low-power cooling codes with efficient encoding and decoding", *IEEE Transactions on Information Theory,* vol. 66, no. 8, pp. 4804–4818, 2020.

[12] Y. L. Guan, G. Han, L. Kong, K. S. Chan, K. Cai, and J. Zheng, "Coding and signal processing for ultra-high density magnetic recording channels," 2014 International Conference on Computing, Networking and Communications (ICNC), 2014, pp. 194–199.

[13] K. A. S. Immink, "A Survey of Codes for Optical Disk Recording," *IEEE J. Select. Areas Communications,* vol. 19, no. 4, pp. 756–764, 2001.

[14] M. Fukuda, Reliability and degradation of semiconductor lasers and LEDs, Artech House, Boston, 1991, ISBN-10:089006465.

[15] K. A. S. Immink, "Runlength-limited sequences," *Proceedings of the IEEE,* vol. 78, no. 11, pp. 1745–1759, 1990.

[16] C. E. Shannon, "A Mathematical theory of communication," *Bell Syst. Tech. J.,* vol. 27, pp. 379–423, 1948.

[17] T. M. Chien, "Upper bound on the efficiency of dc-constrained codes," *Bell Syst. Tech. J.,* vol. 49, no. 9, pp. 2267–2287, 1970.

[18] W. Sriprad, S. Srisawat, and P. Naklor, "Vieta-Fibonacci-like polynomials and some identities," *Annales Mathematicae et Informaticae*, 2021.

[19] R. Gabrys, H. M. Kiah, A. Vardy, E. Yaakobi, and Y. Zhang, "Locally balanced constraints," 2020 Proc. of International Symposium on Information Theory, pp. 664–669, 2020.

[20] K. A. S. Immink, "Codes for mass data storage systems," Second Edition, ISBN 90–74249–27–2, Shannon Foundation Publishers, Eindhoven, Netherlands, 2004. Available online at: https://www.researchgate.net/publication/239666257

[21] D. T. Tang and L. R. Bahl, "Block codes for a class of constrained noiseless channels", *Inform. and Control,* vol. 17, pp. 436–461, 1970.

[22] W. Kautz, "Fibonacci codes for synchronization control", *IEEE. Trans. Inform. Theory,* vol. 11, no. 2, pp. 284–292, 1965.

[23] B. Marcus, R. Roth, and P. Siegel, "An introduction to coding for constrained systems," arXiv: https://ronny.cswp.cs.technion.ac.il/wp-content/uploads/sites/54/2016/05/chapters1-9.pdf

[24] F. J. MacWilliams and N. J. A. Sloane, *The Theory of Error-Correcting Codes*, North-Holland Publishing Company, 1977.