Chopper PWM-Based Class-D Amplifier

MSc Thesis

By

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Abstract

Class-D amplifiers are widely used in audio applications that require a high power efficiency. A high PSRR is beneficial when the power supply contains significant audio band content. Due to mismatches present in the feedback, these can dominate the PSRR of the class-D amplifier, provided the amplifier has sufficient loop gain. No literature has been found that describes a solution to improving the PSRR and CMRR across the full audio band. This work proposes chopping of the input and feedback resistors in a class-D to address this issue. With this technique's application, a >100dB PSRR and CMRR across the audio band is achieved.

Acknowledgements

I would like to express my gratitude towards Dr. Qinwen Fan assisting and challenging me for the duration of this master thesis. She has helped me greatly this project in realizing where my strengths and weaknesses lie, such that I can improve going into the future. I consider that insight one of the most valuable things I have learned during this project.

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Contents

Chapter 1 : Introduction

1.1 Background

1.1.1 Class-D Amplifier Operation

Class-D amplifiers are widely used in audio applications due to their high power efficiency [1, 2, 3, 4, 5]. A class-D amplifier outputs a pulse train whose average is equal to the input signal [6]. The high-frequency content in the output signal can be attenuated by applying a filter to the output. Because the amplifier's output is a switched signal, little power is dissipated inside the amplifier, and power efficiencies of 90% or higher are commonly achieved [1, 2, 3, 4, 5, 7, 8, 9]. In Figure 1.1, a class-D amplifier is shown in a Bridge-Tied-Load (BTL) configuration, which is a common output configuration [4, 10].

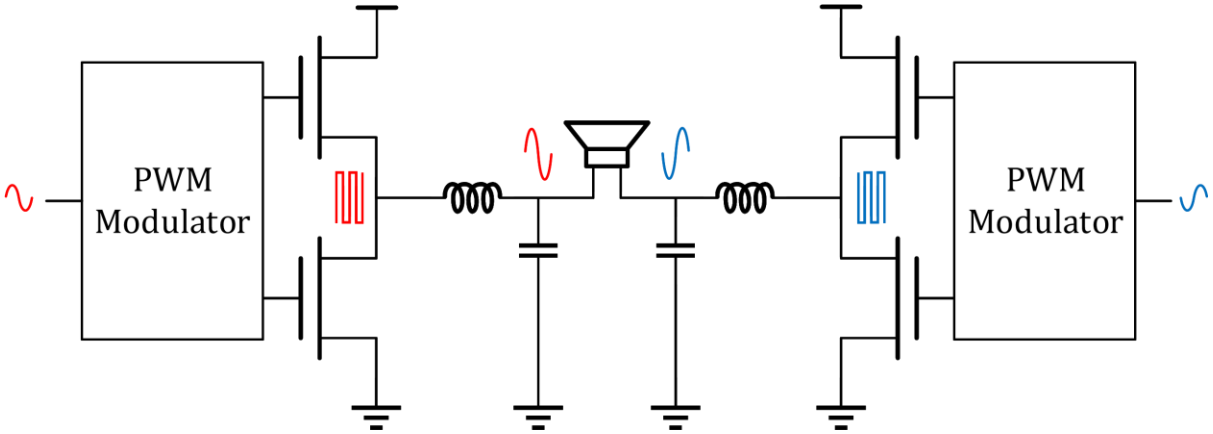

Figure 1.1 : Simplified Class-D Amplifier [4]

Many class-D amplifiers employ pulse width modulation (PWM). This can be implemented by comparing the input signal with a triangle wave reference. For a BTL configuration, there are two typical PWM schemes. The first is AD-PWM (Figure 1.2), where the differential outputs are two complementary PWM pulse-trains, generated from comparing the input signal with the triangle wave reference. The second is BD-PWM (Figure 1.3), generated by comparing two complementary inputs to the triangle wave reference. This results in two non-complementary outputs. In this work, a fully differential Class-D amplifier topology with a BTL configuration is used. The benefits of a fully differential amplifier topology, among others, are a reduction in Total Harmonic Distortion (THD) and an increased Power Supply Rejection Ratio (PSRR) [11].

PSRR is an important requirement for an audio amplifier in certain applications. For example, due to a transmission global system for mobile communications (GSM) signal, a large current is drawn from the supply at 217 Hz in mobile handsets, which causes supply ripple at this frequency [2]. For applications that use multiple audio channels, such as automotive, crosstalk between audio channels can arise due to nonzero impedance in the supply lines and finite PSRR [12]. Dedicated supply regulators [2, 5] or decoupling capacitors can be used to mitigate the power supply ripple. However, this reduces the power efficiency.

Feedback is often applied in an amplifier to mitigate errors introduced in the system [13, 7, 3, 8, 2, 14, 15, 5, 16, 17], such as PSRR and THD. The suppression of errors introduced in the amplifier's output stage is proportional to the amplifier's loop gain. For a class-D amplifier, feedback is often implemented by feeding the class-D output signal into a loop filter, of which the output is then fed into the class-D PWM modulator. The amplifier output and input signals are often fed into the loop filter using resistors connected to one integrator, or multiple cascaded integrators.

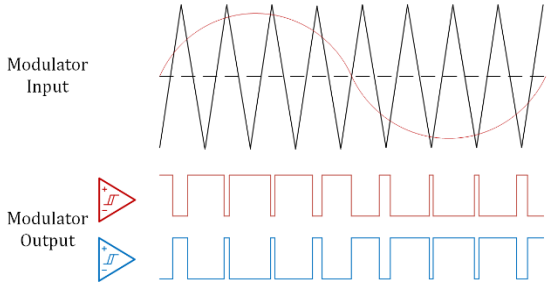

Figure 1.2 : AD-PWM

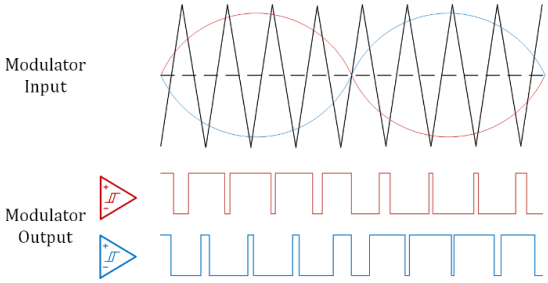

Figure 1.3 : BD-PWM

1.2 Problem Statement

In practice, mismatches between components within the amplifier result in asymmetry in the class-D amplifier's feedback- and input- resistors and degrade the PSRR and common-mode rejection ratio (CMRR).

The size of components that require good matching can be increased to improve the system performance. However, if a PSRR >90 dB with a high yield is required, increasing components sizes leads to an excessive area [2]. In [2, 8], a common-mode feedback loop is introduced to suppress the differential signal resulting from feedback resistor mismatch. Although this technique improves the PSRR and THD at low frequencies, at high frequencies, the performance drops significantly.

1.3 Objectives

The size of components can be increased to improve matching and thus the system performance. Effective methods have been applied in literature to improve the peak PSRR up to 118 dB for low frequencies [2, 8]. However, the highest reported PSRR at 20-20kHz found in literature is 55-65 dB [3, 9, 19, 18], where [5] reports a ~77 dB PSRR from 20-10kHz. This work aims for a PSRR >100 dB from 20-20kHz, at least 20 dB better than state-of-the-art class-D amplifiers across the full audio band [2, 3, 5, 7, 8, 9, 18, 19].

Additional objectives are to improve the CMRR of the amplifier and mitigate the 1/f noise in the audio band while maintaining a competitive Total Harmonic Distortion + Noise (THD+N) and power efficiency relative to other works. lists the target specifications of this work.

Table 1.1 : Target Specifications

Specification	Target
PSRR (20-20kHz)	>100 dB
THD+N (5kHz, 1W)	<-90 dB
SNR (A-weighted)	>110 dB
CMRR (20-20kHz)	>100 dB
Maximum Efficiency	>90%

1.4 Proposed Solution

In this work, as shown in Figure 1.4, dynamic element matching (DEM) of the feedback and input resistors (R_{in} and R_{fb}) of the class-D amplifier's loop filter is applied through choppers. By applying DEM to R_{fb} and R_{in} of the 1st integrator, the mismatches in the system which dominate the PSRR and CMRR are averaged. Furthermore, the operational transconductance amplifier (OTA) in the 1st integrator of the loop filter is also chopped to mitigate it's 1/f noise and offset.

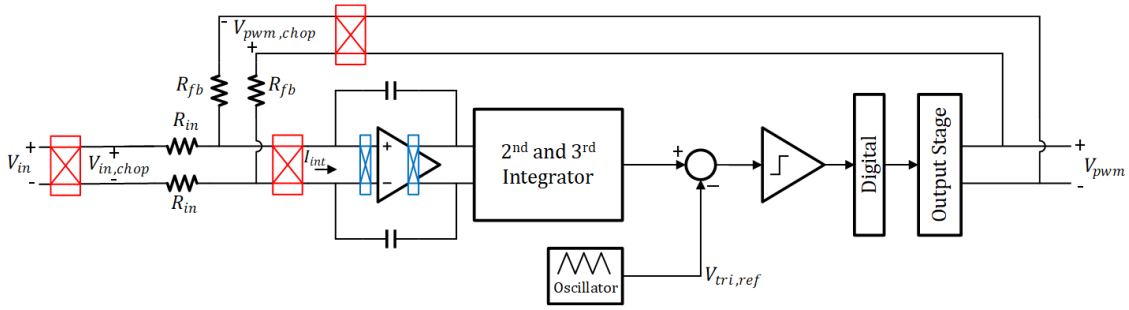

Figure 1.4 : Chopped Class-D Architecture applying DEM to Rin and Rf b and chopping input stage of OTA

The concept of applying DEM using chopping in a class-D amplifier has been proposed in [8]. However, the mismatch in input and feedback resistors is not mitigated in [8], which we address in this work. The main benefit of applying DEM on these signal paths is an improved PSRR and CMRR toward the audio band edge, i.e., 20kHz. This is done by up-modulating the mismatch-related errors to the chopping frequency. However, chopping the PWM signal can also demodulate high-frequency components and degrade THD and PSRR. Chopping the 1st integrator OTA in the loop filter introduces a similar issue [8].

A design challenge of this work is the design of the chopper applying DEM to R_{fb}, connected to the output of the amplifier. The amplifier in this work can produce a PWM waveform with a 14.4 V amplitude. Therefore, the chopper connected to the output should be able to handle these high amplitudes. Most existing high-voltage chopper designs in the literature cannot handle large differential voltages [20, 21], except for [22].

1.5 Thesis Organization

In Chapter 2, the architecture changes made to a baseline design [16] to improve PSRR and CMRR are discussed. The choice of chopping frequency for both the DEM and OTA choppers to achieve high PSRR and low THD is also explained. Chapter 3 details the design of the choppers and the chopper clock generation circuit. Chapter 4 presents the simulation results of the designed amplifier. Chapter 5 concludes the thesis and presents potential improvements for future works.

Chapter 2 : Architecture

2.1 Overview

This chapter explains the architecture of the proposed chopped class-D amplifier. Section 2.2 introduces the baseline amplifier architecture based on the design presented in [16]. Section 2.3 presents the general requirements for the DEM choppers in the system. Section 2.4 shows the effects of mismatches in the DEM chopper on-resistance and defines a mismatch budget for the most critical DEM choppers. Section 2.5 discusses the choice of chopping frequency in regard to PSRR, Signal-to-Noise+Distortion Ratio (SNDR), and Power Supply Induced Intermodulation (PS-IMD) and defines bounds on the choice for the chopping frequency. Section 2.6 summarizes the chapter.

2.2 Baseline Class-D Amplifier Architecture

Figure 2.1 shows the baseline amplifier used in this work [16]. Table 2.1 lists the properties of this amplifier.

Table 2.1 : Basic amplifier properties

Output stage swing	0 - 14.4 V
Modulation scheme	AD-PWM
f_{pwm}	2.1 MHz
Input common-mode voltage	~0.9 V
Output common-mode voltage	~7.2 V
Input peak-peak amplitude	1.8 V

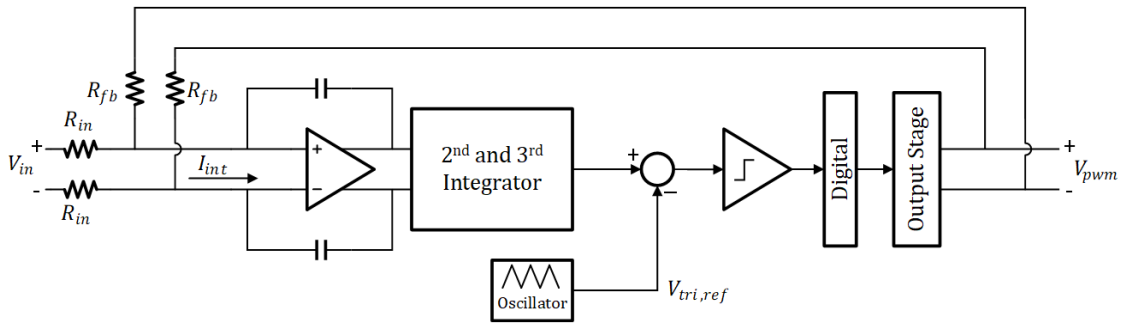

Figure 2.1: Baseline Class-D amplifier [16]

As shown in Figure 1.4, DEM is only applied to the R_{in} and R_{fb} of the 1^{st} integrator, as mismatches in these resistors dominate the PSRR and CMRR. Only the 1^{st} integrator OTA is chopped, as it dominates the 1/f noise and DC offset in the amplifier.

2.3 DEM of Input and Feedback Resistors

In this paragraph, the required DEM chopper clock timing for chopping a PWM signal is established. V_{in} is the differential input signal, $V_{in,chop}$ is the differential input signal after chopping, V_{pwm} is the differential output of the output stage, $V_{pwm,chop}$ is the differential output of the output stage after chopping, $V_{tri,ref}$ is the triangle wave reference used for the PWM modulation and I_{int} is the differential current going into the 1^{st} integrator. The spikes in I_{int} are chopping artefacts from the chopped input and feedback path due to the finite bandwidth of the choppers.

As shown in Figure 2.2, V_{in} and V_{pwm} are chopped at the same time as a peak occurs in the $V_{tri,ref}$ waveform. Because the information of an ideal PWM signal is contained in the pulse widths, no

signal-dependent errors are introduced if the PWM waveform is chopped when the output stage of the class-D is not switching. As is shown in Figure 2.2, the PWM pulses of V_{pwm} are centred around the peaks of $V_{tri,ref}$. Assuming that both V_{pwm} and the chopper modulating V_{pwm} to $V_{pwm,chop}$ have enough bandwidth (covered in 3.2), chopping V_{pwm} does not introduce distortion if the chopping events occur at the same time that the peaks of $V_{tri,ref}$ occur. This means that f_{pwm} should be an integer multiple of $f_{chop,DEM}$, as shown in equation (1).

$$\frac{f_{pwm}}{f_{chop,DEM}} = N,\ N = 1,2,3,\ldots \qquad (1)$$

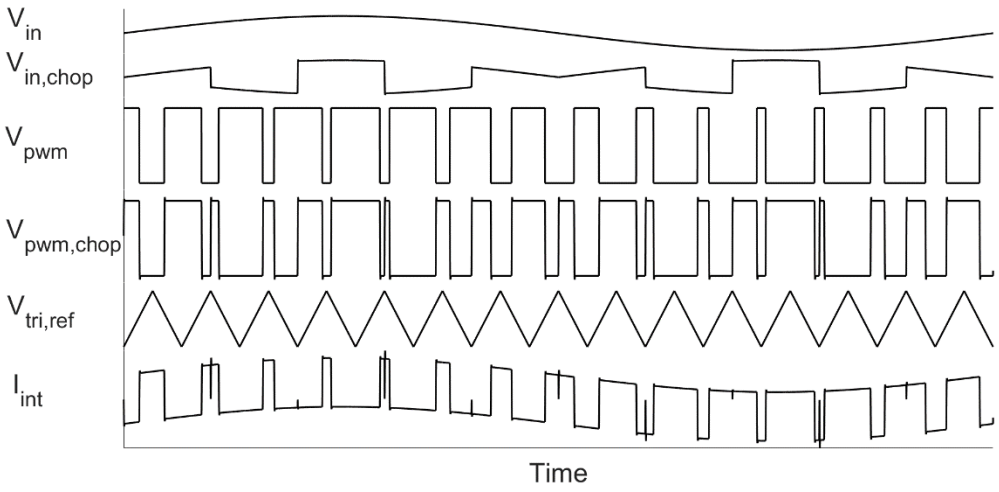

Figure 2.2 : Transients in chopped class-D amplifier

2.4 Random Mismatches in DEM Chopper Switches

2.4.1 Effect of DEM Chopper Switch Mismatches on PSRR and CMRR

When there are no mismatches in the chopper switches, the PSRR and CMRR are mainly defined by the chopper clock's Duty Cycle Error (DCE) and the relative mismatches in R_{fb} or R_{in}. In practice, mismatches will occur between chopper switches. As such, the DEM chopper switches should be appropriately sized to meet the target specifications.

Figure 2.3 and Figure 2.4 show the PSRR and CMRR for a switch on-resistance mismatch ΔR_{on} in one chopper switch according to Periodic Transfer Function (PXF) simulations. $\Delta R_{on,vg}$ is the mismatch in one virtual ground DEM chopper switch, $\Delta R_{on,in}$ is the mismatch in one input chopper switch and $\Delta R_{on,hv}$ is the mismatch in one HV chopper switch. As shown, the mismatches in the DEM chopper at the 1^{st} integrator virtual ground is only dominant at high frequencies. It should be noted that the mismatches in the DEM chopper at the virtual ground are insignificant within the audio band for the same chopper switch ΔR_{on} (see Figure 2.3 and Figure 2.4). Therefore, only the input and feedback chopper mismatches were considered when budgeting for PSRR and CMRR.

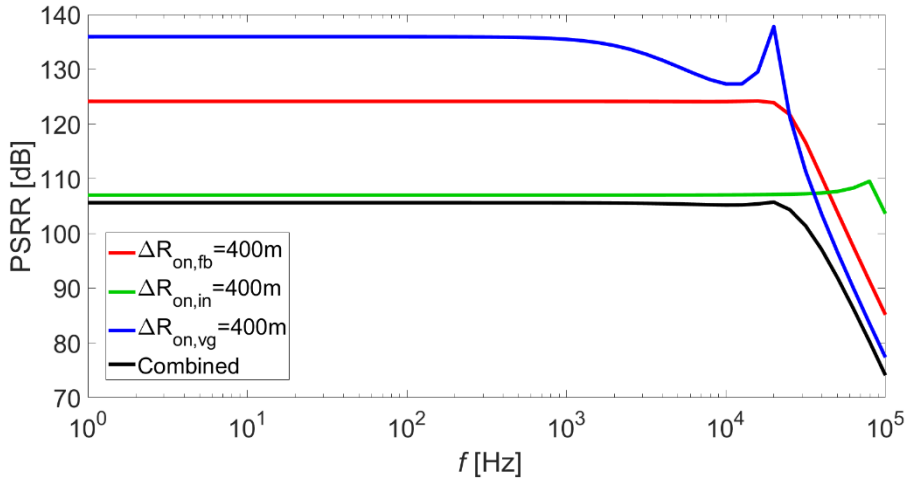

Figure 2.3 : PXF simulation of PSRR in ideal class-D with mismatches in DEM choppers

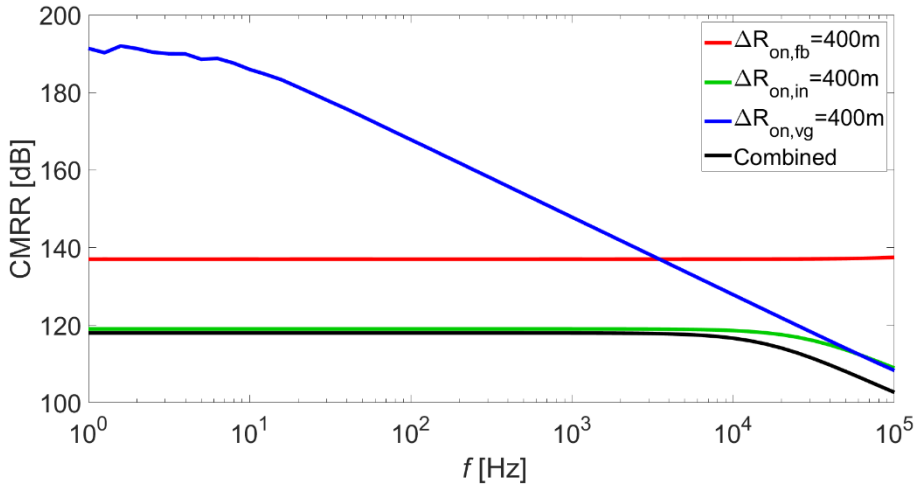

Figure 2.4 : PXF simulation of CMRR in ideal class-D with mismatches in DEM choppers

Assuming $R_{on,vg} \ll R_{in}$, $R_{on,vg}$ can be omitted when approximating the PSRR and CMRR as a function of the chopper mismatches. Figure 2.6 shows the tolerable standard deviation in the input and feedback DEM choppers to meet the target PSRR of > 100 dB, given 1σ and 3σ mismatches, according to the derivation in Appendix 6.1 and PXF simulations. Note that mismatches in the input path also degrades PSRR since the common-mode voltage at the 1^{st} integrator's virtual ground is modulated by the output common-mode. Active common-mode regulation could be used to mitigate this dependence. However, sizing the chopper switches is chosen here for its simplicity. As

shown in Appendix 6.1, the CMRR target can be met if the input and feedback choppers are scaled to meet the PSRR target.

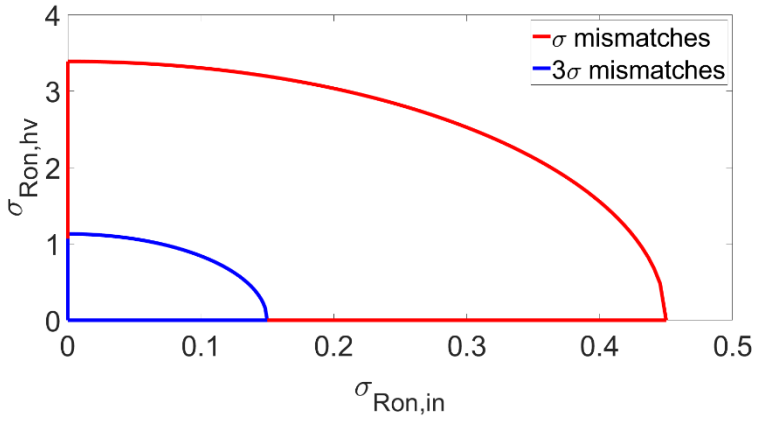

Figure 2.5 : Tolerable $\sigma_{R_{on}}$ of feedback vs input DEM chopper for >100 dB PSRR

2.5 Choice of Chopping Frequency

2.5.1 PSRR Considerations

As stated in Chapter 1, a chopped signal introduces chopping spikes due to the finite bandwidth of the choppers. As a result, signal content around f_{pwm} can be demodulated into the audio band [24].

Figure 2.6 shows the error currents injected into the 1^{st} integrator for an even and odd $f_{pwm}/f_{chop,DEM} = a_{chop}$, with zero and a nonzero input amplitude. The complete 1^{st} integrator input current is shown in Figure 2.2 (for an odd a_{chop}).

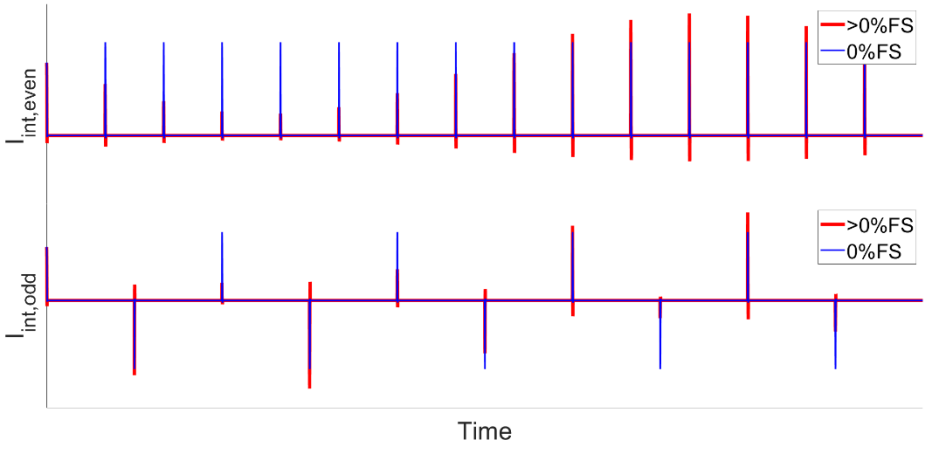

Figure 2.6 : Transients of error current injected in 1st integrator for a_{chop} = 2 and a_{chop} = 3

When analyzing the chopping spikes in Figure 2.6, for an even a_{chop}, a DC component is observed. In Figure 2.7 the spectrum is shown. A baseband component is present for an even a_{chop} but not for an odd a_{chop}. This baseband component is power supply dependent. Therefore, to avoid demodulation of power supply dependent signal components to baseband, a_{chop} should be odd, as shown in equation (2). In Appendix 6.2, this conclusion is drawn based on derivation of the current going into the 1^{st} integrator.

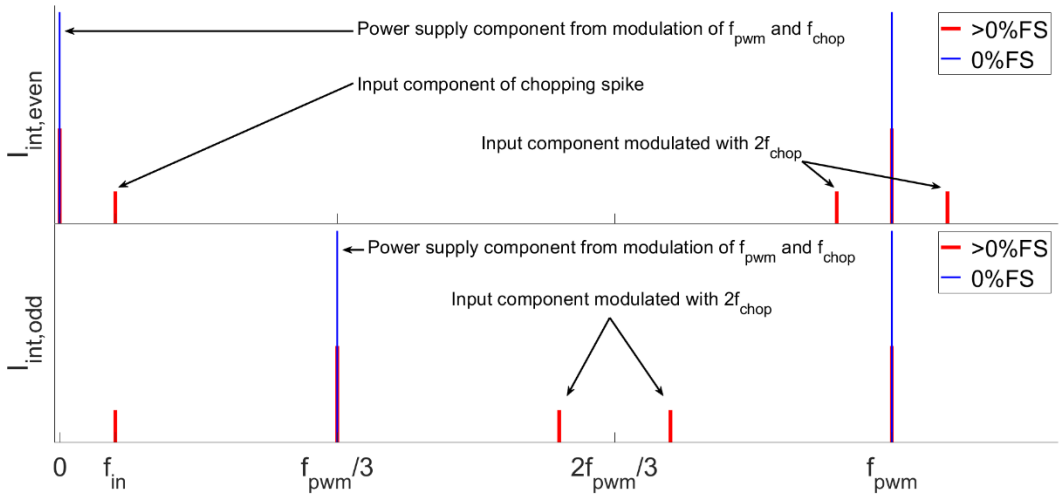

Figure 2.7 : Spectrum of error current injected in 1st integrator for f_{pwm}/f_{chop} = 2 and f_{pwm}/f_{chop} = 3

$$a_{chop} = 2n + 1, n = 1,2,3, \ldots \quad (2)$$

Given the bound for $f_{chop,DEM}$ defined in equation (2), in order to avoid that the power supply ripple modulated around $f_{chop,DEM}$ wraps back into the audio band, equation (3) defines an additional bound for $f_{chop,DEM}$.

$$f_{chop,DEM} > \mathrm{BW_{supp}} + BW_{audio} \quad (3)$$

BW_{supp} is the noise bandwidth of the power supply and BW_{audio} is the audio bandwidth, which is 20 kHz. BW_{supp} is assumed to be at least 20 kHz, in which case $f_{chop,DEM} > 40kHz$. However, it should be noted that it is more desirable to increase $f_{chop,DEM}$ further, as this allows for a more relaxed BW_{supp} requirement, which is in line with the goal of this work. However, as is covered later in this chapter, there are also bounds showing better performance with a decreased f_{chop}. Therefore, besides meeting the hard bounds for $f_{chop,DEM}$ defined so far in equation (2) and (3), a trade-off exists between the application specific tolerable BW_{supp} and the choice of $f_{chop,DEM}$.

In practice, the DEM chopper clock will have a duty cycle error (DCE), which is defined in (4). T_{high} is the time that the clock is high, T_{tot} is the clock period.

$$DCE = |0.5 - \frac{T_{high}}{T_{tot}}| \quad (4)$$

A DCE results in an imperfect cancellation of the mismatches in the feedback and input resistors and can be mitigated by reducing f_{chop}, since it mainly comes from inevitable asymmetric rise and fall logic delays. Also, because the DEM chopper at the class-D output requires a level-shifter to drive the chopper switches, a signal-dependent clock skew occurs in the chopper clock (this is covered in more detail in Chapter 3). This effectively increases the DCE of this DEM chopper clock. When a difference in duty cycle error (DDCE) occurs between the clock of the feedback and virtual ground DEM choppers, a power supply dependent error is introduced. This is shown in Figure 2.8 and Figure 2.9 for the time and frequency domain, respectively. I_{int} is the 1st integrator input current and $I_{int,DDCE}$ is the current with a DDCE. The added error component due to a DDCE shown in Figure 2.8 is marked red. This is the area difference between A_{up} and A_{down}.

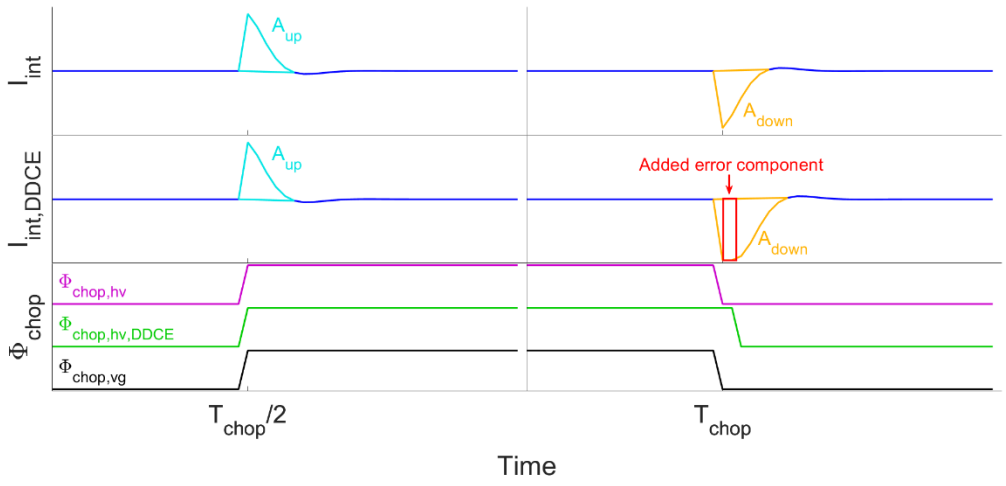

Figure 2.8 : Chopping spikes in 1st integrator w./w.o. a Difference in Duty Cycle Error (DDCE) between DEM chopper clocks

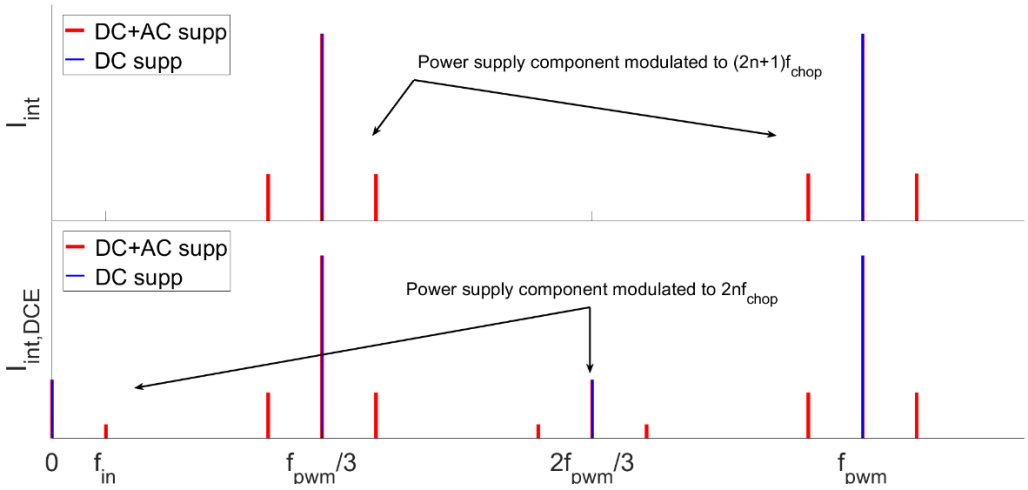

Figure 2.9 : Spectrum of error current injected in 1st integrator with a Difference in Duty Cycle Error (DDCE) between DEM choppers

If no skew is actively applied between the feedback and virtual ground DEM chopper clocks, a DDCE will cause an imbalance between the chopping spikes (Figure 2.8). This results in a power supply dependent error at baseband and odd integer multiples of f_{chop}.

However, the added error signal can be mitigated by balancing the chopping spikes. This can be done by skewing the chopping clock of the feedback DEM chopper relative to the DEM chopper at virtual ground, such that the errors in A_{up} and A_{down} cancel.

In Figure 2.10, the simulated PSRR is shown for a set of DCE in the feedback DEM chopper clock only. In this simulation, the output stage and feedback path are given a finite bandwidth. The rest of the class-D amplifier is ideal. The skew shown in the x-axis is the relative skew applied to the HV chopper clock to average out the introduced DDCE. Note that the best PSRR is found when the chopper timing skew is close to half of the DDCE. This is expected, as this skew shifts roughly half of the error component (Figure 2.8) from A_{down} to A_{up}.

Assuming that the DCE/f_{chop} is constant, the average error introduced with a DDCE can be mitigated with a decreased f_{chop}. However, this does not change that an upper bound exists in the DCE and

the timing skew tolerable between the DEM choppers. Figure 2.10 shows the simulated PSRR using an $f_{chop} = 100\ kHz$. This shows that there is a trade-off between the tolerable DEM chopper clock skew and the DDCE between the DEM chopper clocks.

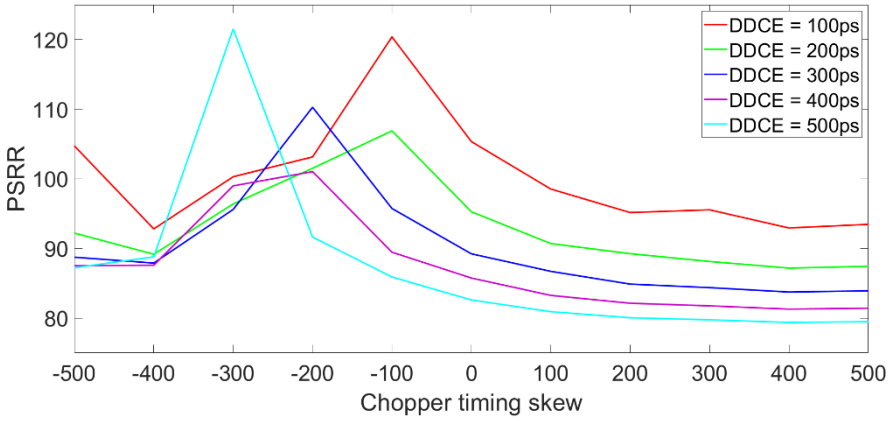

Figure 2.10 : PSRR vs relative chopper clock timing skew and HV chopper DCE/f_{chop} for a 1Vrms power supply ripple at 20kHz

2.5.2 SNDR and PS-IMD Considerations

2.5.2.1 Effect of IR drop at Class-D Output

A practical class-D output stage will have a finite output resistance R_{out}. As a result, due to the current delivered to the load, an IR voltage drop occurs at the output stage's output. This is shown in Figure 2.11. The chopping spike (Figure 2.12) is injected into the 1^{st} integrator. This can cause a degradation in the amplifier's THD.

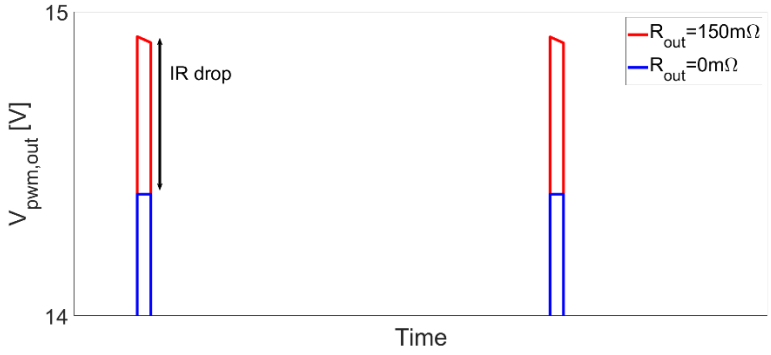

Figure 2.11 : IR drop at output stage due to current drawn by the load

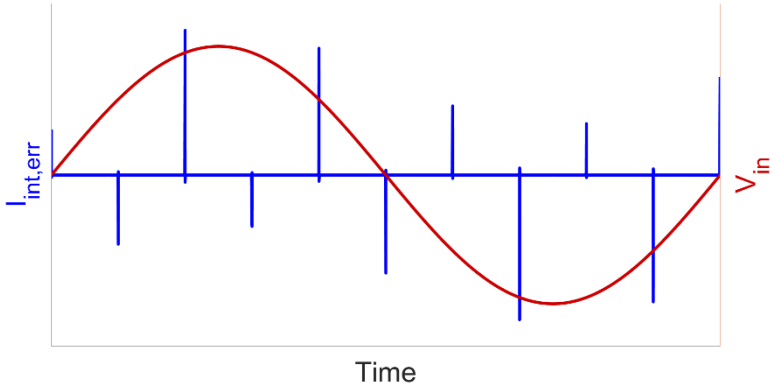

Figure 2.12 : Error current injected into 1st integrator from chopping IR drop

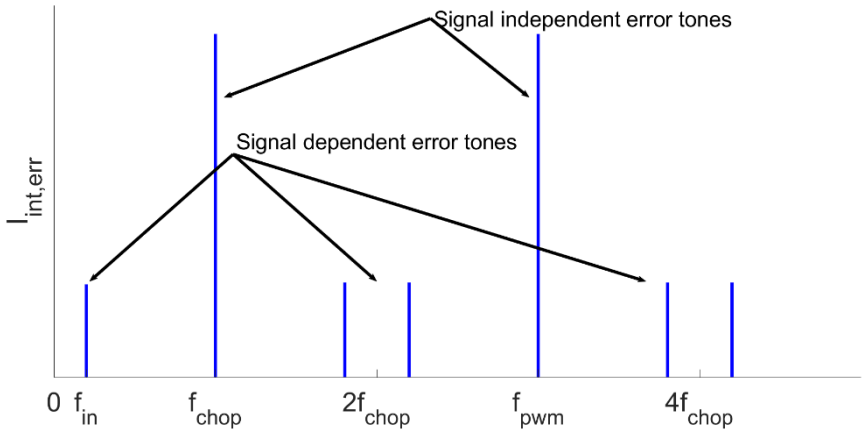

Figure 2.13 : Spectrum of error current injected into 1st integrator from chopping IR drop

In Figure 2.13, the spectrum of the error current (from Figure 2.12) is shown. For simplicity, the IR drop is made to only contain audio band information. The tones at multiples of f_{chop} are the signal independent artefacts from chopping the PWM tone. The signal-dependent content of the IR drop manifests as a baseband tone and also appears at even multiples of f_{chop}. This means that if distortion is present at the output of the output stage, error tones will also appear at harmonics of the input tone. These error tones cannot be mitigated by increasing the loop gain, as they are introduced in the feedback path.

The IR drop's signal content not only contains an audio band signal but can also contain high-frequency ripple. The ripple is visible from the slope of the IR drop shown in Figure 2.11. This high-frequency IR drop can be demodulated into the audio band due to chopping.

Given that the introduced error is due to chopping spikes in the current going into the 1^{st} integrator, this error is also proportional to clock skew between the feedback and virtual ground DEM chopper. This is shown in Figure 2.14, which relates the DEM chopper clock skew and $f_{chop,DEM}$ to the THD. In this simulation, the output stage transistors and drivers are implemented in the schematic so that both the error due to demodulation and the error due to distortion (introduced by the output stage) are included. Also, the feedback resistors to the 1^{st} integrator are modelled with a finite bandwidth (by modelling the resistors as 4 unit resistors in series with a parasitic cap to ground on each end of each resistor). The THD degrades slightly as f_{chop} is increased.

Nominally, there is an LC filter at the output of the class-D (see Figure 1.1) with an L=3.3uH and C=1uF. These values are chosen as they allow for a comparison with [18] and are competitive with [17, 16]. To get a better indication of how the demodulated high-frequency IR drop ripple affects the THD, relative to the low-frequency IR drop ripple, the THD is simulated with varying LC filter component values. The same testbench is used as the one from Figure 2.14. The results are shown in Figure 2.15. Note that at a high LC cutoff frequency f_c, the THD degrades proportional to L. This indicates that chopping the high frequency ripple dominates the added distortion. As Figure 2.14 shows, given the clock skew required to meet the PSRR target (see Figure 2.10), decreasing the chopping frequency is expected to result in a minor improvement in THD.

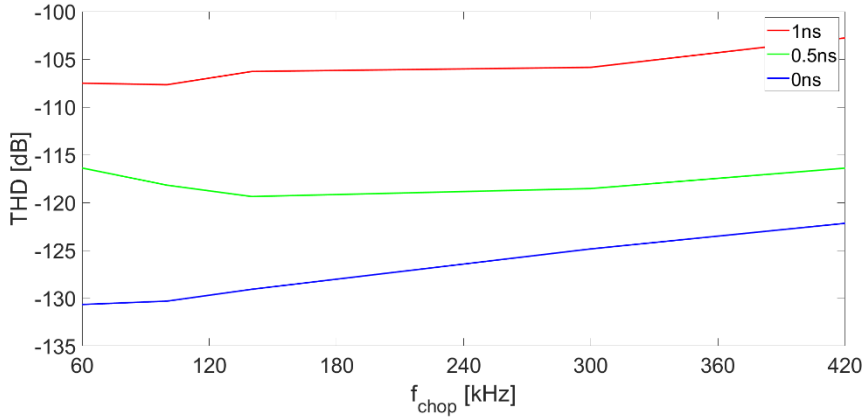

Figure 2.14 : THD vs fchop for relative clock skew between feedback and virtual ground choppers for an input at 85%FS

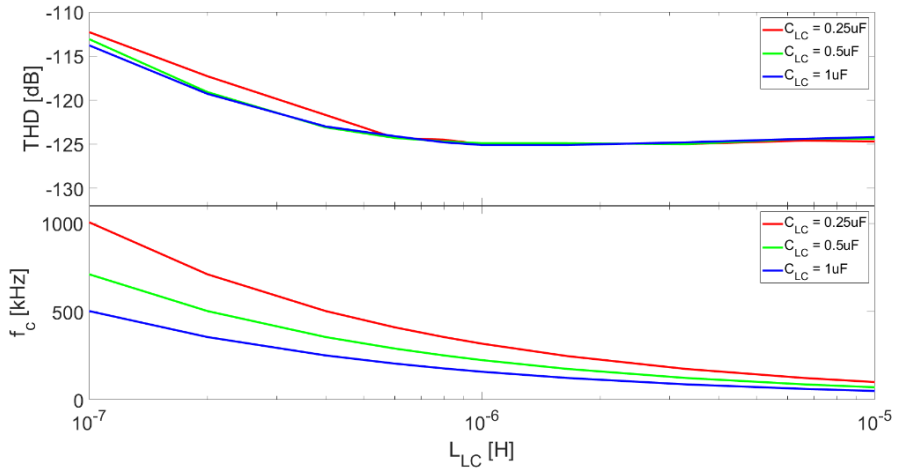

Figure 2.15 : THD vs LC filter cutoff for a 5kHz input at 85%FS with $f_{chop} = 100kHz$ and a 200ps relative chopper clock skew

2.5.2.2 Demodulation of PWM Sidebands from Chopping

It has been established that decreasing f_{chop} can improve the THD. However, there is also a lower bound to be considered due to demodulation. As discussed previously, chopping introduces error spikes containing the input tones, and these tones modulated at even multiples of f_{chop}. However, if there is a DDCE between the DEM choppers, artifacts modulated around odd multiples of f_{chop} will also appear. In order to avoid input tones (within the audio band), modulated around any integer multiples of f_{chop} to wrap back into the audio band, $f_{chop} > 40\ kHz$ is required. Given that a PWM signal also contains sideband components around integer multiples of f_{pwm}, these tones can still be demodulated into the audio band. This is shown in Figure 2.17. Note that this simulation shows an open-loop simulation, with the testbench shown in Figure 2.16.

V_{fb} is the output of a class-D amplifier without chopping and $I_{int,fb}$ is the output of a dummy feedback path with chopping. As such, $I_{int,fb}$ represents the demodulated products that will be present in V_{pwm} when the class-D is chopped.

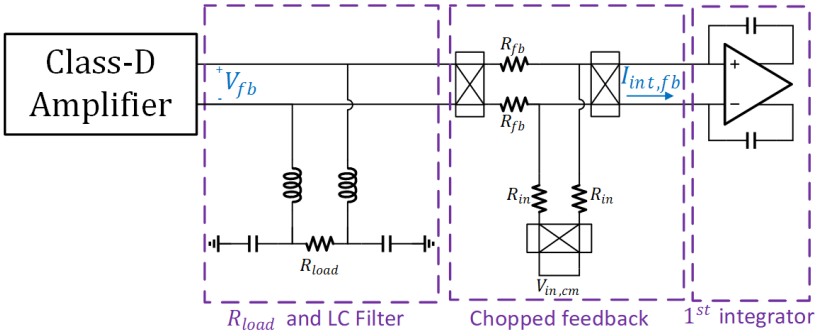

Figure 2.16 : Open-loop testbench for Figure 2.17 *and Figure 2.18 for measuring* $I_{int,fb}$

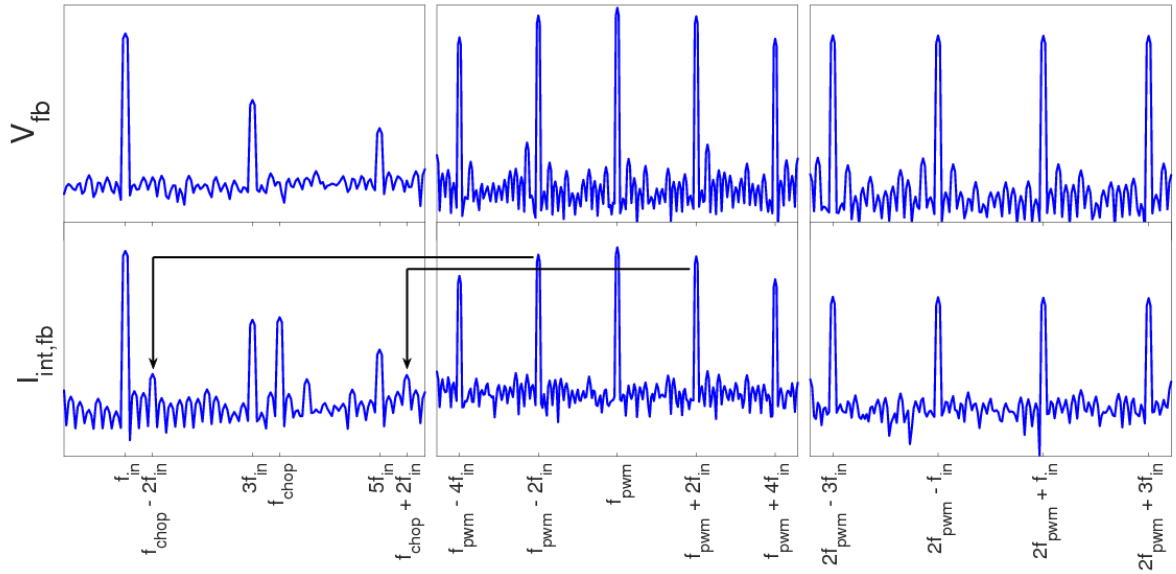

Figure 2.17 : PWM intermodulation due to chopping R_{fb}*, shown at baseband,* f_{pwm} *and* $2f_{pwm}$

2.5.2.3 PS-IMD with Chopped Class-D Amplifier

Another limiting factor for the chopping frequency is power supply induced intermodulation (PS-IMD). Because the output stage of a class-D amplifier essentially operates as a mixer between a PWM waveform and a load driving power supply, modulation products between the power supply ripple and PWM waveform can appear in the audio band. Because these error tones are introduced in the class-D amplifier's output stage, increasing the loop gain will mitigate them [14, 15]. However, chopping causes additional high-frequency PWM tones to be demodulated into the audio band. This is shown in Figure 2.18 (which is also an open-loop simulation). As this occurs in the feedback path, more loop gain will not address this issue.

To obtain a rough approximation if changing $f_{chop,DEM}$ will affect the PS-IMD, the class-D amplifier with a partially schematic-level output stage and schematic-level R_{fb} is simulated. A 200 ps chopper clock skew and 100 ps DDCE between the feedback and virtual ground DEM chopper are applied, which is within the tolerable margin to meet the PSRR target (see Figure 2.10). The THD is simulated with a 20 kHz input tone at 90%FS and $1V_p$ power supply tone with varying frequency f_{ps}, which is shown in Figure 2.19. The PS-IMD doesn't notably improve for $f_{chop} < 100\ kHz$.

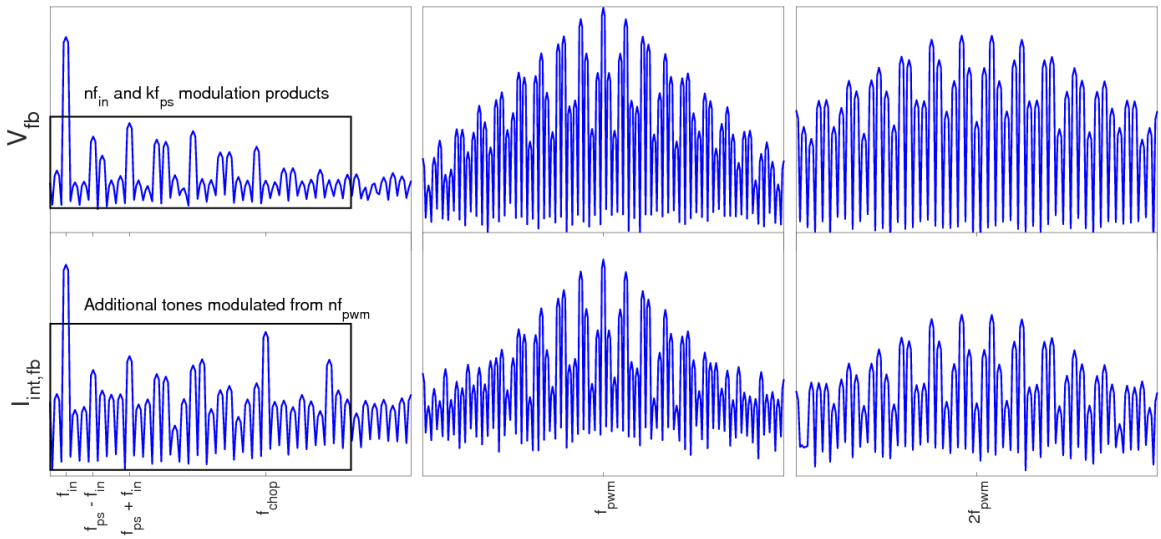

Figure 2.18 : PS-IMD due to chopping R_{fb}, shown at baseband, f_{pwm} and $2f_{pwm}$, *with n and k being integer numbers*

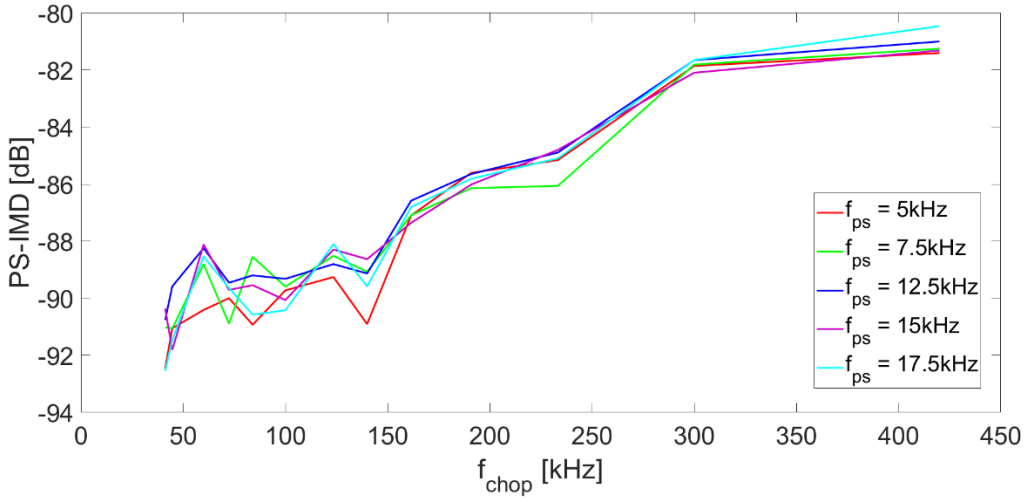

Figure 2.19 : PS-IMD vs $f_{chop,DEM}$ with a 20 kHz input at 90%FS and a 1 V_p supply tone with a frequency f_{ps} and with 100 ps DDCE and 200 ps chopper clock skew applied

2.6 Summary and Conclusions

In this chapter, architecture-level causes of degradation in CMRR, PSRR and THD have been discussed. For an optimal THD and PSRR performance, f_{pwm} should be an odd integer multiple of $f_{chop,DEM}$. Furthermore, although decreasing f_{chop} can have a positive effect on the THD and PS-IMD, no significant improvement is observed for $f_{chop,DEM} < 100\ kHz$ at an architecture-level. However, a clear optimum for f_{chop} is not found. Therefore, f_{chop} is made programmable down to ~63 kHz. Increasing f_{chop} increases the allowed power supply bandwidth, which is in line with the overriding objective of this thesis. $f_{chop,DEM} = 100\ kHz$ is used for further simulations in this thesis, allowing for ample margin in the allowed power supply bandwidth. $f_{chop,OTA}$ will be defined in Chapter 3, where the modifications to the loop filter 1^{st} integrator OTA are covered.

Chapter 3 : Circuit Design

3.1 Overview

This chapter explains the design of the components introduced in this work. In Section 3.2, the sizing of R_{in} and R_{fb} is detailed. In Section 3.3, the modifications to the OTA used in [16] are covered. The choice of chopping frequency $f_{chop,OTA}$ (given the chosen $f_{chop,DEM}$ in Chapter 2) is also discussed.

In Section 3.4 the design of the DEM chopper at the loop filter 1^{st} integrator virtual ground is covered. In Section 3.5, the DEM chopper at the input is covered. In Section 3.6, the design of the high voltage (HV) chopper is discussed. The chopper clock skewing circuit, which adjusts the skew across process and temperature corners without trimming, is covered in Section 3.7.

3.2 Effect of PWM and Chopping Edge Interactions

So far, it is assumed that the chopping spikes and PWM edges do not interact with each other. As stated before, this means that only the signal-dependent components due to the IR drop at the output stage being chopped result in increased THD+N. However, if the bandwidth of the implementation of the feedback resistors in the loop filter is too low, this assumption is not valid. In Figure 3.1 a chopped PWM pulse is shown, with the finite bandwidth of R_{fb} modelled as mentioned for Figure 2.14. The parasitic capacitors coupled to the ground are C_{par}. To get an indication of how this effect will degrade the THD+N, a simulation is done using this modeled feedback resistor and using the same partial schematic-level output stage as used in Figure 2.14. No DDCE is modeled, and the rest of the class-D amplifier is ideal. Note that the clock of the feedback chopper is skewed to compensate for the signal delay introduced due to the finite bandwidth of the feedback resistor. This compensation delay is roughly equal to the 50% settling time of the chopped signal.

Figure 3.2 shows the THD versus the signal amplitude. Here it is shown that the point of heavy degradation in THD occurs at lower amplitudes, dependent on the R_{fb} internal bandwidth. For this reason, the implementation of R_{in} and R_{fb} are given a minimum width to maximize their bandwidth, thus maximizing the THD at high amplitudes.

The same simulation is run with these resistors replaced with the same type of resistors used in the final design. These consist of unit resistors R_{unit} with a minimum width and with the same width used in [16]. The results are shown in Figure 3.3. Note that by scaling the resistors down, the THD does not drastically degrade up to almost 100%FS. This validates the assumption that the PWM and chopping edges do not interact significantly. However, scaling the resistors down poses a trade-off between optimizing the THD at low signal amplitudes and increasing the amplitude for which the THD will drastically degrade. As shown in Figure 3.3, at room temperature, the linearity of the resistors degrades notably with a decrease in size. This has little effect on the THD for the feedback path, as the signal is dominantly a 2-level signal. Therefore, scaling R_{in} causes this degradation. Nevertheless, this distortion is significantly better than the target specification, so the performance with minimum sized input and feedback resistors is chosen due to the increase in performance at high amplitudes.

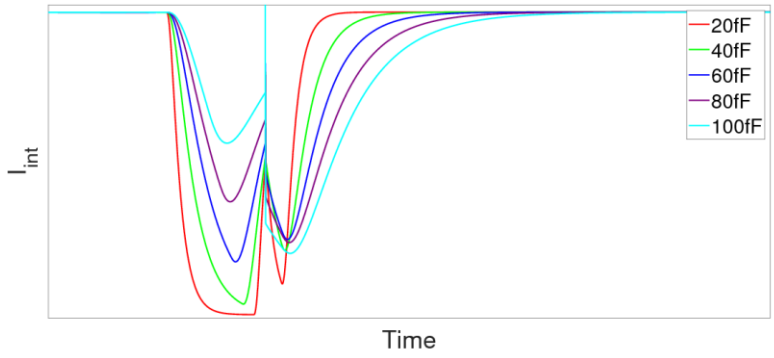

Figure 3.1 : Effect of modelled parasitic capacitance Cpar in Rf b on PWM waveform

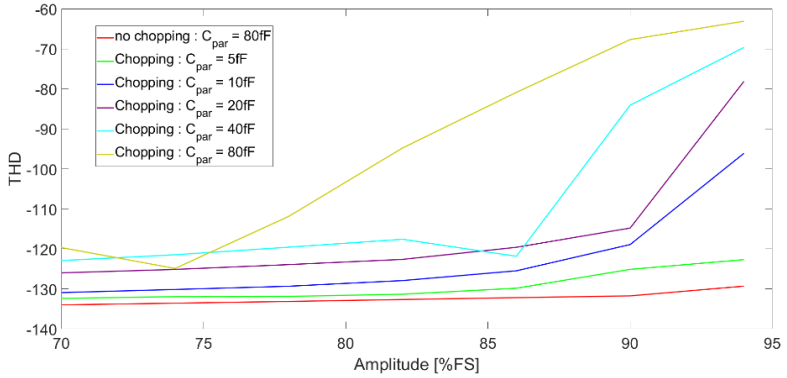

Figure 3.2 : THD vs Amplitude for varying Rfb bandwidth with $f_{chop} = 100\ kHz$

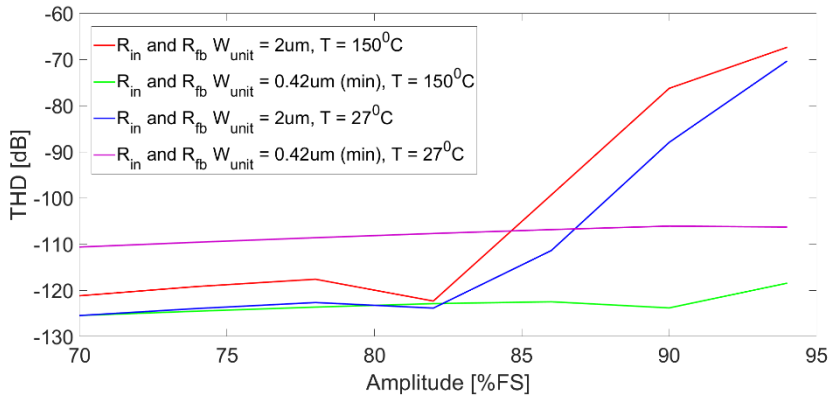

Figure 3.3 : THD vs Amplitude using schematic-level R_{in} and R_{fb} with f_{chop} = 100 kHz

3.3 Chopped OTA Design

3.3.1 Baseline OTA

Figure 3.4 shows the baseline OTA used in this work. It is a two-stage OTA that uses a capacitively coupled feed-forward frequency compensation [17].

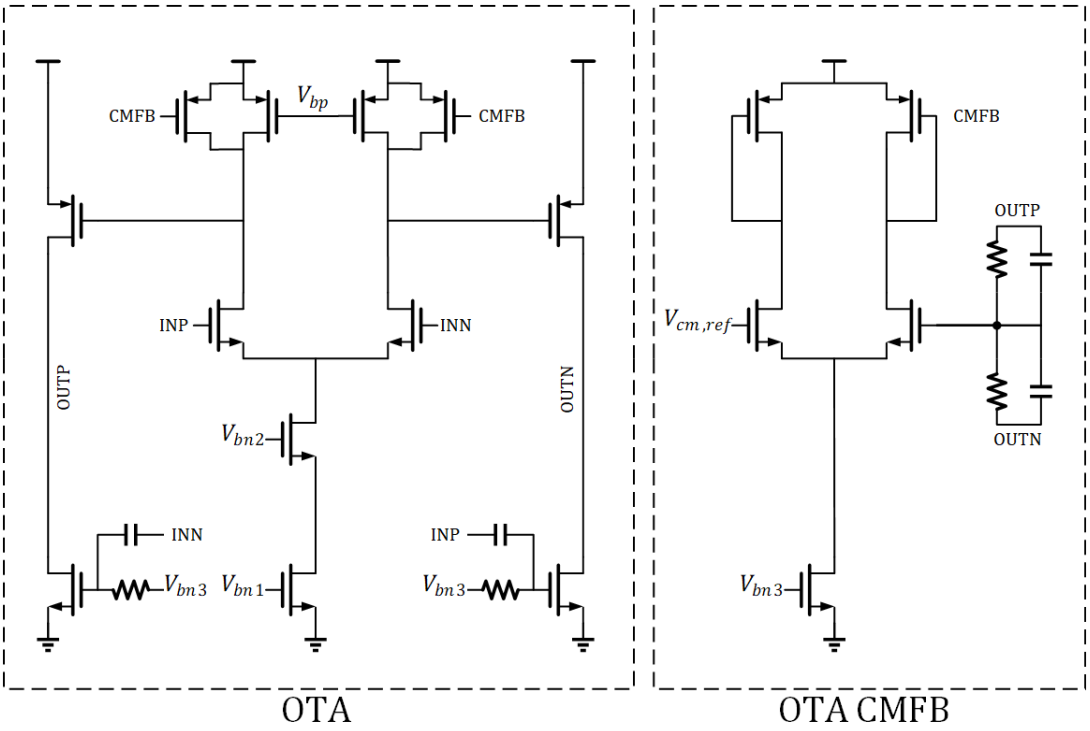

Figure 3.4 : Baseline OTA design

3.3.2 Chopped OTA in 1^{st} Integrator

In order to mitigate the 1/f noise and input-referred offset of the 1^{st} integrator OTA, the 1^{st} stage of the OTA is chopped. The location of the choppers is shown in Figure 3.6. The OTA with implemented choppers is shown in Figure 3.7. To reduce the magnitude of chopping spikes, only the first stage in the low-frequency path is chopped. Because the choppers only process small differential voltages, they are implemented using transmission-gates.

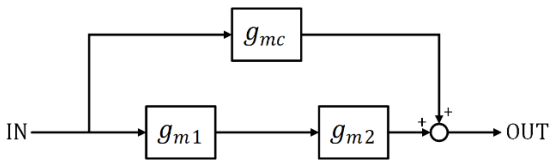

Figure 3.5 : Baseline OTA Diagram

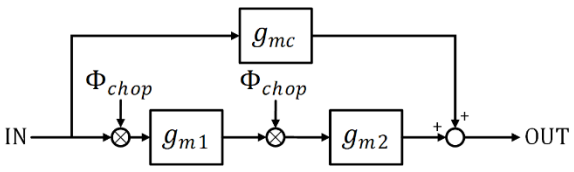

Figure 3.6 : Chopped OTA Diagram

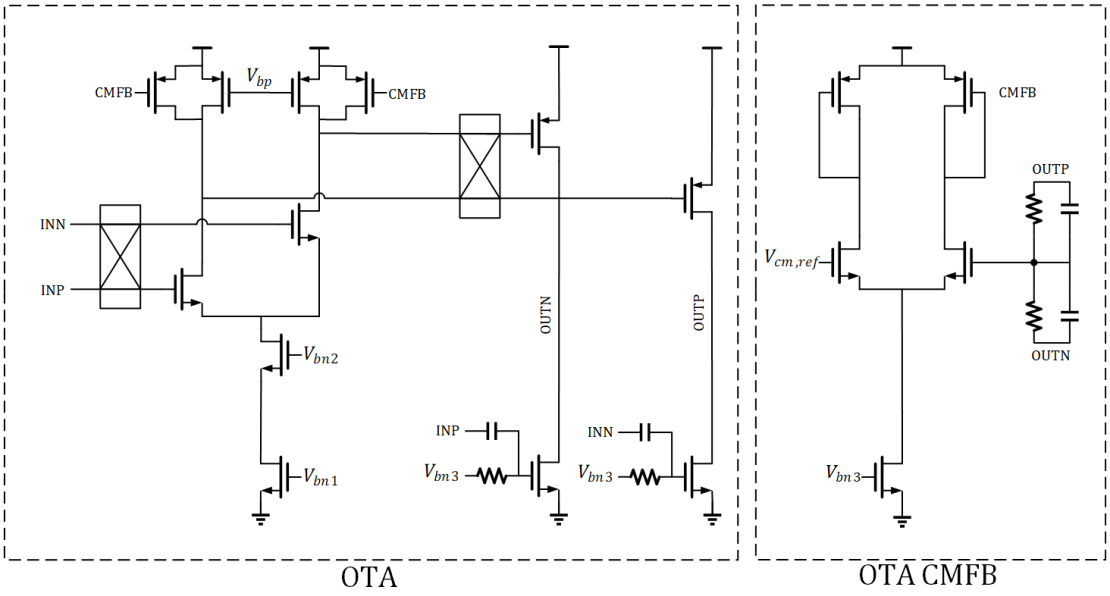

Figure 3.7 : Chopped OTA Design

3.3.3 Sizing of OTA Input Transistors and Choppers

In [24, 25], a similar chopped OTA design is analyzed. [25] shows that at each chopping edge, an "error" charge $Q_{err} \approx 2V_{vg}C_{g_{m1}}$ is injected at the OTA input, where V_{vg} is the voltage at OTA input and $C_{g_{m1}}$ is the input capacitance of g_{m1}. V_{vg} contains high frequency ripple originating from the class-D output, which is proportional to $V_{pwm,out}$. This results in the following output referred error $V_{out,err}(t)$:

$$V_{out,err}(t) \propto I_{int1,err}(t) \propto V'_{pwm,out}(nT_{chop,OTA}/2)C_{gm1}f_{chop,OTA}, \text{ n = 1,2,3,...} \quad (5)$$

$V_{pwm,out}{}'$ is the high frequency content of $V_{pwm,out}$. Equation (5) shows that $V_{out,err}(t)$ can be decreased as the input pair area, which is proportional to C_{gm1}, is decreased. However, as the input pair is scaled down, the dc gain of the first stage is reduced. In Figure 3.8, the open-loop gain of the OTA is shown for various f_{chop}. The input stage W and L are also scaled with a factor S_{in}. The unit W = 32um and L=1um.

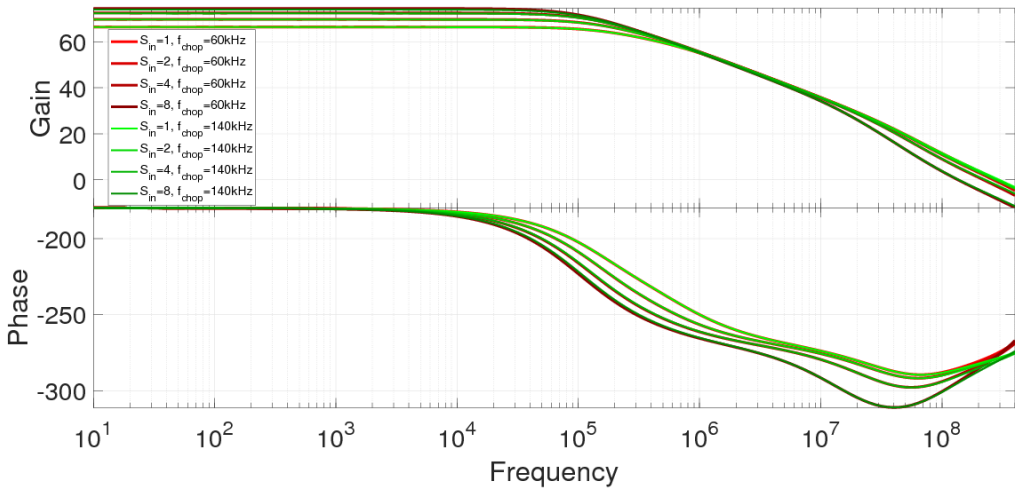

Figure 3.8 : OTA open-loop gain and phase for varying chopping frequency and scaled input stage with scaling factor S_{in}

Figure 3.8 shows that $f_{chop,OTA} < 140\ kHz$ has a neglectable effect on the OTA DC gain and bandwidth for $1 < S_{in} < 8$. However, the DC gain does degrade with a decreased S_{in}. To see how the class-D THD is affected due to the demodulation of high-frequency ripple at the virtual ground, a simulation is performed with a schematic-level 1st integrator OTA, R_{in} and R_{fb} and partial schematic-level output stage (drivers and output switches in schematic). This is shown in Figure 3.9.

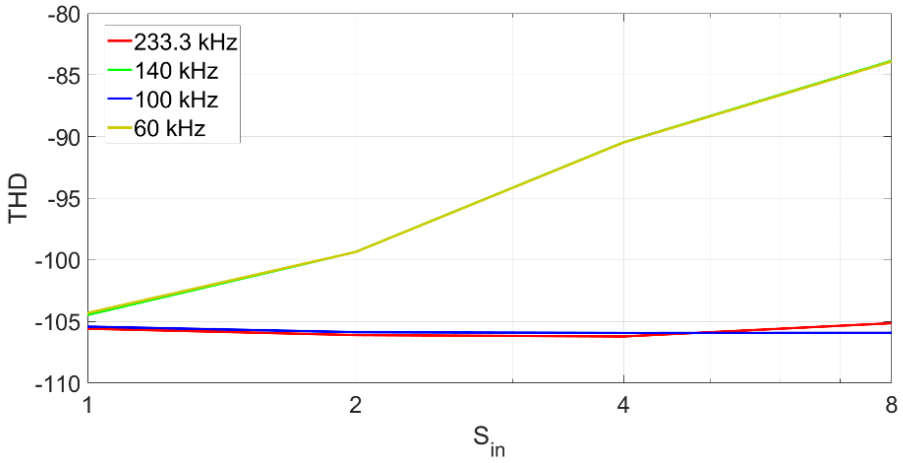

Figure 3.9 : THD vs input stage scaling factor Sin for varying $f_{chop,OTA}$, given $f_{chop,DEM} = 100\ kHz$, simulated at 27^0C

A large discrepancy in THD performance is observed between $f_{chop,OTA} = 60kHz/140kHz$ and $f_{chop,OTA} = 100kHz/233.3kHz$. To explain this, the frequency contents of $I_{int1,err}$ are considered. $I_{int1,err}$ is proportional to the chopped PWM waveform, sampled at $2f_{chop,OTA}$ (see Equation (5)). A more detailed equation is shown in Appendix 6.4. Given that the chopped PWM waveform contains frequencies around odd multiples of $f_{chop,DEM}$, with $f_{chop,OTA} = 60kHz$, a tone is expected at $2f_{chop,OTA} - f_{chop,DEM} = 20kHz$. The same applies for $f_{chop,OTA} = 140kHz$. Applying the same reasoning, no tone demodulates in the audio band when $f_{chop,OTA} = 100kHz/233.3kHz$ is used. Figure 3.10 shows a class-D THD sim confirming this.

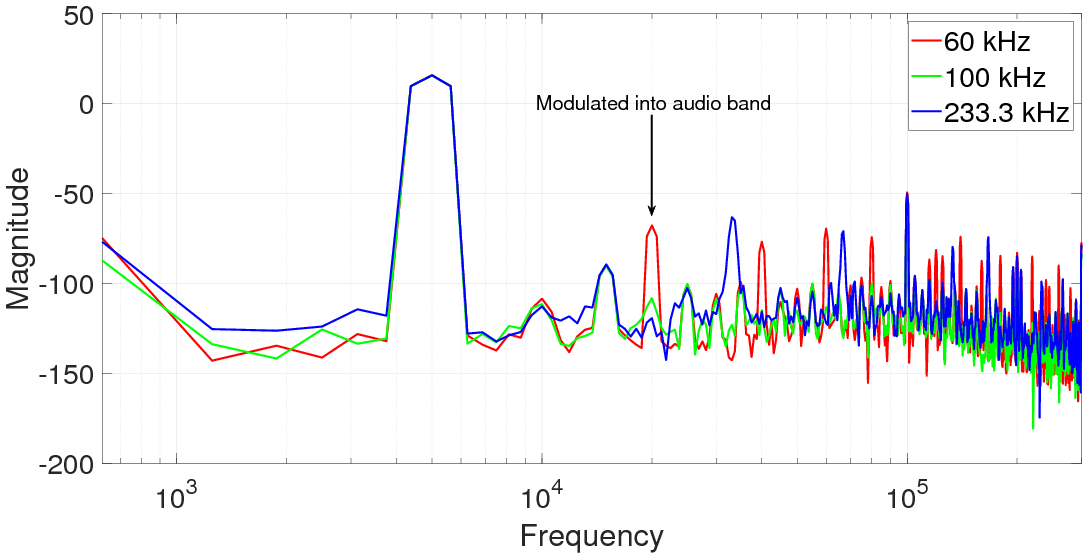

Figure 3.10 : Spectrum of class-D output for varying $f_{chop,OTA}$, given $f_{chop,DEM} = 100\ kHz$

Because $f_{chop,OTA} = f_{chop,DEM}$ (= 100 kHz) doesn't demodulate additional error tones from the PWM output into the audio band, a nominal $f_{chop} = 100\ kHz$ is used for both. However, both frequencies are made programmable down to $f_{chop} \approx 63\ kHz$ by means of a frequency divider of

the clock derived from the PWM reference oscillator (see Appendix 6.6). $f_{chop,OTA}$ can be programmed to either mirror $f_{chop,DEM}$ or default to 100 kHz. The second option allows for observing the demodulation effect covered in this section. Because no degradation in THD is observed in Figure 3.9 for $S_{in} \geq 2$ at $f_{chop} = 100\ kHz$, $S_{in} = 2$ is chosen.

To confirm that the 1/f noise is non-dominant in the audio band for an $f_{chop,OTA} = 100\ kHz$ and $S_{in} = 2$, a periodic noise simulation of the class-D amplifier is performed. The loop filter is implemented in a schematic while the rest of the class-D is kept ideal. Figure 3.11 shows the noise density. When chopping, the dominant 1/f noise is up-modulated outside of the audio band.

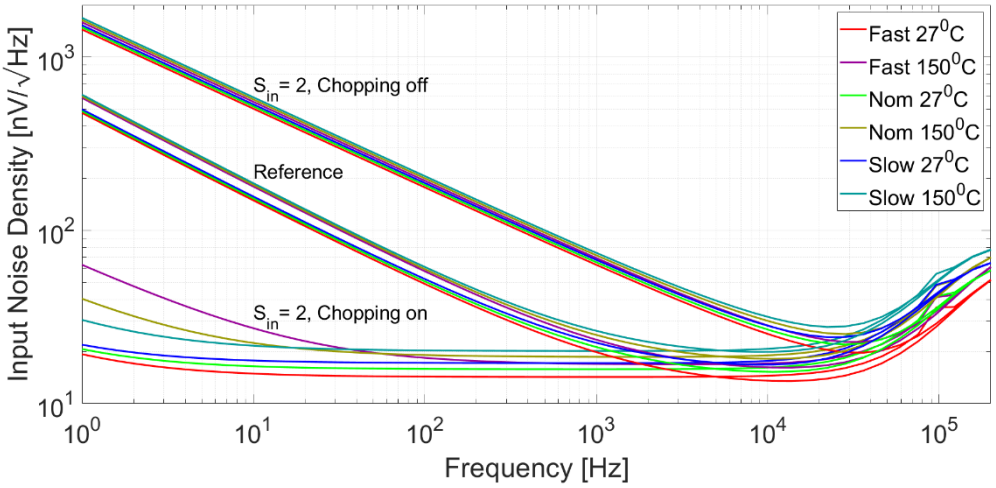

Figure 3.11 : Periodic noise simulation with scaled OTA (with and without chopping) and the reference OTA used in [16] for varying process and temperature corners

3.4 DEM Chopper at Virtual Ground

Because the DEM chopper at virtual ground experiences a small signal swing, transmission gates are used to implement the chopper switches. As the virtual ground common-mode voltage is ~1.6V, the NMOS transistors of the transmission gate are only active during startup. Therefore, they are made minimum size, to minimize charge injection into the virtual ground. The PMOS transistors are scaled for THD and PSRR.

The PSRR is improved by decreasing the chopper switch mismatches, which can be done by scaling the switches' area [23]. The THD can be improved by decreasing the differential voltage across the chopper switches. Both parameters are therefore improved by scaling the width of the PMOS transistors (W_p). Figure 3.12 shows a simulation of the PSRR (at 20kHz) of the amplifier versus W_p, modelling 3σ switch mismatches in the chopper (see Appendix 6.3). Figure 3.13 shows a simulation of the THD with a 5kHz input signal at 90%FS of the amplifier versus W_p. Both simulations are done with the loop filter and output stage transistors and drivers in a schematic. The rest is ideal.

$W_p = 18\mu m$ is chosen. This gives >15dB margin to ensure that the THD+N target is met after layout and gives ~6 dB margin to meet the PSRR target.

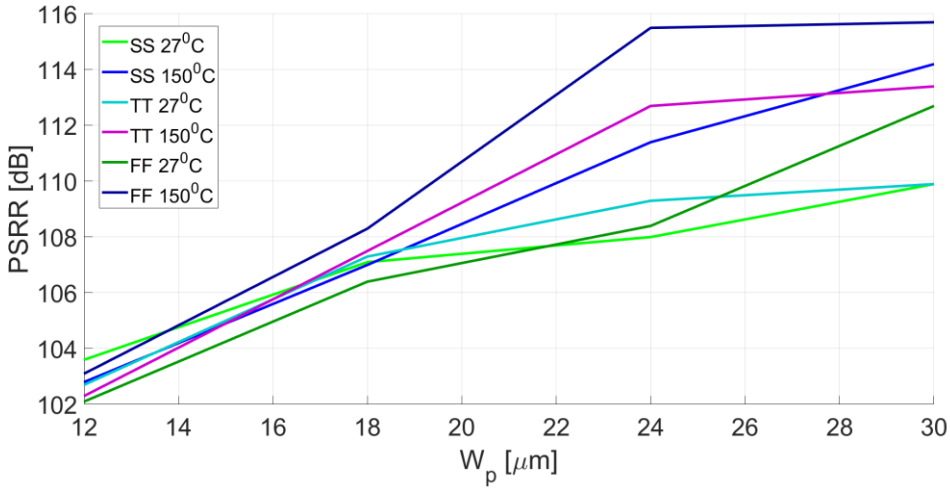

Figure 3.12 : PSRR vs DEM chopper pmos width for varying process and temperature corners

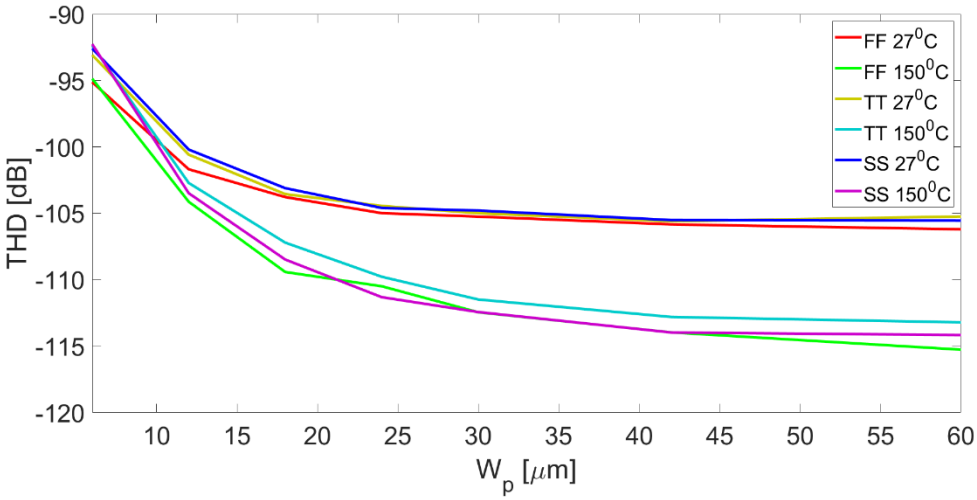

Figure 3.13 : THD vs DEM chopper pmos width for varying process and temperature corners

3.5 Input Chopper

Because the input signal has a large signal swing, a boot strapped switch [26, 27, 28] is used. Due to the presence of parasitic bonding wire inductances [1, 17] at the LV supply, a common-mode supply ripple occurs at f_{pwm} due to a large dI/dt. This can result in the on-chip input voltage becoming lower than AVSS (Figure 3.14), causing the switch overdrive voltage to become positive when it is off. This causes increased leakage in the switch, which can degrade the THD.

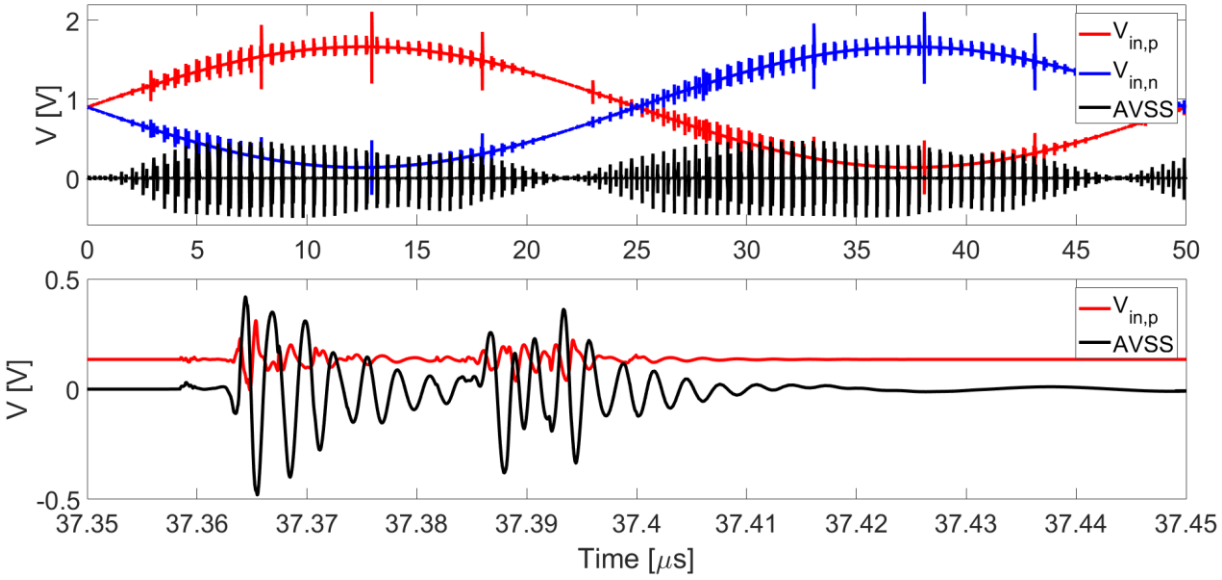

Figure 3.14 : Class-D on-chip single ended inputs and AVSS with bonding wire ringing

Figure 3.15 shows the bootstrapped T-switch used in this work, inspired by [29, 30], which mitigates the leakage through the switch compared to [26, 27, 28].

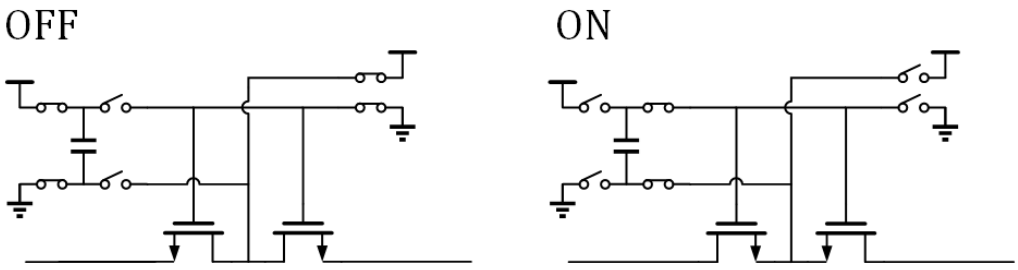

Figure 3.15 : Bootstrapped T-switch

Note that the bootstrapped T-switch does not provide a better leakage under all circumstances. Figure 3.16 shows a DC sim relating the current leakage I_{leak} through a single NMOS switch and T-switch to the voltage across the switch V_{switch} with a common-mode supply increase V_r. The same common-mode voltage as at the class-D input is applied on each end of the switches, which is 0.9V.

The single NMOS switch has an increased leakage, as $|V_{switch}|$ increases. However, the T-switch also notably leaks at the side that approaches 0 V, observed when V_{switch}< 0 V. Because the drain of the T-switch NMOS is made AVDD when off (see Figure 3.15), a leakage from AVDD through one of the switches occurs. This leakage is dependent on the voltage across the NMOS, making it signal-dependent.

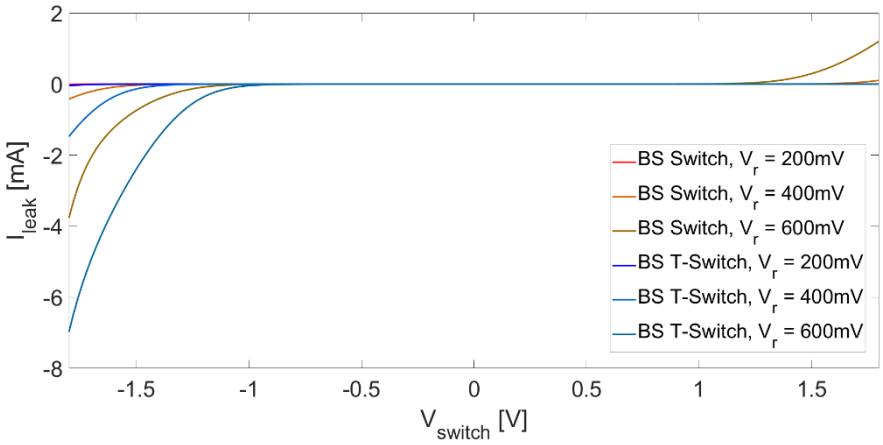

Figure 3.16 : DC sim of I_{leak} vs V_{switch} for an applied V_{ripple} at the gate (and bulk) in fast corner at 150^0C

However, it is observed that the class-D amplifier with the input chopper implemented with boot strapped T-switches maintains a higher THD than a conventional bootstrapped switch for the same switch W/L when the common-mode supply ripple $V_{ripple,p}$ can go beyond V_{in} (see Figure 3.17).

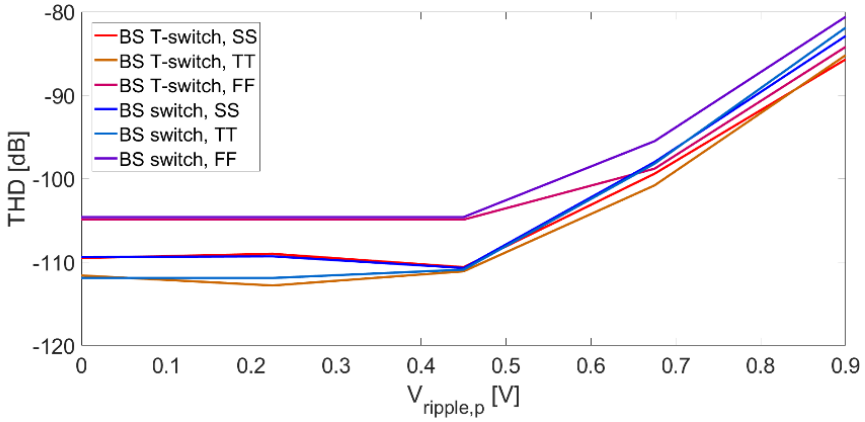

Figure 3.17 : THD vs peak bonding wire ripple with a 5kHz 80%FS input signal simulated at 150^0C

The width of the switches is sized to meet the THD+N target. The approximated chopper mismatch standard deviation for this switch size is $38.5\ m\Omega$ (see Appendix 6.3). With the 3σ mismatches of only this chopper, a 123 dB CMRR and 112 dB PSRR are approximated (see Appendix 6.1). Including the PSRR simulated for the DEM chopper at virtual ground, this leaves ~5 dB PSRR margin for mismatches in the HV chopper and PSRR degradation from a DDCE between DEM choppers.

Figure 3.18 shows the T-switch and its driving circuit, similar to the driving circuit used in [27]. M_1 and M_3 are added to implement the T-switch. M_6 is a single 5V transistor, which replaces the 2 series transistors in [27], to ensure that the V_{ds} and V_{db} of the transistor do not exceed the rated limit.

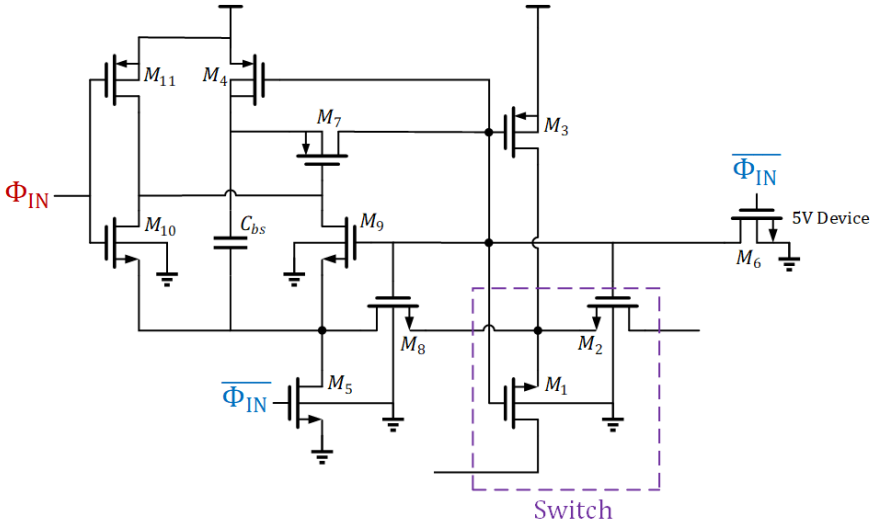

Figure 3.18 : Bootstrapped T-switch Implementation

3.6 Output High Voltage Chopper

3.6.1 Introduction

Because the DEM HV chopper at the output must operate with a 0 – 14.4V fast switching PWM waveform, it is implemented using HV NMOS switches, which are driven by a level-shifted clock. The switch design and sizing are covered first. After which, the level-shifter+driver design is detailed. Lastly, the implementation of the regulators used to power the level-shifter and drivers is covered. The implementation of the chopper in layout is also addressed.

3.6.2 Choice of Switch Device Type and Sizing

The HV chopper must be implemented with HV MOS devices connected back-to-back to block the conduction path through the body diode [22]. Two NMOS topologies are considered, shown in Figure 3.19 and Figure 3.20. When implementing these switches in a chopper, two potential topologies are obtained. These topologies are shown in Figure 3.21 and Figure 3.22.

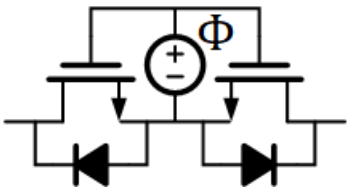

Figure 3.19 : HV switch in common-source configuration

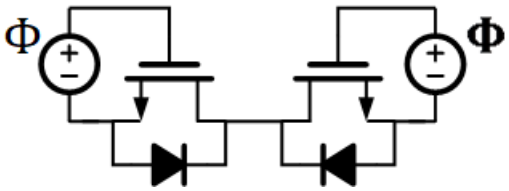

Figure 3.20 : HV switch in common-drain configuration

Both chopper topologies require four level-shifters and the same amount of switches. However, the common-drain chopper topology requires the switch drivers of each level-shifter to only charge 1 gate capacitance C_{gate} per clock phase $\Phi/\overline{\Phi}$, whereas the common-source topology requires $2C_{gate}$ to be charged. This makes the common-drain configuration more attractive as it loads the bootstrapped source less.

The class-D linearity is better when using a common-drain configuration with the HV switch devices used. Figure 3.23 shows a THD simulation with ideal switch drivers (see Figure 3.19 and Figure 3.20). Because the common-drain configuration was chosen at an early stage for the first mentioned benefit, this was observed at a late design stage. Therefore, the reason for this discrepancy is not yet well understood, which should be investigated in future works.

Because there is no mismatch model for the HV NMOS devices used, the mismatches are approximated using a similar HV device (see Appendix 6.3). Because this carries the risk of the results being invalid, the switches are scaled with significant margin to ensure that the PSRR target is met. Therefore, they are given a width $W_{switch} = 200\mu m$ (L_{switch} is fixed).

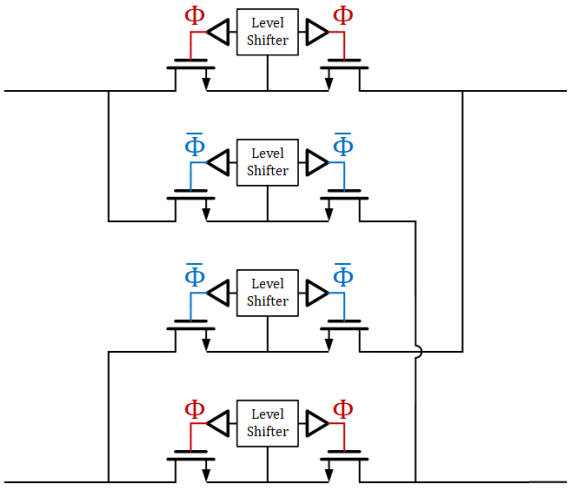

Figure 3.21 : HV chopper using switches from Figure 3.19

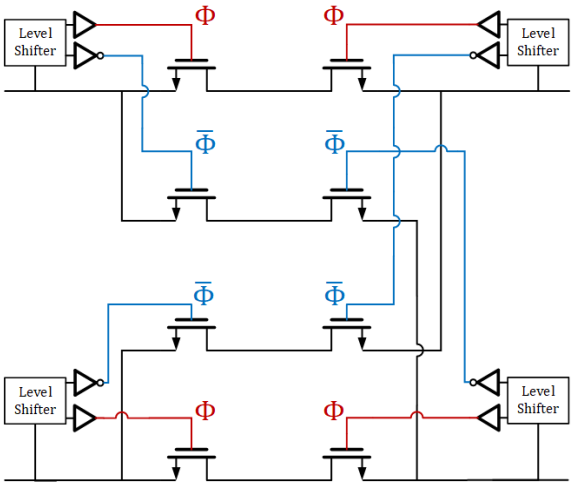

Figure 3.22 : HV chopper using switches from Figure 3.20

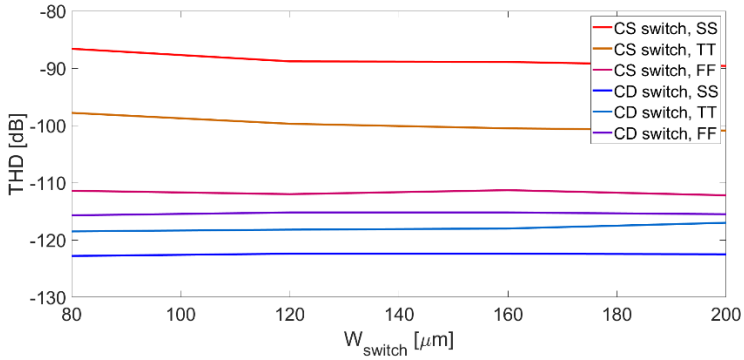

Figure 3.23 : THD vs HV switch width across mos corners at 150^0C

3.6.3 Level-shifter & Driver Design

The main consideration for the level-shifter is to minimize the clock DCE and PWM state dependent asymmetries, which can be done by increasing the level-shifter speed or compensating systematic timing errors that it introduces.

The HV chopper design from [22], which has similar operating conditions as this work, uses a current-controlled switch. However, it consumes high power for fast switching and requires the implementation of 8 level-shifting devices instead of 4 when used with common-drain configured switches, increasing the area requirements. A modification to a cascoded pmos latch level-shifter

[31] is proposed in [32] by adding pulsed current mirrors, increasing the switching speed. However, it is unsuitable for this application as the current mirrors inject a large current into the switch source nodes, degrading the THD when partially injected into the feedback path. The capacitively coupled design in [20] is not suitable for this application, as it cannot handle differential signals larger than the V_{th} of the switch devices. The solution chosen is a modified version of the level-shifter from [16] (Figure 3.24), which is the same as used in the output stage.

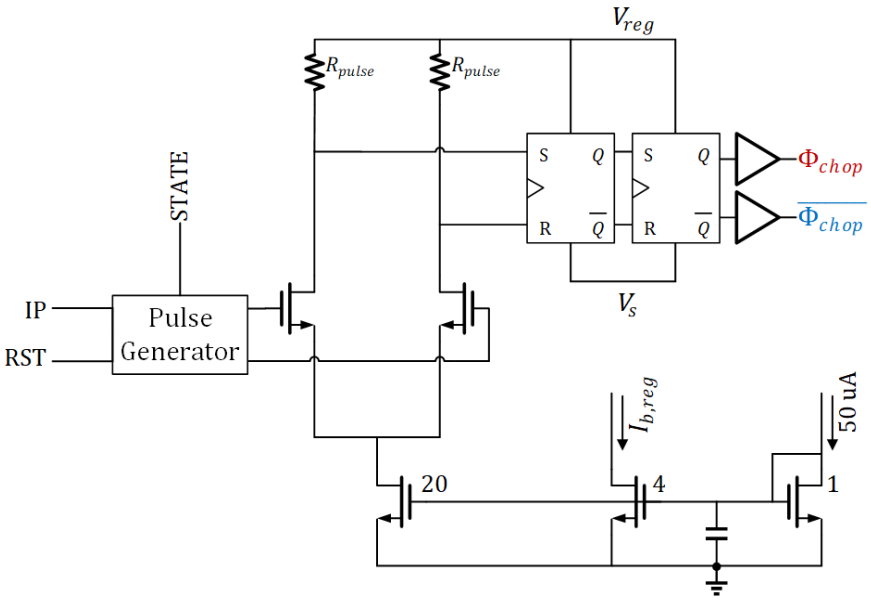

Figure 3.24 : HV chopper level-shifter

Due to the current mirror changing operating regions when $V_s = 0$ V, but remaining in saturation when $V_s = 14.4$ V, the level-shifter introduces delay variations between the two PWM output states. This results in asymmetrical switching, similar to a clock DCE, given that the PWM output is alternatingly chopped at 0 and 14.4 V (Figure 2.2). As Figure 2.10 indicates, by reducing this asymmetry, more chopper clock skew is tolerable to meet the PSRR target. Therefore, a selectable compensation delay is implemented in the pulse generator of each level-shifter. Figure 3.25 shows $\phi_{chop}/\overline{\phi_{chop}}$ of the four level-shifters in the HV chopper with and without the selectable compensation delay. This includes the regulator covered in the following section.

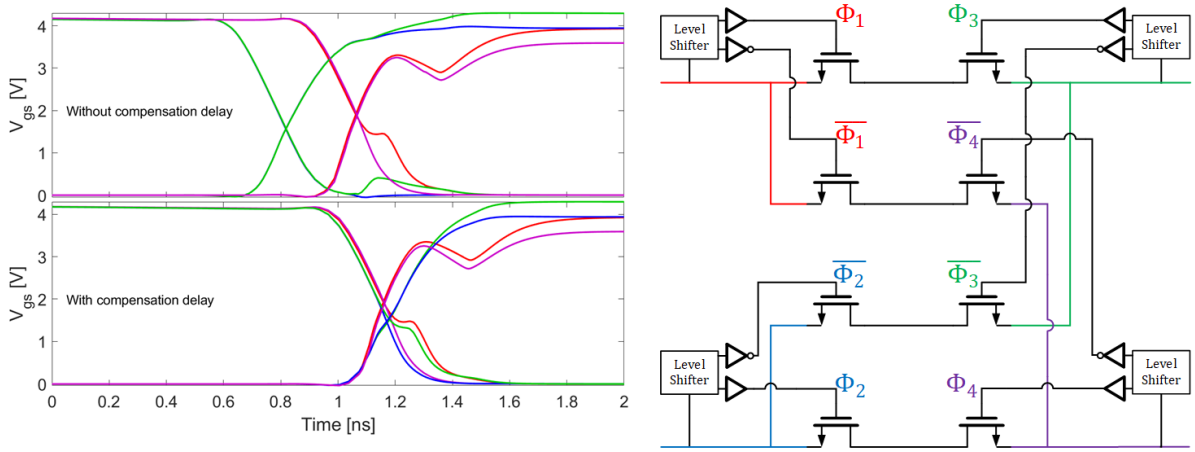

Figure 3.25 : V_{gs} of HV chopper switches with and without a selectable compensation delay

Across PVT, the PWM state dependent level-shifter delay is improved from ~250 – 300 ps to ~50 – 150 ps at a schematic level when using the compensation delay. After layout (with an R+C+CC extraction), the state dependent delay (with compensation) degrades to ~50 – 250 ps due to the decreased speed of the level-shifter and increased supply ripple of the regulator.

3.6.4 Regulator

Because the regulators used for the level-shifters in the output stage [16] contain a significant amount of HV devices, its area would dominate the HV chopper. The output buffer in the design can be scaled down, because the HV chopper switch area is significantly smaller than those in the output stage. However, as the area of the regulator is dominated by the HV barrier layers, the total regulator area remains dominant.

To minimize both the design complexity and amount of HV components in the regulator, a simple source follower [33] is used to generate V_{reg} (Figure 3.24), which is shown in Figure 3.26. Compared to the regulator in [16], a significant area reduction is obtained, shown in Table 3.1.

Table 3.1 : Size comparison of regulator from [16] and this work

From [16]	$290\mu m$ X $180\mu m$ = $52{,}200\mu m^2$
From [16] with min. size output	$220\mu m$ X $160\mu m$ = $35{,}200\mu m^2$
This work	$160\mu m$ X $100\mu m$ = $16{,}000\mu m^2$

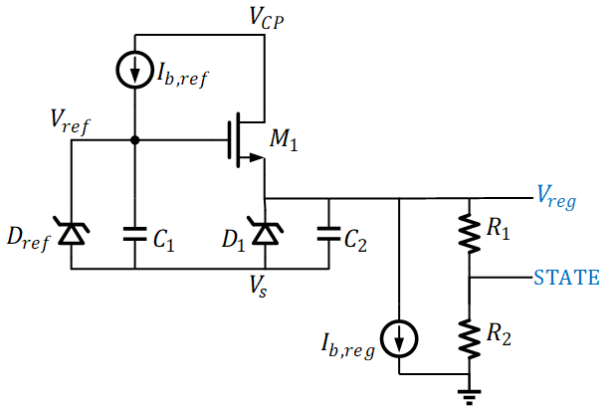

Figure 3.26 : HV chopper regulator

The regulator uses a Zener diode D_{ref} as voltage reference [4], resulting in a $V_{reg} - V_s \approx V_{zener} - V_{th,M1}$. Because V_{zener} and $V_{th,M1}$ fluctuate significantly across PVT, it is important to ensure that $V_{reg} - V_s$ always maintains a sufficiently high voltage to keep the chopper switches on.

The ripple at V_{reg} is induced at V_{ref} due to parasitic coupling from M_1, D_{ref} and the current making $I_{b,ref}$ translating via M_1 to V_{reg}. This is reduced by increasing C_1 and $I_{b,ref}$. Ripple at V_{reg} is also induced at the regulator output due to its finite driving strength. This is reduced by increasing the width of M_1 and by increasing C_2. The ripple at V_{reg} is reduced by scaling M_1, C_2 and C_1 as an area trade-off, such that $V_{reg} - V_s > 3\ V$ during both chopping and PWM switching events in the worst PVT corner. This is shown in Figure 3.27.

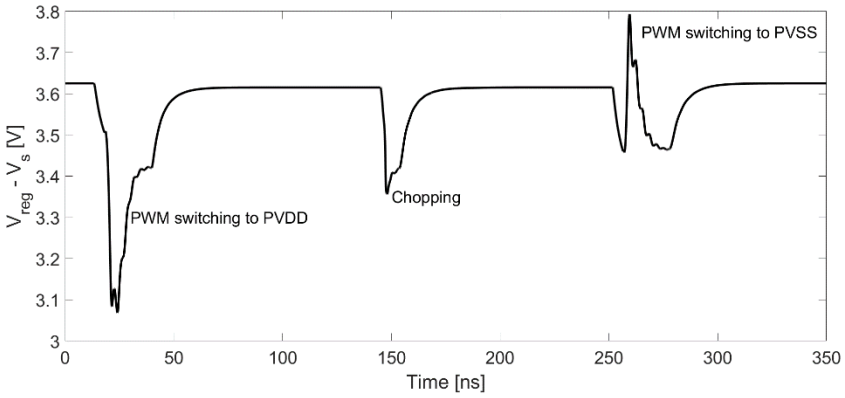

Figure 3.27 : HV chopper regulator $V_{reg} - V_s$

Besides acting as a supply, the regulator also operates as a PWM state sensing device, generating the enable signal "STATE" for the selectable delay in the pulse generator. $R_1/R_2 = 9$, ensuring STATE $\approx AVSS$ when $V_s = 0\ V$ and STATE $\approx AVDD$ when V_s = 14.4 V across PVT. To ensure that the regulator biasing current is dominantly PWM state independent, $I_{b,reg} = 200\ \mu A$ is chosen.

The regulators in the HV choppers are powered from an internal supply V_{CP}, which is made by modifying the output stage to act as a charge pump. Because the AD-PWM modulation scheme causes SWP and SWN to switch complementary (Figure 1.2), this also applies for the boot strapped capacitors $C_{bs,out}$ used to power the high side of the output stage transistors (Figure 1.1) [16]. By connecting diodes from the complementary switching $C_{bs,out}$ to a local buffer capacitor C_{CP}, it can be kept at a voltage $V_{CP} = 2PVDD - 2V_D$. Because $C_{bs,out} \gg C_{CP}$, this does not affect the output stage regulators. Figure 3.28 shows the HV chopper charge pump supply.

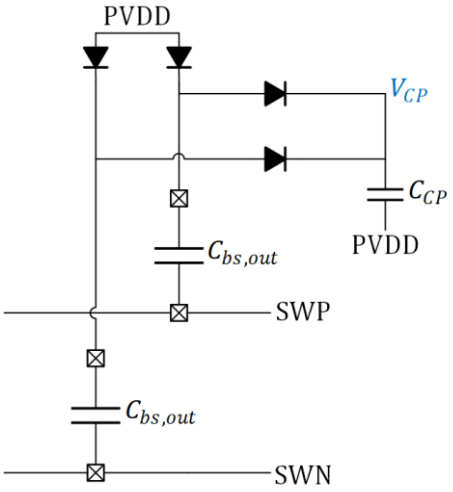

Figure 3.28 : HV chopper charge pump supply

3.6.5 Layout

Figure 3.29 shows the layout of the HV chopper. The clock lines in this layout are routed vertically and the signal lines horizontally to minimize cross-coupling. The signal lines tree-branch out from the centre to the individual switches for matching. C_{CP} is implemented at the top/bottom of the HV chopper to match the distance to each regulator.

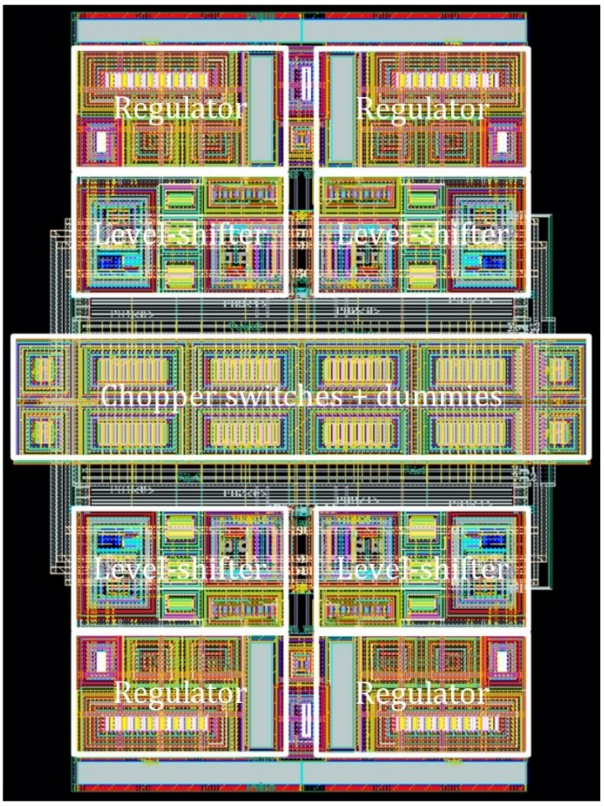

Figure 3.29 : HV chopper layout

3.7 Chopper Clock and Time Matching Circuit Design

3.7.1 Clock Timing Skew Compensation Circuit

The clock timing skew compensation circuit aims to match both the skew of the chopper clocks and chopped analog signals, to average the chopping error current spikes injected in the 1st integrator. Figure 3.30 shows a block diagram with all components in the DEM chopper paths that introduce delays. To compensate the relative mismatches between the DEM choppers, a HV chopper compensation delay and feedback resistor compensation delay are introduced in the LV DEM chopper clock paths. In addition, the fan-out of the VG and input DEM choppers is adjusted to match their delays. Figure 3.31 shows a timing diagram, relating the delays between clock events at the internal oscillator (T_0) and switching events in the current going into the 1st integrator at the VG (T_1). The arrows indicate the delay of each block in Figure 3.30. The times on the x-axis indicate switching events it the output of the blocks. $T_{pwm,comp}$ is for the PWM path compensation delay output, T_{comp} for the comparator, $T_{freq,div}$ for the frequency divider, $T_{HV,fanout}$ for the HV chopper fan-out, $T_{HV,dum}$ for the HV chopper dummy delay, $T_{HV,chop}$ for the HV chopper, T_{logic} for the output stage logic, $T_{R_{fb},dum}$ for the feedback resistor dummy delay, $T_{VG,chop}$ for the VG chopper fan-out and $T_{IN,chop}$ for the input chopper fan-out.

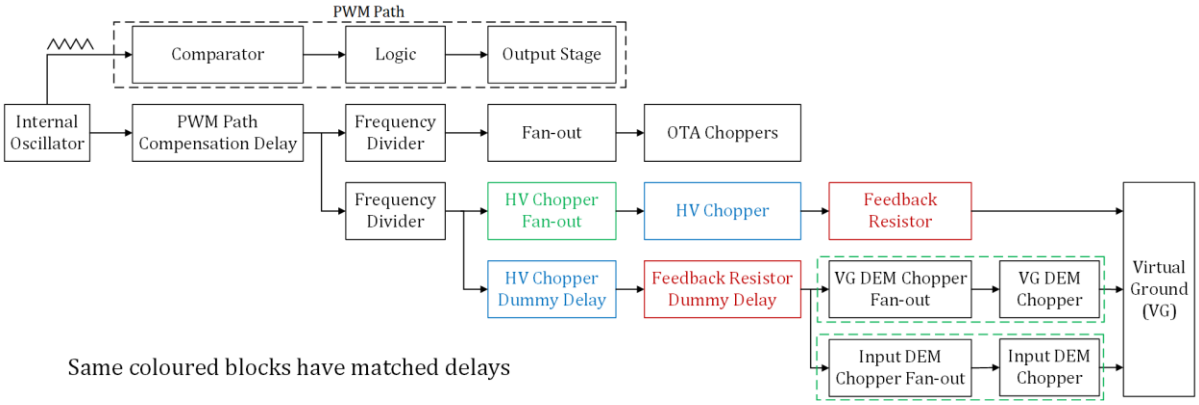

Figure 3.30 : Timing diagram of signal paths from oscillator to virtual ground for choppers

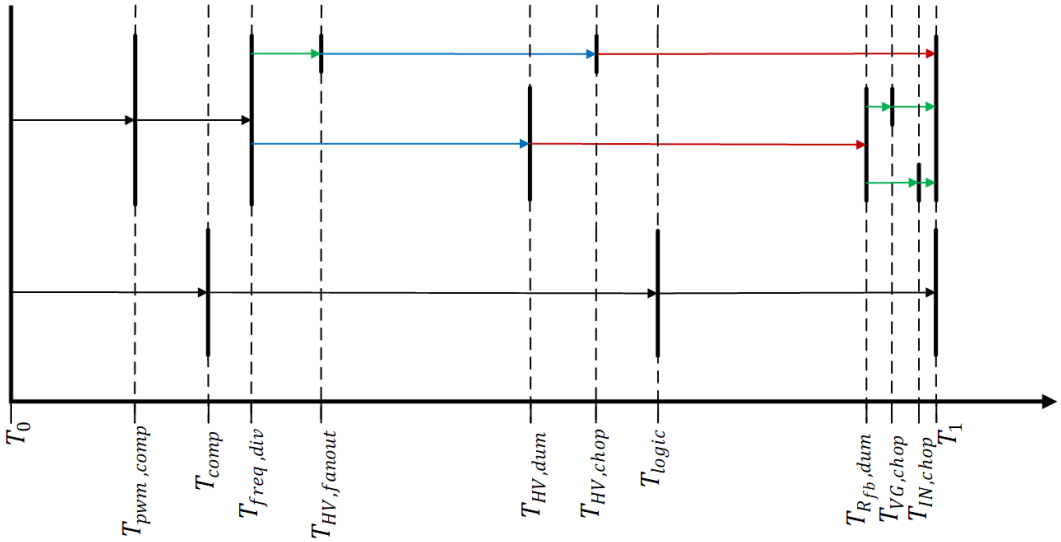

Figure 3.31 : Timing diagram of delays of the blocks shown in Figure 3.30

The timing delays are implemented without the need for process calibration, using dummy delay blocks, aiming to mimic the delays in the DEM clock signal paths. This is shown in Figure 3.32. The delays introduced in the HV chopper are compensated with a dummy level-shifter, driver and regulator, driving a buffer implemented using the same HV NMOS devices as used for the HV chopper switches.

The four HV NMOS devices shown in Figure 3.32, are each given a $W = W_{switch}/2 = 100\mu m$. Because the dummy level-shifter driver drives 2 of these devices at $\phi_{chop}/\overline{\phi_{chop}}$ (Figure 3.24), the fan-out remains the same as in the HV chopper.

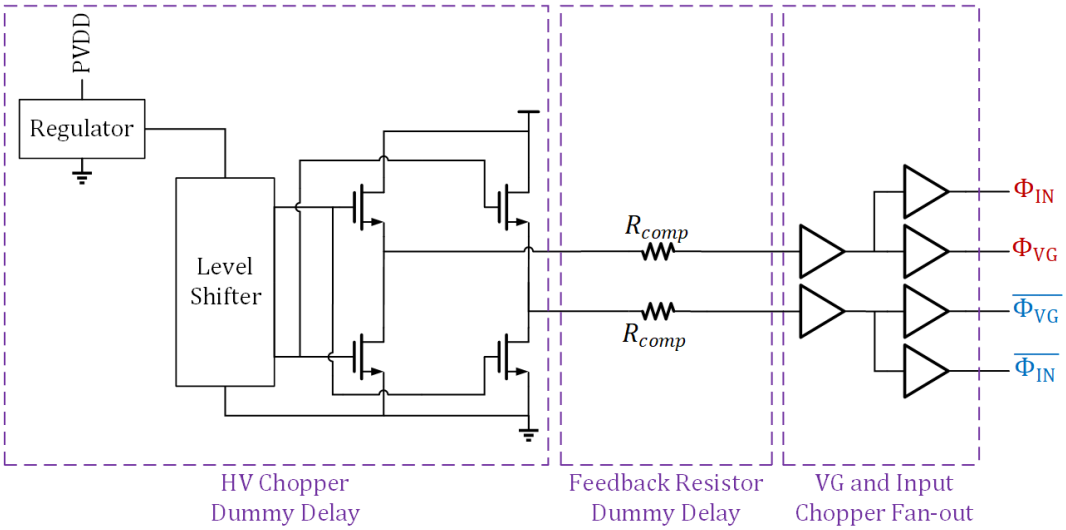

Figure 3.32 : Implementation of HV Chopper Dummy Delay, Feedback Resistor Dummy Delay and VG and Input DEM Chopper Fan-out

3.7.2 Layout

To ensure that the dummy delays accurately match the DEM chopper clock paths post layout, the device structures and routing are also matched in the layout. Figure 3.33 shows the layout of the chopper clock generator with skew compensation and the HV chopper.

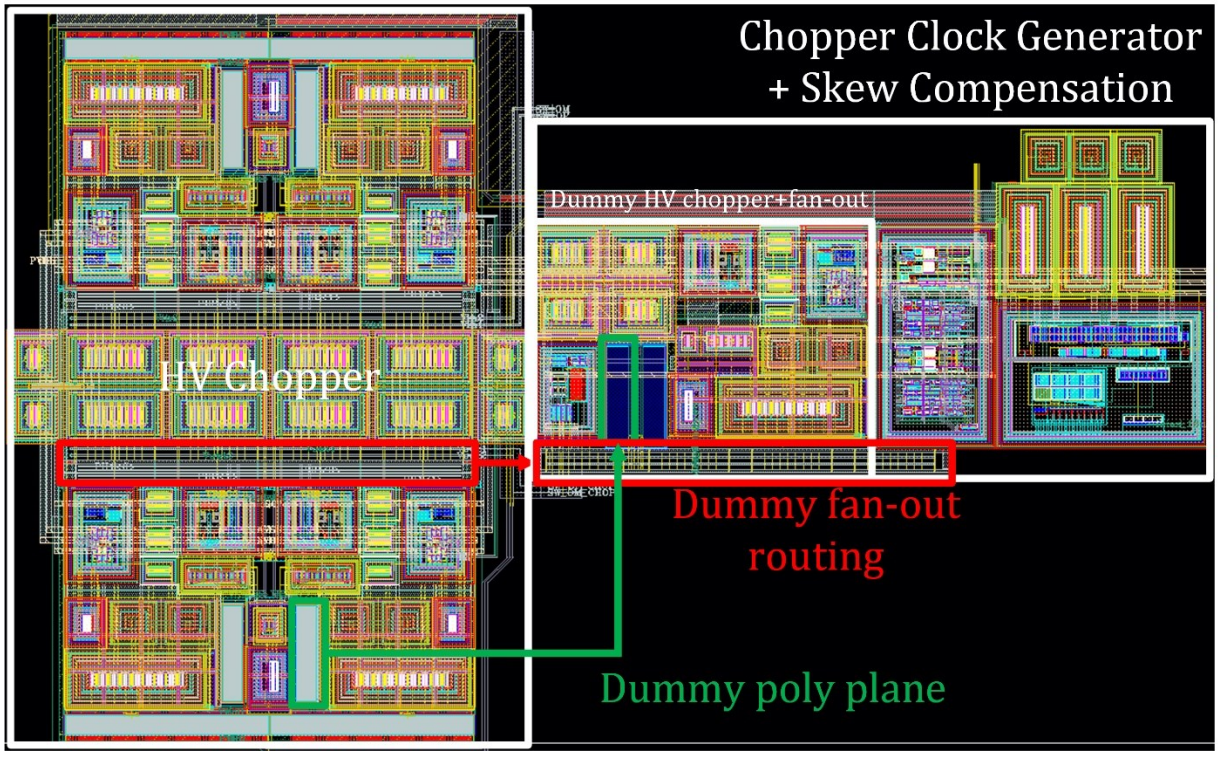

Figure 3.33 : Chopper clock generator with skew compensation and HV chopper

Chapter 4 System-Level Simulation Results

4.1 Simulation Conditions

Unless otherwise noted, all results presented in this chapter were simulated under the following conditions:

- The load resistance is 8Ω
- The output stage power supply PVDD = 14.4V
- The LV power supply AVDD = 1.8V
- In the LC filter (Figure 1.1), $L = 3.3\mu H$ and $C = 1uF$
- $f_{chop,OTA} = f_{chop,DEM} = 100\ kHz$
- Bonding wires are modelled on every pin of the design including a parasitic inductance of $10nH$. The bonding wire model is shown in Figure 4.2.
- An RC snubber is present at the output to mitigate excessive bonding wire ripple. The method described in [34] is used to scale the R and C.
- The design is measured with a parasitic extraction of the post layout top-level (Figure 4.1)

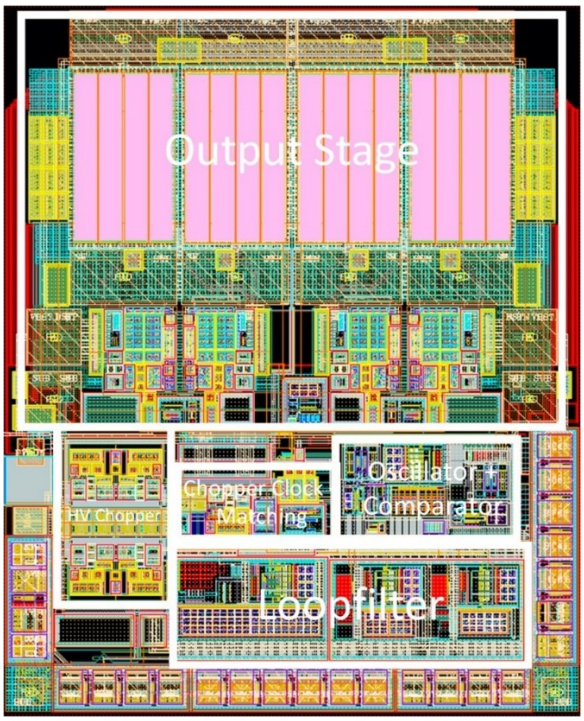

Figure 4.1 : Class-D top-level layout

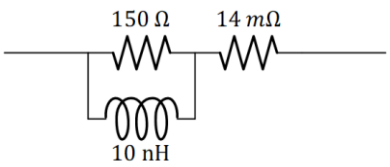

Figure 4.2 : Bonding wire model

4.2 PSRR

4.2.1 Post-layout Extraction Simulations

In order to assess the performance at low and high frequencies, the PSRR is simulated at 5 kHz and 20 kHz. Table 4.1 shows an overview of the results. All audio band noise is added to determine the values shown in the table, to avoid the risk of PWM intermodulation products not being taken into account. The audio band spectrum for the TT corner is shown in Figure 4.3 and Figure 4.4 for a 5 kHz and 20 kHz supply tone respectively.

Table 4.1 : PSRR across process corners simulated at 27^0C with a 1 V_{rms} tone at PVDD

	TT	SS	FF
5 kHz	104.9 dB	106.4 dB	104.6 dB
20 kHz	105.2 dB	105.3 dB	105.8 dB

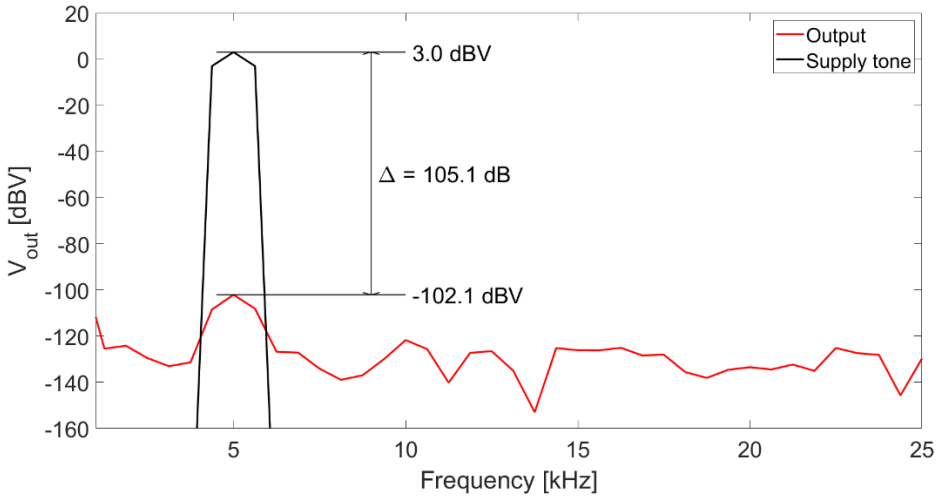

Figure 4.3 : Audio band spectrum of class-D output with a 1 V_{rms} supply tone at 5 kHz applied

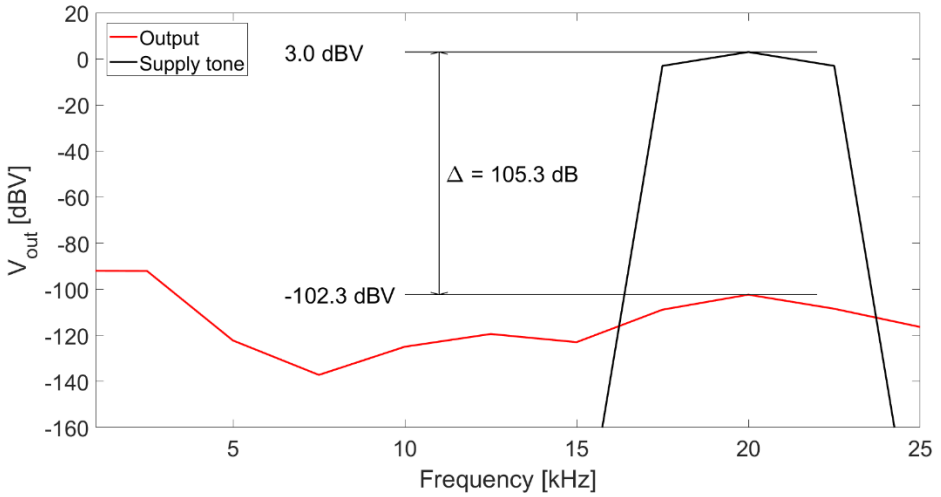

Figure 4.4 : Audio band spectrum of class-D output with a 1 V_{rms} supply tone at 5 kHz applied

4.2.2 Schematic Simulations with Mismatches

The 3σ mismatches of all DEM choppers, R_{fb} and R_{in} are modelled in the design and simulated using a schematic view. The 3σ input-reffered voltage offset at the input of the 1st integrator OTA is also modelled.

The chip is simulated for the nominal operation mode and the test mode where DEM chopping is disabled. It is important to note that the test mode where chopping is disabled contains a bug where the input path to the 2nd and 3rd integrator is disconnected. Therefore, this is not a perfect apples-to-apples comparison. However, as the input is 0 V in this test, there is still considered to be some validity to this comparison. Table 4.2 shows an overview of the results. All audio band noise is added to determine the values shown in the table, to avoid the risk of PWM intermodulation products not being taken into account.

Because R_{in} and R_{fb} are scaled to minimum size, their mismatches also increase notably ($3\sigma_{R_{in}} \approx 150\ \Omega$ and $3\sigma_{R_{fb}} \approx 900\ \Omega$). Therefore, this discrepancy between chopping and not chopping is expected. Figure 4.5 shows a spectrum comparison of the TT corner.

Table 4.2 : PSRR across process corners simulated at 27^0C with a 20 kHz, 1 V_{rms} tone at PVDD

	TT	SS	FF
No Chopping	42.7 dB	44.5 dB	40.4 dB
Chopping	106.1 dB	106.5 dB	103.1 dB

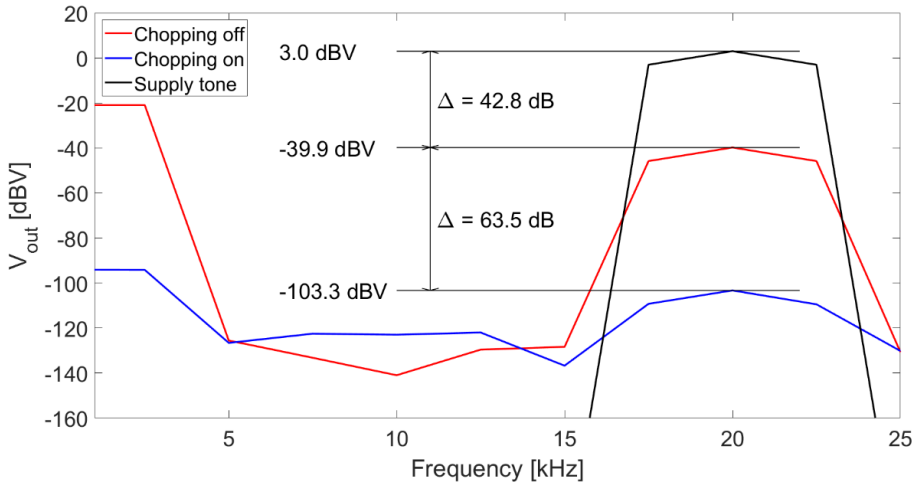

Figure 4.5 : Audio band spectrum of class-D output with a 1 V_{rms} supply tone at 20 kHz applied, w./w.o. chopping

4.3 CMRR

4.3.1 Post-layout Extraction Simulations

In order to assess the performance at low and high frequencies, the CMRR is simulated at 5 kHz and 20 kHz. Table 4.3 shows an overview of the results. All audio band noise is added to determine the values shown in the table, to avoid the risk of PWM intermodulation products not being taken into account. The audio band spectrum for the SS corner is shown in Figure 4.6 and Figure 4.7 for a 5 kHz and 20 kHz supply tone respectively. A_{diff} shown in the figures is the differential amplifier gain.

Table 4.3 : CMRR across process corners simulated at 27^0C with a 100 mV_p input common-mode tone

	TT	SS	FF
5 kHz	107.5 dB	105.8 dB	107.5 dB
20 kHz	102.8 dB	101.6 dB	105.3 dB

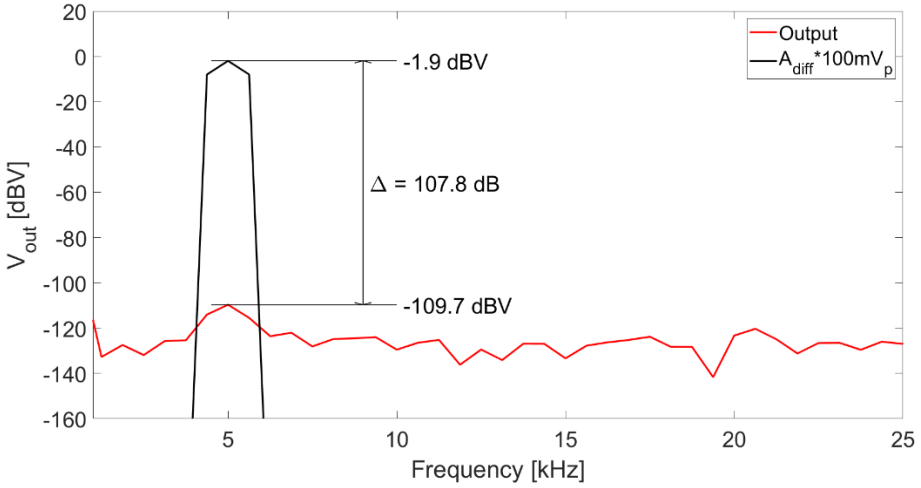

Figure 4.6 : Audio band spectrum of class-D output with a 100 mV_p input CM tone at 5 kHz applied

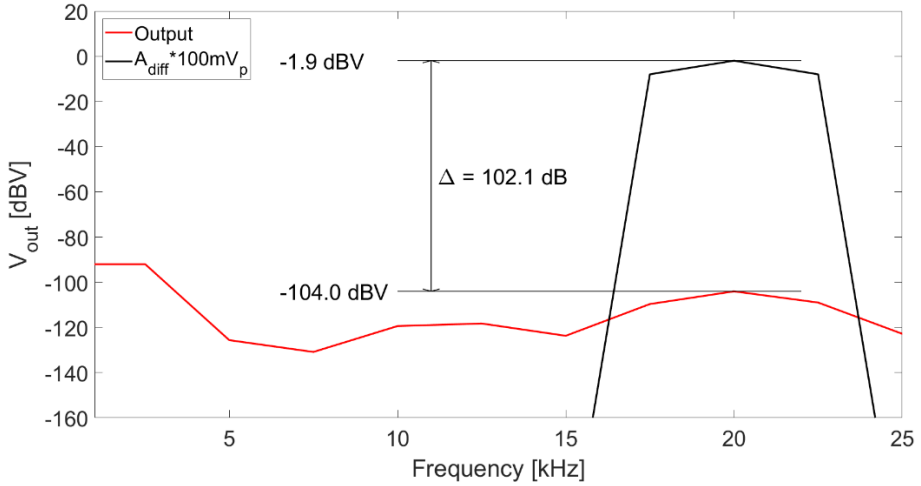

Figure 4.7 : Audio band spectrum of class-D output with a 100 mV_p input CM tone at 20 kHz applied

4.3.2 Schematic Simulations with Mismatches

The same 3σ mismatches are modelled as in the PSRR schematic simulations. The chip is also simulated with the same test modes as done for the PSRR. Table 4.4 shows an overview of the results. All audio band noise is added to determine the values shown in the table, to avoid the risk of PWM intermodulation products not being taken into account. Figure 4.8 shows a spectrum comparison of the FF corner with and without chopping.

Table 4.4 : CMRR across process corners simulated at 27^0C with a 20 kHz, 100 mV_p input common-mode tone

	TT	SS	FF
No Chopping	55.8 dB	57.2 dB	53.6 dB
Chopping	101.2 dB	101.3 dB	100.4 dB

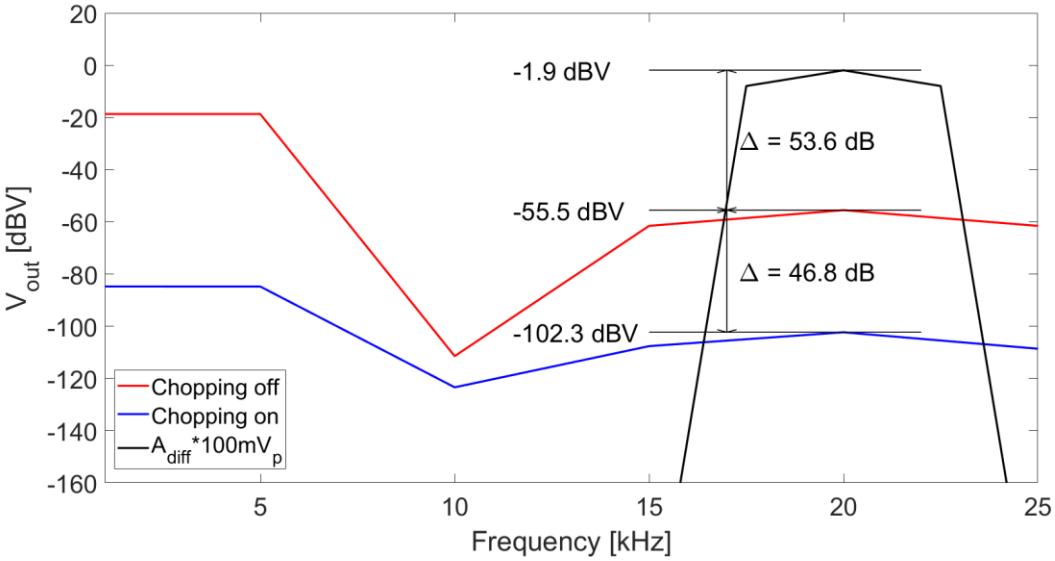

Figure 4.8 : Audio band spectrum of class-D output with a 100 mV_p input CM tone at 20 kHz applied, w./w.o. chopping

4.4 THD

All THD simulations have been done with the bonding wire at AVSS removed, as the amount of ringing observed at high amplitudes is assumed to be less severe after tape-out, due to the presence of multiple AVSS pins on-chip.

Table 4.5 shows the THD at 27^0C with a 5 kHz input tone and 1W output power. Figure 4.9 shows the spectrum of the class-D simulated with a 5 kHz input tone and 1W output power at 27^0C. Figure 4.10 shows the THD versus the input amplitude.

Table 4.5 : THD across process corners simulated at 27^0C with a 5k kHz input and 1W output power

TT	SS	FF
-105.7 dB	-103.9 dB	-102.8 dB

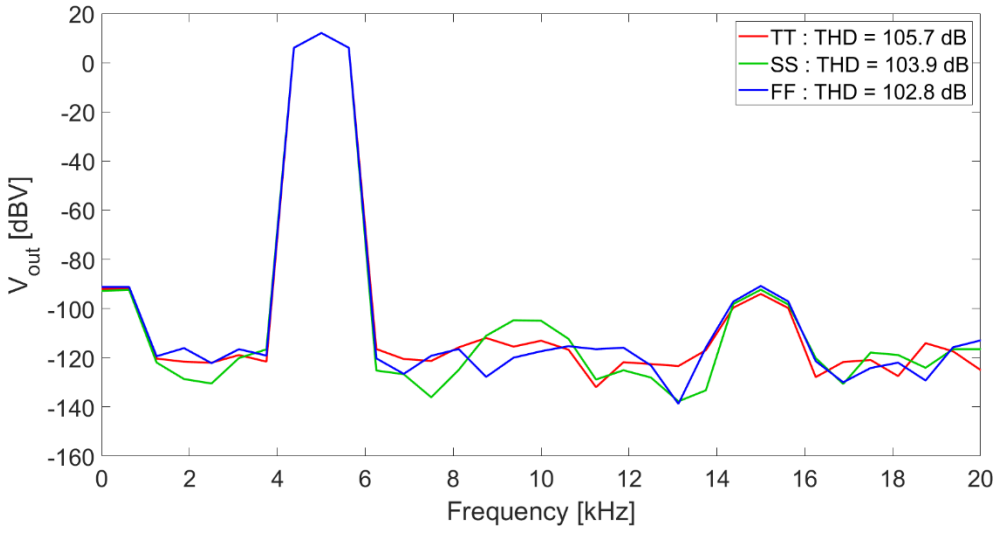

Figure 4.9 : Audio band spectrum of class-D output with a 1 W tone at 5 kHz

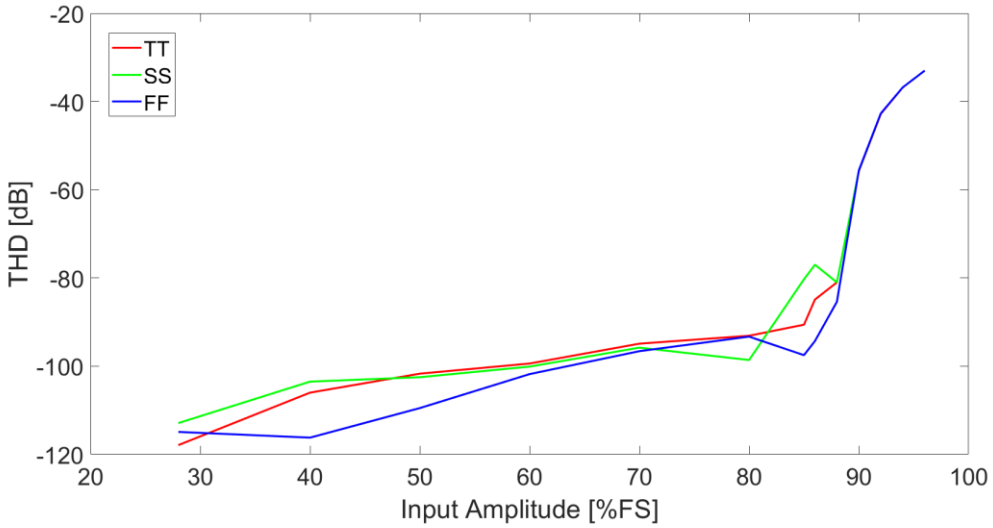

Figure 4.10 : THD versus input amplitude with a 5 kHz input tone, simulated at 150^0C

4.5 Noise

Figure 4.11 shows the noise density from a periodic noise simulation of the class-D (after A-weighting) with the loop filter and choppers implemented in a schematic for the SS corner at 150^0C, as this is the corner where the noise level is the highest. The rest of the amplifier is made ideal to allow for the simulation to converge. When turning the choppers on, a notable improvement is observed in the noise level. The output rms voltage noise is shown in Table 4.6.

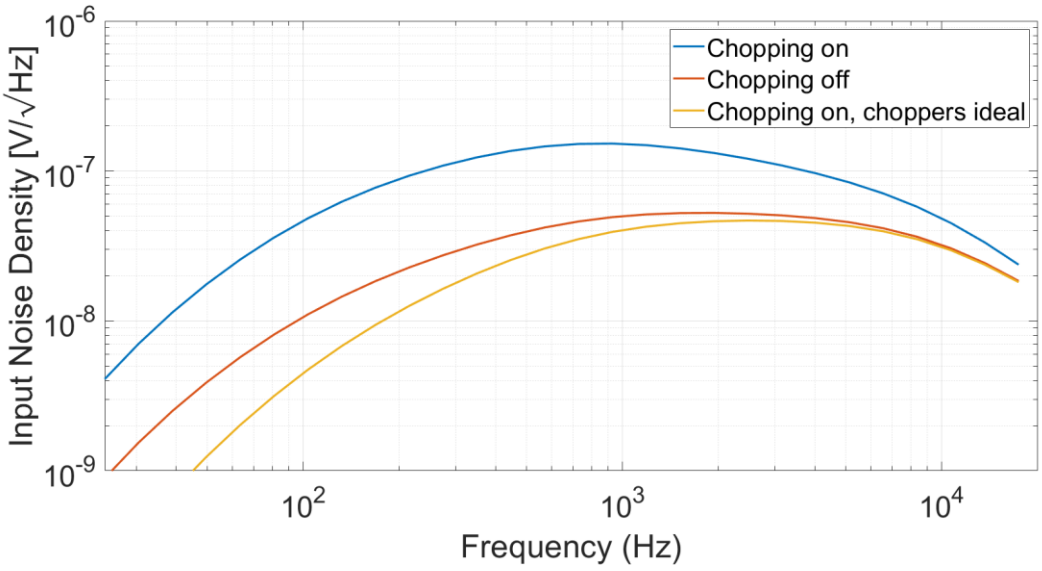

Figure 4.11 : A-weighted input referred noise density w./w.o. chopping and with chopping with ideal choppers (Figure 3.11)

Table 4.6 : Output rms voltage noise in SS corner at 150^0C

Chopping off	Chopping on	Chopping on (ideal choppers)
$84.65\mu V_{rms}$	$41.75\mu V_{rms}$	$38.74\mu V_{rms}$

4.6 PS-IMD

To see the effect of PS-IMD in the audio band, the class-D is simulated across PVT with an input tone at 10 kHz with 1W output and a $1V_{rms}$ tone at 5kHz is applied at PVDD. The tones due to intermodulation in the output stage are expected at 5kHz and 15kHz, which are both in the audio band. Figure 4.12 shows the output spectrum. Table 4.7 details the PS-IMD in the other simulated corners.

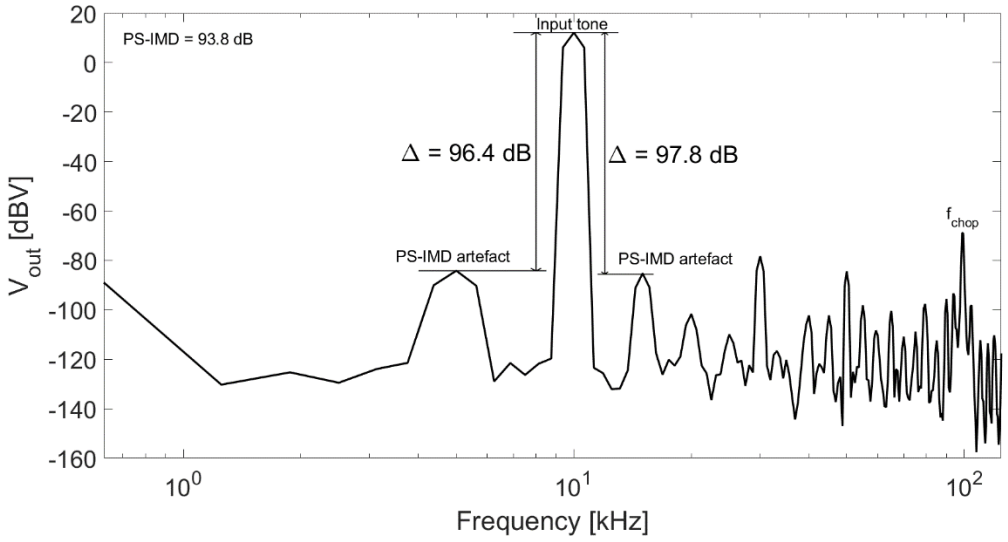

Figure 4.12 : Audio band spectrum of class-D output with a 1W output, 10 kHz input tone and $1V_{rms}$ 5 kHz supply tone, simulated at 150^0C

Table 4.7 : PS-IMD across PVT with a 5kHz, 1 V_{rms} tone at PVDD and a 10 kHz input tone with 1W output power

	TT	SS	FF
27^0C	-96.7 dB	-95.7 dB	-96.1 dB
150^0C	-93.8 dB	-94.3 dB	-93.3 dB

4.7 Idle Power and Power Efficiency

Because a snubber is used in all other simulations, the idle power is also measured with the snubber present. However, this does make the results less competitive. Because idle power is not the main focus of this work, this is not considered an issue.

Depending on the bonding wire inductance at PVDD and PVSS for the packaged chip, the snubbers might not be necessary, in which case this specification can be improved. Table 4.8 details the simulated quiescent current across PVT from AVDD and PVDD. Table 4.9 shows the idle power and Table 4.10 shows the simulated power efficiency.

Table 4.8 : quiescent current I_{AVDD} and I_{PVDD} across PVT

	TT	SS	FF
27^0C	$I_{AVDD} = 4.59\ mA$ $I_{PVDD} = 27.10\ mA$	$I_{AVDD} = 4.09\ mA$ $I_{PVDD} = 24.86\ mA$	$I_{AVDD} = 5.23\ mA$ $I_{PVDD} = 29.61\ mA$
150^0C	$I_{AVDD} = 4.75\ mA$ $I_{PVDD} = 24.73\ mA$	$I_{AVDD} = 4.20\ mA$ $I_{PVDD} = 22.89\ mA$	$I_{AVDD} = 5.44\ mA$ $I_{PVDD} = 27.19\ mA$

Table 4.9 : Idle power across PVT

	TT	SS	FF
27^0C	$398.5\ mW$	$365.3\ mW$	$435.8\ mW$
150^0C	$364.7\ mW$	$337.2\ mW$	$401.3\ mW$

Table 4.10 : Power efficiency simulated at 150^0C with a 10% THD output

TT	SS	FF
91.55%	90.92%	92.57%

Chapter 5 Conclusions and Future Work

5.1 Conclusions

A chopped PWM based class-D audio amplifier has been designed, based on a previous work [16] for applications that require a high PSRR and CMRR. Although this is a HV design originally intended for automotive applications, the techniques proposed in this work are applicable for any class-D design.

DEM is proposed by means of chopping the input- and feedback- resistors R_{in} and R_{fb} in the 1st integrator of the loop filter in the class-D amplifier. Limiting factors for the PSRR and CMRR are the size of the DEM chopper switches in the input and feedback path. To mitigate common-mode PWM artefacts from demodulating into the audio band, it is found that an odd f_{pwm}/f_{chop} is required. In addition, DEM chopping spikes are balanced by means of DEM chopper clock skew compensation.

To chop R_{fb}, a HV chopper design is proposed that can handle a large signal swing. Its PWM state dependent mismatches are compensated by means of a selectable compensation delay in the choppers' level-shifters. The complementary nature of the AD-PWM modulation scheme is used to have the class-D output stage operate as a charge pump to power the HV chopper.

Post-layout simulations indicate that this design meets the main targeted specifications of >100 dB PSRR and CMRR across the audio band, improving on prior art by >20 dB. Therefore, this project is considered a success.

Table 5.1 : Target Specifications

	This Work*	[2]	[3]	[5]	[7]	[16]	[17]	[18]
Supply (PVDD) [V]	**14.4**	3~5.5	14.4/25	3.6	8 - 20	14.4	14.4	14.4
f_{pwm} [kHz]	**2100**	650	500	400	400	4200	2000	2100
f_{LC} [kHz]	**88**	-	~40	-	-	580	100	88
Load [Ω]	**8**	4 / 8	4	4 / 8	8	4 / 8	4	4
Idle Power [mW]	**399**	-	-	-	-	94	-	-
Quiescent Current [mA]	**29.6**	1.45	12	3	20.52	7	17	~40
Output Power [W]	**13**	3.1	80	0.8	20	14 / 28	28	27
Efficiency (10%THD)	**90.9%**	89.5% / 92.4%	>90%	93%	90%	91% / 87%	91%	86%
Output Noise (A-weighted) [μV_{rms}]	**<41.75**	12	34	16	20.5	-	31	42
DR (A-weighted) [dB]	**107.7**	-	118	-	115.5	111.2	110.6	-
Peak THD+N	**0.0011%**	0.00067%	0.004%	~0.003	0.0013%	0.0007% /0.0004%	0.00078%	~0.015%
PSRR (20-20k Hz) [dB]	**>103**	118 - <80	88 - 60	101 - <77	80 - 50	-	70 - 62	~75 - 57
CMRR (20-20k Hz) [dB]	**>100**	-	-	-	-	-	-	-

5.2 Future Work

Although this work has presented a significant improvement in PSRR versus prior art, there are multiple potential improvements possible.

- In Chapter 2 it is stated that R_{fb} and R_{in} are given a minimum width to improve the THD at high amplitudes. However, THD simulations in Chapter 4 show that the THD degrades rapidly at high amplitudes anyway. As non-linearity in R_{in} degrades the THD as it is sized down, possibly there is a better optimum for this resistor scaling than its minimum size.

- In Chapter 3 it is stated that the transmission gate chopper is given a width of $18\mu m$. This was chosen at an early design stage, as this seemingly resulted in an optimal THD. However, simulation results presented in this work indicate that a better optimum is possible with a higher width. For future work, it can be worth re-verifying.

- The bootstrapped T-switches were chosen for the input DEM chopper as a precaution against abundant bonding wire ripple. It could be worthwhile to investigate in future works if an improvement is also observable after tape-out. For instance, by implementing duplicate input paths, allowing for the choppers to be swapped.

- It is stated in Chapter 3 that a better THD is observed for a switch CD configuration than a CS configuration. Due to time constraints when this was found (and because a CD configuration was already chosen anyway), the cause was not investigated. However, it could be valuable to know what effect is causing the discrepancy. Therefore, it is recommended that this is investigated in future works.

- In Chapter 3, the design of the internal voltage source for the HV chopper is covered. As discussed, it uses the class-D output stage as a charge pump, avoiding the need to implement one in addition. However, it causes issues if a clipping event occurs that remains for a significant amount of time.

  During a clipping event, the charge stored in one of the output stage bootstrapped capacitors is used to power the HV chopper, without being replenished, causing the output stage to eventually stop working temporarily.

  The capacitors are scaled large enough, such that all measurements of interest can be made. For a commercial application where this cannot be tolerated, a clipping detection circuit could be a good improvement. This would allow for the HV chopper to be turned off while clipping, such that it does not drain the output stage bootstrapped capacitor.

- As mentioned in Chapter 4, there is a bug in the test mode where the DEM choppers are turned off. It causes the input path to be disconnected from the 2nd and 3rd integrator in the loop filter. This severely limits the comparison options for this test chip and should be resolved in a following work.

Appendix

6.1 Budget derivation of DEM Choppers R_{on} Mismatches

The PSRR and CMRR can be approximated as $G_{fb}/G_{err,fb}$ (for PSRR) or $G_{in}/G_{err,in}$ (for CMRR). G_{in} is the gain from the input voltage to the current going into the 1^{st} integrator. G_{fb} is the gain from the output voltage to the current going into the 1^{st} integrator. G_{err} is the gain of the input common-mode voltage ($G_{err,in}$ for CMRR) or power supply voltage ($G_{err,fb}$ for PSRR) to the current going into the 1^{st} integrator. Approximating the gain of the 1^{st} integrator OTA as infinite, the differential error current I_{err} going into the 1^{st} integrator is linearly approximated as

$$I_{err} = \frac{V_{cm,in} - V_{cm}}{R_{in1}} - \frac{V_{cm,in} - V_{cm}}{R_{in2}} + \frac{V_{ps} - V_{cm}}{2R_{fb1}} - \frac{V_{ps} - V_{cm}}{2R_{fb2}} \quad (6)$$

Where $V_{cm,in}$ is the common-mode voltage at the input of the class-D and V_{ps} is the power supply voltage of the output stage of the class-D. Here the linear approximation is made that the output common-mode is $V_{ps}/2$. R_{in1} and R_{in2} are the input resistors and R_{fb1} and R_{fb2} are the feedback resistors connecting to the 1^{st} integrator of the loop filter. V_{cm} is the common-mode voltage at the virtual ground. This is approximated as follows:

$$V_{cm} \approx \frac{R_{fb1}V_{cm,in}}{2(R_{in1} + R_{fb1})} + \frac{R_{fb2}V_{cm,in}}{2(R_{in2} + R_{fb2})} + \frac{R_{in1}V_{ps}}{4(R_{in1} + R_{fb1})} + \frac{R_{in2}V_{ps}}{4(R_{in2} + R_{fb2})} \quad (7)$$

Substituting equation (7) into equation (6), $G_{err,in}$ and $G_{err,fb}$ can be derived by taking the partial derivative of I_{err} to $V_{cm,in}$ or V_{ps} respectively. G_{in} and G_{fb} are approximated as the following:

$$G_{in} \approx \frac{R_{in1} + R_{in2}}{2R_{in1}R_{in2}} \quad (8)$$

$$G_{fb} \approx \frac{R_{fb1} + R_{fb2}}{2R_{fb1}R_{fb2}} \quad (9)$$

From this, the PSRR and CMRR are approximated:

$$PSRR = \frac{R_{fb1} + R_{fb2}}{\frac{R_{fb1}R_{fb2}(R_{in1} - R_{in2})}{2R_{in2}(R_{in1} + R_{fb1})} + \frac{R_{fb1}R_{fb2}(R_{in1} - R_{in2})}{2R_{in1}(R_{in2} + R_{fb2})} + (R_{fb2} - R_{fb1})(1 - \frac{R_{in1}}{4(R_{in1} + R_{fb1})} - \frac{R_{in2}}{4(R_{in2} + R_{fb2})}} \quad (10)$$

$$CMRR = \frac{R_{in1} + R_{in2}}{\frac{R_{in1}R_{in2}(R_{fb1} - R_{fb2})}{2R_{fb2}(R_{in1} + R_{fb1})} + \frac{R_{in1}R_{in2}(R_{fb1} - R_{fb2})}{2R_{fb1}(R_{in2} + R_{fb2})} + 2(R_{in2} - R_{in1})(1 - \frac{R_{fb1}}{2(R_{in1} + R_{fb1})} - \frac{R_{fb2}}{2(R_{in2} + R_{fb2})}} \quad (11)$$

Although R_{in1}, R_{in2}, R_{fb1}, R_{fb2} are random variables, they are approximated by a deterministic resistor with a value equal to the mean of the mentioned random variables and a random variable with a zero mean and equal distribution to the mentioned random variables. Furthermore, the assumption is made that the absolute value of the random variable is much smaller than the deterministic resistor value and that the random variables are independent from each other. As such, the random variables are approximated as

- $R_{in1} \approx R + \Delta R_{in1}$
- $R_{in2} \approx R + \Delta R_{in2}$
- $R_{fb1} \approx 8R + \Delta R_{fb1}$

- $R_{fb2} \approx 8R + \Delta R_{fb2}$

with $R = 20\ k\Omega$. With this, equation (10) and (11) can be simplified to the following:

$$PSRR \approx \frac{8R}{\frac{32}{9}(\Delta R_{in1} - \Delta R_{in2}) + \frac{17}{36}(\Delta R_{fb2} - \Delta R_{fb1})} \quad (12)$$

$$CMRR \approx \frac{R}{\frac{1}{9}(\Delta R_{in1} - \Delta R_{in2}) + \frac{1}{144}(\Delta R_{fb2} - \Delta R_{fb1})} \quad (13)$$

If the PSRR and CMRR is treated as a random variable, the mean and variance are I'll defined as both are ∞. However, 1/PSRR and 1/CMRR have a well-defined mean and variance. As such, the PSRR (with the same applying for the CMRR) can be approximated as $1/(x\sigma(1/PSRR))$, with x the amount of standard deviations tolerated.

With the relation between input and feedback path mismatches defined, the mismatches in on-resistance between chopper switches have to be translated to the input. In the same way as the previous derivation, the on-resistance of the chopper switches is treated as a deterministic R_{on} and a random variable ΔR_{on} representing the deviation in on-resistance. A chopper consists of 4 switches of which 2 are active during each phase [20]. Treating the ΔR_{on} of these 4 switches as random variables which are independent and with an equal variance, the equivalent $\Delta R_{on,in1/2}$ is the average of two ΔR_{on} resistors. The standard deviation $\sigma_{\Delta R_{on,in1/2}}$ is now computed as follows:

$$\sigma_{\Delta R_{on,in1/2}} = \sqrt{\frac{2\sigma^2_{\Delta R_{on}}}{2^2}} = \frac{\sigma_{\Delta R_{on}}}{\sqrt{2}} \quad (14)$$

This equivalent standard deviation can be now applied to equation (13) and (14) to compute the PSRR and CMRR given xσ mismatches.

6.2 Analysis for Choosing f_{chop} Considering PSRR

The signal content at the output of the class-D amplifier consists of a PWM signal [35] modulated with the power supply [14, 15]. This is because the PWM signal in essence acts a switch control signal for the output stage switches. When chopping this signal twice, in essence the signal is modulated with a square wave function (at f_{chop}) twice. As such, the current going into the 1^{st} integrator can be approximated as follows:

$$I_{int1} = PS(f) * PWM(f) * \sum_{k=0,2,4,\dots}^{\infty} A(k)\delta\left(f \pm k f_{chop}\right) \quad (15)$$

A(k) is a frequency dependent magnitude function, $PWM(f)$ is a PWM signal and $PS(f)$ is the output stage power supply signal content. Given the bound from equation (1), the resulting signal going into the 1^{st} integrator of the loop filter with a zero-input condition can also be approximated as

$$I_{int1} = \sum_{n=1,3,5,\ldots}^{\infty} \sum_{k=0,2,4,\ldots}^{\infty} A(n,k)\delta\left(f \pm \left(k \pm a_{chop}n\right)f_{chop} \pm f_{ps}\right) \quad (16)$$

Where A(n,k) is a frequency dependent magnitude function, a_{chop} is the ratio between f_{pwm} and f_{chop} and f_{ps} is the frequency of a power supply tone present (assuming that it's only one tone). Equation (16) shows that if a_{chop} is chosen even, that power supply dependent information can be demodulated into the audio band. However, if a_{chop} is chosen odd, the power supply dependent information remains modulated at the chopping frequency.

6.3 DEM Chopper Switch Sample Mean and Standard Deviation

The sample mean and standard deviation are of the DEM choppers are found from a 1000 sample Monte Carlo simulation at 150^0C. For the simulation of the feedback DEM chopper, a different HV switch is used than in the design, due to the lack of a mismatch model. The standard deviation from the Monte Carlo simulation is scaled with the root of the ratio between the switch lengths.

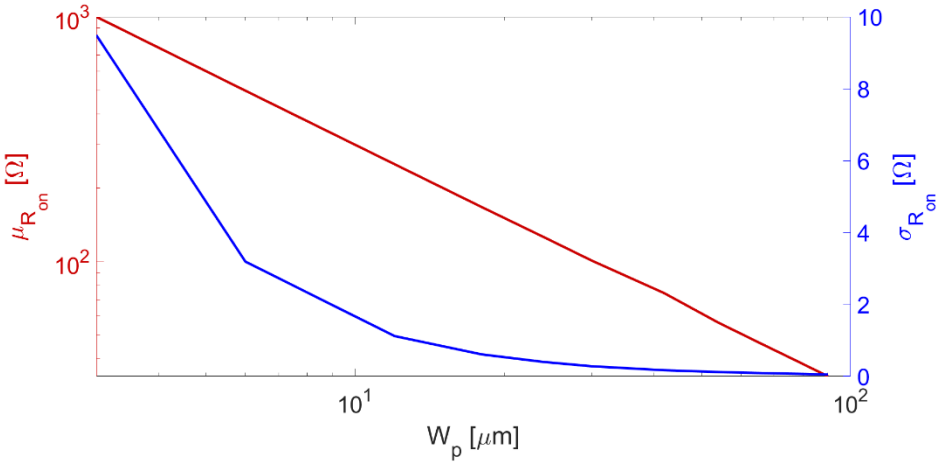

Figure 6.1 : $\sigma_{R_{on}}$ vs switch width at 150^0C of DEM chopper at the 1^{st} integrator virtual ground

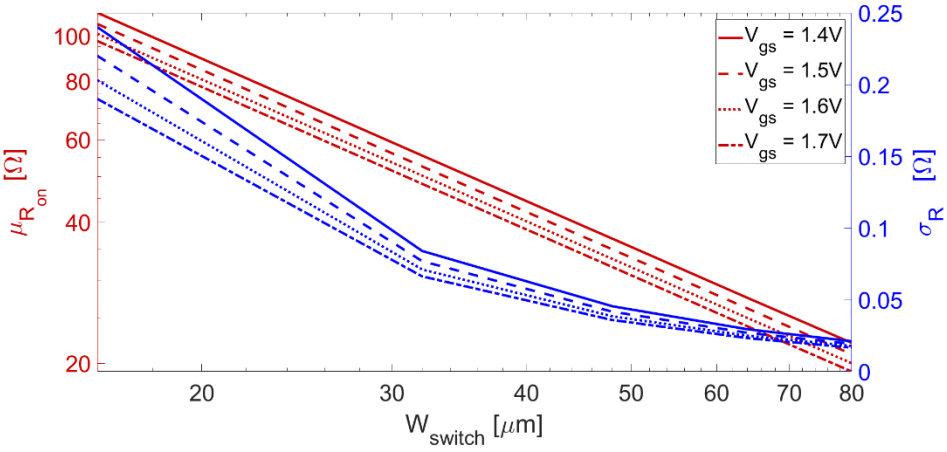

Figure 6.2 : $\sigma_{R_{on}}$ vs switch width at 150^0C of DEM chopper at the class-D input

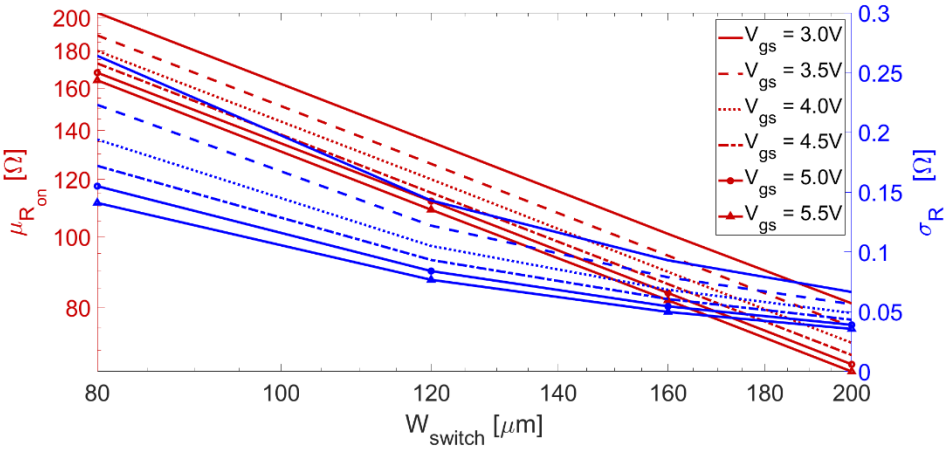

Figure 6.3 : $\sigma_{R_{on}}$ vs switch width at 150^0C of DEM chopper at the class-D output

6.4 Simplified Equation of I_{int1}

$$I_{int1} = PWM(f) * \sum_{k=0,2,4,\dots}^{\infty} A(k)\delta\left(f \pm kf_{chop,DEM}\right) * \sum_{n=0,2,4,\dots}^{\infty} A(n)\delta\left(f \pm nf_{chop,OTA}\right) \quad (17)$$

Combining the two sum functions in Equation (17) results in Equation (18).

$$I_{int1} = PWM(f) * \sum_{k=0,2,4,\dots}^{\infty} \sum_{n=0,2,4,\dots}^{\infty} A(n,k)\delta\left(f \pm nf_{chop,OTA} \pm kf_{chop,DEM}\right) \quad (18)$$

6.5 HV Chopper Biasing

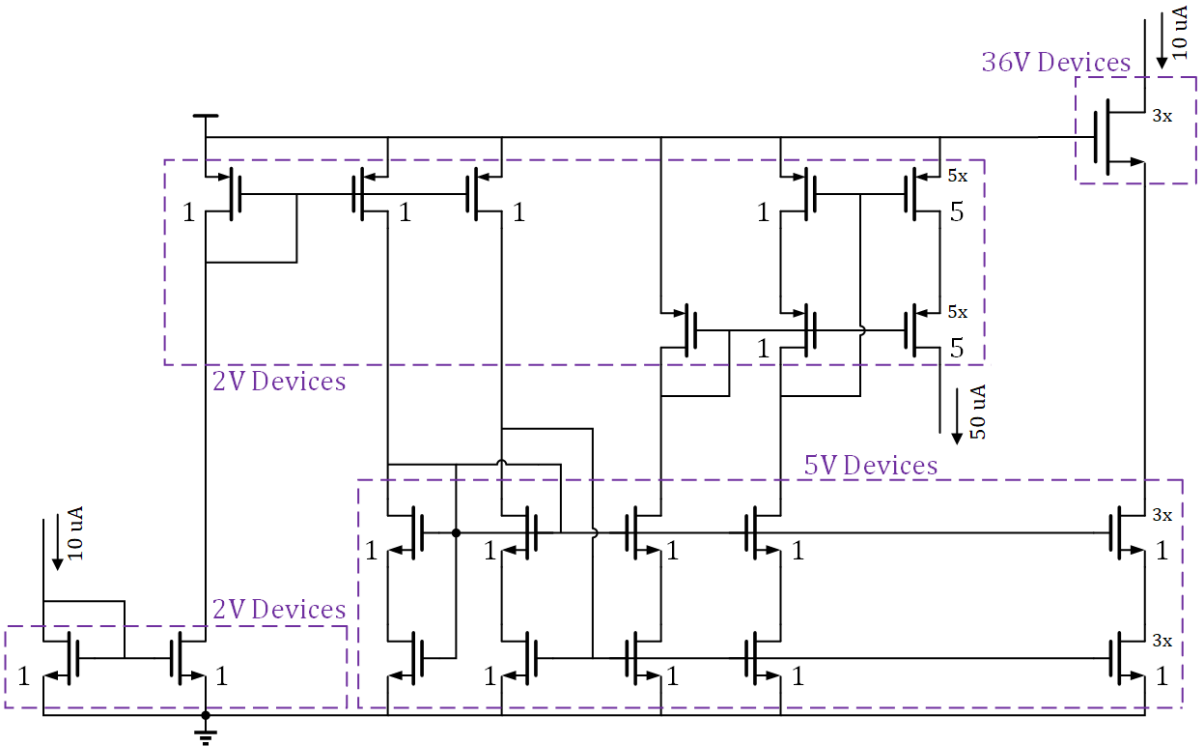

Figure 6.4 : Biasing block for HV chopper and HV chopper dummy delay

6.6 Chopper Clock Generator and Timing

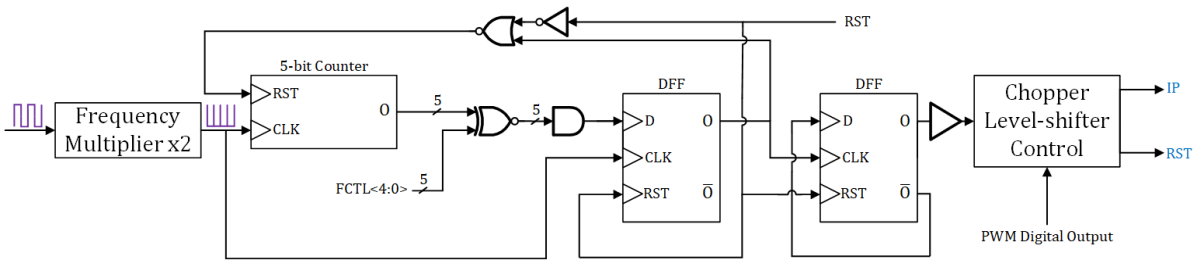

Figure 6.5 : Frequency divider for DEM choppers

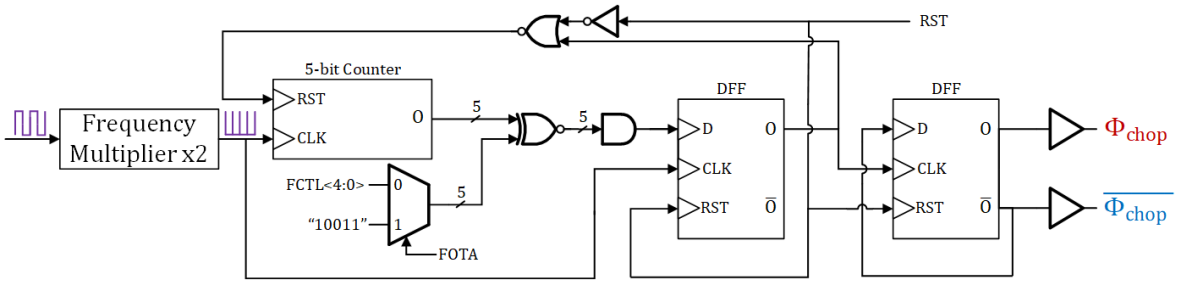

Figure 6.6 : Frequency divider for OTA choppers

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